國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

探討高閘極介電層N通道金氧半電晶體的
新穎閘極電流隨機電報量測法

The Observation of Gate Current Instability in High-k Gate Dielectric MOSFET by a New Gate Current Random Telegraph Noise Approach

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中華民國 九十七 年 七 月

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摘要

為了符合低功率的要求，閘極高介電材質的使用隨著閘級氧化層的微縮越來越有取代二氧化矽的趨勢。除了可以得到一樣的等效氧化層厚度之外，還可以明顯降低閘極漏電流超過三個數量級。但是高介電材質閘極有許多的可靠度問題，主要是來自於高介電閘極層中有許多缺陷抓取電荷，因此在實際電路操作時，會產生臨界電壓，汲極電流等的不穩定。

本論文中，將使用一個新的方法，稱作「閘極電流隨機電報訊號」方法來分析高介電材料閘極層中電荷抓取及放出的現象。透過給一固定的閘極電壓觀察閘極電流，閘極直接穿隧電流會在多個層次間振動，其原因來自於電荷在穿越閘極層時，會掉進閘極層裡面的缺陷並被抓住，但又容易藉著熱從缺陷中散逸。當電荷被抓取時會降低閘極穿隧電流，放出後電流又恢復，透過統計抓取及放出的時間，可以得到缺陷的特性，另外藉由觀察電流振幅了解在電路上的影響。

我們運用此方法來觀察三種不同的缺陷，包括製程產生的缺陷、元件經過不同電壓破壞之後產生的缺陷以及介電層在軟崩潰之後的影響。由此方法觀察到的閘極電流不穩定性可判斷出閘極介電層的劣化程度，不同程度的破壞會使電荷抓取及放出的機制受到影響。另外藉由改變溫度量測，可以更有效的了解此現象並且得知元件的可靠度。

The Observation of Gate Current Instability in High-k Gate Dielectric MOSFET by a New Gate Current Random Telegraph Noise Approach

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ABSTRACT

In order to meet the requirement for low power circuit application, high-k gate dielectrics are being implemented in Si CMOS technologies with aggressive oxide thickness scaling. For the same EOT practical high-k gate dielectrics, one can provide significant reductions (>10^3) in the gate leakage. Reliability characteristics will be one of the primary goals of future development work, in which a large amount of traps in high-k bulk layer demonstrates the trapping and detrapping phenomena of carries. It causes the instability of threshold voltage, drain current, etc.

In this thesis, a newly method, Gate Current Random Telegraph Noise, will be utilized to analyze the phenomenon of carriers trapping/detrapping in high-k gate dielectrics. We observe gate current by biasing the gate at fixed voltage and gate direct tunneling current will show two or three levels. The cause is carriers trapping in the trap site during tunneling through gate dielectrics and detrapping by thermal emission. Gate current is suppressed when traps capture carriers and recovers as traps empty. By statistically extracting capture and emission time, we can understand the

trap properties. Besides, the influence will be understood by observing the variation of current fluctuation.

We then apply this method to study three types of traps, including process induced traps, stress induced traps at distinct stress voltages, and post soft-breakdown character. Through the observation of gate current instability the degradation of gate dielectrics can be recognized. The experiment result shows the capture/emission mechanism affected by degrees of degradation. On the other hand, the appearance of gate current random telegraph noise is effectively investigated by measuring at different temperatures and the reliability of devices can be well understood.

誌　謝

兩年的實驗室生活是精采豐富的，但同時也充滿艱辛與汗水。首先要感謝的是我的指導教授：莊紹勳博士，老師給予的生活上與專業上的指導與建議，讓我在學業上與研究上獲益良多並學習到對事物應有的嚴謹態度以及處理方法。除此之外，對於課業外的生活技能、觀念的督促，讓我必須在此表達感謝之意。

感謝已畢業的亞峻、元亨、耀賢及大正學長當我在實驗遇到瓶頸和挫折時，總是能耐心指導，並給予支持與鼓勵。也感謝在兩年研究生涯中，與我一起嚐遍酸甜苦辣的同學，包括小郭、友良、文彥與易叡，我們一起經歷困苦的研究過程，相信數年後再聚首，一定倍感溫馨。另外我要特別感謝汪老師研究群的小馬學長，此研究論文唯有他無私的教導才能順利完成。對於汪老師研究群的同學，即使我們身在不同的研究群，但我們的感情就像是一家人一樣，希望以後在業界相遇時還能保有我們現在的真誠，也祝福大正、元亨、小馬、達達、阿豆肯與阿雄學長能夠順利取得博士學位，此外也感謝振鵬、米華、健宏、安舜與專題生禎晏，感謝有你們這群學弟妹平日對於實驗室的付出，使學長們能夠專心於研究上，在此，輕遞一份真摯的祝福，希望明年亦能看見你們順順利利的畢業。

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謹將這份榮耀獻給培養我多年的父母親

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Chapter 1
Introduction

1.1 Background

The physical limitations of the conventional silicon dioxide as gate dielectric reached the point where films physical thickness of 15A, the gate leakage current exceeds the specifications ($1A/cm^2$). To face this critical problem, high-k dielectrics have been introduced as hafnium based, zirconium, aluminum oxides. In fact, while keeping the EOT constant high-k dielectrics allow us to increase the physical thickness of the gate stack. Hence, the gate leakage can be reduced by 2 to 3 orders of magnitude. Although a large amount of effort that has been paid on the study of high-k gate dielectrics, many of critical problems still unknown. These problems include defects in the material which can lead to undesired transport through the dielectrics gate band structure induces polarity effects on the leakage and reliability. All of these stack properties lead to an anomalous behavior with respect to the conventional SiO_2.

In aforementioned studies, several reliability issues for high-k gate dielectrics have been indentified: threshold voltage instability [1.1], stress induced film degradation [1.2], and dielectric breakdown [1.3]. Threshold voltage instability is due to the dynamics of carriers charging/discharging in pre-existing high-k bulk defects and negative bias temperature instability (NBTI) in pMOSFETs and positive bias temperature instability (PBTI) in nMOSFETs is the critical bottleneck of high-k gate dielectrics.

1.2 The Motivation of this Work

In recent years, approach in high-k abound with plenty of traps has been studied mostly by transient related methods [1.4][1.5]. Both they are used to look into the interface and near-interface property but the accuracy is challenged if only gate dielectric is heavily destroyed. Although charge pumping method is most reliable to profile the trap density in-depth of gate dielectric stack, some traps do not surely respond to trap/detrap carriers on fixed time (T=1/f) and these kind of traps would be absent using charge pumping method. Conventional I-V and C-V methods are less dependable for high-k dielectric, and hence pulse I-V measurement system is needed just only to precisely identify the characteristic high-k dielectrics MOSFETs. Nevertheless, it costs a lot for purchasing the instruments.

In this thesis, we propose a new method called “Gate Current Random Telegraph Noise (IG RTN)” which is developed to analyze quality and reliability of high-k dielectric MOSFETs. In this approach, the noise from pulse generator could be neglected and it also diminishes AC stress possibility that would destruct devices by charge pumping method. By I_G RTN method, it is easy to understand how single electron affects gate current through existing DC instrument.

1.3 Organization of the Thesis

Large amount of process induced traps exist in high-k dielectric bulk material as mentioned in many papers. We organize I_G RTN method and utilize it to detect existing traps in high-k MOSFETs in detail in Chapter 1. Proposed in Chapter 3 is method to profile stress induced traps behavior. For stress induced drain current positive bias temperature instability (PBTI) in high-k nMOSFETs, we apply Fowler-Nordhiem stress at constant voltage without elevating temperature and produce traps which cause apparent 2-levels of gate current noise. Chapter 4 discusses the characteristic and gate current fluctuation after soft breakdown. Finally in Chapter 5, the results of this thesis and suggestions for future works are summarized.

Chapter 2
Random Telegraph Signal of Gate Current for Process Induced Traps in High-k MOSFETs

2.1 Experimental

2.1.1 Preface

Conventionally, BTI characterization is carried out by periodically interrupting stress to measure electrical parameters, introducing a switching delay between stress and measurement which may give rise to an imprecise or even incorrect result. Recently, a two frequency charge pumping measurement has been utilized to characterize high-k trap properties [2.1][2.2]. First, the charge-pumping current may be too small to be reliably measured in small-size devices at a lower frequency required to probe into the high-k layer. Second, due to the mixture of interface and high-k bulk traps, the two-frequency Charge-pumping method may not be viable when the high-k trap density is comparable to or even less than the interface trap density. Third, charge-pumping current may contain gate leakage as devices are stressed or heavily destroyed even wear out or soft breakdown happen.

In this chapter, a newly developed characterization technique named “Gate Current Random Telegraph Noise” for exploration of high-k and interfacial layer trap properties by measuring the gate current in small-area devices is presented. Single electron capture and emission could be observed. The physic of gate current instability is interpreted in Section 3.2. Based on the temperature and voltage dependence of single charge effect, an analytical model for tunneling mechanism is developed and traps parameters are extracted.

2.1.2 Device Preparation and Previous Work

The devices used in this work are nMOSFETs with a poly-silicon electrode, and a bi-layered gate dielectric stack consisting of HfSiO and an interfacial SiO_xN_y layer. EOT of stacked dielectrics is 12A. The gate width is 0.12μm~10μm, and the gate length range from 0.09μm~1μm. The complete procedure is shown in Fig. 2.1. The devices are first subjected to I_D-V_G and I_G-V_G measurement, and then "detrap" at low negative gate voltage (V_G= -1V, 10s). I_D-V_G is used to check out normal I-V characteristic of devices and then we chose similar gate dielectric properties to compare that have most the same I_G-V_G. To avoid pre-existing electrons trapped in the dielectric affect gate current instability, a "detrap" step is utilized before I_G RTN.

2.1.3 I_G RTN measurement system

The measurement setup of I_G RTN is shown in Fig. 2.2, Fig. 2.3. Gate current is about 10pA ~1nA, three orders of magnitude or more smaller than drain current and hence probe station leakage path is more needed to be calibrated well. It is suggested to have parameter analyzer connecting to probe station directly without passing through switch equipment. On the other hand, large fluctuation may happen as probe needles don't contact with the pad of wafer well, especially for body contact. The sampling rate is maximum 10^3 readings per second, that it means there is minimum 1ms of resolution. RTN phenomenon may be not observed as interval time set too larger due to capture or emission time less than the interval time. RTN happens only during local gate voltage so it's better to detect varying tight gate voltage step as sampling. Otherwise, area of devices also affects I_G RTN articulation; generally it could be seen more clearly as area of devices going down but magnitude of gate current decreases relatively. So it is a trade-off to gain evidence of I_G RTN.

2.1.4 Statistics

The target of RTN measurement is to extract mean capture and emission time and then further profiles traps properties. Therefore, the switch of trap captures and emits electrons must be distinguished. We can determine using naked eye and it is also the most precise method to obtain mean capture and emission time. Nevertheless, it wastes time and not efficient for large amount of data. In our work, we write a program and used a current level that lies in the middle of the high and low current state to differentiate trap holding or releasing an electron automatically. Sequentially, every period of time was added and divided by numbers of events. Consequently, we extracted mean capture and emission time more accurately and can handle much larger amount of data also.

2.2 Cause of 2-Levels Gate Current Fluctuation

2.2.1 Factor of Fluctuation

It is obvious that gate current is more responsible to electrons capture and emission in a trap site than drain/source current in Fig. 2.4. The amplitude, capture and emission time are the critical parameters of random telegraph noise phenomenon and they depend on the trap properties, such as trap depth into dielectrics, trap energy apart from conduction band (valance band if holes are captured and emitted) and magnitude of gate leakage current. Besides, retention of traps holding an electron and how much time an empty trap can capture an electron are also influenced by the electric field distributed among dielectrics and temperature that would involve in the probability of electrons hopping over activation energy mentioned in Chapter 2.

2.2.2 Direct Tunneling Model

Although high-k dielectrics have smaller effective oxide thickness than conventional insulator, SiO_2, their physical thickness is still large over 50A. Therefore, the gate leakage current is considered as

direct tunneling current from the substrate to the gate through a trapezoid energy barrier as gate bias is around V_G=1.2V. Fowler-Nordhiem tunneling current exists as gate bias larger than 1.8V. In our RTN measurement, all used gate voltages for sampling are below 1.5V and large amount of gate current are direct tunneling current.

Gate current becomes smaller as an electron captured in the trap site in Fig. 2.5. The cause is electron trapped will screen the proximity of the trap and hence suppress the local direct tunneling current. It seems like a big stone laying in the flow of river so the flow rate is apparently rolling off. It is believed that the screen area is small compared with gate area and we know that trap induced direct tunneling current varied locally but not globally.

2.3 Process Induced Traps

2.3.1 Gate Current Waveform

In the following, we start to apply this method to analyze process induced traps behavior. It could not be seen absolutely in every device, and sometimes it is available to observe I_G RTN phenomenon; nevertheless analysis afterward is hard to process for some reasons, such as undistinguishable amplitude, multi-levels gate current states. Here below we show two valuable I_G RTN measurement results for process induced traps here and discuss the traps properties in later sections.

First one (PIT1) is measured at T=25℃ shown in Fig. 2.6. Traps start to capture electron as gate bias over 0.9V and then emission. As gate voltage increases, capture events happen more frequently. The events happen twice during 10 seconds at V_G= 0.9V and over 40 times at V_G= 1.1V. The other one (PIT2) is shown in Fig. 2.7. Same trend happens with PIT1 as gate voltage varied but on different gate voltage, V_G= 0.9V ~1.2V.

2.3.2 Capture and Emission Time

Fig. 2.8 shows the mean capture and emission time gathered statistics from Fig. 2.6 and Fig. 2.7. Capture time is affected by gate voltage and emission time keeps constant, i.e., the capture time relates to the electric field on dielectrics and electrons stride over barrier to trap sites by tunneling. On the other hand, emission time has no response to electric field and electrons escape does not go through tunneling possibly. Further study will be shown in Section 3.4. Electron occupation factor, f_t defined below is shown in Fig. 2.8 [2.3]. RTN is undetectable since the trap is always empty in weak inversion regime (i.e., V_G< 0.9V). f_t increases linearly in strong inversion regime since 40% at V_G= 1V to 80% at V_G= 1.15V for PIT1, and saturates as gate voltage going up abidingly. f_t of PIT2 also increases linearly since 10% at V_G=0.95V to 75% at V_G=1.1V but not saturates yet. Electron occupation factor is

$$f_t = \frac{\tau_e}{\tau_c + \tau_e} \tag{2.1}$$

Which is dominated by emission time that is too larger than capture time as we know from Eq. (2.1). Hence, the saturation happens when electron occupation factor is near the maximum “1”. This result is in accordance with the equilibrium case that *ft* (=1/(1+exp(E_T-E_F)/*kT*) increases as the trap energy becomes more negative with respect to the Fermi level.

2.4 Result and Discussion

Based on the Shockley–Read–Hall statistics [2.4], the carrier capture rate $1/\tau_c$ can be written in terms of the carrier density (per unit volume) n in the channel, the average velocity of the carriers v, and the average capture cross-section σ as Eq. (2.2), where

$$\tau_c = \frac{1}{nv\sigma} \tag{2.2}$$

$$\sigma = \sigma_0 \exp\left(-\frac{\Delta E_B}{kT}\right) \tag{2.3}$$

the capture cross section is Eq. (2.3). Here σ_0 is the cross-section prefactor, and ΔE_B is the thermal activation energy for capture. T and v are usually taken to be the equilibrium lattice temperature and average thermal velocity v_{th}. This approximation is invalid at large lateral electric field, and electron heating occurs and affects the electron capture time. Emission time is given as Eq. (2.4) [2.5], g is the

$$\tau_e = \frac{\exp\left[\left(E_F - E_T\right)/k_B T\right]}{g\sigma v n} \tag{2.4}$$

degeneracy factor. The term (E_F-E_T) represents the trap energy with respect to the Fermi energy. k_B are the Boltzmann's constant.

2.4.1 Trap Energy

From the principle of detailed balance, one can write the ratio of the mean emission time τ_e to mean capture time τ_c as below. In nMOSFETs, as the gate bias is increased, the trap occupancy should increase,

$$\frac{\tau_c}{\tau_e} = g\exp\left(\frac{E_T - E_F}{kT}\right) \tag{2.5}$$

$$E_{Tn} - E_{T0} = kT\left[\left(\ln\frac{\tau_c}{\tau_e}\right)_n - \left(\ln\frac{\tau_c}{\tau_e}\right)_0\right] \tag{2.6}$$

and, τ_c/τ_e consequently show a decrease. The change in the mark-space ratio of the switching signal with respect to gate voltage indicates which transition corresponds to capture and which transition corresponds to emission of an electron. E_{T0} is reference trap energy at specific gate bias V_{G0}, such as V_{G0}= 1.025V for PIT1, and E_{Tn} is trap energy at relative gate bias V_{Gn} as represented in Eq. (2.6). From plot of E_{Tn}-E_{T0} versus V_G, relationship of trap energy variation to electric field is understood in Fig.

2.10. The variation is more obvious in PIT2 than in PIT2, and $\Delta E_T/\Delta V_G$ is about 20meV/0.1V for PIT1 and 50meV/0.1V for PIT2. It seems that these two traps distribute in different position of dielectrics and hence gate voltage produces distinct field change. Basically, trap sitting near poly-gate has larger variation as field changed in the same dielectric. From the measurement result, we may conclude that PIT1 is near the substrate and PIT2 is close to poly-gate but it s not the truth proven in the next section. The emission time constant is shown below [2.6], where N_C is the effective conduction band densities of state.

$$\tau_e = \frac{\exp\left(\left(E_{Cd} - E_T\right)/kT\right)}{\sigma v N_C} \tag{2.7}$$

E_{Cd}-E_T is trap energy difference apart from conduction band of dielectric. The emission time constants τ_e depends on the energy E_T and the capture cross-section σ. The electron thermal velocity and effective density of states in the conduction band are shown in Eq. (2.8), Eq.(2.9), allowing the emission time constant to be written as Eq. (2.10), where γ is a coefficient. A plot of $\ln(\tau_e T^2)$ versus $1/kT$ has s slope of (E_{Cd}-E_T) and an intercept on the $\ln(\tau_e T^2)$ axis of $\ln(1/\gamma\sigma)$.

$$v = \sqrt{\frac{3kT}{m_n}} \tag{2.8}$$

$$N_C = 2\left(\frac{2\pi m_n kT}{h^2}\right)^{3/2} \tag{2.9}$$

$$\tau_e T^2 = \frac{\exp\left(\left(\mathrm{E_{Cd}} - \mathrm{E_T}\right)/kT\right)}{\gamma\sigma} \tag{2.10}$$

In our experiment shown in Fig. 2.10-2.11, E_{Cd}-E_T is about 1.02eV and 1.06eV for PIT1 and PIT2 respectively. It can be seen that there is only a slight variation in E_{Cd}-E_T as the gate voltage is increasing. These values set the trap around the conduction band edge when compared to φ_0=3.1eV [2.7] [2.8], the difference between the electron affinities of Si and IL, consistent with an acceptor trap acting as a repulsive center for electrons in the channel.

2.4.2 Trap Depth

By the principle of detailed balance, a relationship between the mean capture and emission times and trap parameters is found as Eq. 2.11 [2.9], where E_{Cd}, E_C, E_F, φ_0 and ψ_s are defined in Fig. 2.13(a).

$$\ln\left(\frac{\tau_c}{\tau_e}\right) = -\frac{1}{kT}\left[\left(E_{Cd} - E_T\right) - \left(E_C - E_F\right) - \varphi_0 + q\psi_S + q\frac{Z_T}{EOT}\left(V_G - V_{FB} - \psi_S\right)\right] \tag{2.11}$$

$$\frac{d\ln\left(\frac{\tau_c}{\tau_e}\right)}{dV_G} = -\frac{q}{kT}\frac{Z_T}{EOT} \tag{2.12}$$

EOT is the effective oxide thickness and V_{FB} is the flat-band voltage. We can estimate Z_T, effective depth from the substrate, from measurements of τ_c/τ_e by varying V_G. Z_T is 5.7A for PIT1and 3.8A for PIT2 shown in Fig. 2.14. It means PIT1 sites into the gate dielectrics is deeper than PIT2 that is obviously contradictory to the assumption in Section 3.4.1. Hence, we could predict PIT1 and PIT2 lying in different type of dielectrics, that PIT1 is in high-k bulk layer and PIT2 is in the interfacial or transition layer. From the prediction, the measurement in Fig. 2.10 is reasonable because electric field variation in high-k bulk layer is small due to large permittivity. To extract reliable effective trap depth, the measurement is repeated in different temperature and result is shown in Fig. 2.15. They result in the same slope and Z_T is extracted to same values as varying temperature.

2.4.3 Activation Energy

The capture and emission of an electron in the conduction band by a defect at the Si–IL interface can be explained utilizing a nonradiative multiphonon emission process. It is believed that the nonradiative multiphonon emission occurs due to the crossing of free electronic states with bound electronic states when sufficiently large lattice displacements exist. Before capturing an electron, the defect center will experience thermal vibrations around an equilibrium position close to the upper level

of the energy gap. After this capture, the defect would relocate at a new equilibrium position in the energy gap with shifted coordinates, creating violent lattice vibration at the defect. This instability subsides by damping down the vibration to the thermal vibration amplitude and emitting phonons. At lower temperatures, this relaxation takes longer time, effectively slowing down the switching events. This thermally activated behavior can be understood in terms of a configuration coordinate diagram of the trap (see Fig. 2.13(b)). An empty trap can be thermally excited to the crossover point B, where it can capture and electron from the silicon conduction band. The occupied trap then relaxes to its lowest stable level and dissipates the excess energy by multiphonon emission. The energy needed for emitting an electron is usually higher than that needed for capturing one [2.10]. The activation energies depend on the trap energy level relative to the silicon conduction band, and therefore, on band bending. Varying the gate voltage will affect the activation energies. This effect is larger in deep traps (larger Z_T). The plot of characteristic time to $1/kT$ is shown in Fig. 2.16-2.17. Firstly we see τ_c and τ_e increasing intensely as temperature going down. For the capture time, electron thermal energy increases in the channel. Larger temperature enhances electrons hopping over activation energy barrier of capture $E_{a,capture}$, same as emission, electrons held in trap have larger possibility to escape over activation energy barrier of emission $E_{a,emission}$. Secondly both $E_{a,emission}$ and $E_{a,emission}$ are lower with gate bias. $E_{a,capture}$ is proven lower than $E_{a,emission}$ here and decreases intensely as gate bias raising slightly, $E_{a,capture}$ varies around 0.38eV~0.61eV, as a result that gate bias would influence activation energy to capture of channel carriers. As illustrated in Fig. 2.18, time constant to tunnel from traps to poly-gate or back to substrate is much longer the time to Frankle-Poole emission.

Procedure

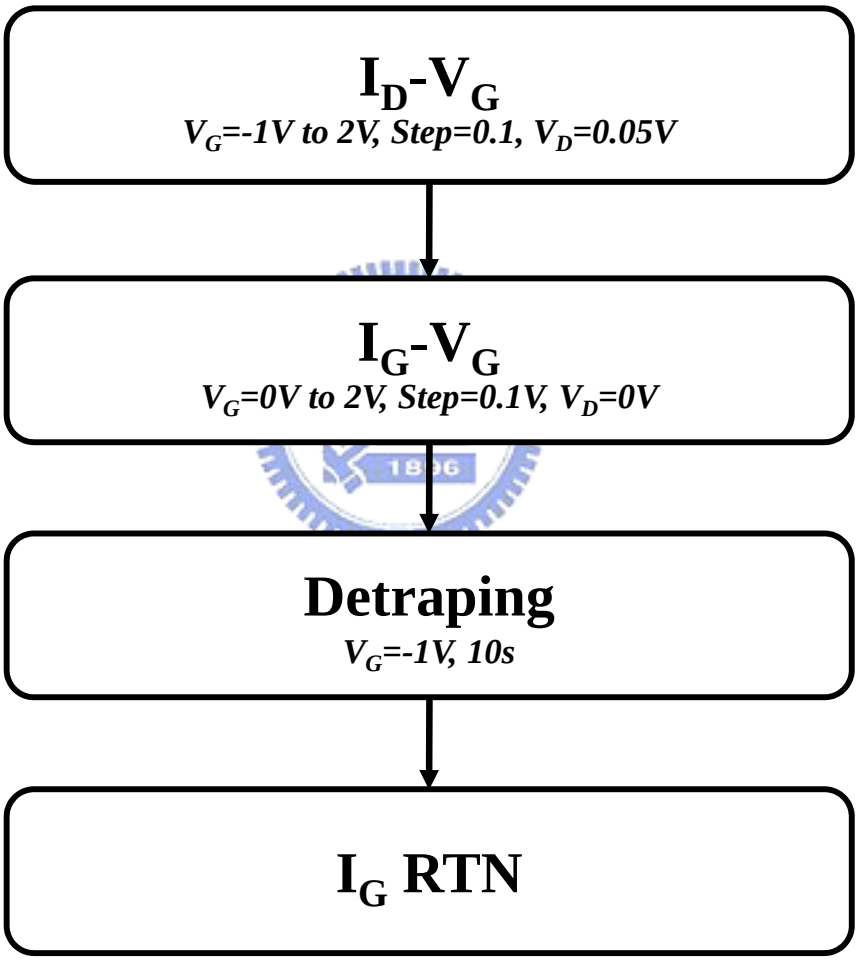


Fig. 2.1 The operating procedure of following measurement applied to DUT.

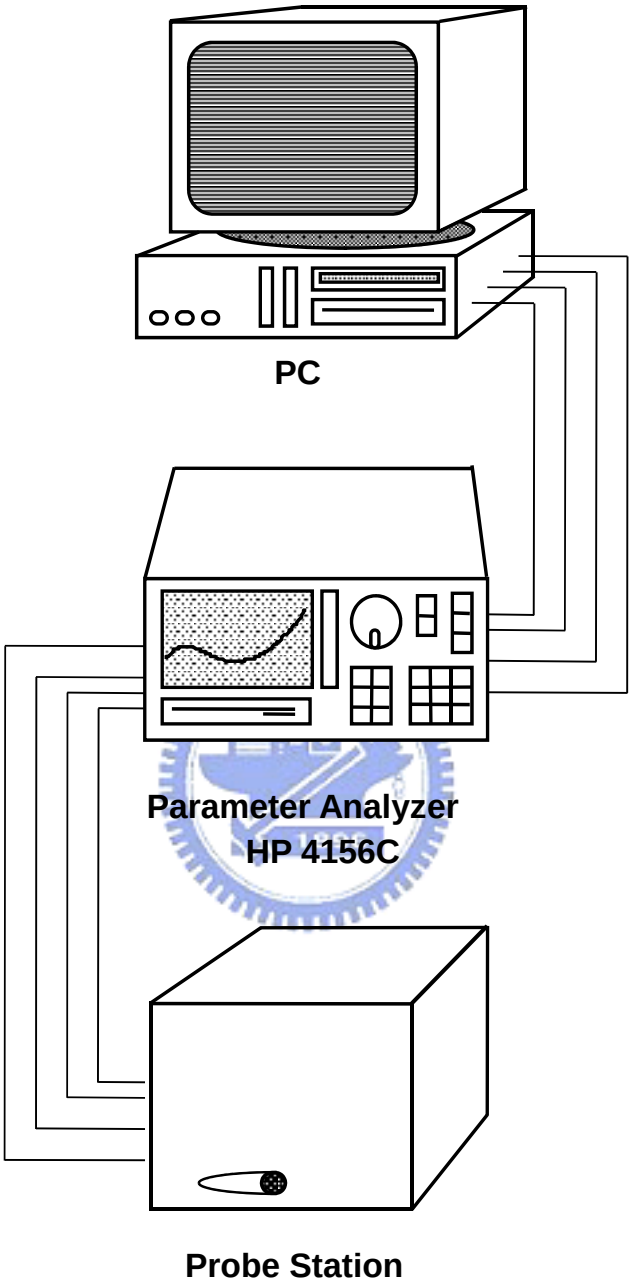


Fig. 2.2 The measurement setup using Analyzer HP 4156C to sampling as RTN processing. Notably there is no switch equipment HP 5250 here.

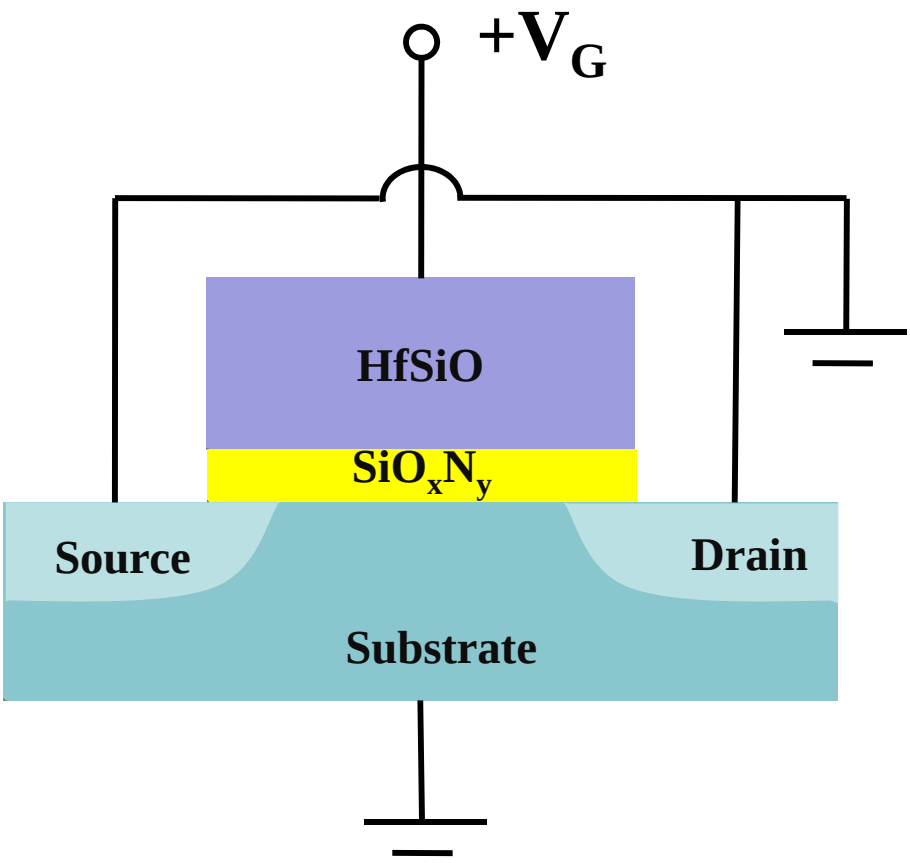


Fig. 2.3 The terminals setup using Analyzer HP 4156C to sampling.

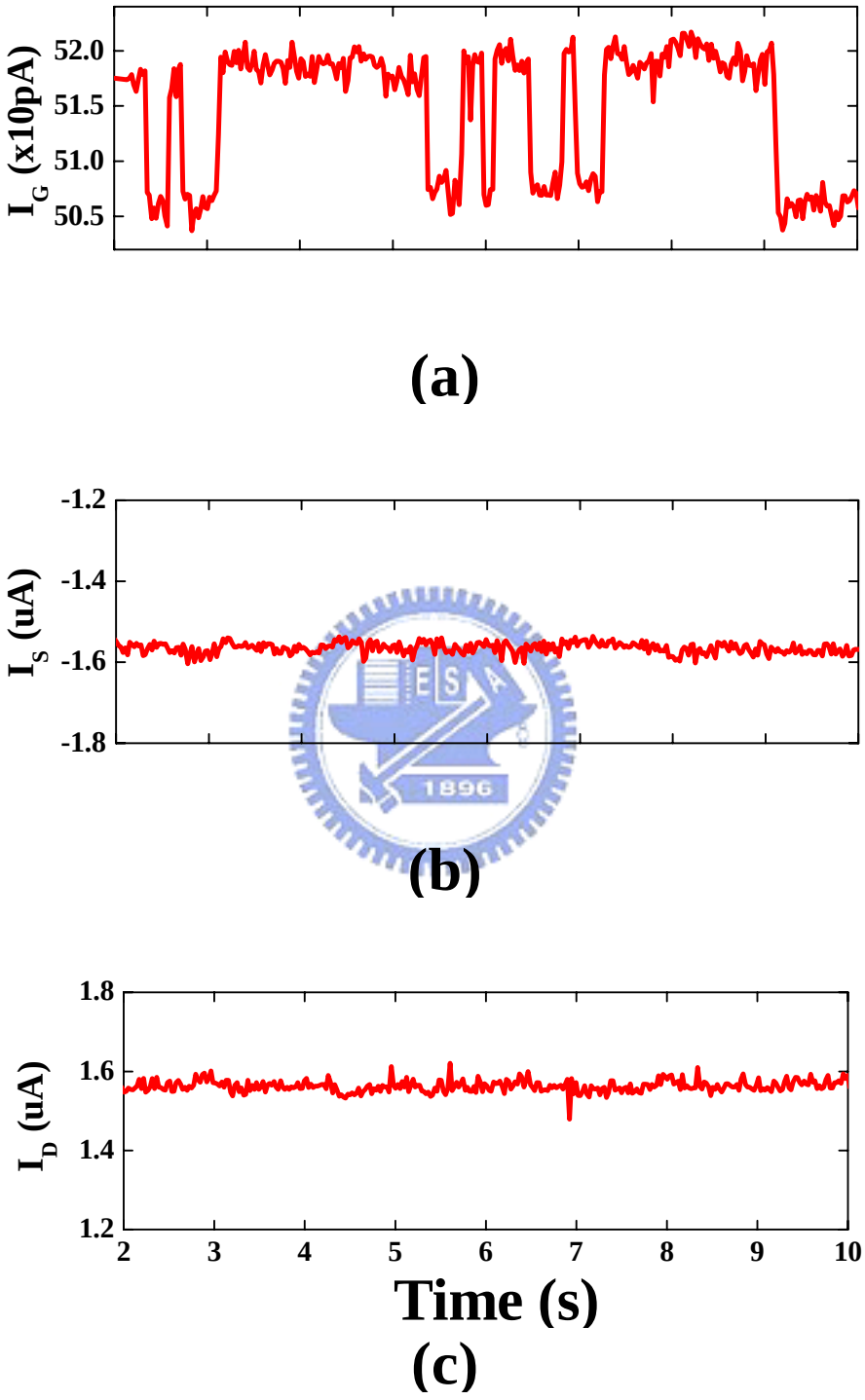


Fig. 2.4 Evolution of current for single electron capture and emission. (a) I_G, (b) I_S, (c) I_D.

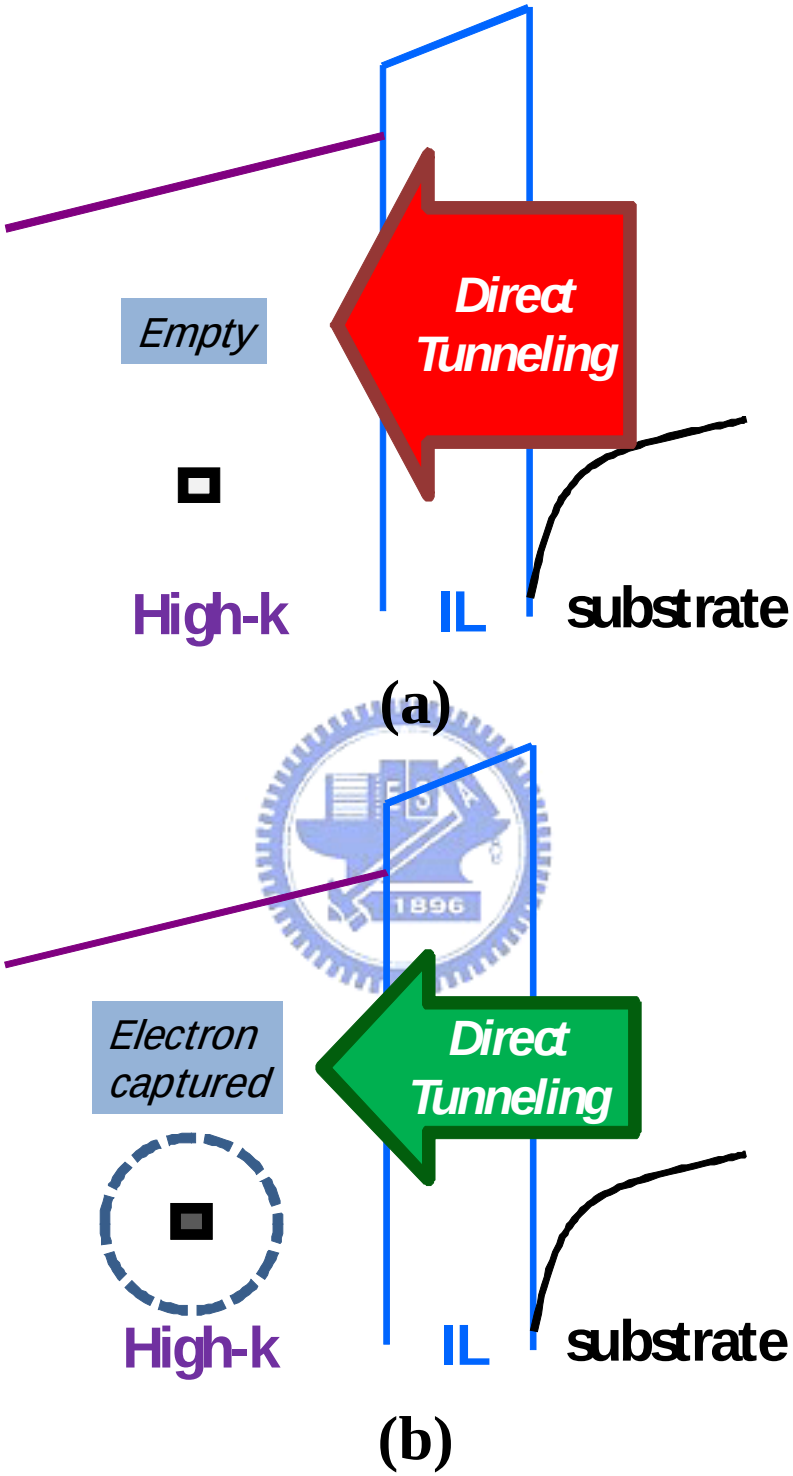


Fig. 2.5 Schematic plot of gate current instability due to electrons trapped. (a) Trap empty state, (b) Trap filled state.

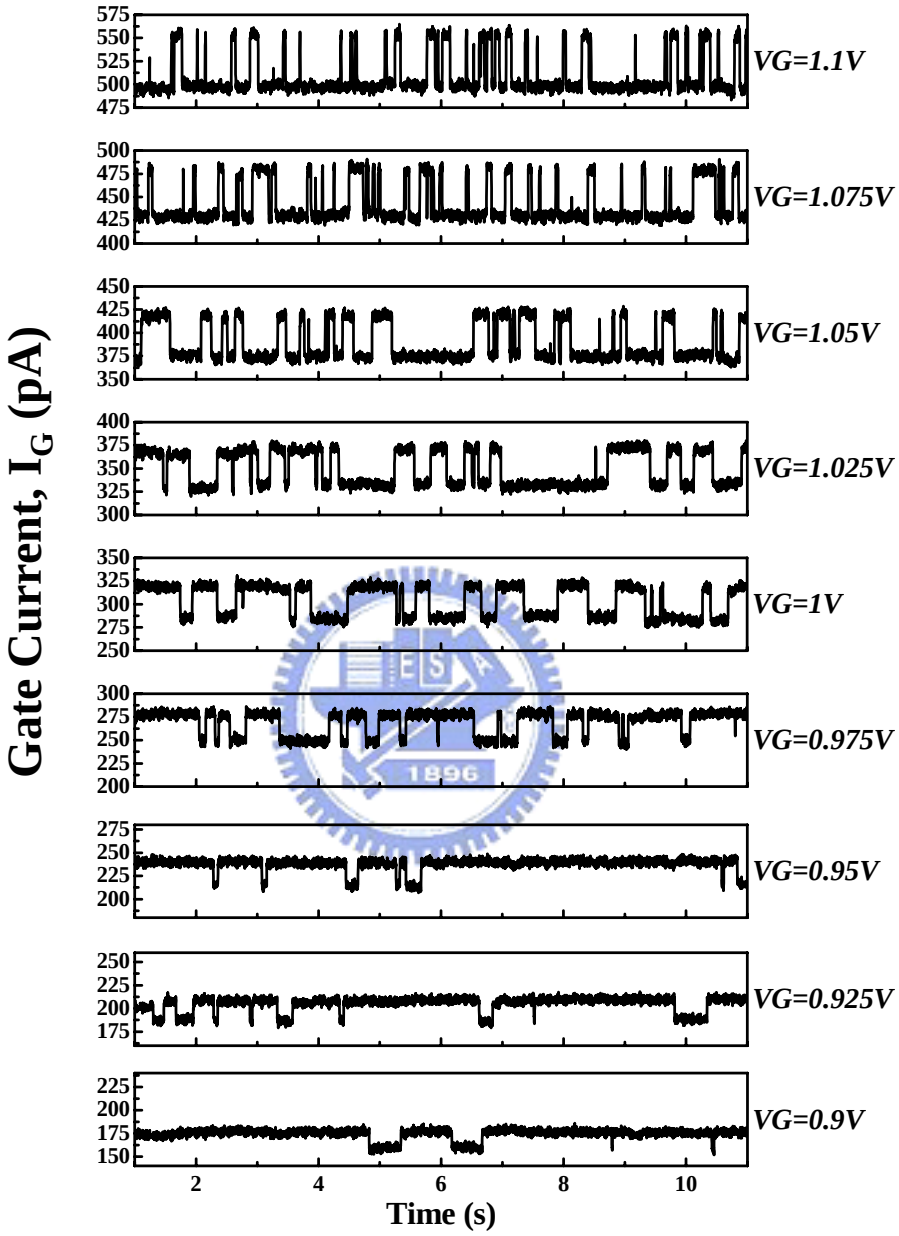


Fig. 2.6 Gate current waveform of high-k nMOSFET with process induced trap (PIT1), **T=25℃**

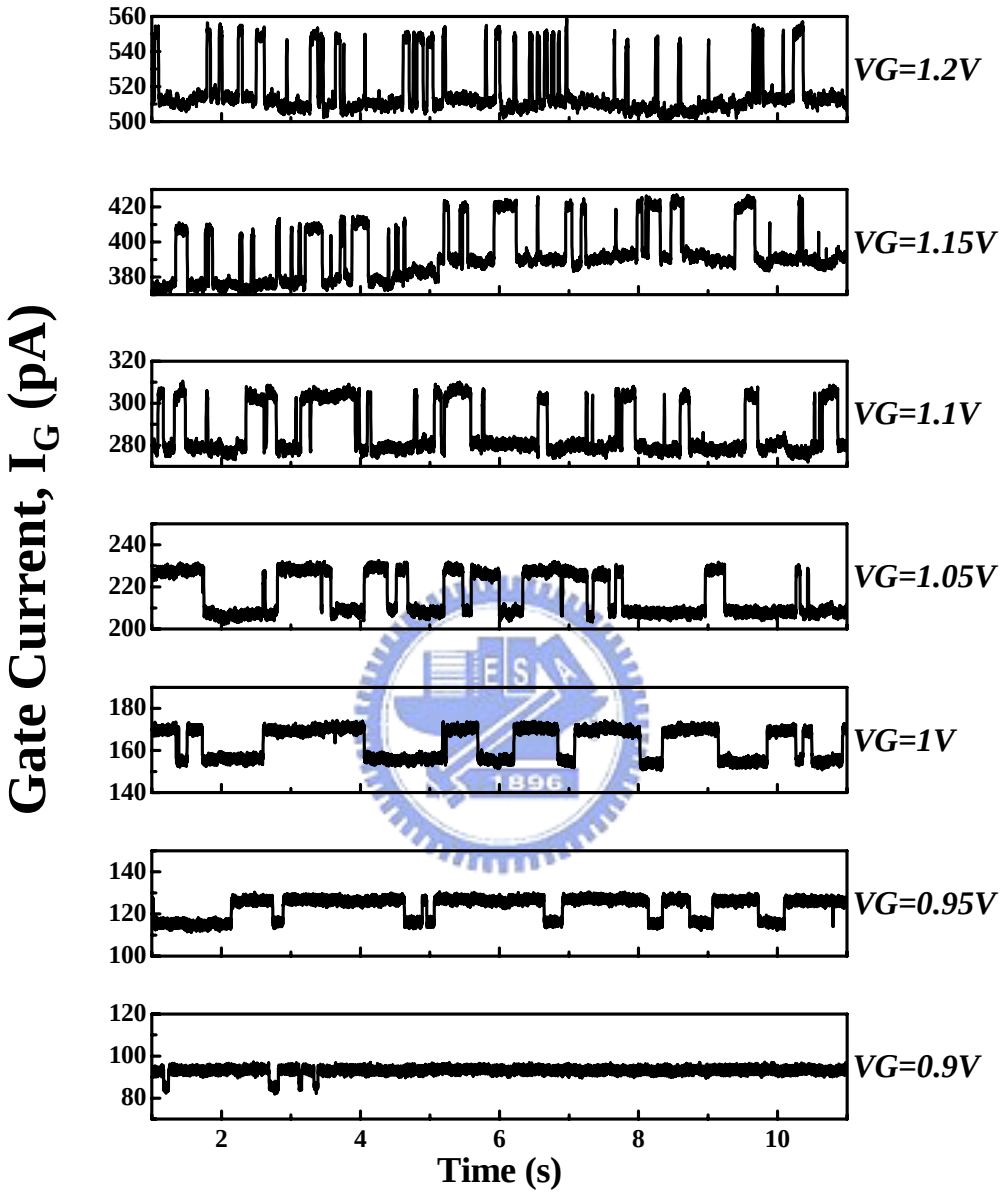
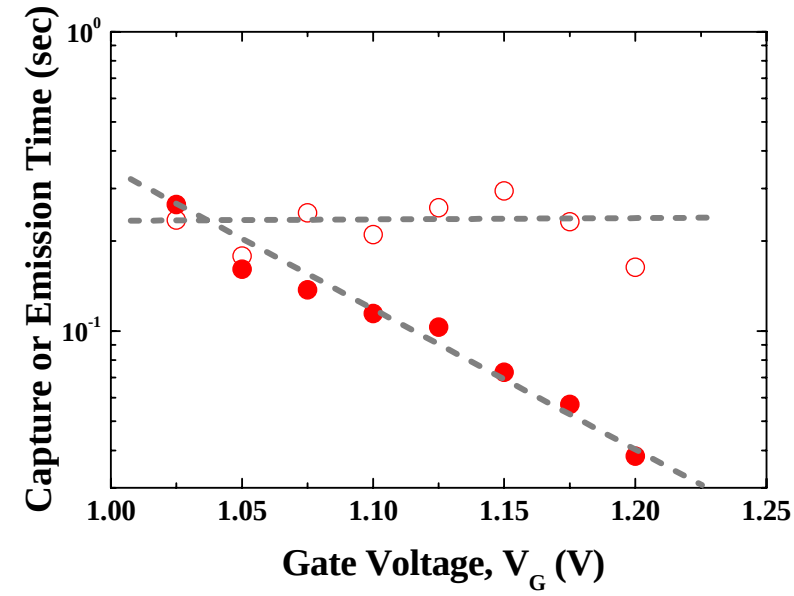
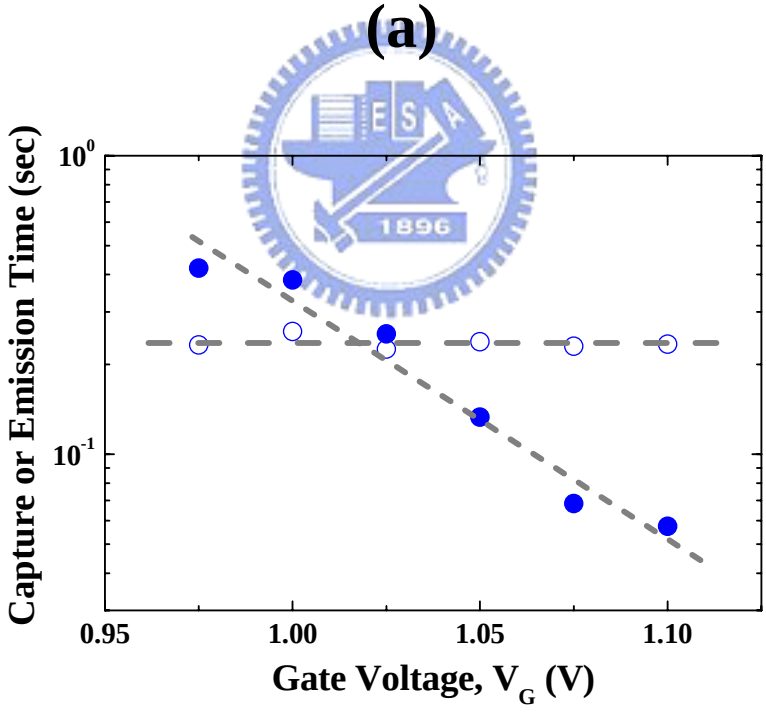


Fig. 2.7 Gate current waveform of high-k nMOSFET with process induced trap (PIT2), **T=25℃**

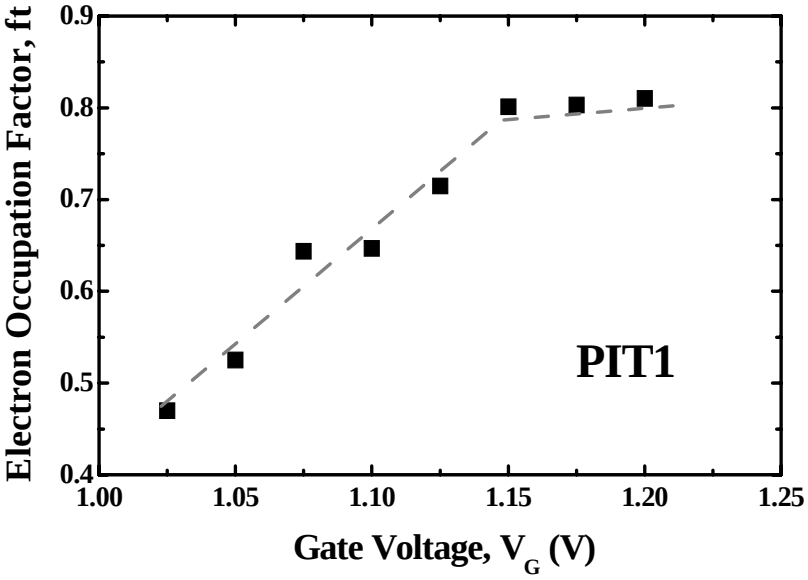


(a)

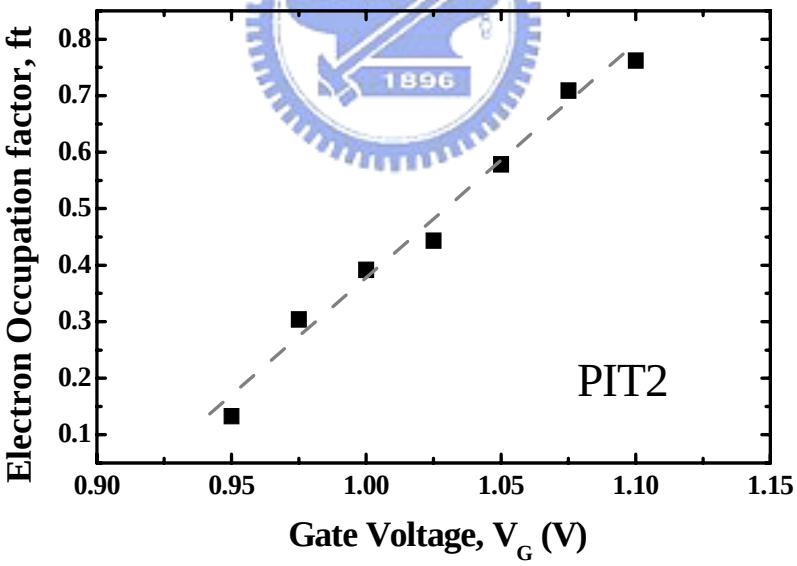


(b)

Fig. 2.8 Variation of capture time τ_c (filled symbol) and emission τ_e (open symbol) as gate voltage increasing (a) PIT1 (b) PIT2.



(a)



(b)

Fig. 2.9 Plot of electron occupation factor *ft* versus gate voltage (a) PIT1, (b) PIT2.

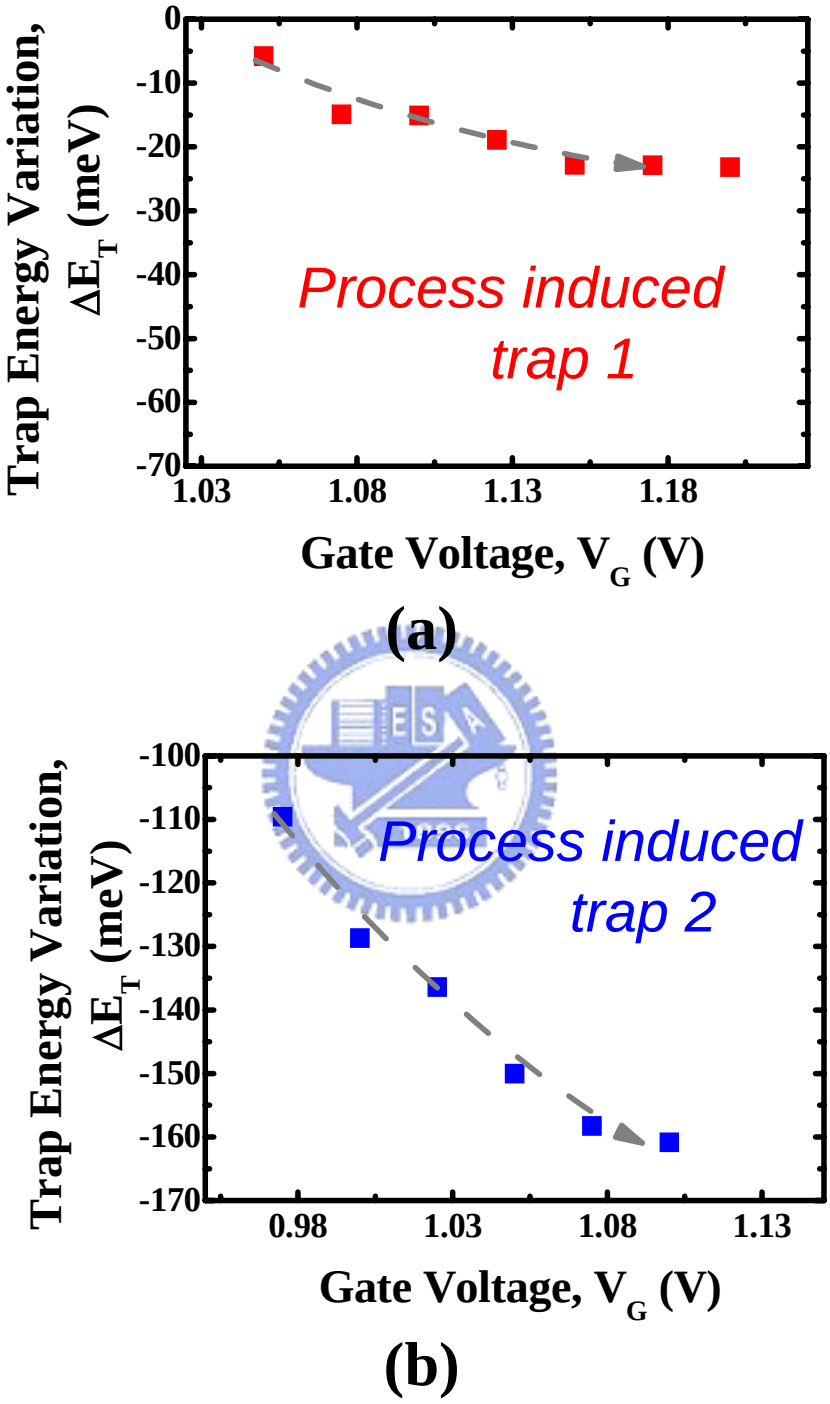


Fig. 2.10 Trap energy variation ΔE_T to gate voltage plots (a) PIT1, (b) PIT2.

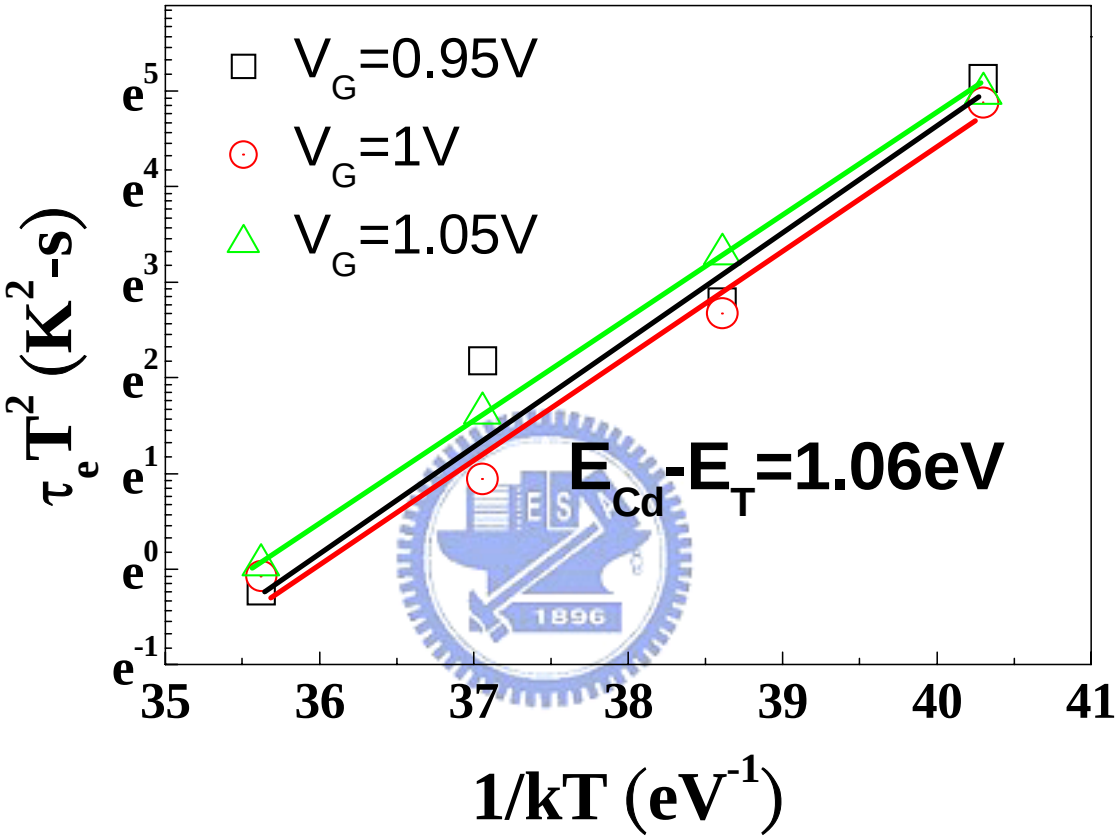


Fig. 2.11 $\tau_e T^2$ versus 1/kT plots for PIT1. Energy difference between conduction band of dielectric and trap E_{Cd}-E_T is around 1.06eV.

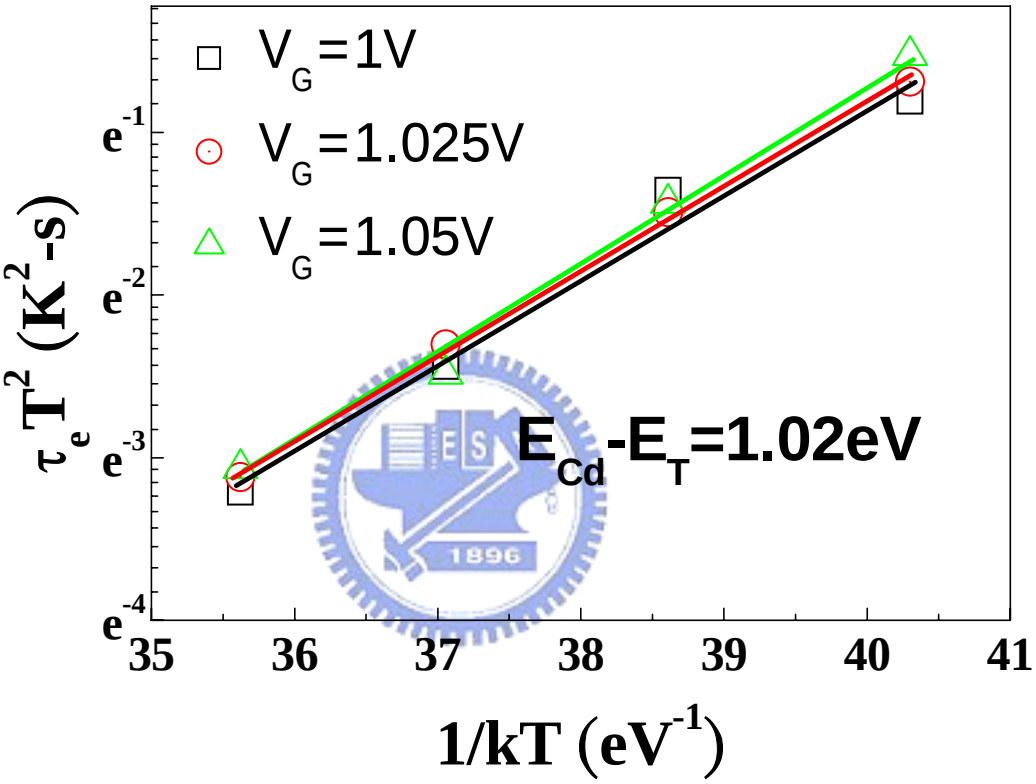


Fig. 2.12 $\tau_e T^2$ versus 1/kT plots for PIT2. Energy difference between conduction band of dielectric and trap E_{Cd}-E_T is around 1.02eV.

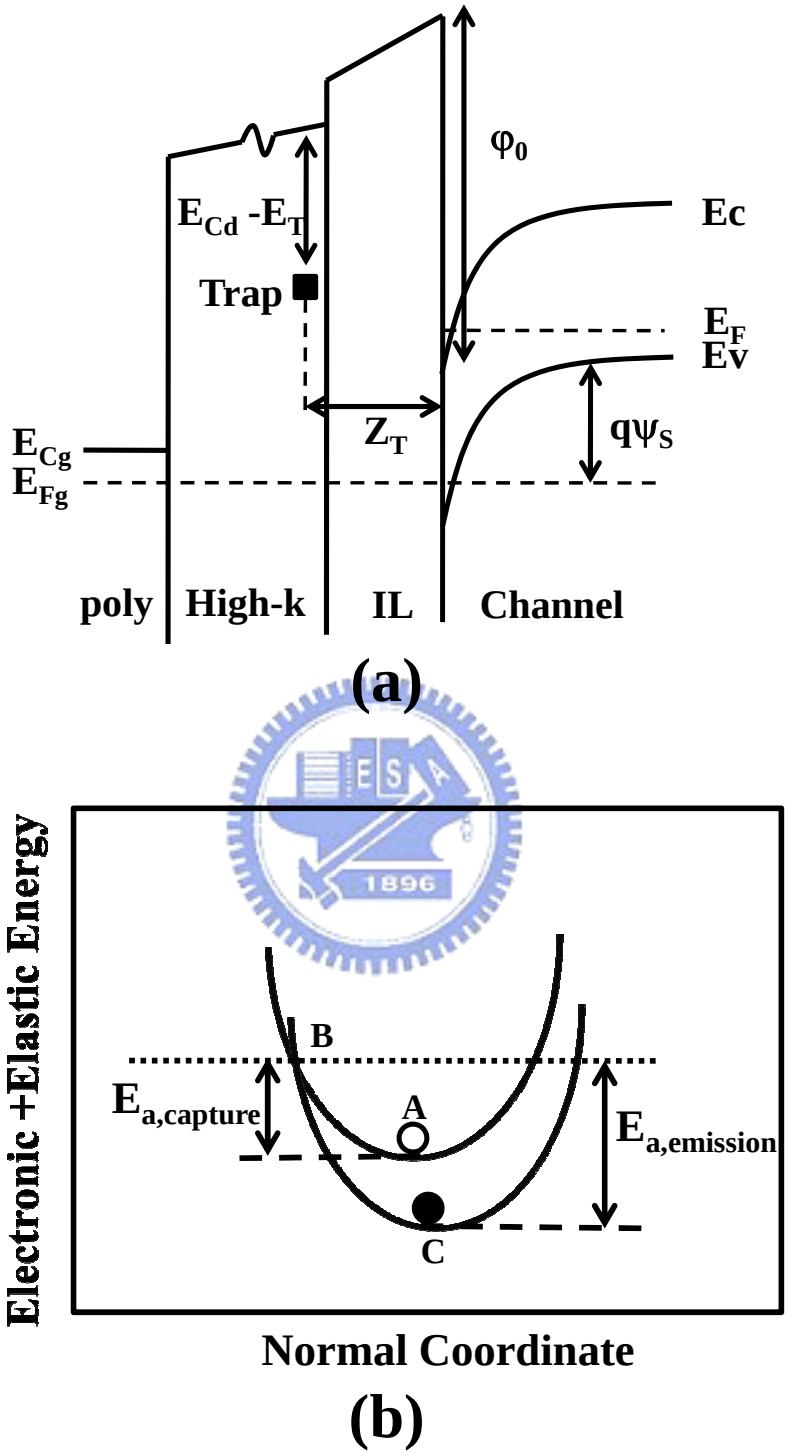


Fig. 2.13 (a) Energy band diagram at the trap position in the channel.

(b) Configuration-coordinate diagram for an acceptor trap. Open circle represents an empty trap and solid one is for a filled trap.

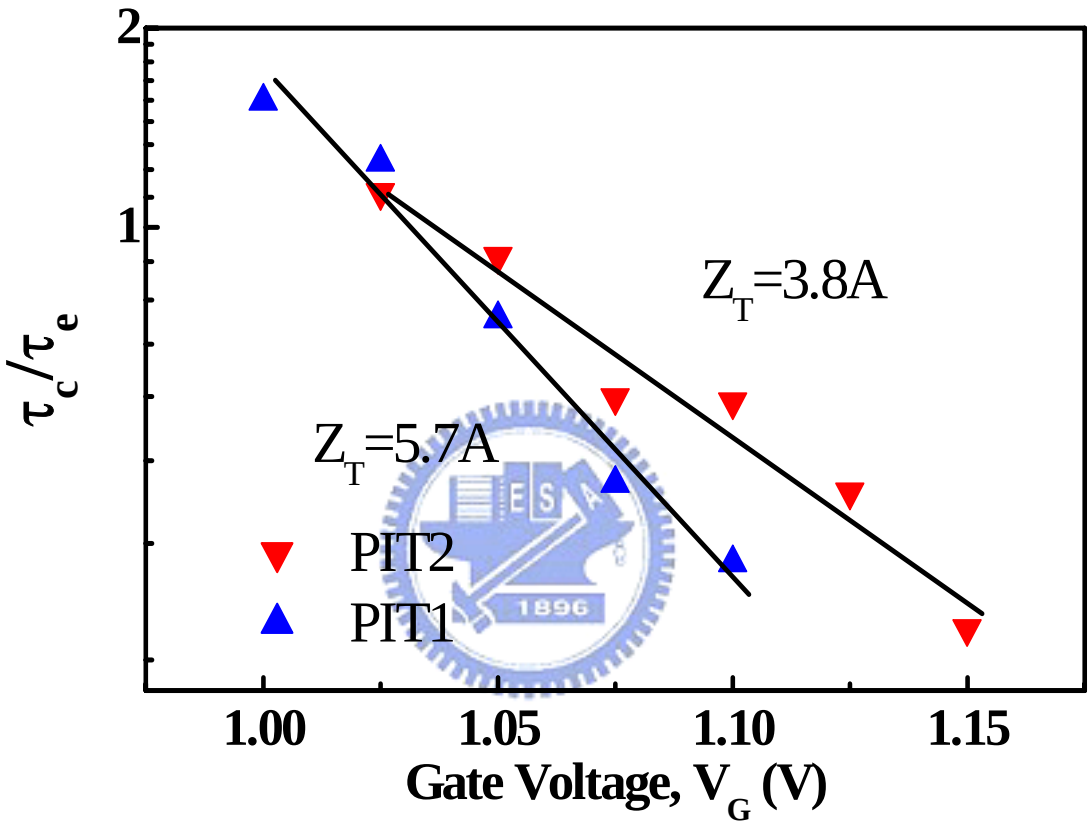


Fig. 2.14 Relationship of τ_c/τ_e to gate voltage. The extracted Z_T from the slope is 5.7A and 3.8A for PIT1 and PIT2 respectively.

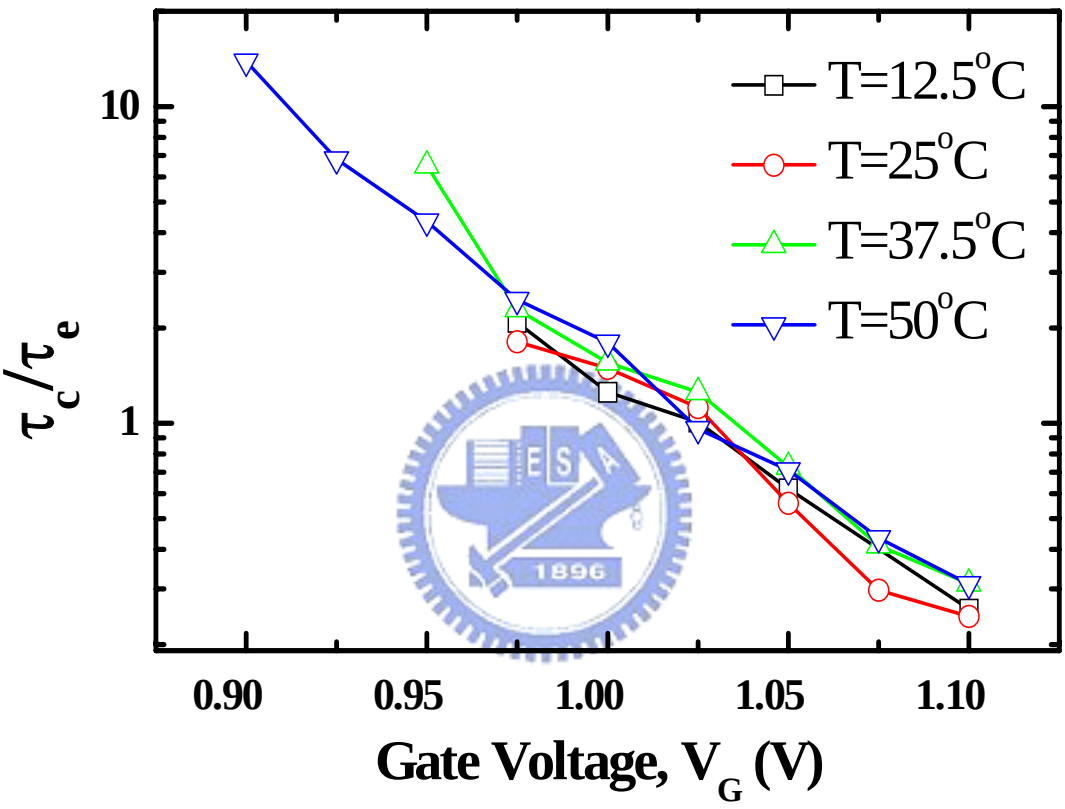
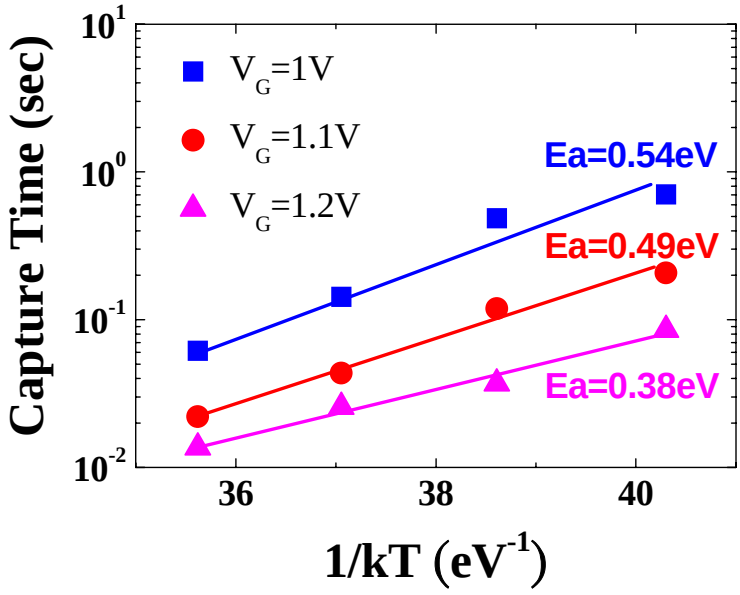
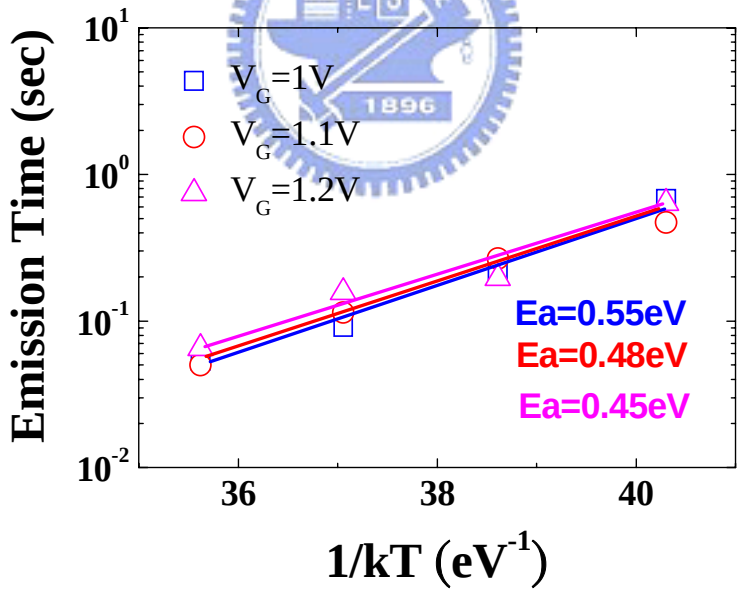


Fig. 2.15 Plot of τ_c/τ_e versus gate voltage at different temperature. The slope of plot at different temperature is identical. (i.e., Z_T is reliable in our extraction.)

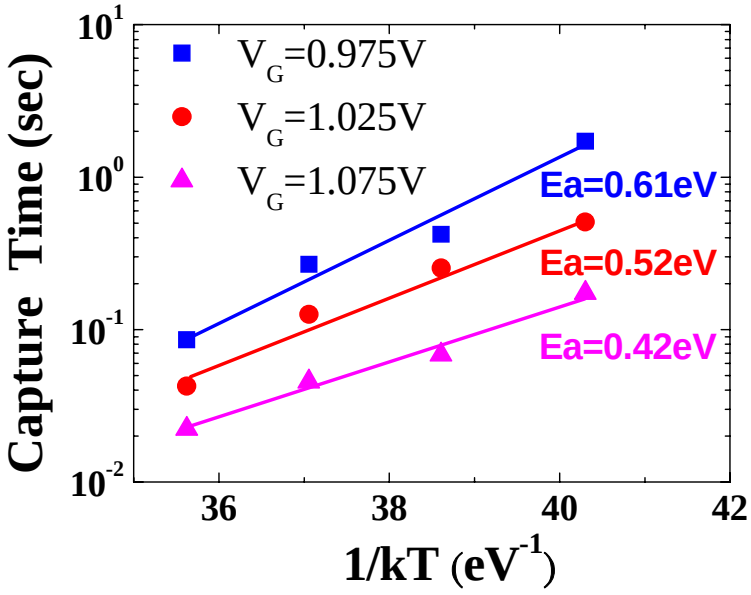


(a)

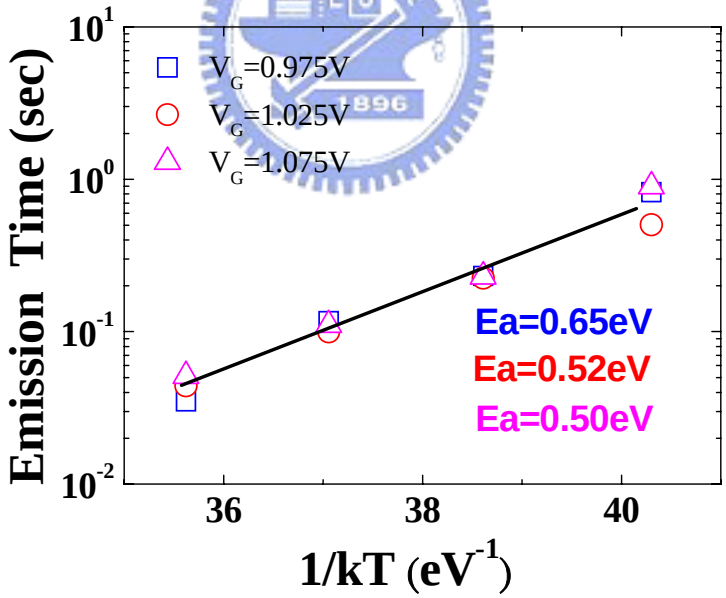


(b)

Fig. 2.16 Dependence of characteristic time to 1/*kT* on distinct gate voltages for PIT1 (a) capture time, (b) emission time. Activation energy E_a is also expressed in the plot.



(a)



(b)

Fig. 2.17 Dependence of characteristic time to 1/*kT* on distinct gate voltages for PIT2 (a) capture time, (b) emission time. The trend of Activation energy E_a is identical with PIT1.

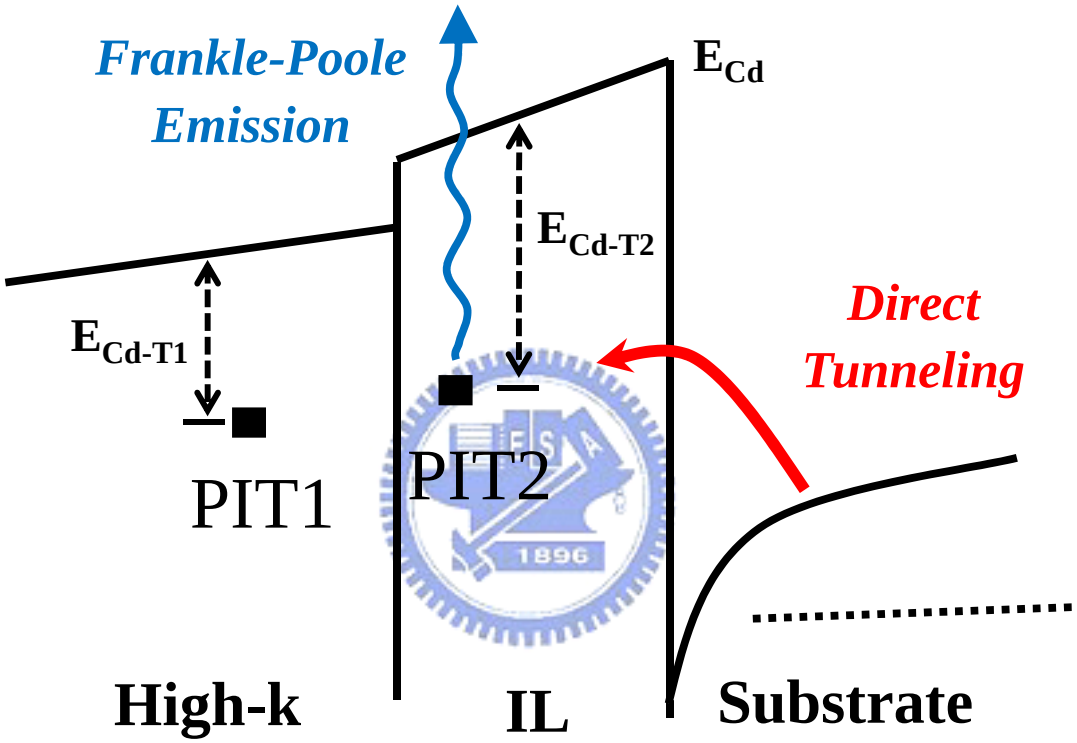


Fig. 2.18 Schematic plot of capture and emission mechanism. This is proven that electrons could be captured by tunneling from substrate and emitted by Frankle-Poole emission.

Chapter 3
Random Telegraph Signal of Gate Current for Stressed Devices in High-k nMOSFETs

3.1 PBTI in NMOSFETs with High-k Dielectrics

Bias Temperature Instability is a degradation phenomenon in MOSFETs. Even though the root causes of the degradation are not yet well understood, it is now commonly admitted that under a constant gate voltage and an elevated temperature, a build up of charges occurs either at the interface Si/SiO_2 or in the oxide layer leading to the reduction of MOSFETs performances. Unlike SiO_2, the high-K dielectrics such as Hf-based dielectrics present serious instabilities for negative and positive bias (NBT), after NBT and PBT (Positive Bias Temperature) stresses. The trapped charges are sufficiently high to represent one of the high-k integration most critical show stopper that causes V_t instabilities and drive current degradation. The instability is worrying, especially in the case of NMOS PBTI. It has been reported that the HfO_2 MOSFETs is limited by nMOSFETs PBTI rather than pMOSFETs PBTI [3.1]. In this section, we focus the discussion on NMOS only.

3.1.1 Threshold Voltage Instability

The NMOS PBTI reported in [3.2] shows an electron trapping ($\Delta V_t > 0$). The main difference with PMOS NBTI is that the whole V_t shift is recovered. That means that no interface traps are generated at this gate bias stress. As for the NBTI, the PBTI characteristics display a logarithmic law and it can be well explained by the direct tunneling electron trapping. The trapping dynamic can be well explained by the model proposed by [3.3]. As explained below, the V_t shift during the stress can be well

explained by an electron tunneling from channel interface to the acceptor traps in the interfacial or high-k bulk layer, i.e.,

$$\Delta V_t = \frac{qN_t}{C_{ox}\alpha}\ln\left(\frac{t}{t_0}\right) \tag{3.1}$$

The V_t could be characterized by pulsed I_d-V_g method only and it is unreliable in D-C measurement system due to transient carriers trapped happening in conventional I_d-V_g and C-V methods. The interfacial oxide thickness effect and the interface treatments on the V_t instability have also been reported [3.4][3.5]. Like ΔV_t, saturation drain current $I_{d.sat}$ is heavily degraded owing to amounts of trap generation near the channel. Unlike ΔV_t and $I_{d.sat}$, sub-threshold swing and maximum transconductance $G_{m,max}$ do not change with stressing thereby indicating that interfacial trap generation is negligible [3.6].

3.1.2 Trap Generation

Compared with SiO_2, high-k based material dielectrics have severe reliability issue post stress operation and affect regular I-V characteristics. In [3.7], the degradation is investigated to exhibits two stages, different degradation rate and stress temperature dependence. The drain current degradation in the first stage is attributed to the charging of pre-existing high-k dielectric traps while the degradation in the second stage is mainly due to additional high-k trap creation by transient measurement system. The two-stage degradation will affect the extrapolation of PBTI lifetime. The cause comes from lots of trap generated in the high-k bulk layer after stress and pre-existing traps would enhance another traps appearance that could be not happen in SiO_2 dielectrics. Trap density at SiO_2/Si interface, high-k/SiO_2 interface, and high-k bulk layer are quantified respectively with a simple charge pumping method. We applied low frequency charge-pumping measurement [3.8] on our high-k dielectric devices as shown in Fig. 3.1. The following is the spatial distribution of interface trap:

$$N_t(x_m) = -\frac{1}{q\lambda_n A \Delta E_t}\frac{dQ_{cp}}{d\ln(f)} \tag{3.2}$$

$$x_m = \frac{1}{\kappa_0}\cdot\ln(t_m\sigma_n v_n) \tag{3.3}$$

As a result, traps close to Si/SiO_xN_y interface have no significant increase. Toward the dielectric deeply about 3A that has the composition of SiO_xN_y only, not the transition region, the amount of traps is much lower. Trap density is largely raising adjacent to HfSiO region and there is a maximum trap density about 5~ $8x10^{21}$ (cm^{-3}) in transition area of SiO_xN_y /HfSiO interface. The IL thickness is about 4.2A apparently and trap density is stable over 4.2A. Post-stress trap density variation is also shown in the figure. There is considerable boost in HfSiO bulk region comparatively.

3.1.3 Fowler-Nordheim Stress Model of Electrons

Here, we discuss the dependence of ΔV_t from the injected electrons without considering temperature dependence. It is obvious that increasing the voltage, a larger ΔV_t is observed for same amount of injected electrons. The effect can be ascribed to three different causes; a generation of additional trap sites at higher voltages, a more effective electron trapping and/or a different spatial position of the trapped electrons within the dielectric stack [3.9]. In the next section, we will discuss F-N stress on high-k devices with distinct stress condition, while contain high and low field F-N stress and treat RTN phenomenon in great detail.

3.2 I_G RTN in High and Low Positive VG stress

The procedure of following experiment is shown in Fig. 3.2. There are same schedules in stressed devices measurement except for additional stress step. Some notable steps should be taken care. In I_D-V_G step, the purpose is to select the regular I-V characteristic devices with similar gate leakage and

magnitude of drain current. Aiming at the observation of RTN with stress induce traps, process induced traps noise is forbidden here and second step, I_G RTN is used to ensure absence of PIT RTN. Subsequently stress is adopted on selected devices. We applied F-N stress in inversion mode with injecting electrons to destruct gate dielectrics. Without elevating temperature here, we could prevent the effect of changing temperature and measure RTN at once. Two different stress conditions here; first one is high field (V_G= 2.5V) and the other one is low field (V_G= 2.1V). The evolutions of gate current during stressing are shown in Fig. 3.3. Traps generating for apparent RTN is hard to say happening on specific time and its dependence with time on different stress voltage is also not regular. In high field stress, we obtain significant RTN appearance and continued subsequent analysis. Nevertheless in low field stress trap would be not generate in short time and more time is needed to derive significant RTN appearance. Avoiding too many traps happen, stress is proceeding in cycles (100 seconds per cycle) and RTN measurement would be execute after every stress cycle until we observe obvious RTN appearance.

3.2.1 I-V Characteristics

The I_D-V_G and I_G-V_G plots of pre and post-stress devices are shown in Fig. 3.4 and Fig. 3.5. Drain current degradation is significant about 30% degradation but gate current has no increase on operating voltage (V_G= 1.2V) after low field stress. Compared with low field stress, drain current degrades only 5% and gate leakage is high after high-field stress. The main cause in drain current degradation is attributed to near Si/IL interface traps generation that will decline channel carriers mobility. Electrons gain energy and would lose energy as tunneling from channel through dielectrics in inversion mode stress. Released energy breaks lattice structure and traps generate. As illustrated in Fig. 3.6, long term and low-field stress would cause near interface damage that happens due to electrons earning less energy and releasing near interface. Short term and high-field stress induces local damage near poly gate because electrons carry larger energy and can penetrate gate dielectrics deeper then release.

Channel carriers mobility would suffer more degraded in low field and long term stress, and hence threshold voltage and saturation current “turn-around” behavior may relate to integrity of near Si/IL interface [3.10]. In Fig. 3.3(b), stress induced leakage current (SILC) happens obviously, so high-field stress would make heavy SILC. Even soft or hard breakdown will appear as stress voltage becomes higher [3.11] [3.12].

3.2.2 Gate current Waveform

Although traps generate a lot after stress, they do not affect I_G RTN appearance. It must be a specific trap distributing in particular gate voltage and we will discuss it in this section. We already generate stress induced traps that contribute to the gate current noise expectantly in latest section and continue to analyze now.

The evolutions of gate current versus time after stress are shown in Figs. 3.7- 3.8. The trap after high field stress (SIT1) is sensed during V_G= 0.8V to 1V. Another fast trap or breakdown path is also sensed for gate voltage higher than 0.85V. The noise amplitude is about 50pA and total gate current is around 200-800pA at different gate bias. The trap after low field stress (SIT2) works during higher gate bias VG= 1.2V to 1.4V. There is a stable 2 levels of gate current until V_G= 1.3V and 3 levels of gate current appears. The additional trap sensed in high V_G is a slow trap that has compatible characteristic time (τ_c and τ_e) with SIT2. The noise amplitude is about 60pA and total gate current is around 0.8-2nA at different gate biases.

3.2.3 Capture and Emission Time

The plots of capture and emission time are shown in Fig. 3.9. There is opposite trend as gate

voltage increasing. SIT2 (low-field stress) has same tendency with previous discussed process induced traps but SIT1 (high-field stress) does not. Capture time of SIT1 is low in low V_G and gets higher as V_G increasing. It seems to be something new in our observation and we will find it out in section 4.3. Here we obtain same emission time (τ_e~ 0.2s) with PIT1 and PIT2 and capture time drops off in higher gate bias, that it means an electron is captured/emitted through same mechanism for SIT2.

3.3 Result and Discussion

Electron occupation probability (defined in Eq. 2.1) of SIT1 decreases with V_G increasing shown in Fig. 3.10. Hence, electrons are easily captured in trap sites and hard to escape in low gate bias. It really does not fit with our expectation that we mentioned before. In general, channel electrons density increases as V_G raises and more carriers would join the tunnel affair and then fall into traps. The contradiction may indicate electrons not tunneling from channel. In our opinion, emission time is invariable and same magnitude in SIT1 and SIT2. Only capture time has completely opposite trend. Where else electrons can tunnel from except for channel? The most possible path is from poly-gate as schemed in Fig. 3.11(a). There are lots of electrons in n+ poly-gate and the native imperfect character is depletion happening in the poly/dielectrics interface. Electron density changes with gate bias varying. We utilize the model that electrons tunnel from poly gate in the following calculation. Indeed, the result is also accord with the behavior electrons tunneling from channel.

3.3.1 Trap Depth

The trap depth is extracted from the slope of $ln(\tau_c/\tau_e)$ versus V_G as shown in Eq. 2.12. Trap character of SIT2 is the same with process induced traps and trap depth is obtained about 3.7A in Fig. 3.12(b) using same equation. Aiming at deriving the trap depth of SIT1, Eq. 2.12 must be corrected

shown as below. The difference is no negative sign at the right side of equal mark. Emission time is treated as a constant and capture time proceeds in opposite trend, so $ln(\tau_c/\tau_e)$ would differ in a minus sign.

$$\frac{d\ln\left(\frac{\tau_c}{\tau_e}\right)}{dV_G} = \frac{q}{kT}\frac{Z_T}{EOT} \tag{3.4}$$

Other coefficients are fixed. Trap depth of SIT1 is about 3.2A away from poly/high-k interface. SIT1 sites near poly gate so electrons tunneling from poly gate is reasonable. SIT2 sites in high-k and SiO_xN_y transition layer near channel compared with SIT1 and hence electrons source is supplied from channel rather than poly gate.

3.3.2 Trap Energy Variation

The plots of trap energy show different variation in Fig. 3.13. The equations in Eq.2.5 are listed in section 2.4.1. Fermi energy level of substrate is fixed mentioned before and (τ_c/τ_e) dependence to gate bias would profile trap energy variation.

$$\frac{\tau_c}{\tau_e} = g\exp\left(\frac{E_T - E_F}{kT}\right) \tag{3.5}$$

$$E_{Tn} - E_{T0} = kT\left[\left(\ln\frac{\tau_c}{\tau_e}\right)_n - \left(\ln\frac{\tau_c}{\tau_e}\right)_0\right] \tag{3.6}$$

Fig. 3.13(b) shows $\Delta E_T/\Delta V_G$ of SIT2 about 80meV/0.1V that is larger than PIT2. Obviously trap energy variation is larger as trap sites near Si/IL interface (Z_T of PIT2 is about 3.8A). On the other hand, trap energy variation of SIT1 shown in Fig. 3.13(a) is positive dissimilar to SIT2. The main cause is shown in Fig 3.11(b). E_F is no longer referring to Fermi energy level of substrate but poly gate. At high V_G, energy band bending is more intense and the difference between trap energy and poly gate Fermi

energy, E_T-E_{Fg} will be larger. $\Delta E_T/\Delta V_G$ of SIT1is about 40meV/0.1V

3.3.3 Temperature Dependence

Now we keep eyes on SIT1 and check it out whether it's also near dielectric conduction band or not. $\tau_e T^2$ versus $1/kT$ plot is shown in Fig. 3.14 and E_{Cd}-E_T is derived about 1.2meV.

Fig. 3.15 is the relationship between capture/emission time and temperature for SIT1. It could be seen that capture time is longer as temperature or gate bias getting higher. Electrons hop into trap sites more hardly as gate voltage increasing because of higher trap energy since Fermi energy of poly gate schemed in Fig. 3.11. Emission time shows no dependence with gate voltage and hence electrons don't escape through tunneling, that is highly dependent of electric field. With temperature higher, both capture and emission time are lower, that it means, more capture/emission events happen during same period of time. Capture time changes about half order of magnitude from T=12.5℃ to T=37.5℃ at low V_G but one order of magnitude at high V_G. The activation energy of capture time in SIT1 intensely gets lower as temperature increasing ($E_{a,capture}$=0.59eV, V_G=0.825V; $E_{a,capture}$=0.68eV, V_G=0.975V). Emission time is same trend with Fig.2.16-2.17 and the activation energy of emission time is identical with the results in process induced traps ($E_{a,emission}$=0.65eV, V_G=0.825V; $E_{a,emission}$=0.50eV, V_G=0.975V). Consequently electrons are captured tunneling from poly gate and emitted by Frankle-Poole emission as schemed in Fig. 3.16. Carriers captured from channel or poly gate is decided by the trap position near poly gate or channel. High field stress would damage near poly/high-k interface and causes traps proximity to poly gate. Low field stress degrades channel carriers mobility and induces lots of traps in IL and near Si/IL interface. Although, emission mechanism is the same no matter where traps site. Elevating temperature will help electrons trapped run away and enhance Frankle-Poole emission.

3.3.4 Noise Amplitude

Gate current and step amplitude of gate current is plotted in Fig. 3.17. Gate current of SIT1 is lower due to lower direct tunneling at V_G= 0.8V~1V and step amplitude is also smaller. Gate current is large about 1~2nA and step amplitude is about 100pA. Step amplitude increases with gate current and $\Delta I_G/I_{G,high}$ is fixed about 10%.

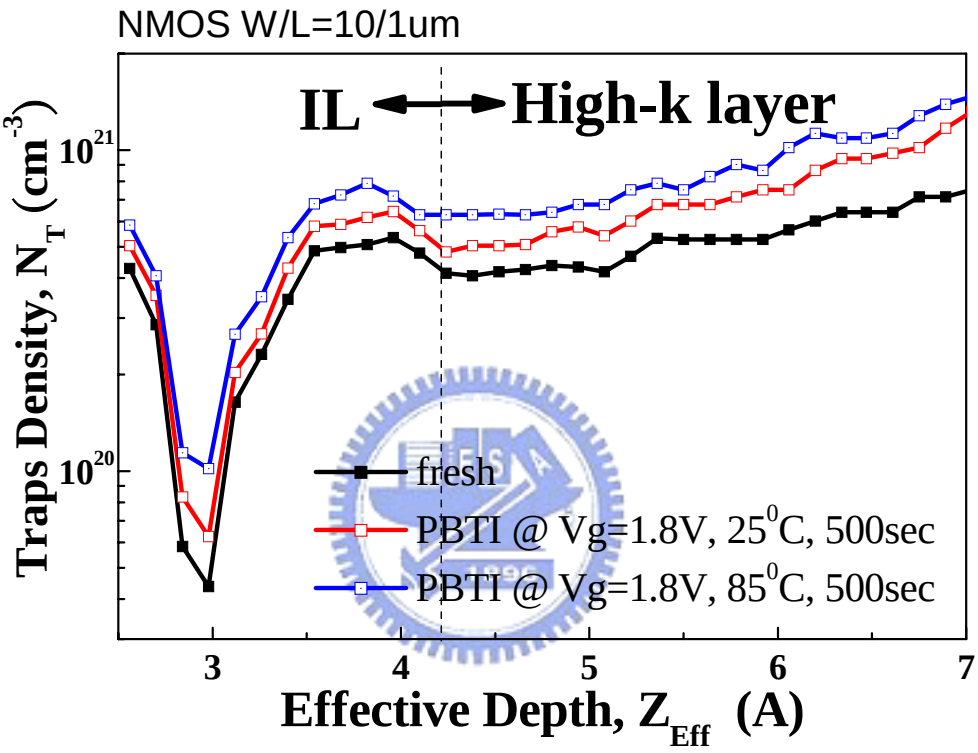


Fig. 3.1 Plot of trap density versus effective depth Z_{eff}. This profile plot is derived by Charge Pumping method.

Procedure

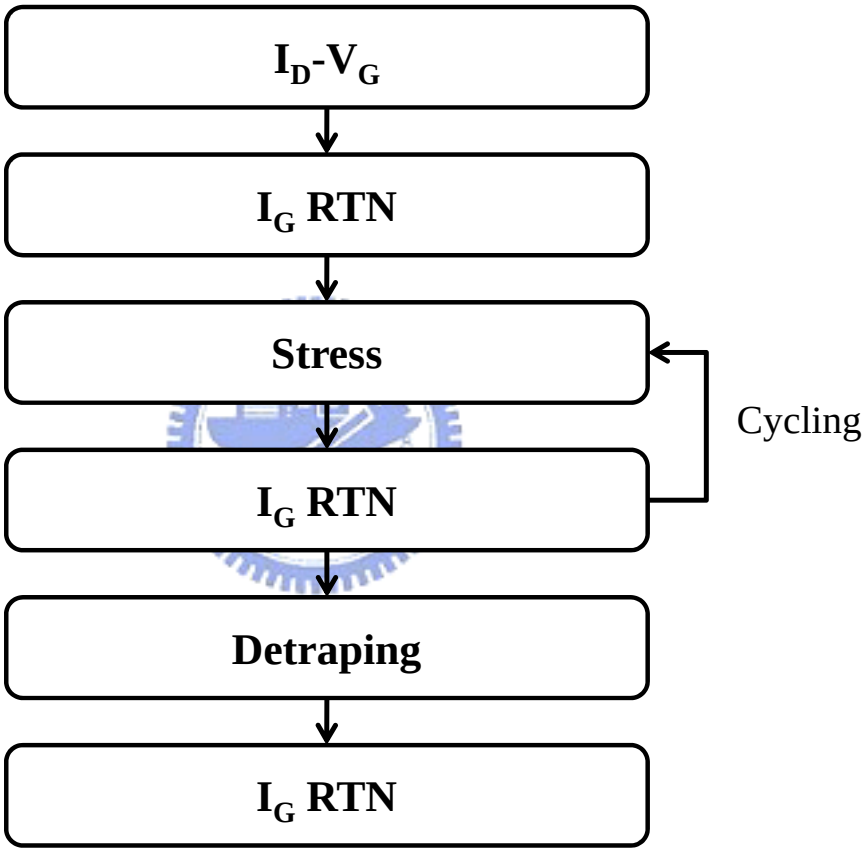
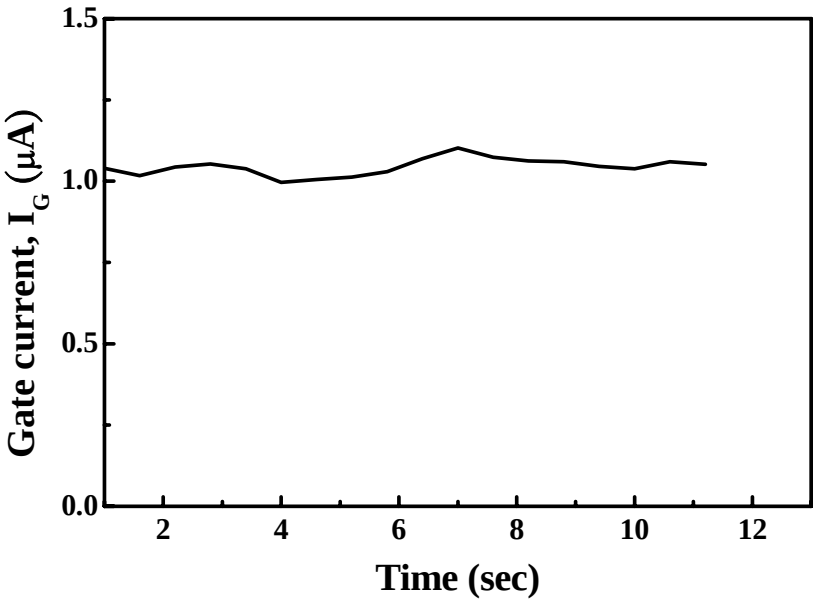
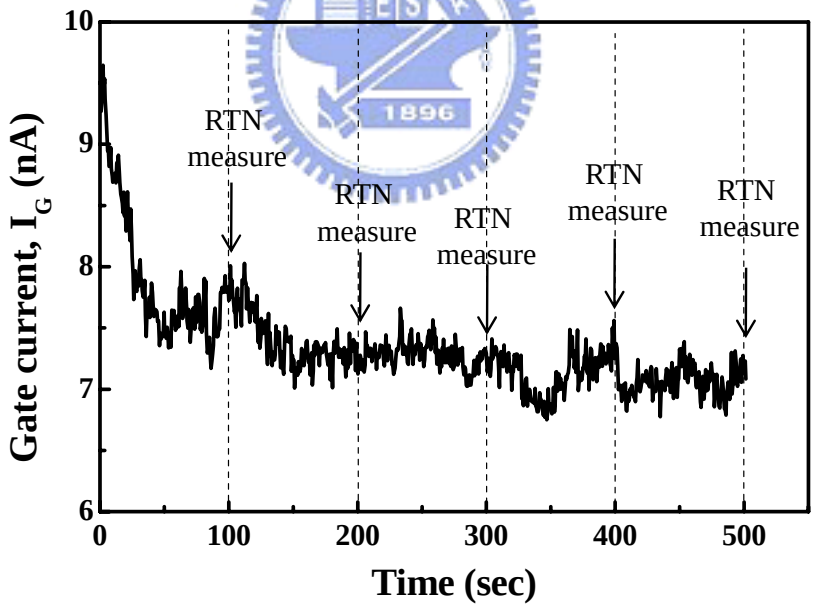


Fig. 3.2 Typical procedure of following analysis in stressed devices. 3rd step "Stress" would continue if 4th step "I_G RTN" has no observation of 2 levels of gate current noise.



(a)



(b)

Fig. 3.3 Evolution of gate current during stress. (a) High-field stress, V_G=2.5V, (b) Low-field stress, V_G=2.1V. Other terminals are grounded.

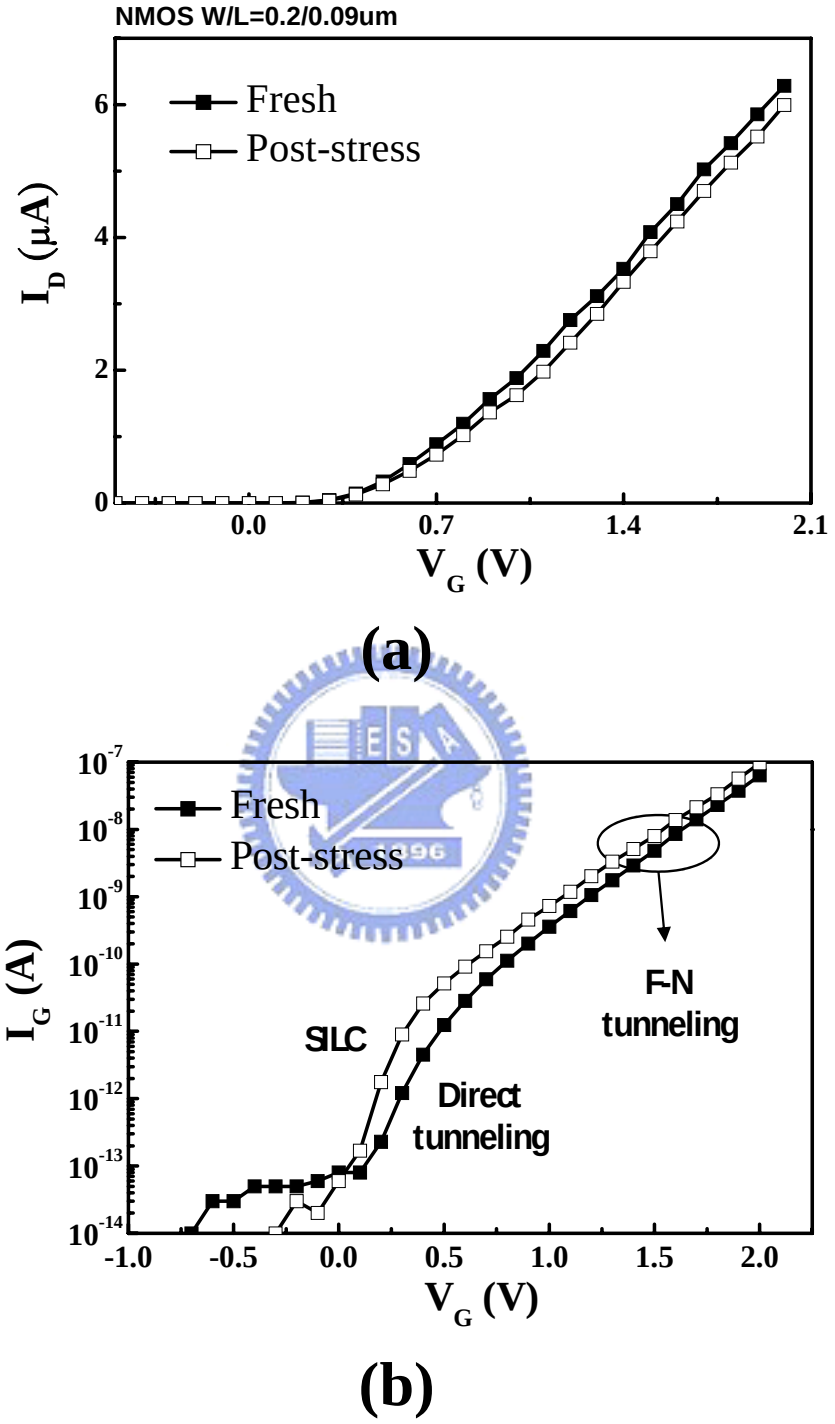


Fig. 3.4 I_D-V_G and I_G-V_G plots before and after high-field stress. Gate current is direct tunneling current at low V_G and F-N tunneling current appears at high V_G. V_D=0.05V, V_S=V_B=0V

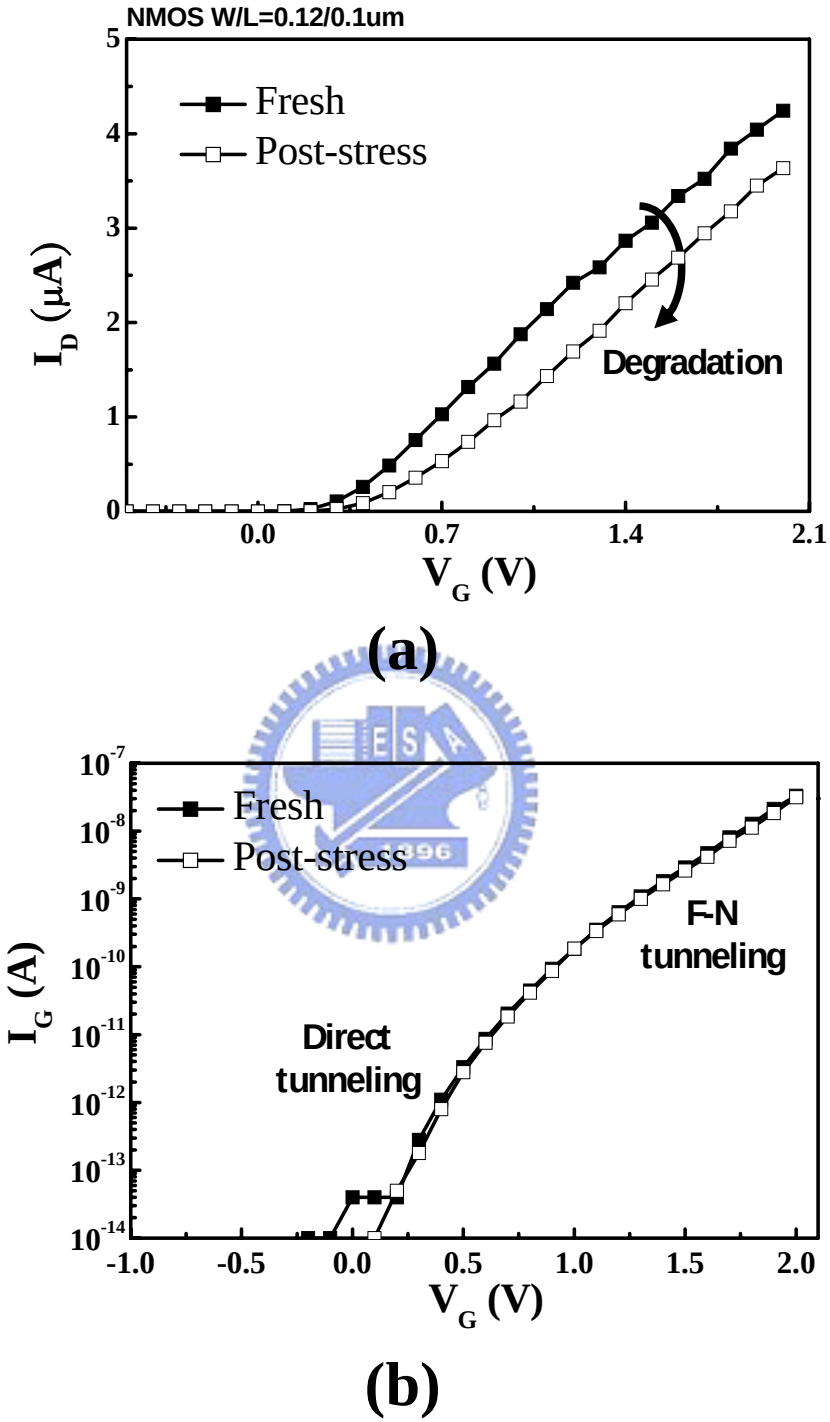
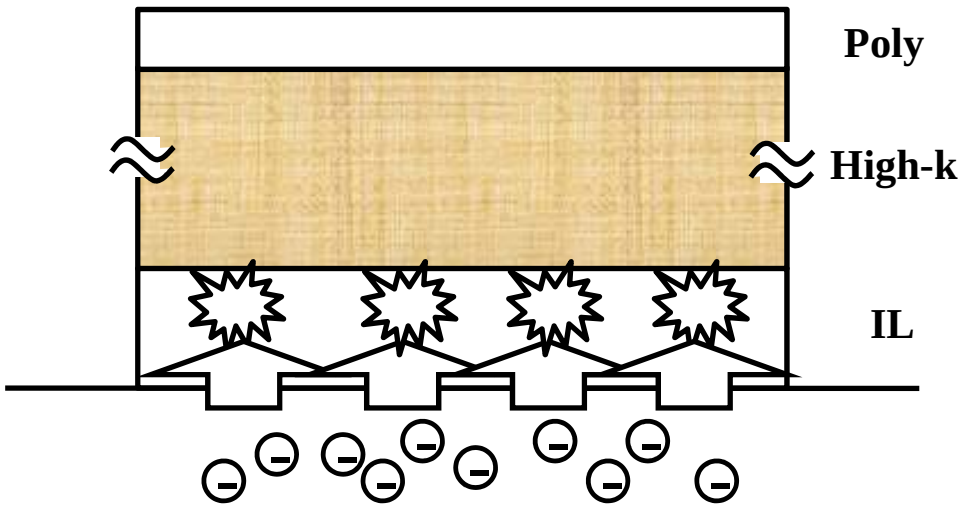
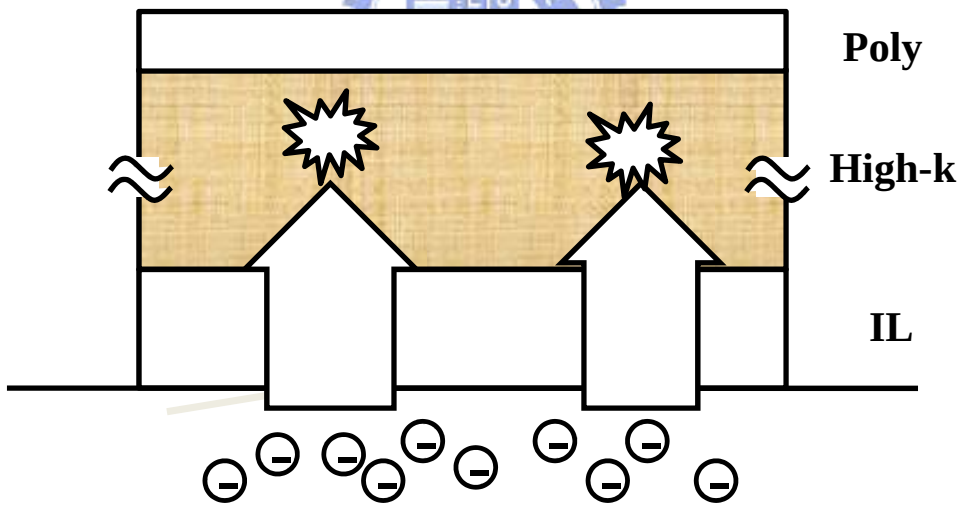


Fig. 3.5 I_D-V_G and I_G-V_G plots before and after low-field stress. V_D=0.05V, V_S=V_B=0V



(a)



(b)

Fig. 3.6 Schematic plot of F-N stress. (a) Low V_G (b) High V_G

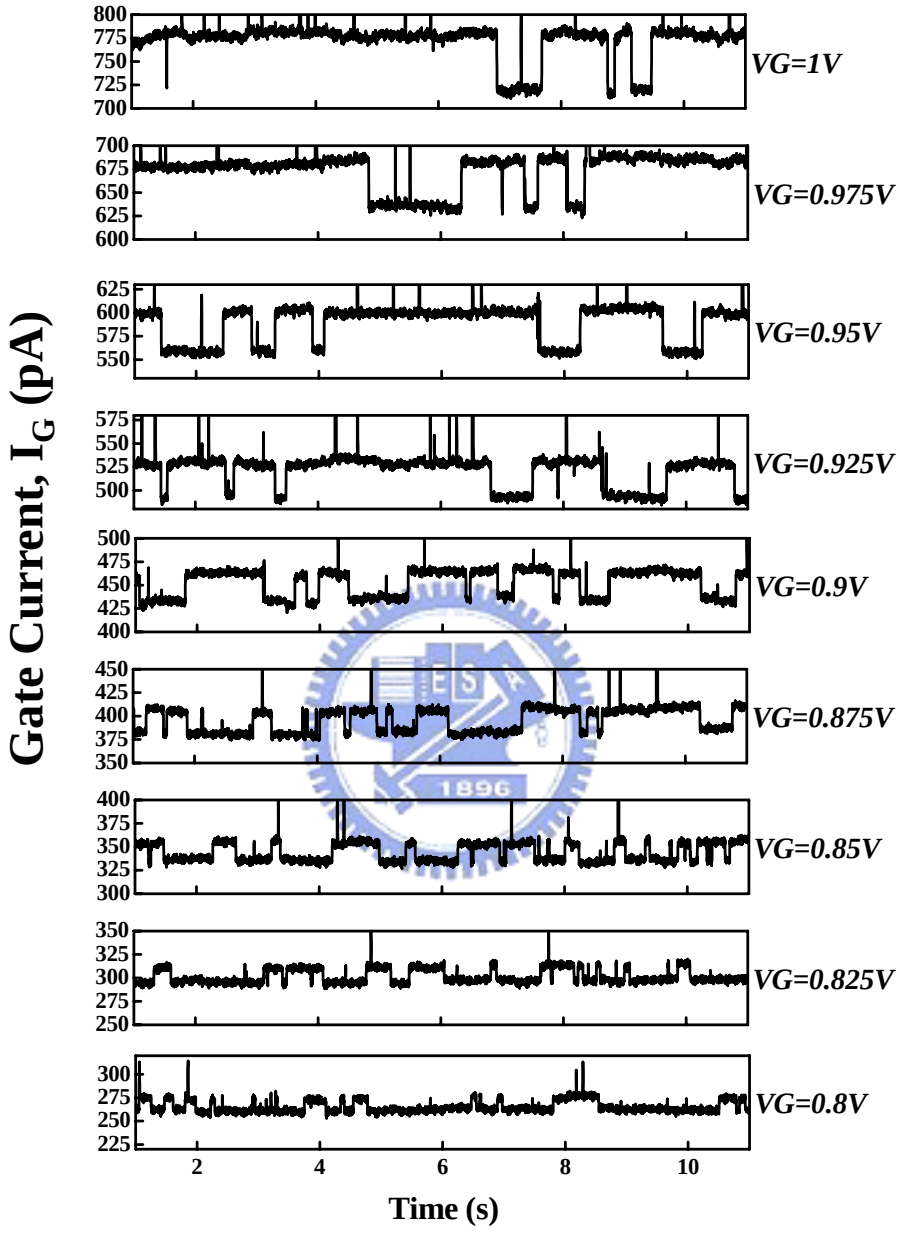


Fig. 3.7 Gate current waveform of high-k nMOSFET with high-field stress induced trap (SIT1), T=25℃

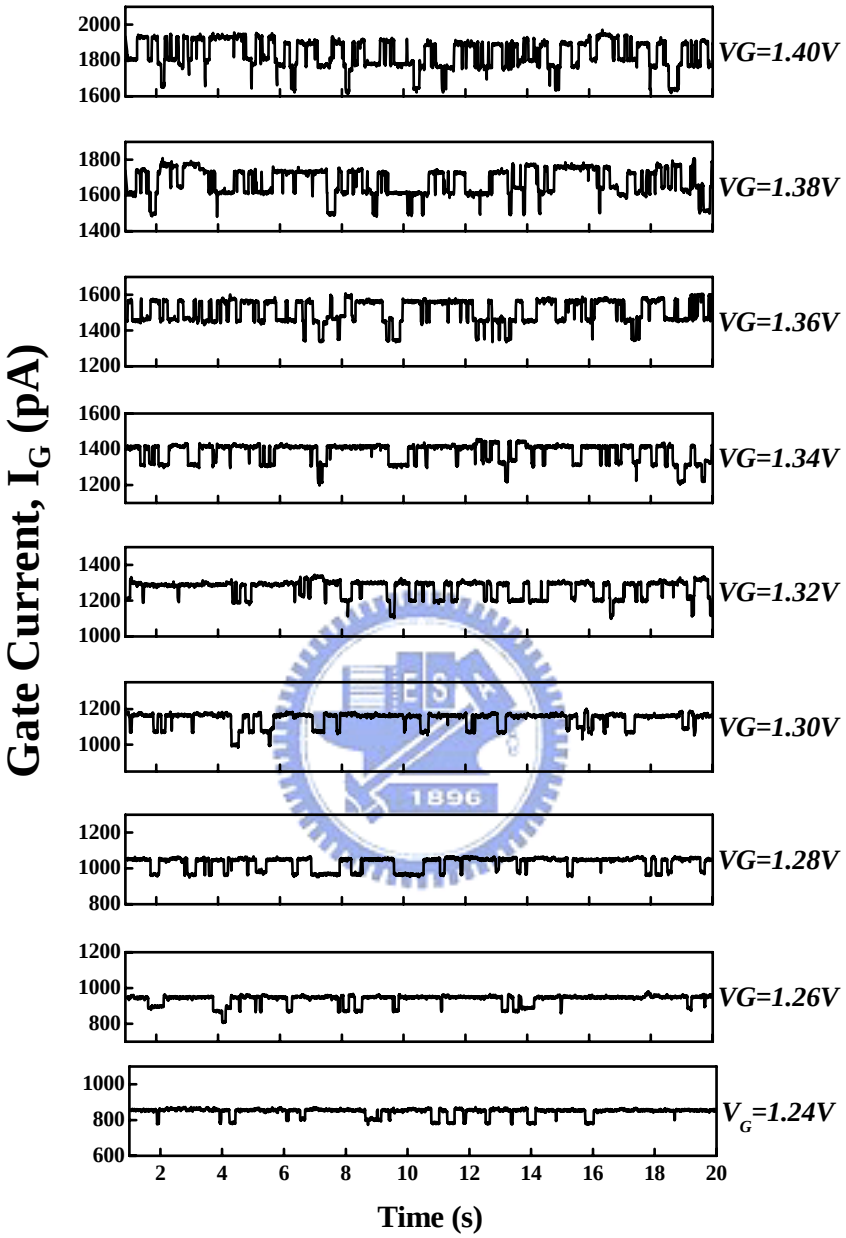
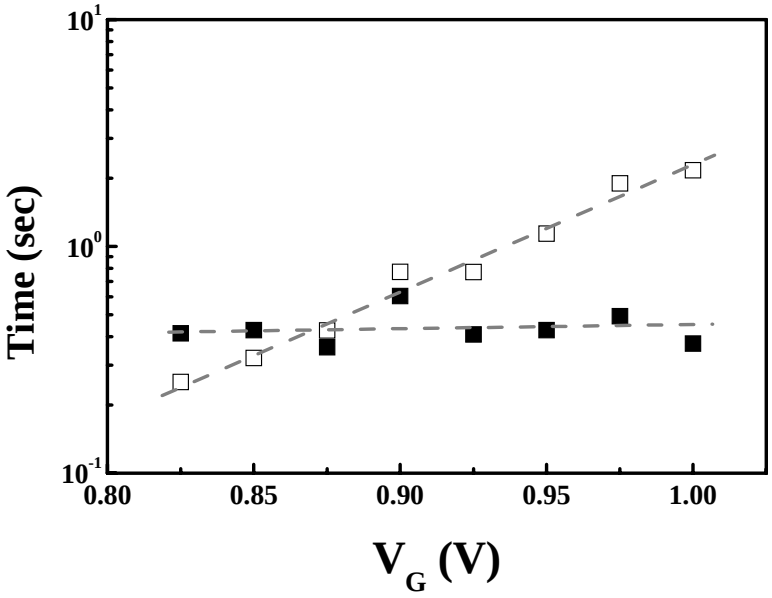
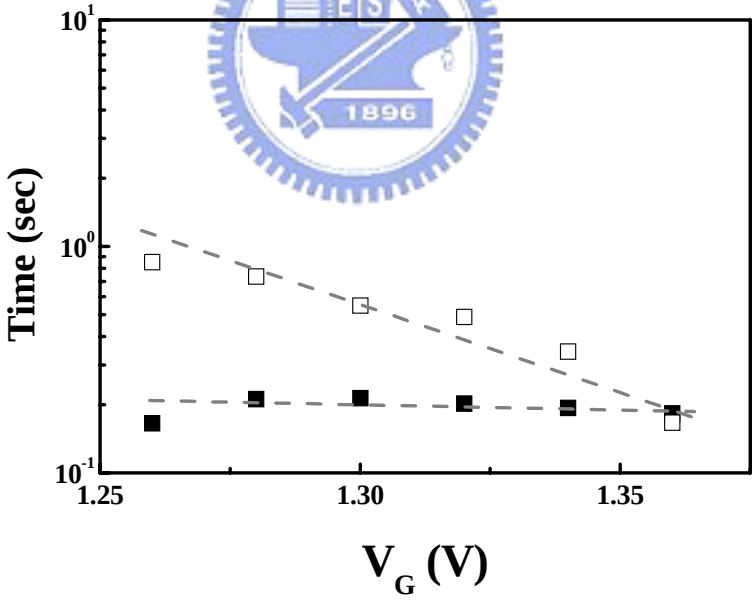


Fig. 3.8 Gate current waveform of high-k nMOSFET with low-field stress induced trap (SIT2), T=25℃



(a)



(b)

Fig. 3.9 Variation of capture time τ_c (open symbol) and emission τ_e (filled symbol) as gate voltage increasing (a) SIT1 (b) SIT2.

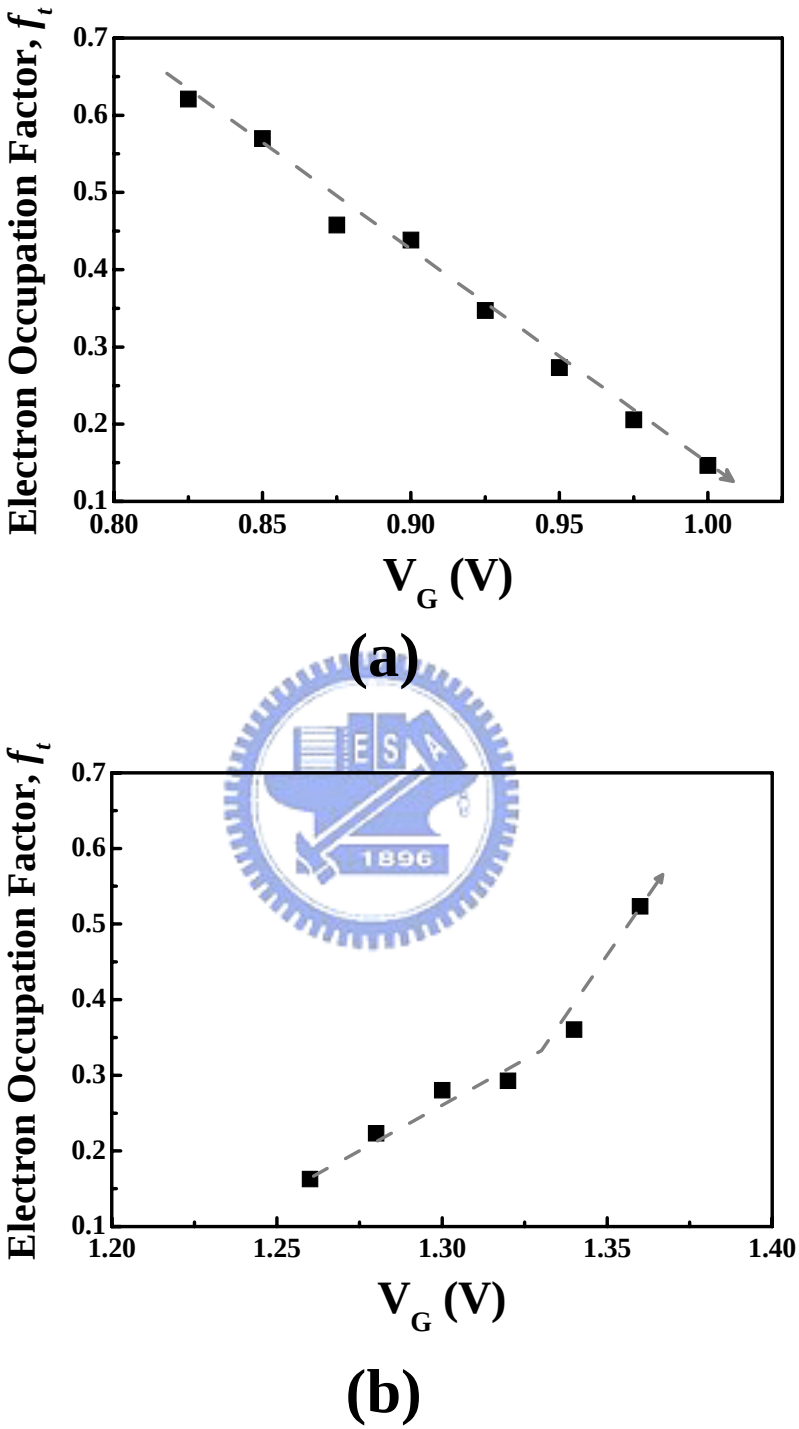


Fig. 3.10 Electron occupation factor versus gate voltage plots, (a) high field stress induced trap (SIT1), (b) low field stress induced trap (SIT2).

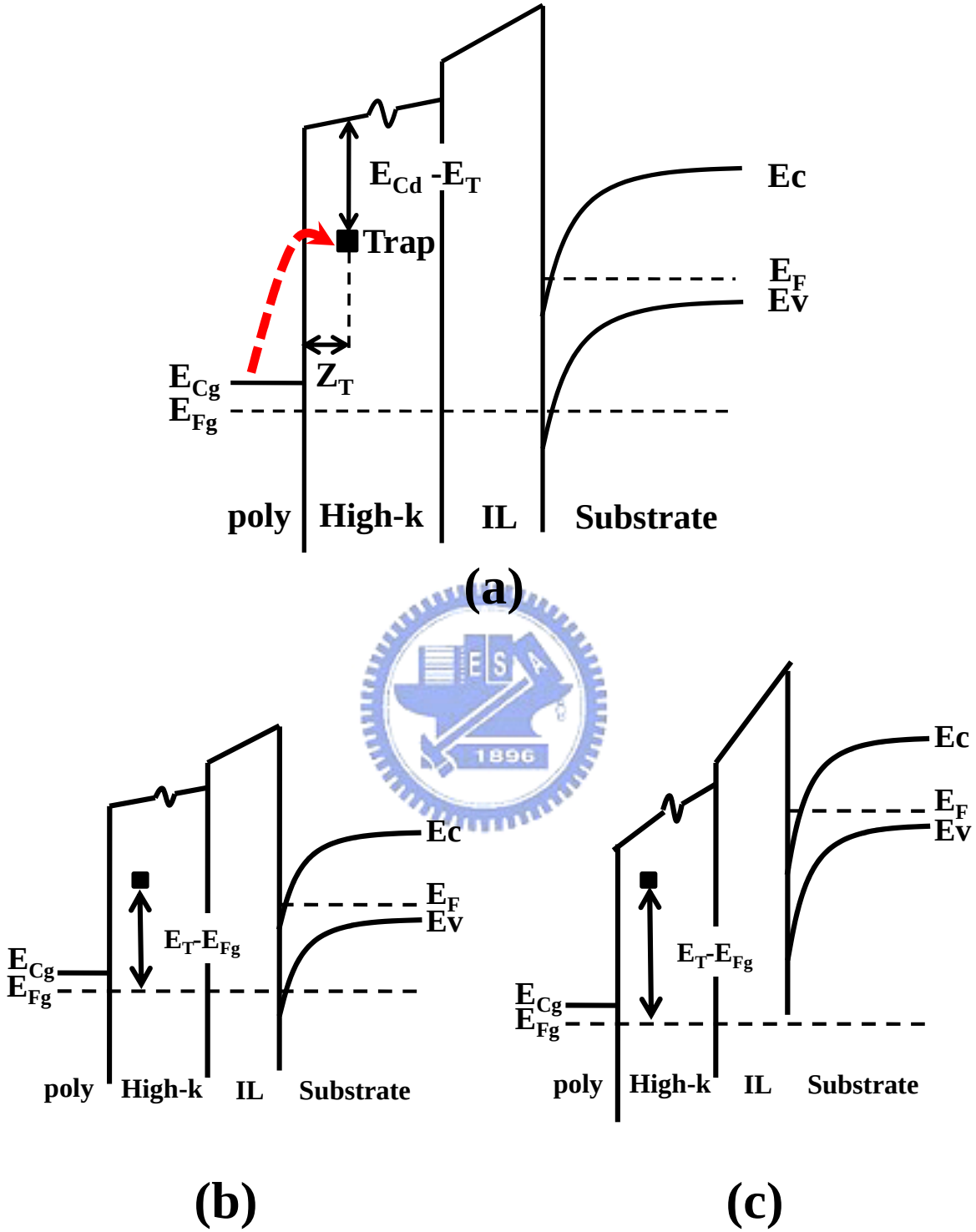
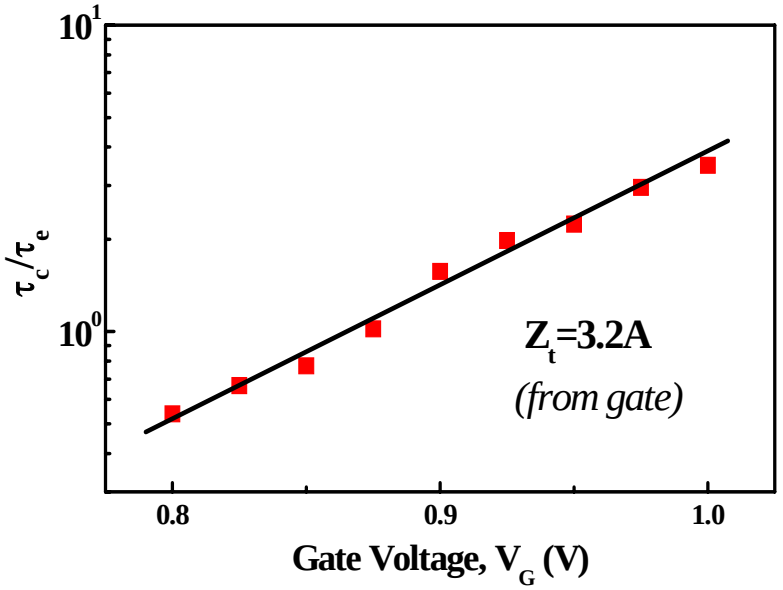
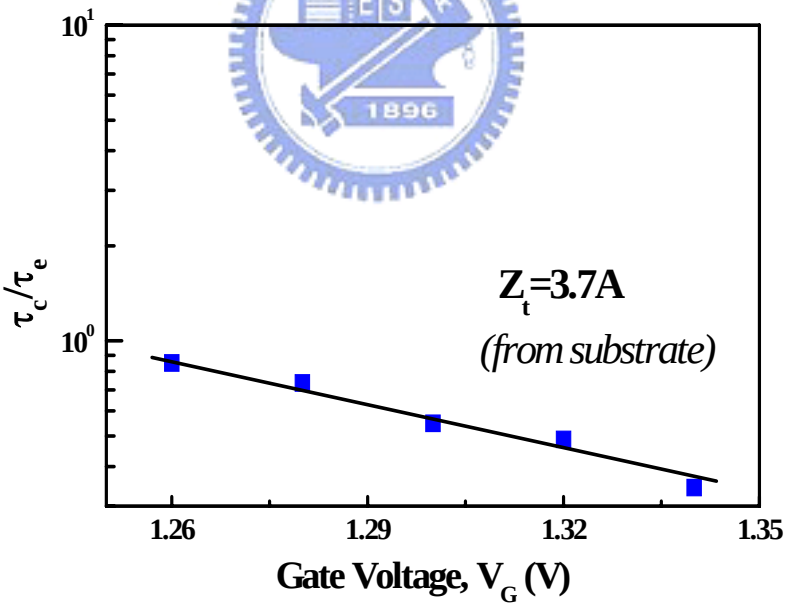


Fig. 3.11 Schematic plots of band diagram in high-k dielectrics MOSFETs. (a) Electrons tunneling from gate model and specific defined parameters, (b) relative trap energy position at low V_G, (c) relative trap energy position at high V_G.



(a)



(b)

Fig. 3.12 Capture time to emission time ratio versus gate voltage plots. (a) high field stress induced trap (SIT1), (b) low field stress induced trap (SIT2).

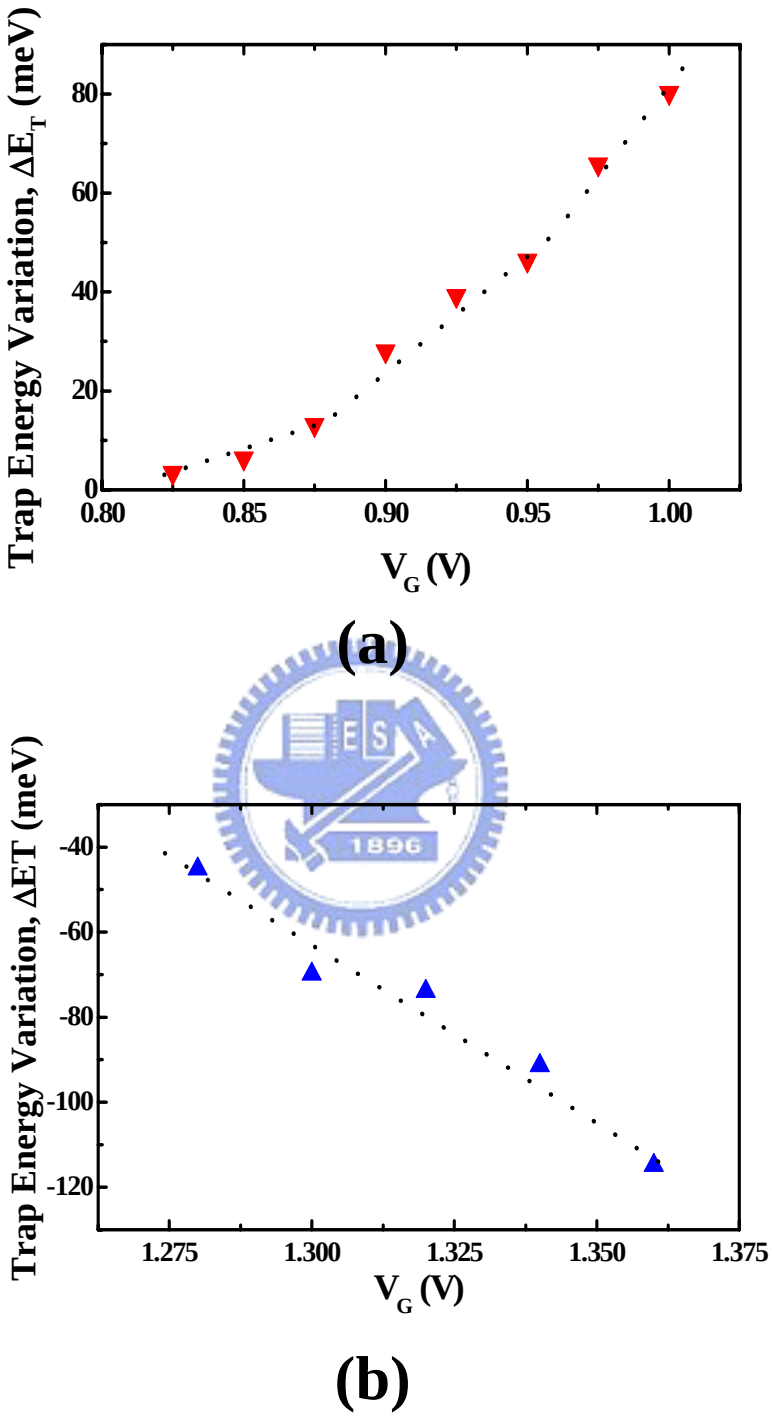


Fig. 3.13 Trap energy variation respect to gate voltage plots (a) positive movement in high field stress induced trap (SIT1) (b) negative movement in low field stress induced trap (SIT2).

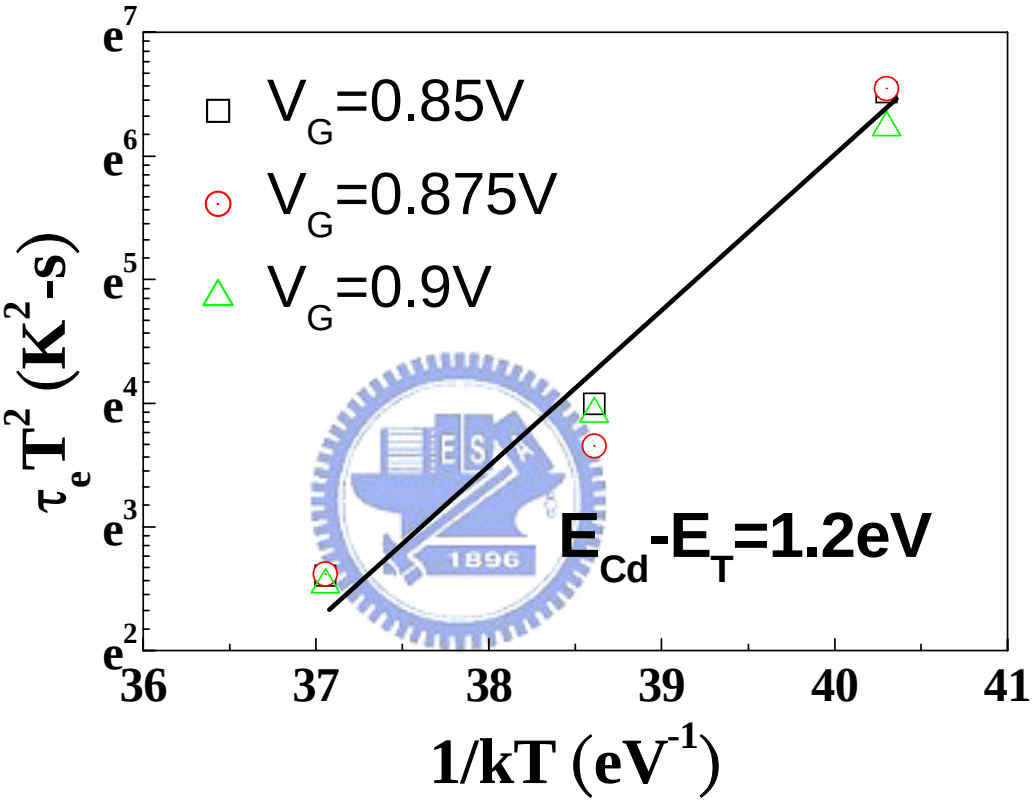
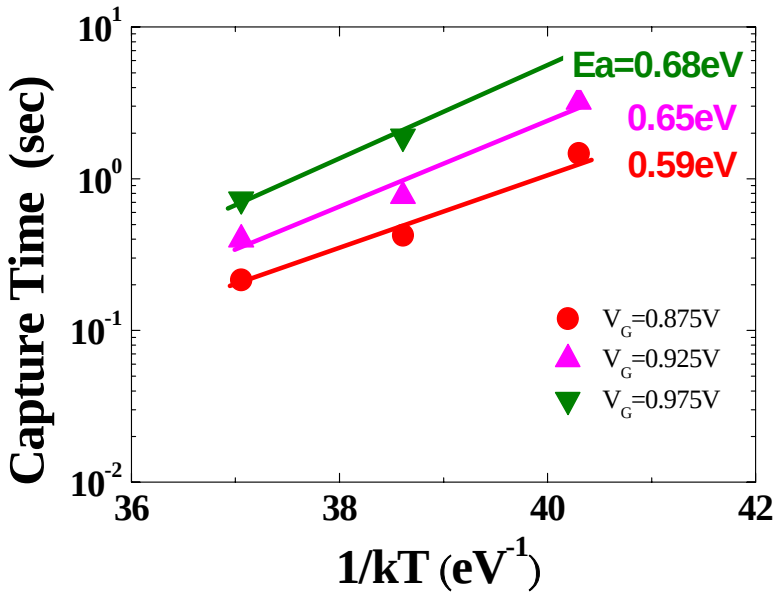
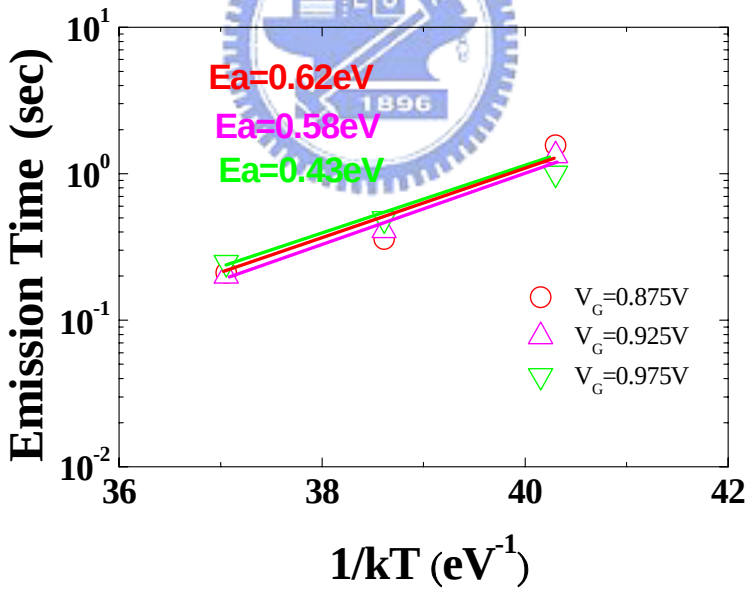


Fig. 3.14 $\tau_e T^2$ versus $1/T$ plots for SIT1. Energy difference between conduction band of dielectric and trap E_{cd}-E_T is around 1.2eV.



(a)



(b)

Fig. 3.15 Dependence of characteristic time to 1/*kT* on distinct gate voltages for SIT1 (a) capture time, (b) emission time. Activation energy E_a is also expressed in the plot.

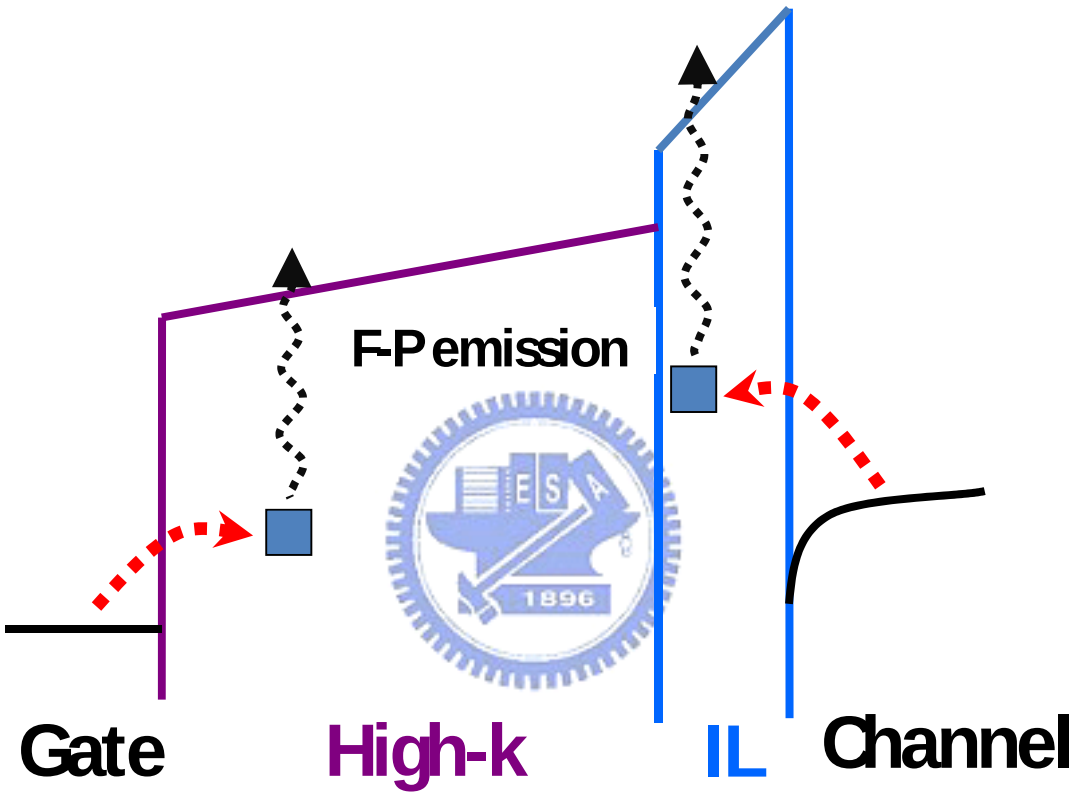
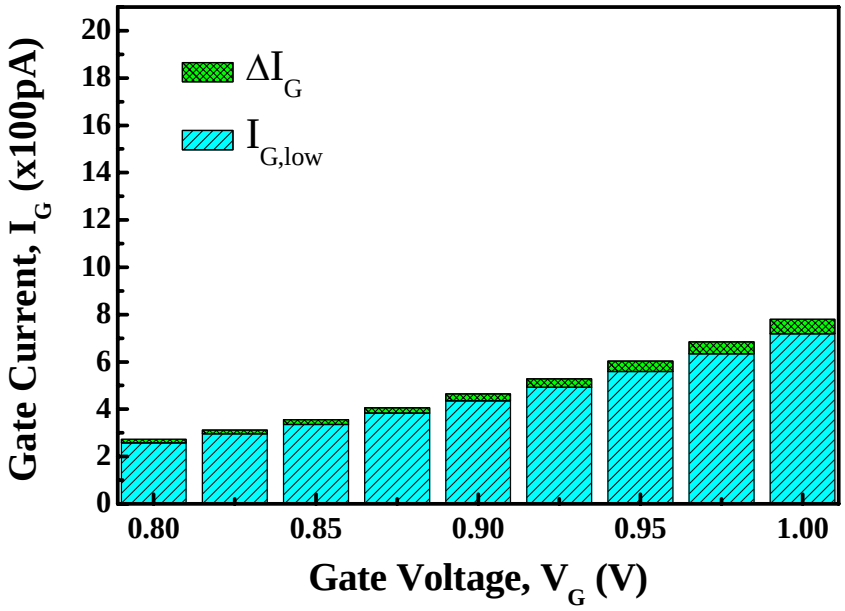
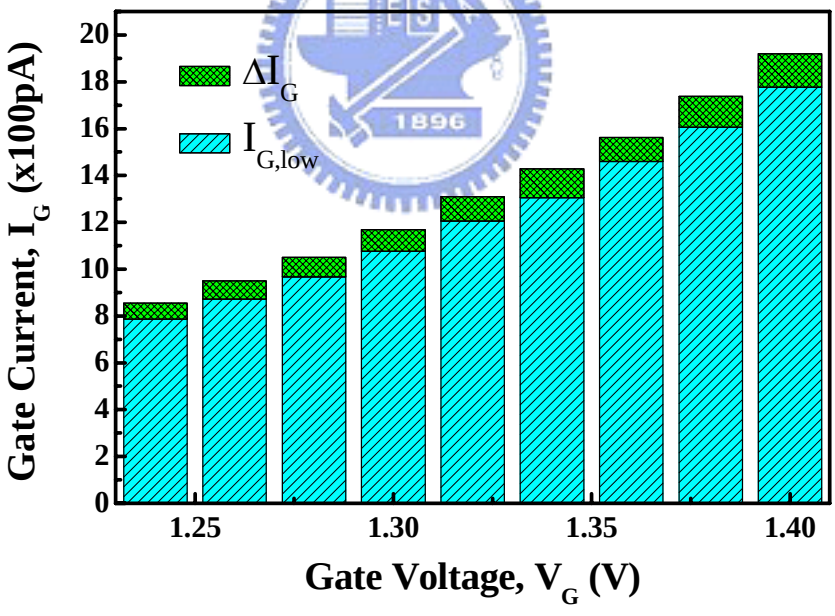


Fig. 3.16 Diagram of electrons captured/emitted mechanism from channel or poly-gate.



(a)



(b)

Fig. 3.17 Magnitude of gate current plot, (a) SIT1 (b) SIT2.

Chapter 4
Random Telegraph Signal of Gate Current for Post Soft Breakdown Devices in High-k nMOSFETs

4.1 Time Dependence Dielectric Breakdown

It has been observed that SiO_2 has strong thickness dependence in terms of intrinsic Weibull distribution [4.1] and the dependence can be explained by percolation model [4.2]. The breakdown failure mechanism in high-k gate dielectrics under constant voltage stress in inversion and accumulation mode is physically analyzed with the aid of high resolution transmission electron microscopy. The results show that the breakdown phenomenon in high-k gate dielectrics is different from that of ultrathin SiO_xN_y and Si_3N_4 gate dielectrics. Dielectric breakdown-induced epitaxy, which is the failure defect responsible for breakdown in SiO_xN_y and Si_3N_4, has also been observed in HfO_2 but in a slightly different morphology. The microstructural damages observed in the breakdown of HfO_2 gate dielectrics are probably related to $HfSi_x$, and $HfSiO_x$, formation during BD event [4.3].

4.1.1 Soft and Hard Breakdown

Hard breakdown of gate dielectrics can be detected by large changes in the voltage or current during stress, while soft breakdown is characterized by smaller offsets in the DC characteristics and an abrupt increase in electrical noise. After constant-current stress, low values of post-breakdown voltage indicate a more abrupt, hard breakdown, while higher values, close to the stress voltage, indicate soft breakdown. An increase is observed in the incidence of soft breakdown as to, decreases, such that hard breakdown is rarely observed for thin gate dielectrics, but dominates the behavior of thicker dielectrics. Additionally, soft breakdown is observed more often when oxides are stressed using lower and more

realistic voltages or current densities. Soft breakdown becomes "softer" and even less abrupt as the thickness or stress is decreased. The characteristic differences between hard and soft breakdown are evident from post-stress I-V curves, with hard breakdown resulting in resistive I-V behavior, while gate current still has an exponential dependence on V, following soft breakdown. For a given thickness, constant voltage testing yields a harder breakdown than constant current stress [4.4]. The post soft breakdown conductance was explained by a multiple trap assisted electron tunneling mechanism in a localized small area of the capacitor. In this model the creation of electron traps in the ultra-thin gate oxide is the most important precursor effect for dielectric breakdown. It was also demonstrated that the ultra-thin gate oxide reliability can be easily overestimated when a constant current stressing is used if the soft breakdown is not taken into account [4.5].

4.1.2 Impact of Soft Breakdown on Device and Circuit Performance

Fluctuations in the gate current directly cause noise at the gate electrode. A series noise-voltage source is required to model the gate noise when the driving impedance is small relative to the gate impedance. The resultant noise across the gate will cause drain-current fluctuations proportional to the gain of the device and the gate current noise can couple directly into the channel. Additionally, the drain-current noise can be modified by correlations between fluctuations in the gate and drain currents. For thicker oxides, the l/f drain-current noise is related to the trapping and detrapping of electrons in the channel. However, in thinner oxides there can be an additional process whereby electrons are captured from the substrate and escape through the gate. This carrier-hopping process causes the gate-current fluctuations and leads to drain-current fluctuations, by modulating the channel potential. Overall, soft breakdown can degrade total device noise in a number of ways, although the precise impact of increased gate noise will depend on the circuit configuration, noise margins, and the device noise prior to soft breakdown. To properly account for these effects, it is essential that gate noise and gate conduction be included in models of devices with ultrathin gate dielectrics [4.4]. Soft breakdown

can produce a strong decrease of the drain current and transconductance in MOSFETs with small width. This effect is due to the formation of a localized oxide damaged region likely trapping negative charge over a large portion of the channel width, around the SB conductive path. The SB impact on the transistor drain current increases as the stress proceeds and the SB current increases, as the damaged region becomes wider due to thermal dissipation and defect generation. The dielectric defects producing the drain current collapse are distributed over a relatively large area, much wider than the area of the SB conductive path evaluated from the QPC model. This effect is evident in devices with small width and fades as width increases. In large width devices, this effect becomes less important as width becomes larger than the damaged region, as in case of electrically stressed components. From the viewpoint of reliability: extrapolations, while evaluating the device lifetime from stresses on MOS capacitors is widely accepted and well justified in case of oxide lifetime evaluation and large width transistors, it may be questionable in MOSFETs with small width.

4.2 I_G RTN in Post Soft-Breakdown Devices

4.2.1 Stress Adjustment

Soft breakdown doesn't happen certainly as stressing continues. It depends on the dielectric thickness, gate area and stress voltage. Hard breakdown rarely appears as gate dielectric scaling down but it still dominates the breakdown mechanism in high-k dielectric MOSFETs due to larger physical thickness of high-k dielectric layer. Compared with high-k layer, the interfacial layer is hard to get hard breakdown and soft breakdown happens normally during stressing for EOT about only 3~4A. EOT of total dielectrics in our devices is only 12A and it's easier to observe soft breakdown appearance, nevertheless it still depends on stress voltage. As experience in our measure, smaller gate area is necessary to gain soft breakdown appearance. Too larger gate area would cause the road of soft

breakdown to hard breakdown shorter and it's difficult to recognize. Breakdown spot happening in large gate area will accumulate the injected carriers and induce more and more breakdown path. It could be avoid in small gate area. Finally, stress voltage is the most critical parameter for soft breakdown observation. Large stress voltage will make dielectrics breakdown faster but it almost hard breakdowns immediately. Adequate small stress voltage is essential but it will need more time to stress aiming at soft breakdown happening. Too small stress voltage would like normal stress and it's not sure to get breakdown appearance. Summarized, it need more tests on different gate area devices and stress voltage and hence some devices will be failure in need.

4.2.2 I-V Characteristics

As aforementioned, constant current stress (CCS) is likely to obtain soft breakdown than constant voltage stress (CVS). We firstly measure I_G-V_G at V_D=V_S=V_B= 0V and choose the magnitude of gate current at V_G= 2.5V as stress condition of CCS. Fig 4.1 shown the evolution of "gate voltage" at I_G= 1.5μA. Measured gate voltage doesn't change at initial stress and soft breakdown happens about T=2300s. After soft breakdown, the digital SBD could be recognized during wear-out. Drain current degrades initially and has no more degradation after stressing time beyond 500s shown in Fig 4.2(a). Beside, gate current lasts increasing during stress. In the beginning, gate current is direct tunneling current, stress induced leakage current (SILC) appears after stress, and gate current has apparent jump from SILC to soft breakdown appearance.

4.3 Result and Discussion

4.3.1 Gate Current Waveform

The magnitude of gate current near operating voltage (V_G= 1.2V) is less than 1nA in former measurement. It increases to several hundreds of nA when devices suffer soft breakdown as shown in Fig. 4.3. Step amplitude is also much larger about 100nA. In the figure, we not only see one large amplitude but also a small noise existing abstrusely whose amplitude is about 25nA. Hence, two SBD paths exist informational by I_G RTN plots. The "on" and "off" of SBD paths involved in gate current plot is shown in Fig. 4.4(a). Four levels of gate current appear and its effect on gate current is very intense that would influence the circuit operation heavily.

The effective area of the conductive region is now given in Fig. 4.4(b) by Eq. 4.1 [4.6], where EOT is the effective oxide thickness. For EOT= 1.2nm and ΔV= 0.16V, the effective area of slow SBD-path is 163nm^2 which is of the same order of magnitude as in other publication [4.6]

$$A = \frac{q}{\varepsilon \Delta E} = \frac{qEOT}{\varepsilon \Delta V} \tag{4.1}$$

4.3.2 Capture and Emission Time

Capture time and emission time after soft breakdown paths existing are shown in Fig. 4.5. Capture time has the same trend that we discussed before as schemed of electrons tunneling from channel. It shows logarithmic decrease with gate voltage stepping up and saturates at about 3 seconds at high gate voltage in T= 20℃. Capture time is lower about one order of magnitude as temperature becoming 40℃ and saturates at 0.8 seconds approximately. On the other hand, emission time is so different with those that we measure in prior sections. It is lower and has same variation with capture time here. Emission time does not only depend on temperature but also gate voltage. The clearer dependence is shown in Fig. 4.6. The activation energy of capture time decreases intensely with gate voltage ($E_{a,capture}$= 0.62eV, V_G= 1.4V; $E_{a,capture}$= 0.22eV, V_G= 1.55V). Compared with capture time, the activation energy of emission time varies slightly and fits with process and stress induced traps as results that activation

energy of emission is lower at high gate bias.

4.3.3 Model

As shown in Fig. 2.16, 2.17, 3.15(b) and 4.6, emission time prior to soft breakdown is independent of gate voltage and hence it is irrelevant to electric field over dielectrics and channel carriers density. After soft breakdown, gate dielectrics suffer heavy destroyed and large amount of traps generate. The spot is a capacitor prior breakdown paths appearing and a short circuit after breakdown. There are a conductive path existing and make current flow through without a barrier. Fig 4.7 presents the trap is distributing in 0.93eV below the conduction band of dielectrics and it's roughly identical with process and stress induced traps. Nevertheless the fit lines in $\tau_e T^2$ versus $1/kT$ plots gradually move upward after soft breakdown. Emission time is dependent with parameters as shown in Eq. 4.2. The Capture cross section σ is assumed as a constant at small gate bias variation prior to SBD but it's not true after SBD. In section 2, Eq. 2.10 also can be represented as below. The intersection with Y-axis in $\tau_e T^2$-$1/kT$ plots means electron capture cross section σ multiplying with pre-factor γ ($-\sigma\gamma$). Prior to SBD, the lines in $\tau_e T^2$-$1/kT$ plots have same slopes and intersection with Y-axis, that it means E_{Cd}-E_T is fixed and capture cross section is independent of gate bias and temperature. After SBD paths existing, E_{Cd}-E_T is roughly identical at distinct gate bias. Nevertheless capture cross section varies with gate bias. It shows capture cross section is smaller at high gate bias. The cause comes from large traps generation after SBD and it would change the area and probability of electron capture. Capture cross section increases at large gate bias and it enhances SBD paths area active for capture electrons.

$$\tau_e = \frac{\exp\left[\left(E_F - E_T\right)/k_B T\right]}{g\sigma v n} \tag{4.2}$$

$$\ln \tau_e T^2 = -\ln \gamma\sigma + \left(E_{Cd}\text{-}E_T\right)/kT \tag{4.3}$$

Frankle-Poole emission is a factor besides the gate voltage that affects the conduction band bending and only dependent of the trap energy distribution. In conclusion, the traps distributing near soft breakdown paths will capture and emit electrons as soft breakdown appearance in devices and it will aplenty induce the current through conductive paths.

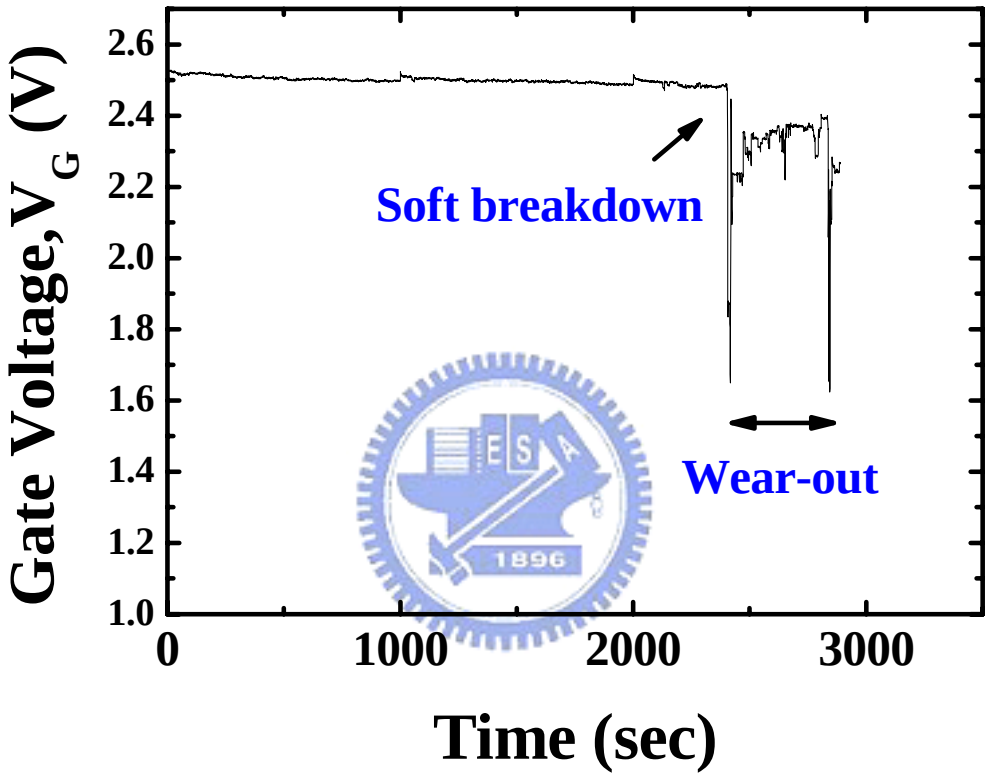


Fig. 4.1 Evolution of gate voltage as the device suffered stress. Soft breakdown occurrence and wear-out are represented in the plot.

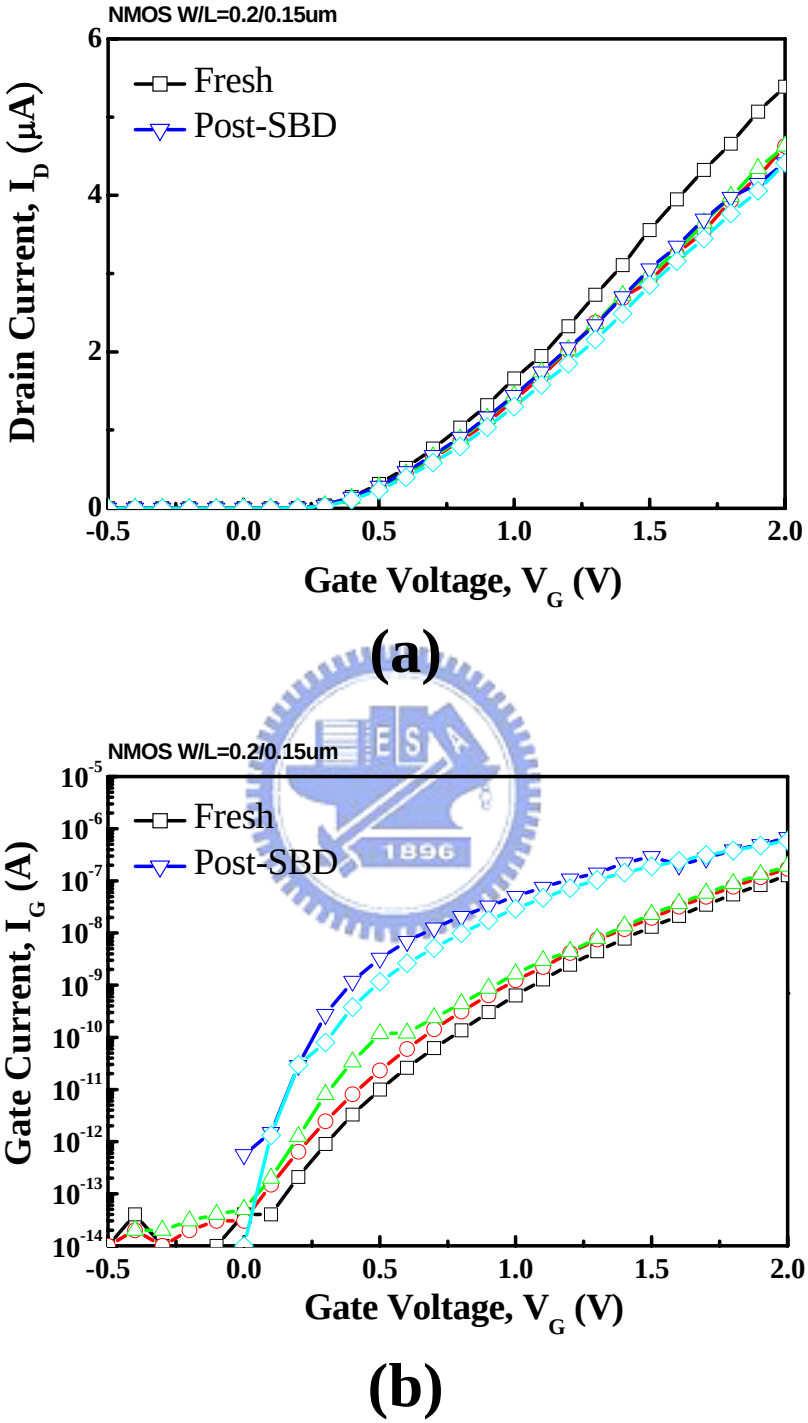


Fig. 4.2 Gate and drain current versus gate voltage plots. Open square is the fresh one and an inverted triangle is post soft breakdown one.

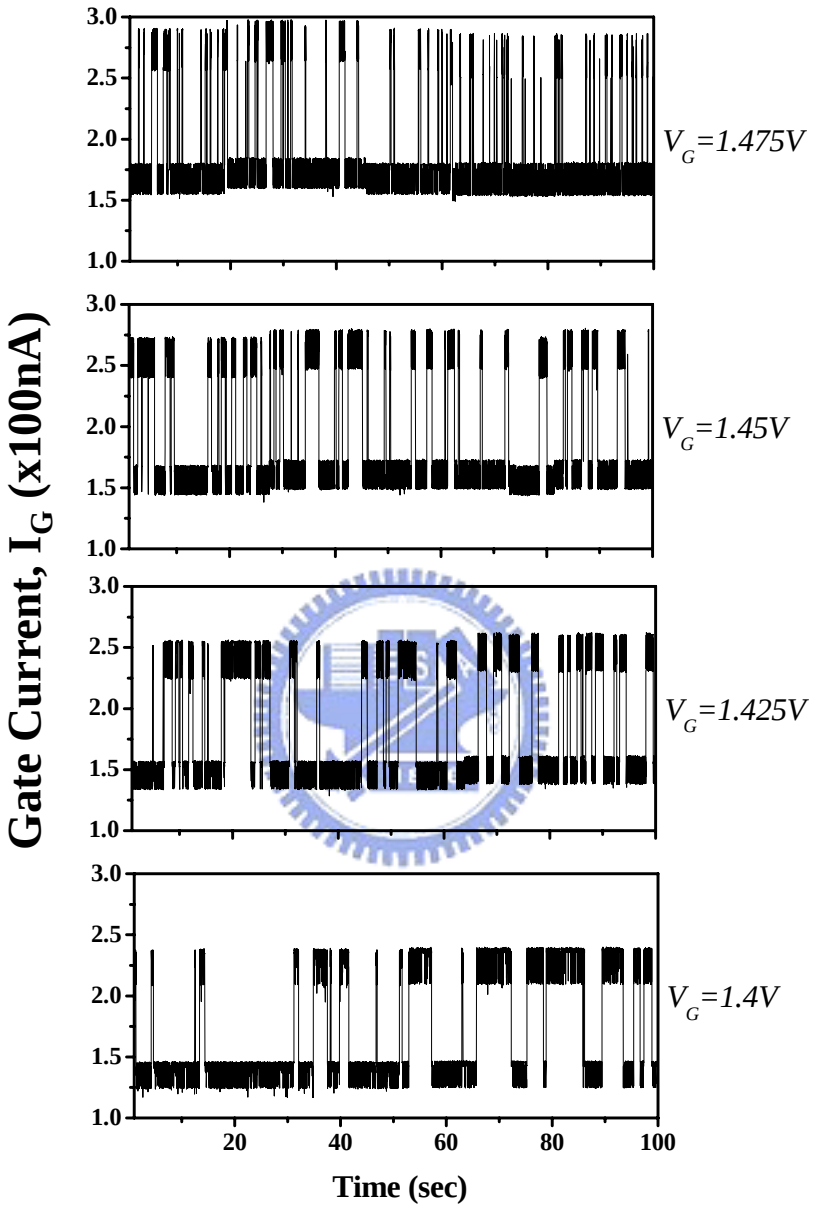
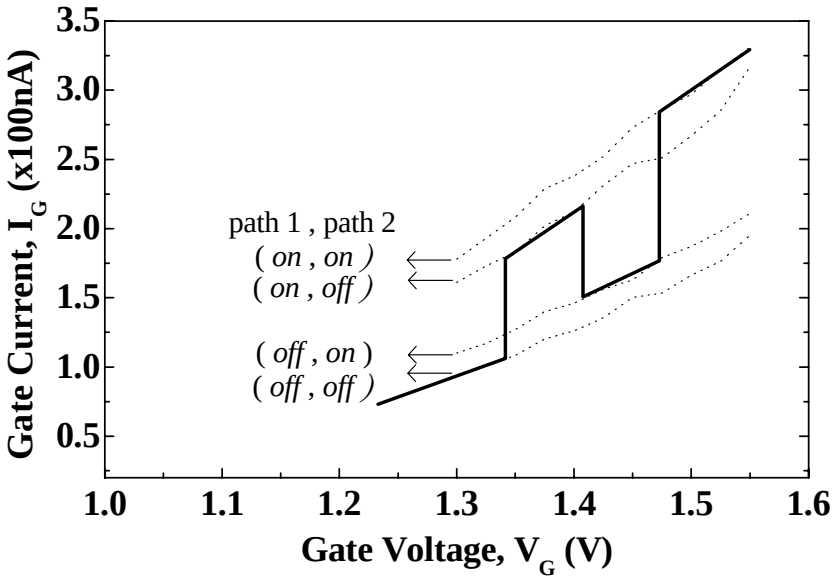
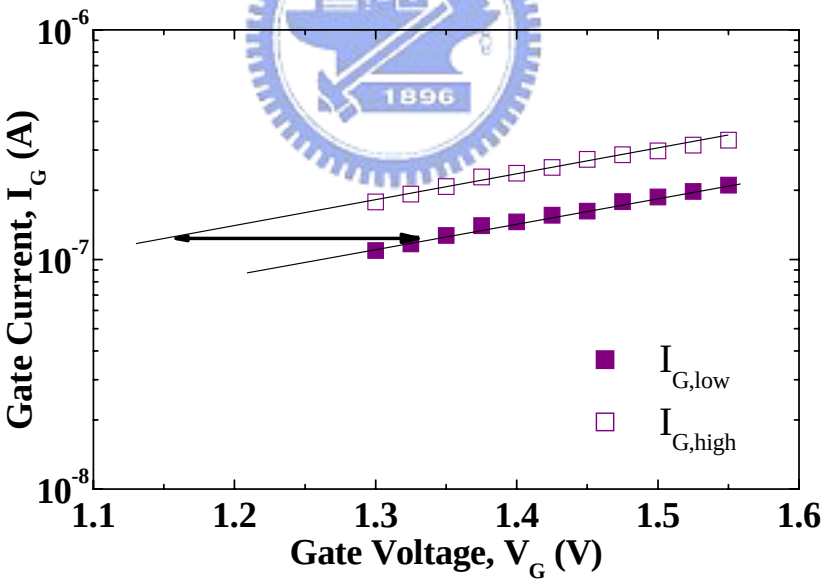


Fig. 4.3 Gate current waveform at different gate voltage during V_G=1.4V to 1.475V. Four levels of gate current are obviously shown and two SBD paths exist.



(a)



(b)

Fig. 4.4 (a) Relation of SBD paths switch to gate current.

(b) Low and high conductive state involved with gate current versus gate voltage plot. ΔV between $I_{G,low}$ and $I_{G,high}$ is 0.16V.

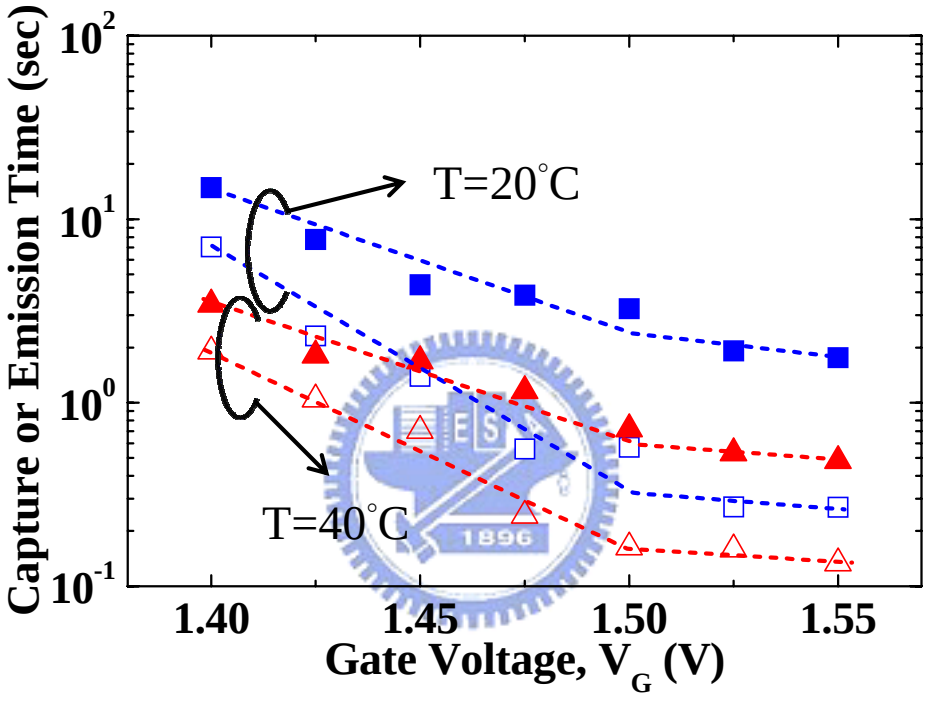
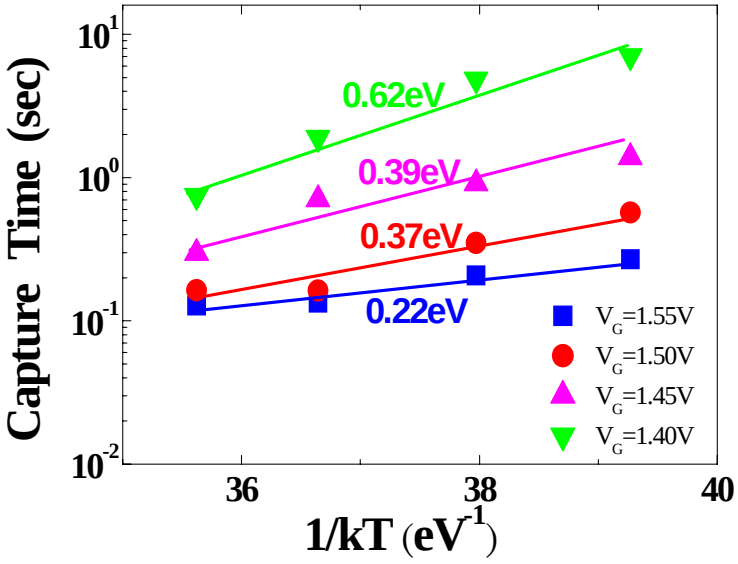
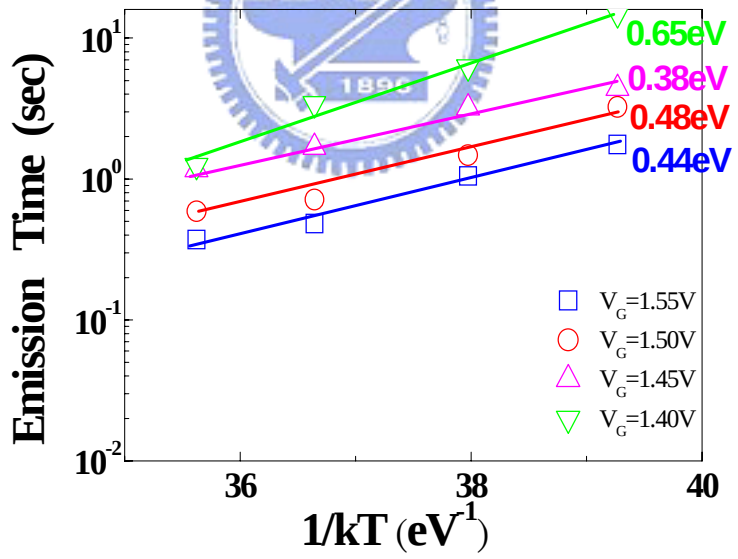


Fig. 4.5 Dependence of capture time (filled symbol) and emission time (open symbol) versus gate voltage plot.



(a)



(b)

Fig. 4.6 Temperature and gate voltage dependence of (a) capture time and (b) emission time. The activation energy is extracted from the slope of log(Time) to 1/kT plot.

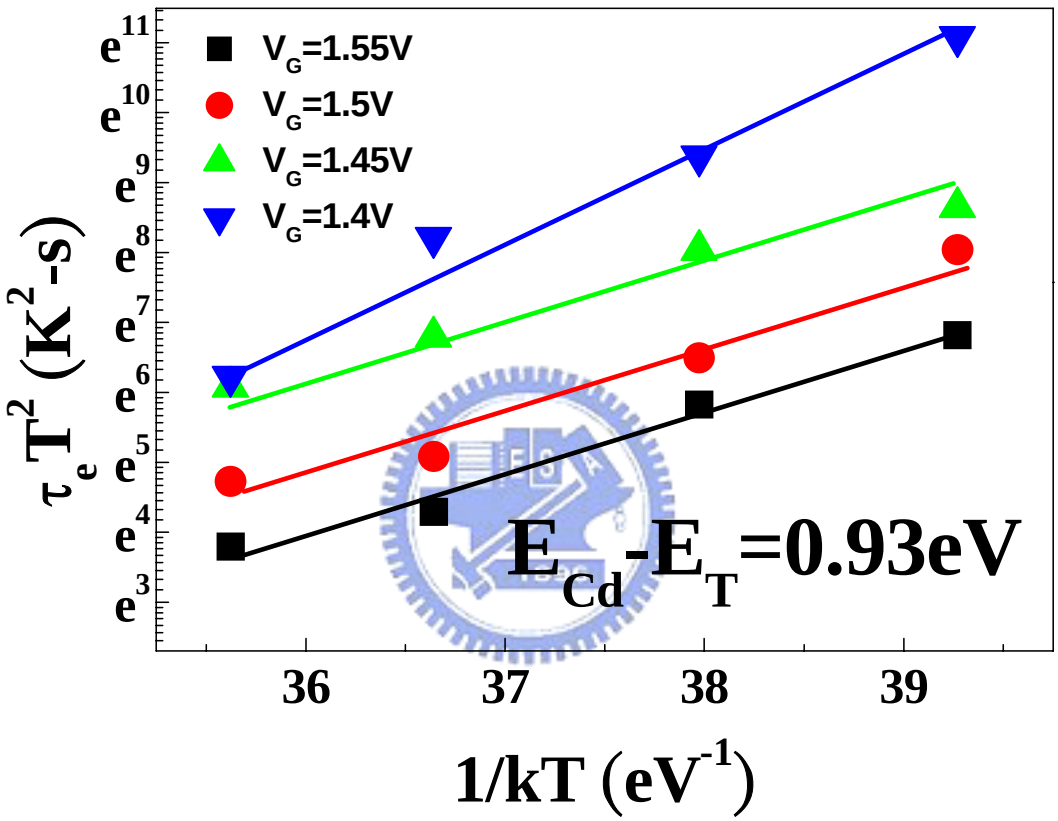


Fig. 4.7 $\tau_e T^2$ verus 1/kT plots at different gate voltage during V_G=1.45V to 1.55V. All the plots have the same scale and E_{Cd}-E_T from the slopes is 0.93eV approximately.

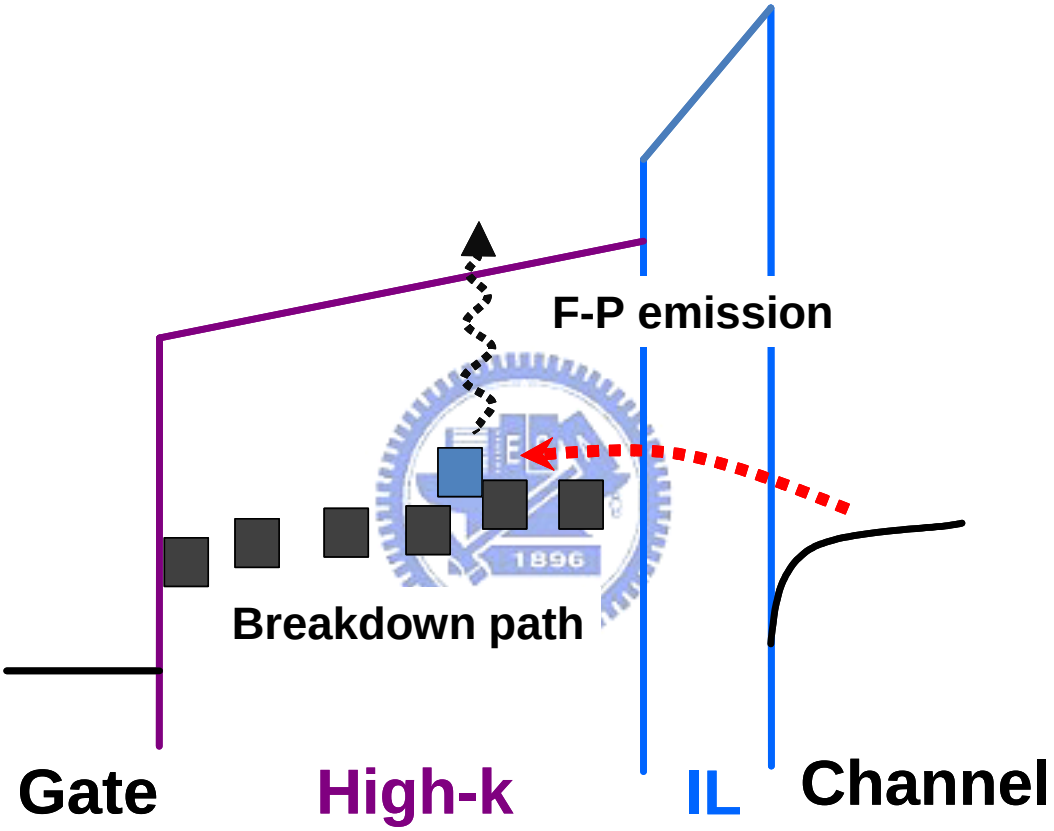


Fig. 4.8 Schematic plot of band diagram post SBD. Breakdown path occurs and near SBD path trap will capture/emit electrons. Emission is through Frankle-Poole emission.

Chapter 5
Summary and Conclusion

The gate current instability is further studied in this thesis and the behaviors of electrons trap/trapping are analyzed. The method “Gate current random telegraph noise” is arranged coherently for our experiments. Through electric field and temperature dependence, we could understand the physics behind the RTN phenomenon in distinct extent destruction.

Firstly, a new I_G RTN method has been successfully implemented to identify the location of traps generated in high-k and interfacial layer. Traps site in high bulk layer that results trap energy level variation less that in interfacial layer. Then, different electrons tunneling mechanism (from the substrate or gate) can be observed for devices under high-field or low-field Fowler-Nordhiem stress. The depth extraction has also been finished by varied equation. Both PIT and SIT site in about 1eV below the conduction band of dielectric. The temperature dependence of capture and emission time indicate activation energy of capture time will decrease with gate bias as electrons are sourced from channel and increase as electrons from poly gate. Emission is independent with electron source and also decreases with gate bias.

Furthermore, application of the method to SBD reveals that capture and emission time are so different from PIT and SIT. The SBD provides larger electron capture cross section with gate bias that would both influence capture and emission time. An extra leakage path in high-k as a result of breakdown can be well estimated in terms of the size of breakdown path.

In conclusion, this I_G RTN method is an effective and direct tool for the diagnosis of generated traps in CMOS with high-k dielectrics and we more understand the physics and the behaviors in high-k dielectrics for distinct extent destruction.

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