國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

新穎的功率電晶體於熱載子效應之特性化分析及模型建立

Characterization and Modeling of Novel Pseudo-Drain(PD) RF Power CMOS under Hot Carrier Stress

研 究 生：陳 勝 杰

指導教授：張 俊 彥 博士

中華民國九十七年九月

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研究生：陳勝杰　　Student：Sheng-Jay Chen
指導教授：張俊彥 博士　　Advisor：Dr. Chun-Yen Chang

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摘要

在最近幾年，先進的CMOS技術已經成熟的應用在射頻RF (radio-frequence)這塊領域上面，像是無線通訊系統、藍芽技術的應用、WLANs以及超寬頻(ultra-wide band)等等。而微波元件又是通訊系統中最重要的骨架。當中又以矽爲基底的金氧半場效電晶體已經成爲射頻元件的主流。

整合的功率放大器對於SOC的應用上相當重要，因此發展適用的功率電晶體是必須的。而功率電晶體則需要可以承受較高的崩潰電壓以達到傳送較高能量和附加功率效能的功用。但傳統CMOS技術的缺點就是限制住輸出的崩潰電壓，這對於RF方面的應用而言，是一種矛盾的關係。所以一些文獻提出了改進的方法，諸如Drain-extended MOS (DEMOS)以及Lateral-Diffused MOS (LDMOS) transistors都可以提高崩潰電壓，但是他們在高頻特性的表現上面，卻沒有這麼地理想。

於是我們利用UMC的製程技術，從DEMOS的結構上去改變以達到改善的效果。而這新的元件命名爲Pseudo-drain MOS (PDMOS)。本篇論文的重點即是討論這顆改善後新元件的直

流特性和高頻特性，並將其結構做些改變，再將改變前後的兩個不同結構深入比較受到熱載子效應後的直流特性和高頻特性以及功率特性方面的行爲，更進一步分析在熱載子效應下的可靠度比較。

最後，透過小訊號模型的建立，經由討論各別小訊號參數的變化情形，我們發現金氧半場效電晶體的互導，汲極到源極的電阻以及閘極到源極的電容還有汲極的電阻受到熱載子效應影響較大，特別是汲極電阻的變化，也輔助說明了這兩種不同結構在直流特性上的差異性。

Characterization and Modeling of Novel Pseudo-Drain (PD) RF Power CMOS under Hot Carrier Stress

Student: Sheng-Jay Chen Advisor: Dr. Chun-Yen Chang

Institute of Electronics
National Chiao Tung University

Abstract

In recent years, advanced CMOS technologies have been investigated and pushed to perform well in RF areas, like in wireless systems: Bluetooth applications, WLANs and UWB (ultra-wide band). Microwave transistors are the backbone of these modern wireless communication systems. Since the Si-based MOSFETs (metal-oxide-semiconductor field-effect transistors) have become the mainstream of RF transistors in recent years.

The integration of the power amplifier for SOC realization is very important. Hence, the development of suitable power cells using MOS transistors is necessary to achieve this goal. Power transistors with high breakdown voltage are required to achieve higher power delivery and power added efficiency (PAE). But, the drawback of CMOS technology is the inherent limitation of a lower output breakdown voltage, and it is incompatible for RF power applications. Therefore, some literatures which addressed this issue introduced devices like the “Drain-extended” MOS (DEMOS) and the “Lateral-Diffused” MOS (LDMOS) transistors to obtain a higher breakdown voltage and power performance. However, the high frequency characteristics were degraded.

In this thesis, we improved the performance from DEMOS by UMC technologies. And the new device is named Pseudo-drain MOS (PDMOS). The purpose of this thesis is to investigate the DC characteristic and RF characteristic of this new RF MOSFETs and then we do some variation on structures. Besides, we compare to go deep into the DC characteristic, RF

characteristic and power performance which suffer hot carrier stress on different structure from changing before and after. Then we try to analyze the reliability under hot carrier stress.

Finally, by way of building a small-signal model, we proposed that individually parameter after hot carrier HC stress, the transconductance(g_{m0}), drain-to-source resistance(R_{ds}), gate-to-source capacitance(C_{gs}), and drain resistance(R_d) suffer more degradation after HC stress. Especially the variation on drain resistance(R_d) could explain the difference between these two structures for their DC characteristics.

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Chapter 1

Introduction

1.1 *RF Transistors*

Currently RF electronics is one of the fast growing parts of semiconductor industry. This is due to explosive growth in the wireless communication market in the past 10 years. However about twenty years ago, this situation was much different. During that time, RF electronics was somewhat mysterious and their applications had been mainly military (e.g. secure communication, electronic warfare system). In the 1990s, the situation changed dramatically. The new global political situation has led to considerable cuts in military budgets. Furthermore, a shift to consumer applications took place, and consumer applications clearly became dominated. Therefore, the design philosophy for many microwave systems changed from “performance at any price” to “sufficient performance at lowest cost”. Microwave transistors are used in a large number of different circuits such as low-noise amplifiers, power amplifiers, mixers, frequency converters and multipliers, attenuators, and phase shifters. Although the requirements on transistor performance differ from application to application, microwave transistors in principle can be distinguished into two groups as small-signal low-noise transistors and power transistors. For microwave electronics, on the other hand, a large variety of different semiconductor materials have been employed, such as Si, SiGe, GaAs, InP, further III-V compounds, and wide bandgap materials [1-3]. In the few years, the silicon-base MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) have become the mainstream of RF transistors.

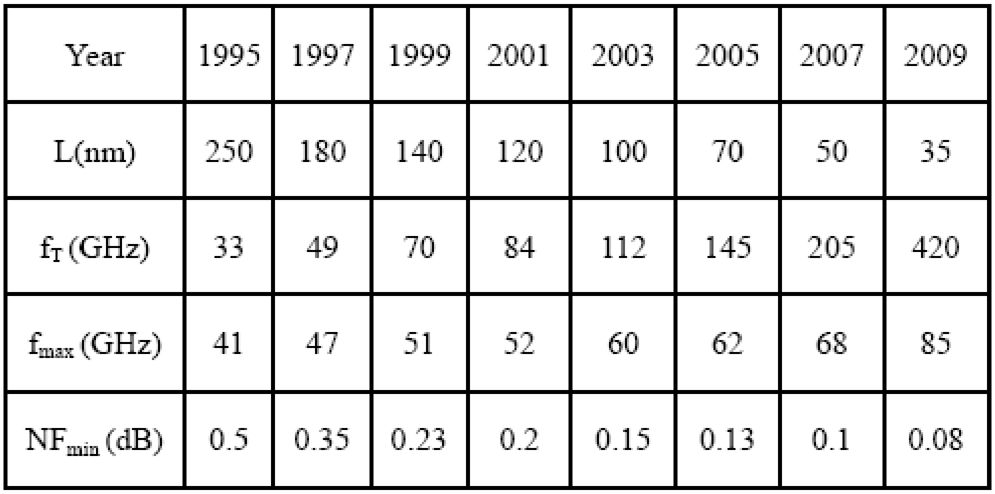
Silicon technology is inherently superior compared to compound semiconductor technologies in terms of cost, compact size, and short time-to-market [4]. Recently, advanced CMOS technologies have been successfully used in RF transceiver systems for Bluetooth, WLANs, and UWB (ultra-wide band) applications. The integration of the power amplifier for these systems is a logical next step for SOC realization. Hence, the development of suitable power cells using MOS transistors is necessary to achieve this goal.

1.2 *Basic Concepts of RF MOSFET*

In the past 20 years, the silicon base MOSFET had widely been used in VLSI (Vary Large Scale Integration) applications. However, most RF circuits and systems have been implemented either compound semiconductor transistors. This is because that the microwave properties of silicon base MOSFET is inferior to other high-frequency transistors. In recent years, with the fast growth in the wireless communications market, the demand for high performance and low cost RF solutions is rising. Fortunately, the continuous down-scaling CMOS technology has resulted in a strong improvement in the RF performance of MOS device [5]. The basic structure of the MOSFET, shown in Fig. 1-1, consisting of a single gate, a semiconductor substrate and a heavily doped source and drain region, has not changed in the past twenty years. Only the dimensions and other features have been scaled down continuously to meet the demands of higher speed and increased compactness. There are several criterions to determine RF MOSFET performance such as cut-off frequency, maximum oscillation frequency, power gain, linearity, and noise figure. Table 1-1 shows the cut-off frequency, maximum oscillation frequency and minimum noise figure versus the gate length of n-channel MOSFET. For today, 50- to 100-nm gate length, the cut-off frequency and maximum oscillation frequency can achieve almost 200GHz and 70 GHz, respectively. The NF_{min} for 70nm gate length RF MOSFET can be reduced to 0.13dB. In addition, very high power gain (>25dB) is possible at realistic current for the most advanced technologies [6]. The VIP3 of 70nm gate length can be lower than 0.81V [7]. Therefore RF MOSFET has been serious alternatively to the traditional microwave transistors. Moreover, MOSFET offers very large scale integration and high reliability. As a result, to realize systems-on-chip, the RF operation must use RF MOSFET to conform to the integration.

1.3 *Hot Carrier Reliability of RF MOSFET*

With the scaling MOS transistor technology, the hot-carrier (HC) reliability becomes a challenging concern while keeping a relatively high drain voltage for both the digital and analog applications. Hot carrier generation and their effects in the characteristics of MOSFET have been known for a long time [8-10]. This results from high electric fields present inside the MOSFET which naturally appears when high biasing voltages are applied to a short-channel device. The general damages from the hot-carriers include the shift of the threshold voltage, the drain current degradation and the decreasing of transconductance. Because the RF circuits are sensitive to the parameters of their components [11], HC effects are also important in RF circuit design.



Year	1995	1997	1999	2001	2003	2005	2007	2009
L(nm)	250	180	140	120	100	70	50	35
f_T (GHz)	33	49	70	84	112	145	205	420
f_{max} (GHz)	41	47	51	52	60	62	68	85
NF_{min} (dB)	0.5	0.35	0.23	0.2	0.15	0.13	0.1	0.08

Table 1-1: Performance of CMOS technology in several generations

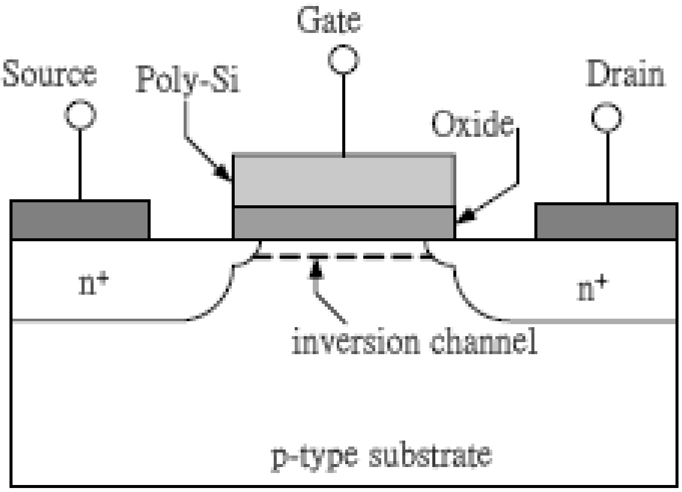


Fig. 1-1: Schematic of a typical bulk MOSFET structure

Chapter 2

Basic Theory and Experiments

2.1 *Hot Carriers Mechanism*

Hot Carriers result from the high electric fields inside the MOSFET when high biasing voltages are applied to a short-channel length device. Electrons in the inversion layer can get high energies in the high electric field. It is possible that carriers with high energy (i.e. hot carriers) have sufficient energy to overcome the potential barrier between the silicon and silicon dioxide and penetrate into the gate oxide. Some of the carriers may get stuck inside the gate oxide at the defect sites or traps, denoted by N_{ox}. Hot carriers also can break the atomic bonds at the interface of the silicon substrate and the gate oxide then generate new traps which called the interface traps. We denoted these traps by N_{it}. The difference between these two types of traps is that interface traps can be in charge exchange with channel whereas the oxide traps cannot be in direct charge exchange with charges in the channel. These two types of traps will degrade the quality of gate oxide and affect the device electric parameters.

As shown in Fig.2-1(a), when the MOSFET is operated in the saturation region, the channel electrons will gain high energy on their way from source to drain and penetrate into gate oxide. The hot carriers are called channel hot electrons (CHE). The event of a carrier gaining energy and entering the gate oxide is a statistical phenomenon. The maximum numbers of hot carriers which penetrate into gate oxide occur when $V_G \cong V_D$ [12]. Another effect that caused by energetic carriers in the channel is that carriers on the way toward drain collide with lattice atoms and generate new electron-hole pairs. These electron-hole pairs can also gain high energy in the electric field and produce new electron-hole pairs. This is similar to avalanche process in a reversed biased p-n junction and called drain avalanche hot-carriers (DAHC) (as shown in Fig.2-1(b). During the same process, the energetic carriers can impinge on the atomic bonds at the interface of the substrate and gate oxide or inside the oxide, and then break them. Therefore new electronic states N_{it} are created at the interface. In an NMOSFET, the extra electrons generated in avalanche process are absorbed by drain, and the extra holes are absorbed by substrate terminal which form the substrate current component I_{sub}. It is known that generation of electron-hole pairs in an avalanche process is proportional to both strength of electric field and the number of primary carriers initially flowing in the channel. For low values of V_G above the threshold, the transistor is in deep saturation and a pinch-off region is formed near the drain which results in a strong lateral electric field in that region. Also, at low values of V_G the drain current is low. As V_G increases, the drain current increases, but transistor comes out of saturation region gradually. This causes that a maximum value for I_{sub} appears at some particular value of V_G. It is reported that at $V_G \cong \frac{1}{2} V_D$ the maximum I_{sub} is generated in MOSFET [13].

The third mechanism of hot carriers is called substrate hot electrons (SHE). Unlike the cases in CHE and DAHC, which were caused by lateral electric field in the channel, SHE is caused by the vertical electric field between gate and the substrate. As shown in Fig 2-2(c), the electrons which are thermally generated in the region below the gate, drift toward the silicon-silicon dioxide interface and gain kinetic energy in the electric field below the gate. Some of these electrons penetrate into oxide and cause a uniform distribution of trapped charge in the oxide. SHE is not a major problem in short channel devices as compared to the long channel devices. Since most of the electrons are absorbed into source and drain region and a smaller fraction of them reaches the device surface.

2.2 *Oxide Breakdown Mechanism*

Generally, in advanced MOS devices, there are two breakdown mechanisms observed in dielectric materials. First is called HBD (Hard-Breakdown) and has a permanently distortion in gate oxide dielectric. It results in a dramatic increase of the output currents due to the increasing gate leakage current. The other breakdown mechanism is called SBD (Soft-Breakdown), and the breakdown process shows smoothly and slightly. The physical mechanism involved in, and leading to, the dielectric breakdown process are very complex. They involve impact ionization in the oxide layer, injection of holes from the anode, creation of electron-hole pairs in the oxide, electron and hole trapping, creation of surface state at the oxide-silicon interface, and the interaction of many or all of these process.

The mechanism of tunneling into an electron trap can be explained by Fig.2-2(a). As electrons tunnel into an oxide layer, some of the electrons can get trapped. The trapped electrons modify the oxide field so that the field decreased near the cathode and increased near the anode. Hence the tunneling current will reach a stable value in Soft Breakdown.

As electrons travels in the conduction band of an oxide layer, it gains energy from the oxide filed. If the voltage drop across the oxide layer is larger than the band-gap energy of silicon dioxide, the electron can get enough energy to cause impact ionization. As shown in Fig.2-2(b), when a tunneling electron arrives to the anode, it could cause impact ionization in the anode near oxide-anode interface. Depending on the energy of the tunneling electron, the hole thus generated could be from deep down in the valence band, and thus could be “hot”. A hot hole in the silicon–oxide interface have a high probability of been injected into oxide layer. On the other hand the injected hole can be trapped in the oxide layer as it travels towards the cathode.

The trapped holes in the oxide layer resulting in an increase in the oxide field near the cathode and a decrease in the oxide field near the anode (shown in Fig.2-2(c)). According to the F-N tunneling equations [14]:

$$J_{FN} = \frac{q^3 E_{ox}{}^2}{16\pi\hbar\Phi_{ox}} \exp\left(-\frac{4\sqrt{2m^*}\Phi_{ox}{}^{\frac{3}{2}}}{3\hbar q E_{ox}}\right) \qquad (2\text{-}1)$$

a small increase in the oxide field near the cathode can cause a large increase in the tunneling current. Thus, hole-trapping in oxide near the cathode provides positive feedback leading to the electron tunneling process. Dielectric hard breakdown occurs when the positive feedback leads to a run away of the electron tunneling current at some local weak spots of the oxide [15]. It appears as a current prominence in current-versus-time plots.

2.3 *Device under Test and Measurement Techniques*

2.3.1 *Device under Test*

The devices under test are n type MOSFETs in N-well. Multi-finger MOS transistors used in this work were fabricated using a 0.13μm baseline technology with channel length *L*= 0.13μm. In our structures, two cells are parallel and each cell have 16 fingers with fingers width L_F= 4μm. The gate oxide thickness is 22Å.

2.3.2 *I-V Measurement*

The DC characterizations and stress experiments of RF MOSFET were performed using

Agilent 4156B precision semiconductor parameter analyzer. The threshold voltage (V_{th}) and transconductance (g_m=dI_D/dV_G) are extracted from the I_D-V_G curve.

2.3.3 *High Frequency Characteristics Measurement*

For microwave devices, the high frequency characteristics are generally obtained by the measurement of the s-parameters. In this work, on-wafer s-parameters measurement was carried out from 0.1 to 50.0 GHz using microwave coplanar probes and HP 8510C Network Analyzer. On-wafer dummy structures were used to de-embed the pad parasitics. Then, the de-embedded parameters were transformed to the H, Z or Y parameters to extract the desired parameters.

2.3.4 *Output Power Measurement*

We used the load-pull system (ATN LP1 measurement system) to measure and discuss power characteristics and linearity in our study. The functions of this load-pull system perform power discussions on output power, power gain, power added efficiency (PAE), and inter-modulation distortion. The configuration of a load-pull system is shown in Fig.2-3(a).

By load-pull test, the output power is measured and plotted as a function of the complex load seen by the transistor. Since a complex load requires two axes, the plot actually appears as constant power contours on a complex impedance plane, for example, a Smith chart. A variable, precisely calibrated tuner operates as a matching network, presenting various complex impedances to the transistor according to a control input. With the aid of an automated system, the real and imaginary parts of Z1 are gradually varied such that the power meter maintains a constant reading. The result is the contour corresponding to that power level shown in Fig.2-3(b). When Z1 arise so does Zin, necessitating the use of the tuner between the signal generator and the transistor to ensure that the impedance seen by the generator remains constant.

If the power delivered to the input is constant, the output power increases as Z1 approaches its optimum value, Zopt. This trend is accompanied by a narrower range for Z1, resulting in the tighter contours and eventually a single impedance value, Zopt, as the output reaches its maximum level, Pmax. In other words, the load-pull test systematically narrows downs the values of Z1 so as to obtain both the maximum output power and corresponding load impedance. The load pull system can also calculate intermodulation distortion using two-tone frequency test.

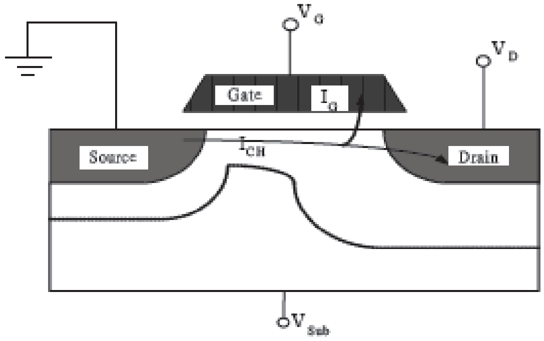


Fig. 2-1 (a)

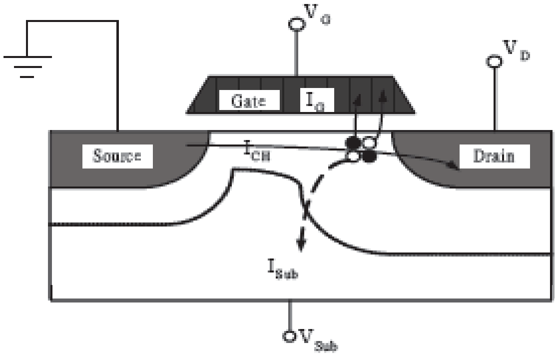


Fig. 2-1 (b)

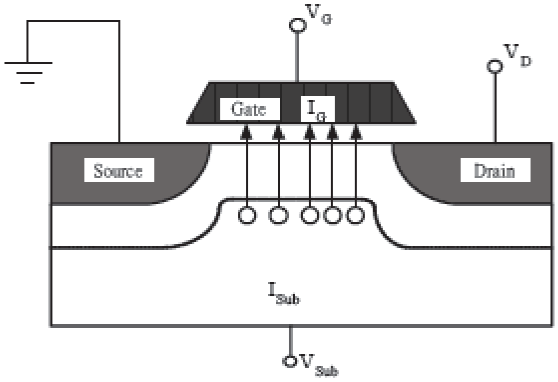


Fig. 2-1 (c)

Fig. 2-1 (a) Channel hot electrons (b) Drain avalanche hot carriers (c) Substrate hot electrons

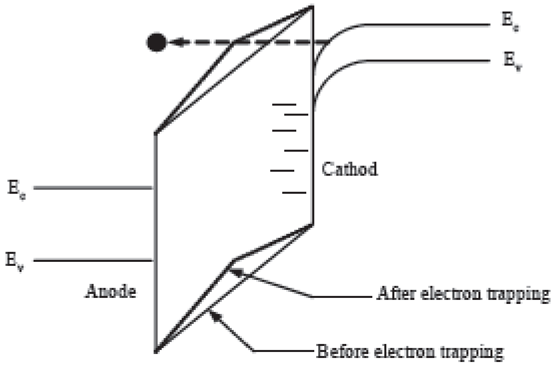


Fig. 2-2 (a)

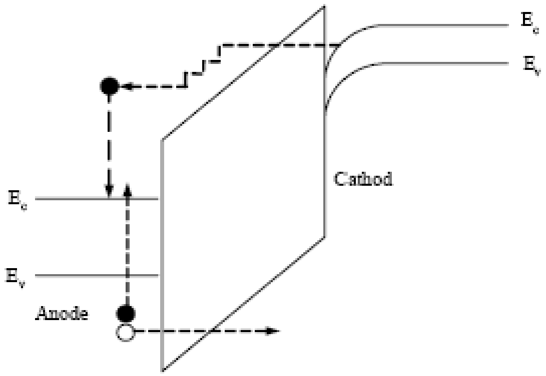


Fig. 2-2 (b)

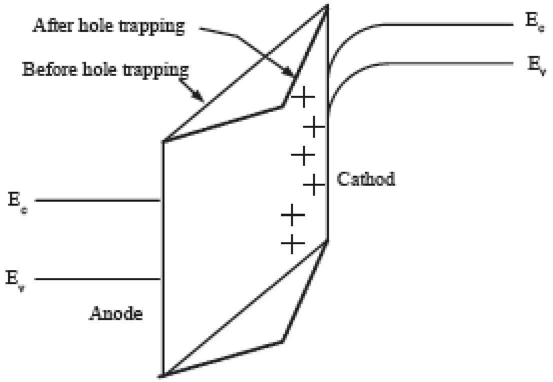


Fig. 2-2 (c)

Fig. 2-2 (a) Schematic illustrating the trapping of tunneling electrons. (b) Schematic illustrating the generation of an electron-hole pair in the anode by a tunneling electron.(c) Schematic illustrating the trapping of holes in the oxide layer

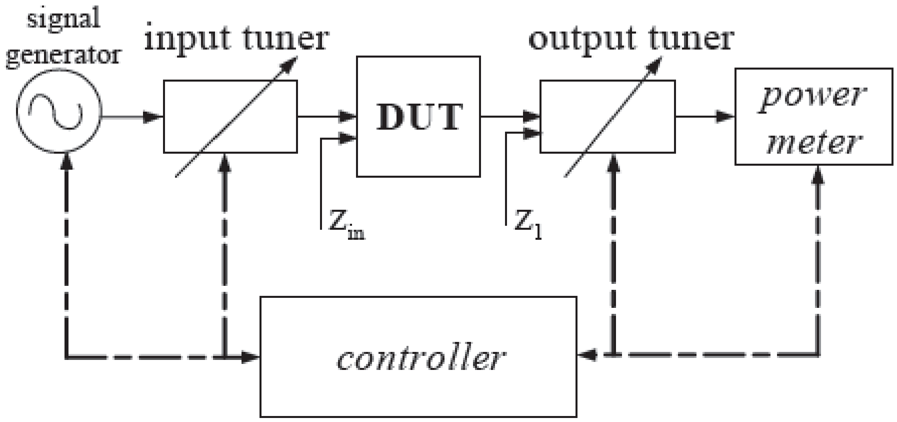


Fig. 2-3 (a)

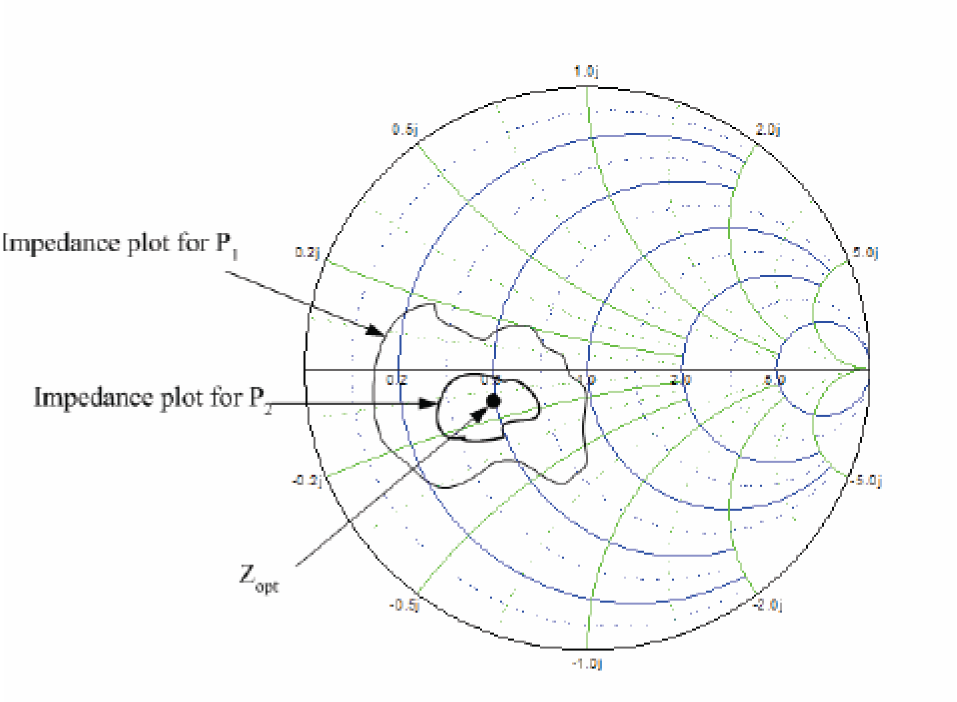


Fig. 2-3 (b)

Fig. 2-3 (a) Block diagram of the load-pull measurement system. (b) Power contours on a Smith chart

Chapter 3

The DC & RF characteristics on RF power transistors

Introduction

In this chapter, a new structure named pseudo-drain MOS (PDMOS) [16] was introduced and investigated. PDMOS improves from a standard Drain-extended MOS (DEMOS). We also make some changes from PDMOS and compare their DC and RF characteristics. Although the BV_{DS} in DEMOS is higher than in PDMOS, the speed and RF performance of the PDMOS is better than that of the DEMOS.

3.1 *Device Fabrication and Design*

The structures under test were fabricated using a standard 0.13μm CMOS process with 22-nm-thick gate oxidation and twin-well technique. Without any additional mask, the device was designed by layout scheme as shown in Fig.3-1(b). The drawn geometry of a single-cell has 16 fingers with a 0.13μm gate length and 4μm gate width. For multi-cell design, 2 cells were parallel to reach higher output current and lower gate resistance.

The DEMOS which shown in Fig.3-1(a) was designed simply with an n-type well structure extending underneath the STI (0.12μm) to the internal drain region of the device adjacent to the actual poly gate. Due to the lateral diffusion caused by the successive thermal treatments inherent in the process, this relatively lower dose N-well ($\sim 10^{18} cm^{-3}$) becomes a high resistance (n^-) drift region and can be regarded as a "series-wound" connection between the channel and drain diffusion region. This drift region acts as a drain-extended (DEMOS) as shown in Fig.3-1(a). In PDMOS, we added an N^+ region to keep the lightly doping N-well extended drift region away from the channel. Therefore, the influence of the (n^-) drift well region on the device channel region can be minimized. This is one of the key features of the device which improves the g_m significantly and resulting in a superior high frequency performance.

3.2 *Compare with DC Performance*

Two structures named HV01 and HV02 were discussed in this study. In HV01, the drawing N-well was located under the STI and drain (as shown in Fig.3-2(a)). In HV02, the N-well diffusion located Source diffusion to half (as shown in Fig.3-2(b)). Fig.3-3 shows the subthreshold characteristics of RF power PDMOS transistors with two different structures. Since the intrinsic gain of a transistor is highly depended on g_m, the higher g_m, the more attractive the device is for analog/RF applications. In addition, it can be observed in Fig.3-3 that not only is the g_m high for PDMOS, but the leakage current (I_{off}) is also suppressed to a level as low as a conventional core-NMOSFET. The low leakage current will result in lower power consumption when the PDMOS is in the off-state.

3.3 *Compare with RF Performance*

3.3.1 *Experimental Procedures*

High-Frequency characteristics were measured on chip using the HP8510 network analyzer from 20MHz to 50GHz. After de-embedding the parasitic pads effects, the current gain h_{21} was calculated to extract the cutoff frequency (f_T) which is one of the main figures-of-merit (FoM) of transistors with different drain biases. Another key RF FoM, maximum oscillation frequency

($f$max), was also calculated and extrapolated from the maximum available gain (MAG). In this Pseudo-Drain MOS transistor, the gm is less influenced by extended drift region than in the DEMOS transistor, so that the high-frequency performance of f_T (82GHz) is comparable to a conventional 0.13μm NMOS transistor, and the RF performance on Pseudo-Drain MOS transistor is better than the Drain-extended MOS.

3.3.2 *RF Performance*

In this study, the bias dependences (f_T) and (f_{max}) in our designed structures (HV01 and HV02) are shown in Fig.3-4(a) and Fig.3-4(b). It was obvious in that picture that the gate biases at peak (f_T) or (f_{max}) were different between HV01 and HV02. This was owing to the different transconductance (g_m) behaviors between them. And the HV02 exhibits higher f_T and f_{max} than those of the HV01 transistors with increasing stress time.

3.3.3 *RF Power Performance*

For RF power circuit design, f_{max} is the key FoM of a power transistor for high frequency response. The f_{max} should be 5~10 times higher than the operation frequency of RF power circuits and the parameters in a power device which influence f_{max} should be taken into account. Fig. Fig. 3-5 shows a typical power amplifier with an intrinsic device model. Using this schematic of a RF power amplifier, the dominant factors that influence f_{max} can be gleaned from the power gain vs. frequency response equation corresponding to this model. The RF power gain is associated with the inherent current gain and the output impedance. When the source and load impedances are matched for maximum output power, the available power gain can be calculated and expressed as:

$$Ga,\max = \frac{{f_T}^2}{4f^2(2\pi f_T R_G C_{GD} + \frac{R_G}{R_{DS}})} \qquad (1)$$

where R_G, C_{GD}, R_{DS} are gate resistance, gate-to-drain capacitance, and output resistance in the device model. The comparison of the model parameters of HV01 and HV02 is summarized and listed in Table I. It was found that the better transconductance (g_m) of the HV02 transistor was the dominant factor contributing to the improvement of both the cutoff frequency ($f_T = g_m / 2\pi C_{gg}$) and the maximum oscillation frequency. The RF power performance of the PDMOS transistor is also better than that of the HV02 as shown in Fig. 3-6. This is all due to the HV02 structure, in which the N-well diffusion located Source diffusion to half to let the drain current concentration higher.

Fig. 3-6 shows the measured output power, power gain and power-added efficiency (PAE) of HV01 and HV02 under the bias condition of V_G=1V and V_D=1.2V, at a frequency of 2.4GHz, and with the total width of 128μm at 2.4GHz. Using the load-pull system, which consists of HP85 122A and ATN LP1 (power parameter extraction software). The source and load impedances were tuned for maximum output power. For load-pull measurements, the operating frequency was chosen at 2.4GHz, a frequency commonly used in wireless communication. The maximum values of output power and power gain in this HV01 and HV02 structure can reach more than 11 dBm and 12 dB, respectively. The PAE, which gives an indication of the efficiency and power consumption, can also be 47% for the HV02 transistor compared to 45% for the HV01.

3.3.4 *RF Linearity*

RF linearity is also one of the major figures-of-merit of RF power characteristics. To characterize the linearity, the third-order intercept point (*IP3*), at which the output power and third-order inter-modulation (IM3) power are equal to let it is commonly used. For low distortion operation, the third-order intercept point should be as high as possible. As shown in Fig.3-7, using a two-tone load-pull measurement, this HV02 shows an OIP3 value of 19 dBm at the bias of V_G=1V and V_D=1.2V. The OIP3 of HV02 is higher than that in HV01 (18.4dBm) and than in a conventional DEMOS.

From the above experimental results, we found that the power performance of the ‘‘pseudo-drain’’ MOS transistors can meet the specifications of Bluetooth, wireless LAN, and other wireless applications.

3.4 *Summary*

A new power MOSFET design for RF power applications that relies on only layout scheme was investigated in this study. Without adding any masks and process modifications, a high breakdown voltage (BV_{DS}) of 4.3V can be achieved in 0.13μm core-NMOS transistors. Because the transconductance (g_m) of HV02 is higher than HV01, the characteristics on DC or RF that seems HV02 better than HC01. In addition, comparison of different CMOS power structures and with a raised biasing voltage was also addressed in this study. The results achieved from the implementation of 0.13μm MOS RF power devices demonstrate the potential power amplification capability of CMOS technologies for future integrated RF applications.

	g_m(ms)	R_g(Ω)	C_{gg}(fF)	f_T(GHz)	f_{max}(GHz)
HV01	**113.5**	**4.441**	**176.5**	**81**	**79.5**
HV02	**118.8**	**4.441**	**176**	**83**	**84**

Table.3-1 Extracted model parameters of HV01 and HV02.

Device (@2.4G)	**DC Bias Condition**	**Pout,max**	**Gain(dB)**	**PAE (%)**	**Pout,1dB(dB)**	**OIP3**
HV01	**VG=1V, VD=1.2V**	**11.5**	**15.2**	**45**	**8.19**	**18.4**
HV02	**VG=1V, VD=1.2V**	**12**	**15.8**	**47**	**8.54**	**19**

Table.3-2. Extracted power parameters of HV01, HV02

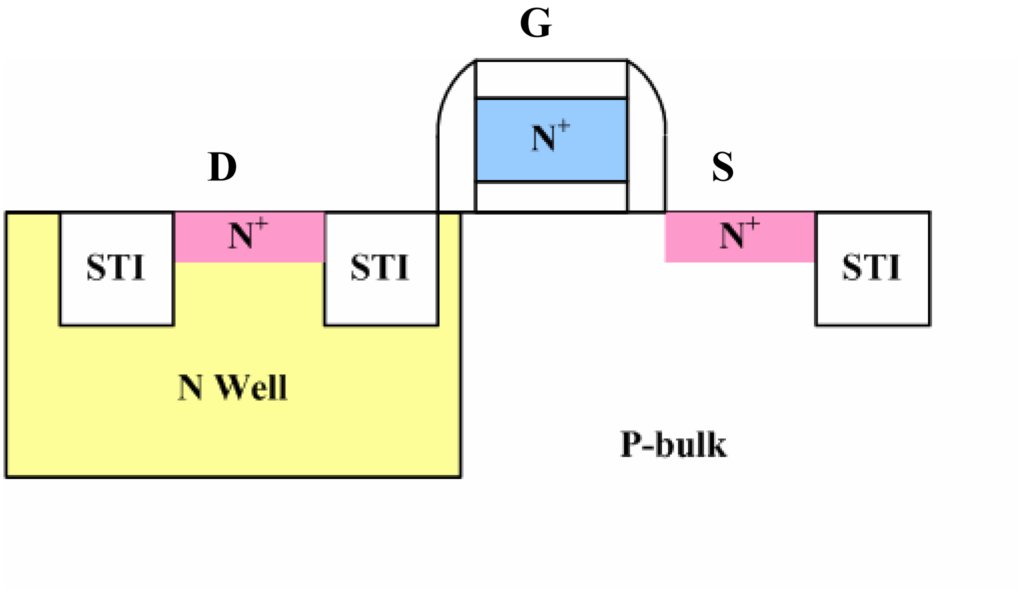


Fig.3-1(a)

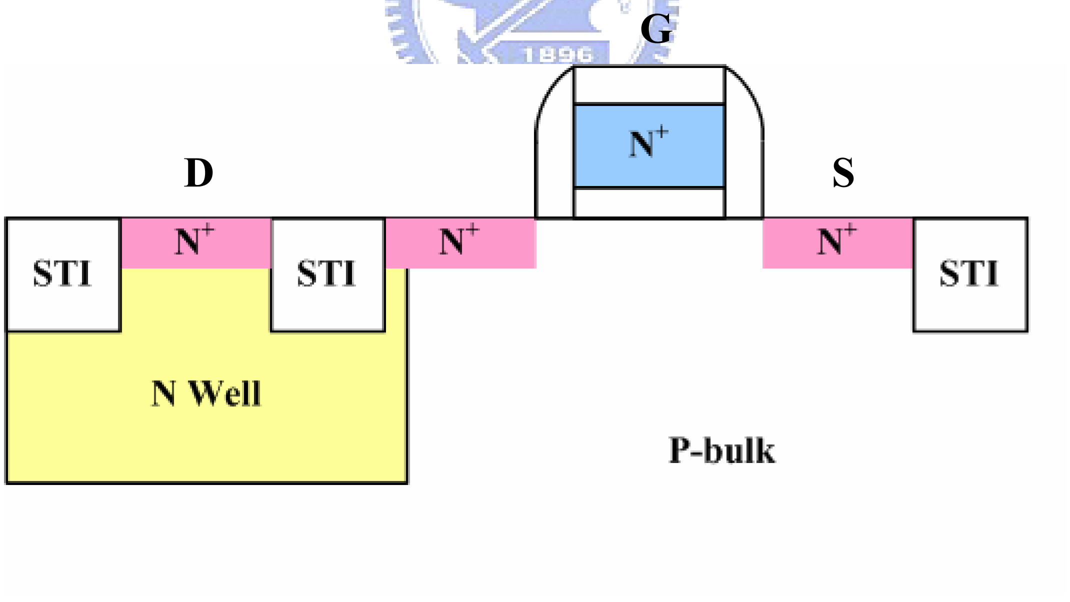


Fig.3-1(b)

Fig.3-1 Cross-sections of (a) Conventional "Drain-Extended" MOSFET, and (b) "Pseudo-Drain"RF power MOS structure

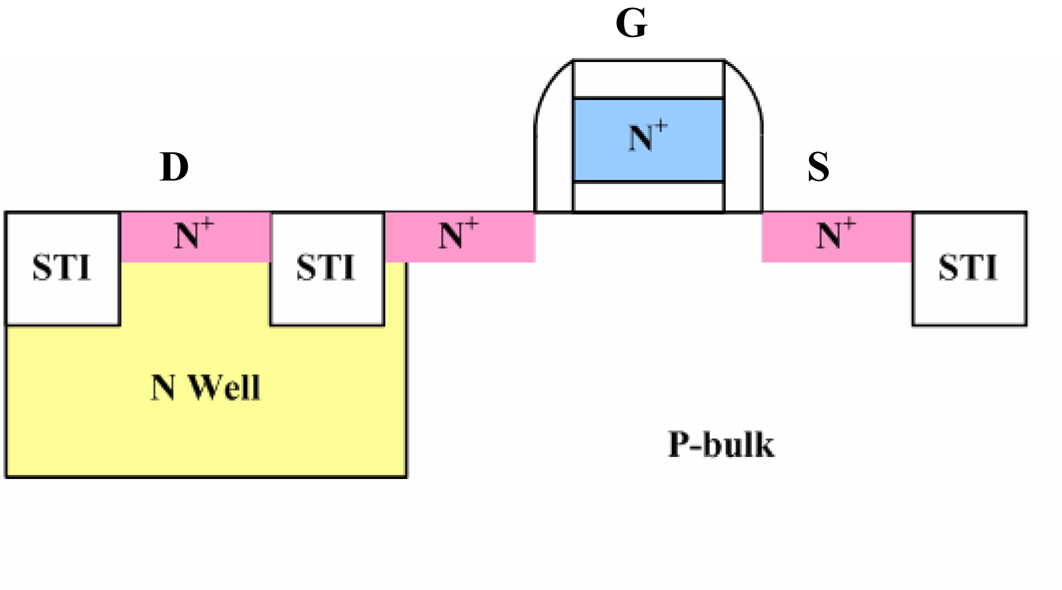


Fig 3-2(a)

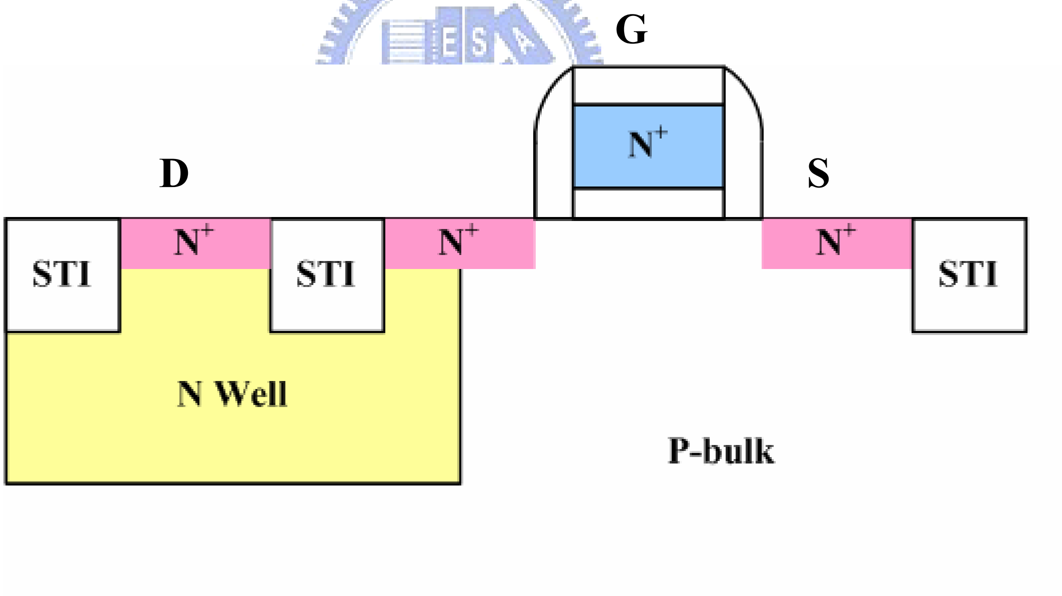


Fig 3-2(b)

Fig 3-2 (a) Schematic cross section of the HV01, and (b) Schematic cross section of the HV02

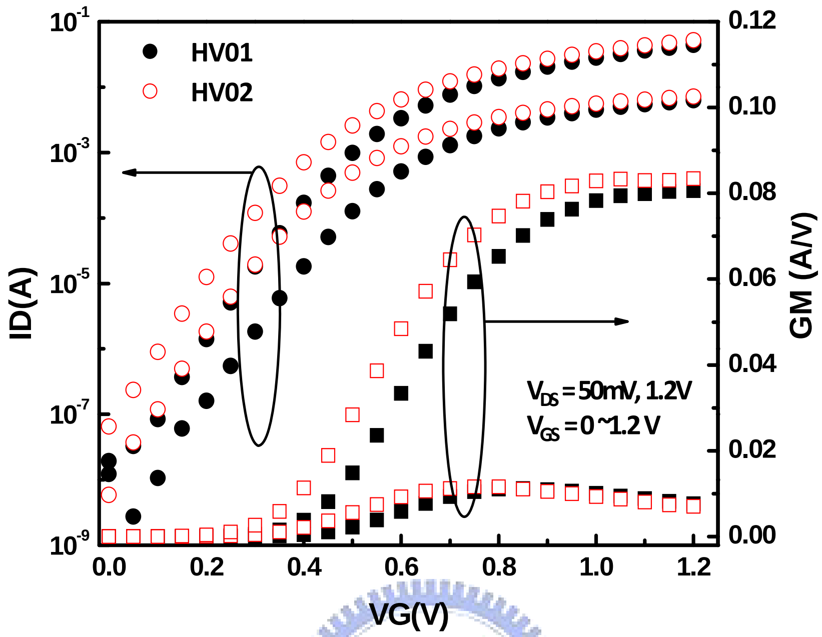


Fig.3-3 Compare the DC characteristic of HV01 and HV02

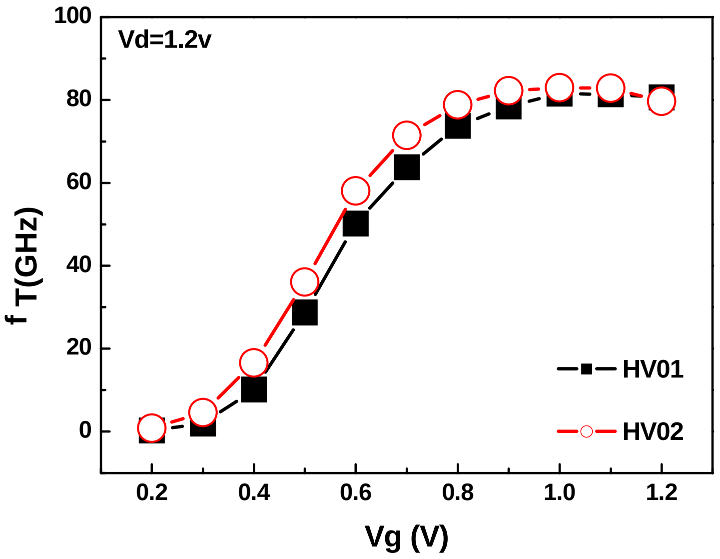


Fig 3-4(a)

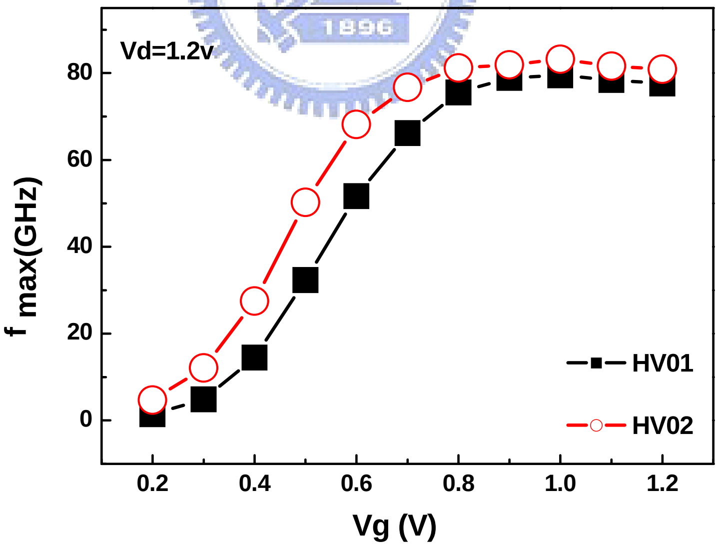


Fig 3-4(b)

Fig 3-4 Comparison of (a) f_T *and (b)* f_{max} *versus VG between HV01 and HV02*

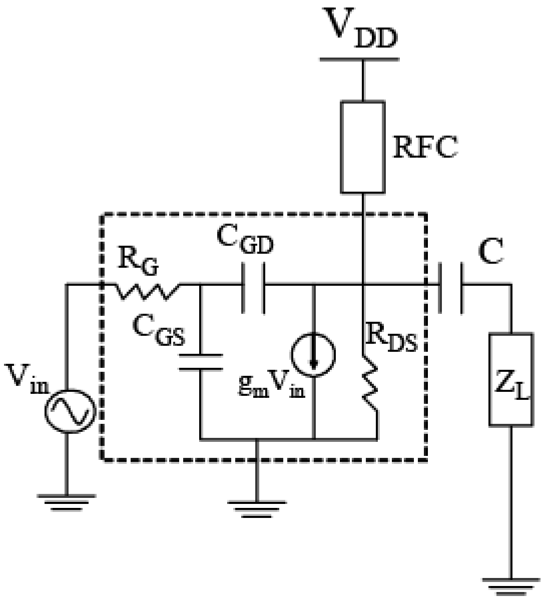


Fig.3-5 Simplified RF Power amplifier with an intrinsic RF small-signal model

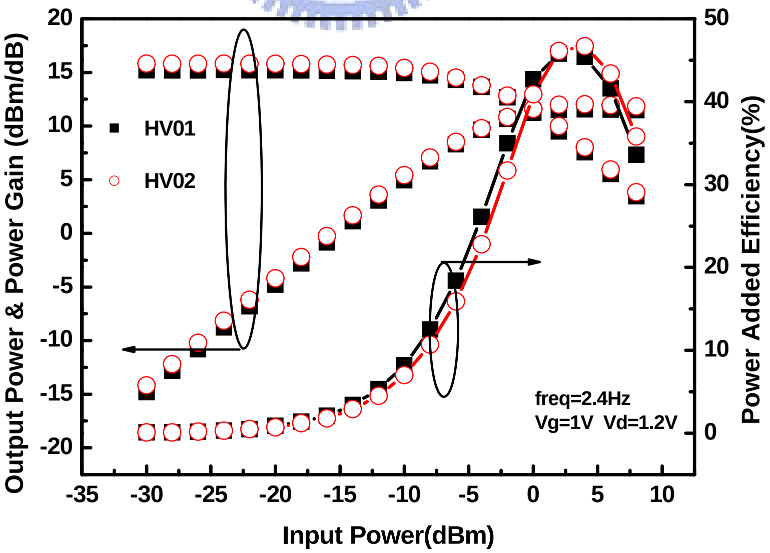


Fig 3-6 Output power, power gain and power-added efficiency of HV01 and HV02

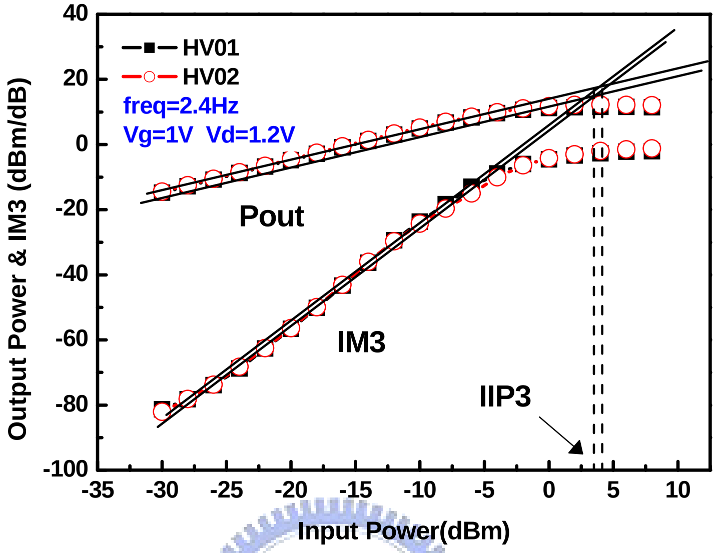


Fig 3-7 Output power, and IM3 power as a function of input power for HV01&HV02 transistor

Chapter 4

Characteristics of RF MOSFETs under Hot Carriers Stress

Introduction

In this chapter, the HC stress effects on DC and high frequency characteristics of RF MOSFETs will be discussed. In our experiments, the degradations are quite different by using different stress bias. We found that the degradations are more serious under drain avalanche hot carrier (DAHC) stress. After we discuss HC effects on the S-parameters, we found that the values of S_{22} and S_{21} are degraded seriously [17]. It implies that the output impedance and voltage gain are influenced after stress. Finally, we focus on the changes of the main figures-of-merit (FOM) of RF MOSFETs after HC stress. It shows that the degradations of power characteristics are obvious due to the HC stress effect.

4.1 *HC Stress Experiments*

In our experiments, the channel length and total width of MOSFETs are 0.13μm and 128 μm, respectively. For DAHC stress, the gate and drain of the test transistors were biased at 1.5V and 3V, respectively. For channel hot electron (CHE) stress, the gate and drain of the test transistors were both biased at 3V. Finally, the third stress condition were biased at V_{th}+0.1V and 3V on gate and drain voltage, respectively. The DC characteristic and S-parameters were measured a fixed stress time that is terminated at 1000 second.

4.2 *Effect of HC Stress on DC Characteristics*

The general effects of the HC stress on the dc characteristics of HV01 and HV02 were showon in Fig.4-1. It shows unobvious variations for device under CHE stress as illustrated in Fig.4-1(a) and Fig.4-1(b). Therefore the channel hot electrons just slightly influence the DC characteristics of MOSFETs. On the contrary, it shows a large degradation for device measured after DAHC stress shown in Fig.4-1(c) and Fig.4-1(d). Hence the degradations caused by drain avalanche hot carriers are much larger compared to channel hot electrons. After DAHC stress, the degradation of saturation drain current in HV01 and HV02 are 14% and 14.2%, respectively. In Fig.4-1(c) and (d), the transconductance (g_m) reduces significantly, and the maximum value shifts to higher gate voltages after HC stress. We also found that g_m and drain current reduction is more serious in low gate bias region and this phenomenon is possibly due to the interface state generation and the oxide trap charge[18],[19].

Now if we set to let g_m degradation 10% and compare the two structure reliability. Figure. 4-2 describes the DC characteristics of these structures on three conditions. We can see obvious variation on condition C. This is because the drain resistance changes serious with high gate voltage. The I_{on} direction is analogue to g_m and it is show in Fig.4-3. Because the oxide traps larger electrons by drain avalanche hot-carriers (DAHC) than channel hot electrons (CHE), the V_{th} was raising obviously in Fig.4-4. Finaly, we noticed the R_{on} behaviors on these conditions almost similar to the $V_{th.}$ And that drawing is exhibition on Fig 4-5.

4.3 *Effects of HC Stress on Cut-off Frequency and Maximum Oscillation Frequency*

The cut-off frequency is defined as the transition frequency at which the small-signal current gain of a transistor with common source configuration and short-circuit load drops to unity. As shown in Fig.4-6, the cut-off frequency drops off conspicuously after HC stress. By using the small-signal equivalent-circuit model, the cut-off frequency (f_T) can be approximated as:

$$f_T = \frac{g_m}{2\pi(C_{gd} + C_{gs})} \tag{4-1}$$

From above equation, f_T is related with g_m and gate-to-source capacitance (C_{gs}). After HC stress, there are many interface states generated near the oxide and semiconductor interface. Therefore C_{gs} increased after stress. In addition, from discussions in Section.4-2, g_m reduced significantly after HC stress. Due to the increase of C_{gs} and the decrease of g_m, f_T reduced dramatically after HC stress. By the observation of Fig. 4-6, it also suggested that the degradation of cut-off frequency is more robust to HC stress when biasing at higher gate voltages which is similar to the degradation of g_m. Then we can find the degradation is serious on condition B. And the HV02 structure has bad ability to against the hot-carrier stress. This characteristic is without reservation to show in the cut-off frequency.

As shown in Fig.4-6, maximum oscillation frequency (f_{max}) also decreases after HC stress. The maximum oscillation frequency is defined as the transition frequency at which the unilateral gain of a transistor with common source configuration drops to unity. It can be approximated as:

$$f_{\max} = \frac{f_T}{2\sqrt{2\pi f_T C_{gd} R_g + G_{ds} R_{in})}} \tag{4-2}$$

Because the maximum oscillation frequency is approximately proportional to the cut-off frequency, the degradations are correlated to the cut-off frequency. Therefore, f_{max} decreased after HC stress and the degradation is more serious while biasing at low VG which is similar to the degradation of f_{T}.

From Fig.4-6, we compared the RF performance degradation with the DC performance degradation. The degradations of f_{T} and f_{max} are proportional to the g_m degradation which can be explained by equation (4-1) and (4-2). Comparing the slopes of these two lines in Fig.4-7, the degradation of f_{T} is much larger than of f_{max}. Since f_{max} is proportional to the square of the g_m, it is less sensitive to HC stress.

4.4 *HC Effects on Power Performance and Linearity*

The effect of HC stress on the output power of a MOS transistor is shown in Fig.4-9. It was measured at gate voltage V_{GS}=1 V and drain voltage V_{DS} =1.2 V, where g_m is the maximum value in device saturation regions, and the frequency was operated at 2.4 GHz. The source and load impedances are matched for maximum output power before stress. The degradations of output power, power gain and power-added efficiency (PAE) are shown in Fig.4-9. The PAE can be expressed by:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out}}{P_{DC}}(1 - \frac{1}{G}) \qquad (4\text{-}3)$$

At low input power, the PAE is less changed under stress, due to the output power and drain current, and thus power dissipation, reduce simultaneously. When input power is larger than 1dB compression point, the degradations of PAE become serious. Because a part of the ac signal of drain current will be cut off as the input power is large enough. For this reason, the average drain current will increase with increasing input power. Since the bias current of the device after HC stress is lower than that of the fresh one, the negative duty cycle of output waveform would enter the cut off region earlier. As a result, the power dissipation of stressed device is higher than that of fresh one, leading to lower PAE. Since the DC degradation is more serious after DAHC stress, the degradations of PAE is more serious after DAHC stress.

To characterize the linearity which is showed in Fig.4-10 that the third-order intercept point (*IP3*), at which the output power and third-order intermodulation (IM3) power are equal, is commonly used. For low distortion operation, the third-order intercept point should be as high as possible. From Table.4-1, we can take notice of the RF linearity degrades under DAHC stress is more serious than CHE stress when the MOSFET operates at a fixed gate bias.

4.5 *Summary*

Compared to HV01, although HV02 had better DC characteristic, the RF and power characteristics were weakly after the same stress condition. Therefore, we could say HV01 has better reliability than HV02. Also, we compared the identical device under the different stress conditions, the HC stress condition B had worse reliability to HC stress condition C on the same device.

		IIP3 (dBm)		OIP3 (dBm)	
		Before Stress	After stress	Before Stress	After Stress
HV01	condition B	4.74	4.4	18.42	17.43
	condition C	5.03	4.77	19.14	18.72
HV02	condition B	5.36	4.8	18.87	17.22
	condition C	5.45	5.08	19.05	18.64

Table.4-1: Extracted linearity parameters of HV01, HV02

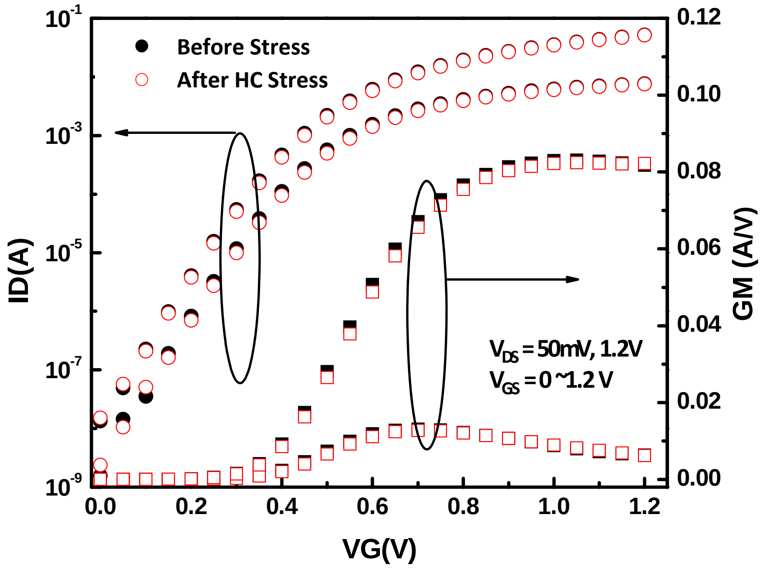


Fig. 4-1 (a)

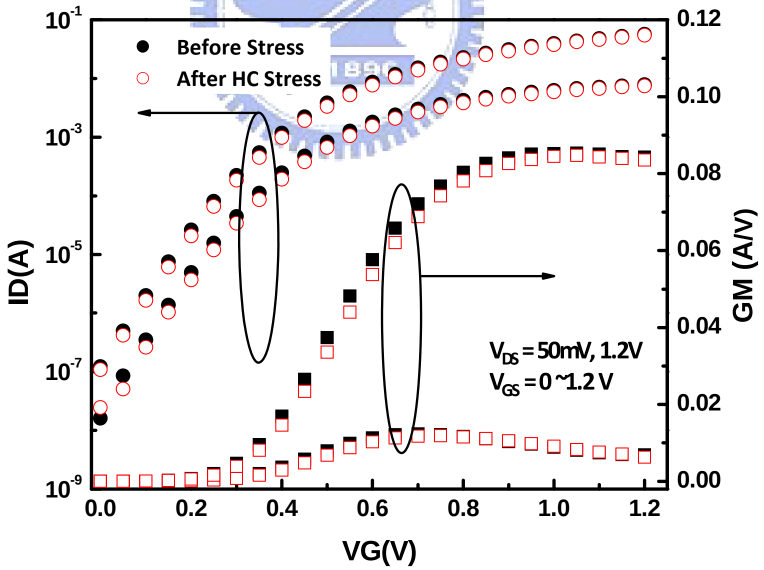


Fig. 4-1 (b)

Fig. 4-1: (a) DC characteristics of HV01 before and after CHE stress
(b) DC characteristics of HV02 before and after CHE stress

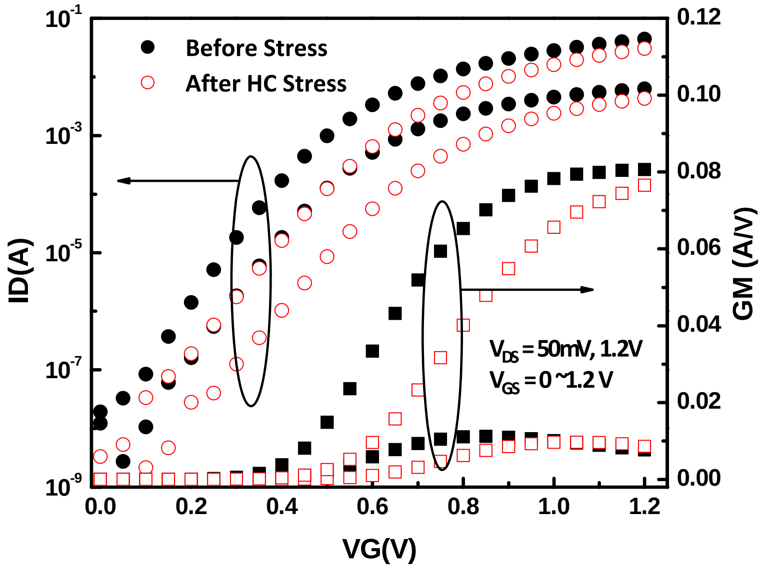


Fig. 4-1 (c)

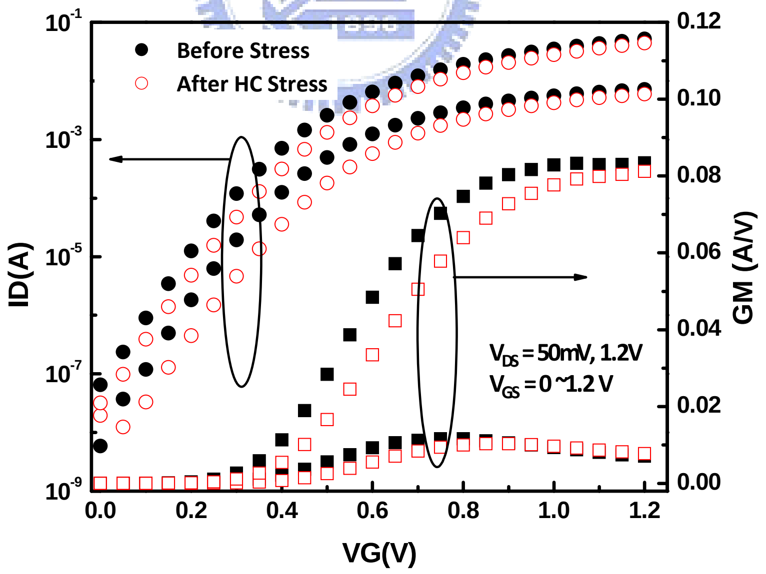


Fig. 4-1 (d)

Fig. 4-1: (c) DC characteristics of HV01 before and after DAHC stress
(d) DC characteristics of HV02 before and after DAHC stress

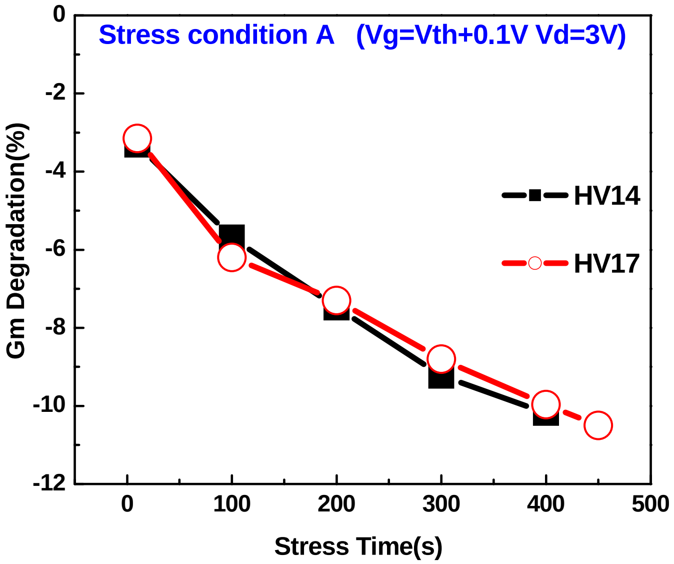


Fig.4-2 (a)

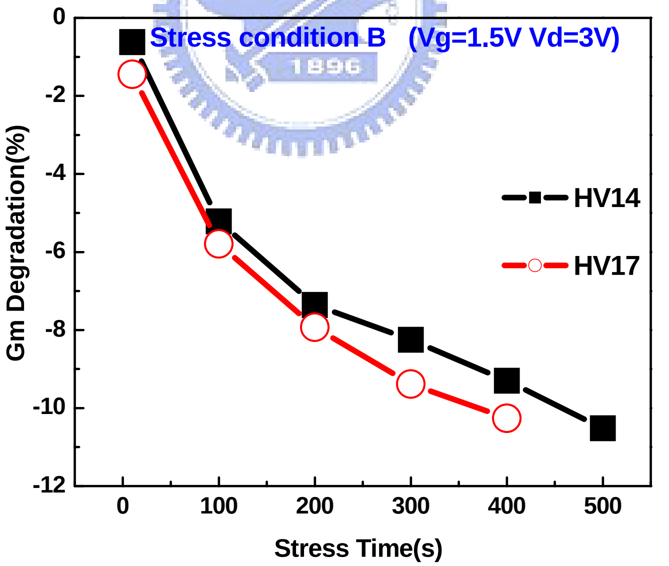


Fig.4-2 (b)

Fig.4-2 (a) To compare gm characteristics of HV01 and HV02 on Condition A with increasing stress time (b) To compare gm characteristics of HV01 and HV02 on condition B with increasing stress time

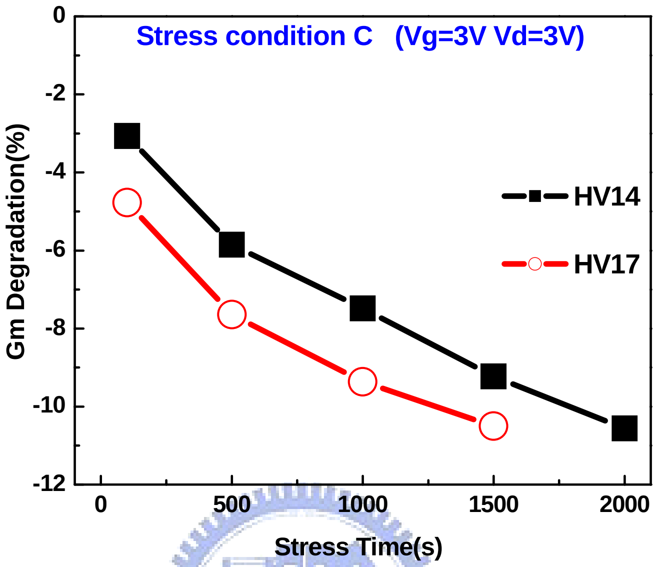
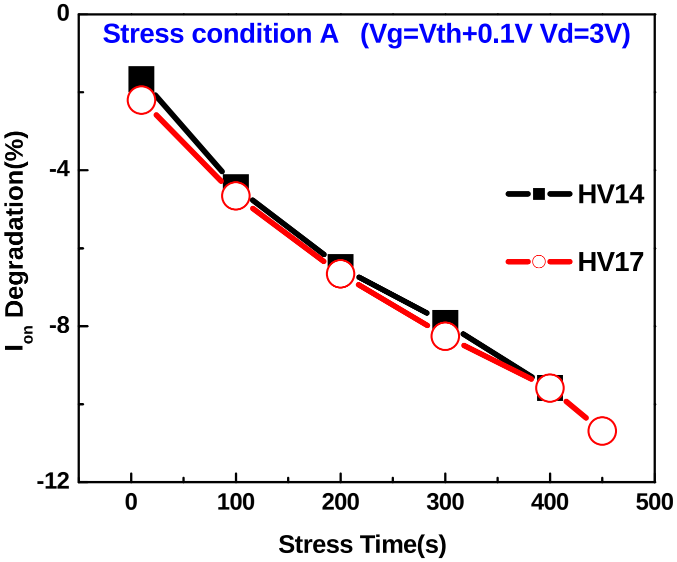


Fig.4-2 (c)

Fig.4-2 (c)To compare gm characteristics of HV01 and HV02 on condition C with increasing stress time



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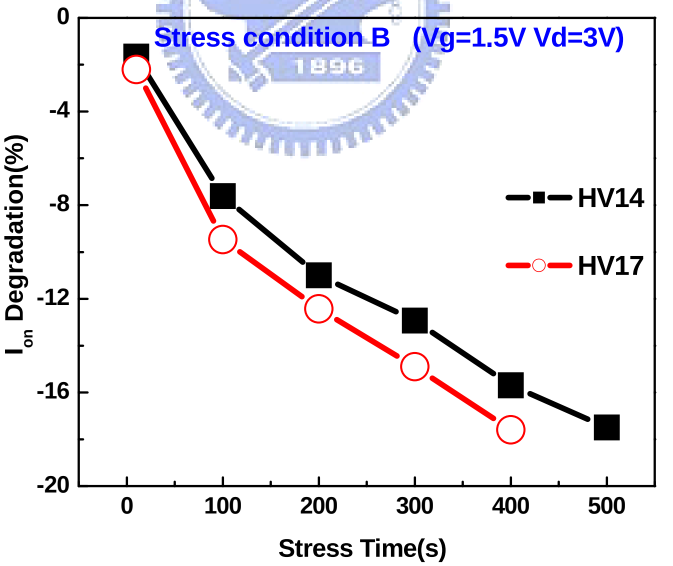

Fig. 4-3 (b)

Fig. 4-3: (a) To compare Ion characteristics of HV01 and HV02 on condition A with increasing stress time (b) To compare I_{on} characteristics of HV01 and HV02 on condition B with increasing stress time

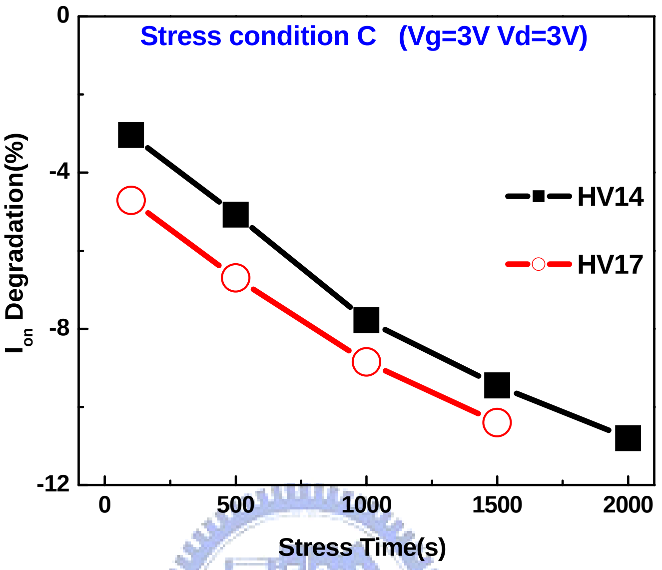

Fig. 4-3 (c)

Fig. 4-3: (c) To compare I_{on} *characteristics of HV01 and HV02 on condition C with increasing stress time*

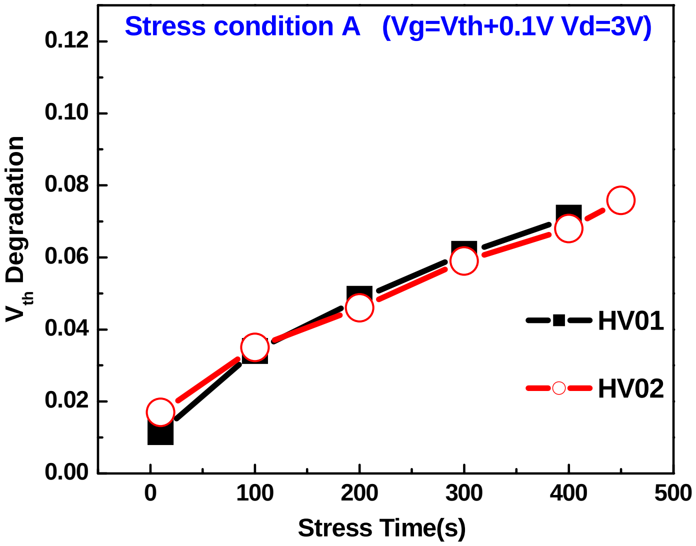

Fig.4-4 (a)

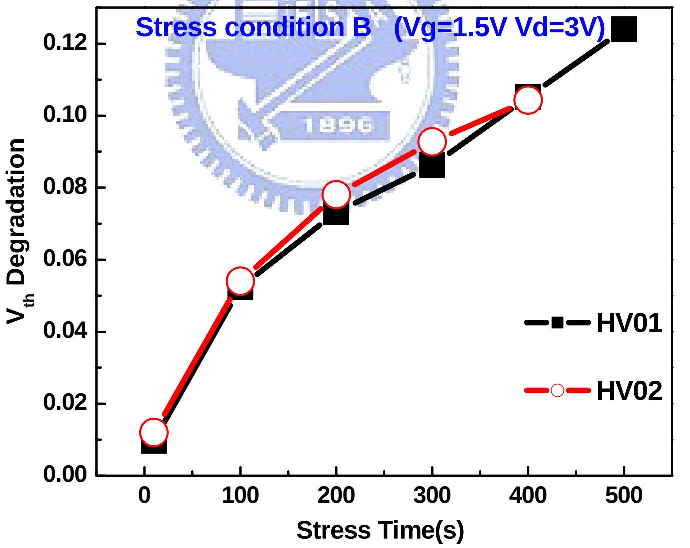

Fig.4-4 (b)

Fig.4-4 (a) To compare V_{th} *characteristics of HV01 and HV02 on condition A with increasing stress time(b) To compare* V_{th} *characteristics of HV01 and HV02 on condition B with increasing stress time*

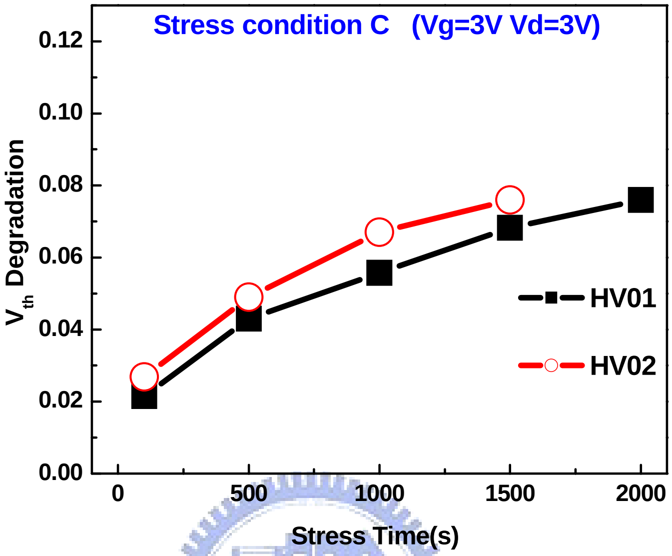

Fig.4-4 (c)

Fig.4-4 (c) To compare V_{th} *characteristics of HV01 and HV02 on condition C with increasing stress time*

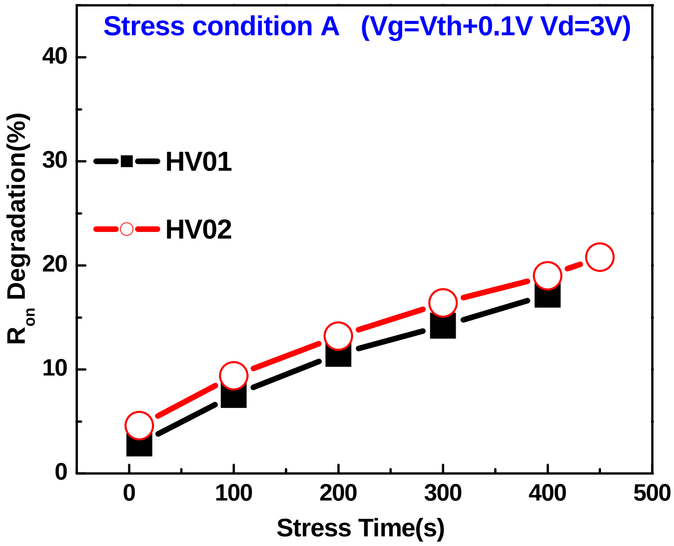

Fig.4-5 (a)

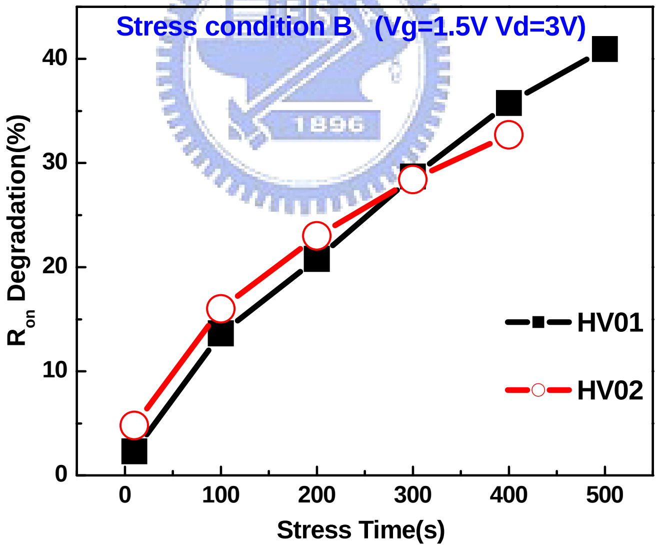

Fig.4-5 (b)

Fig.4-5(a) To compare R_{on} characteristics of HV01 and HV02 on condition A with increasing stress time (b) To compare R_{on} characteristics of HV01 and HV02 on condition B with increasing stress time

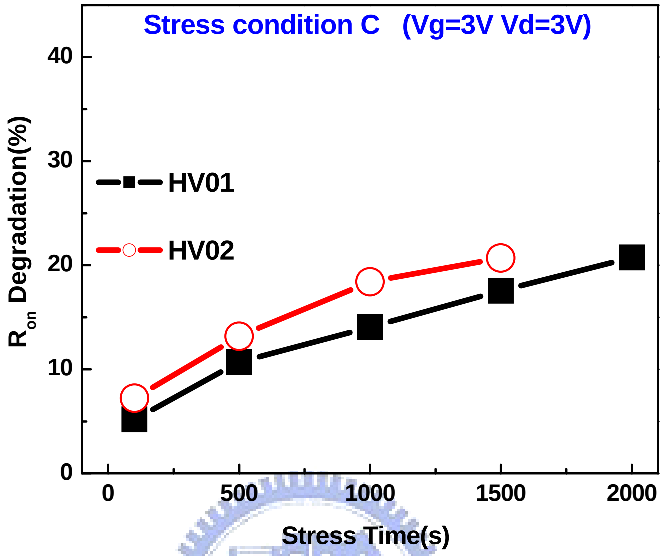

Fig.4-5 (c)

Fig.4-5 (c) To compare R_{on} *characteristics of HV01 and HV02 on condition C with increasing stress time*

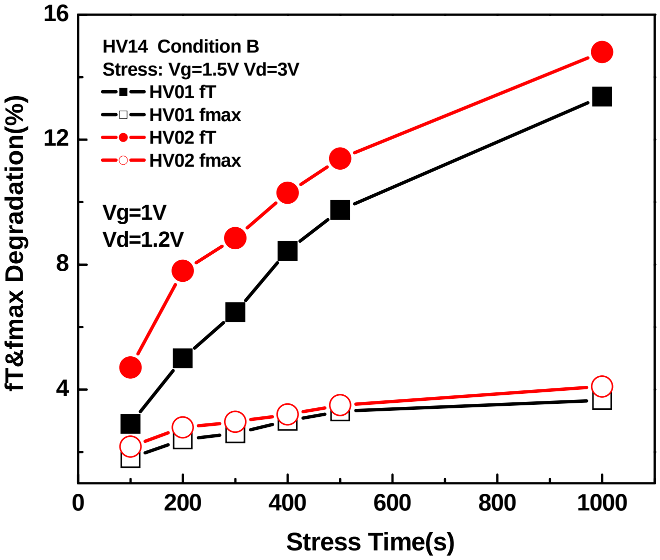

Fig. 4-6 (a)

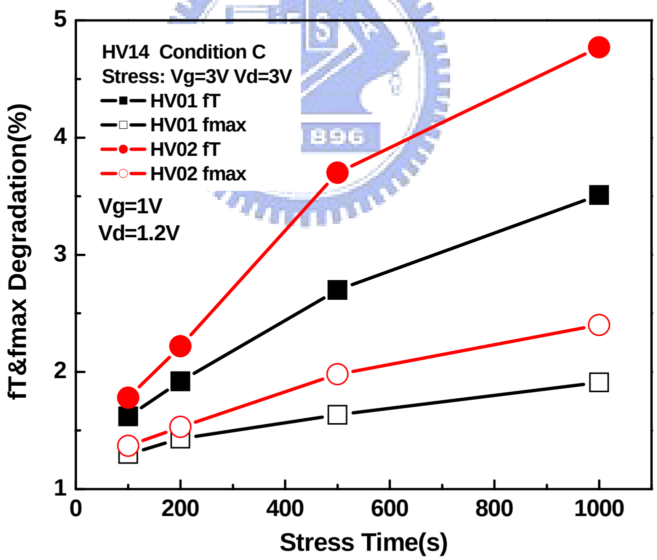

Fig. 4-6 (b)

Fig. 4-6: (a) Cut-off frequency before and after HC stress on HV01 and HV02 (b) Maximum oscillation frequency before and after HC stress on HV01 and HV02

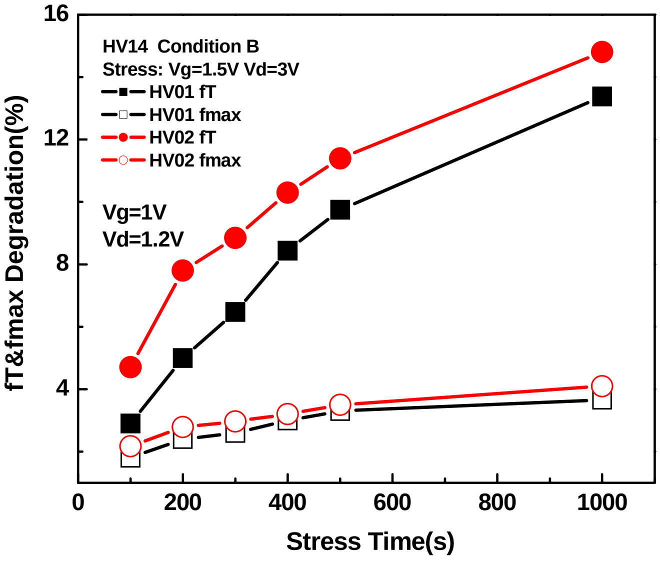

Fig. 4-7 (a)

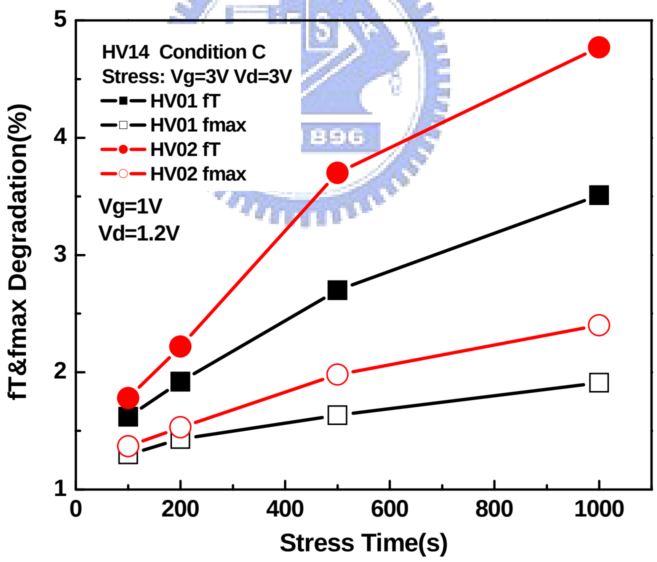

Fig. 4-7 (b)

Fig. 4-7: (a) Cut-off frequency before and after HC stress on HV01 and HV02 (b) Maximum oscillation frequency before and after HC stress on HV01 and HV02

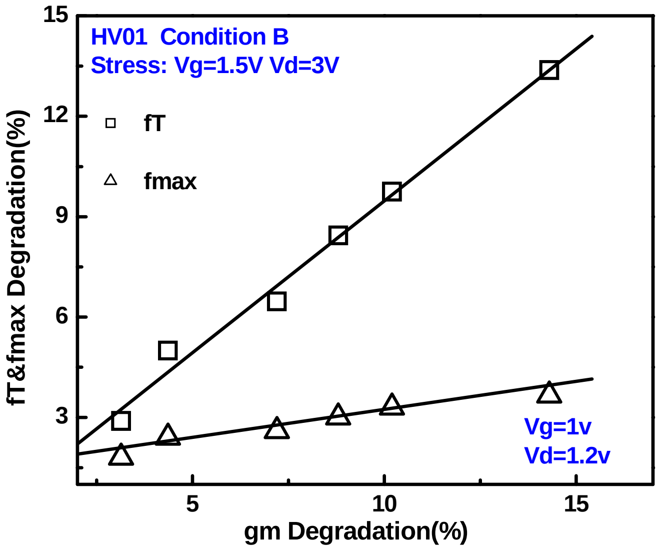

Fig. 4-8 (a)

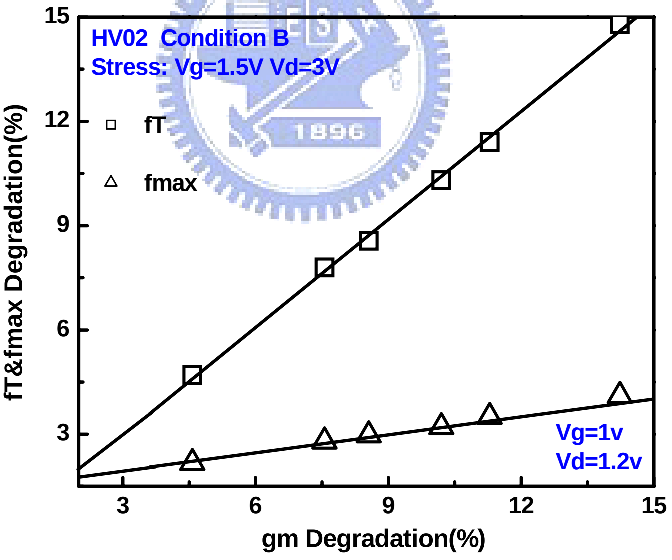

Fig. 4-8 (b)

Fig. 4-8: (a) Relation between f_T and f_{max} degradations and gm degradation on condition B of HV01 (b)Relation between f_T and f_{max} degradations and gm degradation on condition B of HV02

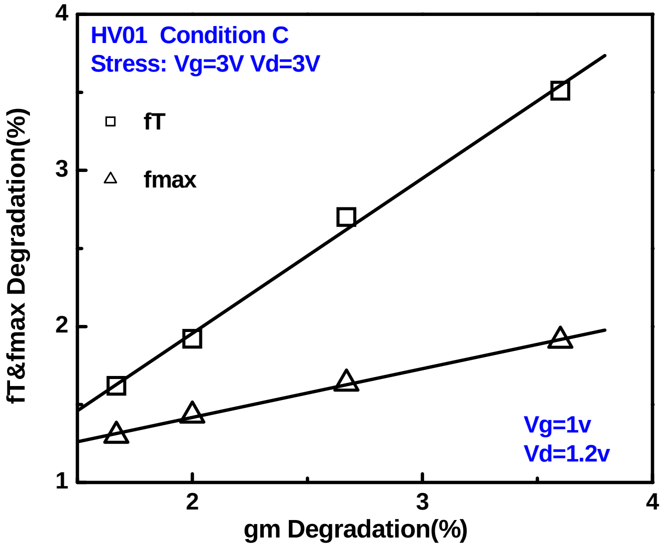

Fig. 4-8 (c)

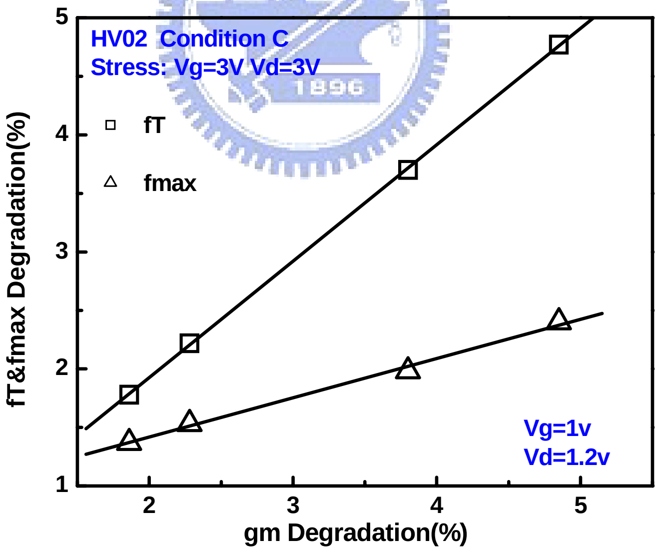

Fig. 4-8 (d)

Fig. 4-8: (c) Relation between f_T and f_{max} degradations and gm degradation on condition C of HV01 (d) Relation between f_T and f_{max} degradations and gm degradation on condition C of HV02

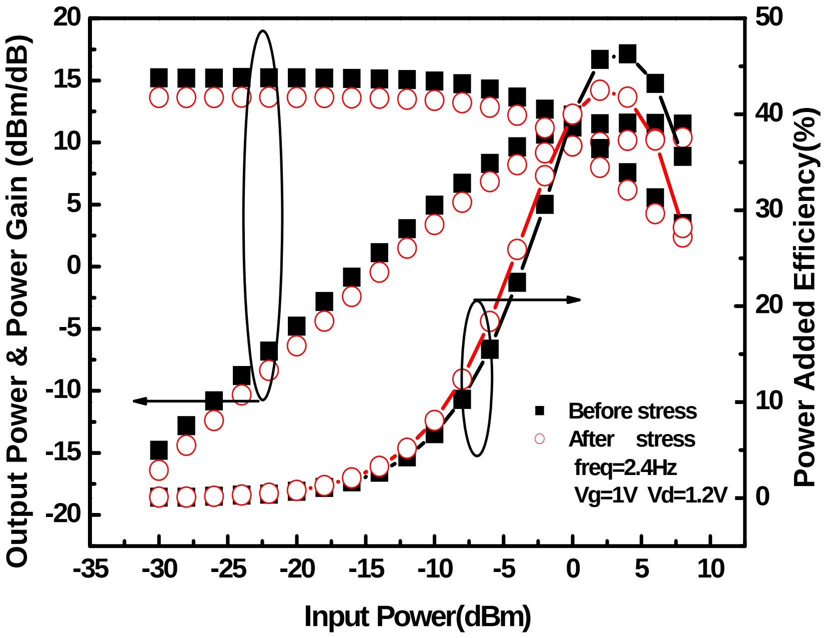

Fig. 4-9 (a)

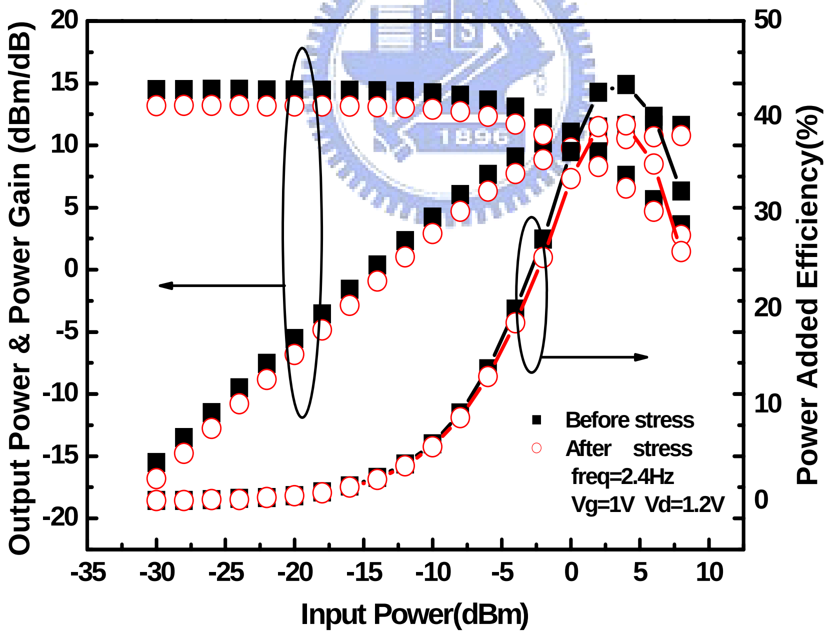

Fig. 4-9 (b)

Fig. 4-9: (a) Output power, power gain and PAE versus input power before and after HC stress on condition B of HV01. (b) Output power, power gain and PAE versus input power before and after HC stress on condition B of HV02

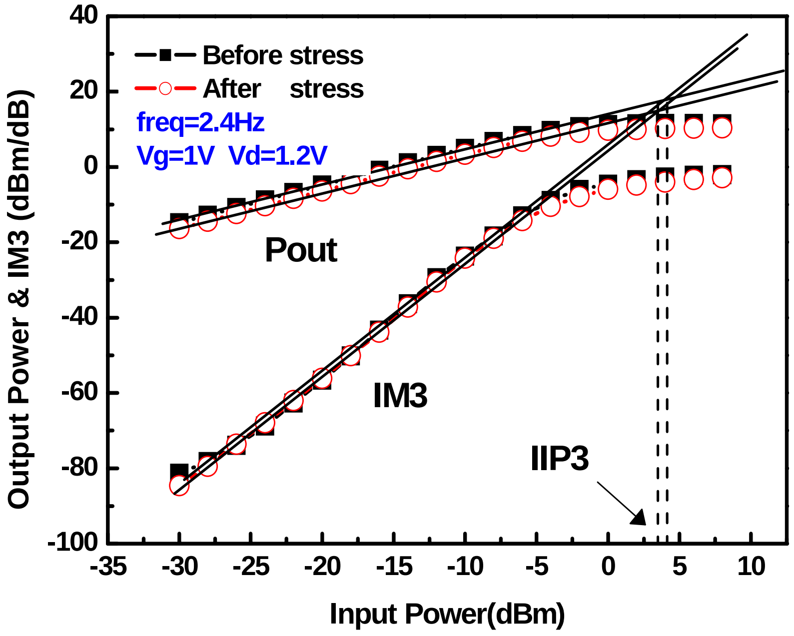

Fig. 4-10 (a)

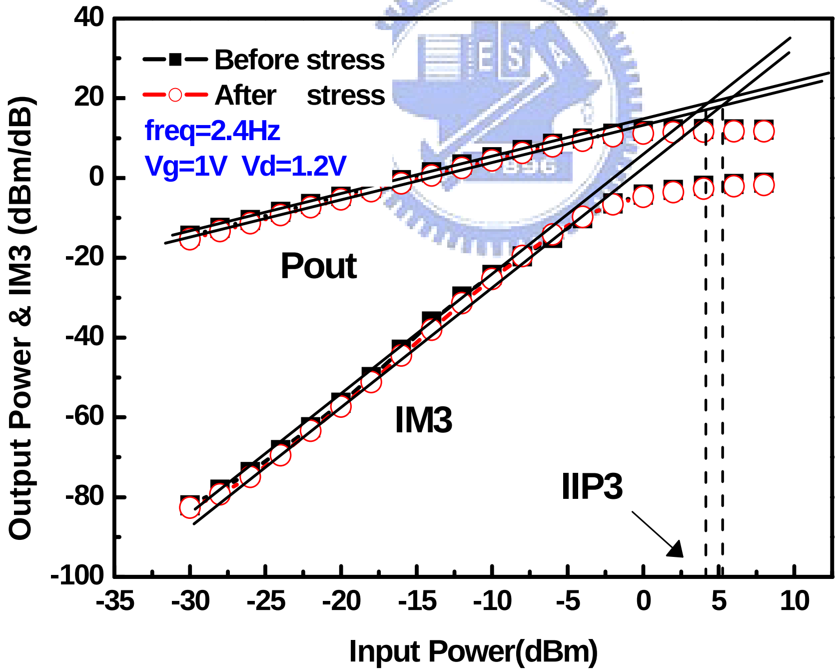

Fig. 4-10 (b)

Fig. 4-10: (a) Output power and 3^{rd}*-order intermodulation (IM3) power versus input power before and after HC stress on condition B of HV01 (b) Output power and* 3^{rd}*-order intermodulation (IM3) power versus input power before and after HC stress on condition B of HV02*

Chapter 5

Modeling of RF MOSFETs under HC stress

Introduction

In this chapter, we create a small-signal model of the RF MOSFET which is valid up to 50 GHz. An extraction approach, which was proposed by S. Lee [20], was adopted to determine the intrinsic circuit parameters. For modeling devices under HC stress, we compare the variations of each parameter after stress. And we use another method to model the substrate parasitic effect. When the drain-side substrate parasitic is taken into account, careful attention must be taken into consideration, especially for RFIC applications.

5.1 *Extraction Method of Small-Signal Model Parameters*

The small-signal model shown in Fig. 5-1(a) can be partitioned into three parts. The first part includes the parasitic series resistors R_g, R_d and R_s, and the second part refers to as the substrate network. The third part is the intrinsic model. We extract the parasitic resistors by using the conventional small-signal equivalent circuit as shown in Fig. 5-2. If the frequency is not high enough, we can ignore the substrate network. Conversion of the measured S-parameters into real components of an equivalent z-parameters network yields the parasitic resistance values. Equations for the parasitic resistances of the model shown in Fig. 5-2 are given by:

$$\mathrm{Re}(Z_{12})=\mathrm{Rs}+\frac{A_s}{w^2+B} \tag{5-1}$$

$$\mathrm{Re}(Z_{11}\text{-}Z_{12})=R_g+\frac{A_g}{w^2+B} \tag{5-2}$$

$$\mathrm{Re}(Z_{22}\text{-}Z_{12})=R_d+\frac{A_d}{w^2+B} \tag{5-3}$$

Fig. 5-3 illustrates the values of Rg, Rd and Rs extracted by this technique. After de-embedding the parasitic parameters, we use the curve-fitting method [21][22][23] to extract the parameters associated with the substrate parasitic. After d-embedding Rg, Rs, and Rd, the resulting network would become that shown in Fig. 5-1(b) and it will produce following equations:

$$\frac{1}{R_{ds}{}^{eff}}=\mathrm{Re}\,al(Y_{out,12}+Y_{out,22})=\frac{1}{R_{ds}}+\frac{k_1\omega^2}{1+k_2\omega^2} \tag{5-4}$$

$$C_{ds}{}^{eff}=\frac{1}{\omega}\mathrm{Im}(Y_{out,12}+Y_{out,22})=C_{ds}+C_{jdb}\left(\frac{1+m_1\omega^2}{1+m_2\omega^2}\right) \tag{5-5}$$

$$R_{sub}=\frac{k_2}{k_1}[1-\frac{m_1}{m_2}]^2 \tag{5-6}$$

$$C_{sub}=\frac{m_1C_{jdb}}{m_2-m_1} \tag{5-7}$$

where k1, k2, m1, m2 can be considered as constants. From above equations, the parameters which are associated with substrate network can be obtained by using curve-fitting method. Finally the parameters of the intrinsic network shown in Fig. 5-1(c) can be directly extracted by following equations [21],[22],[23]:

$$C_{gd}=-\frac{1}{\omega}\mathrm{Im}(Y_{i,12}) \tag{5-8}$$

$$C_{gs}=\frac{1}{\omega}\mathrm{Im}(Y_{i,12}+Y_{i,11}) \tag{5-9}$$

$$C_{ds}=\frac{1}{\omega}\mathrm{Im}(Y_{i,12}+Y_{i,22}) \tag{5-10}$$

$$R_{ds} = \frac{1}{\mathrm{Re}(Y_{i,22})} \quad (5\text{-}11)$$

$$g_{m0} = Mag(Y_{i,21} - Y_{i,12}) \quad (5\text{-}12)$$

$$\tau = -\frac{1}{\omega} Phase(Y_{i,21} - Y_{i,12}) \quad (5\text{-}13)$$

Fig. 5-4 shows the extracted values of each parameter versus frequency. The extracted parameters remained somewhat constant with frequency. Finally we show the measured and modeled S-parameters in Fig. 5-5 to verify the accuracy of this model.

5.2 *Modeling of PDMOS under HC Stress*

From the observations of S-parameters after HC stress, we assume that there are no new components added to the equivalent circuit shown in Fig. 5-1.Therefore, we directly use conventional small-signal model to establish the device model under HC stress. As shown in Fig. 5-6, this model is accurate under HC stress. Table 5-1 shows the extracted parameters of this study structure before and after HC stress on condition B and condition C. We found that only C_{gs}, g_{m0}, R_{ds} and R_d suffer degradations obviously after HC stress.

First of all, we plot the extracted C_{gs} and C_{gd} with increasing stress time, as shown in Fig.5-7 and Fig.5-8. It is obvious that C_{gs} increase in HV01 and HV02 with increasing HC stress time on condition B and condition C. The variations of C_{gd} are very slight compared with that of C_{gs}. We use the definition of small-signal gate-to-source capacitance to explain this observation [24]:

$$C_{gs} = -\frac{\partial Q_g}{\partial V_s} = \frac{WC_{OX}}{v_{sig}} \int_{x=0}^{x=L} v_{ac}(x)dx \quad (5\text{-}12)$$

in which L and W are the length and width of the MOSFET, respectively, v_{ac} is the small signal potential along the channel, v_{sig} is the small signal voltage applied to the source in order to measure C_{gs}, and C_{ox} is the gate oxide capacitance per unit area. For fresh device, there are no negative trap charges near drain. Hence v_{ac} changes uniformly from source to drain terminal. After HC stress, due to the presence of negative trap charges near drain, v_{ac} near drain increases. Therefore the value of equation (5-14) increases and C_{gs} increases dramatically after HC stress. It implies that input matching has been changed at high frequency. It should be pointed out that depending on bias point, C_{gd} changes slightly, as confirmed by the data in [25]. As a result, the variation of C_{gd} is too small to have any significant effects on the RF performance of the MOSFET compared to that of C_{gs}.

Fig. 5-9 shows the degradations of g_{m0} of HV01 and HV02 with increasing stress time on condition B and condition C. The degradations of g_{m0} are more serious when biasing at lower gate voltages. And it direction is similarity to g_m which be measured on DC characteristic.

5.3 *Summary*

From observing the small-signal model, the transconductance(g_{m0}), drain-to-source resistance(R_{ds}), gate-to-source capacitance(C_{gs}), and drain resistance(R_d) suffer more degradation after HC stress. Especially, the R_d was an important factor that was decision the divergence on structures of the HV01 and the HV02. Because R_d in HV01 was bigger than HV02 at the same V_{gd}, voltage dropped in the drain region occupied most voltage than the voltage dropped in the channel between gate to drain. Then the HV02 voltage dropped was occupied most in the channel. Consequently, the reliability was badly in HV02 than in HV01. Finaly, we proved it again by small-signal model.

HV01 Condition B	G_{m0}(ms)	τ(psec)	$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	R_{ds} (Ω)	$R_{sub}(\Omega)$
Before Stress	113.4	2.8	4.441	2.43	6.7	93	60.12
After HC stress	96.36	2.8	4.441	2.4	7.5	96.5	60.12

HV01 Condition B	C_{gd}(fF)	C_{sub}(fF)	C_{ds}(fF)	C_{jdb}(fF)	C_{gs}(fF)
Before Stress	44.27	26.3	23	220	125.7
After HC stress	45.1	26.3	23	220	132.6

Table 5-1 (a)

Table 5-1(a) Extracted parameters before and after HC stress condition B on HV01

HV02 Condition B	G_{m0}(ms)	τ(psec)	R_g(Ω)	R_s(Ω)	R_d(Ω)	R_{ds} (Ω)	R_{sub}(Ω)
Before Stress	118.8	2.8	4.441	2.32	4.82	94.52	34
After HC stress	98.9	2.8	4.441	2.3	5.48	98.61	34

HV02 Condition B	C_{gd}(fF)	C_{sub}(fF)	C_{ds}(fF)	C_{jdb}(fF)	C_{gs}(fF)
Before Stress	48.08	26.6	23	368	122.6
After HC stress	48.46	26.6	23	368	128.1

Table 5-1 (b)

Table 5-1(b) Extracted parameters before and after HC stress condition B on HV02

HV01 Condition C	G_{m0}(ms)	τ(psec)	R_g(Ω)	R_s(Ω)	R_d(Ω)	R_{ds} (Ω)	R_{sub}(Ω)
Before Stress	113.5	2.8	4.441	2.4	6.72	97.6	59.5
After HC stress	103.3	2.8	4.441	2.37	7.18	89	59.5

HV01 Condition C	C_{gd}(fF)	C_{sub}(fF)	C_{ds}(fF)	C_{jdb}(fF)	C_{gs}(fF)
Before Stress	45.24	25	27	216	131.6
After HC stress	46	25	27	216	135.2

Table 5-1 (c)

Table 5-1(c) Extracted parameters before and after HC stress condition C on HV01

HV02 Condition C	G_{m0}(ms)	τ(psec)	$R_g(\Omega)$	$R_s(\Omega)$	$R_d(\Omega)$	R_{ds} (Ω)	$R_{sub}(\Omega)$
Before Stress	118.7	2.8	4.441	2.3	4.81	95.7	36
After HC stress	106.6	2.8	4.441	2.3	5.2	87.55	36

HV02 Condition C	C_{gd}(fF)	C_{sub}(fF)	C_{ds}(fF)	C_{jdb}(fF)	C_{gs}(fF)
Before Stress	48.48	29	24	357	116.2
After HC stress	48.54	29	24	357	119.2

Table 5-1 (d)

Table 5-1(d) Extracted parameters before and after HC stress condition C on HV02

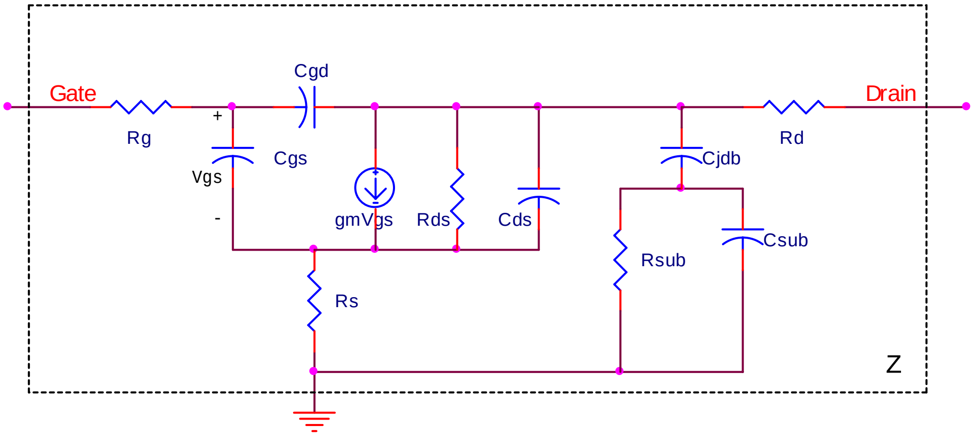

Fig.5-1 (a)

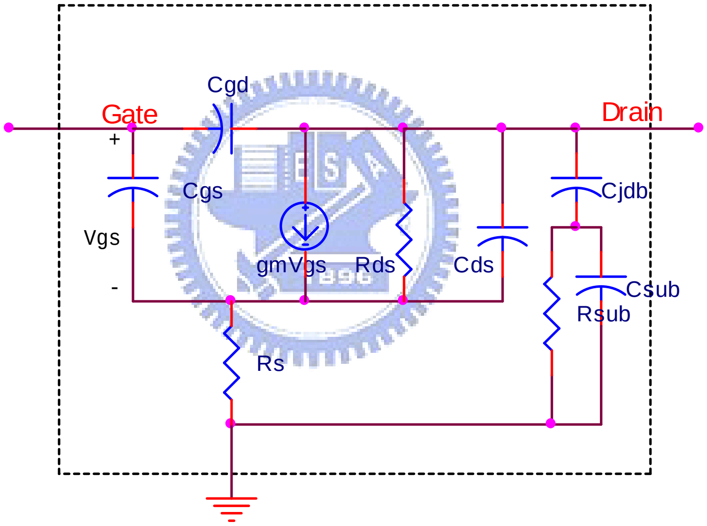

Fig.5-1 (b)

Fig.5-1: (a) Conventional small-signal model of a MOSFET
(b) Equivalent circuit after de-embedding parasitic components

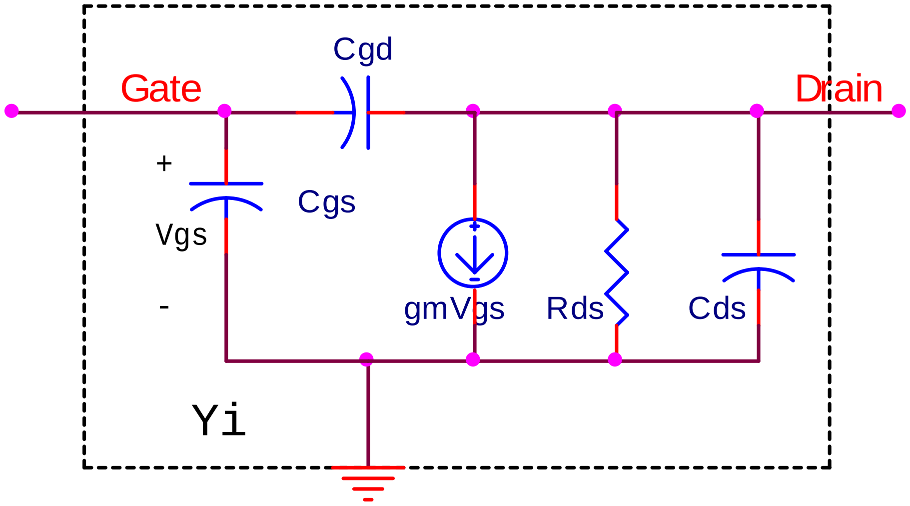

Fig.5-1 (c)

Fig.5-1 (c) Small-signal model for the intrinsic part of a MOSFET

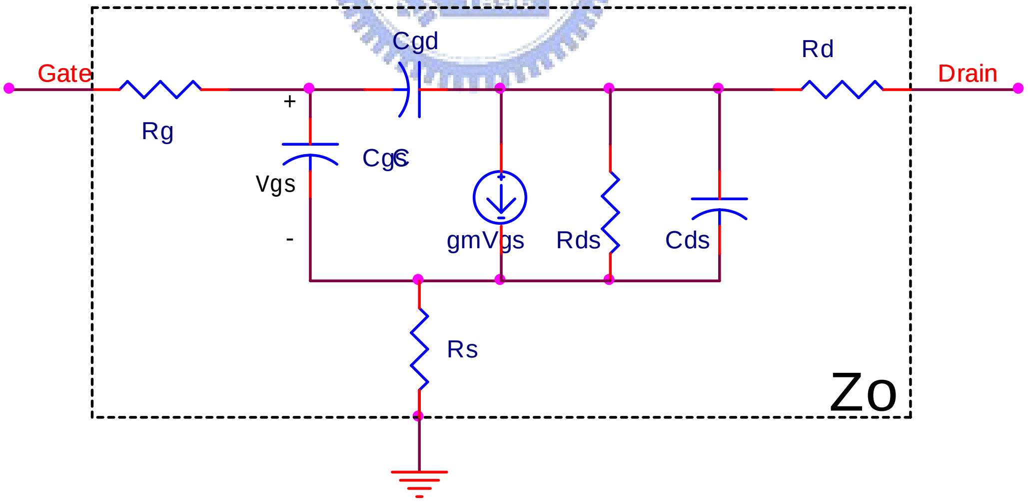

Fig.5-2 Conventional small-signal model for silicon MOSFET's

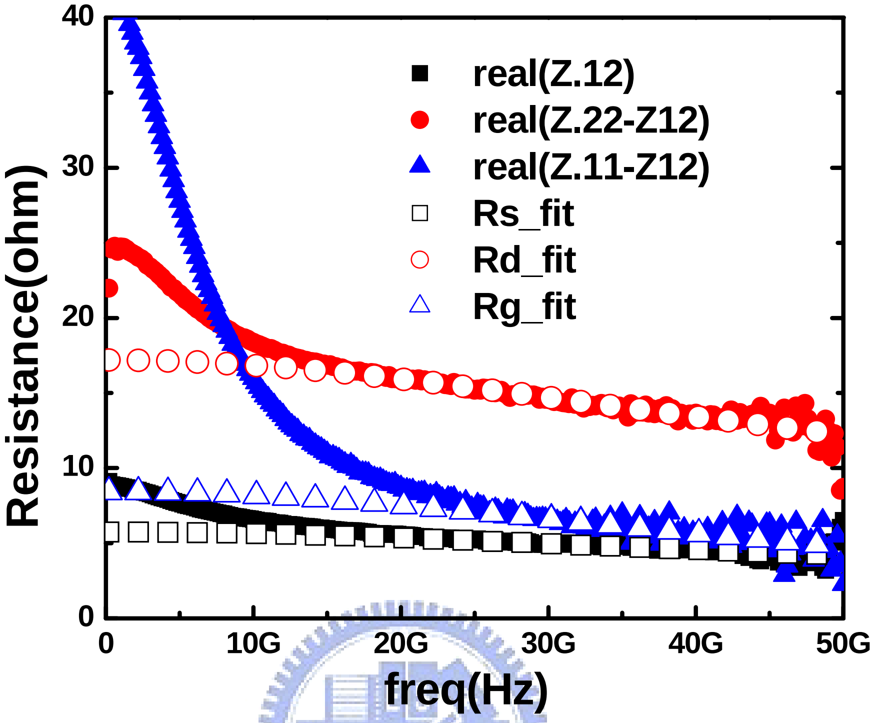

Fig.5-3 Extracted values of R_s, R_g and R_d versus frequency

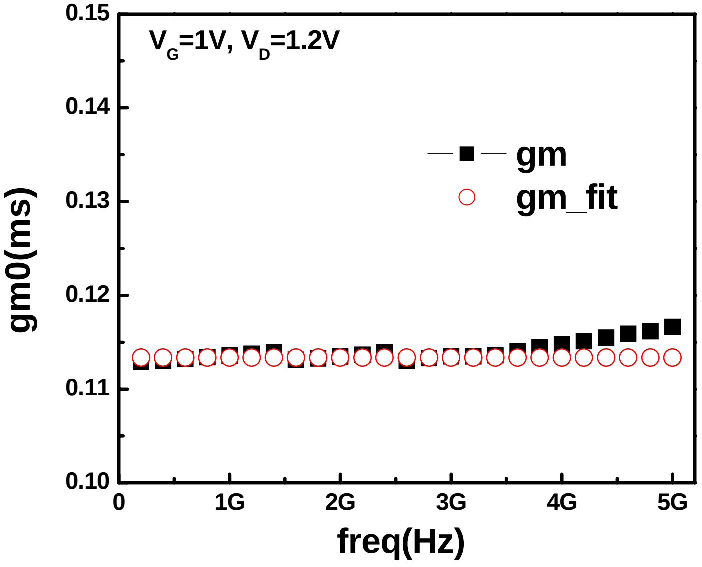

Fig. 5-4 (a)

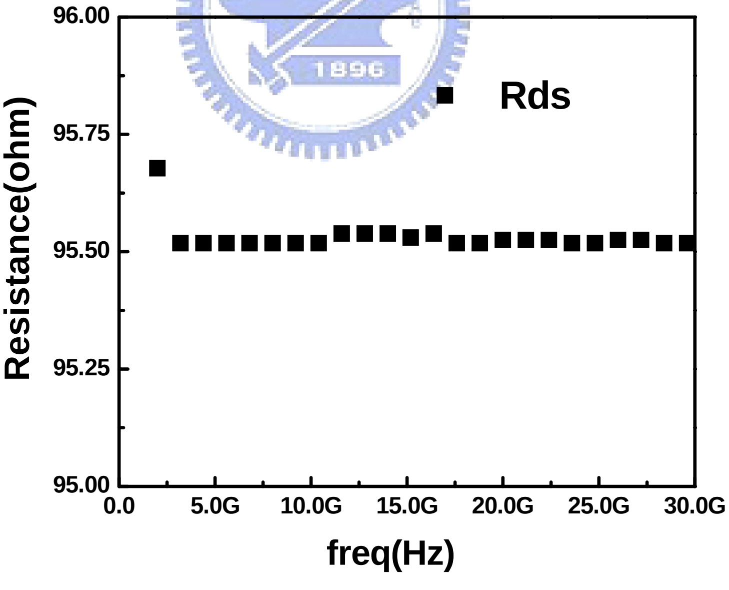

Fig. 5-4 (b)

Fig. 5-4: (a) Extracted g_{m0} *versus frequency*
(b) Extracted R_{ds} *versus frequency*

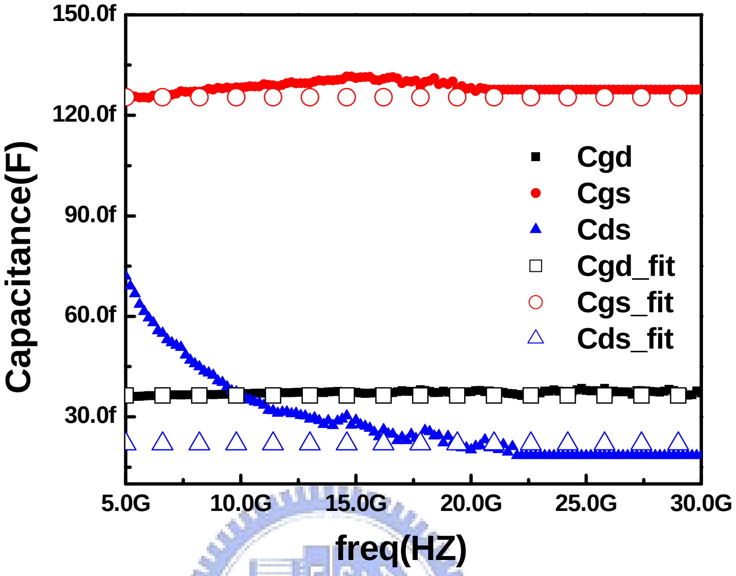

Fig. 5-4 (c)

Fig. 5-4: (c) Extracted capacitance versus frequency

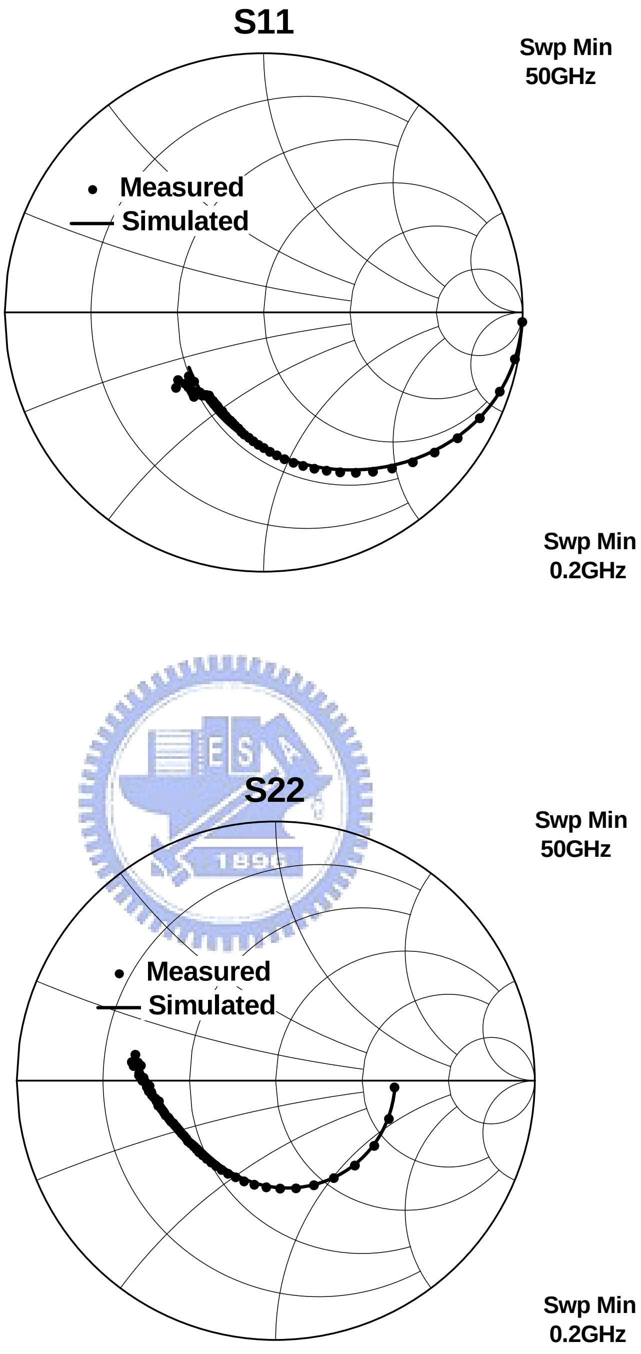

Fig. 5-5(a): Measured and modeled S-parameters of a MOSFET before stress at V_G=1V V_D=1.2V

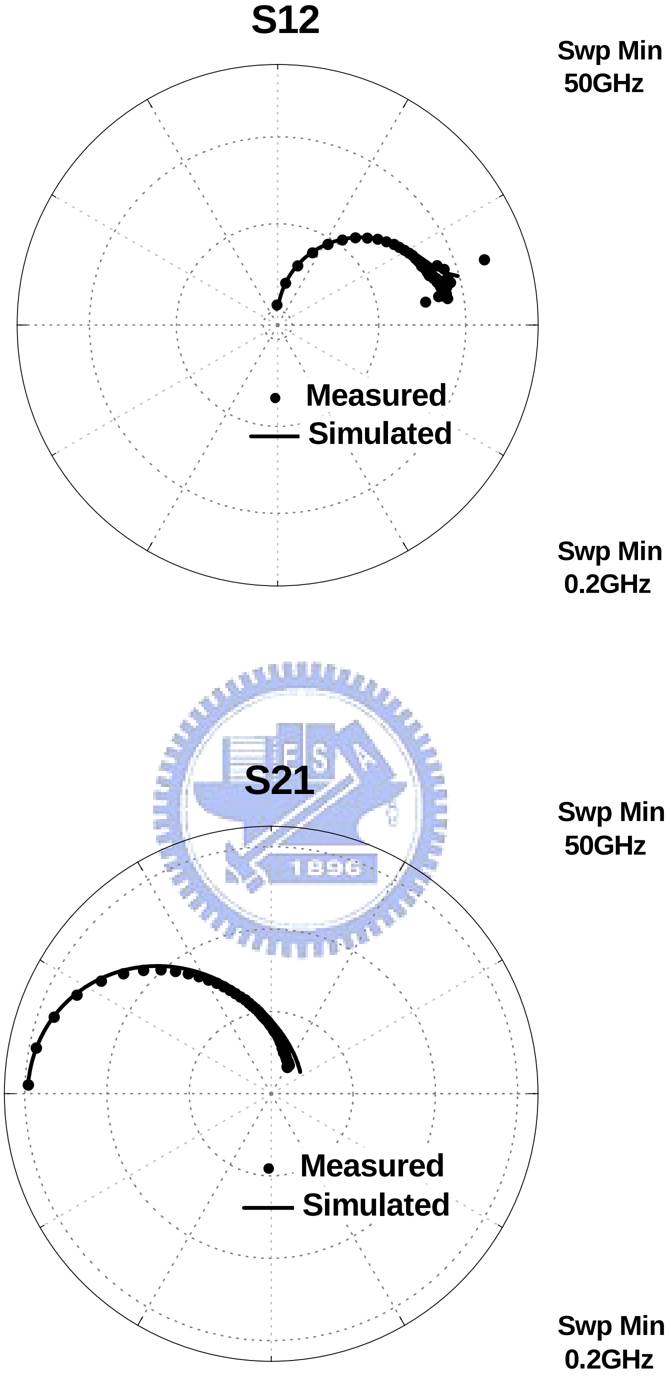

Fig. 5-5(b): Measured and modeled S-parameters of a MOSFET before stress at V_G=1V V_D=1.2V.

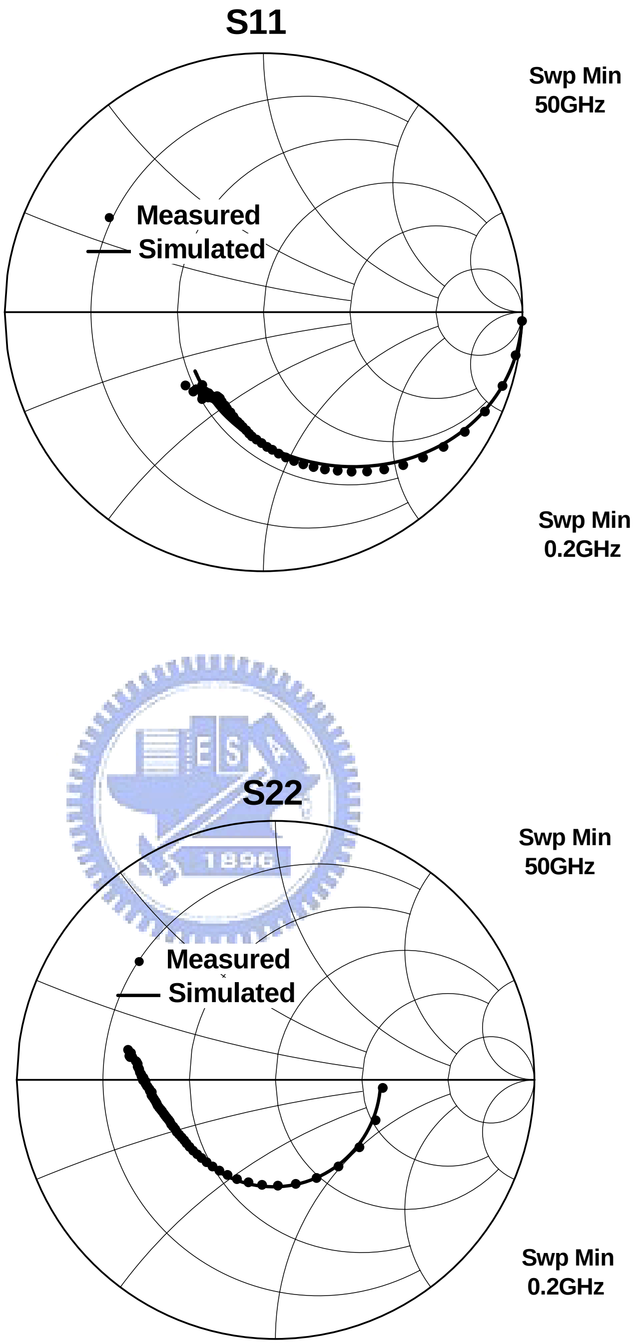

Fig. 5-6(a): Measured and Simulated S-parameters of a MOSFET after1000s HC stress

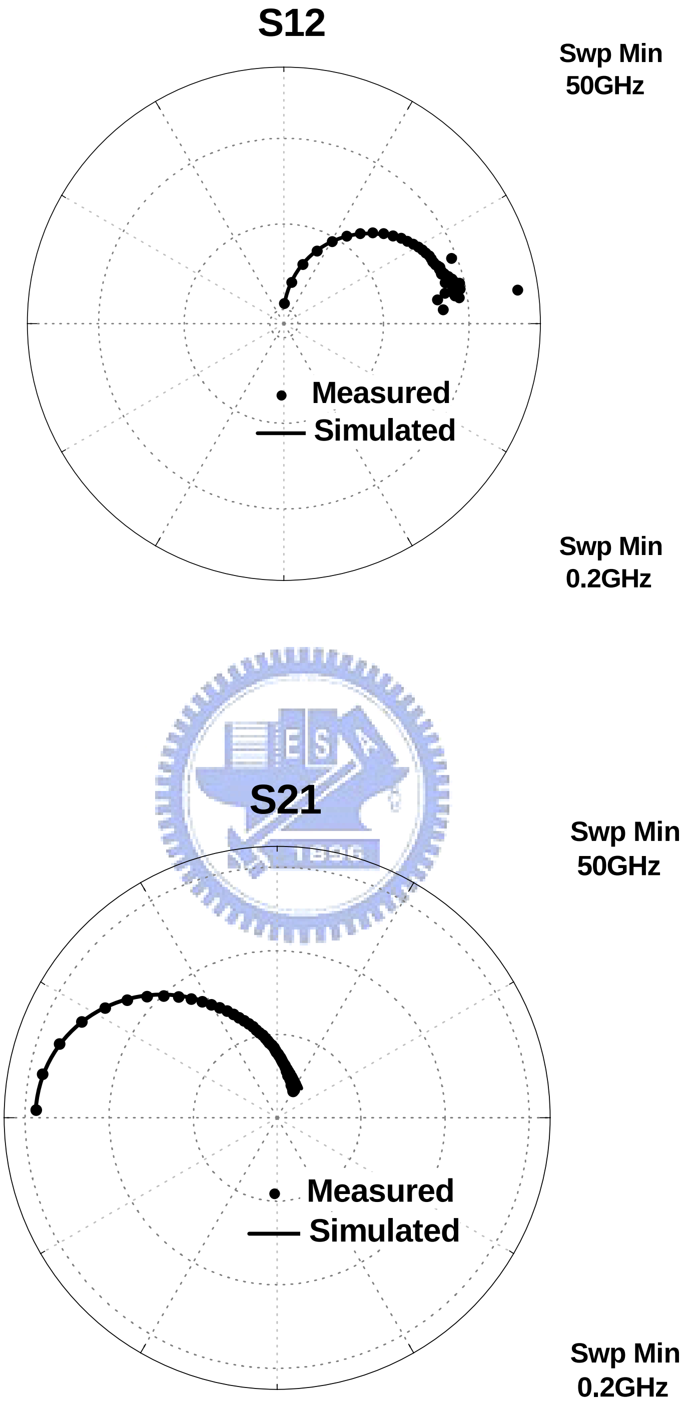

Fig. 5-6(b): Measured and Simulated S-parameters of a MOSFET after1000s HC stress

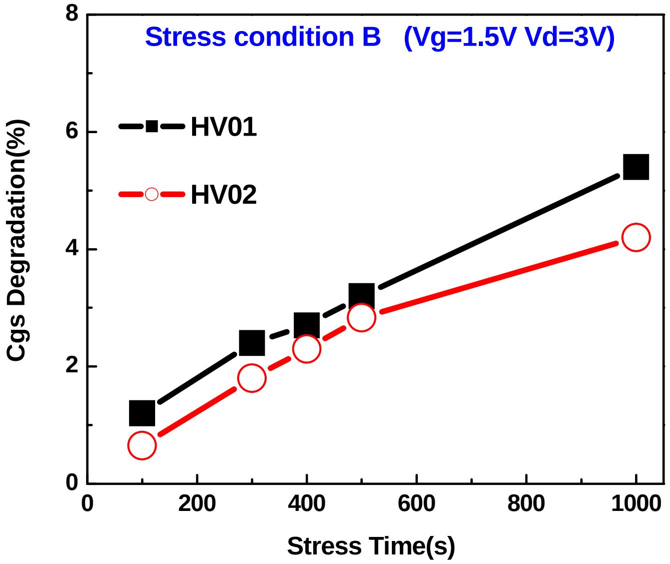

Fig. 5-7 (a)

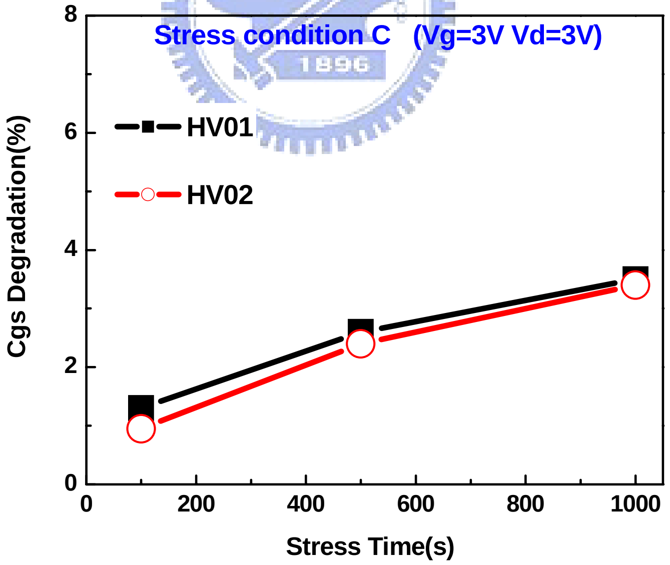

Fig. 5-7 (b)

Fig. 5-7: (a) Extracted C_{gs} *degradation of HV01 and HV02 on condition B with increasing stress time(b) Extracted* C_{gs} *degradation of HV01 and HV02 on condition C with increasing stress time*

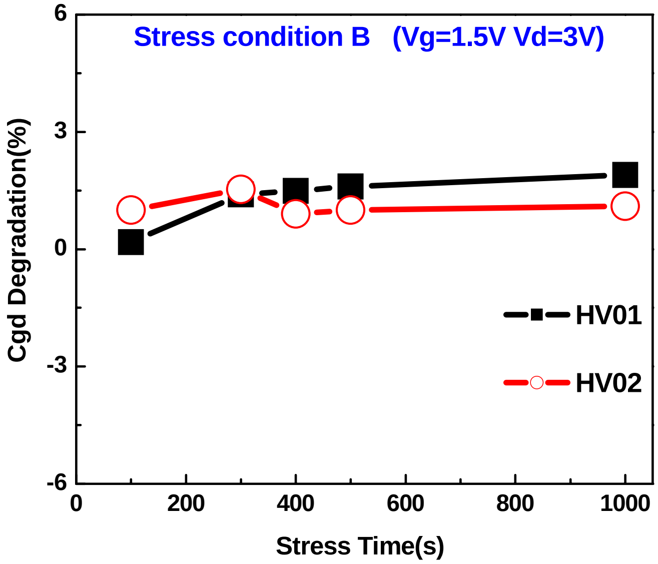

Fig. 5-8 (a)

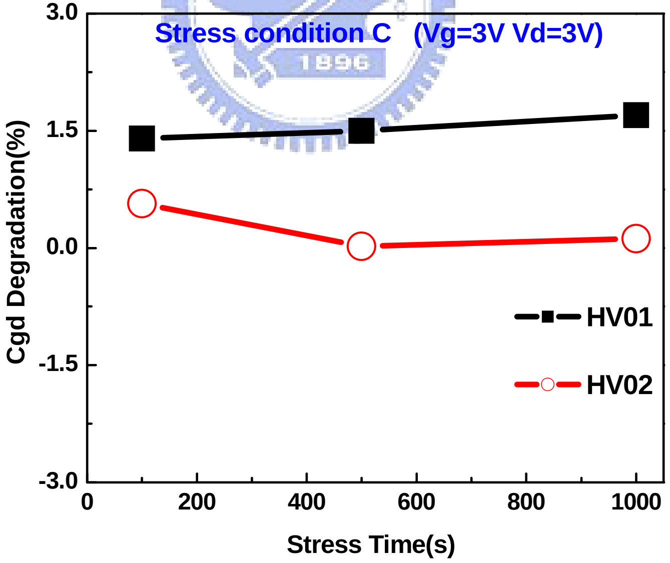

Fig. 5-8 (b)

Fig 5-8: (a) Extracted C_{gd} degradation of HV01 and HV02 on condition B with increasing stress time (b) Extracted C_{gd} degradation of HV01 and HV02 on condition C with increasing stress time

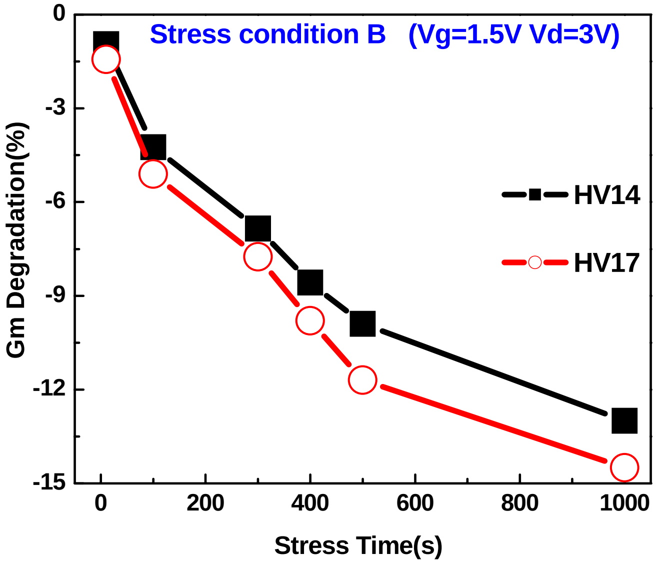

Fig. 5-9 (a)

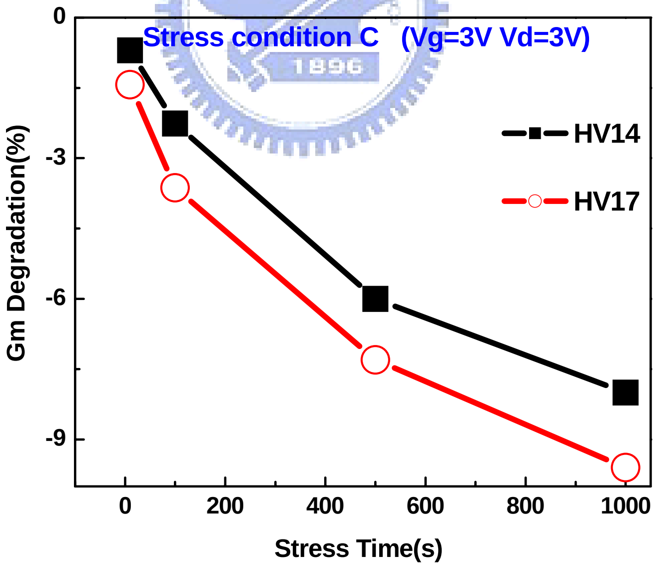

Fig. 5-9 (b)

Fig. 5-9: (a) Variations of Extracted g_{m0} *with increasing HC stress time on condition B (b) Variations of Extracted* g_{m0} *with increasing HC stress time on condition C*

Chapter 6

Conclusions

6.1 *Conclusions*

MOSFET are getting more and more important in current commercial market especially for the RF applications. In this thesis, we used a new power MOSFETs which was called PDMOS designed for RF power applications that relies on only layout scheme was investigated. It was success to improved the high frequency and power performance on traditions power MOS. And we also have established a conventional small-signal model for the MOSFETs under HC stress.

HCS reduce the transconductance, output drain current and enlarge threshold voltage of the MOSFET. Consequently, the high frequency and power characteristics will suffer degradation by those effects. In the first instance, we found that the cut-off frequency and maximum oscillation frequency all decreased after stress. Then the RF output power will suffer degradation after HCS and we find that the RF power and gain are more robust to HC effects by biasing the gate voltage to higher values. In this study, we discussed and compared two structures. The DC and RF characteristics on HV02 were better than HV01, caused the transconductance (g_m) of HV02 was higher. After HC stress, we found that HV01 had superior reliability to against this external force. Maybe the difference drain region of these two structures induced the result. Then we focused on the different HC stress conditions in the some device. The HC stress condition A and condition B had worse reliability to HC stress condition C.

Finally, from observing the small-signal model in chapter 5, the transconductance (g_{m0}), drain-to-source resistance (R_{ds}), gate-to-source capacitance (C_{gs}), and drain resistance (R_d) degrade significantly after HC stress. We also observed that Rd was crucial factor on the PDMOS structure. And the small-signal model was success to support our contention.

The results achieved from the implementation of 0.13μm MOS RF power devices demonstrate the potential power amplification capability of CMOS technologies for future integrated RF applications

References

[1] F. Schwierz, Microwave Transistors: State of the Art in 1980s, 1990s, and 2000s. A Compilation of 100 Top References, TU Ilmenau 2002.

[2] F. Schwierz and J.J. Liou, Semiconductor Devices for Wireless Communications and High-Speed Internet, Proc. SSGRR-2000, pp. 331.1-10, 2000.

[3] F. Schwierz and J.J. Liou, Semiconductor Devices for RF Applications: "Evolution and Current Status", Microelectron. Reliab, pp. 145-168, 2001.

[4] A. A. Abidi, "RF CMOS comes of age," IEEE J. Solid-State Circuits., vol. 39, no. 4, pp. 549-561, April 2004

[5] Pierre H.Woerlee, Mathijs J. Knitel, "RF CMOS Performance Trends," IEEE Trans. Electron Devices, Vol 8, pp. 1778-1782,2001.

[6] E.Morifujiet al, "Future Perspective and Scaling Down Roadmap of RF CMOS", Symposium of VLSI Circuits, pp. 165-166, 1999.

[7] Liou, J.J.; Schwierz, F, "RF MOSFET: Recent Advance and Future Trends" Electron Devices and Solid-State Circuits, pp. 185 – 192, 2003.

[8] H. Hara, Y. Okamoto and H. Ohnuma, "A New Instability in MOS Transistors Caused by Hot Electron and Hole Injection from Drain Avalanche Plasma into Gate Oxide,"Japanese Journal of Applied Physics, Vol. 9, pp. 1103-1112, 1970.

[9] S. A. Abbas and R. C. Dockerty; "Hot-carriers instability in IGFET's" Applied Physics Letter, Vol. 27, NO. 3, pp. 147-148, 1975.

[10] T.H. Ning, C. M. Osburn and H. N. Yu "Effect of Electron Trapping on IGFET Characteristics" Journal of Electronic Materials, Vol. 6, NO. 2, pp: 65-76, 1976.

[11] Qiang Li, Yuan Chen, "RF Circuit Performance Degradation Due to Soft Breakdown and Hot-Carrier Effect in Deep-Submicrometer CMOS Technology" *IEEE Transcations on Microwave Theory and Techniques*, Vol. 49, NO. 9, pp. 1546-1551, 2001.

[12] S. Tam, C Hu "Luck-Electron Model of Channel Hot Electrons Injection in MOSFETs *IEEE Transactions on Electron Device*, Vol. 31, NO. 9, pp. 1116-1125, 1984.

[13] E. Takeda, Y. Nakagome, H. Kumes, "A New Hot carrier Injection a Device Degradation in Submicron MOSFETs " *IEE Proceedings*, Vol. 130, NO.3, pp.144-149,1983.

[14] S. M. Sze and Kwok K. Ng, "Physics of semiconductor devices" 3rd Edition, New York: Wiley (2007)

[15] Taur Ning, "Fundamentals of Modern VLSI Devices" CAMBERIDGE, 1998, chapter 3.

[16] Sheng-Yi Huang, Kun-Ming Chen, Guo-Wei Huang, Chun-Yen Chang,"Novel Pseudo-Drain (PD) RF Power Cell in 0.13 um CMOS" *IEEE* ,Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008.

[17] C. Y. Chang and S. M. Sze, "ULSI Devices," Wiley Interscience, 2000. Chap 6.

[18] W.L. Ng and N. Toledo, "RF HCI testing methodology and lifetime model establishment," *Reliability Physics Symposium Proceedings* (IRPS), pp.1-3, 2004.

[19] Y. T. Yeow, C.H. Ling, " Observation of MOSFET degradation due to electrical stressing through gate-to-source and gate-to-drain capacitance measurement," *IEEE Electron Device Letters*, Vol.12, pp366-369, 1991.

[20] S. Lee *et al.*, "A small-signal RF model and its parameter extraction for substrate effects in RF MOSFET's," *IEEE Trans. Electron Devices*, vol. 48, pp. 1374–1379, 2001.

[21] S. C. Wang, G. W. Huang, "A Practical Method to Extract Extrinsic Parameters for the Silicon MOSFET Small-Signal Model" 2004 Workshop on Compact Modeling, 2004.

[22] S. Lee, H. K. Yu, C. S. Kim, "A novel approach to extracting small-signal model parameters ofsilicon MOSFET's," *IEEE, Microwave and Guided Wave Letters*, 1997

[23] S. Lee, H. K. Yu, C. S. Kim, “A small-signal RF model and its parameter extraction for substrate effects in RF MOSFETs” *Electron Devices, IEEE Transactions on*, 2001

[24] Y. T. Yew, C. H. Ling, “Observation of MOSFET Degradation Due to Electrical Stressing Through Gate-to-Drain Capacitance Measurement,” *IEEE Electron Device Letters*, Vol.12, NO.7, pp.366-368, 1991

[25] C. H. Ling, “A study of Hot Carrier Degradation in NMOSFET’s by Gate Capacitance and charge pumping method,” *IEEE Transaction on Electron Device*, Vol. 42, NO. 7, pp. 1321-1328, 1995.

簡 歷

姓 名: 陳勝杰

性 別: 男

出生日期: 中華民國七十一年十一月十日

籍 貫: 台 北 縣

地 址: 台北縣三峽鎮學勤路89號7樓

學 歷: 台北市立成功高中

私立大同大學 電機工程學系

國立交通大學 電子工程研究所碩士班

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