國 立 交 通 大 學

電子工程學系　　電子研究所

碩 士 論 文

鍺基板及磊晶鍺通道製作 P 型金氧半場效電晶體與電性分析研究

Studies of device fabrication and electrical characteristics of bulk Ge and epitaxial Ge channel pMOSFETs

研 究 生:陳弘森

指導教授:簡昭欣 博士

中華民國九十七年九月

鍺基板及磊晶鍺通道製作Ｐ型金氧半場效電晶體與電性分析研究

Studies of device fabrication and electrical characteristics of bulk Ge and epitaxial Ge channel pMOSFETs

研 究 生:陳弘森　　Student: Hung-Sen Chen

指導教授:簡昭欣 博士　　Advisor: Dr. Chao-Hsin Chien

國 立 交 通 大 學

電子工程學系電子研究所碩士班

碩 士 論 文

A Thesis
Submitted to Department of Electronics Engineering & Institute of Electronics
College of Electrical and Computer Engineering
National Chiao Tung University
in partial Fulfillment of the Requirements
for the Degree of
Master
in
Electronics Engineering & Institute of Electronics

September 2008
Hsinchu, Taiwan, Republic of China

中 華 民 國 九 十 七 年 九 月

鍺基板及磊晶鍺通道製作P型金氧半場效電晶體與電性分析研究

研 究 生:陳弘森　　指導教授:簡昭欣 博士

國立交通大學

電子工程學系電子研究所碩士班

摘要

我們已經成功地利用低溫的 Forming Gas Anneal (FGA) 技術來改善以鍺為基板的金氧半場效電晶體。從電性的分析中，我們發現到在 FGA 技術中 300℃ 為較佳的條件，由於有最低的漏電流。然而在溫度超過 300℃ 後，元件中的漏電流會明顯的上升，尤其是在溫度為 400℃。我們認為是因為在接面附近產生缺陷所導致的。而缺陷的產生是因為鋁融進鍺基板和鍺在高溫會向外擴散所造成的。FGA 技術中 300℃ 還有其他較好的特性。譬如說，有較好的閘集介電質和鍺基板的界面，所以導致有最低的界面態位密度(interface state density)。由於，300℃ 有較低的漏電流，所以使得在這溫度之下的元件有較大的開關比。雖然 300℃ 有上述等的優點，但是，它的載子遷移率卻相對 400℃ 來說卻小的許多。我們認為是因為源集和汲集電阻所造成的。

經過 400℃ 處理之後的元件，雖然會造成閘集介電質和鍺基板的界面退化使得界面態

位密度變高。但是因為有最低的源集和汲集電阻所以導致有最高的電洞遷移率。為了要獲得這兩種溫度之下的好處，所以我們認為改變製程的順序或許是個解決的辦法。

接著為了有更好的界面特性以及大尺寸可應用於矽的製程中，我們使用以矽為基板，利用超高真空化學氣相沉積系統疊上矽鍺的緩衝層、鍺通道，以及不同厚度的矽的保護層。但是由於我們並沒有抓到較好的薄膜沉積條件，使得矽與鍺的接面並不理想，造成較高的接面漏電流。而且，我們也發現到矽保護層的厚度愈厚，電性的表現是愈差的。所以我們也認為較高的漏電流也有可能是因為在矽保護層內的雜質並不能被完全活化所引起的。所以我們認為要獲得更好的金氧半場效電晶體的特性，我們必須要找出更好的薄膜沉積條件以及必需把矽保護層的厚度降低到 1 奈米之下。

Studies of device fabrication and electrical characteristics of bulk Ge and epitaxial Ge channel pMOSFETs

Student: Hung-Sen Chen Advisor: Dr. Chao-Hsin Chien

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University, Hsinchu, Taiwan

Abstract

We had already employed low temperature Forming Gas Anneal (FGA) technique to improve the characteristics of Ge bulk p-MOSFETs. We found out the better temperature condition as 300^{o}C FGA from the electric analysis, due to the lower OFF current. However, OFF current in devices obviously increased when the FGA temperature was over 300^{o}C, especially in 400^{o}C. We expected the cause of higher leakage current was the defects were generated near the p^{+}-n junction region. The causes of generation of defects were Aluminum incorporated into Ge bulk and Ge out-diffusion in high temperature. 300^{o}C FGA samples had other better characteristics. For example, it had the better interface quality between the Ge substrate and gate dielectric resulted in the lower interface state density in our works. Due to

the lower OFF current in 300°C FGA samples, it had the larger ON/OFF ratio. Although, 300°C FGA samples had several advantages, the hole mobility is smaller than 400°C FGA samples. We though the cause of smaller mobility was the source/drain series resistance.

Samples after 400°C FGA would degrade the interface quality between the Ge bulk and gate dielectric resulted in higher interface state density. But it had the lowest source/drain resistance led to the highest hole mobility in our works. In order to obtainment of the advantages in two different temperatures, we thought the change in process orders was a solution to solve this problem. In order to obtainment of better interface quality and application of larger size in Si process, we utilized ultra high vacuum chemical vapor deposition (UHVCVD) to deposit SiGe buffer layer, Ge channel, and Si capping layers top of Si substrate. But we didn't obtain the better deposition conditions to deposit Ge and Si capping layer such that our p^+-n junctions in this substrate were higher. However, we also found out the thicker Si capping layer would cause the poor characteristics in our samples. Hence, we also expected the higher leakage current was resulted in the implant impurities in Si capping layer were not completely removed. In order to obtainment of better characteristics in Ge p-MOSFETS, we must find out the better deposition conditions and reduce the thickness of Si capping layer down to 1 nm.

誌 謝

兩年的碩士生涯在此即將告一段落了。回首這兩年，有許多值得往後再三回憶的點滴。在碩士的第一年，或許是那貪玩的個性使然，所以並沒有很認真於課業及實驗上。以致於在碩二的一整年裡必須加緊補足以前的不足，造成我在今年一整年過的格外的辛苦。但終究還是熬過來了。首先，我要感謝的是我的指導老師簡昭欣教授。在這兩年生活中，老師不僅在學業上不吝嗇地指導我，並且在生活態度及人生觀上都給我很大的啟示。讓我在這兩年中，不僅僅從學校學到專業的知識也或多或少的改變我急躁的個性。兆欽學長，是指導我最用心的學長。在碩二的一整年中，學長非常的用心指導我，不管是在做實驗或是在電性的分析上都給我很大的幫助。而且，在最後的幾個月，學長犧牲他自己的睡眠時間和我一起完成我的實驗數據的分析和探討，讓我十分的感動，學長謝謝你。

實驗室的夥伴們(欣哲、効諭、敬倫、猛飛、小胖、登偉、宇彥、家豪學長），沒有你們我想我的碩士班生涯一定少了許多的回憶。

林鴻志老師 group 裡的學長及學弟們(子儀學長、Benson、大師、樟樟、哲民學長)感謝你們給我大力的支持，讓我盡情地使用你們的儀器且跟我討論一些半導體上的知識，使我對元件上有更進一步的了解。

江忠佑同學，是我在電子所認識到的一位好朋友。感謝你在這兩年中陪我一起渡過，跟我一起分享歡樂與困難。還記得我們一起到屏東吃那好吃的旗魚黑輪，還記得我們一起去球場打球的時光嗎?往後的日子也繼續讓我們互相的扶持下去吧!

君帆，我的女朋友，沒有妳，我想我一定熬不過這一年的歲月。很謝謝妳一直鼓勵我，支持我，並且聽我訴苦和抱怨，讓我有繼續支撐下去的勇氣和動力，希望接下來的日子，我也能繼續守在妳身邊當你的守護神。

爸媽，沒有你們的支持(不管是在精神或是金錢上），我想我這個碩士頭銜是拿不到的，這張畢業證書就是我給你們最好的禮物。

有太多的人要感謝(儀科中心的學長們和組長)沒有你們的幫助，我無法順利的完成我的學業，大家，謝謝你們，我愛你們。

Contents

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Table Captions

Chapter 1

Chapter 3

Chapter 1

Introduction

1-1 General Background

Over the last four decades, the dominate development of the semiconductor industry has been focused on silicon very-large-scale-integration (VLSI) technology. The sustained growth in VLSI technology is supported by the continued scaling of transistors to smaller dimensions. With the reduction in device dimensions of metal-oxide-semiconductor field effect transistors (MOSFETs), silicon dioxide (SiO_2) films used as a gate dielectric have been scaled down to keep the same control over the channel. Devices with the thinner dielectric could improve the short channel effects. Therefore, the thickness of gate dielectric must continue to be scaled down for the gate length scaling. When the SiO_2 thickness decreases to less than 20Å, the gate leakage current density becomes significantly high (>1A/cm^2) because of the direct tunneling effect, as show in Fig 1.1, which shows measured and simulated I_G-V_G characteristics under inversion conditions of SiO_2 nMOSFETs [1]. Hence it has become apparent that the continued scaling of Si CMOS devices would finally lead to a physical obstacle. Therefore, various approaches are being investigated to alleviate the tremendous pressure on continuously improving the performance of scaled device. One of the solutions is that we can use high

dielectric constant (high-*k*) materials to replace SiO_2. Because high-*k* dielectrics can be several times thicker than SiO_2, they reduce gate leakage by over 100 times. Another is using higher carrier mobility as channel materials such as Ge or III-V compounds. In the recent years, Ge attracts great attention because it offers higher electron (2.5x) and hole mobility (4x) than Si, as shown in Table 1.1. However, from the technology point of view, the developments of Ge MOSFETs have been blocked for decades due to the absence of a good thermally grown oxide on Ge. Recently, the successful development of high-*k* dielectrics on Si has facilitated the development of the Ge MOSFETs because it demonstrates that the gate dielectrics are no longer restricted to the thermal oxide. There have been many reports on Ge MOS structures using Al_2O_3 [3], HfO_2 [4] , Dy_2O_3 [5], HfON, and ZrO_2 [6]. However, there is an intrinsic problem in the formation of the gate dielectric on Ge substrate. Germanium oxide is thermally unstable, and water soluble. Hence, minimizing the formation of GeO_x at the interface between high-k dielectric and Ge substrate is a critical issue to form high quality stack on Ge. Surface treatments before high-*k* dielectrics deposition is one of the solution for the problem. Surface treatments include annealing Ge in an NH_3 ambient and annealing in a SiH_4 ambient. The second way removes the native germanium oxide and passivates the germanium surface by an ultra-thin Si cap. They were also reported to be essential to achieve better device performance. Furthermore, Ge had several intrinsic problems such as the band-gap in Ge is smaller than in Si and the intrinsic carrier concentration in Ge is three

orders higher than in Si. They would lead to the higher reverse leakage current. Another, the density of Ge is 3 times heavier than Si such that Ge bulk wafers were applied to Si process equipment is a big challenge.

1-2 Motivation

In order to continuously improve the performance of scaled device, Ge substrates have been used. However, Ge has several practical problems. First, unlike Si, Ge lacks a sufficiently stable thermally grown oxide. Ge oxides (e.g. GeO_x and GeO_2) are either water soluble or volatile, they are easily rinsed off or sublime during the fabrication process [7], [8]. Second, Ge/oxide interfaces are known to exhibit lower quality than Si/oxide interfaces and results in a difficulty to form a gate stack structure on Ge with good interface qualities. Third, Ge has a much smaller direct band gap compared to Si which may give rise to higher leakage.

Recently, germanium MOS structures with high-*k* gate dielectrics have been reported. It demonstrates that the gate dielectrics are no longer restricted to the substrate's thermally grown oxide. We adopt atomic layer deposition (ALD) system to grow Al_2O_3 as the gate dielectric. Atomic layer deposition (ALD) system has lots of excellent abilities, such as almost 100% step coverage, accurate thickness control, large area uniformity, excellent

process stability, and low processing temperatures. Atomic layer deposition (ALD) system just has only one problem is that the slower deposition rate. But we can use the multi-chamber to solve this problem. We chose the Al_2O_3 as the gate insulator due to the similarities of the band-gap, band alignment and thermal stability material characteristics to the SiO_2. Also, Al_2O_3 has a higher dielectric constant value about 2.5 times than SiO_2.

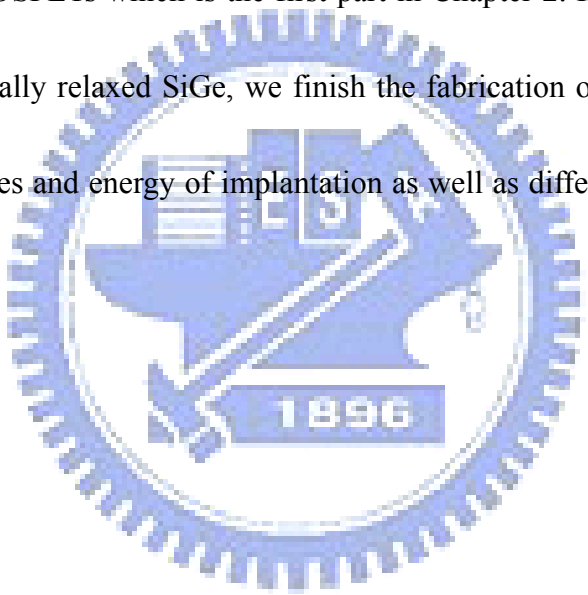
Hydrogenation can be used to significantly decrease the density of interface states, with most of the improvements resulting from passivating the Si dangling bonds (DB) through the formation of Si-H bonds [9]. A recent study reported that high temperature forming gas anneal (FGA) treated on Ge showed significant improvements in the carrier mobility, drive current, and subthreshold slopes of metal-oxide-semiconductor field-effect transistors with HfO_2 gate stack [10]. These improvements can be attributed to the improvements of the interface quality by lowering both interface state density and interface charges.

In our thesis, we employed the low-temperature forming gas anneal to improve the interface between the Ge substrate and high-*k* gate dielectrics. It is found that the low-temperature (≦ 400℃) forming gas anneal can also improve the interface quality by slightly reducing the D_{it}. The reduction of D_{it} can improve the drive current, subthreshold slope, effective mobility (μ_{eff}) and transconductance (G_m). The improvements are represented in the chapter 2. Finally, we used the ultra-thin Si capping layer on the top of Ge channel to prevent Ge native oxides from forming (e.g. GeO_x and GeO_2). Furthermore, it can also decrease the number of the interface

state density and increase both the effective mobility (μ_{eff}) and drive current [11].

1-3 Organization of the thesis

In this thesis, it can be divided into two parts. First, we fabricated the pMOSFETs with the Ge bulk and ALD Al_2O_3 as the gate dielectric in different FGA temperatures ; then, we measure the essential electrical performances, constant voltage stress (CVS) , and charge pumping of Ge pMOSFETs which is the first part in Chapter 2. In the second part, using the strained-Ge on partially relaxed SiGe, we finish the fabrication of the pn junction formation with different dosages and energy of implantation as well as different annealing temperatures and times.



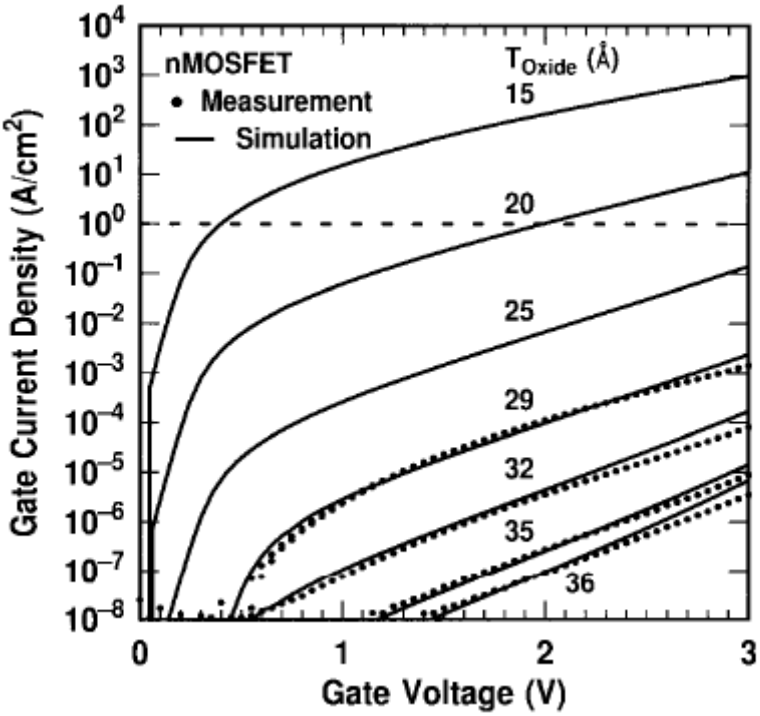


Figure 1.1 Measured and simulated I_G-V_G characteristics under inversion conditions of SiO_2 nMOSFETs [1].

sub. material	Ge	Si	GaAs
μ_p (cm^2/ V- s)	1900	480	400
μ_n (cm^2/ V- s)	3900	1350	8500
E_g (eV)	0.66	1.12	1.42
n_i (cm-3)	$2.4x10^{13}$	$1.5x10^{10}$	$1.8x10^{6}$
ε	16	11.7	13.1
native oxide	GeO_x	SiO_2	As_2O_3 ,Ga_2O_3
density (g/cm^3)	5.33	2.33	5.32

Table 1-1 Si, Ge, and GaAs properties at T=300 K [2].

Method	ALD	MBE	CVD	Sputter	Evapor	PLD
Thickness Uniformity	good	fair	good	good	fair	fair
Film Density	good	good	good	good	poor	good
Step Coverage	good	poor	varies	poor	poor	poor
Interface Quality	good	good	varies	poor	good	varies
Number of Materials	fair	good	poor	good	fair	poor
Low Temp. Deposition	good	good	varies	good	good	good
Deposition Rate	fair	poor	good	good	good	good
Industrial Applicability	good	fair	good	good	good	poor

ALD = atomic layer deposition, MBE = molecular beam epitaxy.
CVD = chemical vapor deposition, PLD = pulsed laser deposition.

Fig. 1-2 The characteristics comparison with several depositing method.

Chapter 2

Low temperature Forming Gas Anneal with Ge p-MOSFETs

2-1 Introduction

In Chapter 2, we investigated the forming gas annealing (FGA) on the electrical characteristics of Ge PMOSFETs. First of all, we should understand the reason why we employed FGA technique. Owing to the interface quality between Ge substrate and high-*k* gate dielectric poor than Si, this degrading phenomenon led to reduce carrier mobility and accordingly lower the operating speed of devices. Then, we employed FGA technique to improve the problem of interface quality. It was reported that high-temperature (500~600°C) FGA successfully improved the interface quality between Si substrate and high-*k* gate dielectric [10]. From this report, we knew that high-temperature FGA had been found to be effective in improving the interface quality by lowering both interface state density (D_{it}) and interface charge. After FGA, the interface state density (Dit) was reduced 4 times. A few years later, high-temperature FGA on the GeOI substrates has been reported [12]. From this report, we knew that the devices after high-temperature FGA exhibited the better carrier mobility, with the interface trap density and the interface fixed charge as low as $10^{10}q/cm^2$. However,

the previous reports are in reference to high-temperature (>400°C) for Ge devices. In this chapter, we used low-temperature (≦400°C) FGA on the Ge pMOSFETs. We found that the devices can be improved in many aspects such as sub-threshold slop, D_{it}, on-off ratio after low-temperature FGA. At the beginning, we showed the characteristics of pn junction after FGA (300, 350, 400 °C). We found that the better FGA temperature is 300 °C because of the lower junction leakage current. Then, we showed the electrical characteristics, such as I_d-V_g, I_d-V_d, and C-V, and discussed the parameters extracted from the essential electrical measurements, such as sub-threshold swing (S.S), threshold voltage (V_{th}), source drain series resistance (R_{SD}), dopant in-diffusion length ($\triangle L$), and effective mobility (μ_{eff}). We also utilized two methods- Conductance method, and Charge-Pumping to estimate the number of D_{it} exists near the substrate surface.

2-2 Experimental Procedures

The starting wafers for the experiments were Sb-doped (concentration~$1.5x10^{14}cm^{-3}$) with a resistivity of 8-13 Ohm cm. The native oxide (GeO_x) was removed by dipping the samples in a diluted HF solution ($HF:H_2O=1:30$) for 5 minutes, followed by rinsing in de-ionized water (D.I water) 10 minutes and N_2 drying. After that, we used a plasma enhanced chemical vapor deposition (PECVD) system to deposit the field oxide SiO_2 (thickness~4200 Å). Then, we defined the source drain(S/D) region by Mask 1 and etched SiO_2 by Buffer Oxide Etching (BOE). To form a boron (B) doped P^+-N junction region for restricting the flow of drain current just under the surface, the samples were implanted B^+ with tilt: 7^o and twist: 22^o. The implant energy was 60 keV while the implant dose was $1x10^{15}$ atoms/cm^2. Before removing the dummy gate by Mask 2, we activated the B-doped region. Annealing of the samples was performed in a N_2 atmosphere in the JETFIRST RTP system at 500 °C or 550 °C annealing temperatures. As soon as the dummy gate was removed, we used an atomic-layer-deposition (ALD) system to grow the gate dielectric (Al_2O_3) at ~170 °C with 100 deposition cycles in Instrument Technology Research Center (ITRS). In this ALD system, tri-methyl-aluminum (TMA), $Al(CH_3)_3$, and H_2O were chosen as the metal source and oxidant that were pulsed alternatively into the chamber for 1 sec; and per pulse separated by N_2 purge of 10 sec to remove residual reactants during the process. During each cycle, the chamber was held at a constant pressure~20 torr. Then, we opened the contact hole by Mask 3. Subsequently, we

coated aluminum (Al) on the wafers with the help of thermal coater. After that coating was done, we used the Mask 4 to define the metal pads. For further improving the device characteristics, some Ge devices were treated in forming gas annealing (FGA) (N_2/H_2, 95:5 %) at 300, 350 and 400 °C for 30 minutes. The overall fabrication processes of the Ge p-MOSFETs were illustrated in Figure 2-1. After the fabrication of pMOSFETs, we measured the capacitance-voltage (C-V) and current-voltage (I-V) characteristics by Agilent 4284 LCR meter and Keithley 4200 semiconductor characterization, respectively. From the I_d-V_g curves, the main parameters of devices, such as threshold voltage (V_t), On-Off ratio, and subthreshold swing (SS), were obtained. We also estimated the density of interface state (D_{it}) from G-V characteristic and charge pumping. In order to investigate the degradation of the device performances, they were undergone a constant gate voltage stressing (CVS) at -3V and -3.2V.

2-3 Results and Discussion

Figure 2-2 illustrates the effect of forming gas anneal (FGA) on 100 μm^2 p^+ n diodes with different activation conditions. (a) 500℃ and (b) 550℃. The activations were done for 30s. We find that the forward current density in our cases is lower than others had been reported [13]. We think the cause of lower forward current is the lower bulk doping level. The lower bulk doping level leads the higher series resistance and reduces the forward current. And the lower bulk doping level also brings out the higher reverse leakage current. Because the lower bulk doping level causes the huge bulk generation current such that the higher leakage current in our samples. From (a), we find that the reverse current of the p^+ n diode after 300℃ FGA is smaller than non-FGA sample while forward current is almost equivalent to others. While the FGA temperature is larger than 300℃ (350 and 400℃), the reverse current is increased immediately. Specially, the reverse current of 400℃ FGA is one order than non- FGA sample at $V_{junc.}$=-1V. We can see the analogous effect from Fig 2-2 (b). Figure 2-3 illustrates the reverse current density at V_{junc}= -1V with different FGA conditions. As we have mentioned, the reverse current density are increased after higher FGA temperature (>300℃). The reverse current after 300℃ FGA is reduced because of the decrease of the defects. Forming gas annealing ambient is H_2 and N_2. Hydrogen (H_2) is confirmed to passivate the defects such that

the reverse current reduced. The reason for the increasing reverse current after higher FGA temperature (>300℃) is that Ge out-diffusion and Al incorporation in Ge bulk introduce defects near the p^+ n junction. Figure 2-4 is published on 2008 Electrochem. Solid-State Lette. from IMEC and ASM Belgium [14]. It shows that the temperature >300℃, large-scale Ge voiding and germanide overgrowth occur because of the out-diffusion of Ge. Figure 2-5 and 2-6 are the channel length dependent I_d-V_g and I_d-V_d electrical characteristics of the 500℃ activated Ge PMOSFETs with different FGA temperatures, respectively. I_d-V_g characteristic of the Al_2O_3 PMOSFETs with 500℃ activation for three different FGA temperatures is shown in Figure 2-7. It shows some interesting events in Figure 2-7. First, I_{off} current is decreased after 300℃ FGA compared to non- FGA sample. However, I_{off} current is increased after higher FGA temperature (400℃) compared to non- FGA sample and 300℃ FGA sample. Second, the 300℃ FGA sample has the steeper slop when V_d is small. Finally, we can find that forming gas annealing shifts the curves of I_d-V_g. We explain the results in order. The reduction of I_{off} current after 300℃ FGA is attributed to H_2 passivates the interface state density (D_{it}: 7.53×10^{11} $eV^{-1}cm^{-2}$ after 300℃ FGA vs. 1.07×10^{12} $eV^{-1}cm^{-2}$ before) and improve the p^+ n junction. But the higher temperature (400℃) introduces Ge out-diffusion in p^+ n junction such that I_{off} current is increased. The steeper slope of I_d-V_g curve after 300℃ FGA is attributed to the lower D_{it}. Finally, the shift of the I_d-V_g curve is attributed to threshold voltage shift. I_d-V_d characteristics of the Al_2O_3 PMOSFETs with 500℃ activation for three different

FGA temperatures are shown in Figure 2-8.

Based on the first order current-voltage approximation, the drive current I_D for a MOSFET in the saturation region can be written as below

$$I_D = \frac{W\mu_n C_{ox}}{2L}(V_{GS} - V_T)^2 \quad (1.1)$$

Where C_{ox} is the gate oxide capacitance and mainly determined by the permittivity and the thickness of the gate insulator. μ_n is the mobility for the electrons or holes. W and L are the channel width and length, respectively. V_{GS} is the applied gate-to-source voltage, and V_T is the threshold voltage. From the above equation, the drain current I_d is affected by C_{ox} and μ_n. The higher drain current I_d after FGA is illustrated in Figure 2-8. We mainly attribute the higher drain current I_d to higher mobility and increasing C_{ox}. However, the higher mobility is attributed to the lower D_{it} and the lower S/D series resistance. The effective mobility of the Ge PMOSFETs with different FGA temperatures are illustrated in Figure 2-9(a). References with HfO_2/Ge (SP and SN) [15] and Ge/Si after PMA (H_2) [16] are compared with our data are illustrated in Figure 2-9(b). The extracted effective hole mobility of the MOSFETs equation is mentioned as below:

$$\mu_{eff} = \frac{g_d L}{WQ_n} \quad (1.2)$$

Where $Q_n = C_{ox}(V_{GS}-V_T)$ and the drain conductance g_d is defined as

$$g_d = \frac{\partial I_d}{\partial V_{DS}}\Big|_{V_{GS}=\text{constant}} \quad (1.3)$$

C_{ox} is obtained by C-V measurement for Ge PMOSFET at f (frequency)=10 kHz and g_d is obtained by I_d-V_g at V_d=-50 mV. From Figure 2-9(a), we find that the mobility after FGA is larger than non-FGA. Specially, the mobility after 400℃ FGA is almost 2 times than non-FGA in all electric field. We can find that our device characteristics are not bad in comparison with others in Figure 2-9(b). However, the C_{ox} is higher after FGA is showed in Figure 2-10. We consider that mobility is affected by C_{ox} in our work. I_d-V_g and I_d-V_d characteristics are shown in Figure 2-11 and 2-12, respectively. In Figure 2-11 and 2-12, it shows the similar subthreshold slope and drive current except I_{off} current for 500 and 550℃ samples. I_{off} current at 550 ℃ sample is larger than 500℃ sample 1.6 times while V_g is negative. Figure 2-13 shows V_{th} characteristics of the Al_2O_3 Ge PMOSFETs with different FGA and activation temperatures. The continuing positive shift of V_{th} is related to Ge out-diffusion [17], [18], [19]. Two possible incorporation mechanism: (a) out-diffusion of gaseous GeO species from the substrate and downward into the high-k layer through airborne transportation and (b) GeO volatilization from the IL and top surface of the Ge substrate [19]. The incorporation mechanism possibly causes V_{FB} shift by inducing negative fixed charges near the interface and into the dielectric.

$$R_m = \frac{V_d}{I_d} = R_{ch} + R_{SD} = \frac{L - \Delta L}{W_{eff} \cdot \mu_{eff} \cdot C_{ox} \cdot (V_g - V_{th})} + R_{SD} \quad (1.4)$$

Where R_{ch} is channel resistance and R_{SD} is source drain (S/D) series resistance. Figure 2-14 shows the R_m-L_g curves for extraction of R_{SD} and ΔL. (a), (b), and (c) are different FGA temperatures at 500℃ activation. (d) is 300℃ FGA with 550℃ activation. We find that the S/D series resistance is reduced after FGA. The S/D series resistance of as-deposited sample is 194Ω and 400℃ is 123Ω. The decreasing S/D series resistance attributes to higher temperature improves the interface between the Ge substrate and metal pads by the formation of alloy. However, the reducing S/D series resistance improves the drive current (I_D) and effective mobility (μ_{eff}) as mentioned previously. It is illustrated in Figure 2-15 that the extraction of R_{SD} and ΔL with different FGA conditions at 500 and 550℃. Figure 2-16 (a),(b) show D_{it} calculated from the Conductance and Charge pumping method, respectively. We can find the similar trend from the two figures. After 300℃ FGA, D_{it} is reduced slightly and D_{it} is increased after higher FGA temperature. It means that 300℃ FGA indeed improve the interface between the substrate and the gate insulator by H_2 and higher FGA temperature (≧400℃) degrade the interface. Figure 2-17 shows charge pumping current v.s V_g with different FGA temperatures was evaluated at f =1MHz. We also find that the I_{cp} current is decreased after FGA treatment in comparison with as-deposited sample. Figure 2-18 (a) shows the on/off ratio of Ge PMOSFETs with different FGA and activation temperatures. I_{on} and I_{off} are extracted at V_{th}+0.8V and V_{th}-4V, respectively. The 300℃ FGA sample have higher value at on/off ratio about 10^3. However, the 400℃ FGA samples have the higher drive

current than others. As a result of the junction leakage, it degrades the on/off ratio. From Figure 2-18 (b), the minimum of sub-threshold slope of Ge PMOSFET is 300℃ FGA sample because of the minimum of D_{it}.

BTI is an important reliability issue of high-k gate dielectrics on silicon. Consequently, it is necessary to evaluate the BTI property of the high-k gate dielectrics on germanium. It is measured in MOSFETs biased under inversion. A negative voltage (V_{stress}) was applied to the gate of a device, while the S/D and the substrate were grounded. I_d-V_g and I_d-V_d measurement were conducted during the stress intervals. The measurement time between the two consecutive stresses was ensured to be minimal in order to reduce the possible de-trapping of the oxide trapped charge. Figure 2-19 show the NBTI degradation of I_d degradation [Figure 2-19 (a)] and G_m degradation [Figure 2-19 (b)] by stress for Ge PMOSFETs. It should be noted that non-FGA samples are subjected to severer the I_d and G_m degradations. Figure 2-20 show the NBTI degradation of V_{th} shift [Figure 2-20 (a)] and SS degradation [Figure 2-20 (b)] by stress for Ge PMOSFETs. It also represents that non-FGA samples have a higher V_{th} shift and SS increase in comparison with FGA samples. It means that non-FGA samples are subjected to NBTI degradation involves interface-trap generation. By employing FGA, Ge PMOSFETs show almost no change in sub-threshold swing. It suggests that the immunity from interface-trap degradation of Ge PMOSFETs could be achieved.

2-4 Summary

We already demonstrated a Ge bulk PMOSFETs by the standard 4 mask process. Most important parameters such as I_d-V_g, I_d-V_d, effective mobility, V_{th}, sub-threshold swing and so on are showed in this chapter. To further ensure the FGA technique can improve the interface between the Ge substrate and gate dielectric, we employed NBTI. It showed that 300℃ FGA can improve slightly the interface between Ge bulk and Al_2O_3 gate dielectric by lowering D_{it}. After 300℃ FGA, the S/D series resistance also reduced from 194 Ω to 181 Ω. Since the improvements of the interface quality and S/D contact, the drive current the mobility increased. But the higher temperature FGA (>300℃) introduced the Ge out-diffusion such that the junction leakage current increased. Although the junction leakage current increased, the S/D series resistance decreased significantly and the interface state density (D_{it}) increased slightly. After 400℃ FGA, it showed the highest mobility in comparison with others in our work. Stressing at V_g=-3.2 or -3V, it showed that FGA samples had smaller V_{th} shift, I_d and G_m degradation and change of sub-threshold swing compared with non-FGA samples.

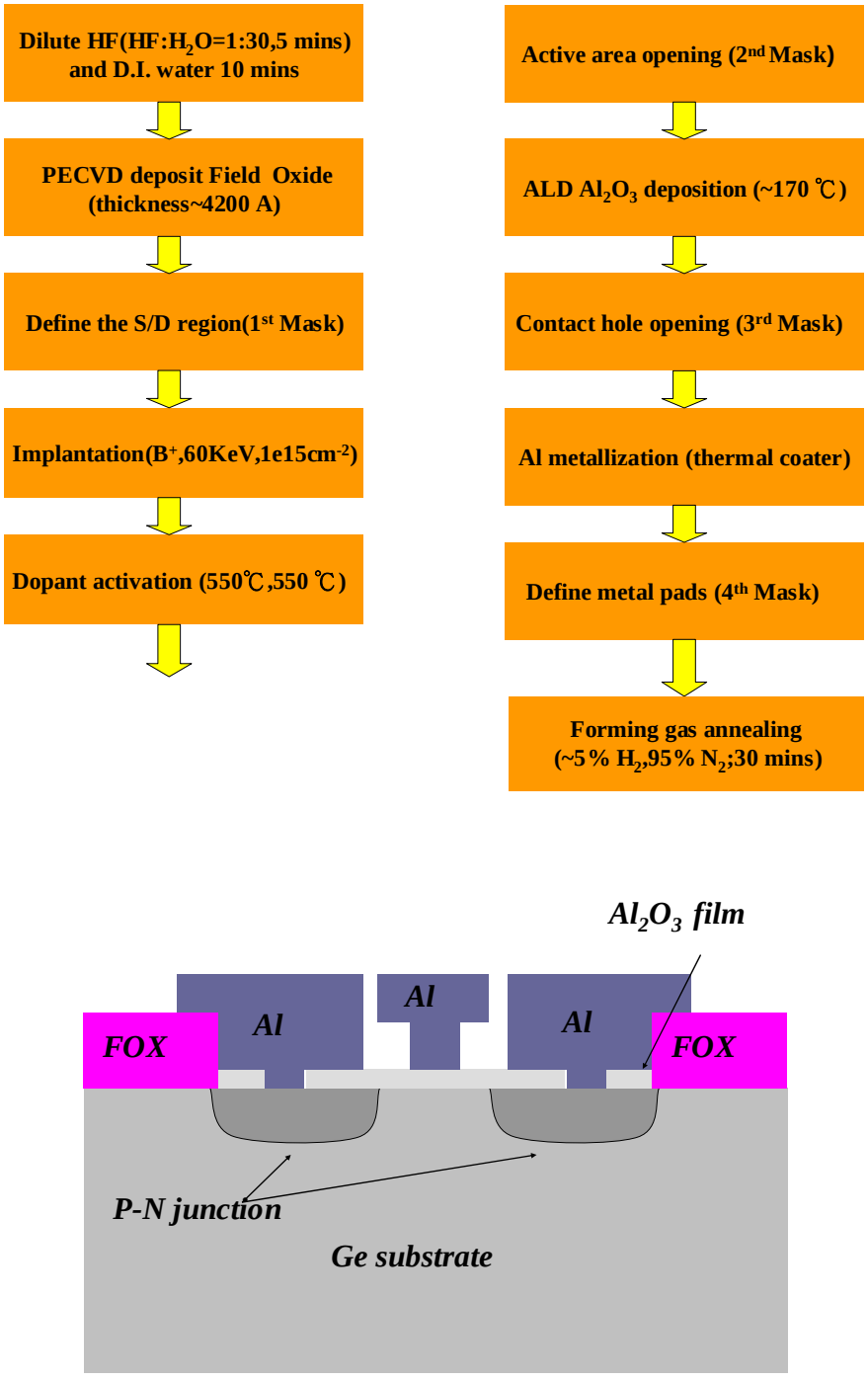
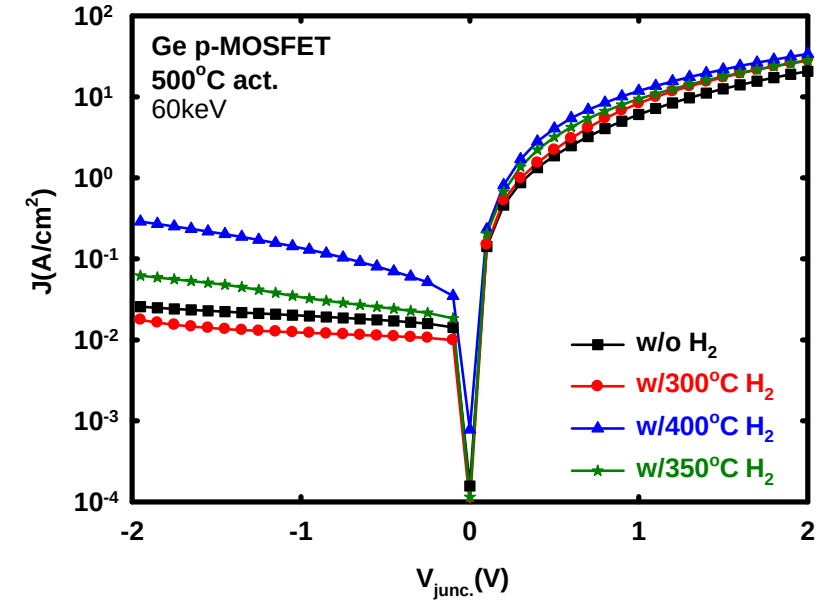
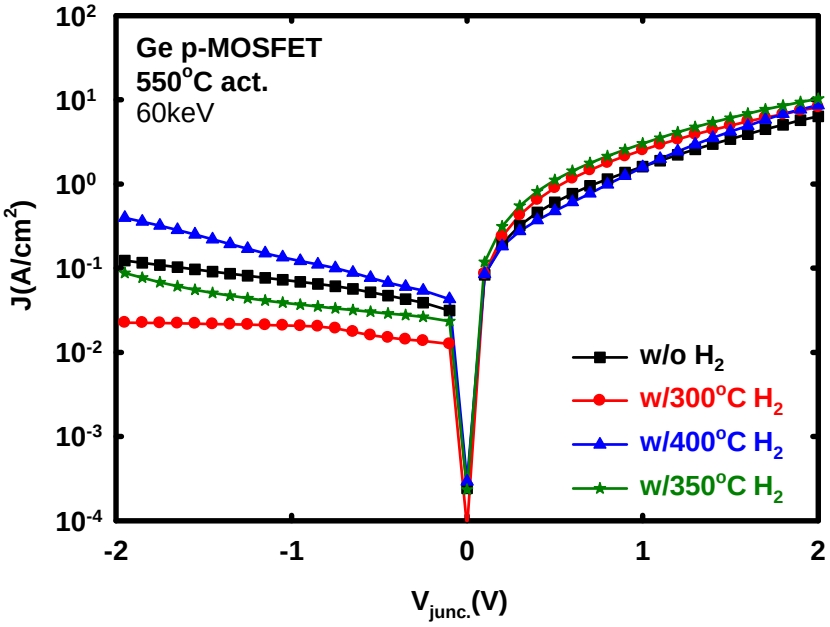


Fig. 2-1 MOSFET fabrication flow chart.



(a)



(b)

Fig. 2-2 Effect of forming gas anneal (FGA) on 100 μm^2 p$^+$ n diodes with different activations (a) 500℃ and (b) 550℃. The activations are done for 30s.

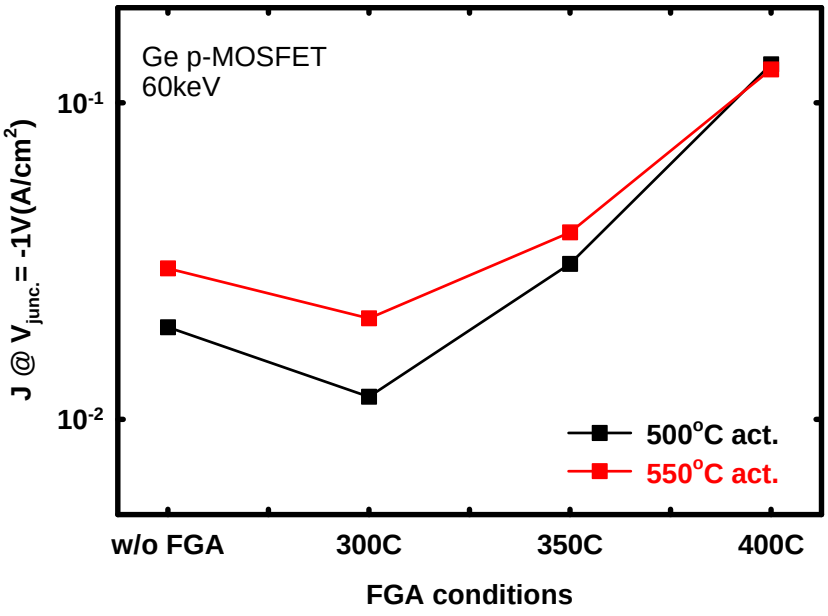


Fig. 2-3 Reverse current density at V_{junc}= -1V with different FGA conditions.

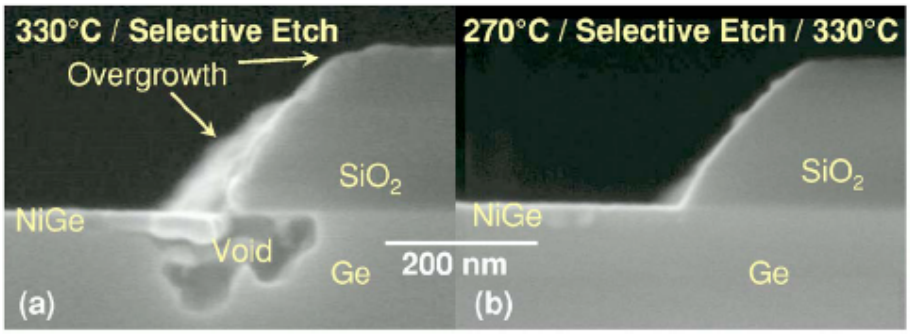


Fig. 2-4 Cross-sectional SEM images of Ni salmanide processes from IMEC. The SEM image is published on 2008 Electrochem. Solid-State Lette.

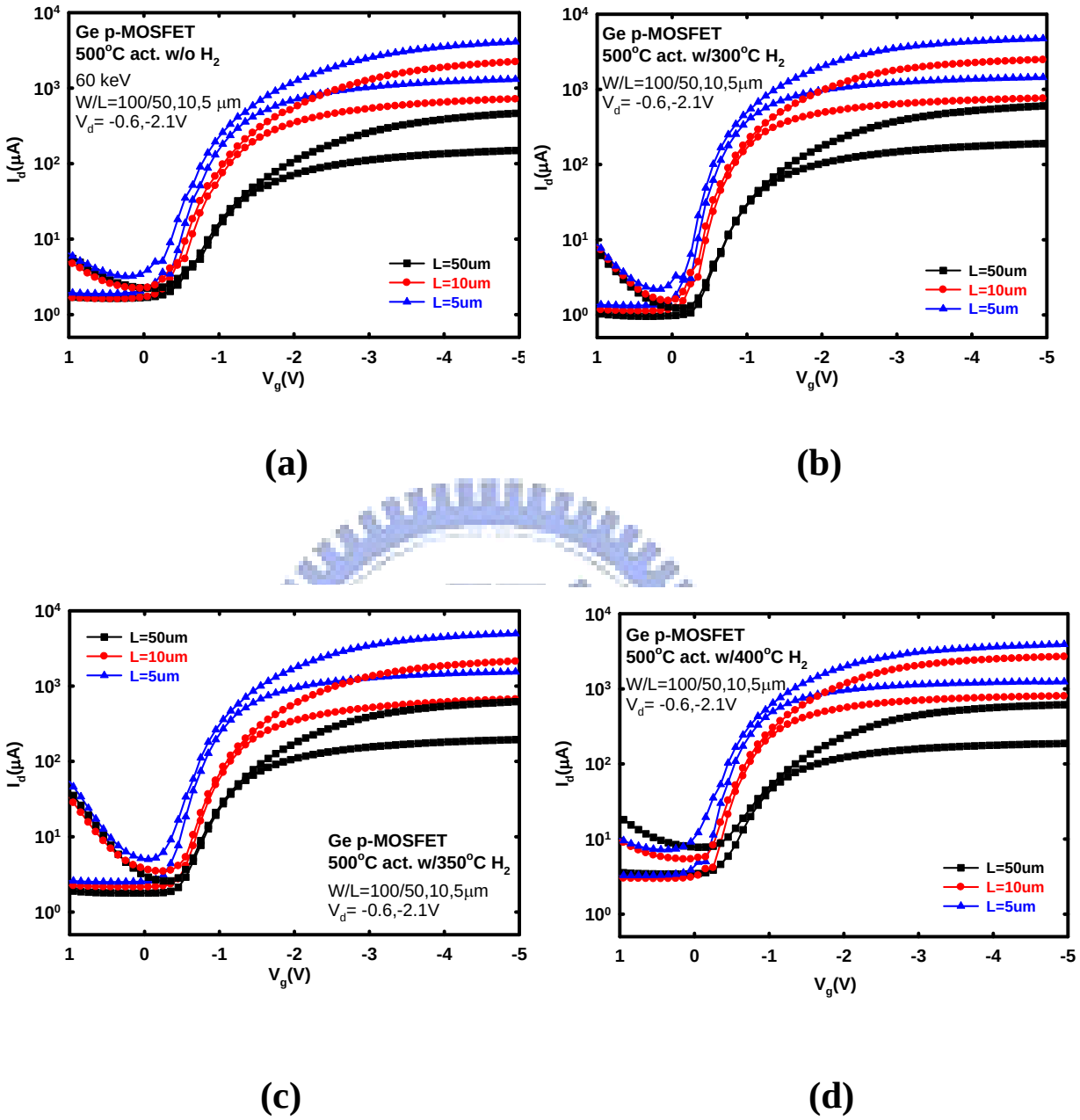


Figure 2-5 The channel length dependent I_d-V_g electrical characteristics of the 500℃ activated Ge PMOSFETs with different FGA temperatures. (a)w/o FGA, (b)w/300℃ FGA, (c) w/350℃ FGA, and (d)w/400℃ FGA.

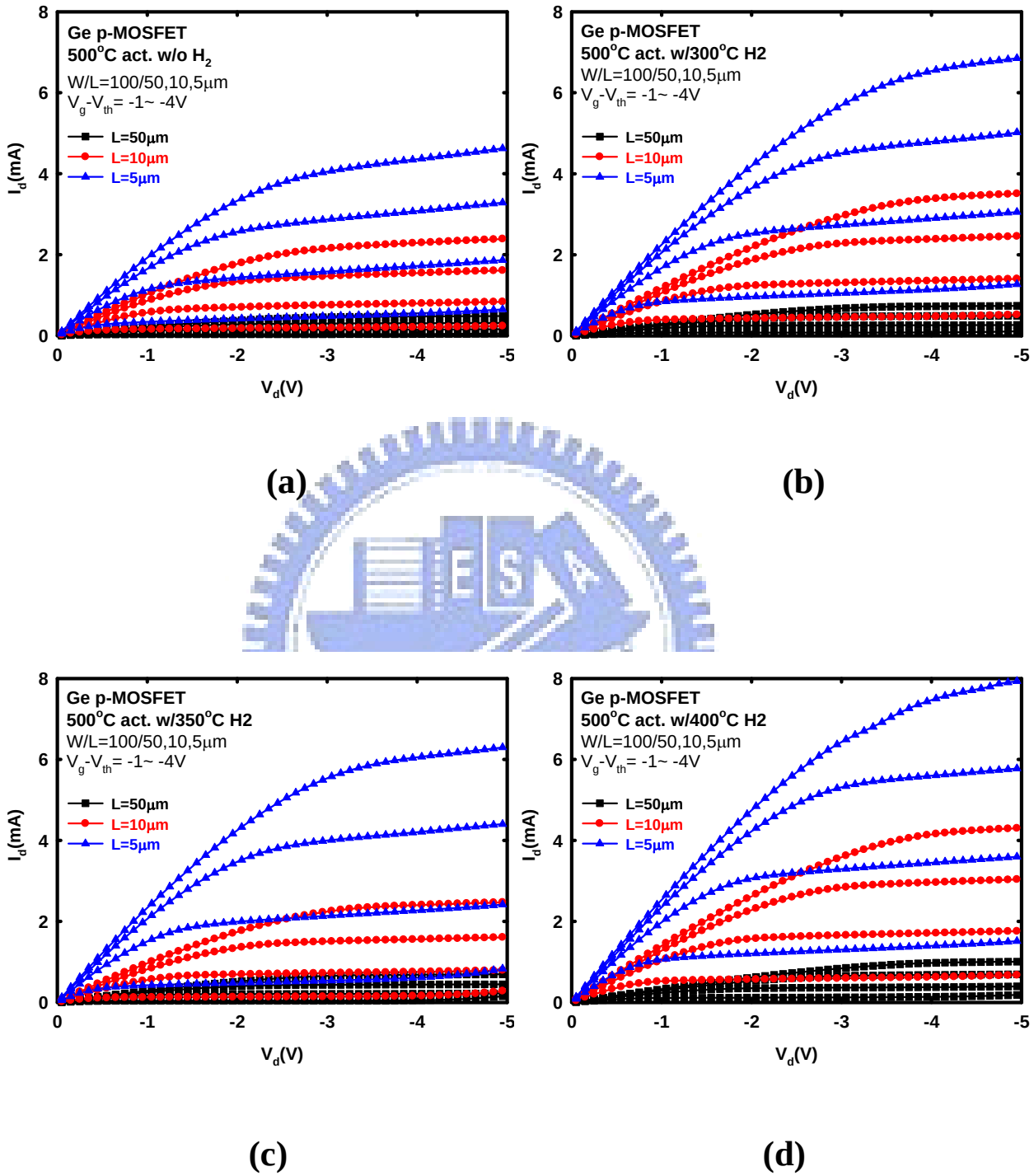


Figure 2-6 The channel length dependent I_d-V_d electrical characteristics of the 500℃ activated Ge PMOSFETs with different FGA temperatures. (a)w/o FGA, (b)w/300℃ FGA, (c) w/350℃ FGA, and (d)w/400℃ FGA.

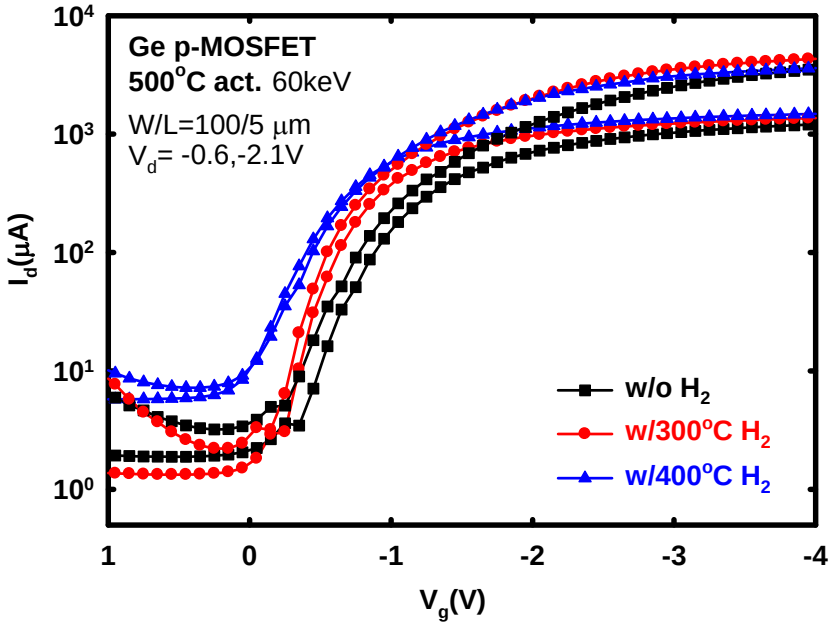


Figure 2-7 I_d-V_g characteristic of the Al_2O_3 PMOSFETs with 500℃ activation for three different FGA temperatures.

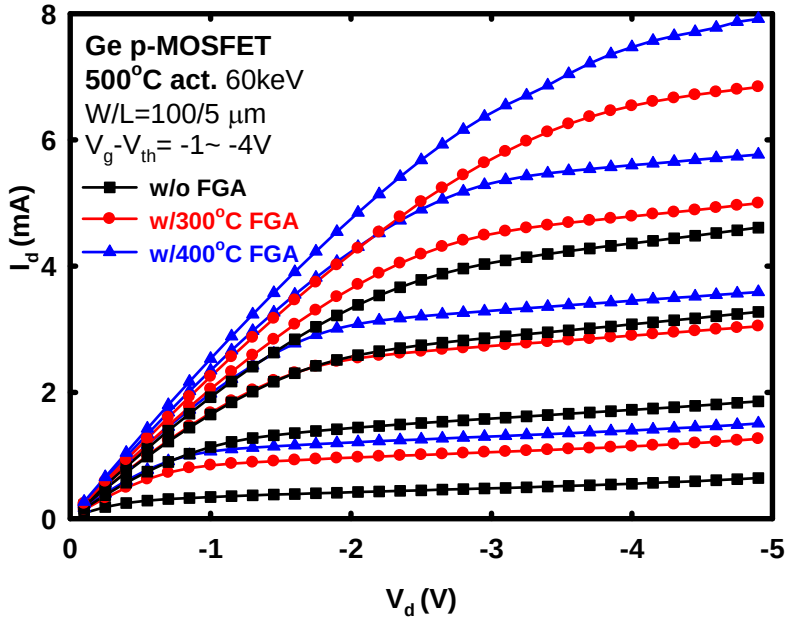
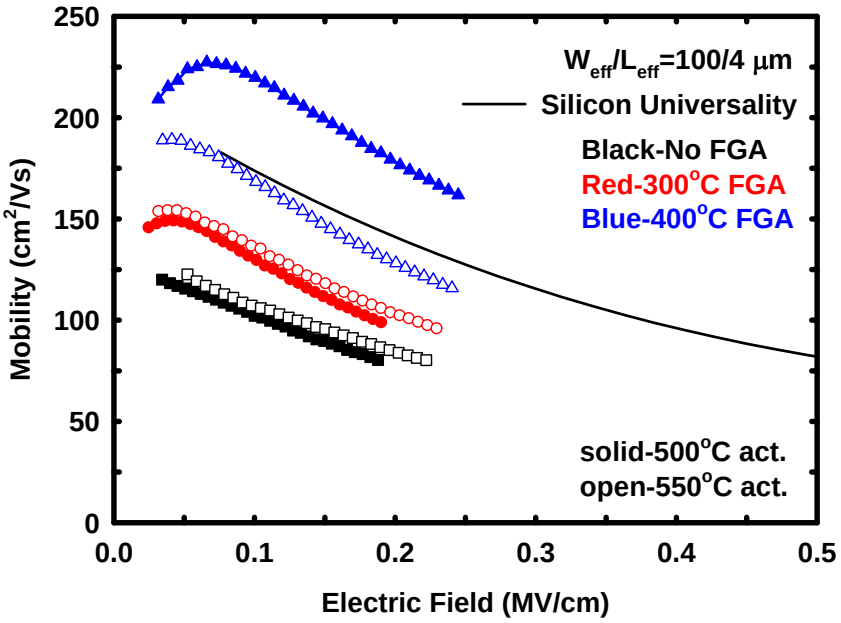
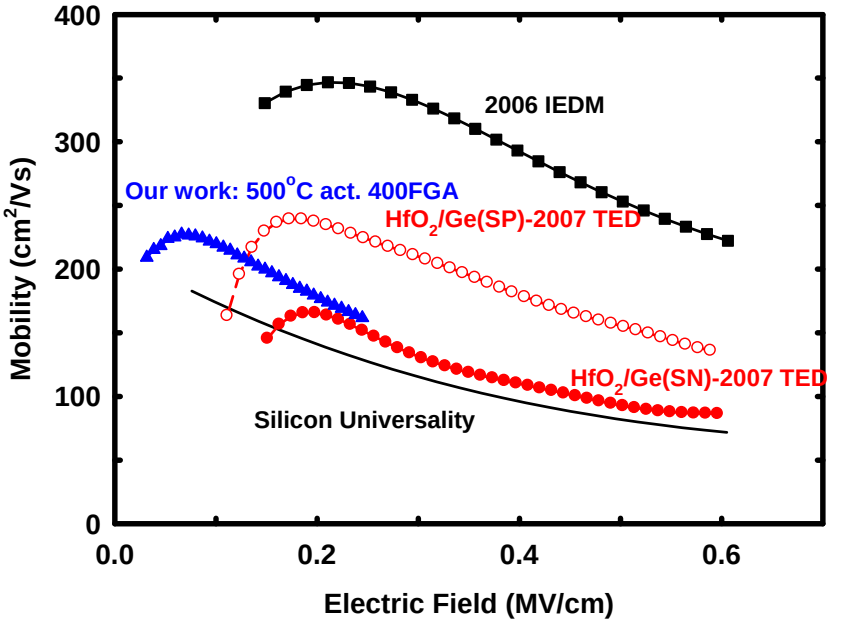


Figure 2-8 I_d-V_d characteristics of the Al_2O_3 PMOSFETs with 500℃ activation for three different FGA temperatures.



(a)



(b)

Figure 2-9 (a) The effective mobility of the Ge PMOSFETs with different FGA temperatures. (b) References with HfO_2/Ge (SP and SN) [12] and Ge/Si after PMA (H_2) [13] are compared with our data.

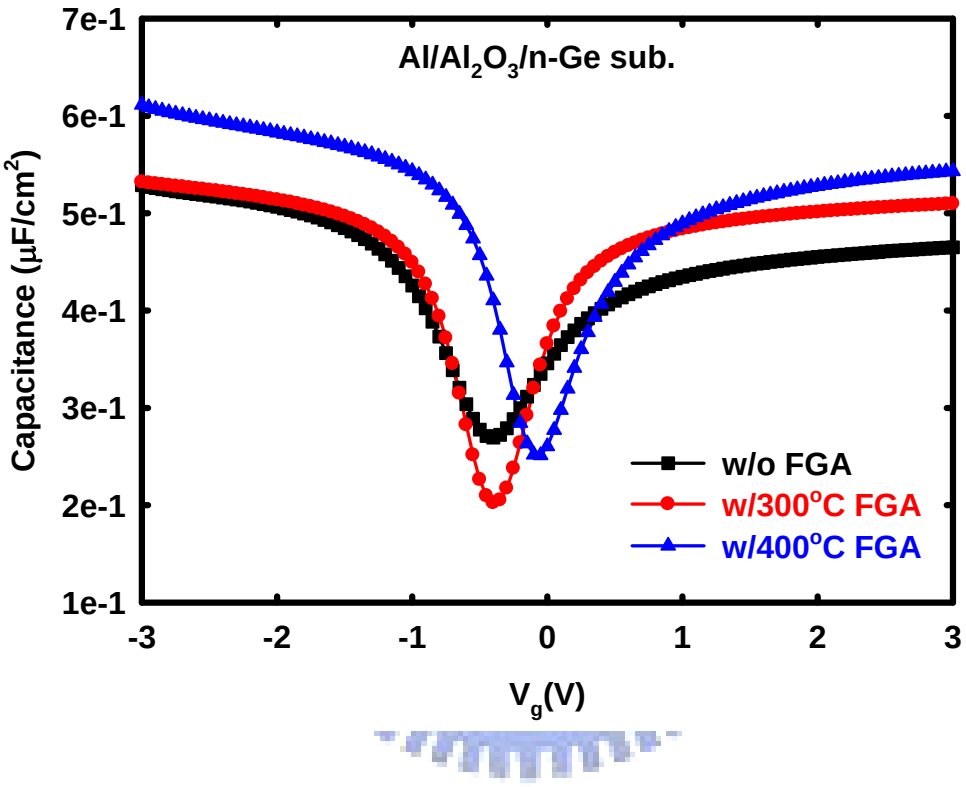


Figure 2-10 C-V characteristics of Ge PMOSFETs with different FGA at 500℃ activation.

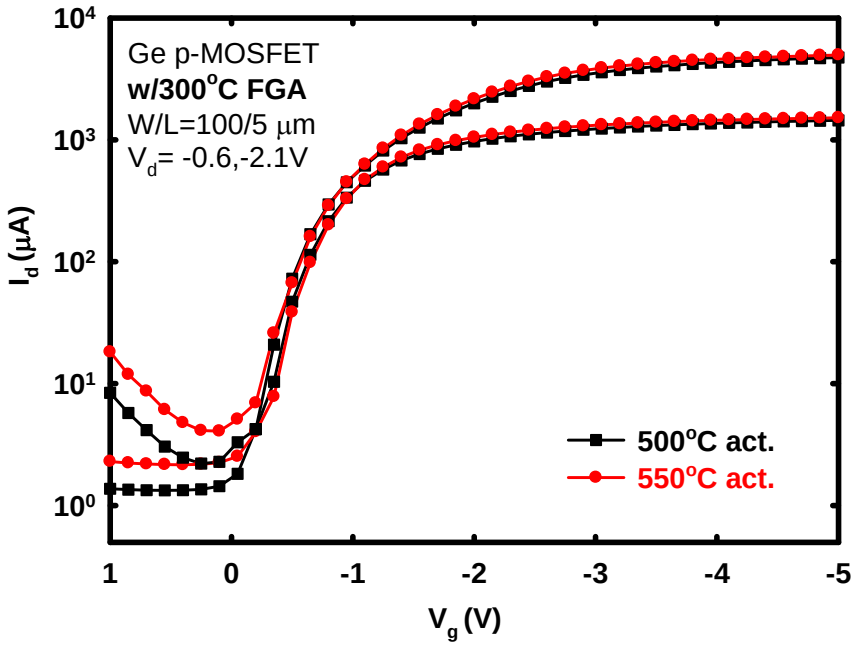


Figure 2-11 I_d-V_g characteristics of the Al_2O_3 Ge PMOSFETs with 300℃ FGA for two different activations.

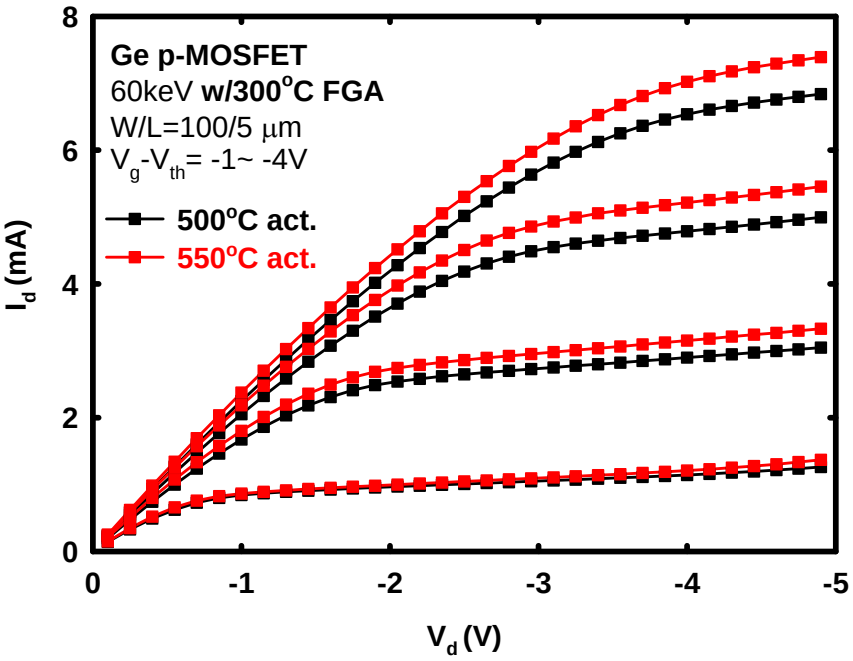


Figure 2-12 I_d-V_d characteristics of the Al_2O_3 Ge PMOSFETs with 300℃ FGA for two different activations.

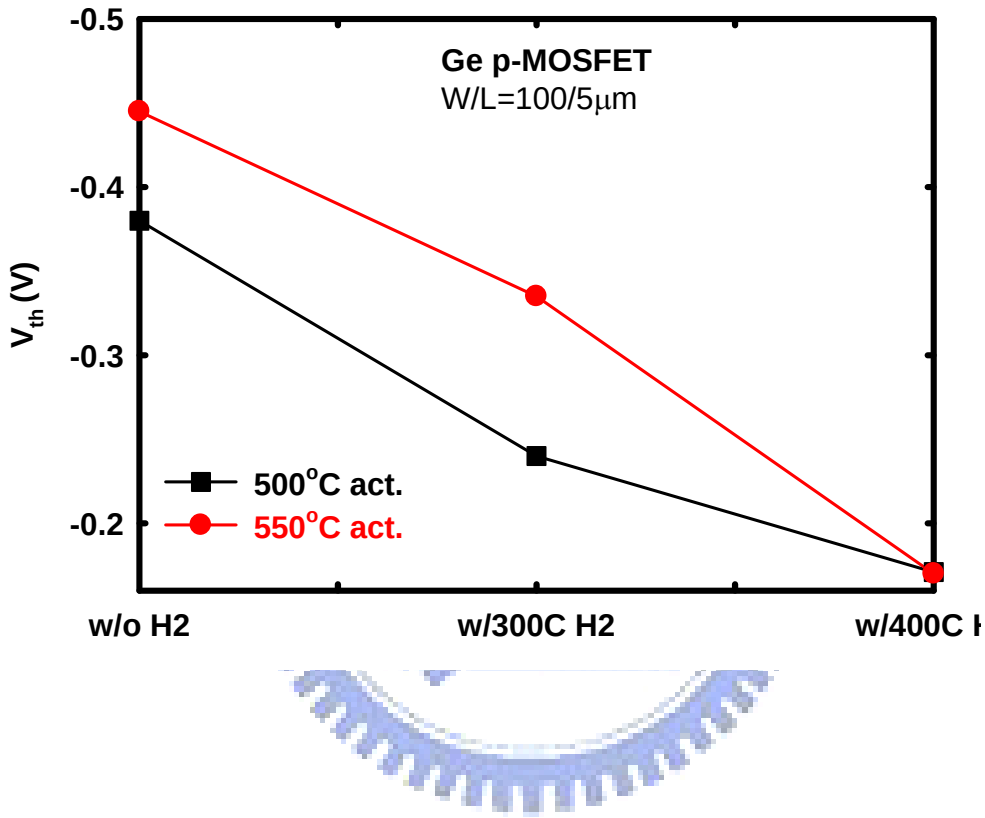


Figure 2-13 V_{th} characteristics of the Al_2O_3 Ge PMOSFETs with different FGA and activation temperatures.

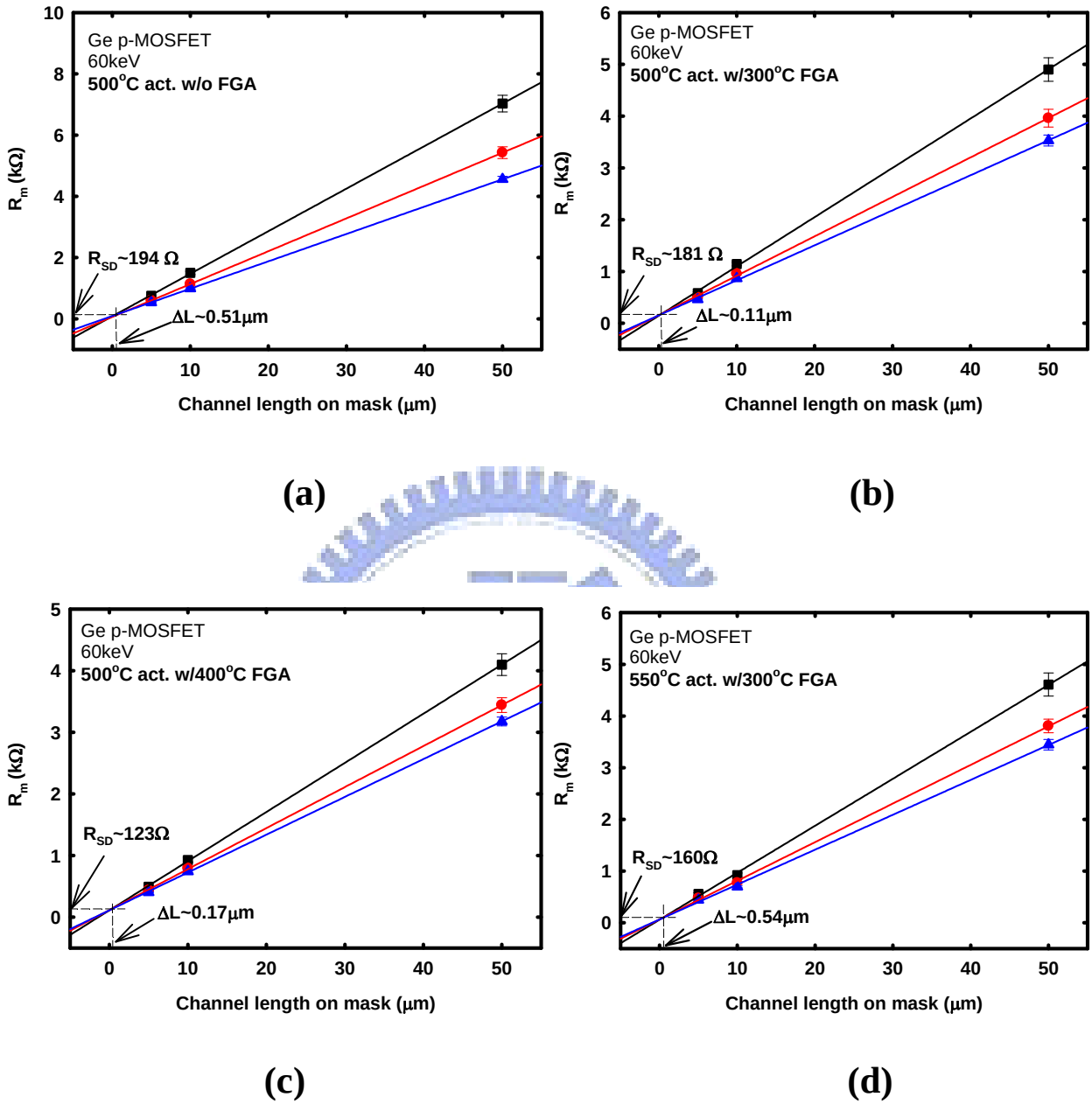


Figure 2-14 The R_m-L_g curves for extraction of R_{SD} and ΔL. (a), (b), and (c) are different FGA temperatures at 500℃ activation. (d) is 300℃ FGA with 550℃ activation.

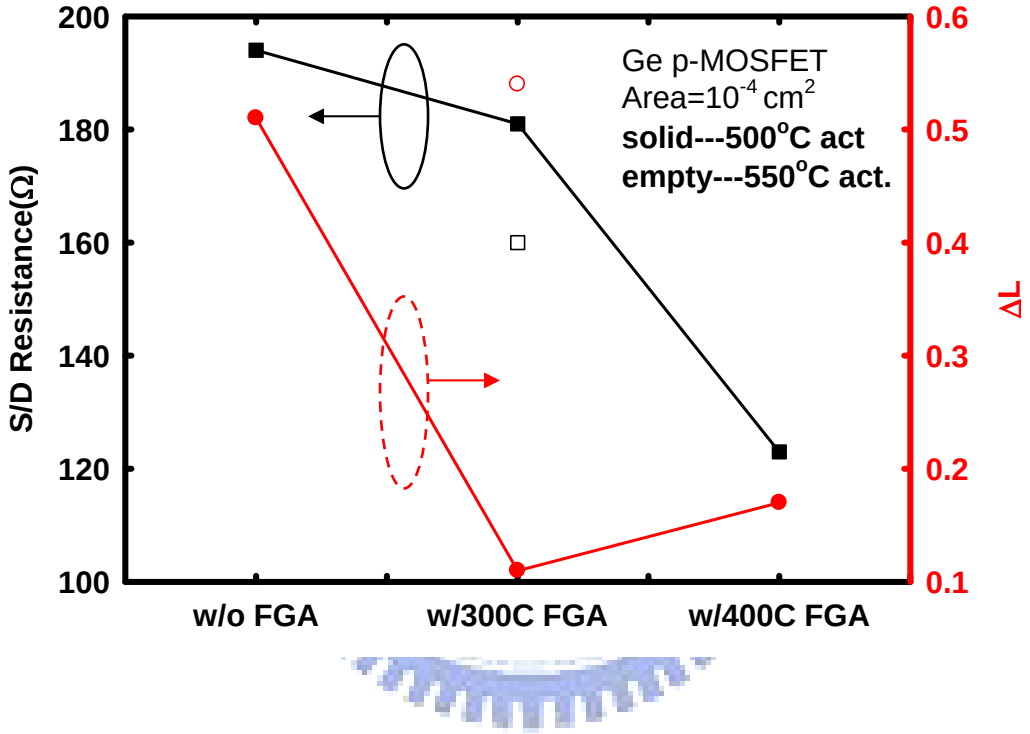


Figure 2-15 The extraction of R_{SD} and ΔL with different FGA conditions at 500 and 550℃.

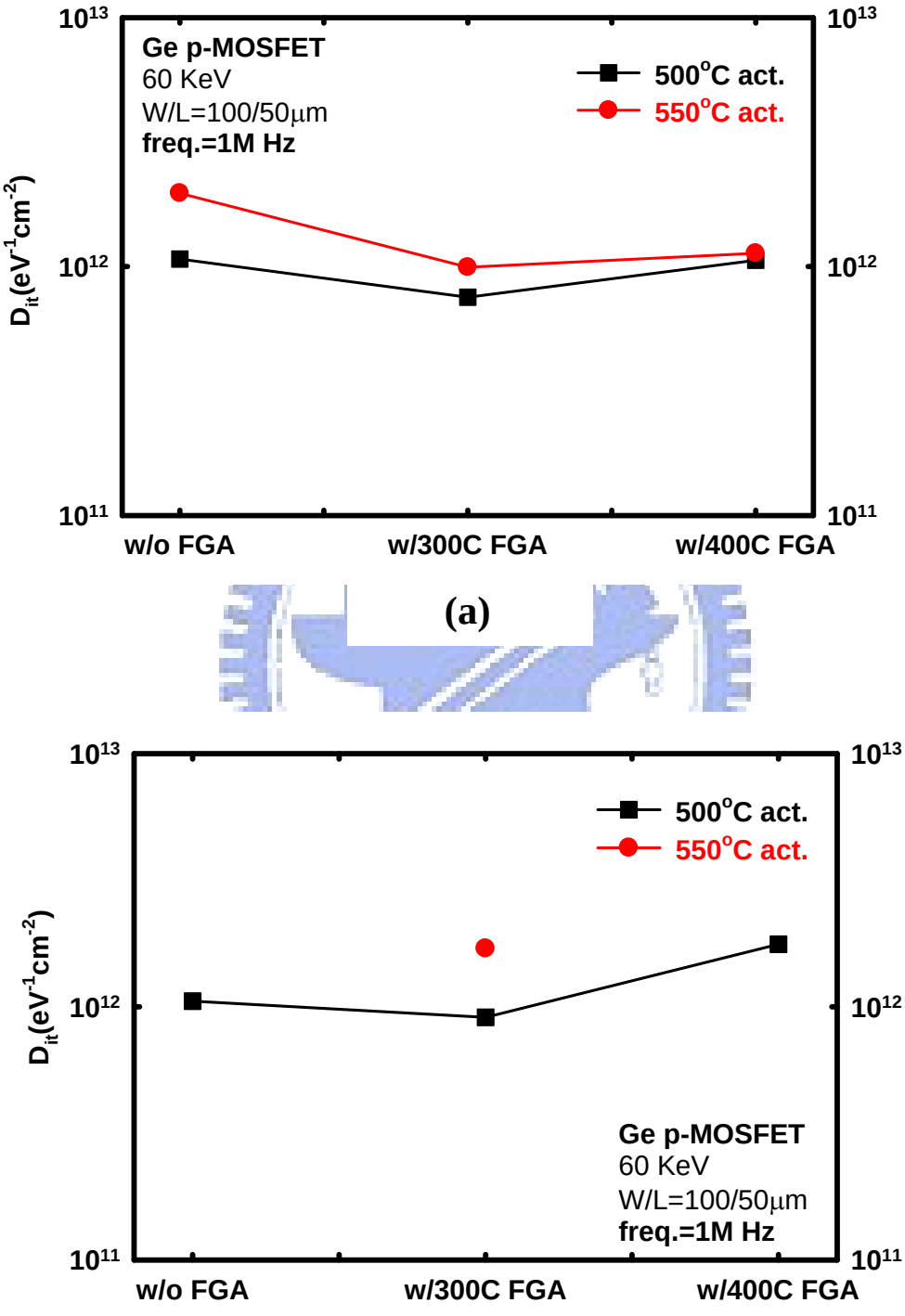


Figure 2-16 (a) D_{it} calculated from the Conductance method. (b) D_{it} calculated from the Charge pumping method.

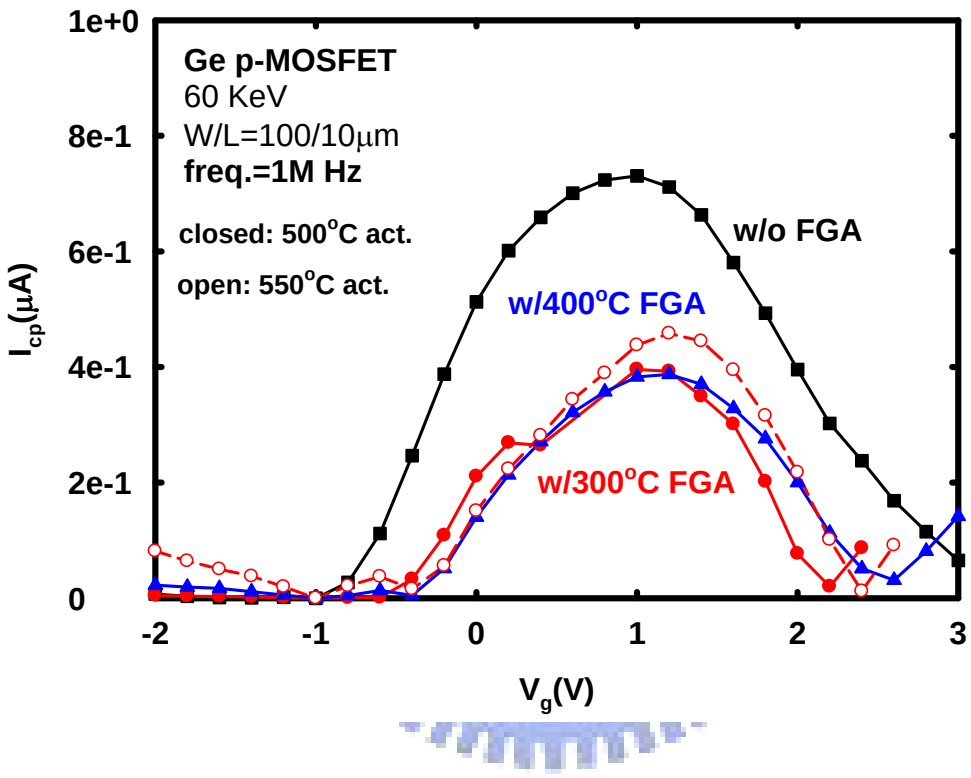
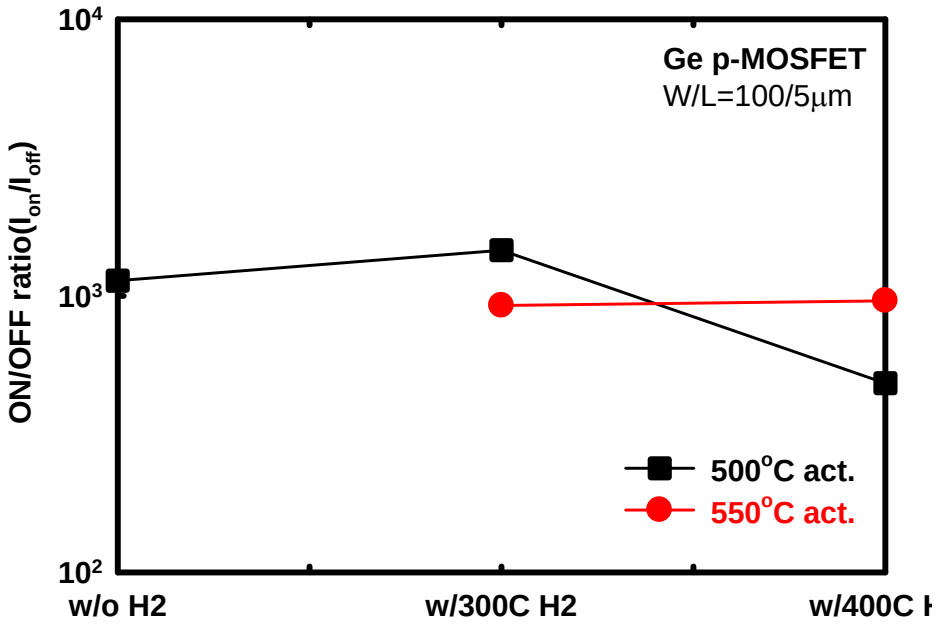
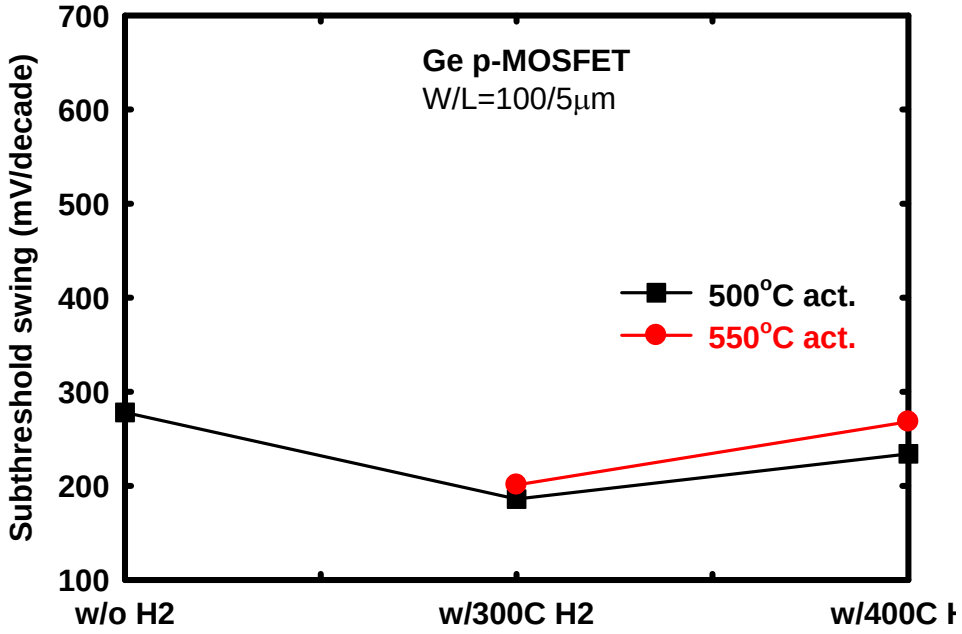


Figure 2-17 Charge pumping current v.s V_g with different FGA temperatures was evaluated at f =1MHz.

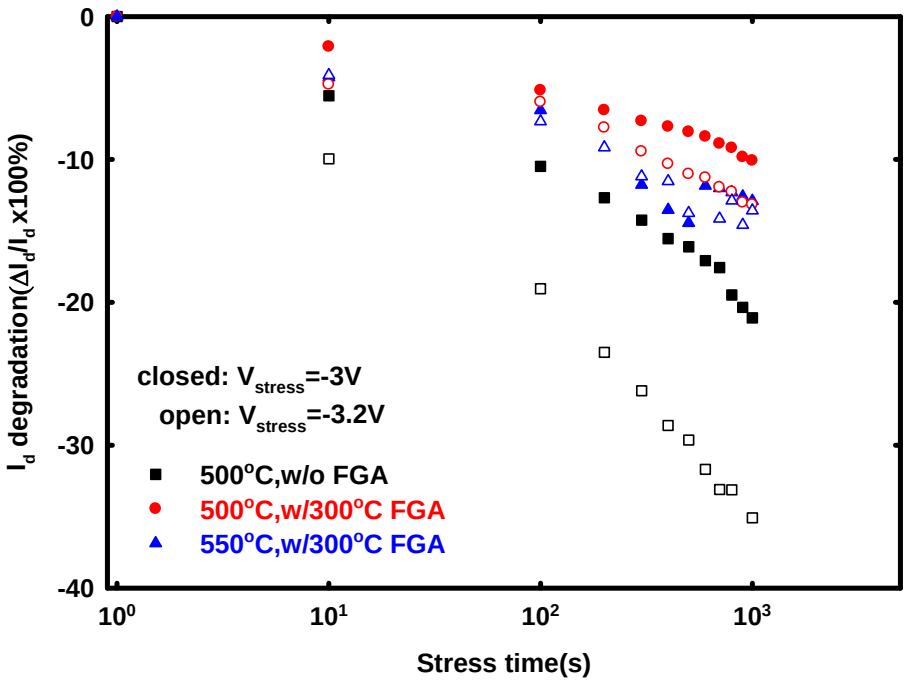


(a)

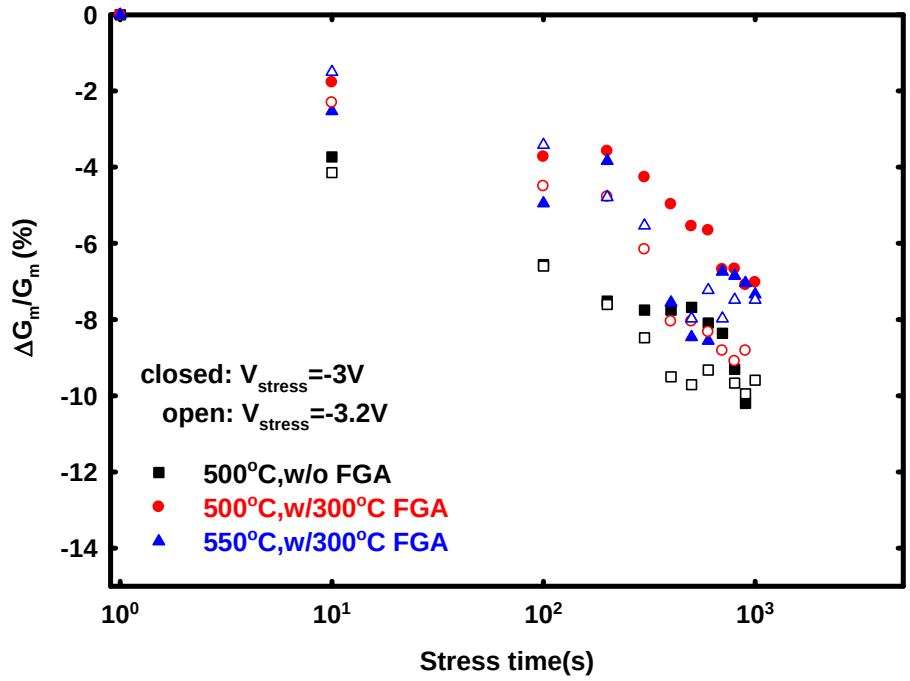


(b)

Figure 2-18 (a) The on/off ratio of Ge PMOSFETs with different FGA and activation conditions. (b) Subthreshold swing of Ge PMOSFETs different FGA and activation conditions.

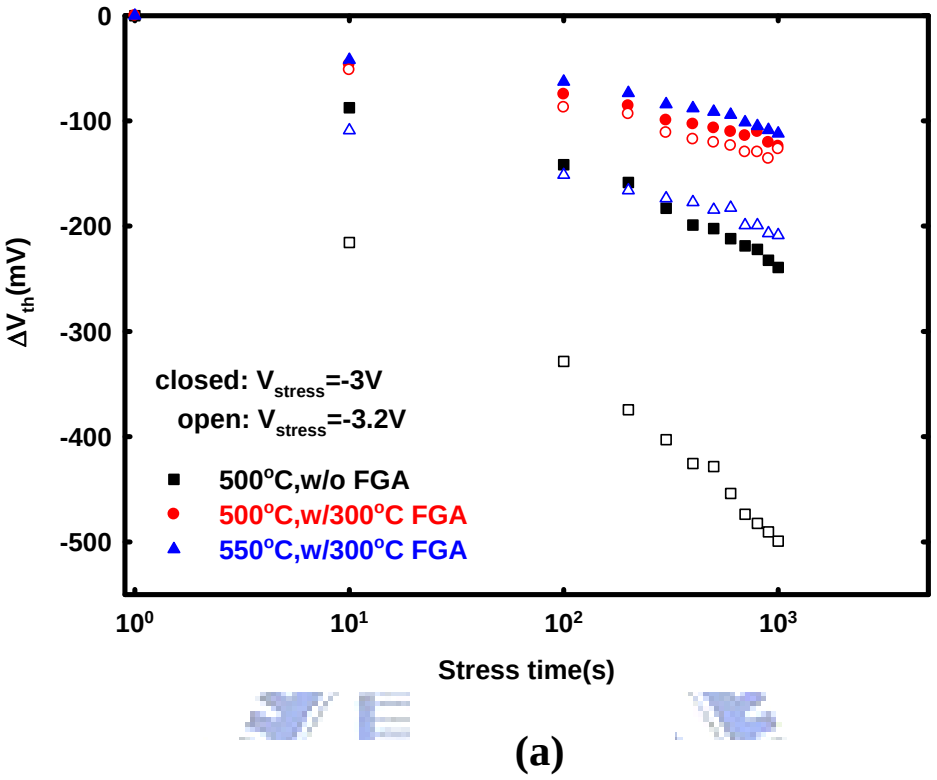


(a)

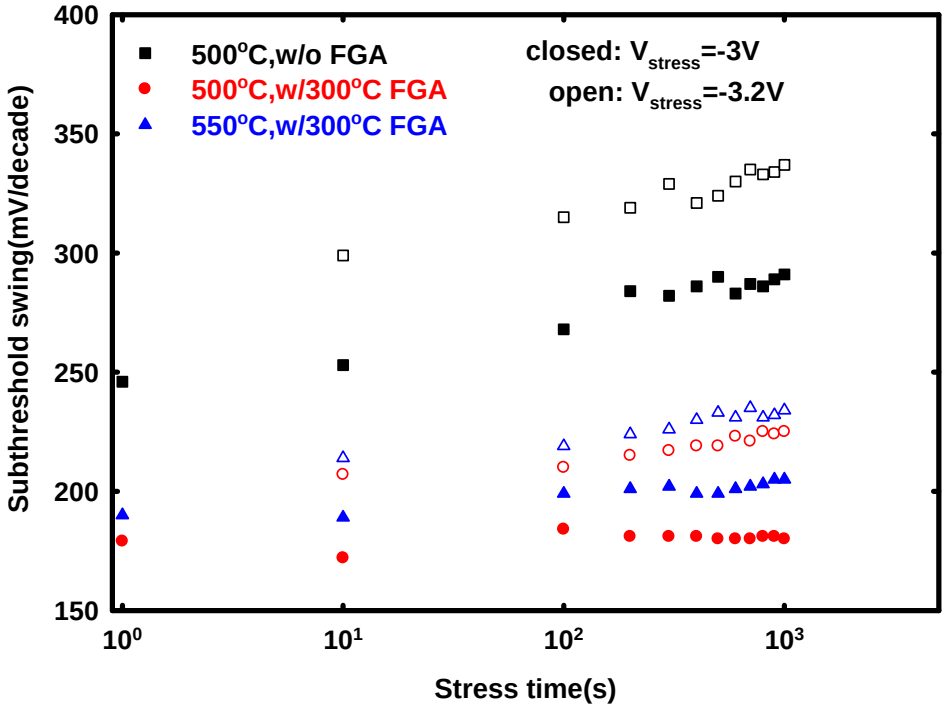


(b)

Figure 2-19 Dependence of (a) I_d degradation and (b) G_m degradation on total stress time at two kinds of inversion stress voltages for all Ge PMOSFETs.



(a)



(b)

Figure 2-20 Dependence of (a) threshold voltage shift and (b) SS on total stress time at two kinds of inversion stress voltages for all Ge PMOSFETs.

Chapter 3

Electric characteristics of p^+-n junction of $Si_{1-x}Ge_x$/Ge/Si

3-1 Introduction

We employed forming gas annealing (FGA) technique to improve the interface quality between the Ge substrate and the high-*k* gate dielectric such that the interface state density (D_{it}) is reduced slightly in Chapter2. As a result of the surface of Ge substrate is Ge bonds, Ge out-diffusion or oxygen inter-diffusion would be able to occur to form the low-k and poor electrical quality GeO_x. It is necessary to employ pretreatment prior the deposition of high-*k* dielectrics. NH_3 surface treatment [3] has been applied on high-*k*/Ge system to improve the electrical characteristics by forming GeO_xN_y interfacial later, but nitrogen incorporation may not be sufficient to fully passivate the dangling bonds on Ge surface and prevent the oxidation of the underlayer. It also induced positive fixed charges and a pretty high interface state density (D_{it}) [3]. Hence, it is reported that Si interlayer passivation on Ge is employed [17]. It is reported that a Si interlayer between a germanium substrate and a high-k gate dielectric, deposited using SiH_4 gas at 580℃, significantly improved the electrical properities of Ge devices in terms of low D_{it} , less C-V hysteresis and frequency dispersion. However, we also employed the same technique of SiH_4 pretreatment prior the deposition of Al_2O_3 gate

dielectric to passivate the Ge surface. But the result of SiH_4 pretreatment in our work is not predicted as we thought to form a thin Si interlayer. It is replaced a thin Si interlayer by a thick Si layer. Figure 3-2 shows the cross section of the capacitor by high-resolution transmission electron microscope (TEM). The Si interlayer was deposited by PECVD at 400℃.The duration of SiH_4 pretreatment was 10s. From Figure 3-2, we found that the thickness of Si layer at least is more than 10 nm. And the quality of this Si layer is not good. Hence, we employed ultra high vacuum chemical vapor deposition (UHVCVD) to deposit the thin Ge and Si layers. In Chapter 3, we investigated the pn junction properties of Si/SiGe/Ge/Si systems. In our work, we employed two kinds of thickness of top Si layer. The thicknesses of Si layers are 2.5 or 5 nm. The range of dosage in our experiment is $1\sim3x10^{15}$ cm^{-2}. And the annealing conditions are 500~700℃.

3-2 Experimental Procedures

The following substrate will be used in Chapter 3 which is different from the substrate we used in Chapter 2. At the beginning, we fabricate the pn junction to find out the better conditions of the dosages, implantation energy, annealing temperatures and annealing times. The starting wafers for the experiments are 5 inch Si (001) nominal n-type substrate with a resistivity of 2-6 Ohm cm. Above the nominal n-type substrate, 40 nm virtual SiGe substrate, 7 nm epitaxial Ge layer and 2.5 or 5 nm epitaxial Si layers are deposited by UHVCVD. First, the substrate is used with the 2.5 nm Si layer, we break it into fragments. After breaking the fresh wafer into fragments, the native oxide is removed by dipping the samples in a diluted HF solution (HF:H_2O=1:100) for 90 seconds, followed by rinsing with de-ionized water (D.I water) 5 minutes and drying with N_2. After that, we use a plasma enhanced chemical vapor deposition (PECVD) system to deposit the field oxide SiO_2 (thickness~4200 Å). Then, we define the implant region by Mask 2 as mentioned in Chapter 2 and etch SiO_2 by Buffer Oxide Etching (BOE). To form a P^+-N junction with a boron doping in the P^+ region by restricting the flow of drain current just under the surface, the samples are implanted by B^+ with tilt: 7^o and twist: 22^o. The implant energy are10, 20, and 40 keV while the implant dose is $1x10^{15}$ atoms/cm^2. Before activating the implant region, we deposit the thin oxide SiO_2 by PECVD to prevent the dopant from losing. Annealing of the samples are performed in a N_2

ambient in the JETFIRST RTP system at 500°C , 600°C and 700°C annealing temperatures. The annealing times are 30 and 120 seconds in 500°C , while it is 30 seconds in 600°C and 700°C. After annealing, we use the Mask 2 to etch the thin oxide SiO_2 and define the metal pads. Subsequently, we coat aluminum (Al) on the backsides of these samples. Finally, all samples are treated in forming gas annealing (FGA) (N_2/H_2, 95:5 %) at 300 °C for 30 minutes. The overall fabrication processes of the epitaxial Ge p^+- n junctions were illustrated in Figure 3-1. After the fabrication of pn junctions, we measure the current-voltage (I-V) characteristics by Keithley 4200 semiconductor characterization. In order to find out the effects in electrical characterization with different dosages and annealing times, we fabricate the pn junction again using the wafer with the 5 nm Si layer. After finishing the pn junction, we find out the better conditions of p^+-n.

3-3 Results and Discussions

Table 2-1 shows the conditions of implantation and annealing for 2.5nm Si capping layer. Note that we didn't have the device about 600^{o}C 40keV. And Table 2-2 shows the conditions of implantation and annealing for 5 nm Si capping layer. Note that we used two different dosages in case of 5nm Si capping layer. Then, we show an equation [20] about the leakage current and a simple diagram about the path of the leakage current in Figure 3-3. We could divide the leakage current into two items. One is area leakage current, the other is perimeter leakage current. First, we discussed 2.5nm Si capping layer at different annealing conditions and we only chose 10keV to discuss. Figure 3-4(a) shows pn diode is implanted by Boron with 10keV energy and 1x10^{15}cm^{-2} dose and annealing at 500^{o}C 30s. Reverse leakage current is divided by different area. We find that the reverse leakage current at different area are not closed. Figure 3-4(b) shows the same conditions of annealing and implantation except the pn junction is divided by different perimeter. We find that the junction current is divided by different perimeter are closed in comparison with area. Consequently, we think the peripheral junction current dominates the junction leakage. Figure 3-5(a) shows p^{+} n diode was implanted by Boron with 10keV energy and 1x10^{15}cm^{-2} dose and annealing at 500^{o}C 2 minutes. Reverse leakage current was divided by different area. The result of junction leakage was like Figure 3-4(a). And Fig. 3-5(b) shows p^{+} n diode was implanted by Boron with 10keV

energy and $1x10^{15}cm^{-2}$ dose and annealing at $500^{o}C$ 2 minutes. Reverse leakage current was divided by different perimeter. We found that the junction current was divided by perimeter is closed compared with area. It meant that the junction leakage is dominated by peripheral leakage current. We also found the same result in Figure 3-6(a) and Figure 3-6(b). Finally, we showed the p^{+} n junction is annealing at $700^{o}C$ activation in Figure 3-7(a) and (b). The result of junction leakage, which one is dominated, peripheral junction leakage dominated the junction leakage. Then, we took all conditions into comparison in Figure 3-8. We found some interesting things. First, the peripheral leakage wasn't affect by implantation energy. Second, the peripheral leakage current was mainly affected by annealing temperature. The leakage current was reduced almost 10 times after $700^{o}C$ annealing compared with $500^{o}C$ activation. Hence, we though that the domination of peripheral leakage current is the defects. Because, $500^{o}C$~$700^{o}C$ annealing temperatures on Si couldn't repair the defects by implantation. The main source of junction leakage came from these un-repair defects. Figure 3-9 shows the leakage current at different thermal budget. The main effect of leakage current is still annealing temperature. Then, we discussed the electrical properties of the p+ n diode with 5nm Si capping layer. Since, we had two different dosages $1x10^{15}$, $3x10^{15}$ cm-2. But, we found that the exhibit of $1x10^{15}$ cm^{-2} with 2.5nm Si capping layer is same as 5nm Si capping layer. Here, we only discussed the result of $3x10^{15}$ cm^{-2} with 5nm Si capping layer. Figures 3-10(a) and (b) show p^{+} n diode were implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$

dose and annealing at 500°C 5 minutes. Reverse leakage current was divided by different area and perimeter, respectively. We found that the similar result with 5nm Si capping layer. The reverse leakage current was dominated by peripheral current. Because, the reverse leakage currents were divided by different perimeters, where are more closely than different areas. Figures 3-11(a) and (b) show p^+ n diode were implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 500°C 10 minutes. Reverse leakage current was divided by different area and perimeter, respectively. We also found the same condition in comparison with 500°C 5 minutes case. Figures 3-12(a) and (b) show p^+ n diode were implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 600°C 2 minutes. Reverse leakage current was divided by different area and perimeter, respectively. Again, we found the similar result at annealing 600°C 2 minutes. Consequently, we thought the defects from implantation would not be able to repair in continuous annealing led to high reverse leakage current. Figures 3-13(a), (b) show the effect of thermal budget on peripheral leakage current (J_p) at V_R=-1V. The measurement of junction leakage is 2.5 and 5nm Si capping layer, respectively. We found that the peripheral leakage current was similar to each other in the range of 10^{-3}~10^{-2} (A/cm). But, the time of annealing with 5nm Si capping layer is longer than 2.5nm Si capping layer. Hence, we thought the thinner Si capping layer is better for Si/Ge/$Si_{1-x}Ge_x$ substrate material.

3-4 Summary

We had shown the electrical properties with different Si capping layer thickness and thermal budget. From the electrical analysis, we found that peripheral leakage current dominated the reverse leakage current with 2.5 and 5nm Si capping layers. And we thought the defects in Si capping layer attributed to peripheral current. Since, 500^{o}C~700^{o}C could not repair defects from implantation. However, higher annealing temperatures ware not good for Ge channel. Hence, we could deposit the thinner Si (<1 nm) capping layer top of Ge channel. Because, the thinner Si layer can be consume in continuous processes and Si capping layer can be the passivation layer to passivate Ge surface to gain the better interface quality.

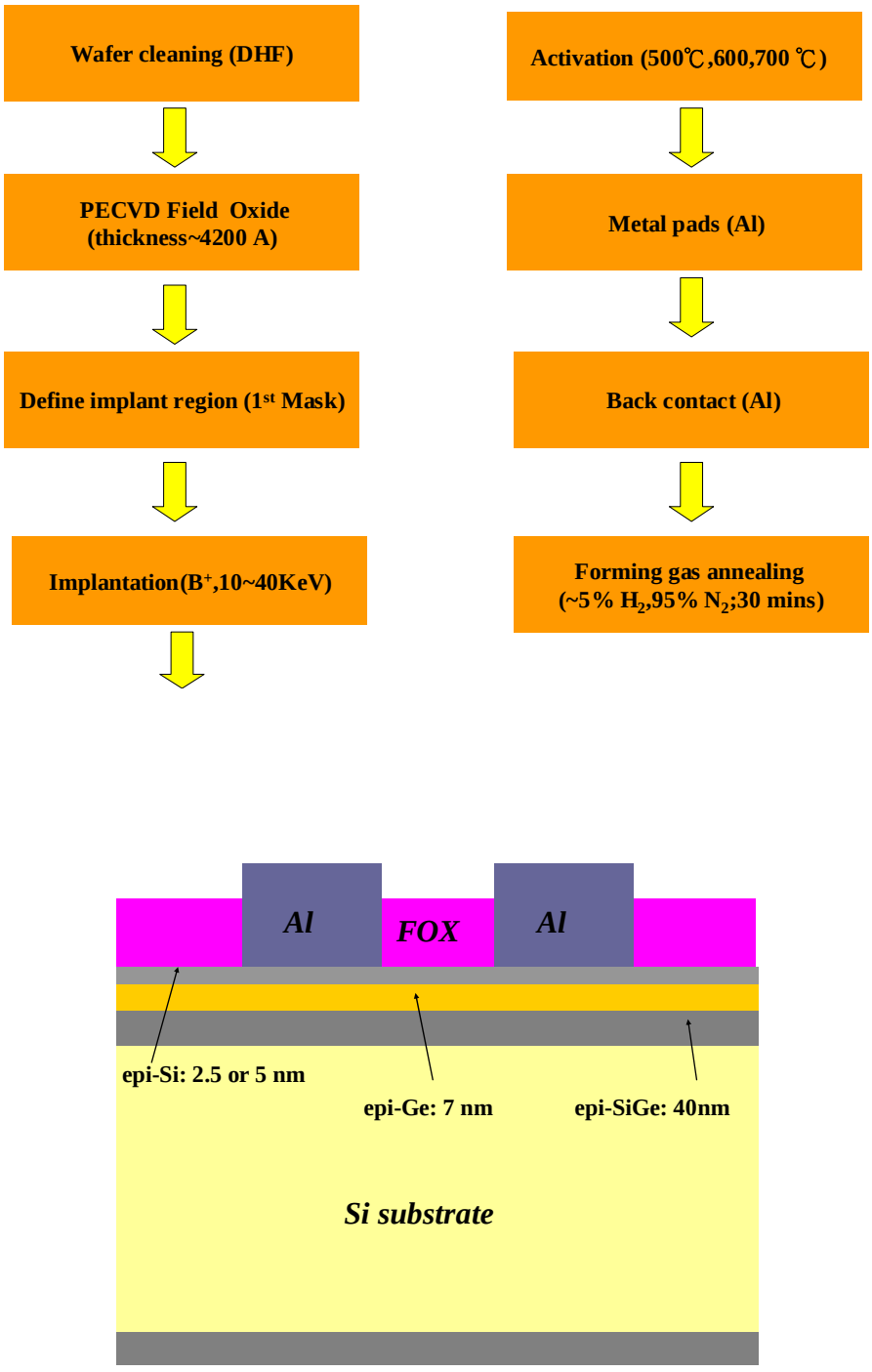


Fig. 3-1 P^+-N junc. fabrication flow chart

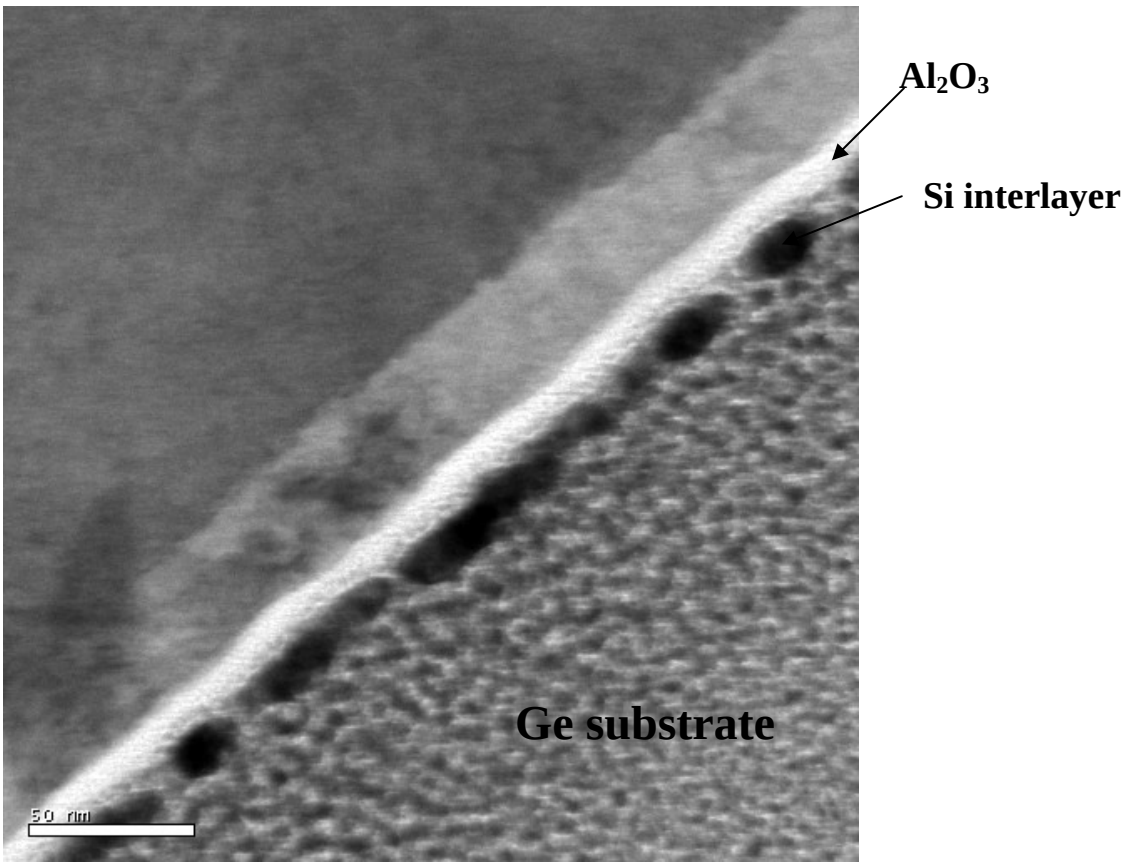


Fig. 3-2 TEM image of the capacitor cross section with SiH_4 pretreatment. The bright layer is Al_2O_3. And under the Al_2O_3 is Si interlayer.

SiGe/Ge/Si(40/7/2.5)nm Dose:1E15 cm-2	500°C 30s	500°C 120s	600°C 30s	700°C 30s
10 keV	A	D	G	L
20 keV	B	E	H	J
40 keV	C	F		K

Table 3-1 Conditions of implantation and annealing for 2.5 nm Si capping layer.

SiGe/Ge/Si(40/7/5)nm	500°C 5 mins	500°C 10 mins	600°C 2 mins
1E15cm-2 20keV	A	B	C
1E15cm-2 40keV	D	E	F
3E15cm-2 20keV	G	H	I
3E15cm-2 40keV	J	K	L

Table 3-2 Conditions of implantation and annealing for 5 nm Si capping layer.

$$I_R = J_A \times \text{Area} + J_P \times \text{Perimeter}$$
$$(a^2) \qquad (4a)$$

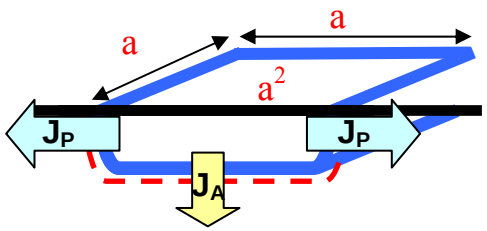


Fig. 3-3 The leakage current equation and a simple diagram about the path of leakage current.

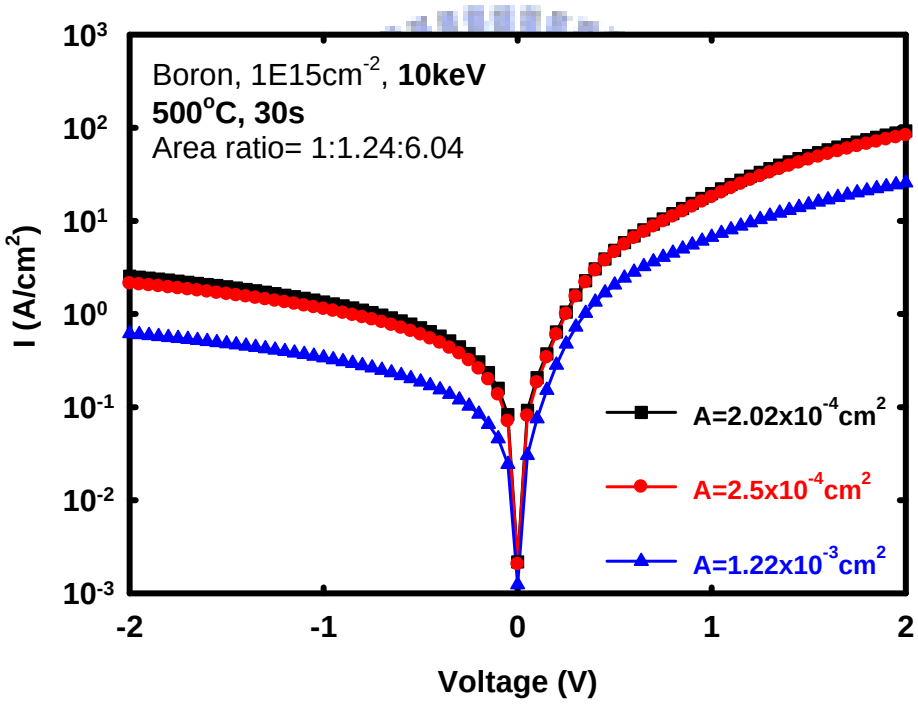


Fig. 3-4(a) This pn diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 500°C 30s. Reverse leakage current was divided by different area.

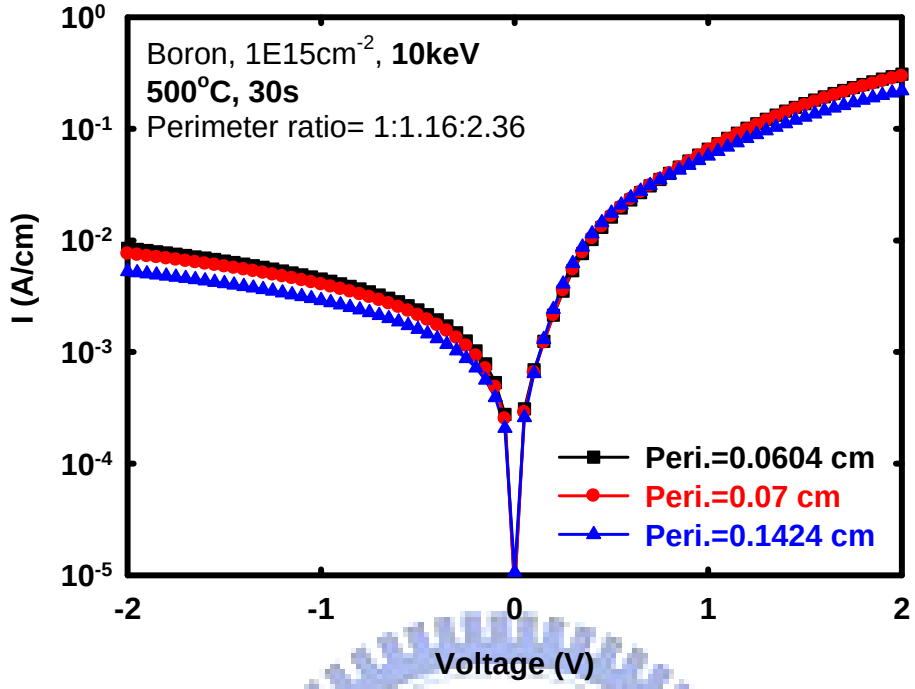


Fig. 3-4(b) This pn diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 500°C 30s. Reverse leakage current was divided by different perimeter.

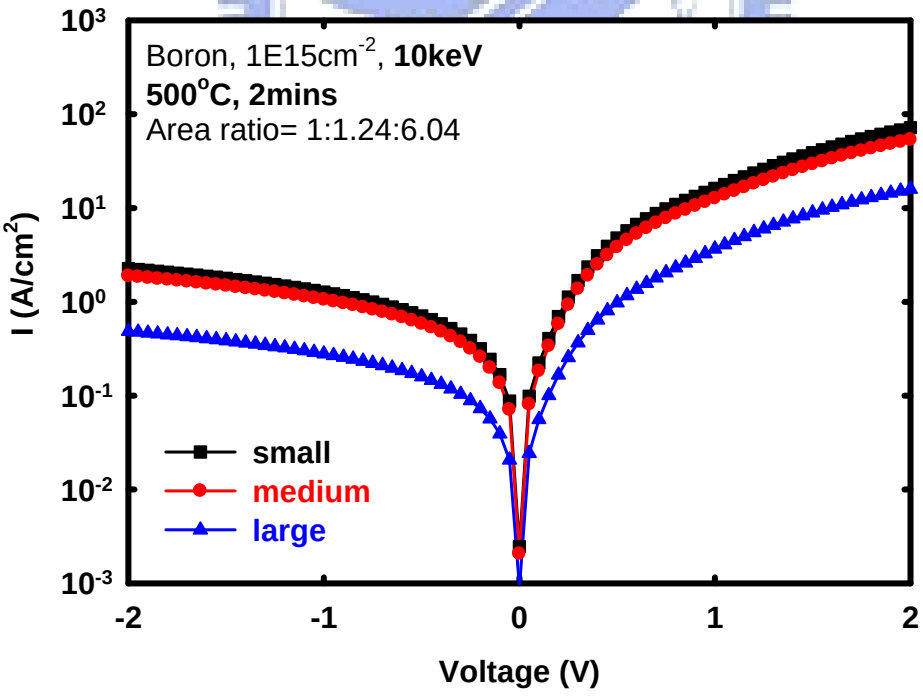


Fig. 3-5(a) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 500°C 2 minutes. Reverse leakage current was divided by different area.

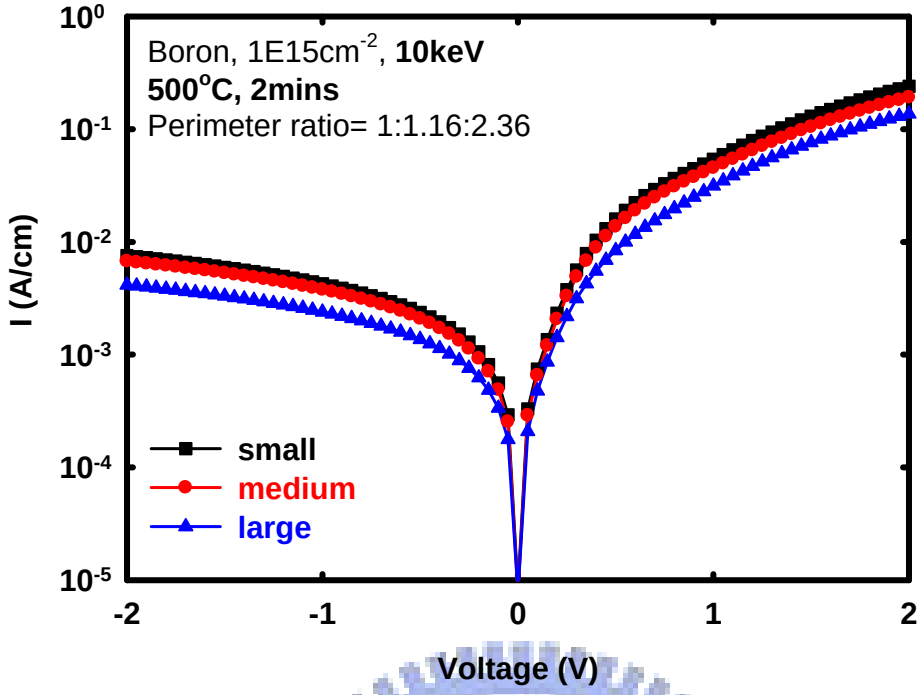


Fig. 3-5(b) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 500°C 2 minutes. Reverse leakage current was divided by different perimeter.

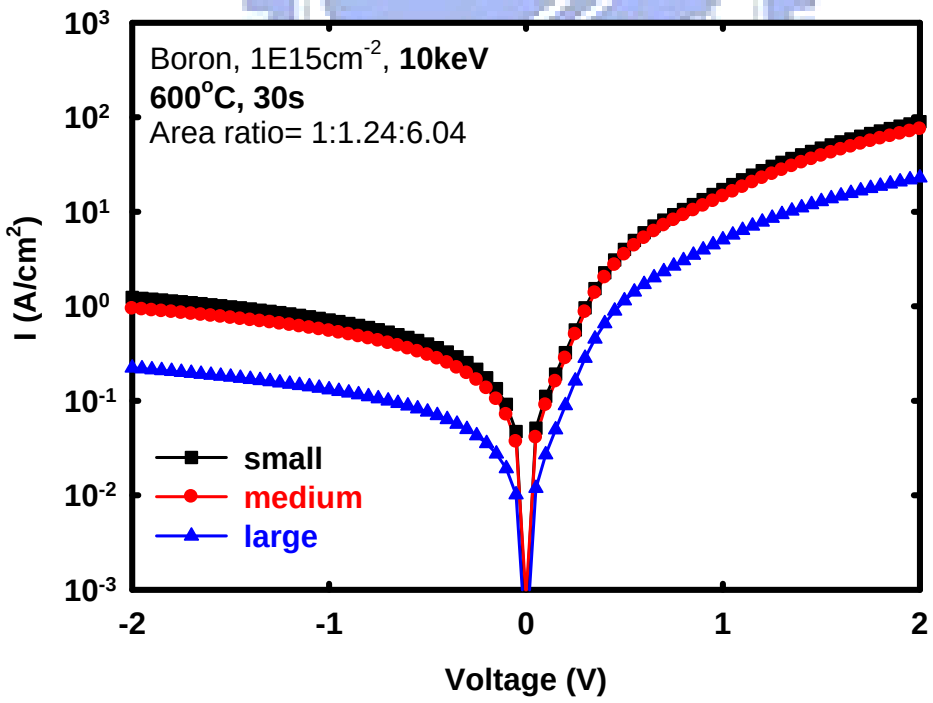


Fig. 3-6(a) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 600°C 30s. Reverse leakage current was divided by different area.

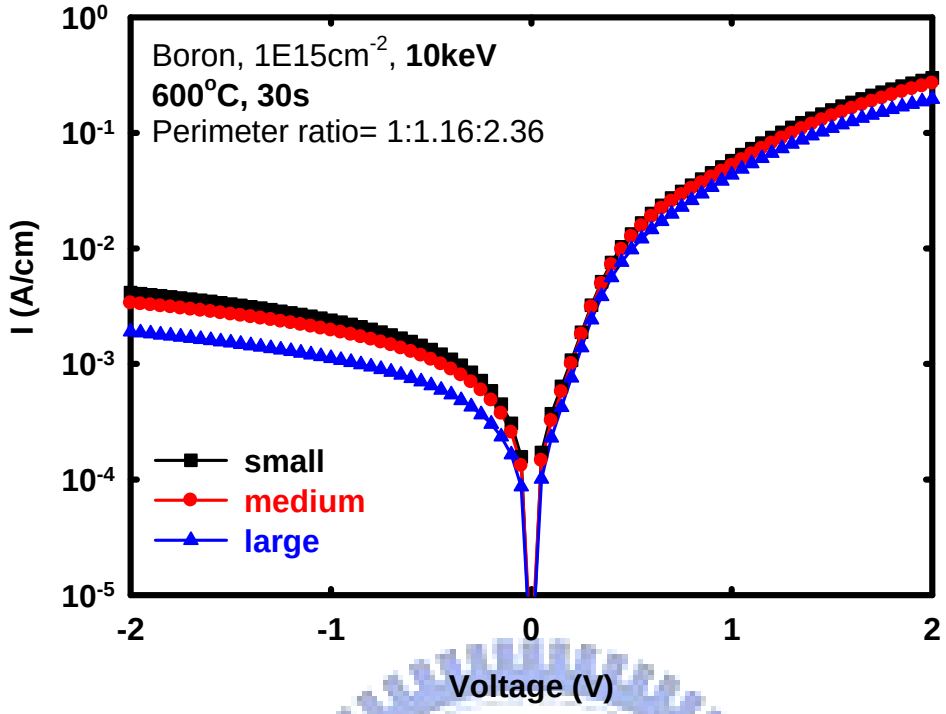


Fig. 3-6(b) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 600°C 2 minutes. Reverse leakage current was divided by different perimeter.

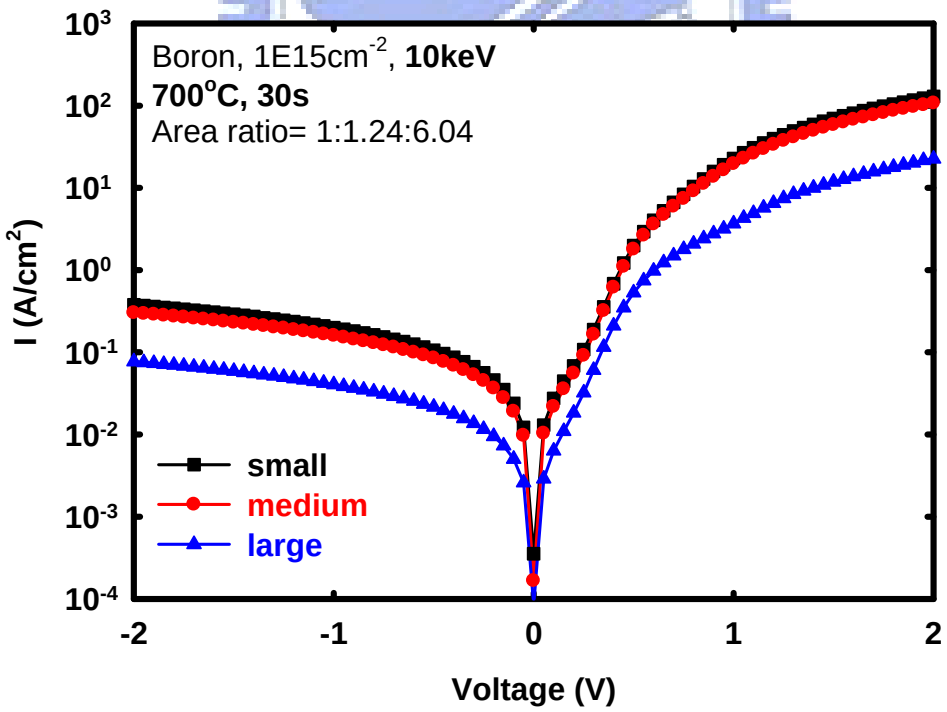


Fig. 3-7(a) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 700°C 30s. Reverse leakage current was divided by different area.

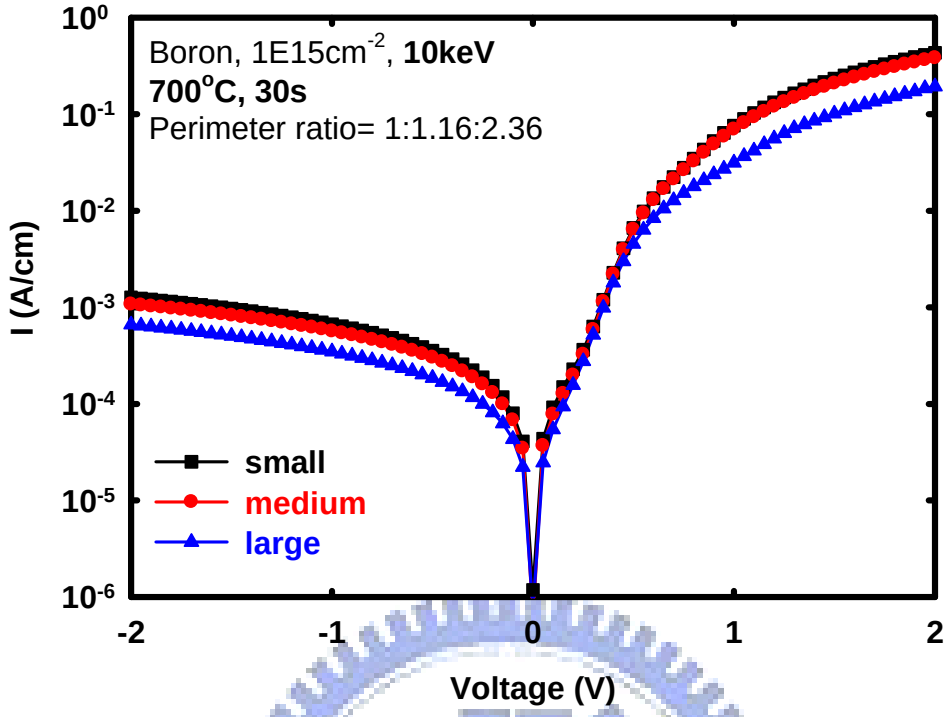


Fig. 3-7(b) P^+ N diode was implanted by Boron with 10keV energy and $1x10^{15}cm^{-2}$ dose and annealing at 700°C 2 minutes. Reverse leakage current was divided by different perimeter.

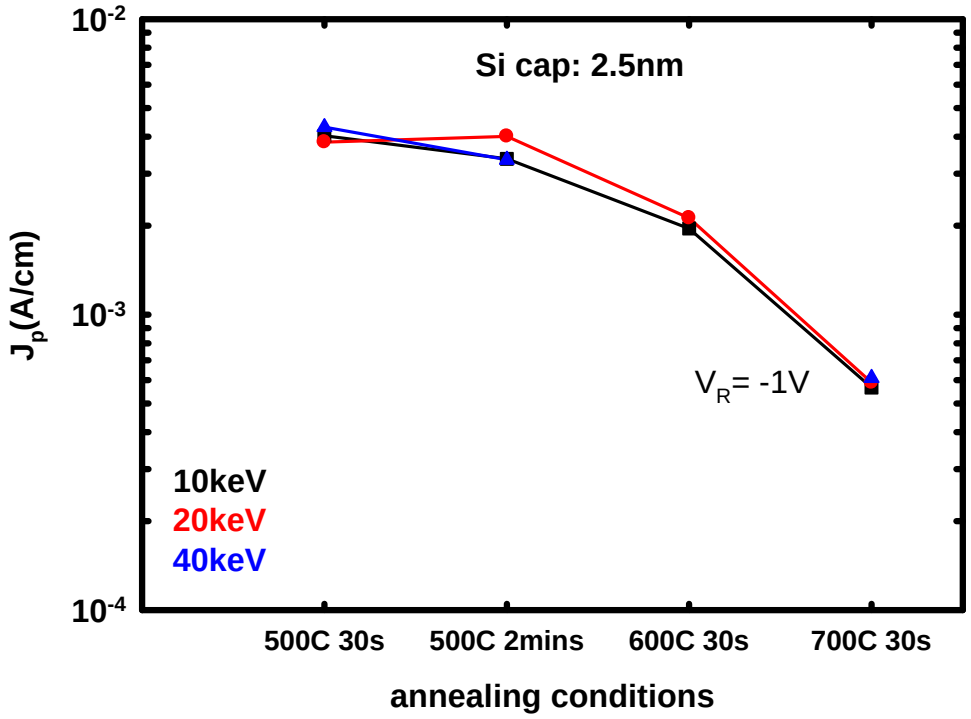


Fig. 3-8 Effects of thermal budget on peripheral leakage current (J_p) at V_R=-1V. The measurement of junction leakage is 2.5nm Si capping layer.

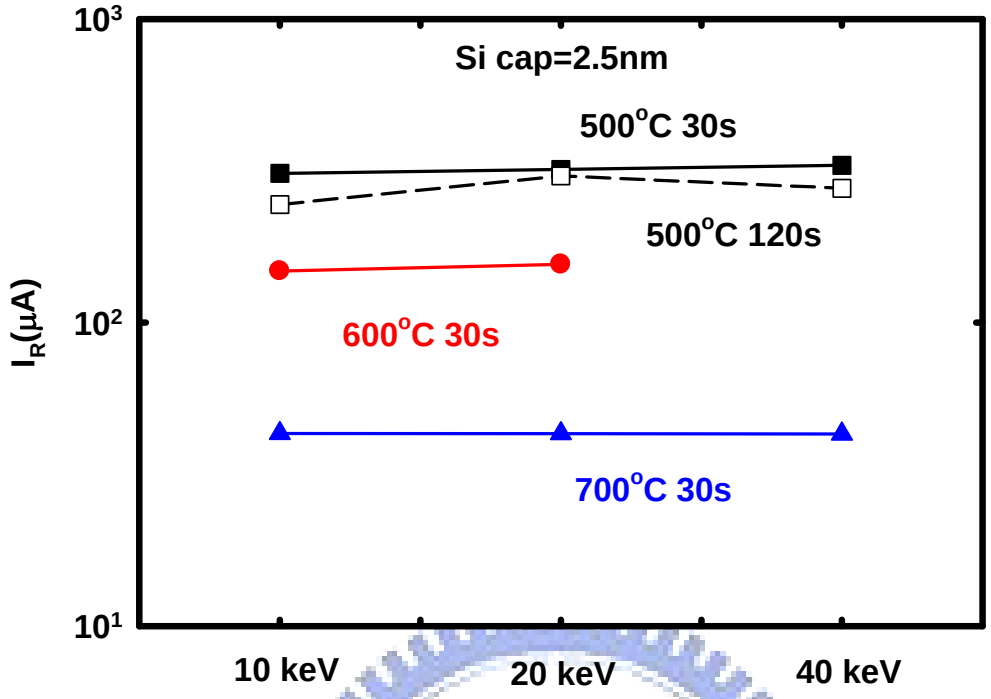


Fig. 3-9 Effects of thermal budget on junction leakage current at V_R=-1V. The measurement of junction leakage is 2.5nm Si capping layer.

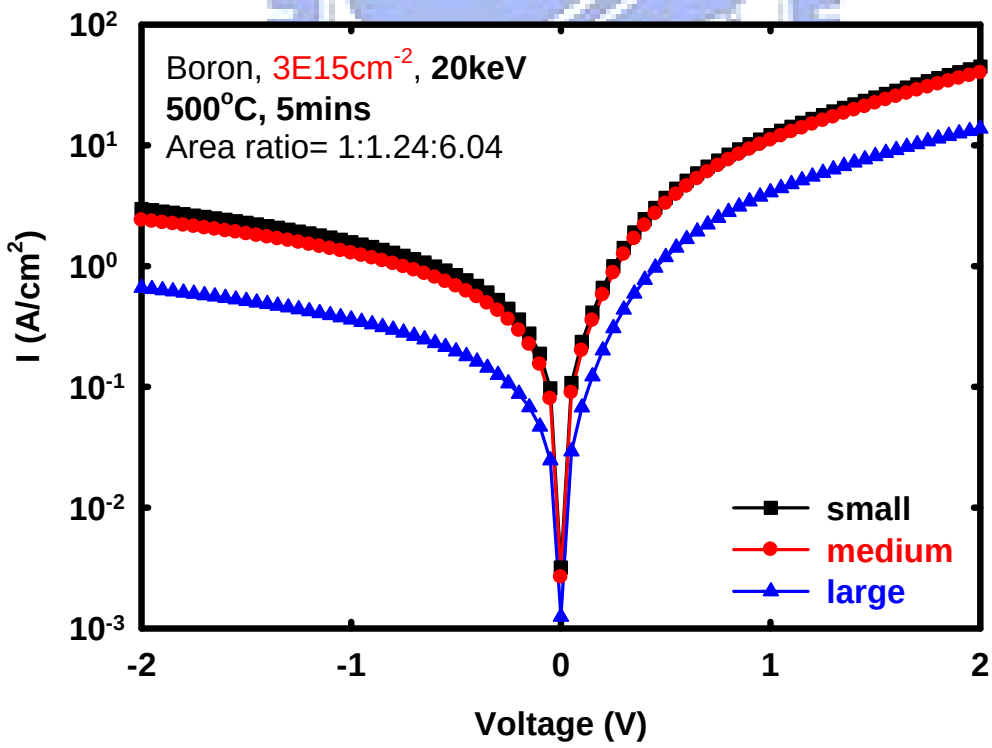


Fig. 3-10(a) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 500°C 5 minutes. Reverse leakage current was divided by different area.

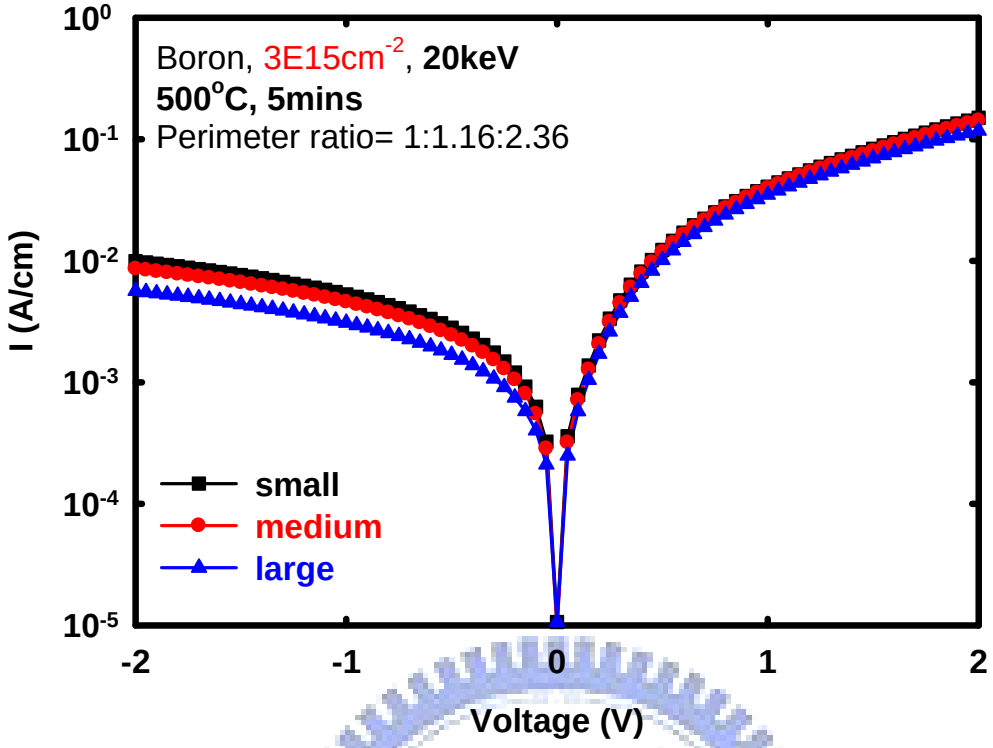


Fig. 3-10(b) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 500°C 5 minutes. Reverse leakage current was divided by different perimeter.

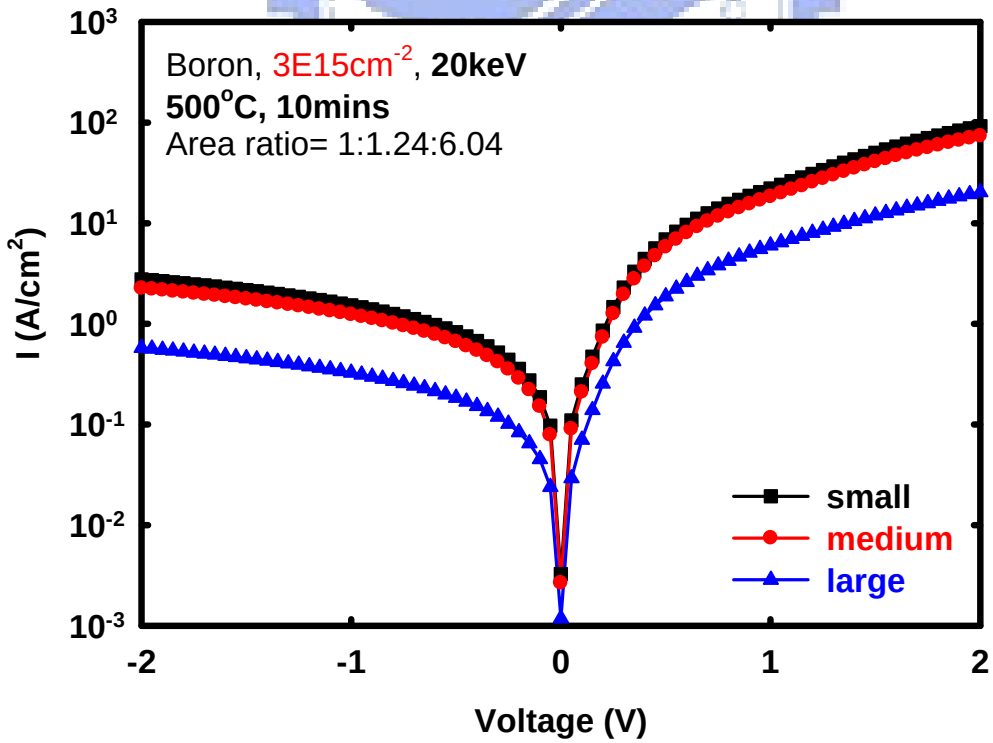


Fig. 3-11(a) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 500°C 10 minutes. Reverse leakage current was divided by different area.

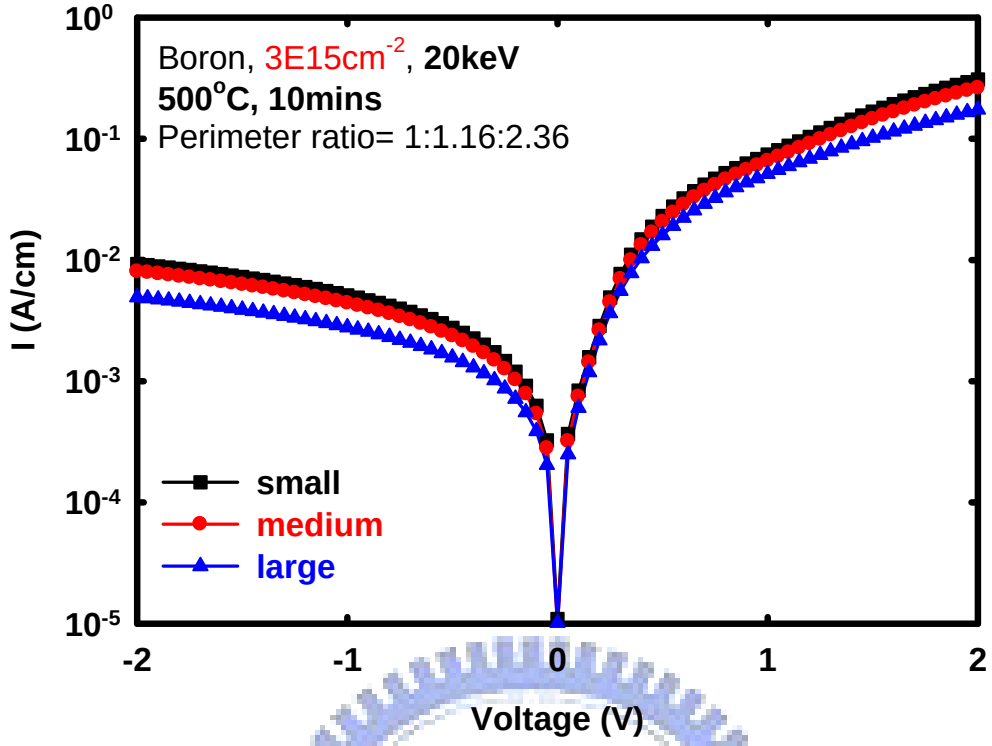


Fig. 3-11(b) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 500°C 10 minutes. Reverse leakage current was divided by different perimeter.

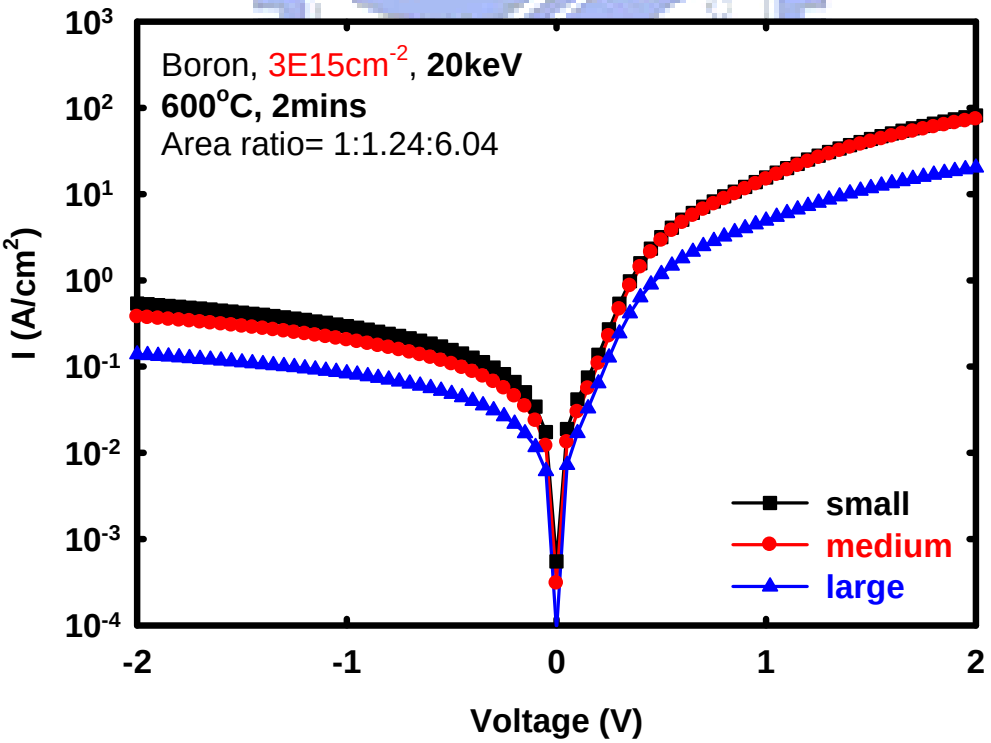


Fig. 3-12(a) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 600°C 2 minutes. Reverse leakage current was divided by different area.

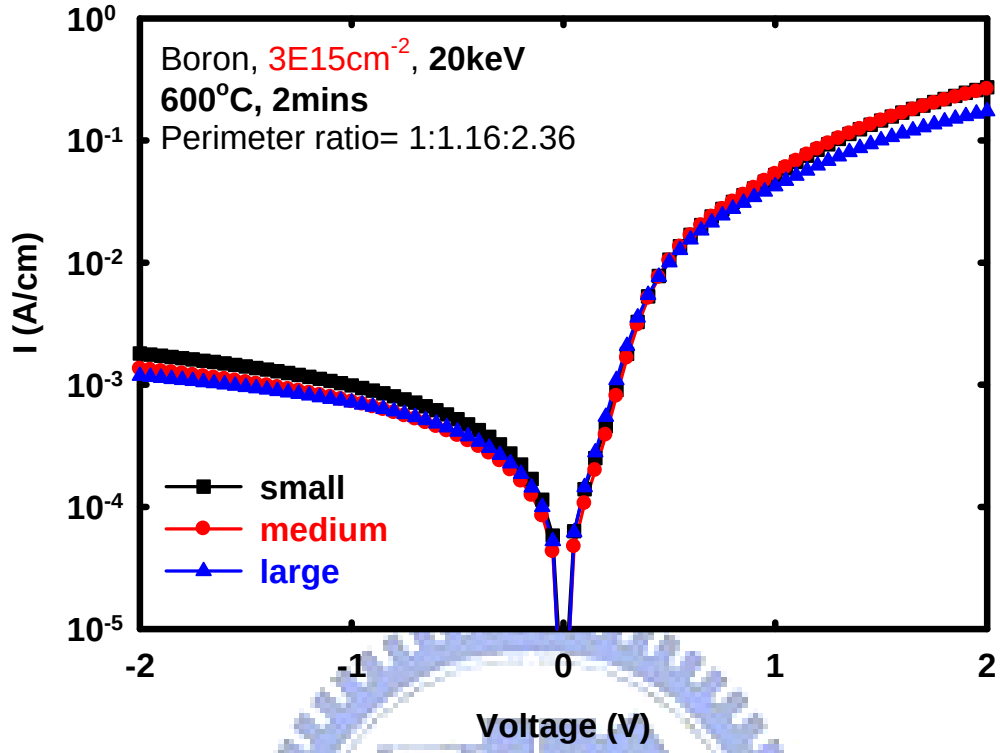


Fig. 3-12(b) P^+ N diode was implanted by Boron with 20keV energy and $3x10^{15}cm^{-2}$ dose and annealing at 600°C 2 minutes. Reverse leakage current was divided by different perimeter.

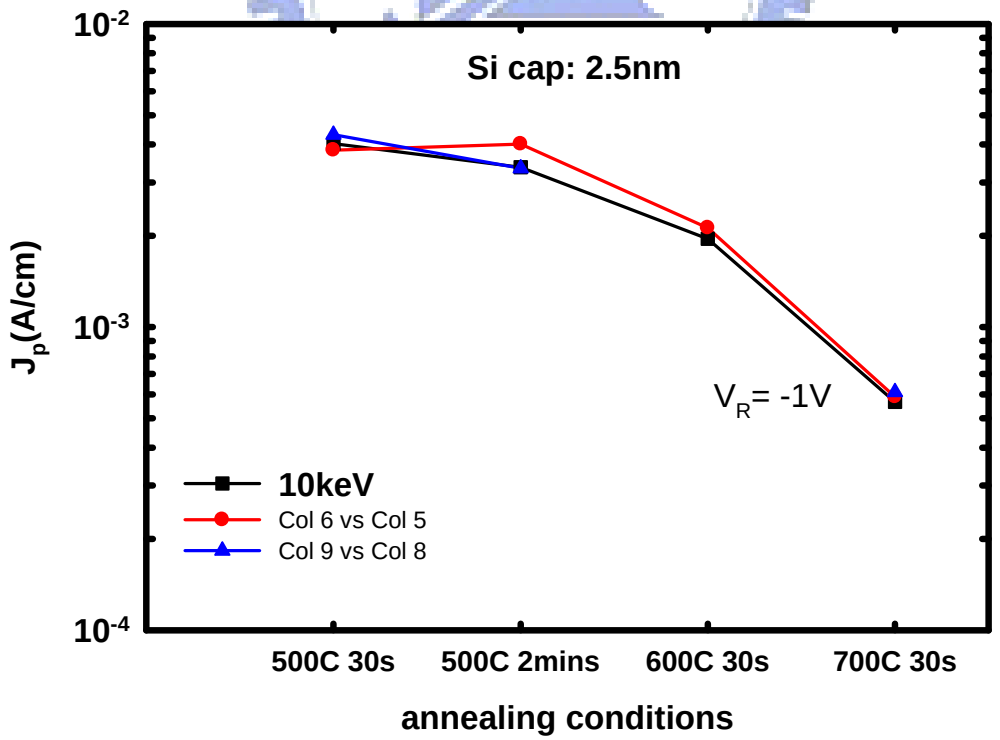


Fig. 3-13(a) Effects of thermal budget on peripheral leakage current (J_p) at V_R=-1V. The measurement of junction leakage is 2.5nm Si capping layer.

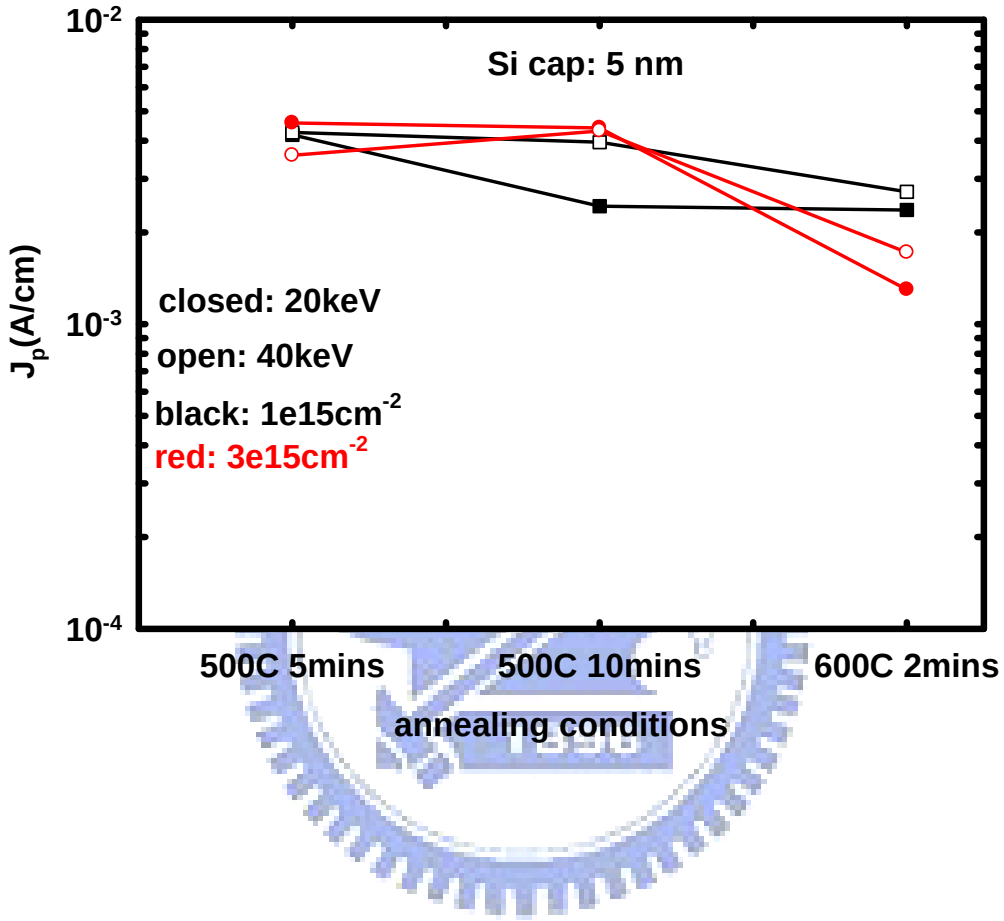


Fig. 3-13(b) Effects of thermal budget on peripheral leakage current (J_p) at V_R=-1V. The measurement of junction leakage is 5nm Si capping layer.

Chapter 4

Conclusions

4-1 Conclusions

Ge PMOSFETs

In this thesis, we presented two different substrate materials. One is the bulk Ge (n-type), the other is epitaxial Ge channel on Si substrate by UHVCVD. At the beginning, we used gate last process to fabricate Ge PMOSFETs. Then, we measured the electrical properties by Agilent 4284 LCR meter and Keithley 4200 semiconductor characterization. We found the mobility of our device is less than Si universality. In order to improvement of our devices, we employed forming gas anneal (FGA) to improve the electrical properties. It has been reported that high temperature FGA could improve the carrier mobility in Si and Ge. As a result of Ge out-diffusion during higher temperature (>400^{o}C), we decided to employed the lower temperature forming gas anneal (<400^{o}C) to improve the interface quality between the Ge substrate and high-k Al_2O_3 dielectric. The reverse current of p+ n junction would be reduced after 300^{o}C FGA. Because hydrogen would passivate the defects near the surface such that the reduction of leakage current. But the leakage current would increase immediately after higher temperature (>400^{o}C). As a result of the formation of pits or voids near the surface and fast diffusion of Al into Ge bulk, these generated defects so that the leakage current increased.

Hence, 300°C FGA device had the lower leakage current, subthershold swing, and interface state density (D_{it}). But the effective mobility after 300°C FGA just had a little improvement compared with as-deposited samples. However, 400°C FGA samples had the larger leakage current, subthreshold swing, and interface state density (D_{it}). But 400°C FGA samples had largest mobility in our work. It had 2 times in comparison with as-deposited samples. Finally, we used CVS to evaluate the quality of dielectric. We found that samples after FGA had better quality in comparison with as-deposited.

$Si_{1-x}Ge_x$/Ge/Si p^+-n junction

We already utilized the epitaxial substrate materials to fabricate the pn junction. From the electrical analysis, we found that peripheral leakage current dominated the reverse leakage current with 2.5 and 5nm Si capping layers. And we thought the defects in Si capping layer attributed to peripheral current. Since, 500°C~700°C could not repair defects from implantation. However, higher annealing temperatures were not good for Ge channel. Hence, we could deposit the thinner Si (<1 nm) capping layer top of Ge channel. Because, the thinner Si layer can be consume in continuous processes and Si capping layer can be the passivation layer to passivate Ge surface to gain the better interface quality.

References

[1] S.-H. Lo, D. A. Buchanan, Y. Taur, W. Wang “Quantum-Mechanical Modeling of Electron Tunneling Current from Inversion Layer of Ultra-Thin-Oxide nMOSFET’s” IEEE Electron Device Lett., Vol. 18, No. 5, p.209(1997).

[2] Donald A. Neamen, Semiconductor Physics And Devices, Mcgraw.

[3] J.J.-H. Chen, N.A. Bojarczuk, Jr., H. Shang, J. B. Hannon, J. Karasinski, E. Preisler, S.K. Banerjee “Ultrathin Al2O3 and HfO2 Gate Dielectrics on Surface-Nitrided Ge” IEEE Trans. Electron Device, vol. 51, no. 9, p.1441-1447, Sep. 2004.

[4] N. Wu, Q. Zhang, Q. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, D. L. Kwong “Alternative surface passivation on germanium for metal-oxide-semiconductor applications with high-*k* gate dielectric” Appl. Phys. Lett., vol. 85, no. 18, p. 4127-4129, Nov. 2004.

[5] A. Dimoulas, D. P. Brunco, S. Ferrari, J. W. Seo, Y. Panayiotatos, A. Sotiropoulos, T. Conard, M. Caymax, S. Spiga, M. Fanciulli, Xh. Dieker, E. K. Evangelou, S. Galata, M. Houssa, M. M. Heyns “Interface engineering for Ge metal-oxide-semiconductor devices” Thin Solid Films ,515, p.6337-6343,2007

[6] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, K. C. Saraswat “Germanium MOS Capacitors Incorporating Ultrathin High-*k* Gate Dielectric” IEEE Electron Device Lett., vol. 23, no.8, Aug. 2002.

[7] D. P. Brunco et al. “Germanium MOSFET Devices: Advances in Materials Understanding, Process Development, and Electrical Performance” I J. Electrochem. Soc., Volume 155, Issue 7, pp. H552-H561 (2008).

[8] Yoshiki Kamata “High-k/Ge MOSFETs for future nanoelectronics” Materialstoday vol. 21, no.1-2, Jan-Feb 2008.

[9] A. Stesmans “Passivation of P_{b0} and P_{b1} interface defects in thermal (100)Si/SiO_2 with molecular hydrogen” Appl. Phys. Lett., Vol. 68, No. 15, Apr. 1996

[10] R. Choi, C. S. Kang, H. J. Cho, Y. H. Kim, M. S. Akbar, J. C. Lee “Effects of high temperature forming gas anneal on the characteristics of metal-oxide-semiconductor field-effect transistor with HfO_2 gate stack” Appl. Phys. Lett., Vol. 84, No. 24, June 2004.

[11] C. C. Yeo, M. H. Lee, C. W.. Liu, K. J. Choi, T. W.. Lee and B. J. Cho “Metal gate/high-*k* dielectric stack on Si cap/ultra-thin pure Gee pi/Si subtrate” Electron Devices, p. 107-110 Dec. 2005.

[12] H. Y. Jin, N. W. Cheung “Forming Gas Annealing Characteristics of Germanium-on-Insulator Substrates” IEEE Electron Devices Lett., vol. 29, no. 7, July 2008

[13] A. Satta, G. Nicholas, E. Simoen, M. Houssa, A. Dimoulas, B. De Jaeger, J. Van Steenbergen, M. Meuris “Impact of germanium surface passivation on the leakage current of shallow planar p-n junctions” Materials Science in Semi. Processing 9 (2006) 716-720.

[14] D. P. Brunco, K. Opsomer, B. De Jaeger, G. Winderickz, K. Verheyden, and M. Meuris "Observation and Suppression of Nickel Germanide Overgrowth on Germanium Substrates with Patterned SiO_2 Structures" Electrochem. Solid-State Lette., 11, H39 (2008)

[15] Nan Wu, Qingchun Zhang, N. Balasubramanian, Daniel S. H. Chan, C. Zhu "Characteristics of self-aligned gate-first Ge p- and n-channel mosfets using CVD HfO_2 gate dielectric and Si surface passivation" IEEE Trans. Electron Device, vol. 54, no. 4, April 2007.

[16] P Zimmerman, G Nicholas, B De Jaeger, B Kaczer, A Stesmans,. L-A Ragnarsson, D P Brunco, F E Leys, M Caymax, k Opsomer, M Meuris, and M M Heyns "High performance ge pMOS devices using a Si-compatible precess flow" IEDM 2006 p.1-4.

[17] W. P. Bai, N. Lu, and D.- L. Kwong "Si Interlayer Passivation on Germanium MOS With High-k Dielectric and Metal Gate " IEEE Electron Devices Lett., vol. 26, no. 6, June 2005.

[18] Ook Sang Yoo, Jungwoo Oh, Chang Yong Kang, et al. "Effect of Si interlayer thickness and post-metallization annealing on Ge MOS capacitor on Ge-on-Si substrate" Mater. Sci. Eng. B (2008) 11728.

[19] Chao-Ching Cheng, Chao-Hsin Chien, Guang-Li Luo, Chun-Hui Yand, Mei-Ling Kuo, Je-Hung Lin, and Chun-Yen Chang "Ultrathin Si capping layer suppresses charge trapping in HfO_xN_y/Ge metal-insulator-semiconductor capacitors" Appl. Phys. Lett., Vol. 90, 012905 (2007).

[20] Yuan Taur, Tak H. Ning Fundamentals of Modern VLSI Devices, Cambridge.

簡　歷

姓 名： 陳 弘 森

性 別： 男

出 生 日 期： 民國 71 年 12 月 30 日

籍 貫： 台灣省新竹市

地 址： 新竹市延平路一段 214 巷 155 號

學 歷： 私立逢甲大學 電子工程學系

(90 年 9 月 ～ 94 年 6 月)

國立交通大學 電子工程研究所碩士班

(95 年 9 月 ～ 97 年 9 月)

碩士論文題目：

鍺基板及磊晶鍺通道製作 P 型金氧半場效電晶體與電性分析研究

Studies of device fabrication and electrical characteristics of bulk Ge and epitaxial Ge channel pMOSFETs