國立交通大學

電子工程學系　電子研究所

碩士論文

以準分子雷射退火製作控制晶界位置之多閘極複晶矽薄膜電晶體之研究

Study on the Polycrystalline Silicon Thin Film Transistors with Location-Controlled Grain Boundary and Multi-Gate Structure Using Excimer Laser Annealing

研 究 生：李序恒　　Syu-Heng Lee

指導教授：鄭晃忠 博士　　Dr. Huang-Chung Cheng

中 華 民 國 九十七 年 七 月

以準分子雷射退火製作控制晶界位置之多閘極複晶矽薄膜電晶體之研究

Study on the Polycrystalline Silicon Thin-Film Transistors with Location-Controlled Grain Boundary and Multi-Gate Structure Using Excimer Laser Annealing

研 究 生：李序恒　　Student : Syu-Heng Lee

指導教授：鄭晃忠 博士　　Advisor : Dr. Huang-Chung Cheng

國立交通大學
電子工程學系 電子研究所碩士班
碩士論文

A Thesis
Submitted to Department of Electronics Engineering
& Institute of Electronics
College of Electrical and Computer Engineering
National Chiao-Tung University
In Partial Fulfillment of the Requirements
For the Degree of Master
In
Electronics Engineering
July, 2008
Hsinchu, Taiwan, Republic of China

中華民國 九十七 年 七 月

以準分子雷射退火製作控制晶界位置之多閘極複晶矽薄膜電晶體之研究

研究生：李序恒　　　　　　　　指導教授：鄭晃忠 博士

國立交通大學

電子工程學系 電子研究所碩士班

摘要

近年來，低溫複晶矽薄膜電晶體成為顯示技術應用中的關鍵元件，由於其高載子遷移率的特性可以應用在系統面板（System on Panel, SOP）上。雖然透過傳統準分子電射退火方式可轉化非晶矽薄膜成為複晶矽，但此方法仍有些許缺點，如較狹窄的雷射製程條件、小晶粒與隨機分佈的晶粒邊界隨機分佈等等。在這篇論文裡，我們提出一種易於控制雷射結晶方式，並利用該雷射結晶方式配合多閘極結構來增進複晶矽薄膜電晶體的特性。

在第一部份，我們提出一種稱為氧化矽臺階式通道結晶法（Recessed-Channel with Oxide Step Method）之側向結晶方式，應用於製作

可控制晶粒邊界位置之低溫複晶矽薄膜電晶體並加以探討，我們分析此種控制晶粒邊界位置技術之結晶機制分為山脊區與凹陷區之結晶：當雷射照射在凹陷區並使得完全熔融時，氧化矽側壁有較厚之未熔融矽薄膜作為晶種，晶粒便會在凹陷區作側向成長；當雷射照射在長度為 2μm之山脊區時，由於山脊區中間部份比邊緣儲熱時間較久，故先有矽晶種產生且成長為小晶粒，阻擋由氧化矽側壁向山脊區中央側向成長之晶粒，我們把山脊區長度縮減為 1.5 μm則可避免此現象；我們可以到均勻且方向一致的大型多晶矽晶粒分佈之複晶矽薄膜，因此可提升薄膜的均勻性與元件的效能。此外，我們利用掃描式電子顯微鏡、掃瞄原子力顯微鏡對控制晶粒邊界之複晶矽薄膜層分析，我們觀察到在谷區中有約 1.5 μm長的人為控制晶粒，在山脊區有約 0.75 μm長的人為控制晶粒。我們也利用此結晶方式製作出單一主要晶粒邊界的低溫複晶矽薄膜電晶體，並對其電特性加以研究。在無氫化過程處理下，其P型元件之場效載子移動率可達到 168 cm^2/V-s，其次臨界擺幅與汲極誘導體能障下降可達 0.226 V/decade和 310 mV。同時我們也比較製作元件於谷區與山脊區的各項電特性，在固定山脊區長度為 2μm條件下，山脊區中間因有小型晶粒分佈，使得元件製作於山脊區之電特性較製作於谷區差，其製作於山脊區之元件的場效載子移動率為 99 cm^2/V-s。

儘管單一主要晶粒邊界之複晶矽薄膜電晶體表現出良好的電特性，然而在元件通道中的單一主要晶粒邊界仍會對電特性產生影響。因此在第二部份，我們引入多閘極結構，研究避開單一晶粒邊界影響之電特性。在沒經過任何氫化處理過程下，P型元件之場效載子移動率更超過 190 cm^2/V-s。量測二十個元件的均勻性，場效載子移動率標準差小於 30 cm^2/V-s，臨界電壓的標準差小於 0.78 V，次臨界擺幅之標準差 0.113 V/decade。透過多閘極之結構，我們可以觀察到陡峭之次臨界擺幅，其可達 0.164 V/decade。另外相較於傳統結晶方式之多閘極複晶矽薄膜電晶體，我們也獲得 6 倍以上之驅動電流。

Study on the Polycrystalline Silicon Thin Film Transistors with Location-controlled Grain Boundary and Multi-Gate Structure Using Excimer Laser Annealing

Student: Syu-Heng Lee **Advisor: Dr. Huang-Chung Cheng**

Department of Electronics Engineering & Institute of Electronics

National Chiao Tung University

ABSTRACT

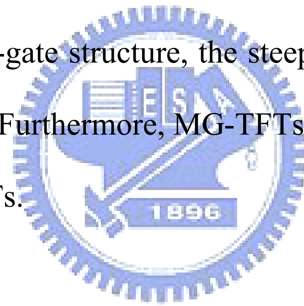
In recent years, polycrystalline silicon (poly-Si) thin film transistors (TFTs) were the key devices in flat-panel display technology and System on a Panel (SOP) applications due to its high mobility. Although conventional excimer laser can transfer amorphous Si to polycrystalline Si in order to fabricate poly-Si TFTs. There were still some disadvantages such as narrow laser process window, random small grain and grain boundaries, and etc.. In this thesis, therefore, we proposed a method, which is so called Recessed-Channel with Oxide Step method, to control the grain growth and grain boundary. With the benefits of this crystallization method and multi-gate structure, high performance multi-gate poly-Si TFTs had been fabricated with no main grain boundary in the channel region.

At the first part, single grain boundary (SGB) thin film transistors (TFTs) fabricated by excimer laser annealing were investigated. The crystallization mechanisms of valley region and ridge region of Recess-Channel with Oxide Step method were studied. A thick amorphous silicon region was formed in the sidewall of

oxide step which acted as the seeds for the grain lateral growth during excimer laser irradiation. As the excimer energy density was controlled to completely melt the amorphous silicon thin film of valley region and partially melt the thick part in the sidewall of the oxide step. The lateral growth grain would be observed in the valley region. When laser irradiated the ridge region with channel length of 2 μm, the holding time of thermal energy of the edge of the ridge region was longer than that of the center of the ridge region. There were small grains in the middle of the ridge region, and the small grains obstructed the growth of the lateral grains from the sidewall to the center. We decreased the length of the ridge region to 1.5 μm, the phenomenon of grain obstruction would be eliminated. Therefore, the lateral growth grain starting from un-melt silicon seeds could extend along the opposite direction toward the complete melt valley region and ridge region. Thus, a uniform and large grain of polycrystalline silicon film would lead to improved device performance. According to the analysis of scanning electron microscope (SEM) and atomic force microscope (AFM), large longitudinal grains were observed to be about 1.5 μm in valley region and about 0.75 μm in ridge region. The electrical characteristics of single grain boundary TFTs fabricated by Recessed-Channel with Oxide Step TFTs were also investigated. High performance p-type SGB-TFTs with field-effect mobility reaching 168 cm^2/V-s had been fabricated without any hydrogenation treatment. The subtheshold swing and drain-induced-barrier-lowing (DIBL) of SGB-TFTs were 0.226 V/decade and 310 mV respectively. In addition, the electrical characteristics of devices located on the valley region and ridge region were studied. While the length of ridge region was 2μm, there was a small grain region in the middle of ridge region. Because the crystalline of ridge region of poly-Si thin film was defective, the electrical characteristics of devices located on ridge region were poorer than that of devices located on valley region. The field-effect mobility of devices located on ridge

region was 99 cm^2/V-s.

Although SGB-TFTs exhibited high performance, the electrical characteristics of SGB-TFTs were affected by the single main grain boundary located in device channel. Hence, we introduced the multi-gate (MG) structure to eliminate the single grain boundary effect and investigated the electrical characteristics of multi-gate TFTs in order to avoid the single main grain boundary in the channel. High performance p-type MG-TFTs with field-effect mobility exceeding 190 cm^2/V-s had been fabricated without any hydrogenation treatment. The characteristics of twenty MG-TFTs devices were taken into discussion. The standard deviation of equivalent field-effect mobility was smaller than 30 cm^2/V-s and the standard deviation of Vth was smaller than 0.78 V, while that of subthreshold swing was smaller than 0.113 V/decade. By means of multi-gate structure, the steeper subthreshold swing reaching 0.164V/decade was obtained. Furthermore, MG-TFTs provided 6 times higher driving current than conventional TFTs.



誌　謝

感謝我的碩士論文指導教授 鄭晃忠博士教導我在實驗、論文上的嚴謹態度及謙恭溫和的待人處事，讓學生受益許多。

感謝蔡春乾學長與韋凱方學長帶我進入低溫多晶矽薄膜電晶體的領域，兩位學長除了原諒我在作人處事上的無知與實驗上的懶惰之外，還在休息時間被我的實驗上問題打擾及給我各方面問題的指點，同時分享生活上的趣事與不斷的幫我打氣加油，真的很感謝你們在我碩士生涯中的幫助。

感謝李逸哲學長與楊柏宇學長在我碩士生涯後半年的指導，教導許多量測知識，同時在量測累的時侯鼓勵我。

感謝 TFT 組的學長，同學，學弟妹，謝謝你們使得我的兩年碩士生涯增加許多樂趣，其中包括張國瑞學長、廖大傳學長、王祐祈學長、劉全豐學長、林心瑜學姐、涂仕煒同學、林偉凱同學、劉政欽同學、胡明哲學弟、鄧茜云學妹、徐邦祐學弟、陳聖凱學弟。

感謝 CNT 組的學長，同學，學弟，謝謝你們使得我在實驗室的日子快樂不少，其中包括林高照學長、張加聰學長、張佩琪學姐、陳俠威學長、柳耀星學長、林君翰學長、許育瑛同學，李建穎同學、魏英彰學弟、蔡萬霖學弟。

感謝老師的助理們，感謝你們在行政上的協助幫忙，其中包括碧蓮助理、依婷助理及采綸助理。

感謝國家奈米中心的裡常幫助我的工程師與技術員，由於你們在實驗機台上的幫助，使得我能完成實驗，特別是彭馨誼小姐、鄭旭君先生、吳志明先生、薛富國先生、趙子綾小姐、林婉貞小姐、陳秉賢學長、簡秀芳小姐。

感謝我的父母與家人和親戚，感謝父母養育我從小到大，且伴我渡過在生活中的困難；感謝哥哥姐姐伴我從小到大的生活；感謝親戚讓我離鄉仍有家的感覺。

感謝鄭晨薇小姐，感謝妳貼心的舉動，準備好的水果與加油打氣的字語帶給我的支持動力。

感謝大學同學鄭淑媖同學，心情低落時常一起喝飲料討論工作與實驗。

最後，感謝所以幫助過我的朋友，謝謝你們。

Contents

Abstract (in Chinese)……………………………………………………………….i

Abstract (in English)………………………………………………………………iii

Acknowledgements (in Chinese)...vi

Contents……………………………………………………………………………...vii

Table Lists…...…………………………………………………………………… x

Figure Captions……………………………………..…………………………..…xii

==

Chapter 1 Introduction……..……………………………………………………...1

1.1 Overview of Low-Temperature Polycrystalline Silicon (LTPS) Thin-Film Transistors (TFTs)………...………………………………………………………1

1.2 Overview of Crystallization of Amorphous Silicon Thin Films…………………..2

1.2.1 Solid Phase Crystallization of Amorphous Silicon Thin Films……………..3

1.2.2 Metal Induced Crystallization of Amorphous Silicon Thin Films…………4

1.2.3 Laser Irradiation Crystallization of Amorphous Silicon Thin Films……….4

1.3 Ion activation…………………………………………………………………....8

1.4 Motivation...10

1.4.1 Fabrication of Polycrystalline Silicon Thin Films with Location-Controlled Grain Boundary Technology……………………………………………..11

1.4.2 Polycrystalline Silicon Thin Film Transistors with Multi-Gate Structure by Recessed-Channel with Oxide Step Process………………………….....12

1.5 Thesis Organization…………………………..……………………………..13

Chapter 2 Fabrication of Location-Controlled Single-Grain-Boundary (SGB) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFTs) by

Recessed-Channel with Oxide Step Methods Using Excimer Laser Annealing (ELA)………………………………………………….....15

2.1 Introduction……………………………………………………………………..15

2.1.1 Introduction to Recessed-Channel with Oxide Step Methods………….....15

2.2 Material Analyses of Single Grain Boundary Polycrystalline Silicon Thin Films Fabricated by Elevated Channel Methods……………………………………… 20

2.2.1 Process Flow of Material Analyses of Location-Control SGB Poly-Si Thin Films Fabricated by Recessed-Channel with Oxide Step Method …........20

2.2.2 Material Analysis of Location-Controlled SGB Poly-Si Thin Film Fabricated by Recessed-Channel with Oxide Step Method…….........21

2.2.2.1 Scanning Electron Microscope (SEM) Analysis…………………21

2.2.2.2 Transmission Electron Microscope (TEM) Analysis…………....24

2.3 Fabrication and Electrical Characteristics Analyses of Location-Controlled Single Grain Boundary (SGB) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFT) Fabricated by Recessed-Channel with Oxide Step Method………..…….25

2.3.1 Process Flow of SGB-TFTs by Recessed-Channel with Oxide Step Method……..……26

2.3.2 Electrical Characteristics of SGB-DG-TFTs……...…………………......27

2.4 Summary……………………………………………………………………29

Chapter 3 Investigation of Main Grain Boundary effect effect of Single-Grain-Boundary (SGB) Thin Film Transistors by Recessed-Channel with Oxide Step method.......……………….....……31

3.1 Introduction……………………………………………………………………31

3.2 The Grain Boundary issue... ………...……………32

3.3 Solution of Reducing Main Grain Boundary Influence……………...…………33

3.3.1 Introduction to Multi-Gate (MG) Polycrystalline Silicon Thin Film

Transistors by Recessed-Channel with Oxide Step method……………..………33

3.3.2 Process flow of MG-TFTs by Recessed-Channel with Oxide Step method.34

3.3.3 Electrical Characteristics Analysis MG-TFTs by Recessed-Channel with

Oxide Step Method………………………………………………….……...35

3.3.3.1 Improvement Comparison of MG-TFTs and SG-TFTs with/without

Location-Controlled Grain Boundary Structure……………….……...35

3.2.3.2 Electrical Characteristics of MG-TFTs by Recessed-Channel with

Oxide Step Method ………………………………………..…….38

3.2.3.3 Uniformity of MG-TFTs by Recessed-Channel with Oxide Step

Method……………………………………………………….......40

3.4 Summary………………………………………………………………….....41

Chapter 4 Conclusions…………………………………………………...…………43

Table………………………………………………………………………………….45

Figure Caption…………………………………………………………………….....49

References…………………………………………………………………………...82

Table lists

Chapter 2

Table 2-1 Measured optimal electrical characteristics of P-type SGB-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)…………………………………………………...45

Table 2-2 Measured optimal electrical characteristics of P-type SGB-TFTs fabricated by Recessed-Channel with Oxide Step method were located above the valley region and ridge region, respectively. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)………45

Chapter 3

Table 3-1 Measured optimal electrical characteristics of P-type MG-TFTs and SG-TFTs fabricated by Recessed-Channel with Oxide Step method. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)…………………………………………………...45

Table 3-2 Measured optimal electrical characteristics of P-type MG-TFTs and SG-TFTs fabricated without any location-controlled grain boundary technology. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)……………………………46

Table 3-3 The improvement of electrical characteristics of devices with/without location-controlled grain boundary……………………………………46

Table 3-4 The improvement of electrical characteristics of different gate structure devices with/without location-controlled grain boundary………………..47

Table 3-5 Measured optimal electrical characteristics of P-type MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional MG-TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)……………………………………………47

Table 3-6 Electrical characteristics of twenty measured P-type MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional MG-TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping)……………………………………………48

Figure Captures

Chapter 2

Fig. 2.1 (a) The schematic illustration of the low energy regime corresponding to energy densities that partially melting the a-Si thin film…………………..49

Fig. 2.1 (b) The schematic illustration of the high energy regime corresponding to energy densities that completely melting the a-Si thin film………………..49

Fig. 2.1 (c) The schematic illustration of the super lateral growth regime corresponding to energy densities that nearly completely melting the a-Si thin film……………………………………………………………….49

Fig. 2.2 The schematic illustration of the grain growth regime of the Recessed-Channel structure by excimer laser annealing…………………….50

Fig. 2.3 The device diagram with Recessed-Channel method……………………….50

Fig. 2.4 The comparison of Recessed-Channel method and Recessed-Channel with Oxide Step method………………………………………………………51

Fig. 2.5 Process flow of preparing samples for material characteristics by Recessed-Channel with Oxide Step method………………………………52

Fig. 2.6 The definition of valley region and the ridge region of the Recessed-Channel with Oxide Step structure……………………………………………….…..53

Fig.2.7 SEM graphs of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the valley region

1896

was varied from (a) 1.5μm to (b) 3μm. The excimer laser energy density was 540 mJ/cm^2……………………………………………………………...53

Fig. 2.8 SEM graphs of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the oxide ridge region was varied from (a) 1.5 μm to (b) 2 μm. The excimer laser energy density was 480 mJ/cm^2…………………………………………………54

Fig. 2.9 SEM graphs of the ridge region of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the oxide ridge was 2 μm. The excimer laser energy density was varied (a) 600 mJ/cm^2 (b) 540 mJ/cm^2 (c)480 mJ/cm^2…………………………………………………….55

Fig. 2.10 SEM graphs of excimer laser crystallized polycrystalline silicon by period step pre-pattern silicon method. The length between the steps was 3 μm. The laser energy density was (a) 520 (b) 560 (c) 600 mJ/cm^2………………….56

Fig. 2.11 SEM graphs of excimer laser crystallized polycrystalline silicon by period step pre-pattern silicon method. The length of the steps was 1.5 μm. The laser energy density was (a) 460 (b) 540 (c) 600 mJ/cm^2………………….58

Fig. 2-12 AFM graphs of valley region of excimer laser crystallized polycrystalline silicon with Recessed-Channel with Oxide Step structure. The length of valley region was 3 μm and the excimer laser energy density was 600 mJ/cm^2…………………………………………………………………...59

Fig. 2-13 AFM graphs of valley region of excimer laser crystallized polycrystalline silicon with Recessed-Channel with Oxide Step structure. The length of

valley region was 1.5 μm and the excimer laser energy density was 600 mJ/cm^2……………………………………………………………………...60

Fig. 2-14 Process flow for fabrication of SGB-TFTs by Recessed-Channel with Oxide Step method………………………………………………………………...61

Fig. 2-15 The typical transfer characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)………………………………………..64

Fig. 2-16 The output characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)………………………………………………………64

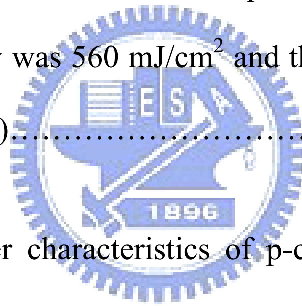


Fig. 2-17 The typical transfer characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)………………………………...65

Fig. 2-18 The output characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)…………………………………………………65

Fig. 2-19 SEM graph of the valley region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method………………………………66

Fig. 2-20 SEM graph of the ridge region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method……………………………….66

Chapter 3

Fig. 3-1 SEM graph of ridge region of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of ridge region was 3 μm. The excimer laser energy density was 600 mJ/cm^2……..67

Fig. 3-2 Process flow for fabrication of MG TFTs by Recessed-Channel with Oxide Step method…………………………………………………………...68

Fig. 3-3 The typical transfer characteristics of SG-TFTs and MG-TFTs with location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………………………………………………..71

Fig. 3-4 The output characteristics of SG-TFTs and MG-TFTs with location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………………………………………………..71

Fig. 3-5 The typical transfer characteristics of SG-TFTs and MG-TFTs fabricated without location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………………………………………………..72

Fig. 3-6 The output characteristics of SG-TFTs and MG-TFTs fabricated without

location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………………………………………………..72

Fig. 3-7 Field-effect mobility improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology……………………………………………………………….73

Fig. 3-8 Subthreshold swing improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology……………………………………………………………….73

Fig. 3-9 Threshold voltage improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology…..74

Fig. 3-10 Leakage current improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology…..74

Fig. 3-11 Field-effect mobility improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology……………………………………………………………….75

Fig. 3-12 Subthreshold swing improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology……………………………………………………………….75

Fig. 3-13 Threshold voltage improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology…..76

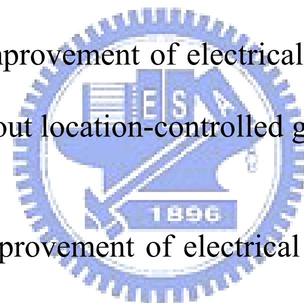


Fig. 3-14 Leakage current improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology…..76

Fig. 3-15 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………77

Fig. 3-16 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs.. The channel length was 2 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)…………………..77

Fig. 3-17 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs.. The channel length was 3 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)…………………..78

Fig. 3-18 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)…………………………………………………78

Fig. 3-19 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 2 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)…………………………………………………79

Fig. 3-20 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 3 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)……………………………………………..79

Fig. 3-21 Statistics and uniformity of equivalent field effect mobility. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping)……80

Fig. 3-22 Statistics and uniformity of threshold voltage. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping)…………………80

Fig. 3-23 Statistics and uniformity of subthreshold swing. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping)…………………81

Chapter 1
Introduction

1.1 Overview of Low-Temperature Polystalline Silicon (LTPS) Thin Film Transistors (TFTs)

Recently, thin film transistors (TFTs) have become important devices in large area electronics system applications in the past ten years, including active-matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs) [1.1]-[1.5].

Amorphous silicon thin film transistors (a-Si:H TFTs) were introduced in the 1970's, which have been used in many applications such as solar cells [1.6], image sensors, printing heads, electronic copiers [1.7]-[1.9], especially in the applications of AMLCDs [1.10]-[1.12] and newly developed AMOLEDs [1.13]-[1.15]. In the AMLCDs, a-Si:H TFTs is used as the pixel switch placed at each pixel for addressing. While in the AMOLEDs applications, a-Si:H TFTs is used as the active device to provide driving current for illumination. Amorphous silicon TFTs exhibit low leakage current because of their high off-state resistivity. In addition, they are compatible with

large glass substrate for low process temperature. However, the electrical characteristics of a-Si TFTs such as carrier mobility (typically below 1 $cm^2/V\text{-}s$) are inadequate for peripheral circuits . That is, additional integrated circuits (ICs) are needed to support the function of gate drivers and source drivers to drive a display panel. This will lead to high cost and poor reliability.

Polycrystalline silicon (poly-Si) was used to be the active material of TFTs for achieving higher performance in the 1980s. The effective carrier mobility in polycrystalline silicon was significantly higher (by two orders of magnitude) than those in amorphous silicon, so that both n- and p-channel TFTs with reasonably high currents could be achieved in polycrystalline silicon [1.16]. The capability to complementary metal-oxide-semiconductor (CMOS) circuits allows low-power driving circuitry to be integrated with the active matrix. The integration of both the active matrix pixel switching elements and the peripheral driving circuitry onto a single glass substrate, thus substantially reducing manufacturing complexity and cost. Therefore, LTPS TFTs have been investigated to achieve the goal of integrating peripheral circuit in a single panel, which is known as system on panel (SOP)

1.2 Overview of Crystallization of Amorphous Silicon Thin Films

The crystallinity of poly-Si thin film has great influence on the performance of poly-Si TFTs because the poly-Si thin film act as the channel region in the poly-Si TFTs. Therefore, a crystallization method was very important for LTPS poly-Si TFTs. For a poly-Si thin film, the grain boundary cause a lot of defects, which is called strained bonds and dangling bonds. These defects act as trap states within the band gap and will degrade the electrical characteristics of poly-Si TFTs, such as carrier

mobility, threshold voltage, subthreshold swing, and the leakage current. It is believed that poly-Si thin film could obtain less defects by enlarging the grain size. Further, it was important to control the grain size ,the orientation of the grains, and the location of the grains to fabricate high quality poly-Si thin films. There are several ways to make the amorphous silicon thin film be re-crystallized into polystalline silicon thin film by additional energy, including solid phase crystallization, metal induced crystallization, and laser irradiation crystallization. These methods have some differences between them and will be introduced in the following three sections.

1.2.1 Solid Phase Crystallization of Amorphous Silicon Thin Films

The solid phase crystallization (SPC) method is which the a-Si thin film can be re-crystallized to polystalline silicon thin film by thermal annealing. The maximum temperature in the SPC method is below 600℃ in order to compatible with glass substrate, the a-Si thin film is deposited at 550℃ using silane (SiH_4), and the following the SPC process, and the process temperature is kept at 600℃ in N_2 ambient, whereas the process time is about 24 hours [1.17]-[1.18].

The grain size of solid phase crystallized poly-Si thin film is several times larger than that of as-deposited poly-Si thin film. Besides, the surface morphology is much smoother in SPC poly-Si thin film than in as-doped ones. However, the SPC TFTs suffers a lot of intra-granular defects and result in a bad performance. The most important of all is the fact that the annealing time is too long and this will limit the throughput to fabricate poly-Si thin film.

1.2.2 Metal Induced Crystallization of Amorphous Silicon Thin Films

The metal induced crystallization (MIC) method is which inducing certain metals during the SPC process. The SPC's process annealing temperature of amorphous silicon could be lowered (<500℃) and process duration could be reduced (<5hrs). The higher throughput will be obtained. Several metals have been proposed to be applied to MIC process, such as aluminum (Al), aurum (Au), nickel (Ni), platinum (Pt). Among these metals, Ni has been shown to be the best candidate of metal induced crystallization method at low temperature for good performance polystalline silicon TFTs. When nickel was deposited on amorphous silicon, followed by thermal annealing, octahedral precipitates $NiSi_2$ would be formed on amorphous silicon films. Owing to the very small mismatch (0.4%) of crystal lattice constant between the <111> orientation faces of nickel silicide and crystalline silicon, the defects in crystal can be minimized [1.19]-[1.22].

However, because it is lower the SPC's annealing temperature by the addition of certain metals, the MIC re-crystallization method suffers high leakage current and cannot be avoided from MIC process. The metal residues act as metal contamination and offer leakage path under carrier transportation.

1.2.3 Laser irradiation Crystallization of Amorphous Silicon Thin Films

Laser crystallization process in fabrication silicon-on-insulator devices for microelectronics and thin-film transistors for displays has been receiving considerable attention [1.23]-[1.29]. Laser crystallization can produce large-grained poly-Si thin film with low intra-grain defects via liquid phase crystallization. Therefore, many

researches of laser crystallization of amorphous silicon films for the preparation of poly-Si films for LTPS TFTs have been studied using various kinds of lasers techniques, such as CO_2, Ar, Nd:YAG, Nd:YVO_4, excimer, femtosecond lasers, and etc [1.28]-[1.36]. Among these laser techniques, excimer laser annealing, to date, is the widely used method to prepare poly-Si thin films because of its high pulsed-laser power for large area glass substrate and the large absorption coefficient for a-Si in the UV light region (optical absorption coefficient > 10^6 cm^{-1}) for no damage to glass substrate. According the mixture gas used in the laser tube, excimer laser radiation of output wavelengths between 157 – 351 nm (157, 193, 248, 308 and 351 nm for F_2, ArF, KrF, XeCl and XeF laser, respectively) by the transient high voltage discharge with a short pulse duration (full width of half maximum ~ tens of nanoseconds). The basic principle of excimer laser crystallization is the phase transformation of silicon thin film from amorphous to single-crystal material via melting the Si thin film within a very short time. Actually, the a-Si thin film is heated to the temperature of about 1200℃ during laser irradiation. However, the high temperatures are only persistent for tens of nanoseconds during laser pulse duration. In consequence, the introduction of thermal damage to the glass substrate and the thermal compaction problem are relaxed, which are serious issues in the solid phase crystallization. Another unique advantage of excimer lasers is the strong optical absorption of UV light in silicon. As a result, most of the incident laser energy is absorbed closed to the surface of the thin film without causing severe thermal strain on the substrate. The unique advantages of strong optical absorption of the UV light in silicon and short pulse duration of the excimer laser imply that high temperature can be produced in the silicon surface region, causing rapidly melting and solidifying quickly, without significant heating the substrate and impurities contamination form the substrate diffusion into the silicon thin film. This technology yield high quality and large-grained poly-Si thin film for

high-performance LTPS TFTs on glass or plastic substrate with high throughput.

Owing to the advantageous features of excimer laser crystallation for large area microelectronics fabrication, many researches have been done to study the dynamics kinetics and transformation mechanisms of the laser crystallization of a-Si thin films. The characteristics of poly-Si thin film have been shown to be related to the process conditions of ELC, such as laser energy density, laser pulse duration, laser shot number per area, crystallization ambient, and substrate temperature [1.37]-[1.41]. Moreover, the initial status of a-Si precursor film, including a-Si film thickness, hydrogen content, and impurity content, has a profound effect on the properties of the resulting poly-Si film [1.41]-[1.44]. According to the reports of James. S. Im et al., excimer laser crystallization of amorphous silicon thin films on foreign substrate can be divide into three transformation regimes with respect to the applied laser energy densities [1.45]-[1.46]. These are the partial-melting, full-melting, and near-chomplete-melting regimes.

Partial-melting regime (Low energy density regime)

In the partial melting regime, the incident laser energy density is larger than the threshold energy of melting of a-Si films the applied laser energy density can cause only surface melting of a-Si thin films but not the entire silicon films (i.e., melting deptn < film thickness). Therefore, a-Si thin film can be partially melted and subsequently be recrystallized from the underlying continuous layer of remained solid Si. In this regime, the poly-Si grain size increases with the increases of the laser energy density. In addition, it is characterized that explosive crystallization of a-Si thin film occurs at the onset of the transformation and follows by vertical grain growth, and competitive occlusion of grains [1.47]. The early trigger of explosive crystallization may be attributed to the presence of microcrystalline clusters or to the

presence of impurities in the silicon films.

Complete-melting regime (High energy density regime)

In the complete melting regime, the incident laser energy density is sufficient high to cause the complete melting of the entire a-Si thin films. Since the glass substrate is amorphous structure, epitaxial layer growth from the substrate is not possible. For the complete-melting Si thin film, a deep suercooling of the liquid silicon film leads to homogeneous nucleation before the transformation of poly-Si in solid phase [1.48]-[1.49]. In this regime, the final microstructure is insensitive to the applied laser energy densities. Fine-grained and small-grained poly-Si thin films are attained due to the low substrate temperature. In addition, a phenomenon of amorphization is observed in thinner silicon films [1.50].

Near-complete-melting regime (Super-lateral-growth regime)

In the near-complete-melting regime, the incident laser energy density leads to a complete melting a-Si thin film consisting of un-melted discrete silicon islands (i.e. melting depth ≈ film thickness). James. S. Im et al. identified the third transformation regime, the end of the low energy density regime and the beginning of the high energy density rgime, in a narrow experimental window [1.45]-[1.46]. In this regime, large-grained poly-Si films with grain sizes many times larger than the film thickness are observed. Since the grain size is much larger than that in the other two transformation regimes, Im named it super lateral growth (SLG) regime due to its unique nature [1.46]. based on Im's model, it is argued that the un-melted portion of the under lying Si no longer forms a continuous layer but instead consists of discrete solid silicon islands which are separated by small local regions in the completely melting silicon film. The un-melted silicon islands act as nucleation seeds and lateral

grain growth can proceed toward the complete melting region. Therefore, a significant lateral growth takes place before the impingement of the grain grown from the other side depending on the separation distance between these seeds. There is a limit for the maximum lateral growth distance; however, since the continuous cooling of the liquid layer via thermal conduction to the underlying substrate eventually would leads to copious nucleation of solids in bulk liquid ahead of the interface. According to the SLG model, the super lateral grain growth distance will increase with thicker film thickness, higher substrate temperature, lower thermal conductivity of the substrate, and longer laser pulse duration. In addition, the applied energy density for super lateral growth regime increases with thicker film thickness, shorter laser pulse duration, higher thermal conductivity of the substrate, and lower substrate temperature. It is concluded that the lateral grain growth is resulted from the thermal gradient between the solid and liquid interface and the lateral grain growth distance is determined by the quenching rate of liquid silicon and the residual solid Si seed distance. As a result, the SLG distance can be prolonged by enlarging the lateral thermal gradient and increasing the solidification duration. However, a very non-uniform grain size distribution is observed in the SLG regime due to the fluctuation of pulse-to-pulse laser energy density, non-uniform laser beam profile, and non-uniformity of a-Si thin film thickness. The non-uniform grain distribution causes device degradation and poor device-to-device uniformity as the laser energy density is controlled in the SLG regime. It is very undesirable for device and circuits applications.

1.3 Ion activation

For millions of transistors fully functional working, dopants in the channel,

LDD, and source/drain regions must all be well activated. The energetic dopant ions cause significant damage to the silicon crystal structure near the surface regions during ion doping process. Activation is a thermal heating process to repair the lattice damaged regions into single-crystal structure and to activate the dopants. Only when the dopant atoms are at the single-crystal lattice sites can they provide electrons and holes as the majority carriers for device application. It has been reported that device with thinner active layer displays higher driving current, lower off-state leakage current, reduced kink current, and superior short channel characteristics. However, the high parasitic resistance of the thin source/drain regions degrades device performance such as effective field-effect mobility and driving current. In ULSI silicon semiconductor processing, activation is performed by either furnace annealing or rapid thermal processing (RTP) at temperature above 900℃. However, the maximum fabrication process temperature of LTPS TFTs is restricted to the softening point of glass substrate (~ 600℃). Activation poses a considerable challenge to LTPS TFTs producers owing to the temperature limitations. Because of the temperature restriction and the thin active layer, the high series resistance from source/drain regions will degrade device performance. In order to achieve low sheet resistance, the dopants in the source and drain regions must be activated to a high degree. The efficiency of the activation is dependent upon the doped impurities, activation temperatures and activation duration. Basically, activation methods used in LTPS TFT technology include furnace annealing, rapid thermal annealing, and laser annealing.

The most common approach of dopant activation is furnace annealing. This process is typically carried out at 600℃ for as long as tens of hours in nitrogen ambient. The long process time at low temperature is necessary in order to effectively activate the dopants while preventing the substrate free from warpage or damage. It is a technique of poor efficiency and low throughput for mass production.

Another concern for furnace annealing is the high thermal budget. The long-time furnace annealing process will cause severe dopant lateral diffusion which is intolerable for small geometrical transistors. Therefore, rapid thermal annealing (RTA) process is preferred for post-implantation annealing in the advanced fab. A RTA system can ramp up the temperature from room temperature to 900℃ in a very short time, typically within 10 seconds. The RTA process can precisely control temperature uniformity of the substrate and within substrate. At about 750℃, the single-crystal structure can be recovered and the dopant atoms will move to locate substitutional sites in about 1 second, with minimum lateral dopant diffusion. By processing at high temperatures while minimizing substrate damage, short process times, lower cost and high throughput can be achieved via RTA.

Since RTA method will also cause deformation of the glass substrate, laser annealing is the best candidate for dopant activation without substrate damage. Laser annealing process, the silicon is heated, melted and re-crystallized without heating the substrate, can achieve the highest activation efficiency compared to the other methods. Despite the high efficiency, some damages to device may occur during laser irradiation, such as the gate metal damage. In addition, throughput may be another potential bottleneck to the mass production.

1.4 Motivation

The low temperature polycrystalline silicon (LTPS) thin film transistors (TFTs) have been widely applied to high-definition active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting displays (AMOLEDs). The quality of the polycrystalline silicon thin film acts as the active layer of the devices plays an important role in the device to influence the electric characteristics greatly. In

order to fabricate a high performance LTPS TFTs, we introduce several aspects to improve the electrical characteristics of the LTPS TFTs: to reduce the defects of polycrystalline silicon thin, to raise the gate ability, and suppress the leakage current. The defects in the inter-grain will make the electrical characteristics of the device low, as reduce the carrier mobility and raise the leakage current of the device. In addition, the interface between the gate insulator and the active layer will influence the gate control ability. Form the views of reducing the defect of the polycrystalline silicon thin film, we introduced a simple method to fabricate the high quality polycrystalline silicon thin film, which is so called recessed-channel with oxide step structure. We also propose the multi-gate structure to enhance the gate control ability.

1.4.1 Fabrication of Polycrystalline Silicon Thin Film with Location-Controlled Grain Boundary Technology

Among the various crystallization technologies for preparing polycrystalline silicon thin films, excimer laser crystallization (ELC) is the most promising technology to produce high quality polycrystalline silicon thin films on forein substrates at low temperature. Although pulsed excimer laser crystallization had the potential to improve the crystallinity of polycrystalline silicon thin films, narrow excimer laser crystallization process window, the uniformity and serious roughness of the crystallized polycrystalline silicon thin films were important issues. The excimer laser energy should be kept at a certain threshold value to make the amorphous silicon thin films which without laser irradiation is nearly completely melted, which is so called "super lateral growth" (SLG) regime; that is, excimer laser crystallization suffer narrow process window. In addition, the shot-to-shot laser energy of excimer laser crystallization is not stable enough and the seeds of crystallization distribute

randomly during laser re-crystallization. The excimer laser crystallization come out to a poor device-to-device uniformity.

For the purpose of the issues mentioned above, many laser crystallization technologies have been proposed to produce large grains with uniformly grain size distribution, including sequential lateral solidification (SLS) [1.51]-[1.52], grain filters method [1.53], capping the reflective or anti-reflective layer [1.54], phase-modulated ELC [1.55], dual beam ELA [1.56], double-pulsed laser annealing [1.57]-[1.58], selectively floating a-Si active layer [1.59], continuous-wave laser lateral crystallization [1.60]-[1.61], selectively enlarging laser crystallization [1.62]-[1.63], and so on. However, these methods are not compatible with the existing excimer laser annealing system or need complex process flows. Therefore, a simple method to control the direction of grain growth and the location of grain boundary has been developed in the thesis, which is called "Recessed-Channel with Oxide Step Method". In this method, we can artificially control the thermal gradient in selective region, which is the step region and valley region, formed by pre-pattern buffer oxide step structure. The amorphous silicon thin film at the corner of oxide step region is thicker than elsewhere of the other region. If the laser energy density is controlled to completely melt the thinner region and partially melt the thicker region, a lateral thermal gradient will determine the grain growth from the un-melting solid phase seeds towards the melting liquid phase region. For the whole thesis, the crystallization is based on the structure.

1.4.2 Polycrystalline Silicon Thin Film Transistors with Multi-Gate Structure by Recessed-Channel with

Oxide Step Process

It has been demonstrated that the performance of devices can be enhanced with multi gate structure. Many kinds of gate structure, including double gates, dual-gates, tri-gate, Ω-gate, T-gate, and surrounding gate…etc. [1.64]-[1.68], are concentrated on the extension of the field induced device channel region. We could obtain better gate control ability and steeper Subthreshold swing than that of conventional single top gate structure. Among the gate structures mentioned above, the multi gate structure is adopted in this due to the compatibility with the location-controlled technology we propose. At first, we fabricate the polycrystalline silicon thin film by Recessed-Channel with Oxide Step method. There is a single grain boundary located in device channel region. After that, we use multi gate method to reduce the influence of main grain boundary.

1.5 Thesis Organization

In chapter 1, an overview of LTPS TFTs technology was given. The polycrystalline silicon crystallization process and ion activation process were brief explain. The motivations of this thesis were explained to introduce this thesis subsequently.

In chapter 2, experimental processes of elevated channel thin films were introduced. The mechanism of lateral growth of thin films fabricated by Recessed-Channel with Oxide Step method was proposed by material analysis. The material properties were analyzed by scanning electron microscope (SEM) and atomic force microscope (AFM). Then experimental procedures of polycrystalline silicon thin-film transistors fabricated by Recessed-Channel with Oxide Step structure were introduced. The electrical characteristics, including the field-effect mobility, the

subthreshold swing, and the threshold voltage were investigated by using Agilent 4156 system.

In Chapter 3. With a view to reduce the influence of main grain boundary located in device channel region, the MG-TFTs were fabricated by Recessed-Channel with Oxide Step method. The process flows and the grain boundary influence would be discussed in detail. The electrical characteristics of MG-TFTs, including the field-effect mobility, the subthreshold swing, the threshold voltage, and the uniformity were investigated.

Finally, conclusions were given in chapter 4.

Chapter 2
Fabrication of Location-Controlled Single-Grain-Boundary (SGB) Polycrystalline Silicon (Poly-Si) Thin Film Transistors (TFTs) by Recessed-Channel with Oxide Step Methods Using Excimer Laser Annealing (ELA)

2.1 Introduction

2.1.1 Introduction to Recessed-Channel with Oxide Step Methods

Recently, Low-temperature Polycrystalline Silicon (LTPS) technology has been the most promising method to fabricate the high performance thin-film transistors (TFTs). High driving-current capacity, low leakage-current, and good uniformity are the characteristics of TFTs and those are imperative for devices aiming at the

application of AMLCD, AMOLED, and 3-dimensional ICs [2.1]-[2.6]. In comparison with amorphous silicon (a-Si) TFTs, the electric characteristics of polycrystalline silicon (poly-Si) TFTs is better than that of a-Si TFTs. Higher driving-current of LTPS TFTs due to the mobility of poly-Si TFTs was generally much higher than that of a-Si TFTs. The high driving-current make LTPS TFTs to act as pixel switching devices which are very small in size. In addition, LTPS TFTs are compatible with complementary metal-oxide-semiconductor (CMOS) circuits and allow the low-power accessional driver circuitry to be integrated within the active matrix circuit on a single substrate for the goal of system on panel (SOP), due to the better reliability and low power consumption of LTPS TFTs. As comparison with high temperature polycrystalline silicon (HTPS) TFTs, the LTPS TFTs technology was compatible with glass substrate even plastic substrate because the thermal budget was much lower for HTPS TFTs, and the cost of LTPS TFTs technology is much lower than that of HTPS TFTs in large panel application.

For preparing the LTPS thin films, several ways have been reported to date, including solid phase crystallization (SPC), metal induced lateral crystallization (MILC), and laser annealing [2.7]-[2.10]. The excimer laser annealing (ELA) method was most commendable to prepare the high quality of LTPS thin films. The excimer laser emits in UV light region with short pulse duration (10-30ns) by the laser source of ArF, KrF, or XeCl (output wavelengths 193, 248, and 308nm, respectively) gas source. The strong optical absorption of UV light and small diffusion length during the laser pulse in silicon imply that high temperature can be produced and cause melting of silicon without significant damage of glass substrates [2.11]. Besides, ELA poly-Si films have good crystallinity and few intra-grain defects due to the melt-regrowth process. The mechanism of grain growth during ELA process is quite sensitive to the laser energy density. Fig. 2-1 schematically illustrates the grain growth

corresponding to the different laser energy densities. As shown in Fig. 2-1 (a), if the laser energy is controlled to melt the part thickness of a-Si thin film, vertical solidification occurs and the un-melted solid layer remains to be a-Si, while the melted Si layer transforms into poly-Si with small grain size [2.12]. Refer to Fig. 2-1 (b), if the laser energy density is high enough to completely melt the a-Si thin film, homogeneous nucleation occurs for deep supercooling to form small grain size [2.13]. Only when the laser energy density is controlled around a certain threshold value that leads to larger grain size, it is as large as 1 μm in diameter, as shown in Fig. 2-1 (c). This is so called *Super Lateral Growth* (SLG) regime [2.14], which illustrates the behavior of melted a-Si to recrystallize from very few un-melted a-Si residues to each other. The very few residues act as the grain growth seeds, the lateral growth phenomenon causes large grain size.

The LTPS thin film fabricated by ELA technology showed good crystallinity with very few intra-grain defects and large grain. But the conventional ELA LTPS TFTs have some failings. The high surface roughness between active layer and gate insulator is due to the ridges formation between grain boundaries. Besides, the location of grain boundaries cannot be controlled due to the random position of nucleation by excimer laser crystallization, and many small grains still spread between these large grains in the super lateral growth (SLG) regime. A lot of process fluctuation factors exist, i.e., the pulse-to-pulse variation of excimer laser energy, the variation of a-Si film thickness, and the narrow process window with ELA process.

Many crystallization methods have been proposed to solve the above problems. They includes sequential lateral solidification (SLS) [2.15]-[2.22], grain-filters (or substrate-embedded seeds) method [2.23]-[2.25], phase-modulated ELC using an optical phase-shift mask [2.26]-[2.30], capping reflective or anti-reflective layer [2.31]-[2.36], ELC of selectively floating a-Si thin film [2.37]-[2.41], ELC of

pre-patterned a-Si thin film [2.42]-[2.45], dual beam ELA [2.46], and so on. Although all of them provided alternatives to produce large grain poly-Si thin films, however, most of them were not a simple solution for the fabrication of LTPS TFTs.

A novel and simple crystallization method to control lateral grain growth in the desired region was using excimer laser irradiation, called Recessed-Channel method. Fig. 2-2 schematically illustrates the grain growth regime of the Recessed-Channel structure. In this method, a-Si thin film with two kinds of thicknesses in a local region was utilized for excimer laser irradiation. As a proper laser energy density was applied on the a-Si thin film, in which the thin part of a-Si was completely melted, a large lateral thermal gradient would exist between the complete melting silicon and partial melting silicon, and the grains would grow laterally from the un-melting solid silicon seeds in the thick part of a-Si towards the thin region where the silicon was completely melted. As a result, large and uniform longitudinal grains could be artificially produced in the desired local region.

As the principle of crystallization was applied to the fabrication of low temperature polycrystalline silicon thin film transistors, the thick part of a-Si was always served as the source/drain region, while the thin part of a-Si was served as the channel region, as shown in Fig. 2-3. Therefore, the large and uniform longitudinal grains could be formed in the channel region.

Although the poly-Si thin film with recessed-channel structure method had been successfully used to fabricate the large grain with high quality poly-Si thin film and the high performance ELA poly-Si TFTs, the location-controlled lateral growth grains would be obtained in the thin part of the ELA poly-Si thin film with Recessed-Channel method and the channel region of the device were in-situ designed in the thin part of the poly-Si thin film only. There were many small grains in the thick part of the poly-Si thin film with Recessed-Channel method due to the thick part

of the amorphous silicon could not be full-melted during the excimer laser irradiation. The poly-Si TFTs would have poor electrical characteristics due to the small grains if the channel region of the TFTs was designed in the thick part of the ELA poly-Si thin film with Recessed-Channel structure. In order to obtain high performance poly-Si TFTs, the channel region of the TFTs must be designed to avoid the thick part of the ELA poly-Si thin film with the Recessed-Channel structure.

A novel method was carried out to improve the electrical characteristics of the ELA poly-Si thin film transistors with Recessed-Channel structure, namely Recessed-Channel with Oxide Step method. In this method, the buffer oxide thin film was patterned like the Recessed-Channel structure by excimer laser irradiation. According to the crystallization mechanism of excimer laser irradiation, we expected that the thick silicon in the corner of the oxide steps acted as the grain growth seeds during excimer laser irradiation. The grain boundaries with location-controlled distributed not only in the valley region (the thin part of the buffer oxide layer) but also in the step region (the thick part of the buffer oxide layer), and the uniformity of the devices will be improved. The drawback of the ELA poly-Si thin film with Recessed-Channel method can be excluded. Moreover, we obtained much larger process window rather than that of conventional whole flat thin film by ELA process.

Comparing with the Recessed-Channel method, the poly-Si thin film fabricated by Recessed-Channel with Oxide Step method will not need more than one additional amorphous silicon thin film deposition. The buffer oxide layer is formed as Recessed-Channel structure directly. The cost of the fabrication of the ELA poly-Si thin film fabricated by Recessed-Channel with Oxide Step method will be lower than that of Recessed-Channel method. Fig. 2-4 shows the diagrams of the Recessed-Channel method and the Recessed-Channel with Oxide Step method.

In this chapter, the experimental procedures of Recessed-Channel with Oxide

Step Process would be introduced. We studied the mechanism of lateral growth of Recessed-Channel with Oxide Step Process by material analysis equipments. The material properties of elevated channel thin films were investigated by scanning electron microscope (SEM) and atomic force microscope (AFM)..

2.2 Material Analysis of Location-Control Single Grain Boundary Polycrystalline Thin Films Fabricated by Recessed-Channel with Oxide Step Method

2.2.1 Process Flows for Material Analyses of Location-Controlled SGB Poly-Si Thin Film by Recessed-Channel with Oxide Step Method

Detailed process flow of preparing samples was shown in Fig. 2-5. At first, a thermal oxide layer with thickness of 10000Å were deposited as buffer oxide layer by atmospheric pressure chemical vapor deposition (APCVD) at 980℃. Then, the buffer oxide layer was defined as period step with thickness of 1000Å by TEL5000-RIE. Next, a 1000 Å amorphous silicon thin film was deposited as the active layer by low pressure chemical vapor deposition (LPCVD) at 550℃ with SiH_4 as gas source. The Recessed-Channel with Oxide Step method was named as the first buffer oxide layer was pattern before buffer oxide layer deposited. Laser crystallization was performed using KrF excimer laser (λ = 248nm) in a vacuum chamber pumped down to 10-3 torr. During the laser irradiation, the samples were located on a substrate which is

maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. The grain structure of the crystallized polycrystalline silicon thin film was analyzed using scanning electron microscope (SEM), atomic force microscopy (AFM) and transmission electron microscope (TEM). In order to facilitate the SEM observation, all the samples were processed by secco-etch before SEM analysis.

2.2.2 Material Analysis of Location-Controlled SGB Poly-Si Thin Film by Recessed-Channel with Oxide Step Method

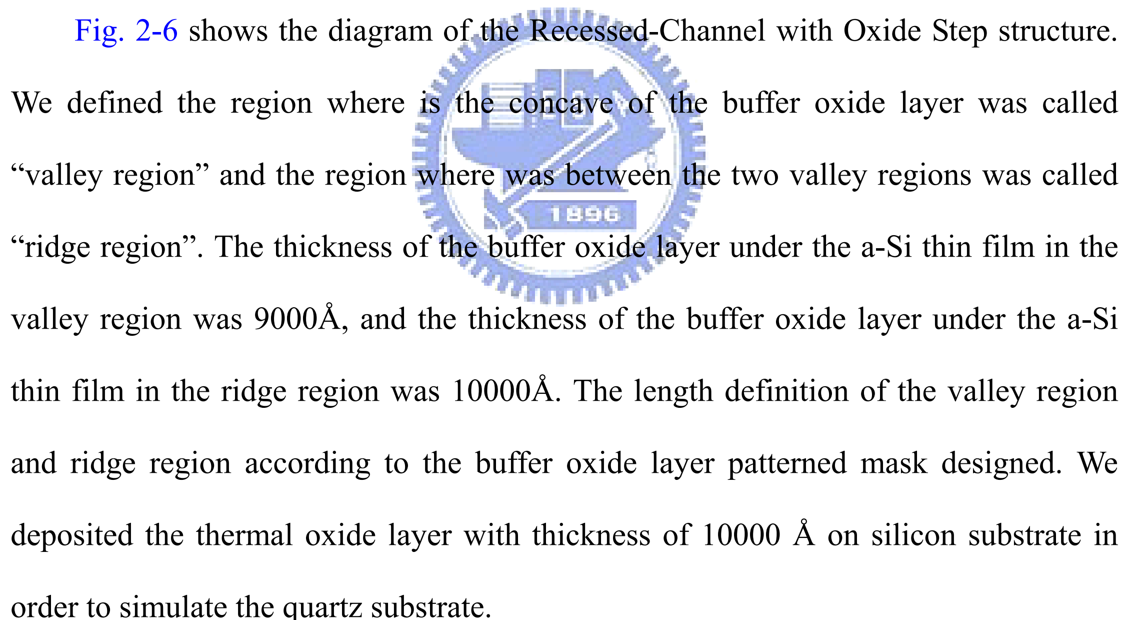


Fig. 2-6 shows the diagram of the Recessed-Channel with Oxide Step structure. We defined the region where is the concave of the buffer oxide layer was called “valley region” and the region where was between the two valley regions was called “ridge region”. The thickness of the buffer oxide layer under the a-Si thin film in the valley region was 9000Å, and the thickness of the buffer oxide layer under the a-Si thin film in the ridge region was 10000Å. The length definition of the valley region and ridge region according to the buffer oxide layer patterned mask designed. We deposited the thermal oxide layer with thickness of 10000 Å on silicon substrate in order to simulate the quartz substrate.

2.2.2.1 Scanning Electron Microscope (SEM) Analysis

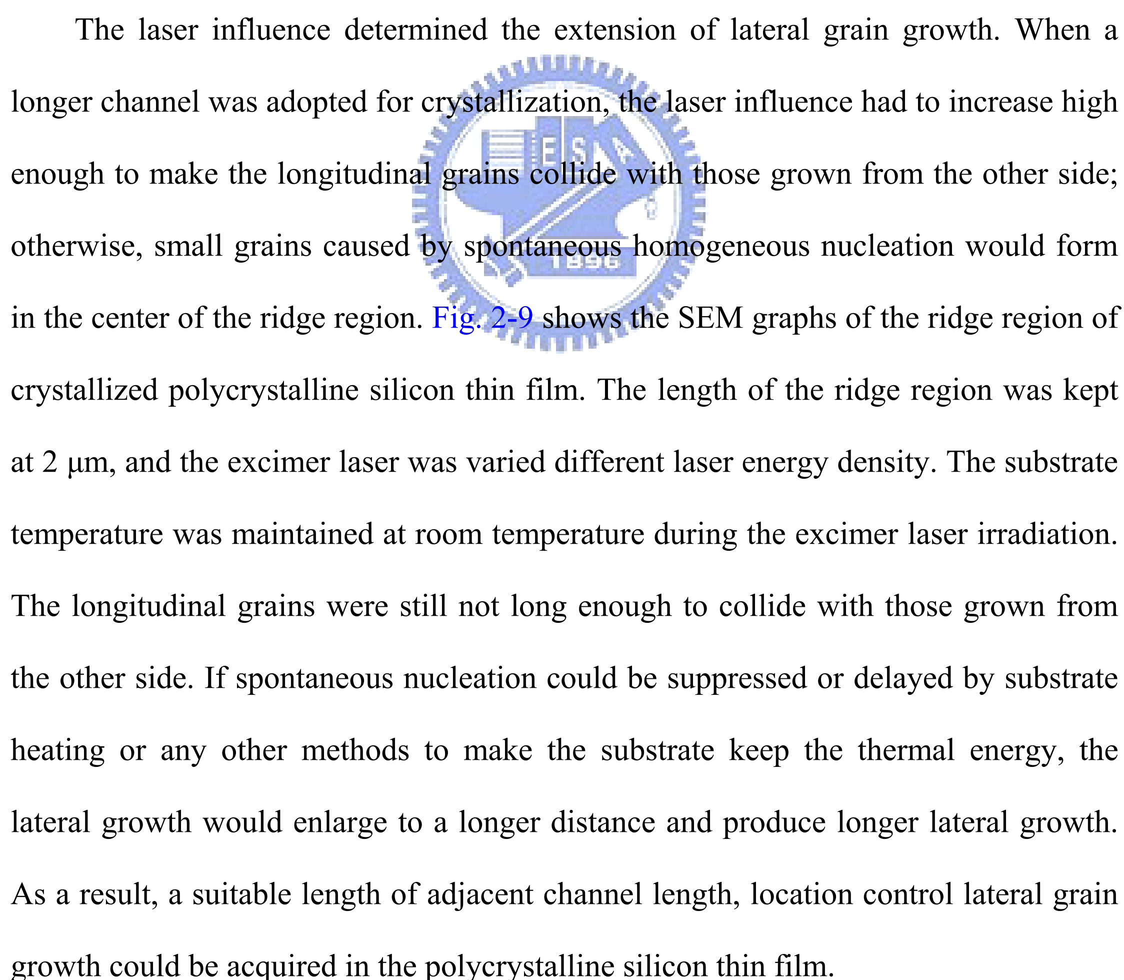
Fig. 2-7 shows SEM graphs of excimer laser crystallized polycrystalline silicon thin film in the thin part of the buffer oxide was 9000Å (valley region) by Recessed-Channel with Oxide Step method. The length between the steps was (a) 1.5µm and (b) 2 µm, respectively. The excimer laser energy was 540 mJ/cm^2 and the

substrate temperature was maintained at room temperature during the excimer laser irradiation. The longitudinal grains with 1 μm were formed in the valley region. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interface [2.47]. When a controlled laser energy density irradiated the amorphous silicon thin film on the buffer oxide layer which containing different thicknesses, the valley region was completely melted while the thick part in the corner due to the poly-Si thin film fabricated by Recessed-Channel with Oxide Step method was only partially melted, leaving behind islands of solid material. As a result, grains would grow laterally towards the complete melting region from the retained solid seeds. The lateral growth would start from the solid amorphous silicon spacer seeds and stretch toward the completely melted region until the solid-melt interface from opposite direction collided. Due to the in-situ design of thin film transistors at the valley region, the grain boundaries perpendicular to the current flow in the valley region could be reduced. Thus the field-effect mobility of polycrystalline silicon TFTs could be greatly improved with this crystallization technique.

Comparison with the valley region of the polycrystalline silicon thin films with Recessed-Channel with Oxide Step method by excimer laser annealing, the surface morphology at the thick part of the buffer oxide layer with the thickness was 10000Å (ridge region) was observation by SEM analysis. Fig. 2-8 shows the SEM graphs of grain morphology of the ridge region of excimer laser crystallized polycrystalline silicon thin film by Recessed-Channel with Oxide Step method. The length of the oxide ridge was (a) 1.5μm and (b) 2μm, respectively. The excimer laser energy was 480 mJ/cm^2 and the substrate temperature was maintained at room temperature during the excimer laser irradiation. The longitudinal grains with 0.75 μm were formed in the ridge region. The amorphous silicon thin film at step region would be completely melted during excimer laser annealing process, and the thick silicon in the corner of

the buffer oxide steps would be partially melted. The silicon thin film at the corner region had more thermal energy than the silicon in the middle of ridge region due to the silicon thin film at the corner region had more vacuum space than the silicon in the middle of ridge region. As a result, grain growth would come up from the residual, un-melted silicon islands in the corner of ridge-valley structure and in the middle of ridge, and then grain growth must toward opposite direction. The grains grown from the corner with step structure and the middle of ridge region toward opposite direction due to the action of the vertical expanded solid material on the remaining (denser) liquid material. When two opposite freezing of capillary waves (maybe two or more grains) met, there was a grain boundary formation.

The laser influence determined the extension of lateral grain growth. When a longer channel was adopted for crystallization, the laser influence had to increase high enough to make the longitudinal grains collide with those grown from the other side; otherwise, small grains caused by spontaneous homogeneous nucleation would form in the center of the ridge region. Fig. 2-9 shows the SEM graphs of the ridge region of crystallized polycrystalline silicon thin film. The length of the ridge region was kept at 2 μm, and the excimer laser was varied different laser energy density. The substrate temperature was maintained at room temperature during the excimer laser irradiation. The longitudinal grains were still not long enough to collide with those grown from the other side. If spontaneous nucleation could be suppressed or delayed by substrate heating or any other methods to make the substrate keep the thermal energy, the lateral growth would enlarge to a longer distance and produce longer lateral growth. As a result, a suitable length of adjacent channel length, location control lateral grain growth could be acquired in the polycrystalline silicon thin film.



With a view to investigate the process window of the valley region fabrication by Recessed-Channel with Oxide Step method, we altered the laser energy density

irradiated on amorphous silicon thin film. Fig. 2-10 shows SEM graphs of the valley region and ridge region of poly-Si thin films with different laser energy densities while the length between the steps was kept at 2 μm. The laser energy density was increased from 520 mJ/cm^2 to 600 mJ/cm^2 and the substrate temperature was maintained at room temperature during the excimer laser irradiation. We concluded that the process window of Recessed-Channel with Oxide Step method is much larger than that of conventional excimer laser annealing on whole flat amorphous silicon thin film.

The grain lateral growth phenomenon happened not only in the valley region but also in the ridge region of the poly-Si thin film by Recessed-Channel with Oxide Step process. Therefore, the crystallinity of the ridge region of poly-Si thin film was determined by laser influence. The laser process window of the ridge region fabrication of poly-Si thin film with Recessed-Channel with Oxide Step process is investigated. Fig. 2-11 shows SEM graphs of the ridge region of poly-Si thin film by Recessed-Channel with Oxide Step process with different excimer laser energy densities. The length of the oxide ridge was 1.5μm and the substrate was maintained at room temperature during excimer laser irradiation. The excimer laser density was increased from 460 mJ/cm^2 to 600 mJ/cm^2. The excimer laser process window of the Recessed-Channel with Oxide Step method is large and easy to control.

2.2.2.2 Atomic Force Microscope (AFM) Analysis

By using AFM analysis the grains could be distinguished apparently due to the hung hillock formation at the grain boundaries. The hillock was resulted from the freezing of capillary waves excited in the melting silicon during excimer laser crystallization [2.48]. Grain boundaries and vertices which typically were the laser to freeze during lateral grain growth, had accumulated silicon due to the action of the

expanded solid material on the remaining (denser) liquid material. When the excimer laser crystallization began, nucleated grains advanced laterally through the denser liquid at first. As the solid regions grew, they filled a larger volume than the melt they consume. Eventually, the remaining liquid extended above the surrounding film. Where two grains met to form a grain boundary, a ridge developed. Where three or more grains met to form a vertex, a hillock might develop. As shown in Fig. 2-12, the length of the valley region was 2 μm and the excimer laser energy density was 600 mJ/cm^2. The longitudinal grains with 1.5μm in length were formed in the excimer laser annealing silicon thin film of valley region. The roughness analysis was carried out at the valley region. The roughness of valley region of the thin film carried out by Recessed-Channel with Oxide Step method was smaller than the whole flat ELA thin films. Fig. 2-13 shows the AFM graph of the ridge region of poly-Si thin film with Recessed-Channel with Oxide Step method. The longitudinal grains with 0.75μm in length were formed in the excimer laser annealing silicon thin film of the ridge region. The roughness analysis at the ridge region was also shown the same smooth with the one of valley region. There were many small grains at the corner was rough due to the excimer laser energy was not full-melting the amorphous silicon where the silicon in the corner was thicker than the other.

2.3 Fabrication and Electrical Characteristics Analysis of Location-Controlled Single-Grain-Boundary (SGB) Polycrystalline Silicon (Poly-Si) Thin-Film Transistors (TFTs) Fabricated by

Recessed-Channel with Oxide Step Method

2.3.1 Process Flow of SGB-TFTs by Recessed-Channel with Oxide Step method

More detailed process flows of device fabrication were shown in Fig. 2-14. At first, the thermal oxide layer with thickness of 10000Å were deposited by atmospheric pressure chemical vapor deposition (APCVD) at 980℃ with hydrogen and oxygen as gas source. Then, the buffer oxide layer was defined as period step by TEL5000-RIE. Next, a 1000 Å amorphous silicon thin film was deposited as the active layer by LPCVD at 550℃ with SiH_4 as gas source. The period step pre-pattern oxide method was named as the first buffer oxide layer and was pattern before amorphous silicon layer deposited. Laser crystallization was performed using KrF excimer laser (λ = 248nm) in a vacuum chamber pumped down to 10^{-3} torr. During the laser irradiation, the samples were located on a substrate which is maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. Next, the active region was defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700℃ followed by in-situ doping phosphorus polycrystalline silicon layer as top gate electrode. The top gate electrode was defined by TCP-RIE, and gate insulator was defined by TEL5000-RIE. Next, a BF_2 ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 50 keV was performed to form source and drain regions. A 4000 Å TEOS oxide layer was then deposited as passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then contact hole opening by TEL5000-RIE and metallization with Aluminum

were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, conventional top-gate ELC polycrystalline silicon TFTs was also fabricated without any location-controlled grain boundary technology.

2.3.2 Electrical Characteristics of SGB-TFTs

It has been demonstrated that large and longitudinal grains could be formed in the channel region by Recessed-Channel with Oxide Step method in section 2.1. The grain structure would have a significant influence on the electrical characteristics of the fabricated TFTs.

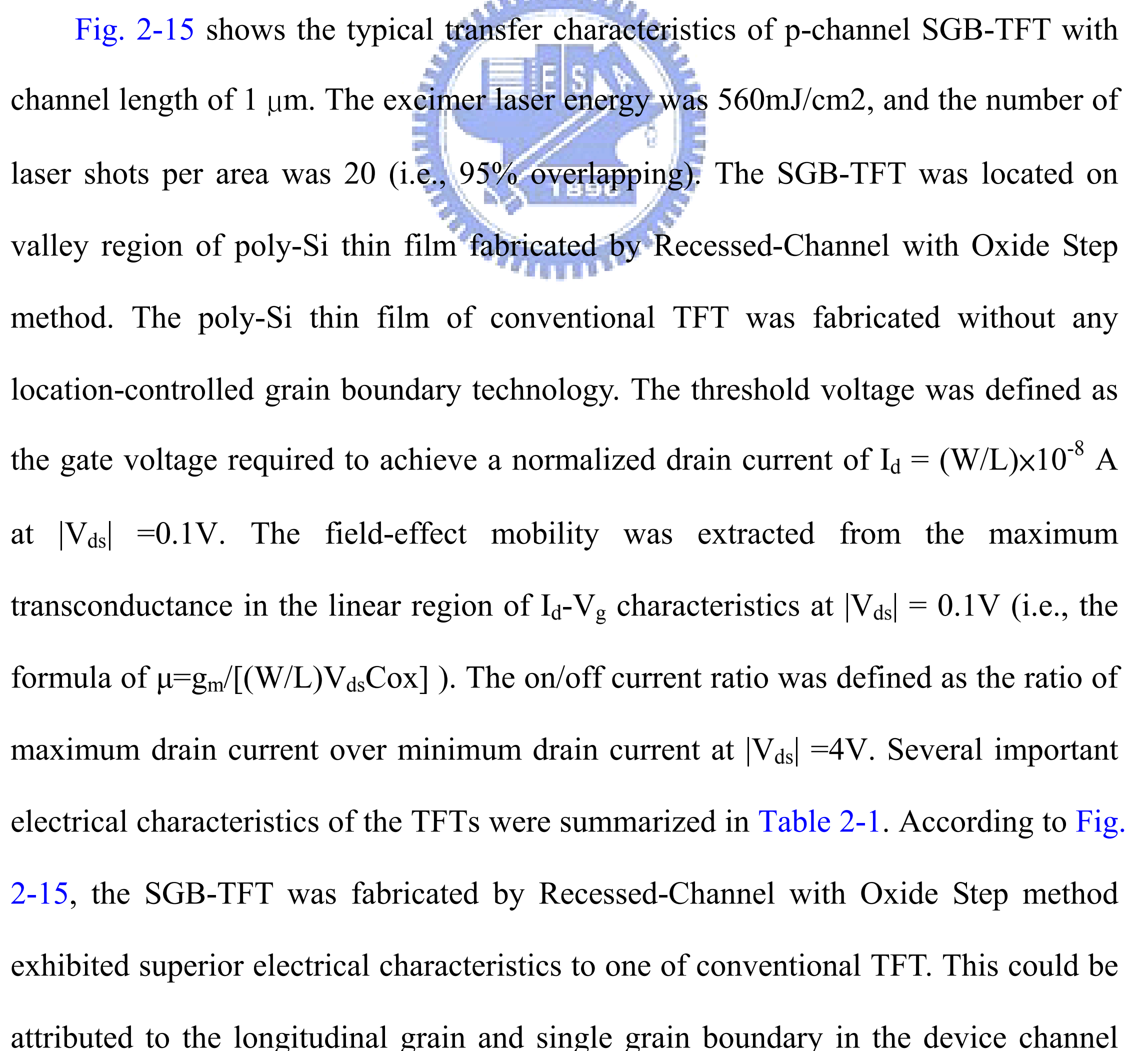


Fig. 2-15 shows the typical transfer characteristics of p-channel SGB-TFT with channel length of 1 μm. The excimer laser energy was 560mJ/cm2, and the number of laser shots per area was 20 (i.e., 95% overlapping). The SGB-TFT was located on valley region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method. The poly-Si thin film of conventional TFT was fabricated without any location-controlled grain boundary technology. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_d = (W/L)\times10^{-8}$ A at $|V_{ds}|$ =0.1V. The field-effect mobility was extracted from the maximum transconductance in the linear region of I_d-V_g characteristics at $|V_{ds}|$ = 0.1V (i.e., the formula of $\mu=g_m/[(W/L)V_{ds}Cox]$). The on/off current ratio was defined as the ratio of maximum drain current over minimum drain current at $|V_{ds}|$ =4V. Several important electrical characteristics of the TFTs were summarized in Table 2-1. According to Fig. 2-15, the SGB-TFT was fabricated by Recessed-Channel with Oxide Step method exhibited superior electrical characteristics to one of conventional TFT. This could be attributed to the longitudinal grain and single grain boundary in the device channel

region. The SGB-TFTs with location-controlled grain boundary structure could reduce the grain boundary influence in device channel region. Take the dimension of W = L = 1 μm and laser shots of 20, SGB-TFTs with field-effect mobility of about 168 cm^2/V-s could be achieved by using Recessed-Channel with Oxide Step method while the mobility of the conventional TFTs was about 61 cm^2/V-s. Besides, the electrical characteristics of subthreshold swing and drain-induced-barrier-lowering (DIBL, which was defined as the difference of threshold voltage between $|V_d|$ =0.1V and $|V_d|$ = 3V). In W = L = 1 μm devices, we obtained subthreshold swing of SGB-TFT about 0.226 V/decade, while that of conventional TFT was about 0.539 V/decade. Similarly, the DIBL of SGB-TFT was 310 mV while the one of conventional TFT was 1000 mV. The DIBL of SGB-TFT was lowered about 690 mV rather than that of conventional TFT. Because the grain boundary influence of device channel region was reduced by Recessed-Channel with Oxide Step method, the SGB-TFTs exhibited superior electrical characteristics than conventional TFTs.

Fig. 2-16 displays the output characteristics of p-channel SGB-TFT. The laser shots were 20 and the laser energy density was 560 mJ/cm^2. It was demonstrated that SGB-TFTs provided about 4.25 times higher driving current than conventional poly-Si TFTs under the same bias condition.

From the observation of SEM graphs in section 2.2, the poly-Si thin film fabricated by Recessed-Channel with Oxide Step method had good uniformity. The longitudinal grain boundaries were located on the ridge region and valley region. Fig. 2-17 and Fig. 2-18 show the typical transfer characteristics and output characteristics of p-channel SGB-TFTs with channel length of 1 μm. The excimer laser energy was 560 mJ/cm2, and the number of laser shots per area was 20 (i.e., 95% overlapping). Several compared electrical characteristics of the propose TFTs were summarized in Table 2-2. The proposed TFTs located on valley region and ridge region were

fabricated by Recessed-Channel with Oxide Step method. The devices located on the valley region had better electrical characteristics than the one located on the ridge region. For example, the field-effect mobility of device located on the valley region was 168 cm^2/V-s while the mobility of the conventional counterpart was about 99 cm^2/V-s. According to Fig. 2-18, the driving current of devices located on the valley region was 2.43 times higher than device located on the ridge region. Many researches were focus on the relation between the field-effect mobility and grain boundary [2.49]-[2.50]. In order to clarify it in a simple way, we demonstrated the grain boundary influence by observing the SEM of poly-Si thin film. Fig. 2-19 and Fig. 2-20 show SEM graphs of the valley region and ridge region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method. There were many small grains located on the center of ridge region, but there was a single grain boundary located on the center of the valley region. During devices located on the ridge region operation, the current flow might meet the grain with small size. The probability of carrier scattering of device located on ridge region was higher than one of device located on valley region, the field-effect mobility of devices located on ridge region would be reduced.

2.4 Summary

In this chapter, we successfully fabricated poly-Si thin-film transistors by Recessed-Channel with Oxide Step method. The material analyses of Recessed-Channel with Oxide Step thin films and the electrical analysis of SGB-TFTs were carried out by SEM, AFM, and Agilent 4156 system.

In the first part, we introduced the location-controlled grain boundary technology of Recessed-Channel with Oxide Step thin films. After that, various efforts were

focused to investigate Recessed-Channel with Oxide Step thin films. From the analysis of SEM and AFM, large longitudinal grains about 1 μm were grown in the valley region and longitudinal grains about 0.75 μm were grown in the ridge region artificially. Furthermore, the lateral grain growth starting from the silicon seeds of corner region could progress until the opposite grain direction impinged and single grain boundary was controlled in the center of the valley region artificially. The device density in per area could arise due to the ridge region also had large grains.

In the second part, high-performance SGB-TFTs with equivalent field-effect mobility approaching 170 $cm^2/V\text{-}s$ for P-type devices had been fabricated with Recessed-Channel with Oxide Step method proposed in the first part. The steeper subthreshold swing is also observed in SGB-TFTs rather than conventional TFTs. Furthermore, the DIBL of SGB-TFTs was lower than conventional ones about 690mV. The conspicuous improvement of driving current (4.25 times higher driving current than conventional TFTs) attributed to good crystallinity of Recessed-Channel with Oxide Step structure was also demonstrated. Finally, the comparison of electrical characteristics of device located on valley region and ridge region was investigated and revealed the devices located on the valley region exhibited fewer grain boundaries than ones located on the ridge region.

During the device on-state operation, the electrical characteristics might be influenced due to the single main grain boundary in device channel region. In order to avoid the main grain boundary influence, the multi-gate structure will be introduced to reduce the main grain boundary influence.

Chapter 3
Investigation of Main Grain Boundary effect of Single Grain Boundary (SGB) Thin Film Transistors (TFTs) by Recessed-Channel with Oxide Step method

3.1 Introduction

Currently, low-temperature polycrystalline silicon (LTPS) technology has been the most promising method to fabricate the high performance thin-film transistors (TFTs). High driving-current capacity, low leakage-current and good uniformity are the characteristics of TFTs and those are imperative for devices aiming at the application of AMLCD, AMOLED, and 3-dimensional ICs. Furthermore, they should be produced with low cost and high throughput. It was desired that the growth of high-quality large grain could be controlled in the device channel region from the viewpoint of device performance and uniformity. In last chapter, a novel process for high quality LTPS thin films for producing high-mobility polycrystalline silicon TFTs was described above. We called this novel method, Recessed-Channel with Oxide

Step method. In this method, a single grain boundary (SGB) LTPS-TFTs was formed. Thus, a longitudinal large-grain polycrystalline silicon thin film was obtained fabricated by Recessed-Channel with Oxide Step method. There is only a longitudinal grain boundary in the center of the device channel.

In this chapter, we would investigate the grain boundary influence of SGB-TFTs. The defects in grain boundary might cause the carrier scattering in device on-state. The electrical characteristics, including field-effect mobility and on-current, might reduce due to the grain boundary influence. The detail of grain boundary influence would be demonstrated. After the ascertainment of grain boundary issue, we proposed the multi gate structure to avoid grain boundary influence of SGB-TFTs fabricated by Recessed-Channel with Oxide Step method.

3.2 The Grain Boundary issue

During the analysis of SEM graphs of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method, we found there was longitudinal grain boundary located in the device channel. Fig. 3-1 shows SEM graph of excimer laser crystallized polycrystalline silicon thin film in the thick part of the buffer oxide (ridge region) fabricated by Recessed-Channel with Oxide Step method. The length between the ridges was 1.5 μm. The excimer laser energy was 600 mJ/cm^2 and the substrate temperature was maintained at room temperature during the excimer laser irradiation. There is a longitudinal grain boundary in the center of ridge region. It is demonstrated that the field-effect mobility was highly sensitive to the grain size. The grain boundary had strong scattering center in poly-Si thin film. When carriers meet at grain boundary, the carriers might be scattered due to the grain boundary influence [3.1]. In order to clarify the grain boundary influence, we investigate the distribution of the

longitudinal grain boundary. From the observation of SEM graph, the longitudinal grain boundary locates in the center of the ridge region. Therefore, the single top gate was in-suit designed locate on the grain boundary, there is the longitudinal grain boundary perpendicular the current flow direction. During the device on-state operation, the current flow will meet the longitudinal grain boundary cause the carriers scattering. When the carriers are scattering during the device on-state, the field-effect mobility will degrade. In other words, device on-current will be reduced due to the reducing of field-effect mobility.

3.3 Solution of Eliminate Main Grain Boundary TFTs fabrication

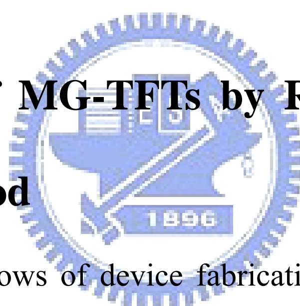
3.3.1 Introduction to Multi-Gate (MG) Polycrystalline Silicon Thin Film Transistors by Recessed-Channel with Oxide Step method

In last chapter, we proposed a novel method to fabricate single grain boundary poly-Si thin film, called Recessed-Channel with Oxide Step method. The poly-Si thin film by Recessed-Channel with Oxide Step method had longitudinal grain boundary in the valley region and ridge region. It had been clarified that the grain boundary influence of SGB-TFTs by Recessed-Channel with Oxide Step method. Therefore, avoid the longitudinal grain boundary in the device channel region might be a solution. A simple method to solve longitudinal grain boundary located in device channel issue is to make the single gate separate into multi-gate structure. With multi-gate structure, the longitudinal grain boundary which was controlled in the channel region of the

device could be avoiding the main grain boundary (the direction was perpendicular to the current flow direction). Without the influence of main grain boundary, the probability of the carriers' scattering and the traps in the grain boundaries will be reduced greatly.

Another advantage of the multi-gate structure was that the lateral electric field would be reduced [3.2]-[3.4]. Because of the field emission and tunneling of carriers through the poly-Si grain traps, when the devices were at the off state, the lateral electric field in the drain depletion region of the poly-Si TFTs could be suppressed and the leakage current could be reduced. Stepper subthreshold slope and a higher on/off ratio would be obtained due to low leakage current.

3.3.2 Process flow of MG-TFTs by Recessed-Channel with Oxide Step method



More detailed process flows of device fabrication were shown in Fig. 3-2. At first, the thermal oxide layer with thickness of 10000 Å were deposited by atmospheric pressure chemical vapor deposition (APCVD) at 980℃ with hydrogen and oxygen as gas source. Then, the buffer oxide layer was defined as period step by TEL5000-RIE. Next, a 1000 Å amorphous silicon thin film was deposited as the active layer by LPCVD at 550℃ with a SiH_4 gas source. The period step pre-patterned oxide method was named as the first buffer oxide layer was patterned before amorphous silicon layer deposited. Laser crystallization was performed using KrF excimer laser (λ = 248 nm) in a vacuum chamber pumped down to 10^{-3} torr. During the laser irradiation, the samples were located on a substrate which is maintained at room temperature. The number of laser shots per area was 20 (i.e., 95% overlapping) and laser energy density was varied. Next, the active region was

defined by TCP-RIE. Then, a 1000 Å TEOS oxide layer was deposited as top gate insulator by LPCVD at 700℃ followed by in-situ doping phosphorus polycrystalline silicon layer as top gate electrode. The top gate electrode was defined by TCP-RIE, and gate insulator was defined by TEL5000-RIE. Next, a BF_2 ion implantation with a dosage of 5×10^{15} cm^{-2} and energy of 50keV was performed to form source and drain regions. A 4000 Å TEOS oxide layer was then deposited as the passivation layer by LPCVD at 700℃ and the implanted dopants were activated by thermal annealing in furnace at 600°C for 9 hours. Then, contact hole opening by TEL5000-RIE and metallization with Aluminum were carried out. Finally, Aluminum sintering was carried out at 400 ℃ to reduce the series resistance. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, conventional top-gate ELC polycrystalline silicon TFTs were also fabricated.

3.3.3 Electrical Characteristics Analysis MG-TFTs by Recessed-Channel with Oxide Step Method

3.3.3.1 Comparison of MG-TFTs and SG-TFTs with/without Location-Controlled Grain Boundary Structure

Fig. 3-3 and Fig. 3-4 show the p-type devices transfer characteristics and output characteristics of the SG-TFTs and MG-TFTs fabricated by Recessed-Channel with Oxide Step method. The equivalent channel length and width were 1μm and laser energy was 560 mJ/cm^2. The number of laser shots was 20 shots (ie. 95% overlapping). The devices were in-suit located above the ridge region. The propose SG-TFT and MG-TFT were single-gate/multi-gate devices fabricated by Recessed-Channel with Oxide Step method. For the comparison of the MG-TFT and SG-TFT, the MG-TFT with location-controlled grain boundary technology exhibited

better electrical characteristics than SG-TFT, including higher driving current, field-effect mobility, and threshold voltage. This might arise from the fact that the longitudinal grain boundary located in the center of device channel region was eliminated due to the multi-gate structure. Using the multi-gate structure, the longitudinal grain boundary was directly doping p-type ion in device fabricated process by ion implantation and the longitudinal grain boundary was the heavy doping region acts as a small series resistance in device channel. The probability of that current flow in device channel met the grain boundary with perpendicular current flow direction might be reduced and the carrier scattering would be reduced too. The mobility and on-current will be improved due to the probability of carrier scattering reducing. Because of the defects in grain boundary were reduced in the device channel, the electrical characteristics, including subthreshold swing and absolute value of threshold voltage of MG-TFT is lower than SG-TFT. Fig. 3-5 and Fig.3-6 show transfer characteristics and output characteristics of the devices fabricated without any location-controlled grain boundary technology and the devices were p-type devices. The equivalent channel was 1μm and laser condition was the same as proposed ones. Form the observation of the graph of output characteristics, the kink effect of SG-TFT was reduced by multi-gate structure. Because of the peak lateral electric field drain region was reduced by multi-gate structure, thus reducing the impaction ionization in the active channel of the MG-TFT causes kink effect reduce. Several important electrical characteristics of the SG-TFT and MG-TFT were summarized in Table 3-1, Table 3-2

For the improvement of location-controlled grain boundary structure, we compare the improvement of electrical characteristics of TFTs with/without location controlled technology while top gate structure changes form single gate structure into multi-gate structure. Fig. 3-7 ~ Fig. 3-10 show the improvements of electrical

characteristics of SG-TFT and MG-TFT with/without location-controlled grain boundary technology, including field-effect mobility, subthreshold swing, threshold voltage, and leakage current. The electrical characteristics, field-effect mobility, subthreshold swing, and threshold voltage of the devices with location-controlled grain boundary technology had more improvement than that without any location-controlled grain boundary technology due to the grain boundary influence is reduced by Recessed-Channel with Oxide Step method and multi-gate structure. The improvement of field-effect mobility of Recessed-Channel with Oxide Step method was about 95.96% while the improvement of mobility of device without any location-controlled grain boundary technology was about 22.06%. In addition, the improvement of subthreshold swing of Recessed-Channel with Oxide Step method was about 64.27% while the improvement of mobility of device without any location-controlled grain boundary technology was about 17.84%. The improvement of subthreshold swing of Recessed-Channel with Oxide Step method indicated that the propose MG-TFT had better gate control ability than conventional MG-TFT. The improvement of leakage current was smaller than one of device without any location-controlled grain boundary technology due to the crystallinity of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method was better one without any location-controlled grain boundary technology. The improvements of electrical characteristics of devices with/without location-controlled grain boundary technology were listed in Table 3-3.

In improvement of location-controlled grain boundary technology, the electrical characteristics of SG-TFTs and MG-TFTs with/without location controlled technology were investigated. Fig. 3-11 ~ Fig. 3-14 show the improvements of electrical characteristics of SG-TFT and MG-TFT with/without location-controlled grain boundary technology, including field-effect mobility, subthreshold swing, threshold

voltage, and leakage current. Because the small grains were reduced by Recessed-Channel with Oxide Step structure, the improvement of field-effect mobility of SG-TFT fabricated by Recessed-Channel with Oxide Step method was about 162.16% while the improvement of mobility of device without any location-controlled grain boundary technology was about 62.3%. The improvement of subthreshold swing of SG-TFT fabricated by Recessed-Channel with Oxide Step method was about 75% while the improvement of mobility of device without any location-controlled grain boundary technology was about 14.84%. The improvements of field-effect mobility and subthreshold swing show the same trends due to the good crystallinity and smooth surface of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method. The improvements of electrical characteristics of devices with/without location-controlled grain boundary technology were listed in Table 3-4.

3.3.3.2 Electrical Characteristics of MG-TFTs by Recessed-Channel with Oxide Step Method

Fig. 3-15 ~ Fig. 3-17 show the typical transfer characteristic of p-channel MG-TFTs with equivalent channel length of 1 μm ~ 3 μm. The excimer laser energy density was 560 mJ/cm^2 and the number of laser shot was 20 (i.e., 95% overlapping). The length of valley region was 3 μm and the length of ridge region was 2μm. The laser process condition was optimized and the conventional MG-TFTs fabricated without any location-controlled grain boundary technology were included for comparison. Several important electrical characteristics of the TFTs were summarized in Table 3-5. According to Fig. 3-15 ~ Fig. 3-17, the MG-TFTs fabricated by Recessed-Channel with Oxide Step method exhibited better electrical characteristics than the conventional TFTs. In the dimension of W = L = 1 μm, the proposed MG-TFTs with field-effect mobility of were about 194 $cm^2/V\text{-}s$ and it could be

achieved by using this Recessed-Channel with Oxide Step method while the mobility of the conventional counterpart was about 73.6 $cm^2/V\text{-}s$. In addition, the subthreshold swing of propose MG-TFTs was about 0.164 V/decade while the subthreshold swing of conventional MG-TFTs was about 0.656 V/decade. The electrical characteristics of suthreshold swing of proposed MG-TFT is better than convention MG-TFT due to the grains in channel region were reduced by Recessed-Channel with Oxide Step method. The gate control ability was arisen due to the low subthreshold swing of the proposed MG-TFTs. The electrical characteristics of the TFTs with device dimension up to W = L = 3 μm were still superior to those of conventional ones. This could also ascribed to the long longitudinal rain growth at the oxide step edge even though many small grains resulted from spontaneous nucleation existed in the channel center as well. In addition to the high performance characteristics, the proposed MG-TFTs exhibit low drain-induced-barrier-lowing (DIBL, which was defined as the difference of threshold voltage between $|V_d|$ =0.1V and $|V_d|$ =3V). The DIBL of proposed MG-TFT was about 380 mV while the DIBL of conventional TFT was 880mV.

Fig. 3-18 ~ Fig. 3-20 display the output characteristics of MG-TFTs using Recessed-Channel with Oxide Step structure with laser shots 20 and laser energy density was 560 mJ/cm^2. It is demonstrated that MG-TFTs fabricated by Recessed-Channel with Oxide Step method provide superior driving current than conventional MG-TFTs under the same bias condition. The driving current of MG-TFTs fabricated by Recessed-Channel with Oxide Step method provide about 6.27 times than conventional MG-TFTs. The high driving current of propose MG-TFTs due to there is no main grain boundary located on the channel region.

3.3.3.3 Uniformity of MG-TFTs by Recessed-Channel with Oxide Step Method

In the previous section the superior performance of MG-TFTs fabricated by Recessed-Channel with Oxide Step method than conventional MG-TFTs without any location-controlled grain boundary technology was highlighted. The uniformity issue of DG-TFTs fabricated by Recessed-Channel with Oxide Step method would be discussed in this section.

Take the dimension of W = L = 1μm and laser shots for example, Fig.3-21 ~ Fig. 3-23 show the comparison of equivalent field-effect mobility, threshold voltage, and subthreshold swing for P-type devices. Twenty TFTs were measured to investigate the device-to-device variation for each dimension, then twenty of which were chosen for the exclusion of unexpected extreme value under statistics. Table 3-6 lists the average and standard deviation of electrical characteristics. For the accuracy to investigate the precise variation from the mean value, we introduced a parameter from statistics which is called coefficient of variance (C.V) and defined by the ratio of standard deviation over mean value in percentage.

Referring to Fig. 3-21 ~ Fig. 3-23, the values of standard deviation of electrical characteristics, including field-effect mobility, threshold voltage, and subthreshold swing of MG-TFTs fabricated by Recessed-Channel with Oxide Step method were smaller than those conventional MG-TFTs without any location-controlled grain boundary technology. When it came to C.V, we obtained about smaller electrical characteristics variation of MG-TFTs fabricated by Recessed-Channel with Oxide Step method than MG-TFTs without any location-controlled grain boundary technology. Therefore, we concluded that high performance MG-TFTs with good uniformity could be achieved easily by Recessed-Channel with Oxide Step method with the laser shot number of 20.

3.4 Summary

In this chapter, the grain boundary issue could be clarified by SEM graphs of the valley region and ridge region in poly-Si thin film fabricated by Recessed-Channel with Oxide Step method. The grain boundary influence can be reduced by introducing the novel multi-gate structure.

The comparisons of electrical characteristics of TFTs with/without location controlled technology were carried out while top gate structure changes form single gate structure into multi-gate structure. The improvement of subthreshold swing of Recessed-Channel with Oxide Step method was about 64.27% while the improvement of mobility of device without any location-controlled grain boundary technology was about 17.84%. The gate controlled ability of proposed MG-TFTs fabricated by Recessed-Channel with Oxide Step method was raised. We also carried out the comparisons of improvements of electrical characteristics of SG-TFTs and MG-TFTs with/without location controlled technology. The improvement of field-effect mobility of SG-TFT fabricated by Recessed-Channel with Oxide Step method was about 162.16% while the improvement of mobility of device without any location-controlled grain boundary technology was about 62.3%. It demonstrated that the crystallinity of propose MG-TFT fabricated by Recessed-Channel with Oxide Step method was better than that of the conventional TFT.

The high performance MG-TFTs with field-effect mobility of 194 cm^2/V-s for p-type devices had been fabricated by Recessed-Channel with Oxide Step method proposed in this chapter. Better electrical characteristics, including subthreshold swing, threshold voltage, and DIBL, and better uniformity were also observed. The standard deviation of mobility was 29 cm^2/V-s, the standard deviation of V_{th} was 0.78 V, and the standard deviation of subthreshold swing was 0.113 V/decade for P-type

devices.

Chapter 4
Conclusions

In this thesis, we have demonstrated the high performance multi-gate polycrystalline silicon thin film transistors fabricated by Recessed-Channel with Oxide Step method with excimer laser annealing. The results and discussions will be summarized in the chapter.

In chapter 2, material analyses were performed to investigate the poly-Si thin films fabricated by Recessed-Channel with Oxide Step method. The location-controlled grain boundary mechanism of Recessed-Channel with Oxide Step method was also explained by two parts at first. In the valley region, the excimer laser energy was controlled to make the thin part of silicon thin film completely melt and the thick part of silicon thin film partially melt, respectively. The grains would grow laterally from un-melt silicon toward the center of valley region. In the ridge region, as the length of ridge region was 2 um, for example, the edge of ridge region stored more thermal energy than the center of the ridge region, and there was silicon nucleation acted as seeds in the meddle of ridge region. The lateral grown grain would be obstructed by small grains in the middle of ridge region. When length of ridge region was decreased to 1.5 um, the phenomenon of grain obstruction would be eliminated. The lateral growth grain starting from un-melt silicon seeds could extend along the opposite direction toward the complete melt silicon region and, therefore,

single grain boundary was controlled in the center of the ridge region and valley region. Furthermore, from the analysis of scanning electron microscope (SEM) and atomic force microscope (AFM), large longitudinal grains were observed to be about 1.5 μm in valley region and about 0.75 μm in ridge region. Besides, poly-Si TFTs were also fabricated using proposed crystallization method and the electrical characteristics of SGB-TFTs were studied. High performance p-type SGB-TFTs with field-effect mobility reaching 168cm^2/V-s had been fabricated. The subtheshold swing and drain-induced-barrier-lowing (DIBL) of SGB-TFTs were 0.226 V/decade and 310 mV, respectively. The performance of SGB-TFTs fabricated by Recessed-Channel with Oxide Step method exhibited better than that of conventional TFTs. Further, the electrical characteristics of devices located on the valley region and ridge region were investigated. While the length of ridge region was 2 μm and the length of valley region was 3 μm, the electrical characteristics of devices located on ridge region were poorer than that of devices located on valley region. The reason could be that the crystallinity of ridge region of poly-Si thin film was more defective that of valley region.

In the chapter 3, we investigated the influence of main grain boundary in device channel. With a view to eliminate main grain boundary influence, we introduce multi-gate structure. The electrical characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method were studied. The improvements of MG-TFTs and SG-TFTs fabricated with/without location-controlled grain boundary technology were compared. Consequently, the improvements of field-effect mobility and subthreshold swing were 95.96% and 60%., respectively High performances MG-TFTs with equivalent field-effect moility exceeding 190cm2/V-s for p-type devices had been fabricated. The subthreshold swing of MG-TFTs fabricated by Recessed-Channel with Oxide Step method reached 0.164 V/decade. The standard

deviation of equivalent field-effect mobility was smaller than 30 $cm^2/V\text{-}s$ and the standard deviation of Vth was smaller than 0.78 V, while that of subthreshold swing was smaller than 0.113 V/decade.

To sum up, the Recessed-Channel with Oxide Step method was an efficient technology to fabricate the high performance TFTs, especially in the short channel devices. Utilizing multi-gate structure, the performance of MG-TFTs fabricated by Recessed-Channel with Oxide Step method could be enhanced, such as superior field-effect mobility, steeper subthreshold swing, superior DIBL, and large driving-current. It is potential for the applications of SOP and 3D-IC.

Table

STRUCTURE (gate length=1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	DIBL (mV)	ON/OFF RATIO @ |Vds|= 4V
Proposed single-gate TFT	-3.97	168	0.226	310	4.64E+08
Con. single-gate TFT	-6.07	61	0.539	1000	1.09E+07

Table 2-1 Measured optimal electrical characteristics of P-type SGB-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping).

STRUCTURE (gate length=1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	DIBL (mV)	ON/OFF RATIO @ |Vds|=4V
Proposed TFT (on valley region)	-3.97	168	0.226	310	4.64E+08
Proposed TFT (on ridge region)	-4.99	99	0.459	560	1.85E+08

Table 2-2 Measured optimal electrical characteristics of P-type SGB-TFTs fabricated by Recessed-Channel with Oxide Step method were located above the valley region and ridge region, respectively. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping).

STRUCTURE (W/L=1um/1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	ON/OFF RATIO @ |Vd|=4V
Proposed MG-TFT (gate number=2, gate length=0.5um)	-2.59	194	0.164	2.58E+08
Proposed SG-TFT (gate number=1, gate length =0.5um)	-4.99	99	0.459	1.85E+08

Table 3-1 Measured optimal electrical characteristics of P-type MG-TFTs and SG-TFTs fabricated by Recessed-Channel with Oxide Step method. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was

20 (ie. 95% overlapping).

STRUCTURE (W/L=1um/1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	ON/OFF RATIO @ |Vd|=4V
Con. MG-TFT (gate number=2, gate length=0.5um)	-5.92	74	0.656	6.79E+06
Con. SG-TFT (gate number=1, gate length =0.5um)	-6.07	61	0.539	1.09E+07

Table 3-2 Measured optimal electrical characteristics of P-type MG-TFTs and SG-TFTs fabricated without any location-controlled grain boundary technology. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping).

STRUCTURE (W/L=1um/1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	OFF-CURRENT (A)
Proposed MG-TFT (gate number=2, gate length=0.5um)	-2.59	194	0.164	-1.07E-10
Proposed SG-TFT (gate number=1, gate length=1um)	-4.99	99	0.459	-2.41E-10
Improvement with location-controlled method	48.1%	95.96%	64.27%	reduce 2.25 times
Con. MG-TFT (gate number=2, gate length=0.5um)	-5.92	74	0.656	-7.42E-10
Con. SG-TFT (gate number=1, gate length=1um)	-6.07	61	0.539	-3.25E-9
Improvement without location-controlled method	2.47%	22.06%	17.84%	reduce 4.38 times

Table 3-3 The improvement of electrical characteristics of devices with/without location-controlled grain boundary.

STRUCTURE (W/L=1um/1um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	OFF-CURRENT (A)
Con. SG-TFT (gate number=1, gate length=1um)	-6.07	61	0.539	-3.25E-9
Proposed SG-TFT (gate number=1, gate length=1um)	-4.99	99	0.459	-2.41E-10
Improvement with location-controlled method	17.79%	62.3%	14.84%	reduce 13.49 times
Con. MG-TFT (gate number=2, gate length=0.5um)	-5.92	74	0.656	-7.42E-10
Proposed MG-TFT (gate number=2, gate length=0.5um)	-2.59	194	0.164	-1.07E-10
Improvement without location-controlled method	56.25%	162.16%	75%	reduce 6.93 times

Table 3-4 The improvement of electrical characteristics of different gate structure devices with/without location-controlled grain boundary.

STRUCTURE (each gate length = 0.5um)	VTH (V)	MOBILITY (cm2/V-s)	SS (V/dec)	DIBL(mV)	ON/OFF RATION @ |Vds|= 4V
Proposed TFT (W/L=1um/1um, gate number=2)	-2.59	194	0.164	380	2.58E+08
Con. TFT (W/L=1um/1um,gate number=2)	-5.92	73.6	0.656	880	6.79E+06
Proposed TFT (W/L=2um/2um, gate number=4)	-3.19	167	0.322	110	2.06E+08

Con. TFT (W/L=2um/2um,gate number=4)	-5.19	74.3	0.534	620	1.96E+07
Proposed TFT (W/L=3um/3um, gate number=6)	-4.27	145	0.343	500	2.16E+08
Con. TFT (W/L=3um/3um,gate number=6)	-7.76	46	0.646	1370	2.74E+06

Table 3-5 Measured optimal electrical characteristics of P-type MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional MG-TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping).

Structure (W/L=1um/1um, gate length=0.5um, gate number = 2)	Mobility (cm2/V-s)		Vth(V)		SS(V/decade)	
	AVG± STDEV	C.V.	AVG± STDEV	C.V.	AVG± STDEV	C.V.
Con. TFT	60.95±34.75	57.01%	-4.23±1.68	39.72%	0.402±0.313	77.86%
Proposed TFT	177±29	16.38%	-3.21±0.78	24.3%	0.202±0.113	55.94%

Table 3-6 Electrical characteristics of twenty measured P-type MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional MG-TFTs. The excimer laser energy density was 560mJ/cm^2 and number of laser shot was 20 (ie. 95% overlapping).

Figure Captures

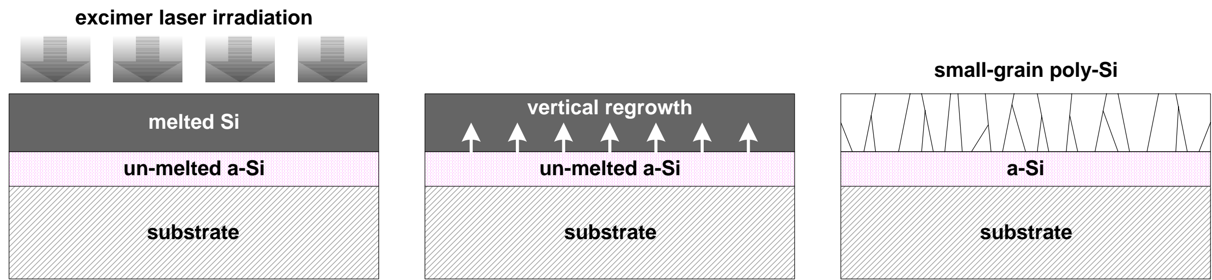


Fig. 2.1 (a) The schematic illustration of the low energy regime corresponding to energy densities that partially melting the a-Si thin film.

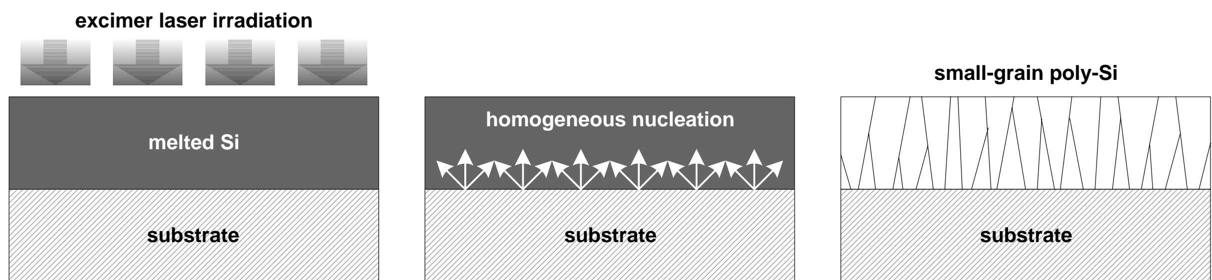


Fig. 2.1 (b) The schematic illustration of the high energy regime corresponding to energy densities that completely melting the a-Si thin film.

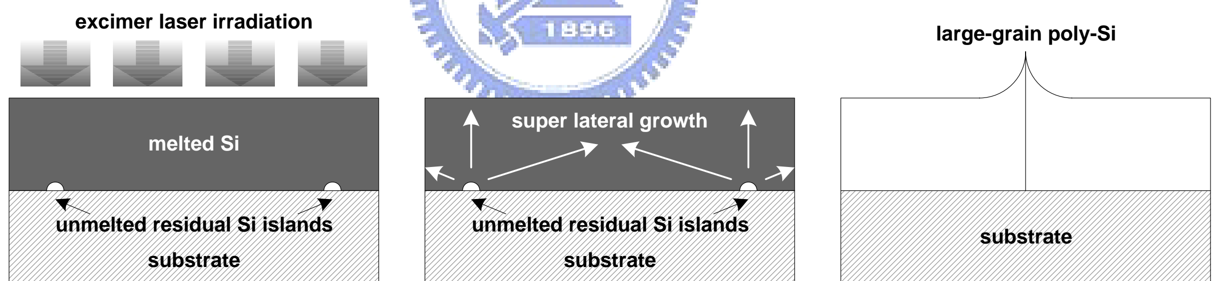


Fig. 2.1 (c) The schematic illustration of the super lateral growth regime corresponding to energy densities that nearly completely melting the a-Si thin film.

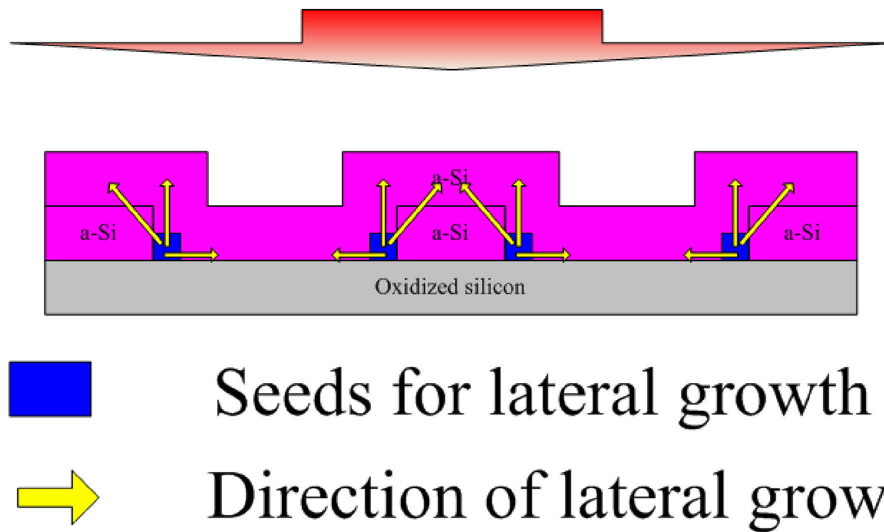


Fig. 2.2 The schematic illustration of the grain growth regime of the Recessed-Channel structure by excimer laser annealing.

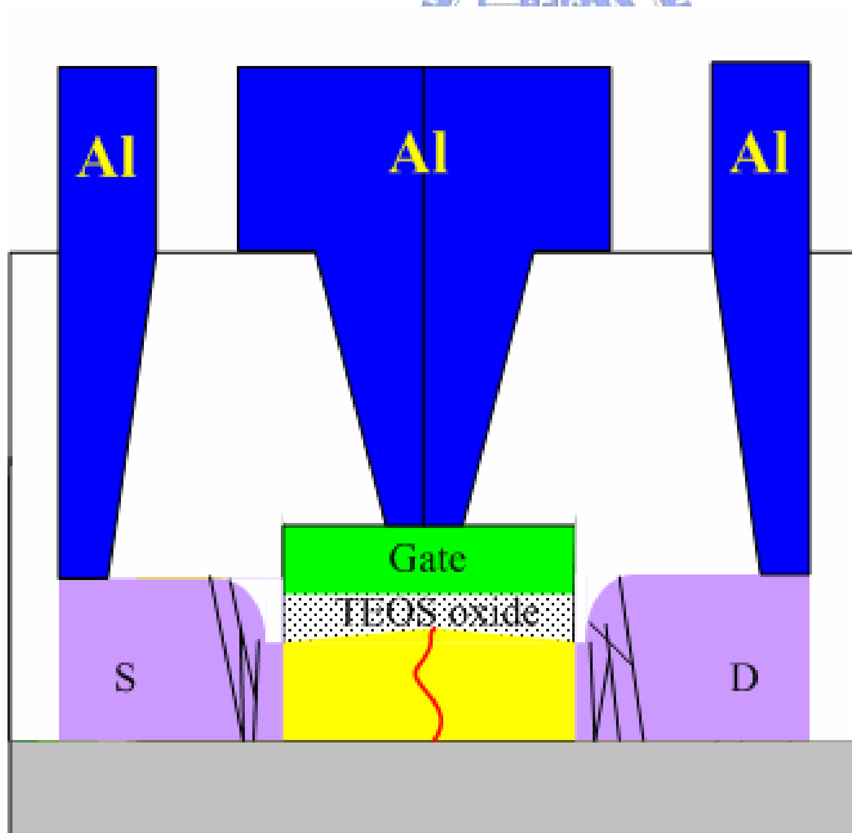
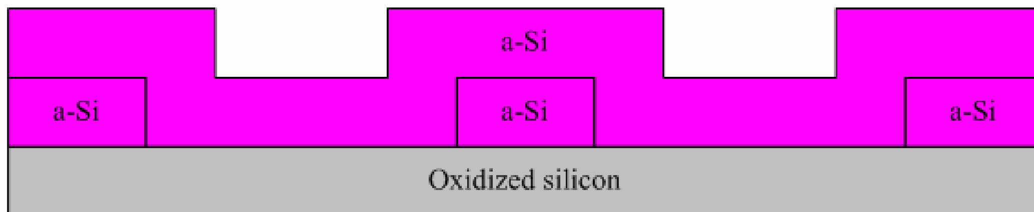


Fig. 2.3 The device diagram with Recessed-Channel method.

Recessed-Channel method



Recessed-Channel with Oxide Step method

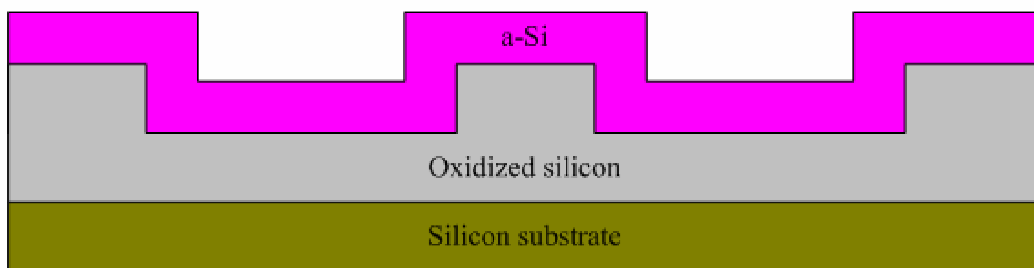


Fig. 2.4 The comparison of Recessed-Channel method and Recessed-Channel with Oxide Step method.

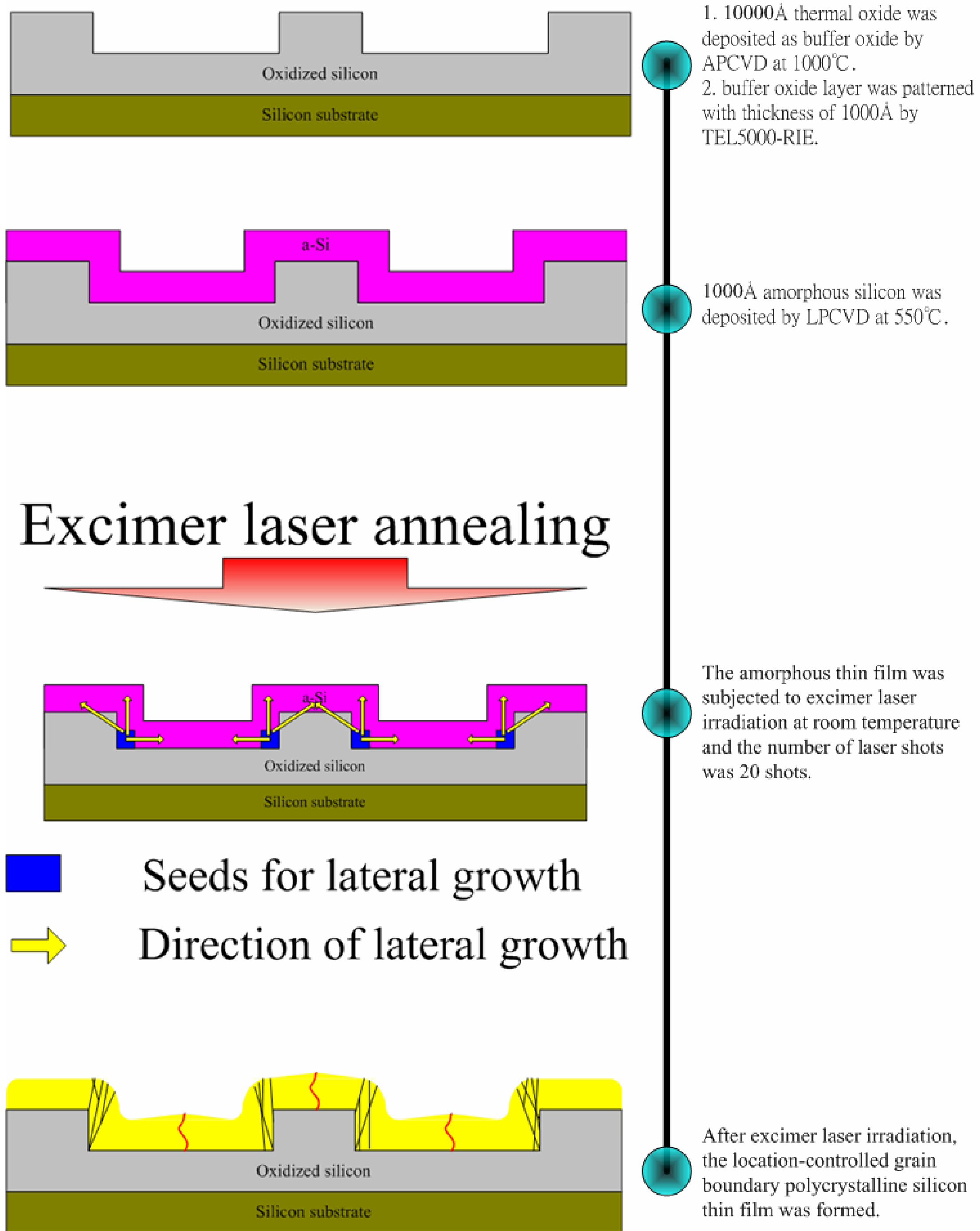


Fig. 2.5 Process flow of preparing samples for material characteristics by Recessed-Channel with Oxide Step method.

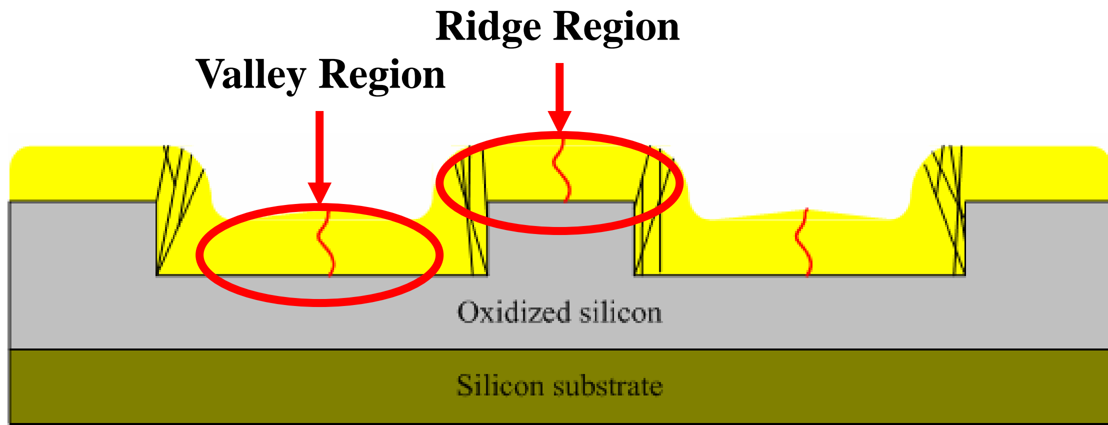
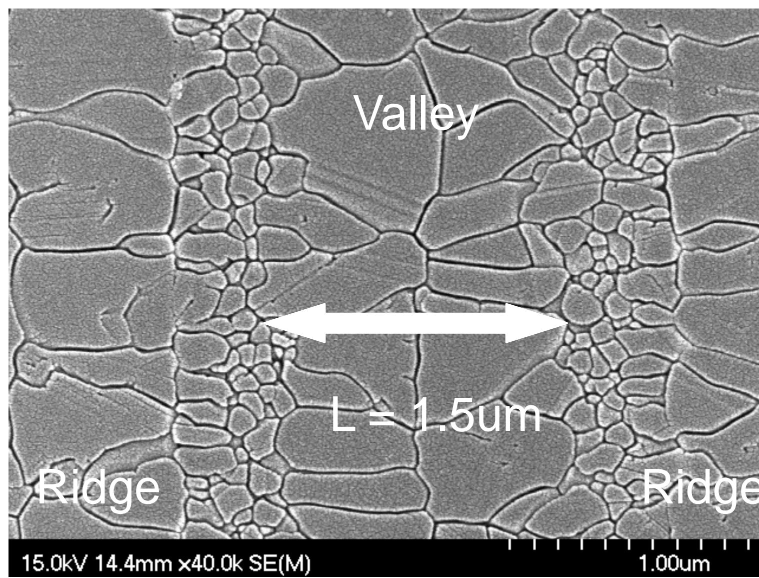
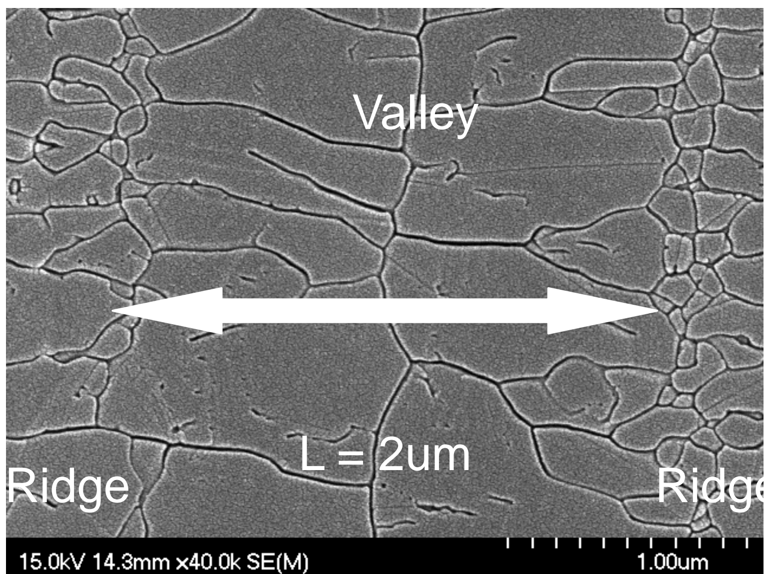


Fig. 2.6 The definition of valley region and the ridge region of the Recessed-Channel with Oxide Step structure.

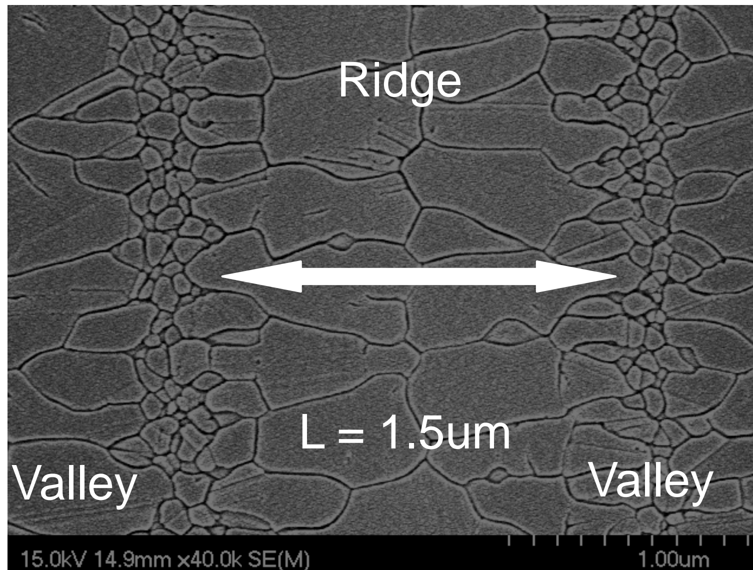


(a)

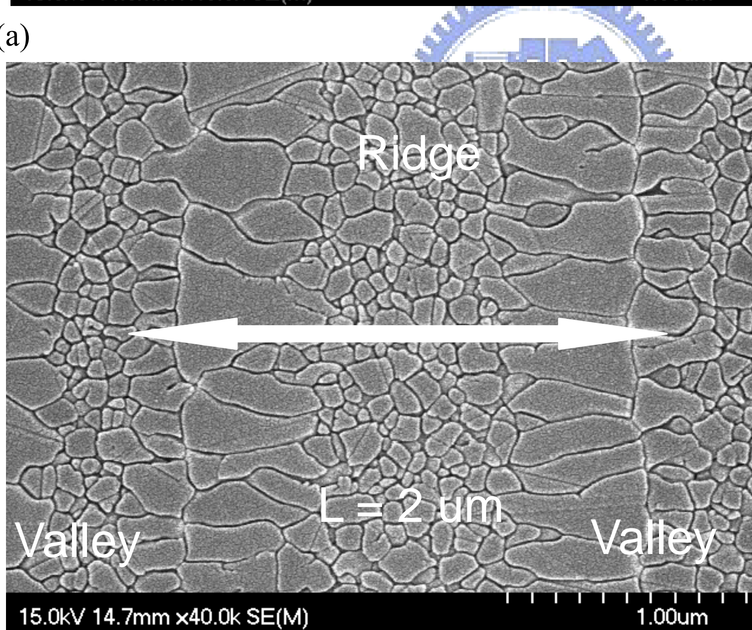


(b)

Fig.2.7 SEM graphs of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the valley region was varied from (a) 1.5μm to (b) 2μm. The excimer laser energy density was 540 mJ/cm^2.

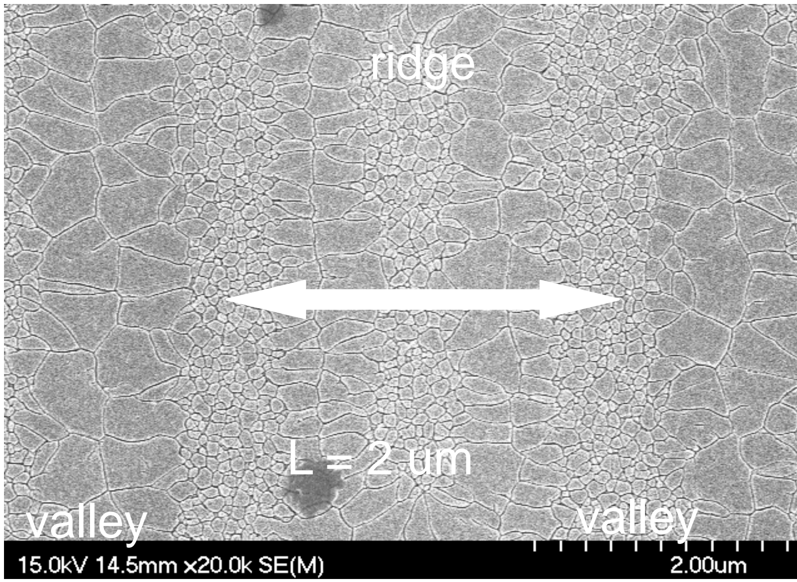


(a)

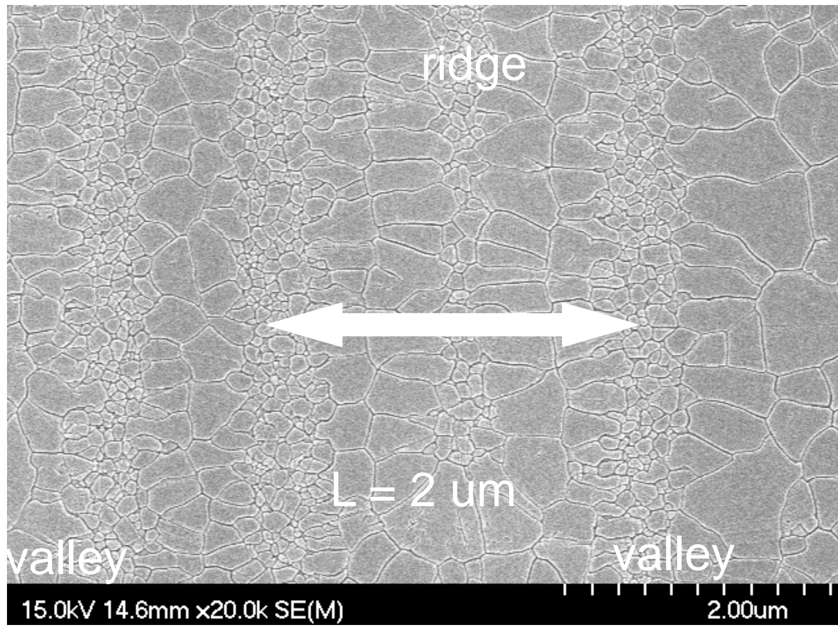


(b)

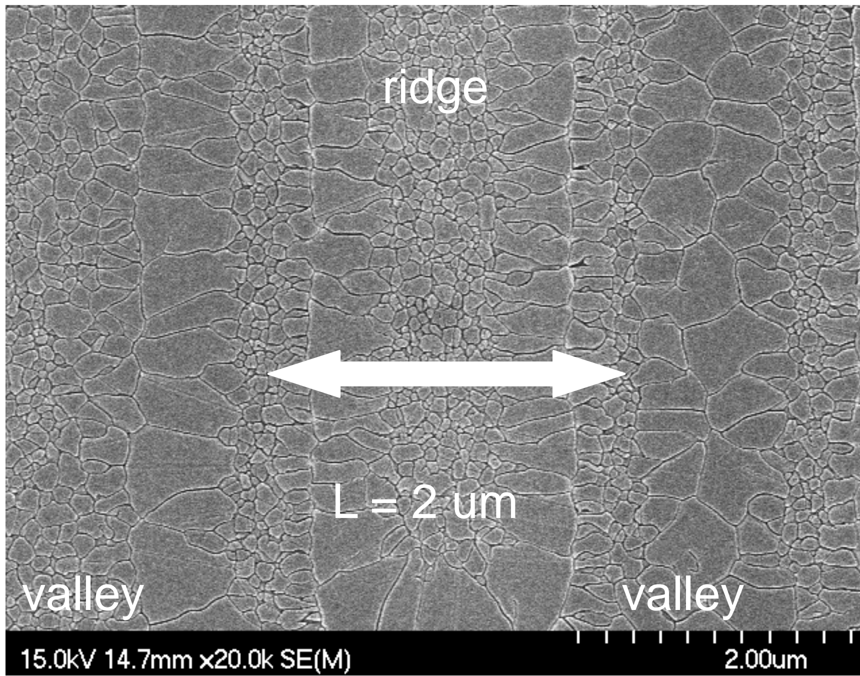
Fig. 2.8 SEM graphs of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the oxide ridge region was varied from (a) 1.5 μm to (b) 2 μm. The excimer laser energy density was 480 mJ/cm^2.



(a)

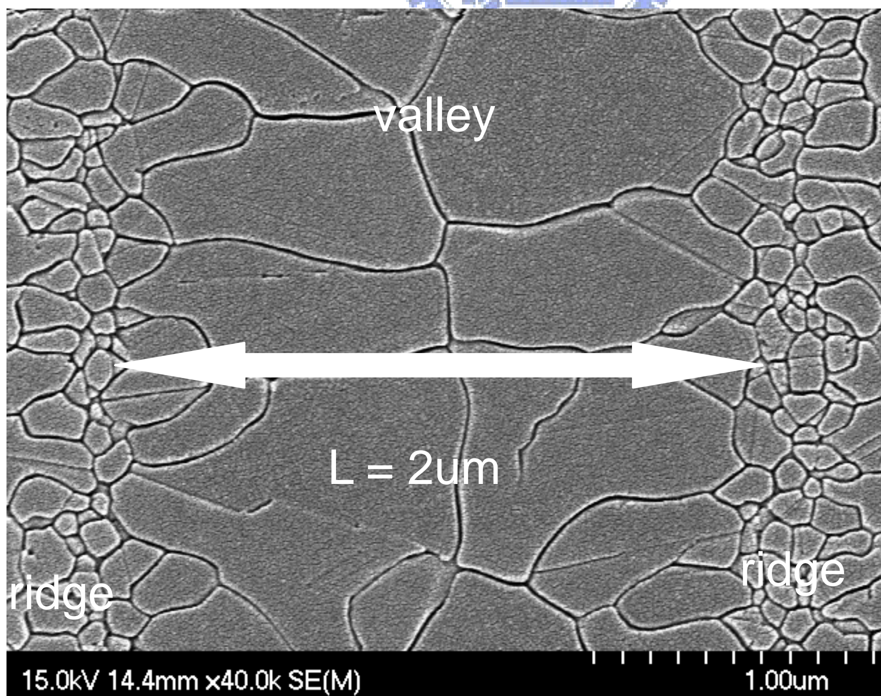


(b)

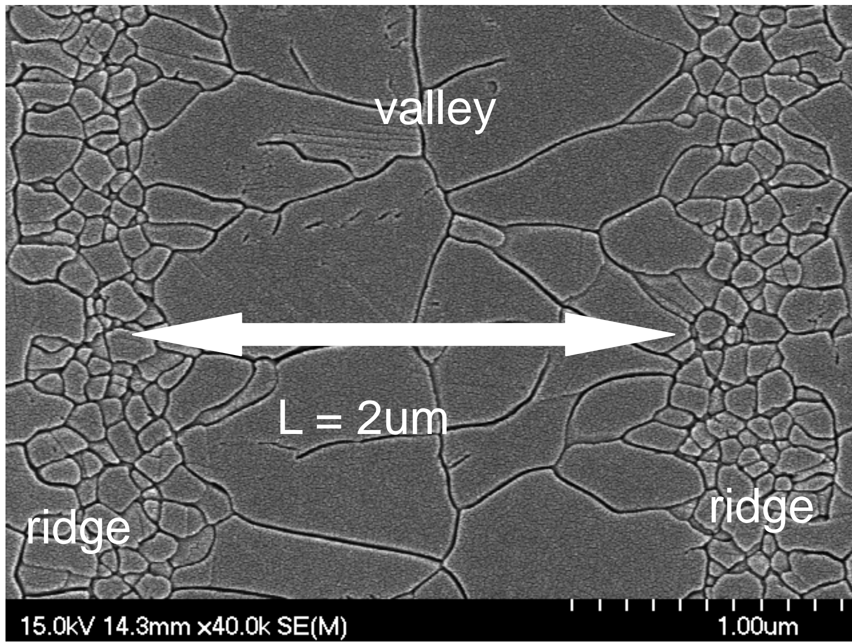


(c)

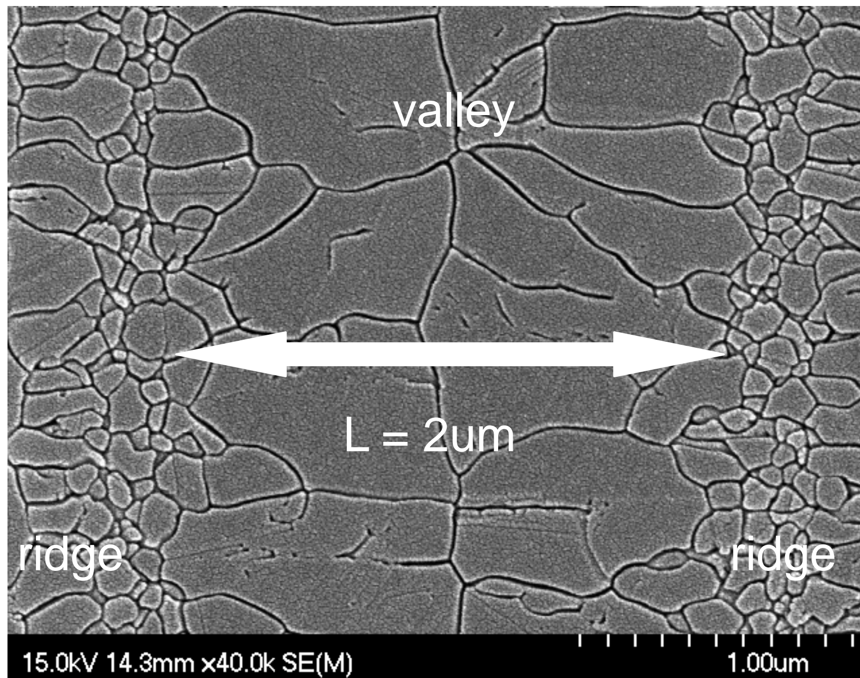
Fig. 2.9 SEM graphs of the ridge region of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of the oxide ridge was 2 μm. The excimer laser energy density was varied (a) 600 mJ/cm^2 (b) 540 mJ/cm^2 (c)480 mJ/cm^2.



(a)

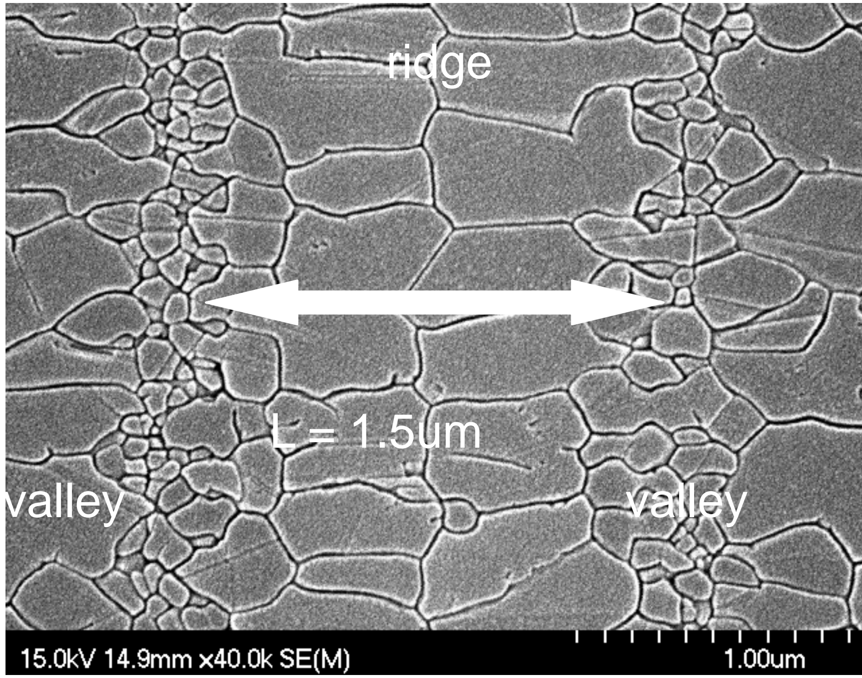


(b)

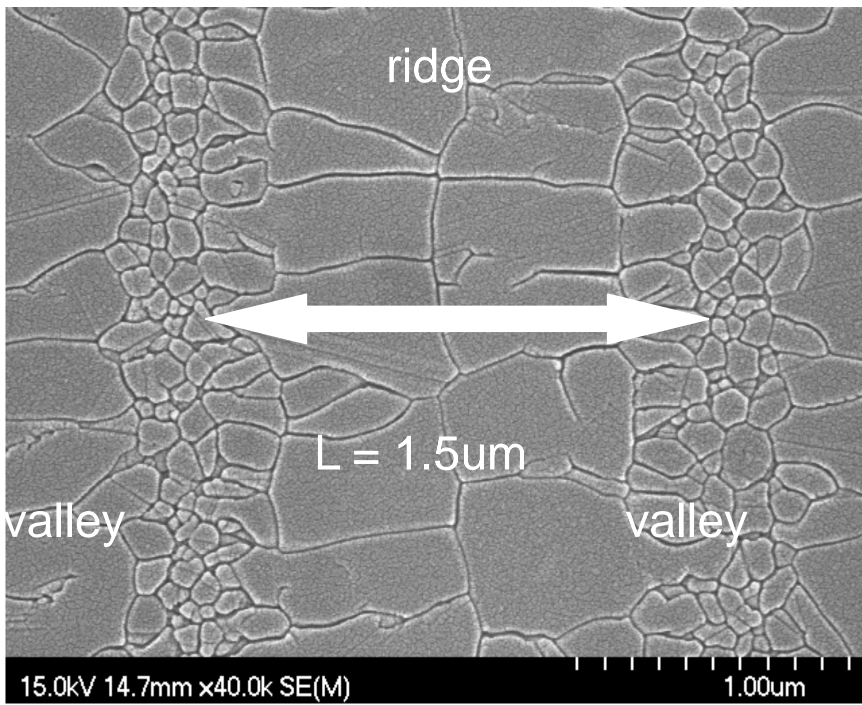


(c)

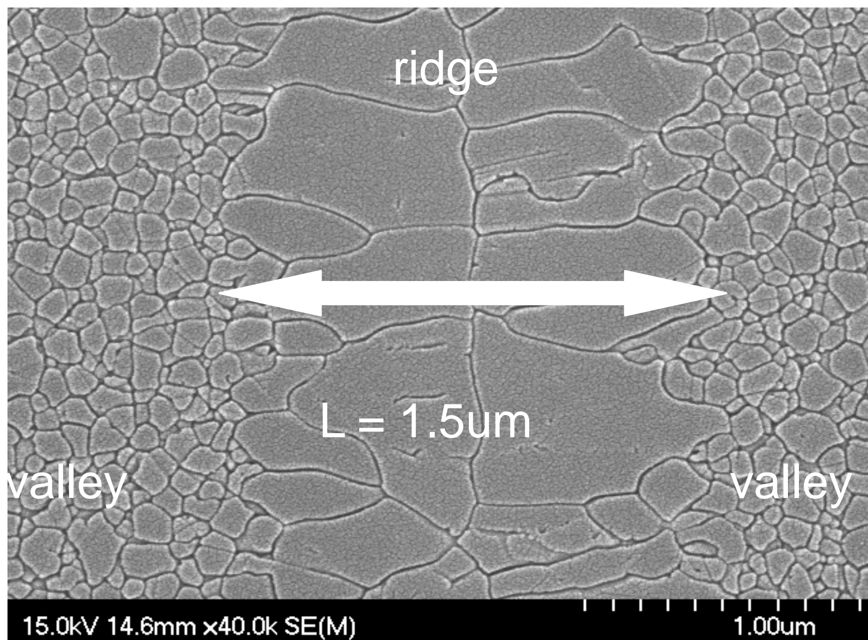
Fig. 2.10 SEM graphs of excimer laser crystallized polycrystalline silicon by period step pre-pattern silicon method. The length between the steps was 2 μm. The laser energy density was (a) 520 (b) 560 (c) 600 mJ/cm^2.



(a)



(b)



(c)

Fig. 2.11 SEM graphs of excimer laser crystallized polycrystalline silicon by period step pre-pattern silicon method. The length of the steps was 1.5 μm. The laser energy density was (a) 460 (b) 540 (c) 600 mJ/cm^2.

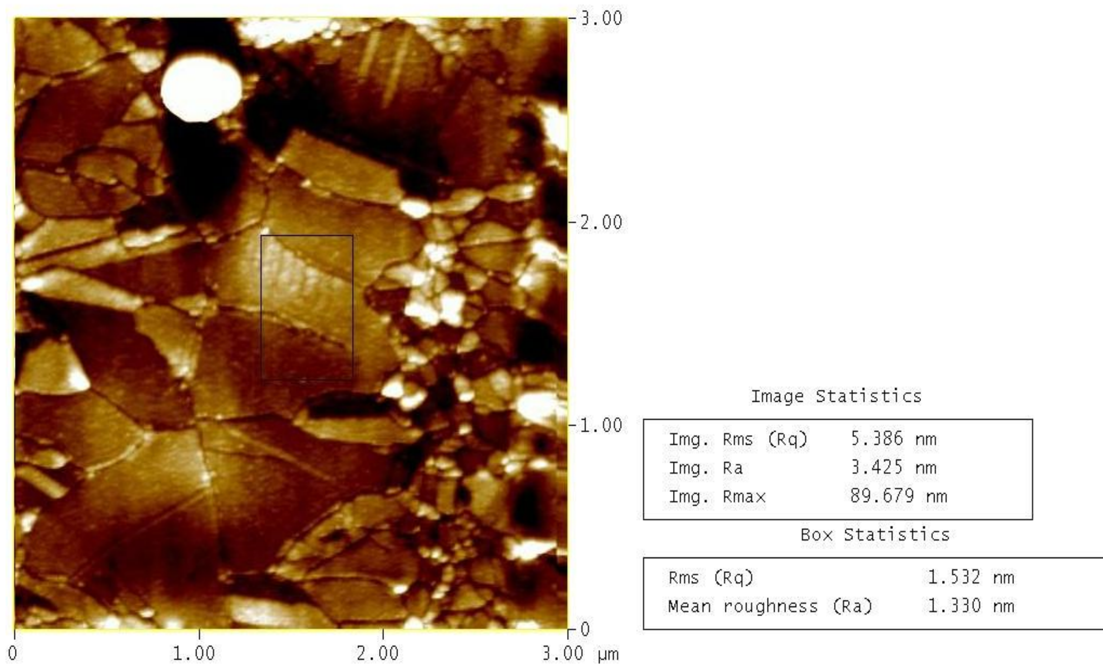


Fig. 2-12 AFM graphs of valley region of excimer laser crystallized polycrystalline silicon with Recessed-Channel with Oxide Step structure. The length of valley region was 2 μm and the excimer laser energy density was 600 mJ/cm^2.

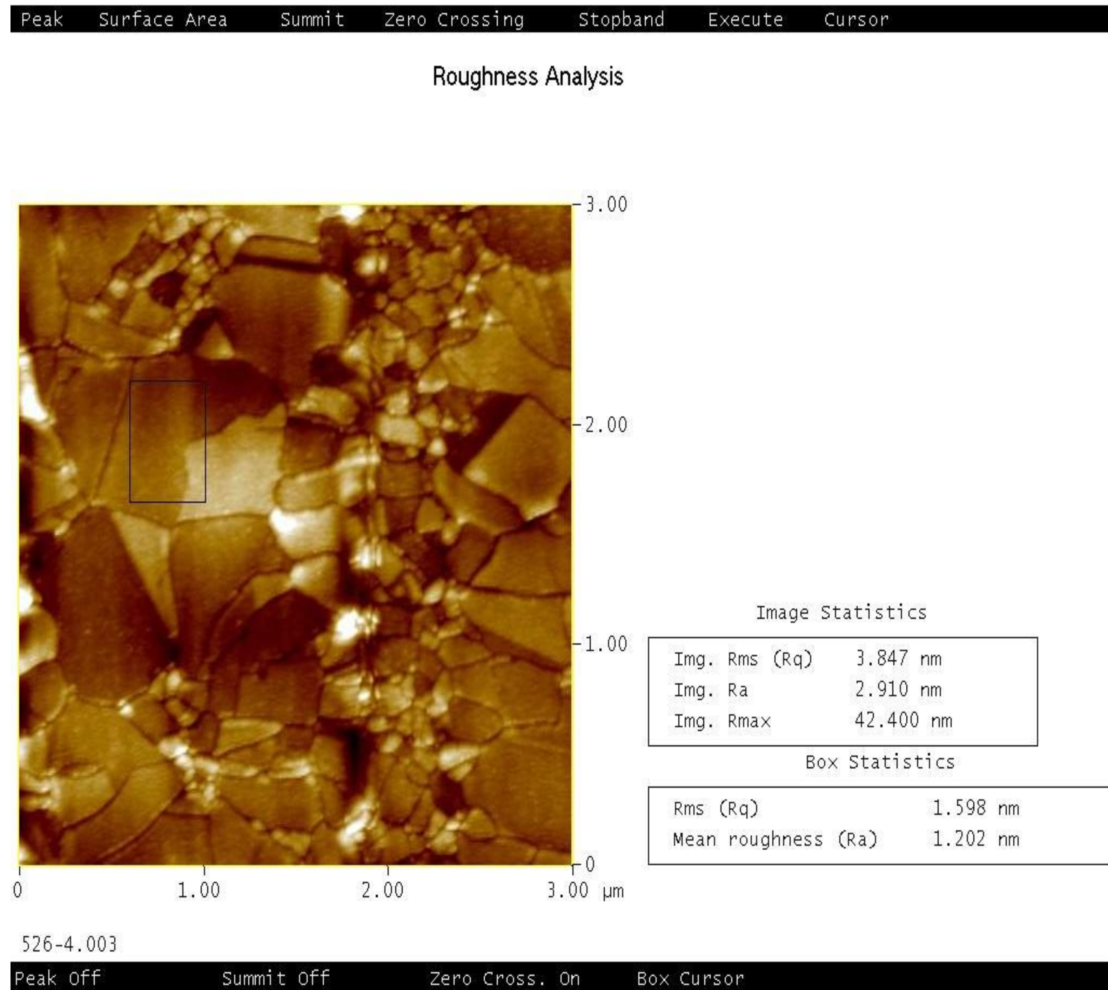


Fig. 2-13 AFM graphs of valley region of excimer laser crystallized polycrystalline silicon with Recessed-Channel with Oxide Step structure. The length of valley region was 1.5 μm and the excimer laser energy density was 600 mJ/cm^2.

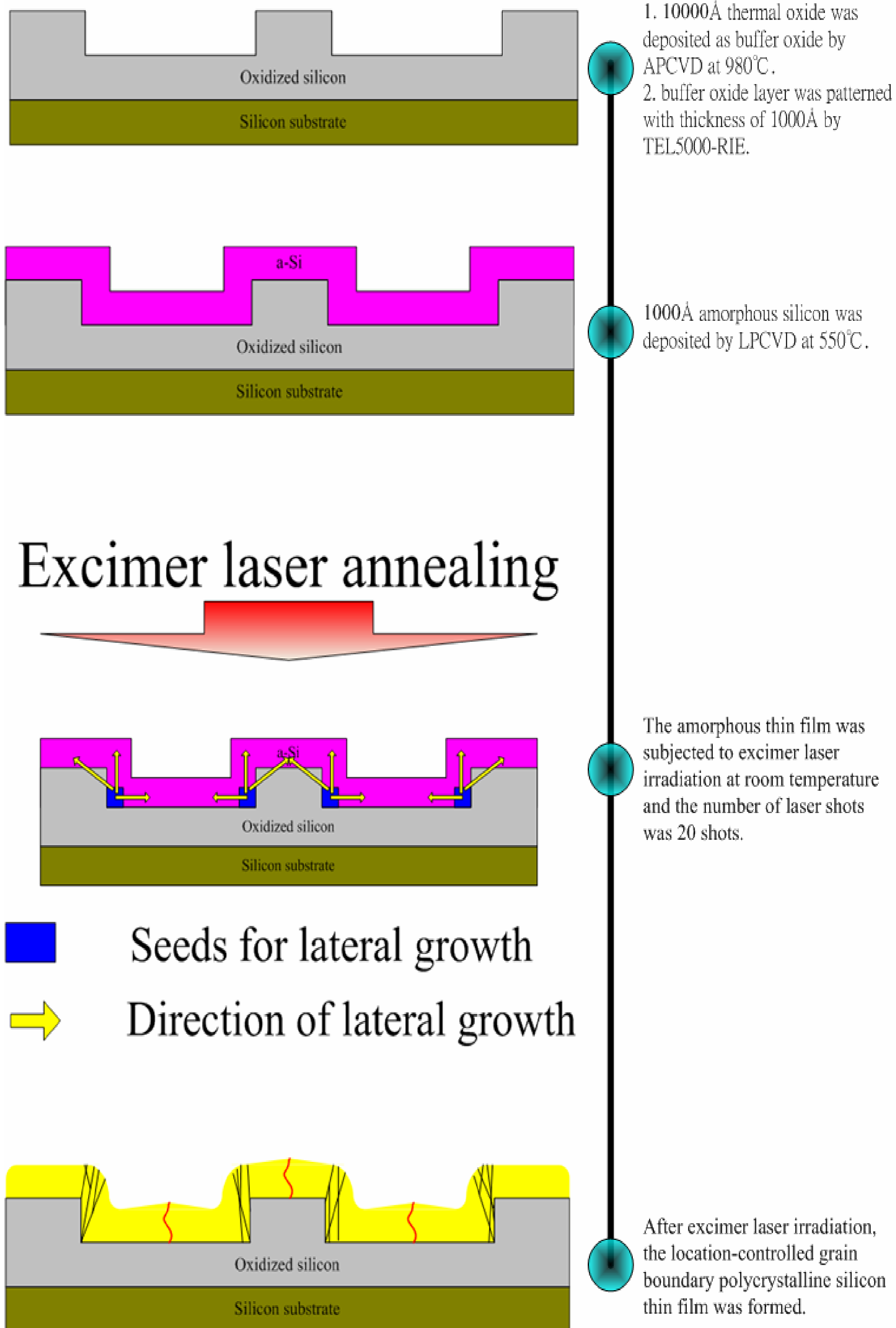


Fig. 2-14 Process flow for fabrication of SGB-TFTs by Recessed-Channel with Oxide Step method (I).

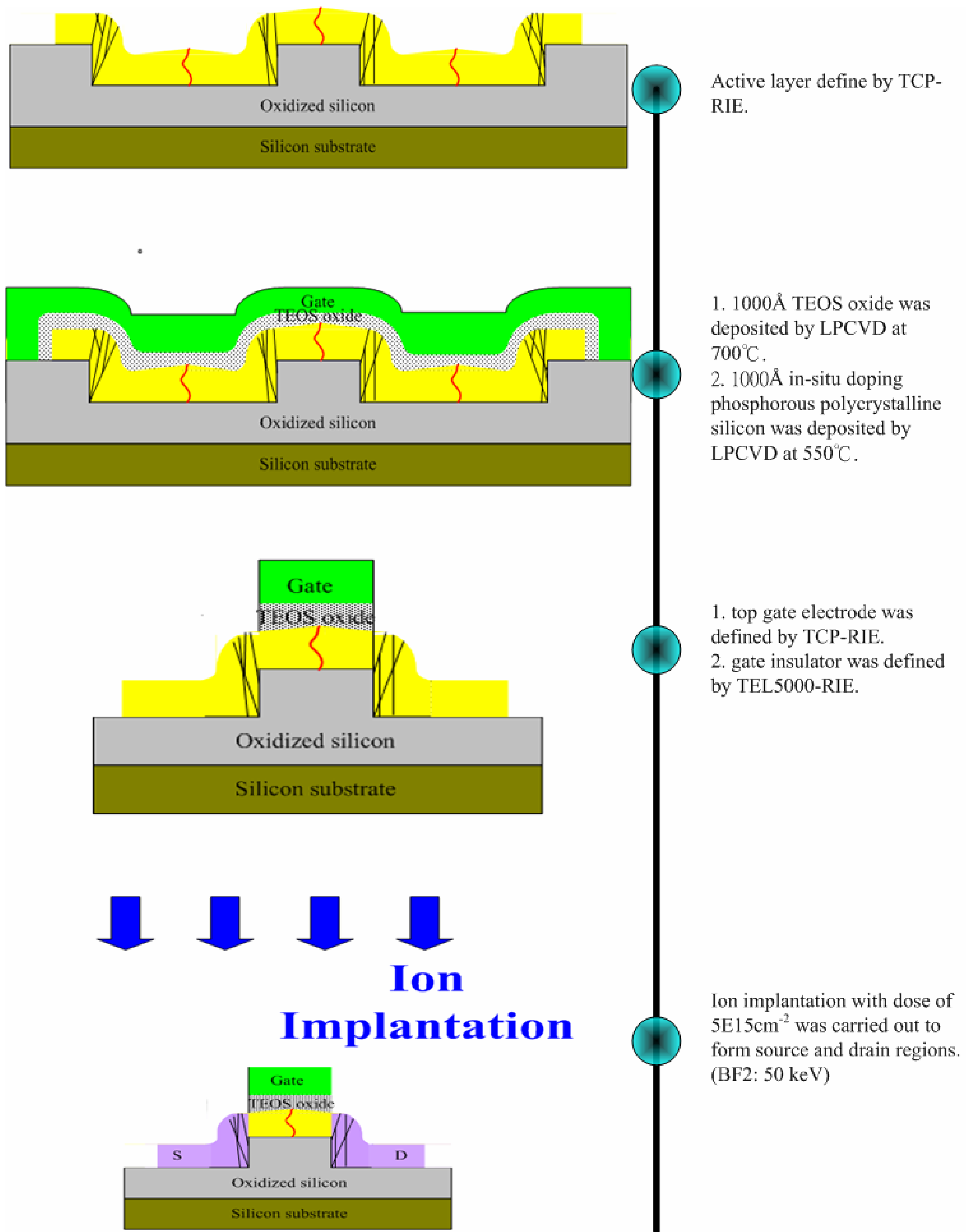
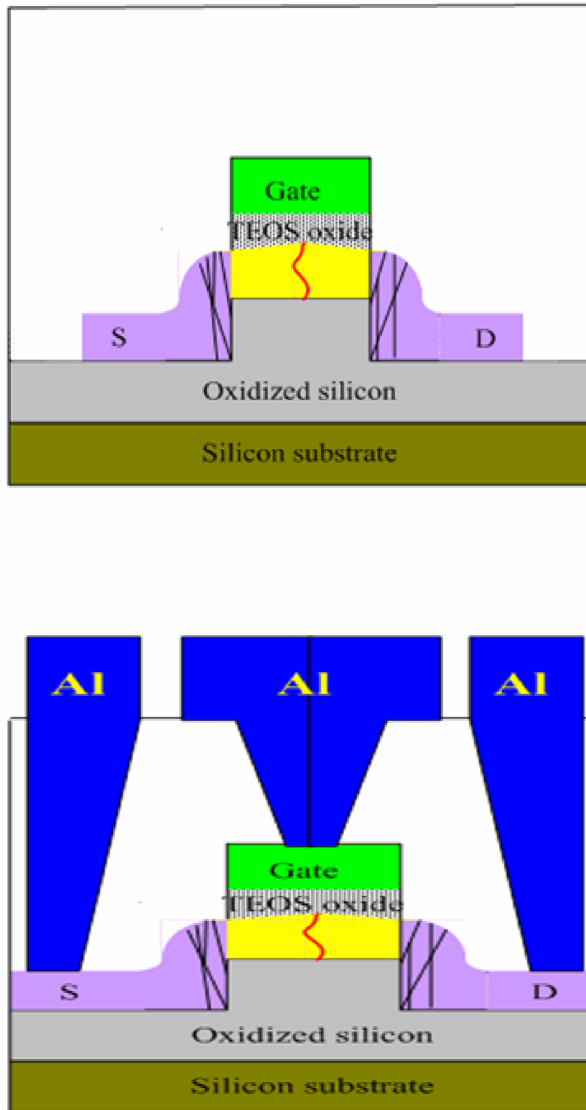


Fig. 2-14 Process flow for fabrication of SGB-TFTs by Recessed-Channel with Oxide Step method (II).



4000Å TEOS oxide was deposited by LPCVD at 700℃ followed by thermal annealing for 9hr to activate the dopants.

Contact hole formation by TEL5000-RIE and metallization was carried out by thermal coater and dry etching.
Finally Al sintering at 400℃ was carried out.

Fig. 2-14 Process flow for fabrication of SGB-TFTs by Recessed-Channel with Oxide Step method (III).

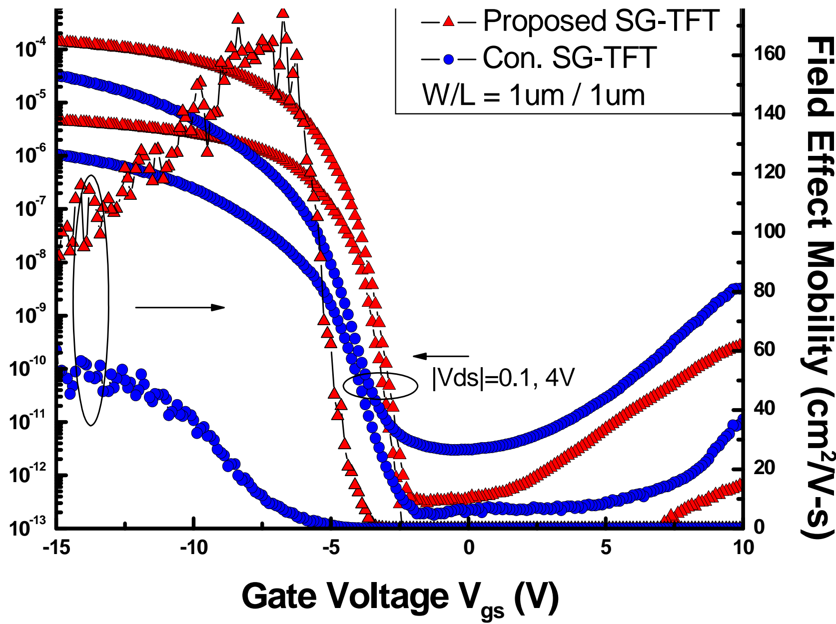


Fig. 2-15 The typical transfer characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

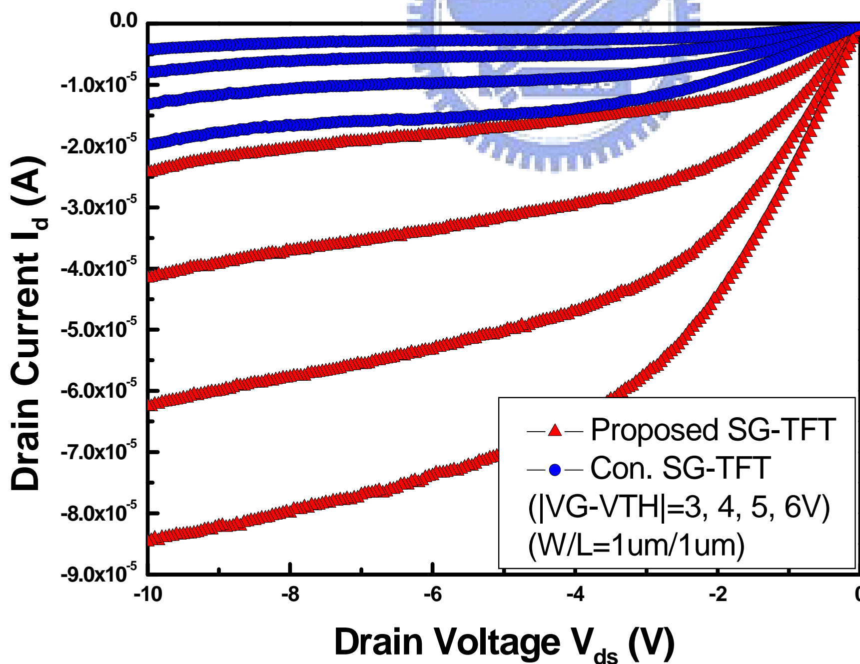


Fig. 2-16 The output characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

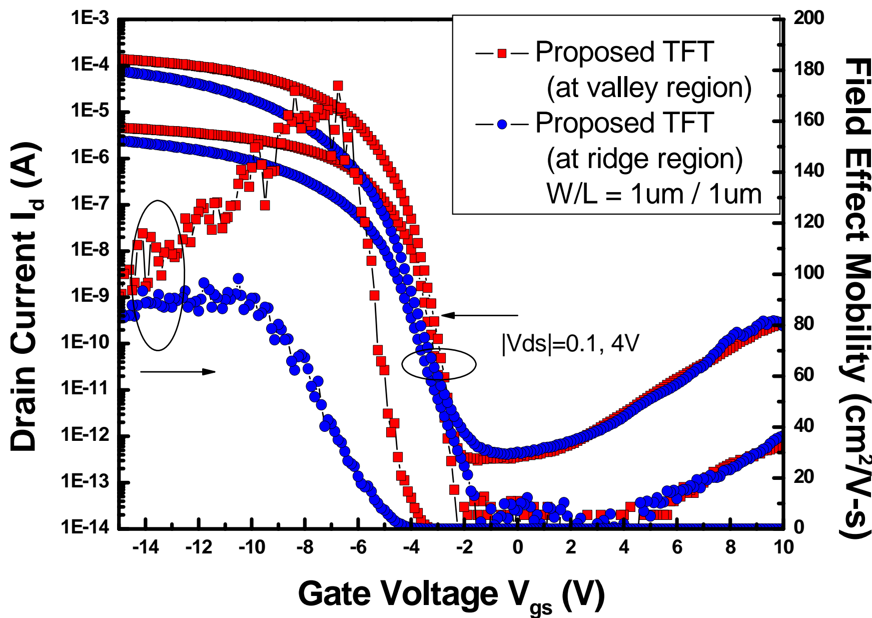


Fig. 2-17 The typical transfer characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

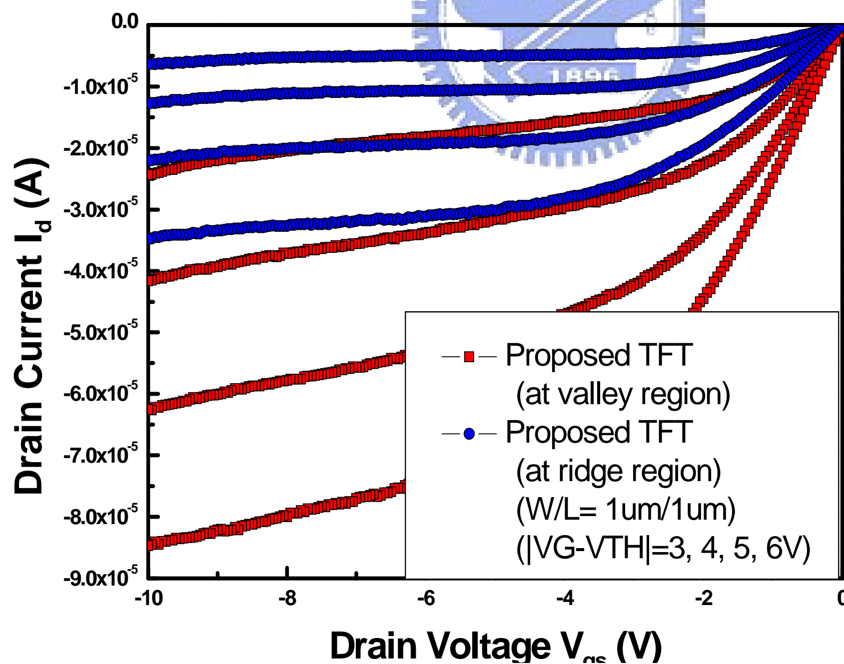


Fig. 2-18 The output characteristics of p-channel single gate LTPS-TFTs crystallized using Recessed-Channel with Oxide Step method. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping).

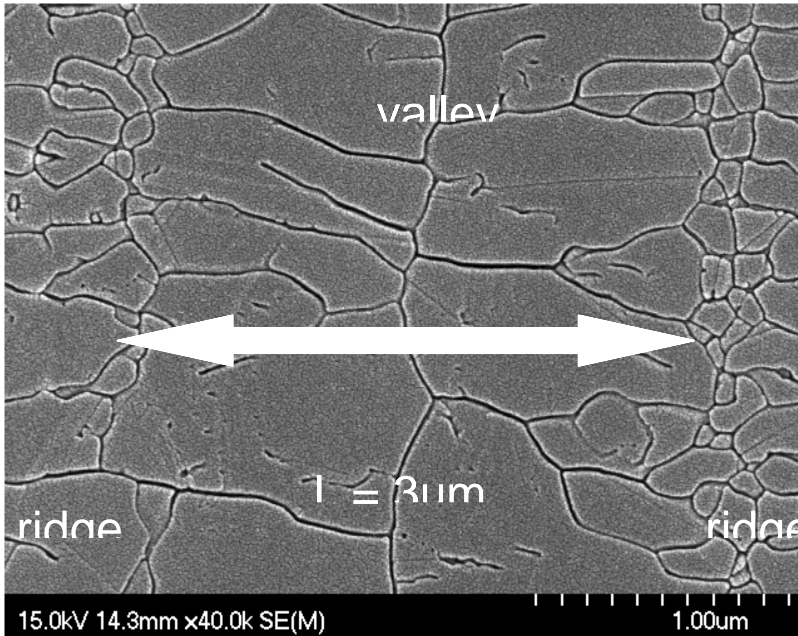


Fig. 2-19 SEM graph of the valley region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method.

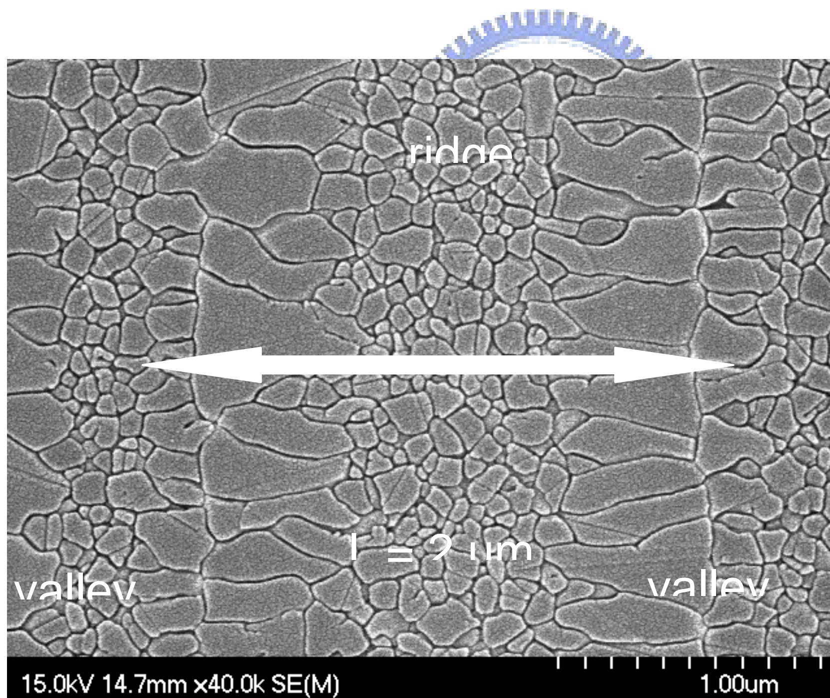


Fig. 2-20 SEM graph of the ridge region of poly-Si thin film fabricated by Recessed-Channel with Oxide Step method.

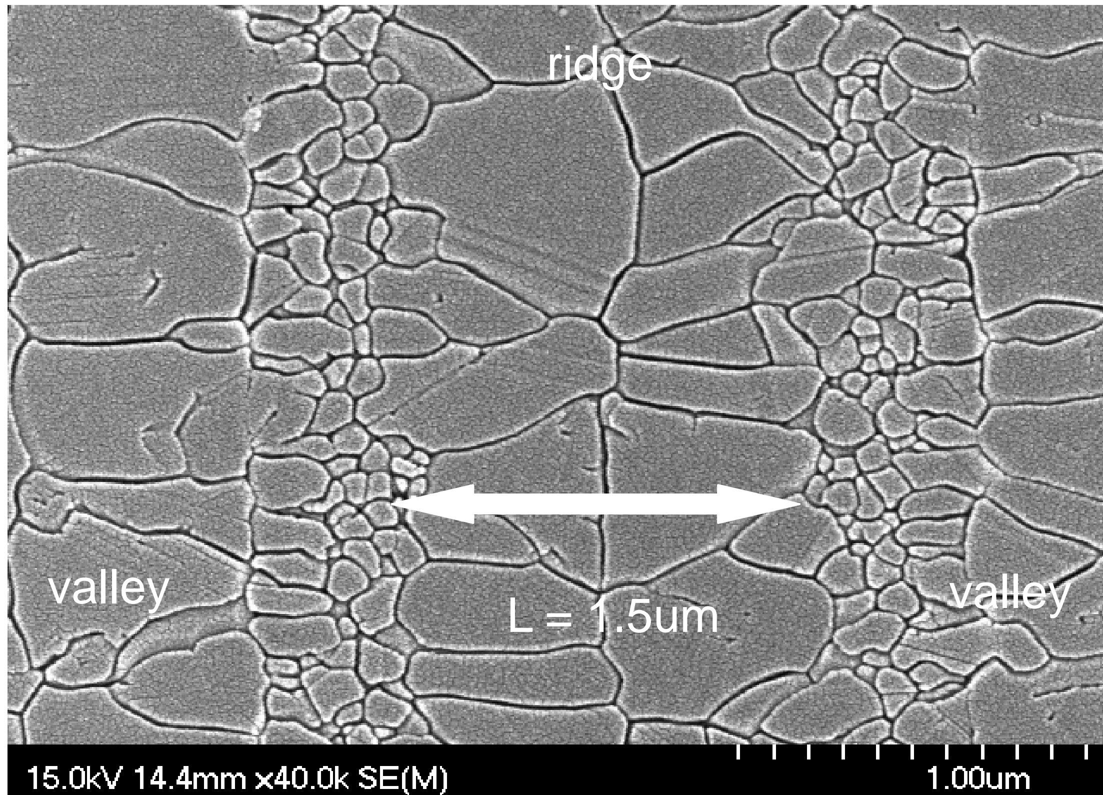


Fig. 3-1 SEM graph of ridge region of exceimer laser crystallized polycrystalline silicon by Recessed-Channel with Oxide Step method. The length of ridge region was 1.5 μm. The excimer laser energy density was 600 mJ/cm^2.

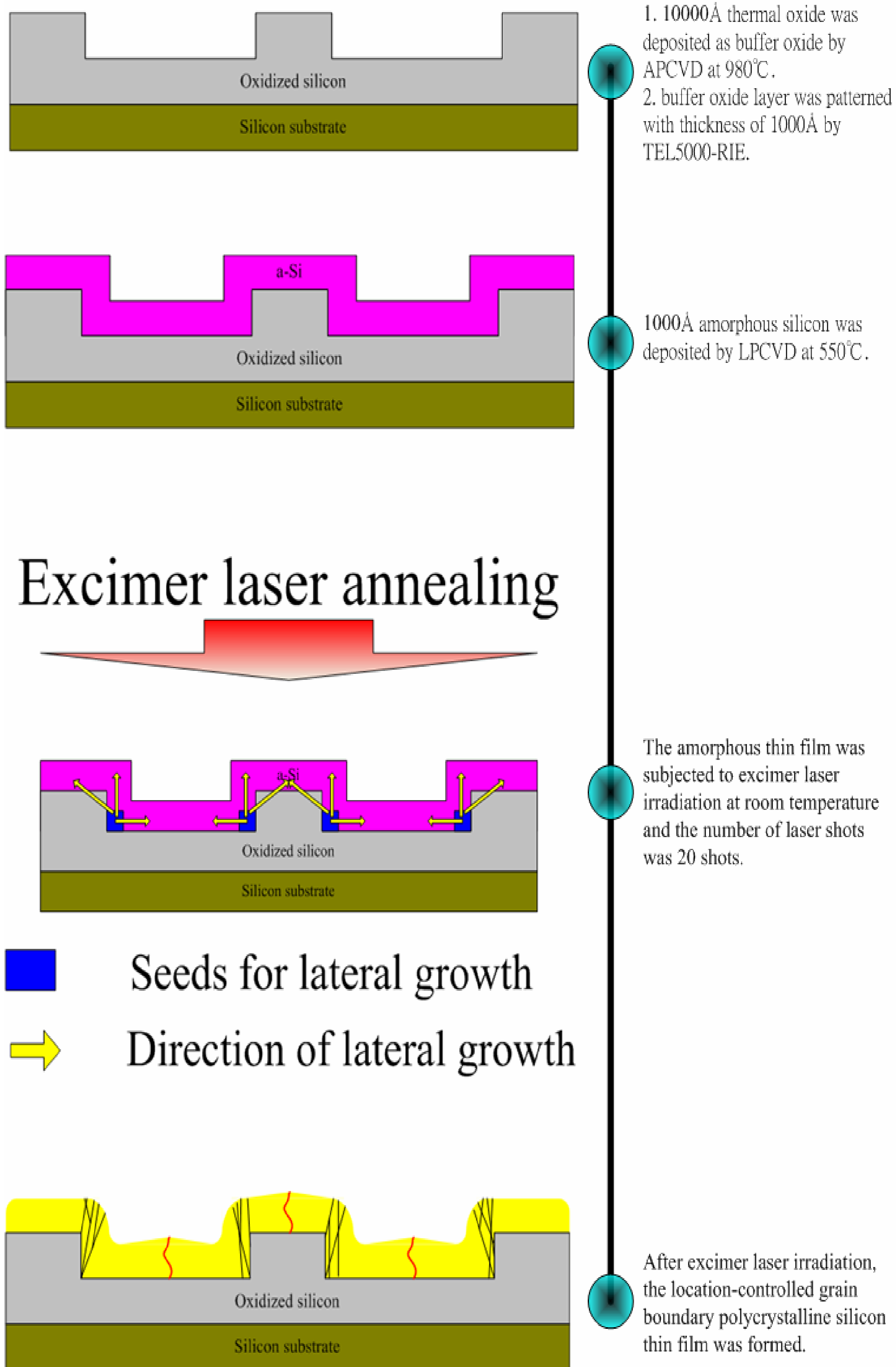


Fig. 3-2 Process flow for fabrication of MG TFTs by Recessed-Channel with Oxide Step method (I)

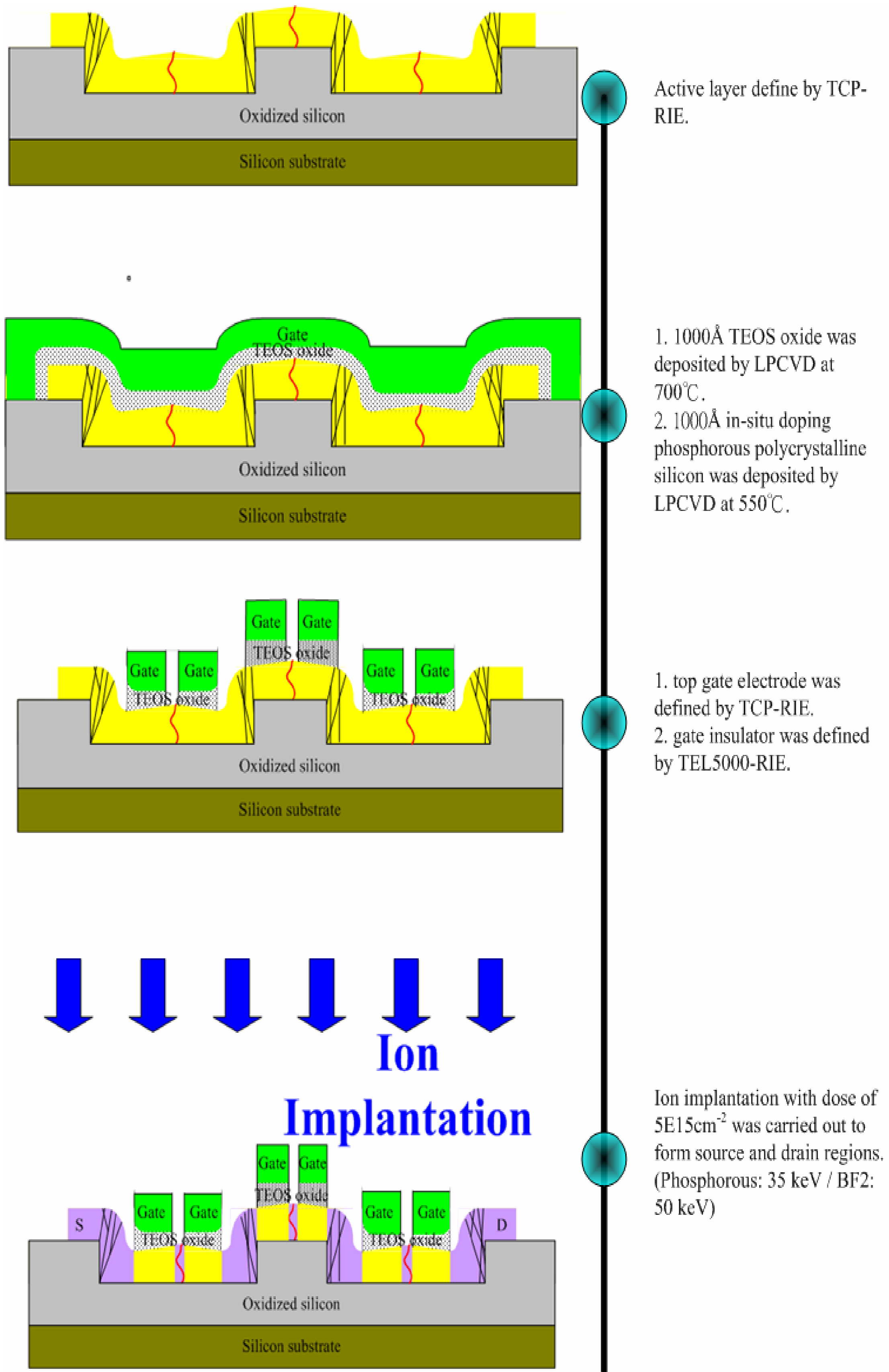
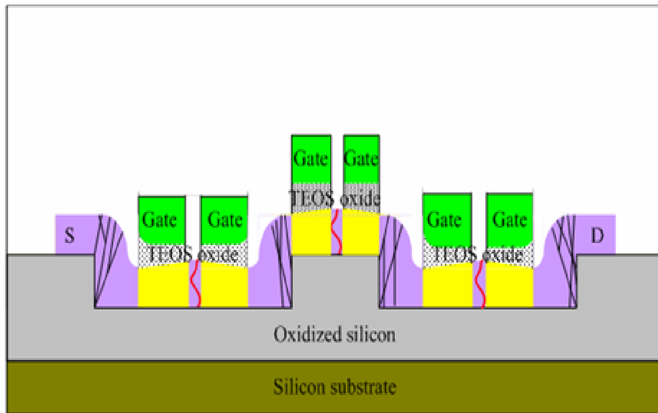
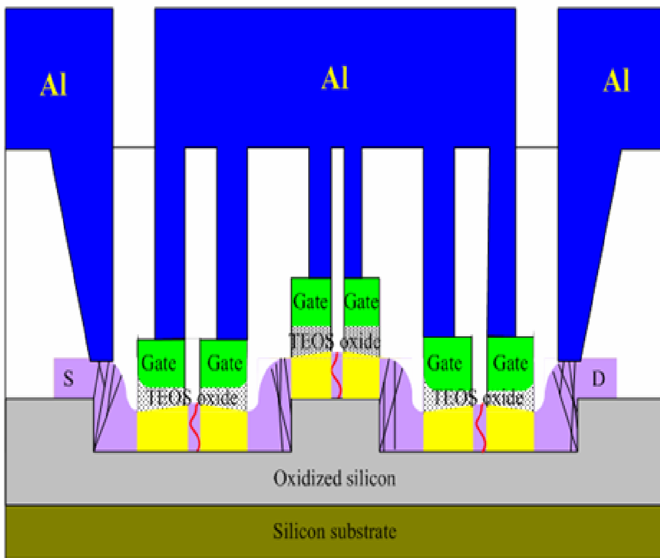


Fig. 3-2 Process flow for fabrication of MG TFTs by Recessed-Channel with Oxide Step method (II)



4000Å TEOS oxide was deposited by LPCVD at 700℃ followed by thermal annealing for 9hr to activate the dopants.



Contact hole formation by TEL5000-RIE and metallization was carried out by thermal coater and dry etching.

Finally Al sintering at 400℃ was carried out.

Fig. 3-2 Process flow for fabrication of MG TFTs by Recessed-Channel with Oxide Step method (III)

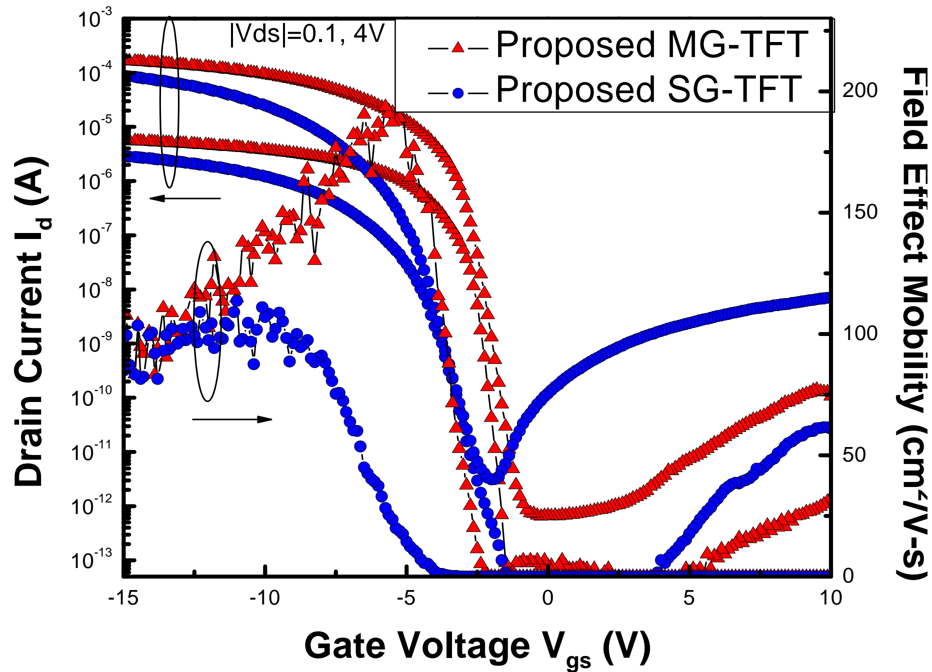


Fig. 3-3 The typical transfer characteristics of SG-TFTs and MG-TFTs with location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

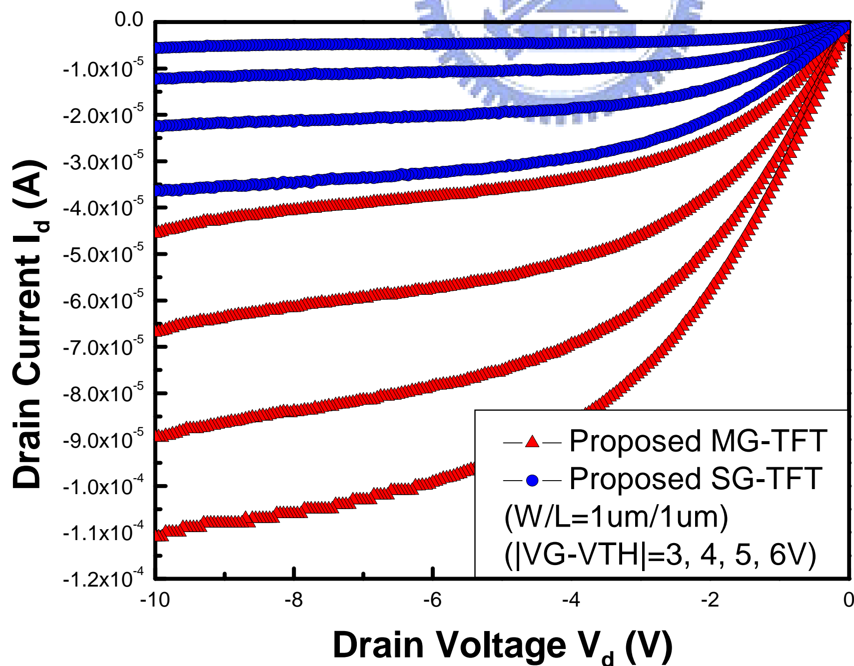


Fig. 3-4 The output characteristics of SG-TFTs and MG-TFTs with location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

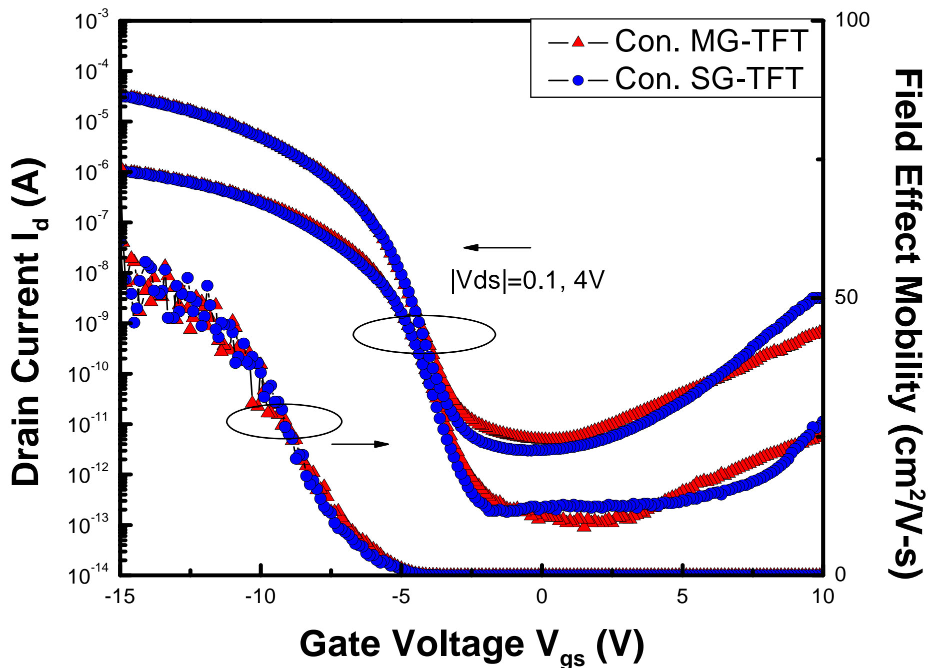


Fig. 3-5 The typical transfer characteristics of SG-TFTs and MG-TFTs fabricated without location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

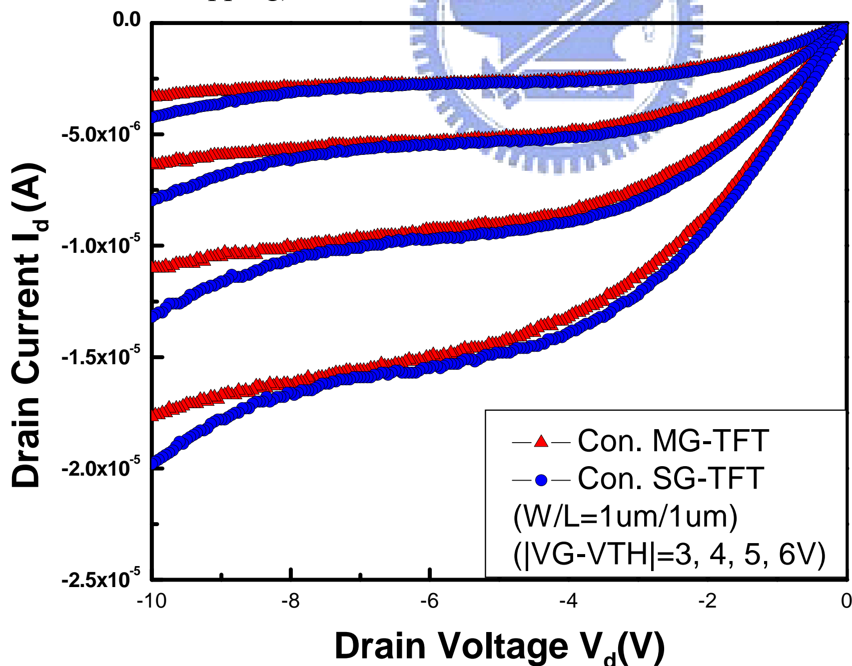


Fig. 3-6 The output characteristics of SG-TFTs and MG-TFTs fabricated without location-controlled technology. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

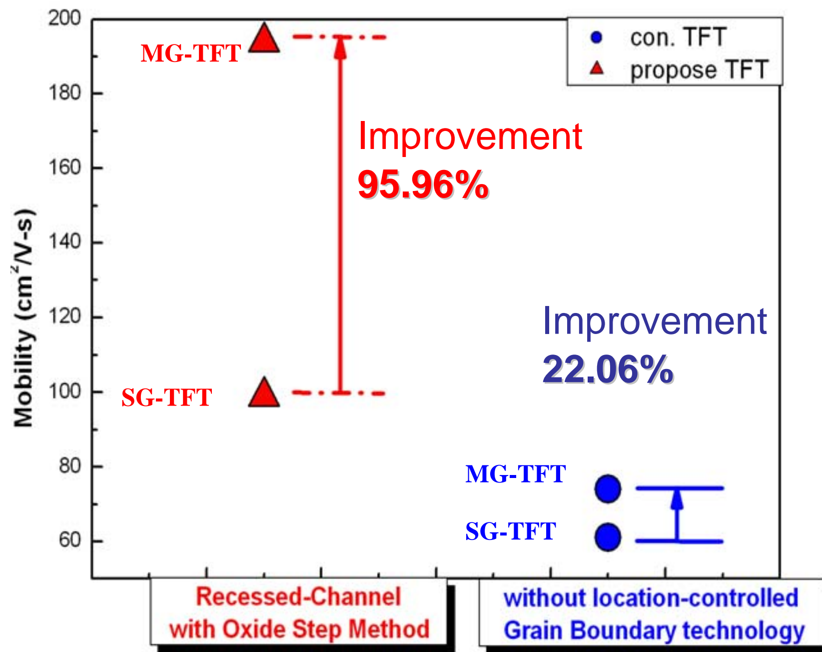


Fig. 3-7 Field-effect mobility improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

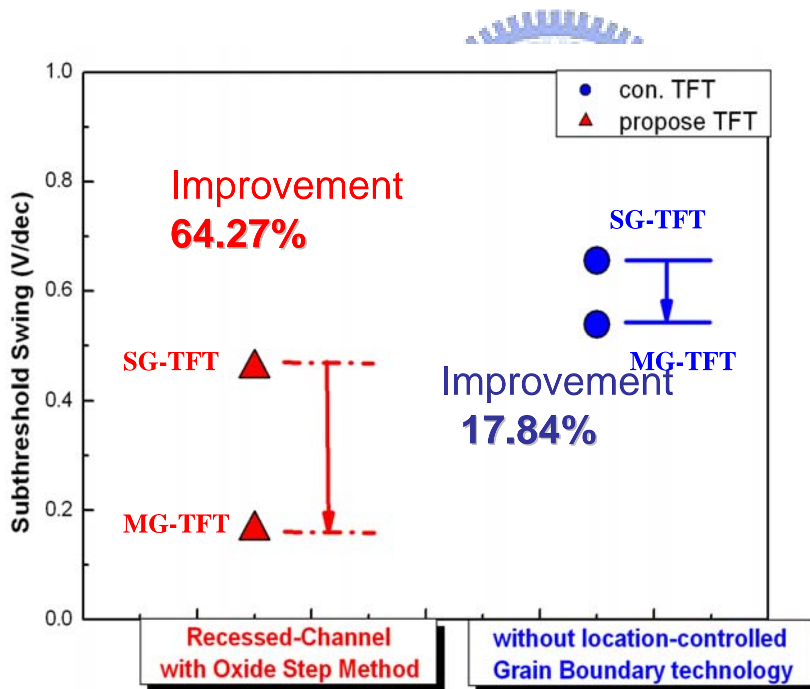


Fig. 3-8 Subthreshold swing improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

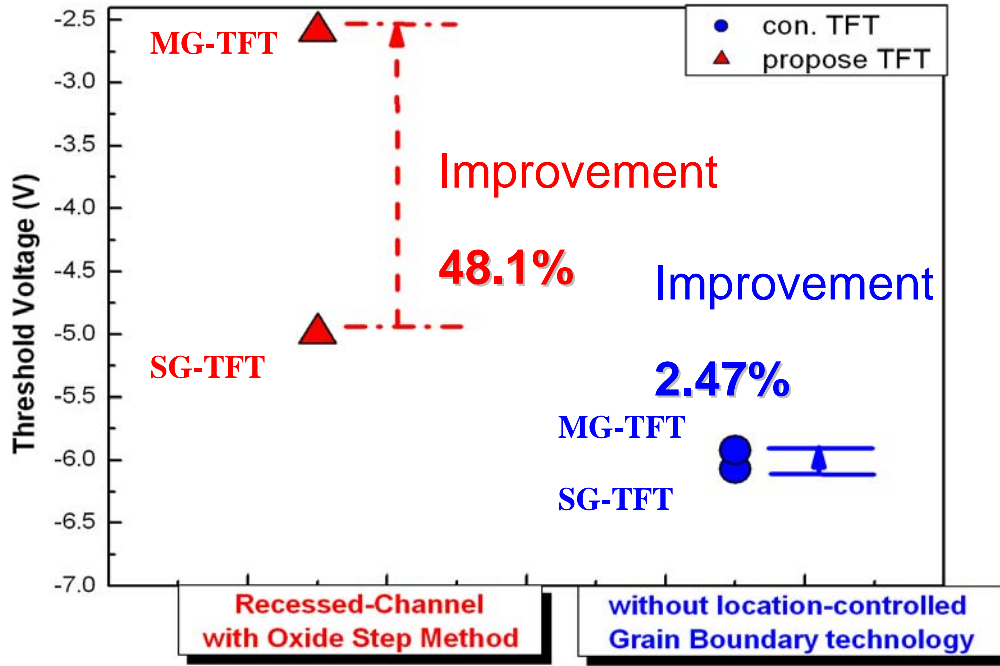


Fig. 3-9 Threshold voltage improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

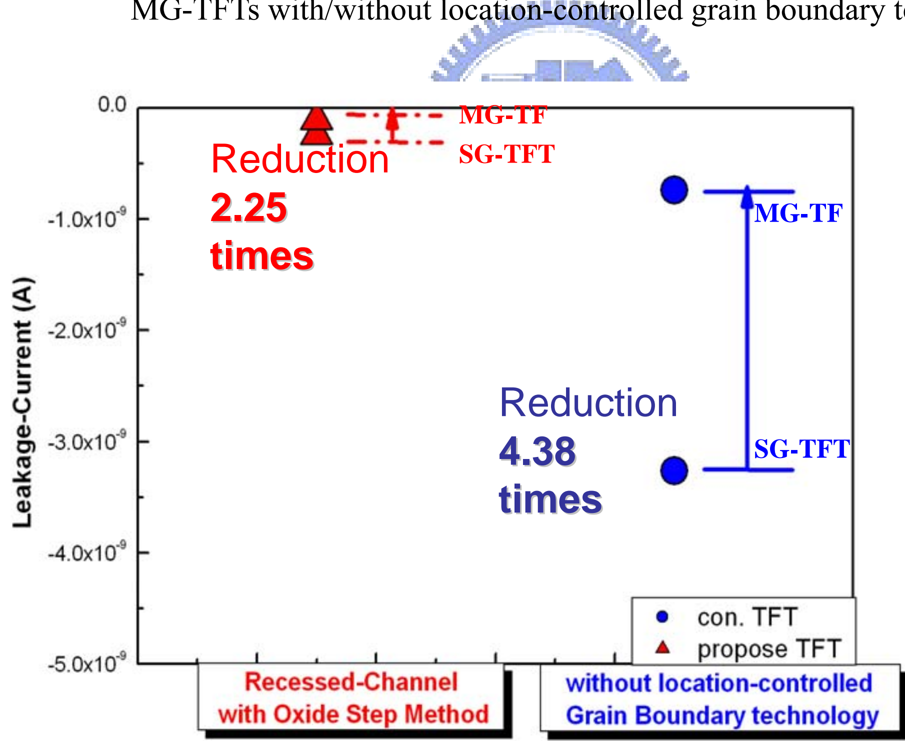


Fig. 3-10 Leakage current improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

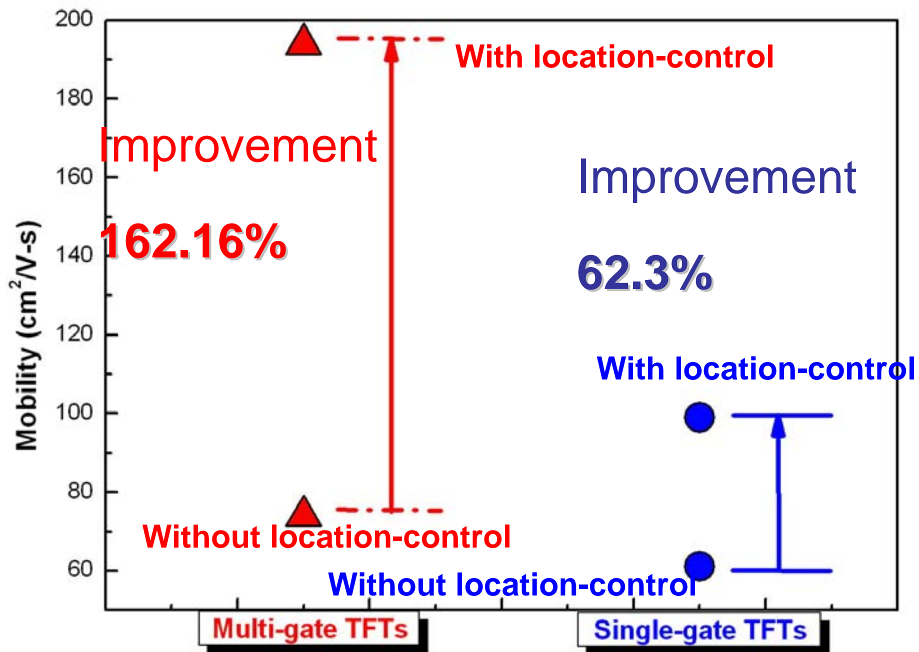


Fig. 3-11 Field-effect mobility improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

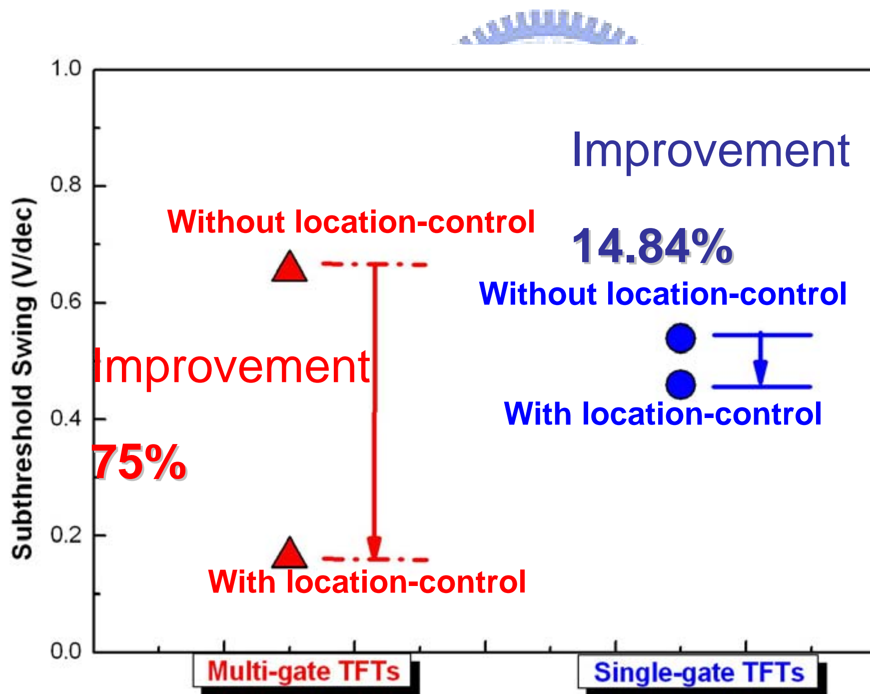


Fig. 3-12 Subthreshold swing improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

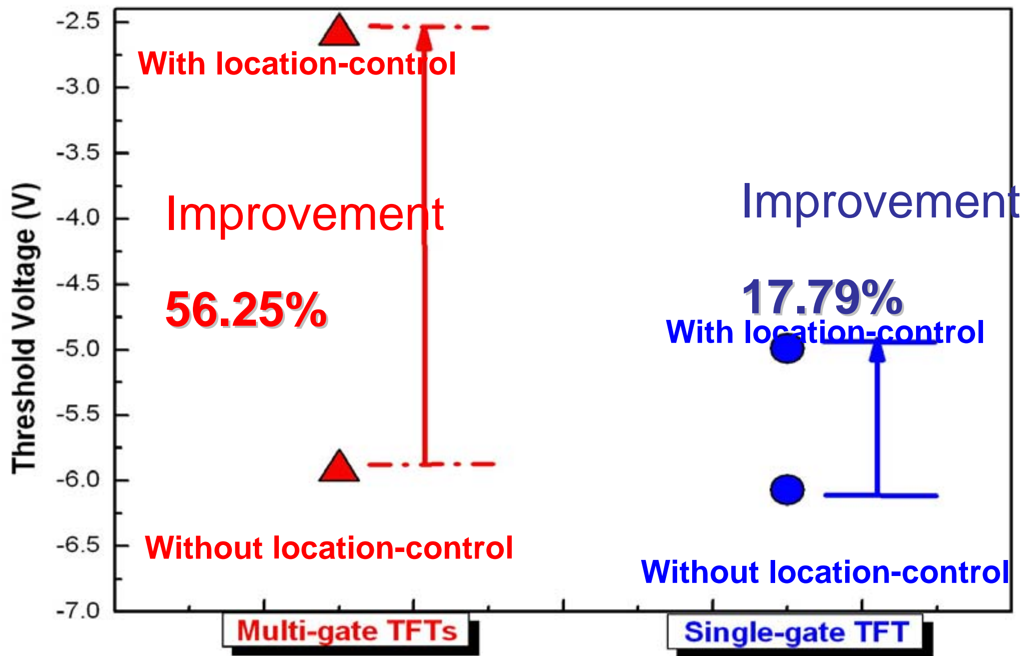


Fig. 3-13 Threshold voltage improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

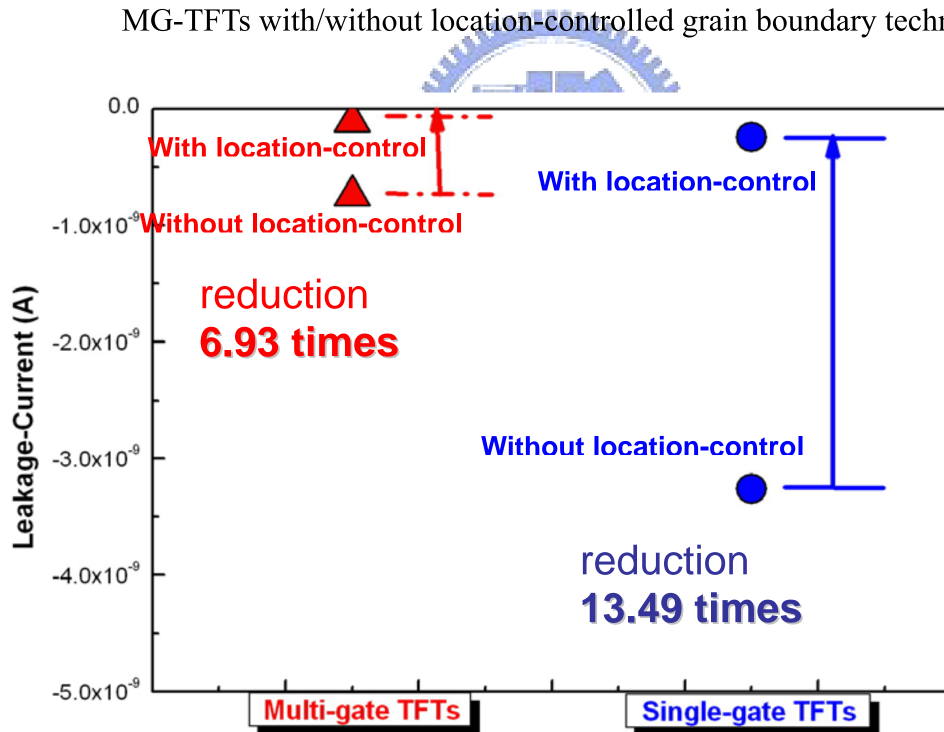


Fig. 3-14 Leakage current improvement of electrical characteristics of SG-TFTs and MG-TFTs with/without location-controlled grain boundary technology.

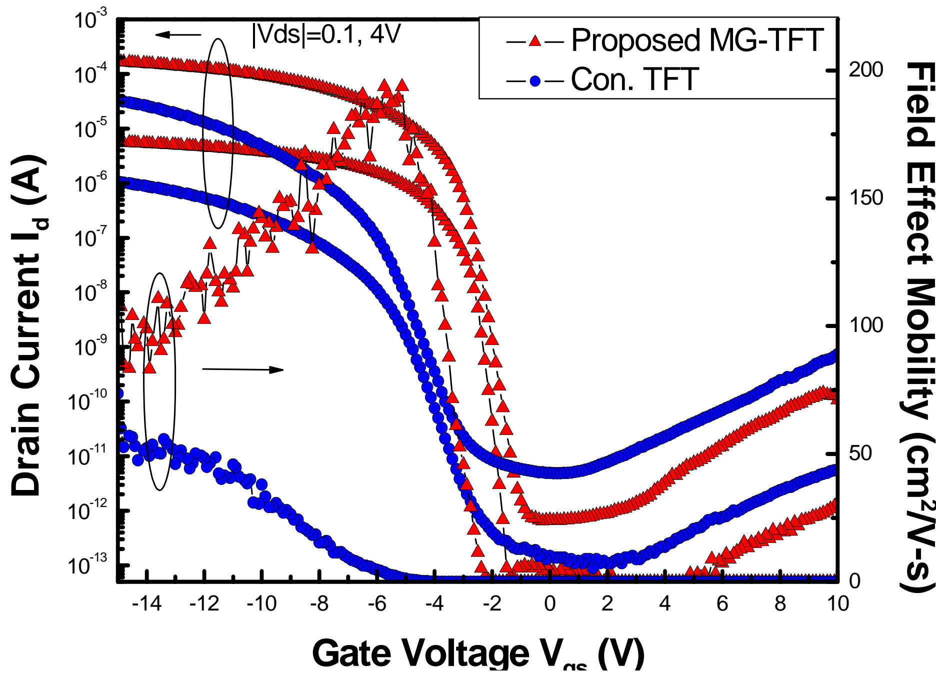


Fig. 3-15 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 1 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

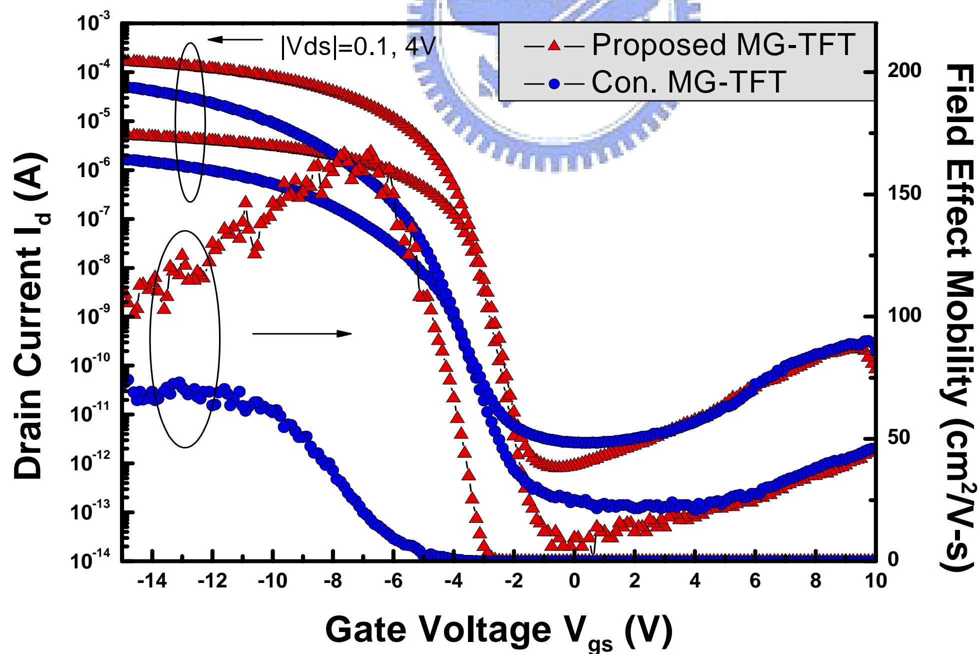


Fig. 3-16 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs.. The channel length was 2 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

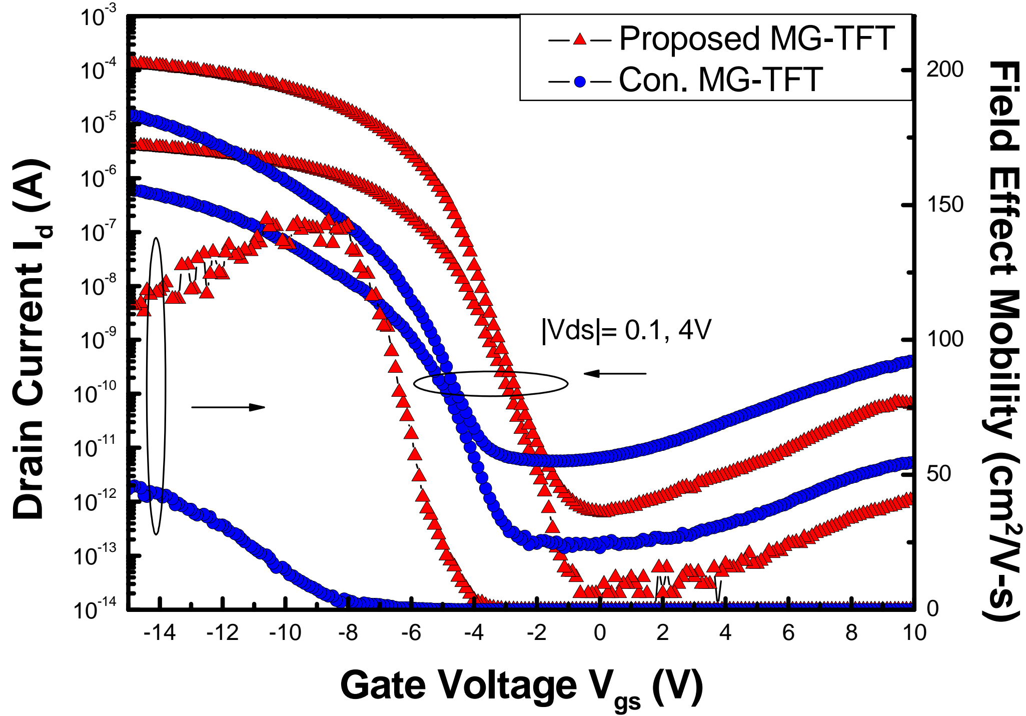


Fig. 3-17 The typical transfer characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs.. The channel length was 3 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

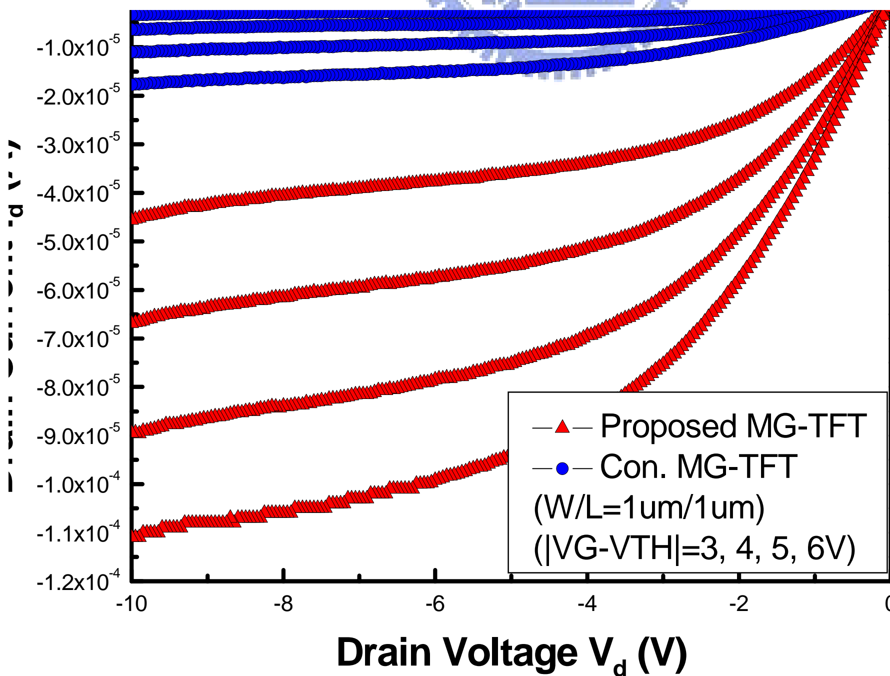


Fig. 3-18 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 1um. The laser energy was 560 mJ/cm^2 and the number of laser shots was

20 (ie. 95% overlapping)

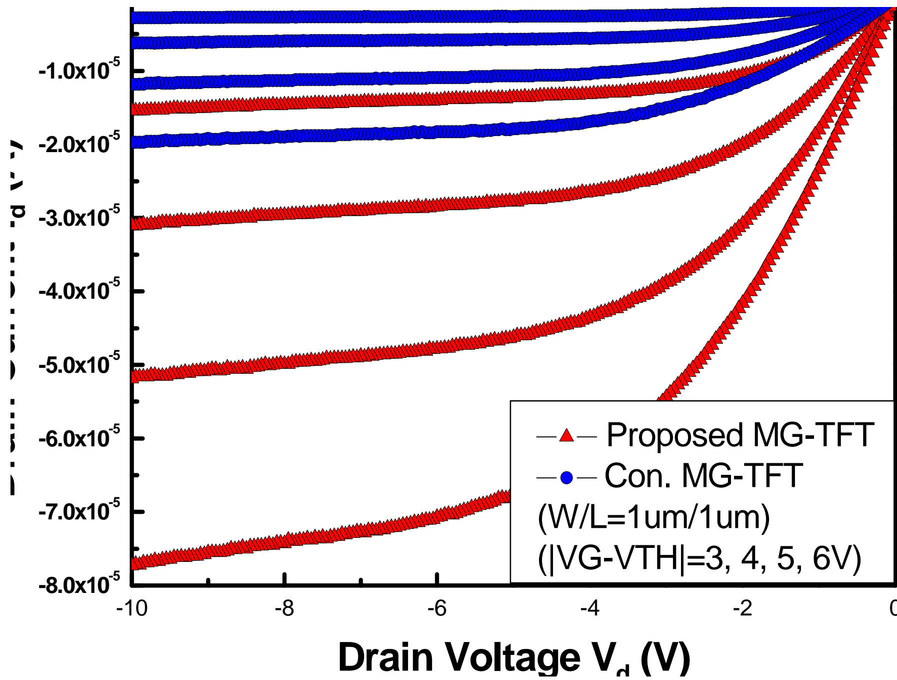


Fig. 3-19 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 2 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was 20 (ie. 95% overlapping)

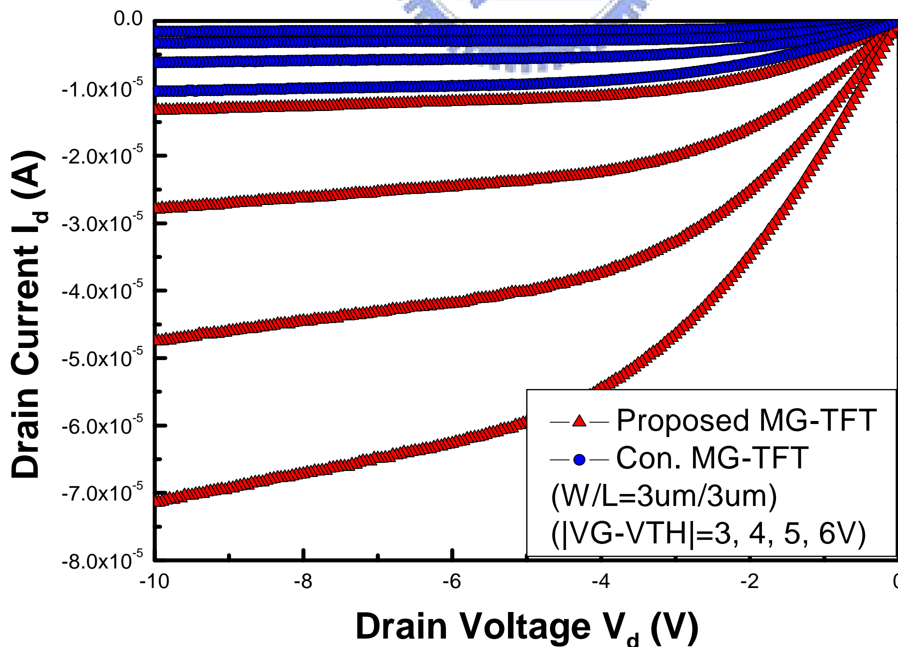


Fig. 3-20 The output characteristics of MG-TFTs fabricated by Recessed-Channel with Oxide Step method and conventional TFTs. The channel length was 3 um. The laser energy was 560 mJ/cm^2 and the number of laser shots was

20 (ie. 95% overlapping)

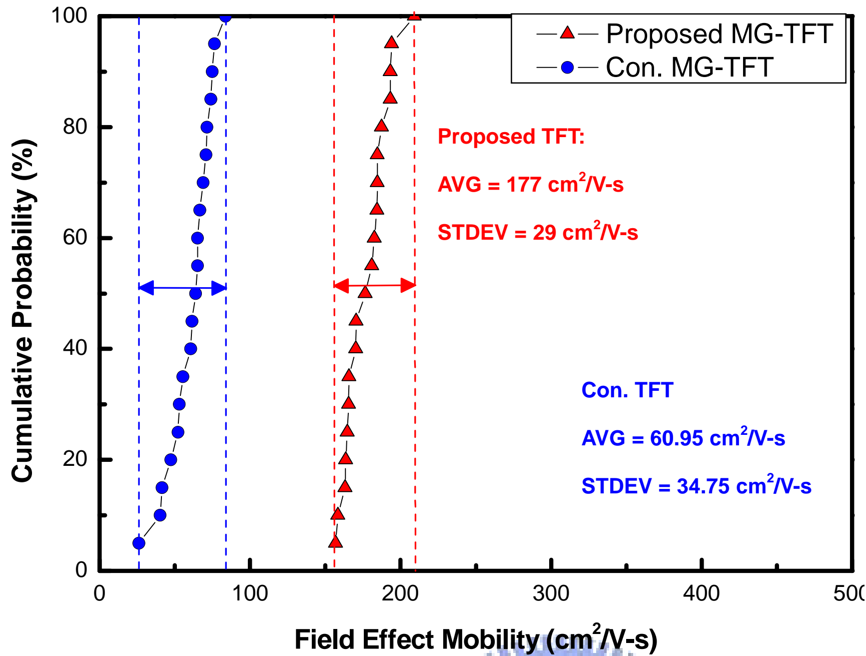


Fig. 3-21 Statistics and uniformity of equivalent field effect mobility. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping).

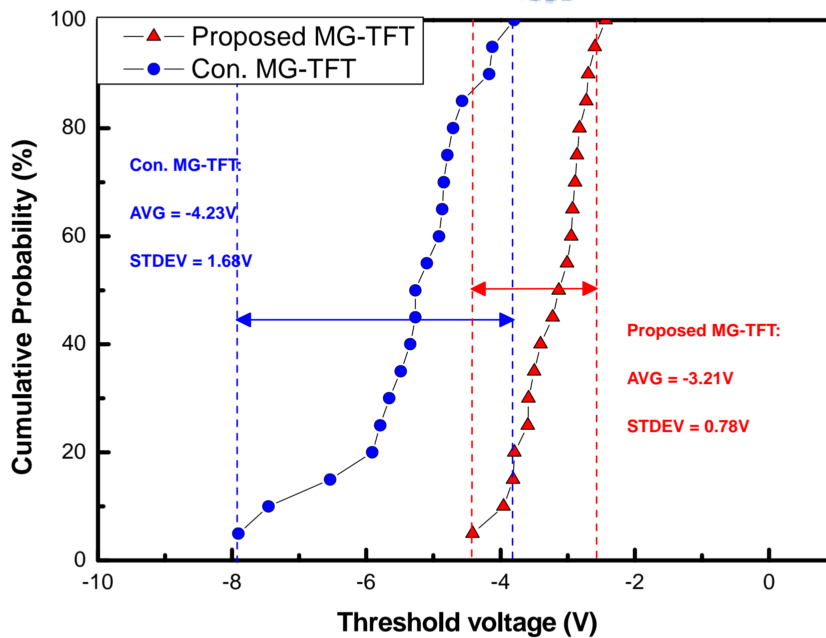


Fig. 3-22 Statistics and uniformity of threshold voltage. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and

conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping).

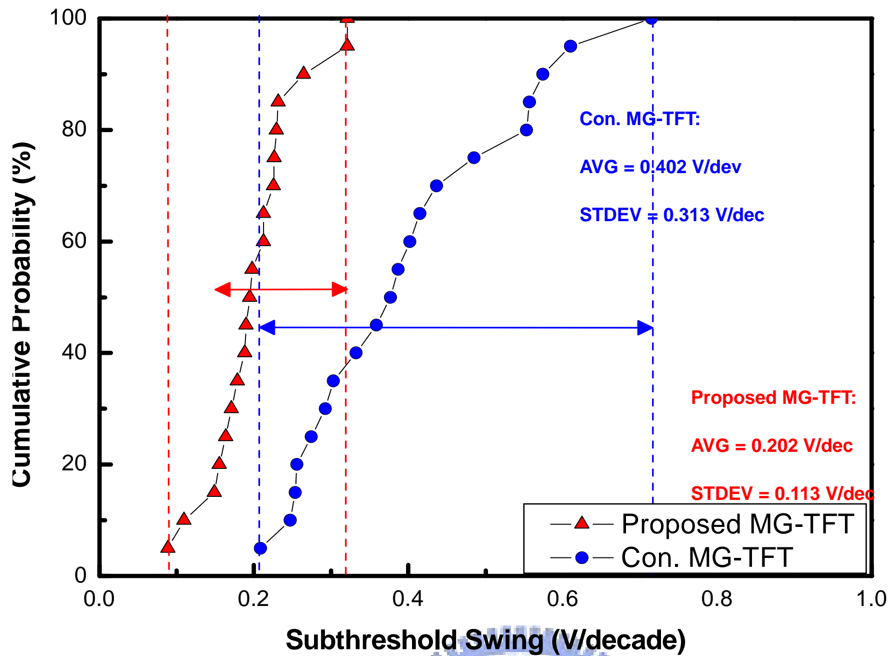


Fig. 3-23 Statistics and uniformity of subthreshold swing. Twenty p-channel MG-TFTs crystallized by Recessed-Channel with Oxide Step method and conventional MG-TFTs were measured. The laser energy was 560 mJ/cm^2, the number of laser shots was 20(ie. 95% overlapping).

References

Chapter 1

[1.1] S. D. Brotherton, "polycrystalline silicon thin film transistors," *Semi-conduct. Sci. Technol.*, vol. 10, pp. 712-738, 1995

[1.2] Yasuhisa Oana, "Current and future technology of low-temperature polycrystalline silicon TFT-LCDs," *Journal of the SID*, vol. 9, pp. 169-172, 2001.

[1.3] J. G. Blake, J. D. III Stevens, and R. Young, "Impact of low temperature polycrystalline silicon on the AMLCD market," *Solid State Tech.*, vol. 41, pp. 56-62, 1998.

[1.4] Mutsumi Kimura, Ichio Yudasaka, Sadao Kanbe, Hidekazu Kobayashi, Hiroshi Kiguchi, Shun-ichi Seki, Satoru Miyashita, Tatsuya Shimoda, Tokuro Ozawa, Kiyofumi Kitawada, Takashi Nakazawa, Wakao Miyazawa, and Hiroyuki Ohshima, "Low-temperature polycrystalline silicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," *IEEE Trans. Electron Devices*, vol. 46, pp. 2282-2288, 1999.

[1.5] Mark Stewart, Robert S. Howell, Leo Pires, and Miltiadis K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001.

[1.6] D. E. Carlson and C. R. Wronki, "Amorphous Silicon Solar Cell," Appl. Phys. Lett. Vol. 28, pp. 671-673, 1976.

[1.7] M. J. Thompson and H. C. Tuan, "Amorphous Si Electronic Devices and Their Applications," Technical Digest - International Electron Devices Meeting, pp. 192-195, 1986.

[1.8] S. Tomiyama, T. Ozawa, H. Ito and T. Nakamura, "Amorphous silicon thin film transistors and application to image sensors," Journal of Non-Crystalline Solids,

Volume 198-200, Part 2, pp. 1087-1092, 1996.

[1.9] L. E. Fennell, M. J. Thompson, H.C. Tuan and R. Weisfield, “Page-Wild a-Si TFT Arrays for Electronic Printing and Copying,” International Display Research Conference (IDRC), pp.167-169, 1988.

[1.10] F. Morin, “Amorphous silicon TFTs and their applications,” Microelectronic Engineering, vol.19, pp.171-178, 1992.

[1.11] P. G. LeComber, W. E. Spear and Ghaith, “Amorphous Silicon Field-Effect Device and Possible Application,” Electronics Letters, vol.15, pp.179-181, 1979.

[1.12] Kinoshita H., Kitahara H., Schleupen K., Colgan E.G., Nunes R., Kodate M., and Takasugi S., “High-resolution AMLCD made with a-Si:H TFTs and an Al gate and IZO structure,” Journal of the Society for Information Display, vol.7, pp.265-267, 1999.

[1.13] Chi-Wen Chen, Ting-Chang Chang, Po-Tsun Li, Hau-Yan Lu, Kao-Cheng Wang, Chen-Shuo Huang, Chia-Chun Ling and Tesung-Yuen Tseng, “High-performance hydrogenated amorphous-Si TFT for AMLCD and AMOLED applications,” IEEE Electron Device Letters, vol.26, pp.731-733, 2005.

[1.14] Corbin Church and Arokia Nathan, “Amorphous-silicon TFT AMOLEDs,” Information Display, vol.21, pp.22-26, 2005.

[1.15] J.H. Jung, H. Kim, , S.P. Lee, U.C. Sung, J.S. Rhee, C.S. Ko, J.C. Goh, B.R. Choi, J.H. Choi, N.D. Kim and K. Chung, “A 14.1 inch full color AMOLED display with top emission structure and a-Si TFT backplane,” in SID Tech. Dig., pp.1538-1541, 2005.

[1.16] Atsushi Kohno, Toshiyuki Sameshima, Naoki Sano, Mitsunobu Sekiya, and Masaki Hara, “High performance polyrystalline silicon TFTs fabricated using

pulsed laser annealing and remote plasma CVD with low temperature processing," IEEE Trans. Electron Devices, vol. 42, pp. 251- 257, 1995.

[1.17] K. Zellama, P. Germain, S. Squelard, and J. C. Bourgoin, "Crystallization in amorphous silicon," *J. Appl. Phys.*, vol. 50, pp. 6995-7000, 1979.

[1.18] Miltiadis K. Hatalis and David W. Greve, "Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous silicon films," *J. Appl. Phys.*, vol. 63, pp. 2260-2266, 1988

[1.19] Zhonghe Jin, Keith Moulding, Hoi S. Kwok, and Man Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films," IEEE Trans. Electron Devices, vol. 46, pp.78-82, 1999.

[1.20] Hansuk Kim, J. Greg Couillard, and Dieter G. Ast, "Kinetic of silicide-induced crystallization of polycrystalline thin-film transistors fabricatied form amorphous chemical-vapor deposition silicon," Appl. Phys. Lett., vol. 72, pp803-805, 1998.

[1.21] Zhonghe Jin, Hoi S. Kwok, and Man Wong, "performance of thin-film transistors with ultrathin Ni-MILC polycrystalline silicon channel layers,"IEEE Electron Device Lett., vol. 20, pp. 167-169., 1999.

[1.22] Zhiguo Meng, Mingxiang Wang, and Man Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," IEEE Trans. Electron Devices, vol. 47, pp.404-409, 2000.

[1.23] G. K. Celler, H. J. Leamy, L. E.Trimble, and T. T. Sheng, "Annular grain structures in pulsed laser recrystallized Si on amorphous insulators, " Appl. Phys. Lett., vol. 9, pp. 425-427, 1981.

[1.24] N. M. Johnson, D. K. Giegelsen, H. C. Tuan, M. D. Moyer, and L. El Fennell, "Single-crystal silicon transistors in laser-crystallized thin films on bulk glass,"

IEEE Electron Device Lett., vol. 3, pp. 369-372, 1982.

[1.25] G. J. Willems, J. J. Poortmans, and H. E. Maes "A semiempirical model for the laser-induced molten zone in the laser recrystallization process," J. Appl. Phys., vol. 62, pp. 3408-3415, 1987.

[1.26] H. W. Lam, R. F. Pinizzotto, and A. F. Tasch, Jr, "Single Crystal Silicon-on-Oxide by a Scanning CW Laser Induced Lateral Seeding Process," J. Electrochem. Soc. Vol. 128, pp. 1981-1986, 1981.

[1.27] J. P. Colinge, E. Demoulin, D. Bensahel, and G. Auvert, "Use of selective annealing for growing very large grain silicon on insulator films," Appl. Phys. Lett., vol. 41, pp. 346-347, 1982.

[1.28] K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," IEEE Trans. Electron Devices, vol. 36, pp. 2868-2872, 1989.

[1.29] T. Sameshima, S. Usui, and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," IEEE Electron Device Lett., vol. 7, pp. 276-278, 1986.

[1.30] Y.F. Tang, S. R. P. Silva, and M. J. Rose, "Super sequential lateral growth of Nd:YAG laser crystallized hydrogenated amorphous silicon," Appl. Phys. Lett. Vol. 78, pp. 186-188, 2001.

[1.31] Akito Hara, Fumiyo Takeuchi, Michiko Takei, Katsuyuki Suga, Kenichi Yoshino, Mitsuru Chida, Yasuyuki Sano, and Nobuo Sasaki, "High-performance polycrystalline silicon thin film transistors on non-alkali glass produced using continuous wave laser lateral crystallization," Jpn. J. Appl. Phys., Part 2, vol. 41, pp.L311-L313, 2002.

[1.32] Bohuslav Rezek, Christoph E. Nebel, and Martin Stutzmann, "Polycrystalline

silicon thin films produced by interference laser crystallization of amorphous silicon," Jpn. J. Appl. Phys., Part2, vol. 38, pp. L1083-L1084, 1999.

[1.33] Y. Helen, R. Dassow, M. Nerding, K. Mourgues, F. Raoult, J.R. Kohler, T. Mohammed-Brahim, R. Rogel, O. Bonnaud, J.H. Werner, and H.P. Strunk, "High mobility thin film transistors by Nd:YVO4-laser crystallization," Thin Solid Films, vol. 383, pp. 143-146, 2001.

[1.34] Jia-Min Shieh, Zun-Hao Chen, Bau-Tong Dai, Yi-Chao Wang, Alexei Zaitsev, and Ci-Ling Pan, "Near-infrared femtosecond laser-induced crystallization of amorphous silicon," Appl. Phys. Lett., vol. 85, pp. 1232-1234, 2004.

[1.35] W. G. Hawkins, J. G. Black, and C. H. Griffiths, "Growth of single-crystal silicon islands on bulk fused silica by CO2 laser annealing," Appl. Phys. Lett., vol. 40, pp. 319-321, 1982.

[1.36] K. Masumo, N. Kato, and M. Kunigita, "Anisotropically High Mobility Polycrystalline Silicon by High-speed Scanning Beam Annealing," in AMLCD Tech. Dig., 1997, pp. 183-186.

[1.37] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Tsuda, and S. Nakano, "High Mobility Poly-Si TFT by a New Excimer Laser Annealing Method for Large Area Electronics," in IEDM Tech. Dig., 1991, pp.563-566.

[1.38] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, and M. J. Trainor, "Influence of melt depth in laser crystallized poly-Si thin film transistors," J. Appl. Phys., vol. 82, pp. 4086-4094, 1997.

[1.39] H. Kuriyama, T. Nohda, S. Ishida, T. Kuwahara, S. Noguchi, S. Kiyama, S. Tsuda, and S. Nakano, "Lateral grain growth of poly-Si films with a specific orientation by an excimer laser annealing method," Jpn. J. Appl. Phys., Part 1, vol. 32, pp. 6190-6195, 1993.

[1.40] H. Kuriyama, S. Kiyama, S. Noguchi, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, H. Kawata, M. Osumi, S. Tsuda, S. Nakano, and Y. Kuwano, "Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor," Jpn. J. Appl. Phys., vol. 30, pp. 3700-3703, 1991.

[1.41] A. T. Voutsas, A. M. Marmorstein, and R. Solanki, "The impact of annealing ambient on the performance of excimer-laser-annealed polysilicon thin-flim transistors," J. Electrochem. Soc., vol. 146, pp. 3500-3505, 1999.

[1.42] D. Toet, P. M. Smith, T. W. Sigmon, T. Takehara, C. C. Tsai, W. R. Harshbarger, and M. O. Thompson, "Laser crystallization and structural and structural characterization of hydrogenated amorphous silicon tin films," J. Appl. Phys., vol. 85, pp. 7914-7918, 1999.

[1.43] Jae-Hong Jeon, Juhn-Suk Yoo, Cheol-Min Park, Hong-Seok Choi, and Min-Koo Han, "A novel method for a smooth interface at poly-SiOx/SiO_2 by employing selective etching," IEEE Electron Device Lett., vol. 21, pp. 152-154, 2000.

[1.44] Maron Marmorstein, Apostolos T. Viutsas, and Rai Solanki, "A systematic study and optimization of parameters affecting grain size and surface roughness in excimer laser annealed polysilicon thin films," J. Appl. Phys., vol. 82, pp. 4303-4309, 1997.

[1.45] James S. Im, H. J. Kim, and Michael O. Thompson, "Phase transformation mechanisms involved on excimer laser crystallization of amorphous silicon films," Appl. Phys. Lett., vol. 63, pp. 1969-1971, 1993.

[1.46] James S. Im and H. J. Kim, "On the wuper lateral growth phenomenon observed in excimer lase-induced crystallization of thin Si films," Appl. Phys. Lett., vol. 64, pp. 2303-2305, 1994.

[1.47] M. O. Thompson, G.J. Galvin, J. W. Mayer, P. S. Peercy, J. M. Poate, D. C. Jacobson, A. G. Cullis, and N. G. Chew, "Melting temperature and explosive crystallization of amorphous silicon during pulsed laser irradiation," Phys. Rev. Lett., vol. 52, pp. 2360-2363, 1984.

[1.48] S. R. Stiffler, Michael O. Thompson, and P. S. Peercy, "Supercooling and nucleation of silicon after laser melting," Phys. Rev. Lett., vol. 60, pp. 2519-2522, 1988.

[1.49] S. R. Stiffler, M. O. Thompson, and P. S. Peercy, "Transient nucleation following pulsed-laser melting of thin silicon films," Phys. Rev. B, vol. 43, pp. 9851-9855, 1991.

[1.50] T. Eiumchotchawalit and James S. Im, "The mechanism of excimer laser-induced amorphization of ultra-thin Si films," Mat. Res. Soc. Symp. Proc., vol. 321, pp.725-730, 1994.

[1.51] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on SiO_2," Appl. Phys. Let., vol. 69, pp. 2864-2866, 1996.

[1.52] M. A. Crowder, P. G. Carey, P. M. Smith, R. S. Sposili, H. S. Cho, and J. S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," IEEE Electron Device Lett., vol. 19, pp. 306-308, 1998.

[1.53] P. C. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," Appl. Phys. Lett., vol. 79, pp. 1819-1821, 2001.

[1.54] L. Mariucci, R. Carluccio, A. Pecora, V. Foglietti, G. Fortunato, and P. Legagneux, D. Pribat et al., "Lateral growth control in excimer laser crystallized polysilicon," Thin Solid Films, vol. 337, pp. 137-142, 1999.

[1.55] C. H. Oh, M. Ozawa, and M. Matsumura, “A novel phase-modulated excimer-laser crystallization method of silicon thin film,” Jpn. J. Appl. Phys. Part 2, vol. 37, pp. L492-L495, 1998.

[1.56] R. Ishihara, and A. Burtsev, “Location Control of Large Grain Following Excimer-Laser Melting of Si Thin-Films,” Jpn. J. Appl. Phys. Part 1, vol. 37, pp. 1071-1075, 1998.

[1.57] K. Yamazaki, T. Kudo, K. Seike, D. Ichishima and C. G. Jin, “Double-pulsed laser annealing system and polycrystallization with green DPSS laser,” in AMLCD Tech. Dig., 2002, pp. 149-152.

[1.58] S. Sakuragi, T. Kudo, K. Yamazaki and T. Asano, ”High field effect mobility poly-Si TFTs fabricated by advanced lateral crystal growth process using double-pulsed laser annealing system,” in the proceeding of the 12th Internation Display Workshops, 2005, pp.965-968.

[1.59] C. H. Kim, I. H. Song, W. J. Nam, and M. K. Han, ”A poly-Si TFT fabricated by excimer laser recrystllization on floating active structure,” IEEE Electron Device Lett., vol. 23, pp. 325-327, 2002.

[1.60] A. Hara, F. Takeuchi, and N. Sasaki, ”Selective single-crystalline-silicon growth at the pre-defined active regions of TFTs on a glass by a scanning CW laser irradiation,” in IEDM Tech Dig, 2000, pp.209-212.

[1.61] A. Hara, M. Takei, F. Takeuchi, K. Suga, K. Yoshino, and M. Chida et al., ”High performance low temperature polycrystalline silicon thin film transistors on non-alkaline glass produced using diode pumped solid state continuous wave laser lateral crystallization,” Jpn. J. Appl. Phys. Part 1, vol. 43, ppl 1269-1276, 2004.

[1.62] M. Hatano, and T. Shiba, “Selectively enlarging laser crystallization technology for high and uniform performance poly-Si TFTs,” in SID Tech. Dig,

2002, pp. 158-161.

[1.63] M. Tai, M. Hatano, S. Yamaguchi, T. Noda, S K. Park, and T. Shiba et al., ”Performance of poly-Si TFTs fabricated by SELAX,” IEEE Trans. Electro Devices, vol. 51, pp. 934-939, June. 2004.

[1.64] Zhang, S.; Han, R.; Sin, J.K.O.; Chan, M., “A novel self-aligned double-gate TFT technology” *IEEE Electron Device Letters*, v 22, n 11, November, pp. 530-532, 2001.

[1.65] Sung, Man Young; Lee, Dae-Yeon; Ryu, Jang Woo; Kang, Ey Goo, “Electrical characteristics of single-silicon TFT structure with symmetric dual-gate for kink-effect suppression” *Solid-State Electronics*, v 50, n 5, May, pp. 795-799, 2006.

[1.66] Doyle, B.S. ; Datta, S.; Doczy, M.; Hareland, S.; Jin, B.; Kavalieros, J.; Linton, T.; Murthy, A.; Rios, R.; Chau, R., “High performance fully-depleted tri-gate CMOS transistors”, *IEEE Electron Device Letters*, v 24, n 4, April, pp. 263-265, 2003.

[1.67] Cho, Hyun-Jin; Plummer, James D., “High performance fully and partially depleted poly-Si surrounding gate transistors”, *Digest of Technical Papers - Symposium on VLSI Technology*, pp. 31-32 , 1999.

[1.68] Joon-ha Park, Ohy un Kim, “A Novel Self-Aligned Poly-Si With Field-Induced Drain Formed by the Damascene Process,”, IEEE Electron Device Lett., Vol. 26. No. 4, 2005.

Chapter 2

[2.1] S. D. Brotherton, “polycrystalline silicon thin film transistors,” *Semi-conduct. Sci. Technol.*, vol. 10, pp. 712-738, 1995

[2.2] Yasuhisa Oana, “Current and future technology of low-temperature

polycrystalline silicon TFT-LCDs," *Journal of the SID*, vol. 9, pp. 169-172, 2001.

[2.3] J. G. Blake, J. D. III Stevens, and R. Young, "Impact of low temperature polycrystalline silicon on the AMLCD market," *Solid State Tech.*, vol. 41, pp. 56-62, 1998.

[2.4] Mutsumi Kimura, Ichio Yudasaka, Sadao Kanbe, Hidekazu Kobayashi, Hiroshi Kiguchi, Shun-ichi Seki, Satoru Miyashita, Tatsuya Shimoda, Tokuro Ozawa, Kiyofumi Kitawada, Takashi Nakazawa, Wakao Miyazawa, and Hiroyuki Ohshima, "Low-temperature polycrystalline silicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," *IEEE Trans. Electron Devices*, vol. 46, pp. 2282-2288, 1999.

[2.5] Mark Stewart, Robert S. Howell, Leo Pires, and Miltiadis K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," *IEEE Trans. Electron Devices*, vol. 48, pp. 845-851, 2001.

[2.6] Wang, Hongmei ;Chan, Mansun; Jagar, Singh; Wang, Yangyuan; Ko, Ping K., "Submicron super TFTs for 3-D VLSI applications" *IEEE Electron Device Letters*, v 21, n 9, pp. 391-393, 2000.

[2.7] K. Zellama, P. Germain, S. Squelard, and J. C. Bourgoin, "Crystallization in amorphous silicon," *J. Appl. Phys.*, vol. 50, pp. 6995-7000, 1979.

[2.8] Zhonghe Jin, Keith Moulding, Hoi S. Kwok, and Man Wong, "The effects of extended heat treatment on Ni induced lateral crystallization of amorphous silicon thin films," *IEEE Trans. Electron Devices*, vol. 46, pp. 78-82, 1999.

[2.9] S. D. Brotherton, D. J. McCulloch, J. P. Gowers, J. R. Ayres, C. A. Fisher, and F. W. Rohlfing, "Excimer laser crystallization of polycrystalline silicon TFTs for AMLCDs," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q7.1.1-Q7.1.12, 2000.

[2.10] A. Hara, Y. Mishima, T. Kakehi, and F. Takeuchi," High performance

polycrystalline silicon TFTs on a glass by stable scanning CW laser lateral crystallization," in *IEDM Tech. Dig.*, pp. 747-750, 2001.

[2.11] P. M. Smith, P. G. Carey, and T. W. Sigmon, "Excimer laser crystallization and doping of silicon films on plastic substrates," *Appl. Phys. Lett.*, vol. 70, pp. 342-344, 1997.

[2.12] M. O. Thompson, G. J. Galvin, J. W. Mayer, P. S. Peercy, J. M. Poate, D. C. Jacobson, A. G. Cullis, and N. G. Chew, "Melting temperature and explosive crystallization of amorphous silicon during pulsed laser irradiation," *Phys. Rev. Lett.*, vol. 52, pp. 2360-2363, 1984.

[2.13] S. R. Stiffler, Michael O. Thompson, and P. S. Peercy, "Supercooling and nucleation of silicon after laser melting," *Phys. Rev. Lett.*, vol. 60, pp. 2519-2522, 1988.

[2.14] James S. Im and H. J. Kim, "On the super lateral growth phenomenon observed in excimer laser-induced crystallization of thin Si films," *Appl. Phys. Lett.*, vol. 64, pp. 2303-2305, 1994.

[2.15] Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on SiO_2," *Appl. Phys. Lett.*, vol. 69, pp. 2864-2866, 1996.

[2.16] James S. Im, Robert S. Sposili, and M. A. Crowder, "Single-crystal Si films for thin-film transistor devices," *Appl. Phys. Lett.*, vol. 70, pp. 3434-3436, 1997.

[2.17] M. A. Crowder, P. G. Carey, P. M. Smith, Robert S. Sposili, Hans S. Cho, and James S. Im, "Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification," *IEEE Electron Device Lett.*, vol. 19, pp. 306-308, 1998.

[2.18] Hans S. Cho, Dongbyum Kim, Alexander B. Limanov, Mark A. Crowder, and James S. Im, "Sequential lateral solidification of ultra-thin a-Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.9.1-Q9.9.6, 2000.

[2.19] Y. H. Jung, J. M. Yoon, M. S. Yang, W. K. Park, H. S. Soh, H. S. Cho, A. B. Limanov, and J. S. Im, "The dependence of poly-Si TFT characteristics on the relative misorientation between grain boundaries and the active channel," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.14.1-Q9.14.6, 2000.

[2.20] Y. H. Jung, J. M. Yoon, M. S. Yang, W. K. Park, H. S. Soh, H. S. Cho, A. B. Limanov, and J. S. Im, "Low temperature polycrystalline Si TFTs fabricated with directionally crystallized Si film," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q8.3.1-Q8.3.6, 2000.

[2.21] M. A. Crowder, Robert S. Sposili, A. B. Limanov, and James. S. Im, "Sequential lateral solidification of PECVD and sputter deposited a-Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.7.1-Q9.7.6, 2000.

[2.22] M. A. Crowder, A. B. Limanov, and James. S. Im, "Sub-grain boundary spacing in directionally crystallized Si films obtained via sequential lateral solidification," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q9.6.1-Q9.6.6, 2000.

[2.23] Paul Ch. Van der Wilt, Ryoichi Ishihara, and Jurgen Bertens, "Location-controlled large-grains in near-ablation excimer-laser crystallized silicon films," *Mat. Res. Soc. Symp. Proc.*, vol. 621, Q7.4.1-Q7.4.6, 2000.

[2.24] Barry D. van Dijk, Paul Ch. Van der Wilt, G. J. Bertens, Lis.K. Nanver, and Ryoichi Ishihara, "Single-crystal thin film transistor by grain-filter location-controlled excimer-laser crystallization," *Mat. Res. Soc. Symp. Proc.*, vol. 685E, D12.3.1-D12.3.6, 2001.

[2.25] Paul Ch. van der Wilt, B. D. van Dijk, G. J. Bertens, R. Ishihara, and C. I. M. Beenakker, "Formation of location-controlled crystalline islands using substrate-embedded seeds in excimer-laser crystallization of silicon films," *Appl. Phys. Lett.*, vol. 79, pp. 1819-1821, 2001.

[2.26] Chang-Ho Oh, Motohiro Ozawa, and Masakiyo Matsumura, "A novel

phase-modulated excimer-laser crystallization method of silicon thin films," *Jpn. J. Appl. Phys. Part 2*, vol. 37, pp. L492-L495, 1998.

[2.27] Chang-Ho Oh and Masakiyo Matsumura, "Preparation of position-controlled crystal- silicon island arrays by means of excimer-laser annealing," *Jpn. J. Appl. Phys. Part 1*, vol. 37, pp. 5474-5479, 1998.

[2.28] Motohiro Ozawa, Chang-Ho Oh, and Masakiyo Matsumura, "Two-dimensionally position-controlled excimer-laser-crystallization of silicon thin films on glassy substrate," *Jpn. J. Appl. Phys. Part 1*, vol. 38, pp. 5700-5705, 1999.

[2.29] Masakiyo Matsumura and Chang-Ho Oh, "Advanced excimer-laser annealing process for quasi single-crystal silicon thin-film devices," *Thin Solid Films*, vol. 337, pp. 123-128, 1999.

[2.30] Chang-Ho Oh and Masakiyo Matsumura, "A proposed single grain-boundary thin-film transistor," *IEEE Electron Device Lett.*, vol. 22, pp. 20-22, 2001.

[2.31] H. J. Kim and James S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," *Appl. Phys. Lett.*, vol. 68, pp. 1513-1515, 1996.

[2.32] H. J. Kim and James S. Im, "Optimization and transformation analysis of grain-boundary-location-controlled Si films," *Mat. Res. Soc. Symp. Proc.*, vol. 397, pp. 401-406, 1996.

[2.33] L. Mariucci, R. Carluccio, A. Pecora, V. Foglietti, G. Fortunato, P. Legagneux, D. Pribat, D. Della Sala, and J. Stoemenos, "Lateral growth control in excimer laser crystallized polysilicon," *Thin Solid Films*, vol. 337, pp. 137-142, 1999.

[2.34] Jae-Hong Jeon, Min-Cheol Lee, Sang-Hoon Jung, and Min-Koo Han, "Excimer laser recrystallization of a-Si employing aluminum masking window," *Mat. Res. Soc. Symp. Proc.*, vol. 609, A25.3.1-A25.3.5 , 2000.

[2.35] Jae-Hong Jeon, Min-Cheol Lee, Kee-Chan Park, and Min-Koo Han, "A new polycrystalline silicon TFT with a single grain boundary in the channel," *IEEE Electron Device Lett.*, vol. 22, pp. 429-431, 2001.

[2.36] Jae-Hong Jeon, Min-Cheol Lee, Kee-Chan park, and Min-Koo Han, "New excimer laser recrystallization of poly-Si for effective grain growth and grain boundary arrangement," *Jpn. J. Appl. Phys. Part 1*, vol. 39, pp. 2012-2014, 2000.

[2.37] Cheon-Hong Kim, Juhn-Suk Yoo, In-Hyuk Song and Min-Koo Han, "Excimer laser recrystallization of selectively floating a-Si active layer for large-grained poly-Si film," *Mat. Res. Soc. Symp. Proc.*, vol. 664, A6.11.1-A6.11.6 , 2001.

[2.38] Cheon-Hong Kim,In-Hyuk Song,Woo-Jin Nam, and Min-Koo Han, "Excimer laser recrystallization of selectively floating a-Si thin film," *J. Non-Cryst. Solids*, vol. 299-302, pp. 721-725, 2002.

[2.39] Cheon-Hong Kim, In-Hyuk Song, Woo-Jin Nam, and Min-Koo Han, "A poly-Si TFT fabricated by excimer laser recrystallization on floating active structure," *IEEE Electron Device Lett.*, vol. 23, pp. 325-327, 2002.

[2.40] Do-Hyun Choi, Kazuhiro Shimizu, Osamu Sugiura, and Masakiyo Matsumura, "Drastic enlargement of grain size of excimer-laser-crystallized polysilicon films," *Jpn. J. Appl. Phys. Part 1*, vol. 31, pp. 4545-4549, 1992.

[2.41] Do-Hyun Choi, Eiichi Sadayuki, Osamu Sugiura, and Masakiyo Matsumura, "Lateral growth of poly-Si film by excimer laser and its thin film transistor application," *Jpn. J. Appl. Phys. Part 1*, vol. 33, pp. 70-74, 1994.

[2.42] Min Cao, Somit Talwar, K. Josef Kramer, Thomas W. Sigmon, and Krishna, C. Saraswat, "A high-performance polysilicon thin-film transistor using XeCl excimer laser crystallization of pre-patterned amorphous Si films," *IEEE Trans. Electron Devices*, vol. 43, pp. 561-567, 1996.

[2.43] G. K. Giust and T. W. Sigmon, “Comparison of excimer laser recrystallized prepatterned and unpatterned silicon films on SiO_2,” *J. Appl. Phys.*, vol. 81, pp. 1204-1211, 1997.

[2.44] G. K. Giust and T. W. Sigmon, “Performance improvement obtained for thin-film transistors fabricated in prepatterned laser-recrystallized polysilicon,” *IEEE Electron Device Lett.*, vol. 18, pp. 296-298, 1997.

[2.45] Akito Hara and Nobuo Sasaki, “Use of necked-down areas to control nucleation site and direction of solidification of polycrystalline silicon using excimer laser crystallization,” *J. Appl. Phys.*, vol. 88, pp. 3349-3353, 2000.

[2.46] Ryoichi Ishihara, Artyom Burtsev, and Paul F. A. Alkemade, “Location-control of large Si grains by dual-beam excimer-laser and thick oxide portion,” *Jpn. J. Appl. Phys. Part 1*, vol. 39, pp. 3873-3878, 2000.

[2.47] M .H .Lee, S. J. Moon, M. Hatano, K. Suzuki, and C. P. Grigoropoulos, “Relationship between fluence gradient and lateral grain growth in spatially controlled excimer laser crystallization of amorphous silicon films,” *J. Appl. Phys.*, vol. 88, pp. 4994-4999, 2000.

[2.48] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, “Capillary waves in pulsed excimer laser crystallized amorphous silicon,” Appl. Phys. Lett., vol. 68, pp. 2138-2140, 1996.

[2.49] Alert W. Wang, Krishna C. Saraswat, “A Strategy for Modeling of Variations due to Grain Size in Polycrystalline Thin-Film Transistors,” IEEE Trans. Electron Device, vol. 47, No. 5, May, 2000.

[2.50] N. Lifshitz, S. Luryi, “Enhanced Channel Mobility in Polysilicon Thin Film Transistors,” IEEE Electron Device Lett., vol. 15, No. 8, August, 1994.

Chapter 3

[3.1] A. Hara, F. Takeuchi, and N. Sasaki, "Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors," J. Appl. Phys., vol. 91, pp. 708-714, 2002.

[3.2] Jae-Hong Park and Chul-Ju Kim, "A Study on the Fabrication of a Mulgate/Multichannel Polysilicon Thin Film Transistor," Jpn. J. Appl. Phys., vol. 36, pp. 1428-1432, 1997.

[3.3] Y.-C. Wu, T.-C. Chang, Po-T. Liu, C.-Wei Chou, Y.-C. Wu, C.-Hao Tu, and C.-Y. Chang, "Reduction of Leakage Current in Metal-Induced Lateral Crystallization Polysilicon TFTs With Dual-Gate and Multiple Nanowire Channels," IEEE Electron Device Lett., vol. 26, no. 9, 2005.

[3.4] Y.-C. Wu, T.-C. Chang, P.-T. Liu, C.-W. Chou, Y.-C. Wu, C.-H. Tu, and C.-Y. Chang, "High-Performance Metal-Induced Lateral-Crystallization Polysilicon Thin-Film Transistors With Multiple Nanowire Channels and Multiple Gates," IEEE Trans. On Nanotech., vol. 5, no. 3, 2006.