國 立 交 通 大 學

電子工程學系 電子研究所

碩 士 論 文

在二氧化鉿為基底之高介電係數閘極介電層中的載子捕捉與逃逸的電性行為

Charge Trapping and De-trapping Behaviors in Hf-Base High-k Gate Dielectrics

研 究 生：詹效諭

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中 華 民 國 九十七 年 八 月

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研 究 生：詹効諭　　Student：Shiao-Yu Chan

指導教授：簡昭欣 博士　　Advisor：Dr. Chao-Hsin Chien

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摘要

隨著 CMOS 技術急速的微縮到奈米技術點，傳統以二氧化矽或氮氧化矽為閘極介電層將達到物理與電性的極限。主要的問題是量子效應引發的直接穿隧電流，導致無法接受的大量載子穿隧超薄的氧化層。高介電係數的材料當閘極介電層，它可以提供較厚的物理厚度並且得到想要的等效電性氧化層厚度，而二氧化鉿為基底的高介電係數閘極介電層已經被認為最有希望的替補者。不過，以二氧化鉿為基底的高介電係數閘極介電層具有相當嚴重的可靠度問題—臨界電壓的不穩定性，起因於高介電層早已存在的主體缺陷中的載子捕捉與逃逸現象。另一方面，我們也可以利用一些方法來減緩元件的微縮，而遷移率的增加最有用的方法之一。遷移率增加的技術提供了有效且必要的方法，讓操作電壓和功率的輸出降低，而不會失去電路的表現。

首先，高拉應力的接觸蝕刻停止層(contact etch stop layer (CESL))，對 N 型金氧半場效電晶體可以很明顯的增加電子的遷移率和打開的電流，而且它是最熱門的遷移率增加技術之一。所以我們會探討，拉應力效應在 N 型金氧半場效電

晶體的基本的電性特性和載子捕捉的情形。再來，利用適合(fit)臨界電壓的偏移對施加應力(stress)/恢復(recovery)時間的數據，我們可以研究，在 N 和 P 型金氧半場效電晶體，載子捕捉和逃逸的物理機制。最後，我們要討論，氟的效應在 P 型金氧半場效電晶體的基本的電性特性和負偏壓高溫度不穩定性(negative bias temperature instability，NBTI）。此外，我們利用脈波 I-V 的量測方法，來研究快速載子捕捉的情形。

Charge Trapping and De-trapping Behaviors in Hf-Base High-k Gate Dielectrics

Student：Shiao-Yu Chan Advisor：Dr. Chao-Hsin Chien

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University

Abstract

As COMS devices are scaled aggressively into nanometer regime, the conventional SiO2 or SiON gate dielectrics are approaching their physical and electrical limits. The major issue is the intolerably huge leakage current caused by the direct tunneling of carriers through the ultrathin oxide. High permittivity materials as gate dielectrics have been proposed to offer thicker dielectric physical thickness with the desired equivalent oxide thickness in electrical properties and Hf-base high-k gate dielectrics have been recognized as the most promising candidates. However, the Hf-based high-k gate dielectrics are known to suffer from the reliability concern of threshold voltage instability due to the charge trapping and de-trapping in the pre-existing bulk traps in Hf-based high-k gate dielectrics. On the other hand, in order to retard the downscaling of Si based CMOS device, mobility enhancement is one of the most useful methods. Mobility enhancement techniques represent an effective and essential way to reduce V_{dd} and resulting power consumption without losing circuit performance.

First, one of the most popular mobility enhancement technologies is using high

tensile-stress contact etch stop layer (CESL), which can obviously improve electron mobility and I_{ON} for nMOSFETs. The basic electrical properties and the charge trapping condition of strain effect are investigated in nMOSFETs. Next, the physical mechanisms of charge trapping and de-trapping can be investigated by fitting the data of the threshold voltage shifts versus stress/recovery time in nMOSFETs and pMOSFETs. Final, the basic electrical properties and the negative bias temperature instability of fluorine effect are investigated in pMOSFETs. Moreover, the fast charge trapping is investigated by pulsed I-V measurement.

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Chapter 1
Introduction

1.1 Hf-base High-k Gate Dielectrics

According to Moore's law, the continuous downscaling of the dimension of Si based CMOS device has approaching the physical limit of conventional SiO_2-based ultrathin oxides. In recent years, the equivalent oxide thickness of silicon oxynitride SiON has reduced below 2.0 nm that lead to the serious concerns gate dielectric integrity, reliability issues, and stand-by power consumption. However, one of the major challenges to overcome is the rapidly-increasing tunneling gate leakage current with the downscaling of the equivalent oxide thickness. From ITRS roadmap in Fig. 1-1 [1], the two Jg of LSTP and high-performance logic curves cross shortly before or at 2008, and hence, for 2008 and beyond, the leakage current limit cannot be met using silicon oxy-nitride because of direct tunneling.

In order to solve the tunneling current and power consumption in the ultrathin oxides, high permittivity materials as gate dielectrics have been proposed to offer thicker dielectric physical thickness with the desired equivalent oxide thickness in electrical properties. Table 1-1 summarizes the electrical properties of several high-k materials [2], and Fig. 1-2 the bandgap and band offset of these high-k materials with respect to Si [3]. Among these investigated high-k gate dielectrics, Hf-base high-k gate dielectrics have been recognized as the most promising candidates due to their moderate dielectric constant (20~25), large energy bandgap (5.7~6.0eV), high conduction band offset (1.5~1.9eV), excellent thermal stability on the Si substrate (950℃). However, several issues in high-k technology are believed to retard its development such as

mobility degradation as a result of soft optical phonon scattering and threshold voltage instability by charge trapping and de-trapping.

On the other hand, mobility enhancement techniques represent an effective and essential way to reduce V_{dd} and resulting power consumption without losing circuit performance. One of the most popular technologies is using high tensile-stress contact etch stop layer (CESL), which can obviously improve electron mobility and I_{ON} for nMOSFETs [4].

1.2 Threshold Voltage Instability in the High-k Gate Dielectrics

Compared with SiO_2 and SiON, there are plenty of pre-existing bulk traps in the high-k gate dielectrics, and this is an intrinsic issue related to specific properties or crystal structure of high-k gate dielectrics, despite the deposition technique or process condition. Because of this characteristic, the pre-existing high-k bulk defects could lead to undesired transport through the dielectrics inducing gate leakage. Moreover, charge trapped by these defects would cause the continued threshold voltage shift, drain current and transconductance degradation during operation. As the gate bias is positive (negative), the injected electrons (holes) through the interfacial oxide would be trapped by the pre-existing bulk defects of the HfO_2 layer. As the gate bias is negative (positive), these trapped electrons (holes) would be relaxed through the interfacial oxide to the Si conduction band in high-k nMOSFETs.

According to the threshold voltage shift and the drain current degradation of the high-k devices during operation, we could build the models which can fit the experiment results and conform to the physical mechanisms of charge trapping and de-trapping. There have been many models built in recent years. Zafar et al. predicted that Vt would shift with power law dependence in the initial stages of stressing whereas

Vt would become constant at long stressing times [5]. Shanware et al. predicted that Vt would shift with logarithmic dependence [6]. These models above would be built by static Id-Vg measurement, and therefore the detected charge carriers in high-k gate dielectrics would only belong to slow traps.

As has been reported recently, the charge trapping in high-k gate dielectrics comprise slow and fast trapping processes. The slow high-k traps have been widely discuss from the hysteresis of C-V curves and the threshold voltage shift of static Id-Vg characteristics. Moreover, the fast high-k traps have been proposed to investigate by the pulse I-V technique and charge pumping method. It is reported that the fast electron trapping is a significant source of device DC performance degradation [7]. The fast high-k traps can instantly capture and emit the charge carriers by tunneling through the thin interfacial oxide [8]-[11]. The tunneling model through the thin interfacial oxide is similar to that of tunneling into near-interface oxide traps in the heavily-irradiated SiO_2 that has already been studied and proposed [12] [13]. These near-interface oxide traps are defined as the oxide traps located near the interface that can instantly exchange charge carriers with underlying Si substrate through direct tunneling [14] [15].

This thesis will concentrate on analyzing the data to better understand the fundamental characteristic and the physical mechanisms of charge trapping and de-trapping in Hf-based high-k gate dielectrics. Moreover, the strain effect and the fluorine effect are also investigated completely.

1.3Dissertation Organization

The organization of this dissertation is briefly described below. Chapter 2 studies the basic characteristics and reliability discussion of strain effect by CESL. The fast trap behavior is discussed under strain effect. Chapter3 discusses the electron trapping and de-trapping behavior under positive bias temperature instability (PBTI) and dynamic PBTI stress. The electron trapping/de-trapping model and the meaning of the parameters by fitting are discussed. The fast trap in nMOSFETs is discussed under various temperatures. Chapter 4 discusses the hole trapping and de-trapping behavior under constant voltage stress (CVS) and recovery. The hole trapping/de-trapping model and the meaning of the parameters by fitting are discussed. The basic characteristics and negative bias temperature instability discussion of fluorine effect are discussed. The fast trap in pMOSFETs is discussed under various temperatures and fluorine effect.

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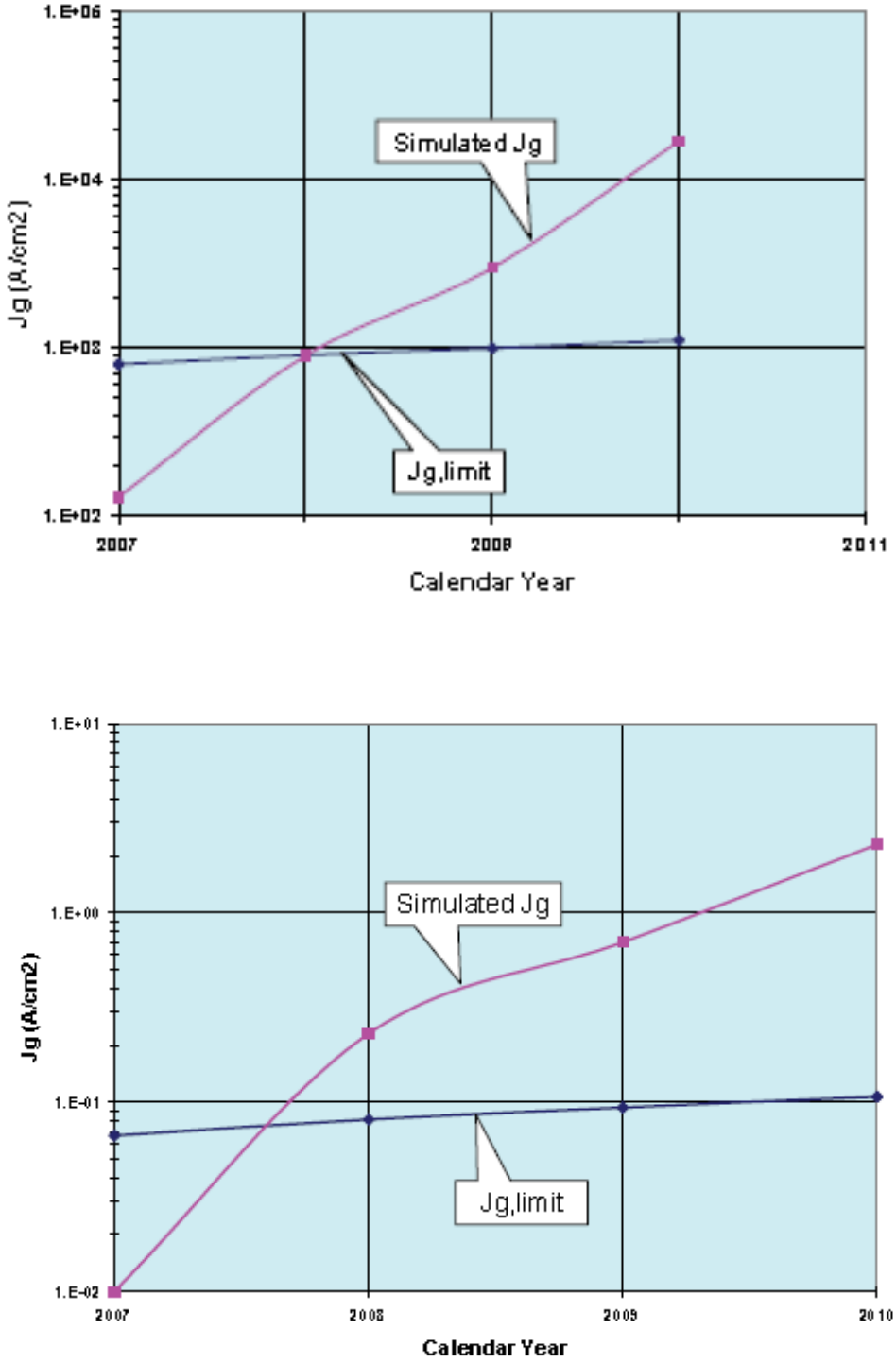

Fig.1-1 (a) High-Performance Logic: $J_{g,limit}$ versus simulated gate leakage current density for SiON gate dielectric. (b) LSTP: Jg,limit versus simulated gate leakage current density for SiON gate dielectric. [1]

Dielectric	*Dielectric constant (bulk)*	*Bandgap* (eV)	*Conduction band offset* (eV)	*Leakage current reduction w.r.t. SiO_2*	*Thermal stability w.r.t. silicon (MEIS data)*
Silicon dioxide (SiO_2)	3.9	9	3.5	N/A	>1050°C
Silicon nitride (Si_3N_4)	7	5.3	2.4		>1050°C
Aluminum oxide (Al_2O_3)	~10	8.8	2.8	10^2–10^3×	~1000°C, RTA
Tantulum pentoxide (Ta_2O_5)	25	4.4	0.36		Not thermodynamically stable with silicon
Lanthanum oxide (La_2O_3)	~21	6*	2.3		
Gadolinium oxide (Gd_2O_3)	~12				
Yttrium oxide (Y_2O_3)	~15	6	2.3	10^4–10^5×	Silicate formation
Hafnium oxide (HfO_2)	~20	6	1.5	10^4–10^5×	~950°C
Zirconium oxide (ZrO_2)	~23	5.8	1.4	10^4–10^5×	~900°C
Strontium titanate ($SrTiO_3$)		3.3	−0.1		
Zirconium silicate ($ZrSiO_4$)		6*	1.5		
Hafnium silicate ($HfSiO_4$)		6*	1.5		

*Estimated value.

Table 1-1 Summarized material and electrical properties of various selected high-k gate dielectrics [2].

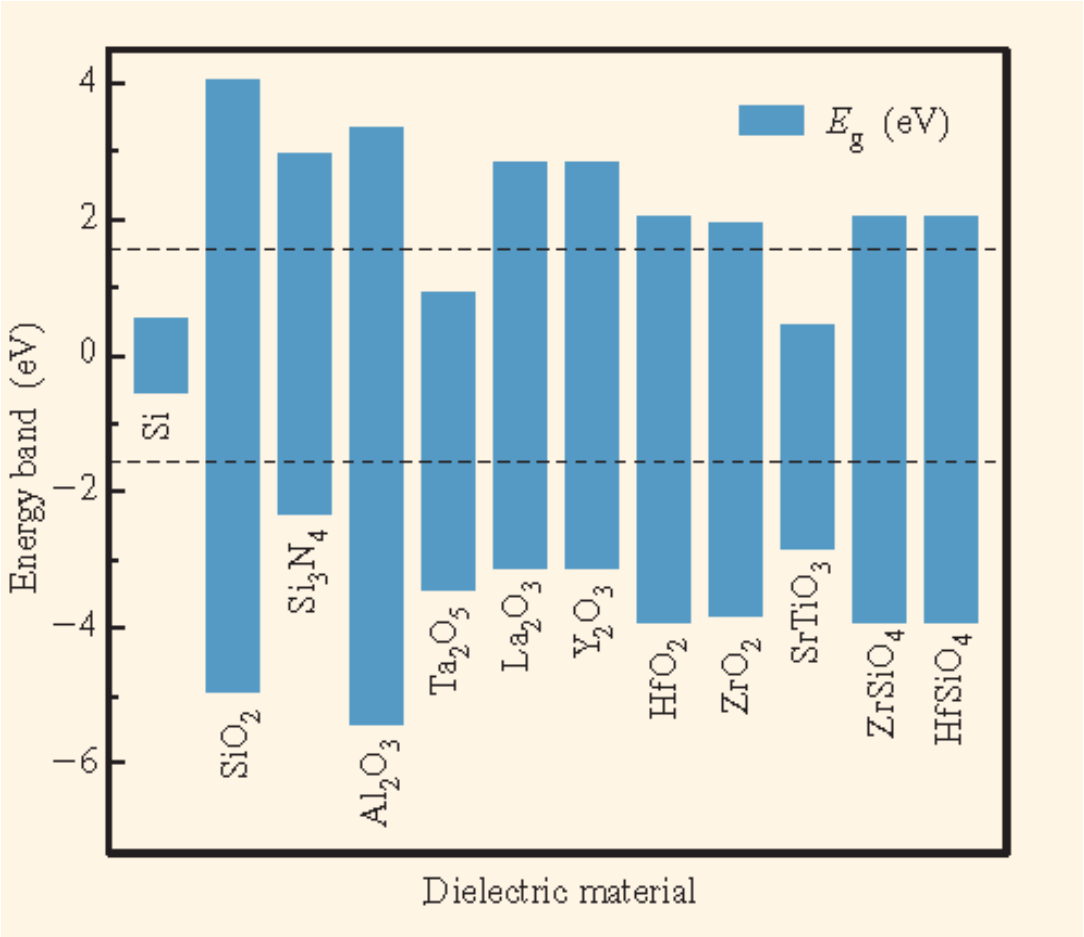

Fig 1-2 Bandgap and band alignment of various high-k gate dielectrics with respect to silicon. The dashed line represents 1 eV above/below the conduction/valence bands, which indicate the minimum barrier height to suppress the gate leakage current [3].

Chapter 2

Contact etchant stopping layer in nMOSFETs with HfO_2/SiO_2 High-k Gate Stacks

2.1 Introduction

As conventional SiO_2-based ultrathin oxides are scaling down, the rapidly-increasing tunneling gate leakage current has been a major challenge. In order to retard the downscaling of Si based CMOS device, mobility enhancement is one of the most useful methods. Mobility enhancement techniques represents an effective and essential way to reduce Vdd and resulting power consumption without losing the circuit performance, relieving the burden of gate dielectric scaling. There are many methods of mobility enhancement: a) channel-strain engineering, b) substrate and channel orientations ((100) or (110)), and c) new channel materials (SiGe, Ge and III-V). The channel-strain engineering comprises biaxial and uniaxial strain (tensile or compressive). The biaxial tensile strain uses the technique of the so-called SiGe-relaxed buffer or virtual substrate [1]-[3]. Recently, this technique has also been successfully implemented on SOI wafers [4]. In contrast, it is difficult to fabricate a biaxial compressive strain in silicon; it's very beneficial effect to holes has been demonstrated with SiGe channels in [5]. The uniaxial tensile strain in the channel can be produced with SiC epitaxial source–drain regions and with the contact-etch-stop-layer (CESL) nitride layer. The uniaxial compressive strain can be obtained with SiGe epitaxial source–drain regions [6], with a SiGe stressor located under the channel region [7], and with CESL. The contact-etch stop layer nitride layer can induce both tensile strain for nMOSFETs and compressive strain for pMOSFETs, so that dual stress liner with SiN capping is one of the most popular

techniques of mobility enhancement.

In this chapter, the high-k nMOSFETs with the contact-etch-stop-layers that induce tensile strain in the channel are introduced. The strain effect can be realized by basic characteristics in section 2.3. In section 2.4, the difference of the charge trapping between the stained and unstrained devices will be studied during the positive bias stress. Finally, the transient charge carriers in stain effect will be analyzed by pulsed I-V techniques in section 2.5.

2.2 Device Fabrication

nMOSFET devices with the poly-Si/HfO_2/SiON high-k gate stacks were fabricated using the standard CMOS process technology. The interfacial oxide (～1.0 nm) was formed by oxide rapid thermal anneal (RTA) at 800℃ in N_2O ambient with 30s, followed by the deposition of the HfO_2 (～3.0 nm) high-k gate dielectric using atomic layer deposition (ALD) technique. The 200 nm poly-Si was deposited by low pressure chemical vapor deposition (LPCVD). After gate definition, spacer formation, and S/D implantation, the tensile strain induced by SiN capping layer was deposited by plasma chemical vapor deposition (PECVD). The capping nitride layers were divided into three kinds of thickness such as 200 nm, 300 nm and without SiN. The equivalent oxide thickness of above mentioned high-k gate stack was extracted to be 2.0～2.5 nm by using C-V measurement. The structure of the devices are shown in Fig. 2-1

2.3 Basic Characteristic

Fig. 2-2 (a) (b) show I_d-V_g and G_m-V_g curves of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in different thickness of capping nitride layers. From

Id-Vg curves, as the thickness of capping nitride layer was thicker, drain current would be larger. In G_m-V_g curve, the same phenomenon would also be occurred. Turn-on current which varies with gate voltage also represented larger in thicker nitride layer in Fig. 2-3. The reason of improvement of the stained devices is mobility enhancement as a result of electron effective mass. The channel stressed by capping nitride layer would induce the electrons of 2-fold valley with lighter transport effective mass to increase. As the inverted electrons with lighter effective mass increase, the mobility of the strained devices will enhance. Fig. 2-4 shows I_{cp}-V_{base} curves by charge pumping method of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in different thickness of capping nitride layers. From I_{cpmax} of I_{cp}-V_{base} curves, the interface trap density could be obtained. Moreover, the interface trap density of the strained devices was smaller than that of the unstrained device because of hydrogen passivation by capping nitride layers of PECVD. From Fig. 2-5, the $G_{m,max}$ enhancement could decrease with gate length increasing because of CESL belonged to local strain [8].

2.4 Positive Bias Temperature Instability (PBTI) stress

Threshold voltage instability induced by charge trapping has been recognized as one of the critical reliability issues in high-k gate dielectrics, especially for nMOSFETs under substrate electron injection conditions [9]. Fig. 2-6 shows threshold voltage shift of nMOSFETs as a function of the stress time in difference thickness of capping nitride layers. The V_t shift of strained devices showed more serious than that of unstrained devices. Moreover, thicker capping nitride layers would increase more V_t shift. The physical mechanism or the modeling of the fitting lines in Fig. 2-6 will be discussed in chapter 3. In order to confirm the reason of the more V_t shift of the strained devices, the comparing of trapped energy level by Frenkel-Poole (F-P) fitting and the barrier height

for electrons from Si substrate by Fowler-Nordheim (F-N) tunneling fitting between the unstrained and the strained devices should be extracted. Fig. 2-7 shows $\ln(J_G/E_{eff})$ as a function of $E_{eff}^{1/2}$ in the (a) unstrained and (b) strained devices. The curves of the two plots followed Frenkel–Poole emission as indicated by a good linear fit to the experimental data. Then, the trapped energy levels could be obtained from the y-axis intercept (Eq. (2.1)). It could be found that almost the same trapped energy levels of the unstrained and strained devices. Fig. 2-8 shows the $\ln(J_G/E_{eff})$ as a function of $1/E_{eff}$ in unstrained and strained devices. The slops of the lines fit to the experiment data could be obtained the barrier height (Eq. (2.2)). The similar slope represented the similar barrier height in unstrained and strained devices. Thus, the trapped energy level and the barrier height for electrons from Si substrate are not change by strain. It can be assumed that the more V_t with increasing capping nitride layer is due to the generated bulk traps of HfO_2 by stain. Moreover, the thicker capping nitride layer represents the more generated bulk traps of HfO_2.

Frenkel-Poole emission:

$$J = B \cdot a \cdot E_{ox} \cdot \exp\left(\frac{-q(\Phi_T - \sqrt{aqE_{ox}/\pi\varepsilon_{HfO_2}\varepsilon_0}}{kT}\right); B = q\mu N_T; a = \frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2}}$$

$$\ln(J/E_{ox}) = \frac{-q\sqrt{aq/\pi\varepsilon_{HfO_2}\varepsilon_0}}{kT}\sqrt{E_{ox}} - \left[\frac{q\Phi_T}{kT} + \ln(aB)\right] \quad (2.1)$$

F-N tunneling: $J \approx E_{ox}^2 \cdot \exp(-B/E_{ox})$

$$B(slope) = -\frac{8\pi(2qm^*)^{1/2}}{3h}\Phi^{1/2} \quad (2.2)$$

Fig. 2-9 shows the drain current degradation of nMOSFETs as a function of the stress/recovery time with a fixed stress/recovery voltage +2.0V/0V in difference thickness of capping nitride layers. From every single line in Fig. 2-9, the charge trapping and de-trapping behavior changed since the trapped charge had not been completely removed at weak recovery voltages during previous recovery cycles. Moreover, the trapped electrons and the residual electrons during stress/recovery time of strained device would induce more drain current degradation than that of unstrained device.

2.5 Pulsed I-V Techniques and Fast Trap Behaviors

Fig. 2-10 shows I_d-V_d curves of (a) unstrained (b) SiN = 200nm (c) SiN = 300nm devices by two measurement methods: DC ramp and pulsed I-V. The measurement time of the conventional DC ramp measurement is about several milliseconds to seconds. The pulse width of the pulsed I-V measurement we used is 100ns and raising/falling time is 20ns. Thus, the different of $I_{d,sat}$ by two methods could be the charge loss with the capture time ranging from 100ns to several milliseconds. The charge loss decreased in thinner capping nitride layer device and increased in thicker capping nitride layer device. The behavior of these fast traps would be a little different from that of the slow traps by PBTI measurement. It can be assumed that the hydrogen passivation is dominant in thinner capping nitride layer device and the trap generation is dominant as the capping nitride layer is thicker. Fig. 2-11 shows $I_{d,sat}$ as a function of stress time ranging several nanoseconds to100ns by single pulse measurement. The detected traps would be more close to the interface of Si/SiON. Thus, the result are almost the same with the interface state by charge pumping measurement and the reason of the result can be also assumed the hydrogen passivation.

2.6 Summary

The contact-etch-stop-layer (CESL) is one of mobility enhancement methods and it can induce tensile strain to improve mobility for nMOSFETs. In our data, the strained devices could improve the electrical characteristics of NMOS, but they would induce more threshold voltage shift in high-k material. By F-P and F-N tunneling fitting, the trapped energy levels and the barrier heights of stained and unstrained devices are almost the same. Thus, we conclude that the strain effect induces bulk traps generated in HfO_2. Form the transient effect by pulsed I-V, the competition of hydrogen passivation and trap generated by strain can be found. The charge loss detected by single pulsed ranging several nanoseconds of strained and unstrained devices represents the interface states improvement due to hydrogen passivation.

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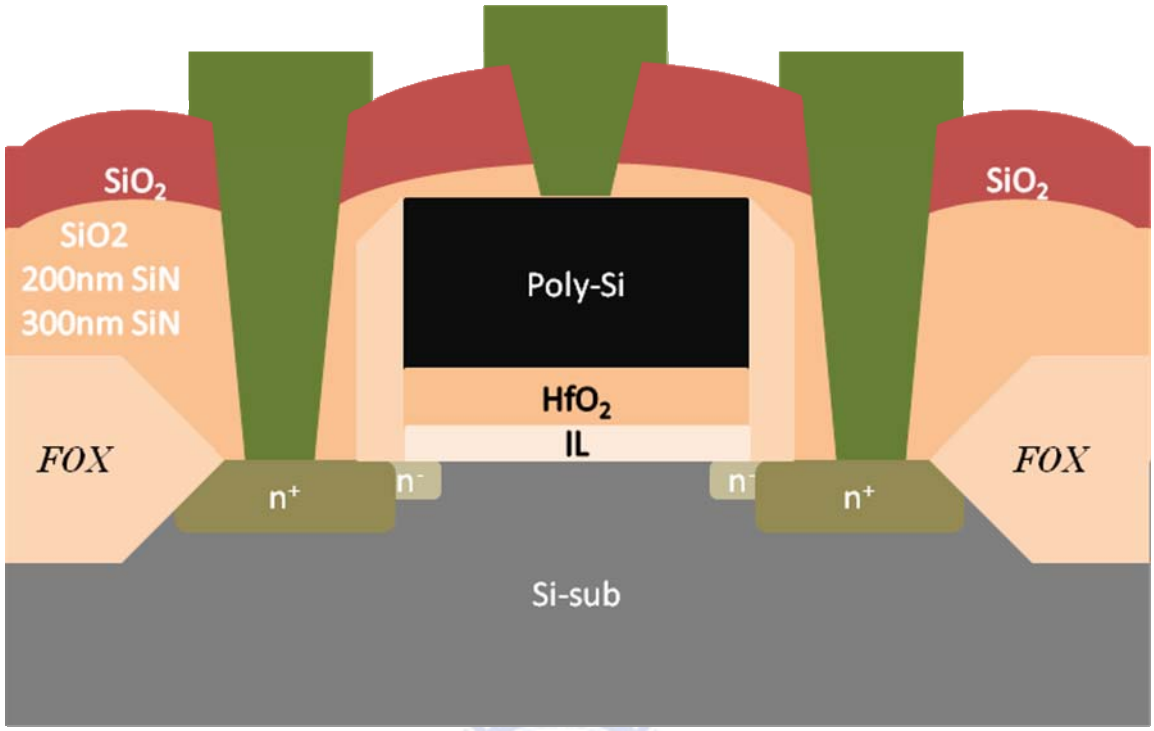
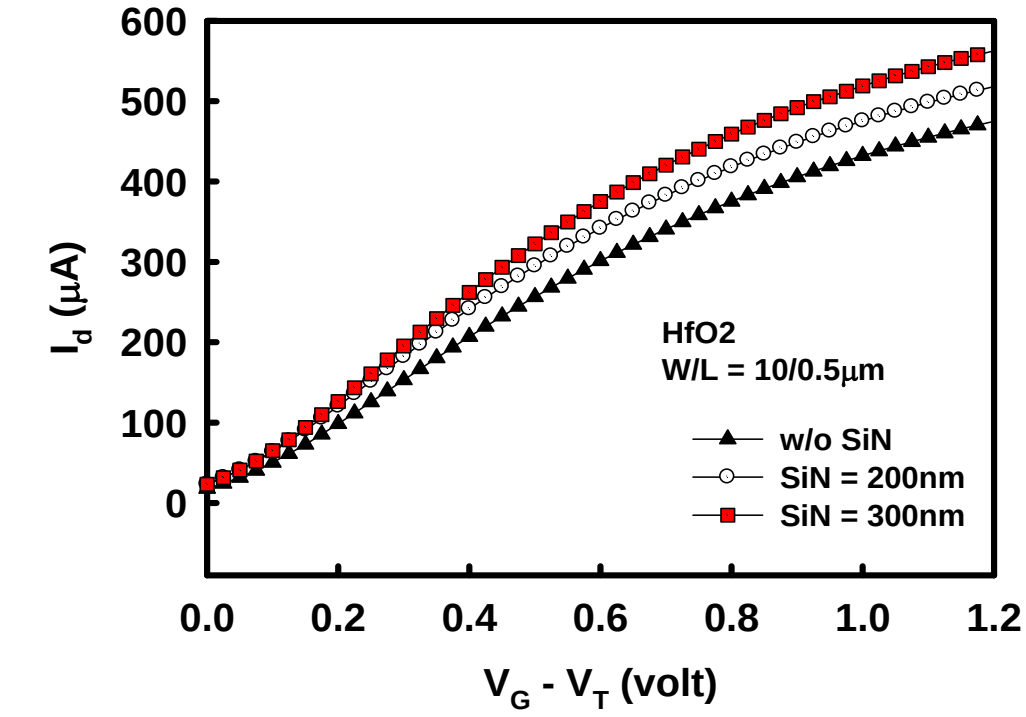


Fig. 2-1 The structure of the devices in strained and unstrained samples.



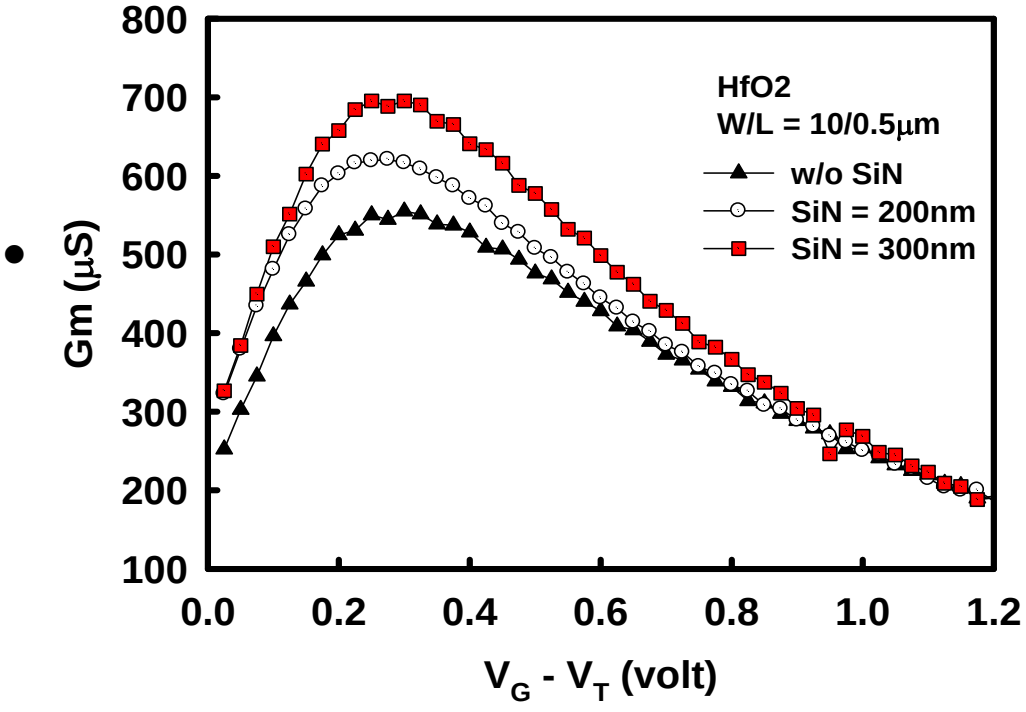


Fig. 2-2 (a) I_d-V_g and (b) G_m-V_g curves of nMOSFET with dual-layer HfO_2/SiON high-k gate stack in different capping nitride layers.

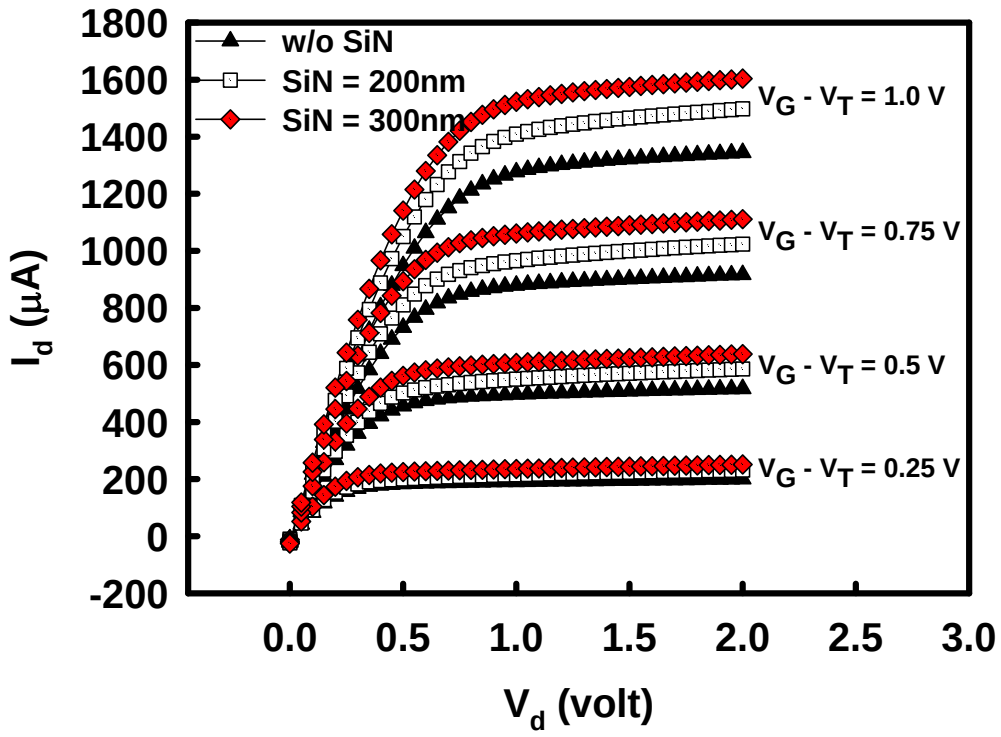


Fig. 2-3 I_d-V_d curves of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in different thickness of capping nitride layers.

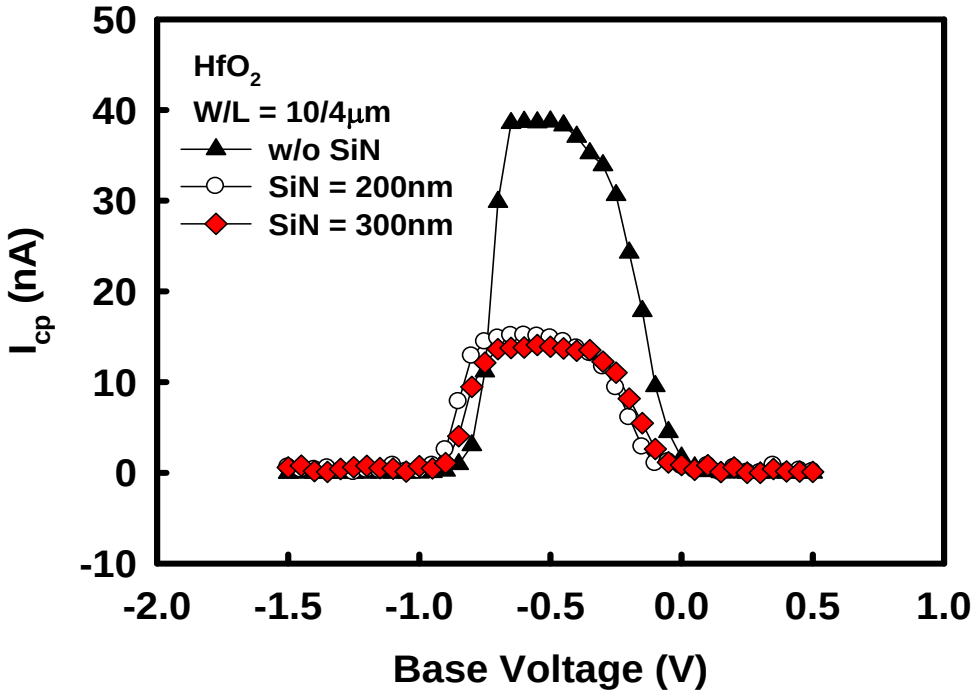


Fig. 2-4 I_{cp}-V_{base} curves of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in different thickness of capping nitride layers.

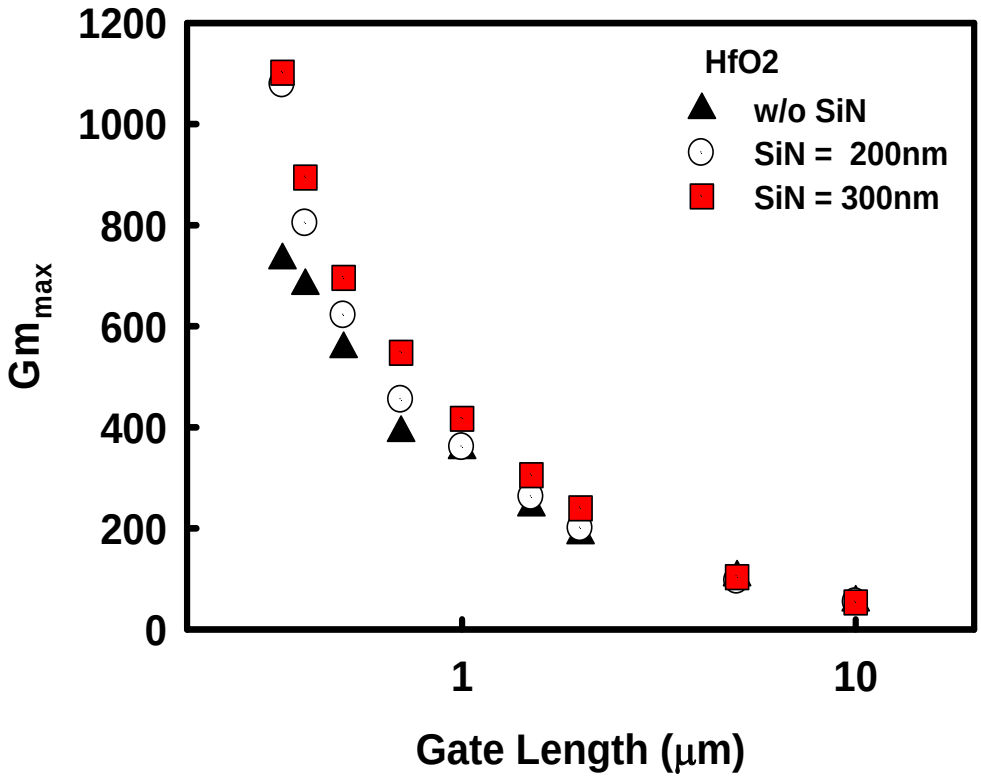


Fig. 2-5 $G_{m,max}$-L_{gate} curves of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in different thickness of capping nitride layers.

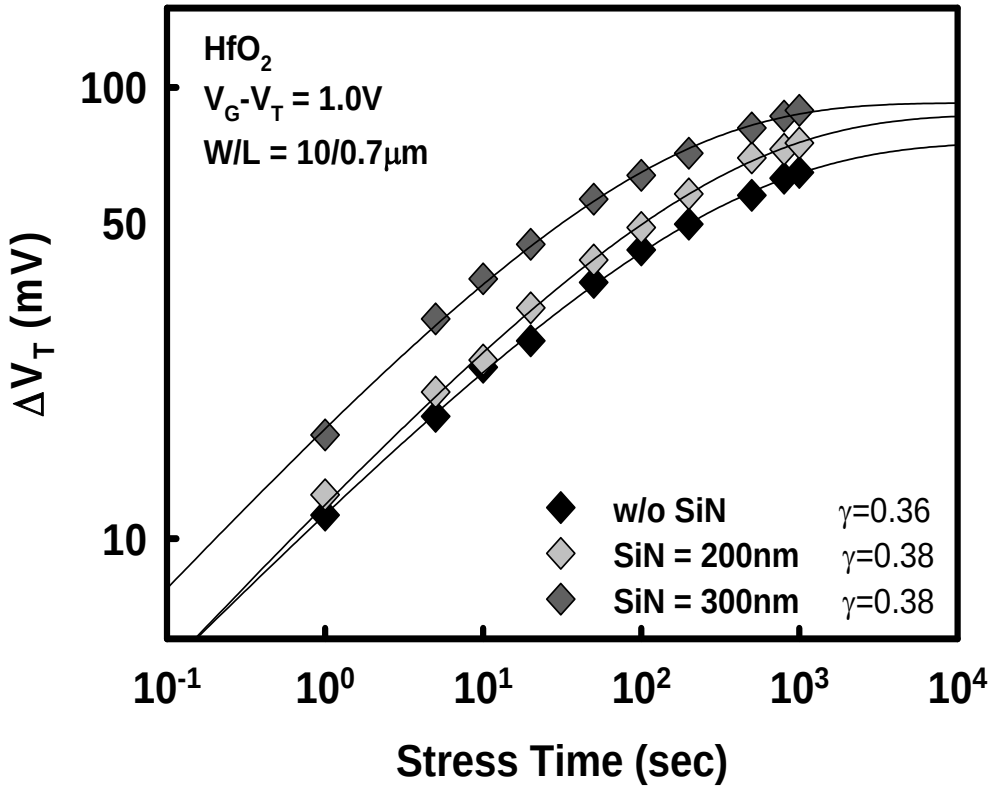


Fig. 2-6 Threshold voltage shift of nMOSFETs as a function of the stress time in difference thickness of capping nitride layers.

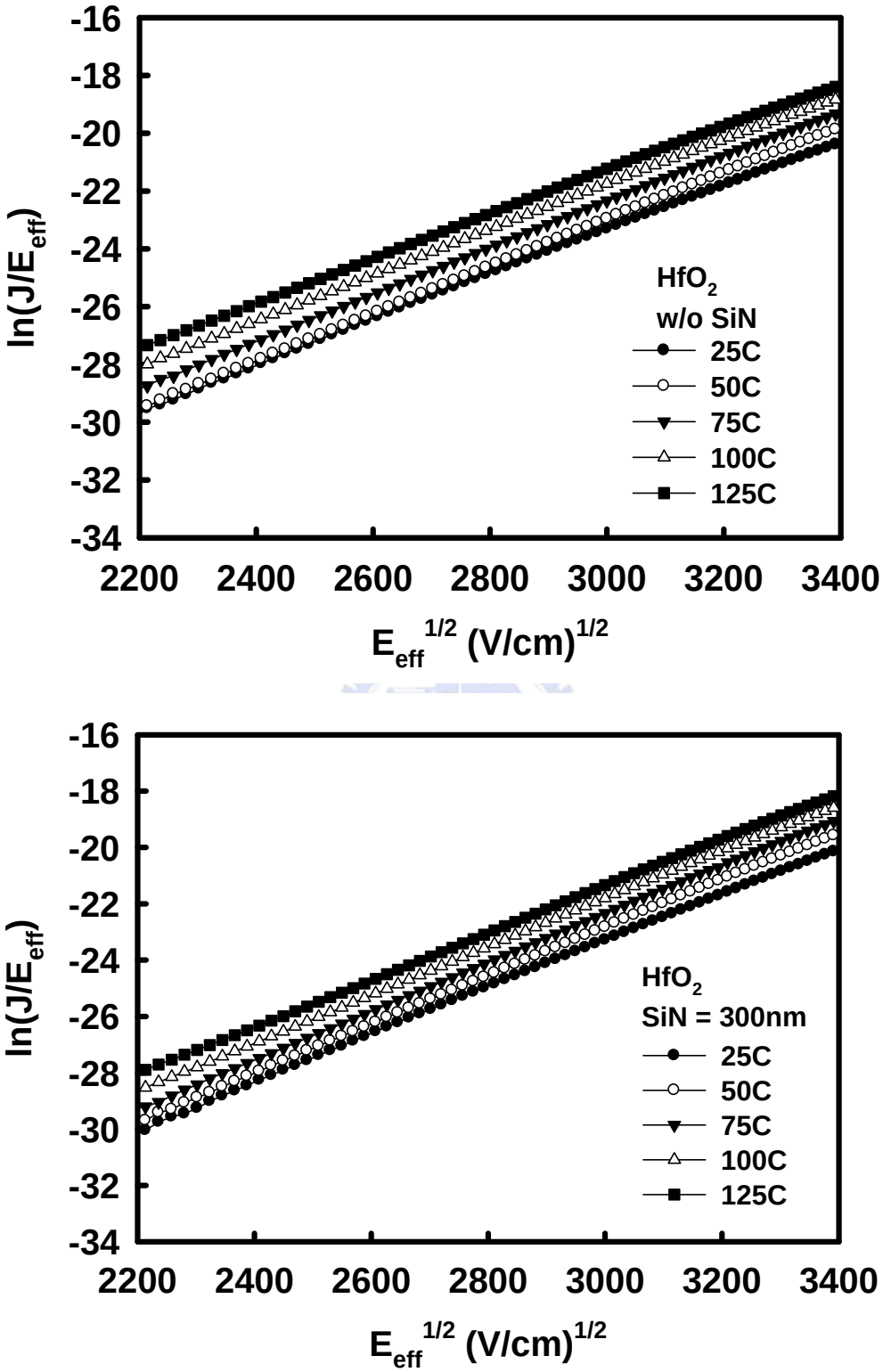


Fig. 2-7 $\ln(J_G/E_{eff})$ as a function of $E_{eff}^{1/2}$ in the (a) unstrained and (2) strained devices. The trapped energy levels can be obtained by y-axis intercept.

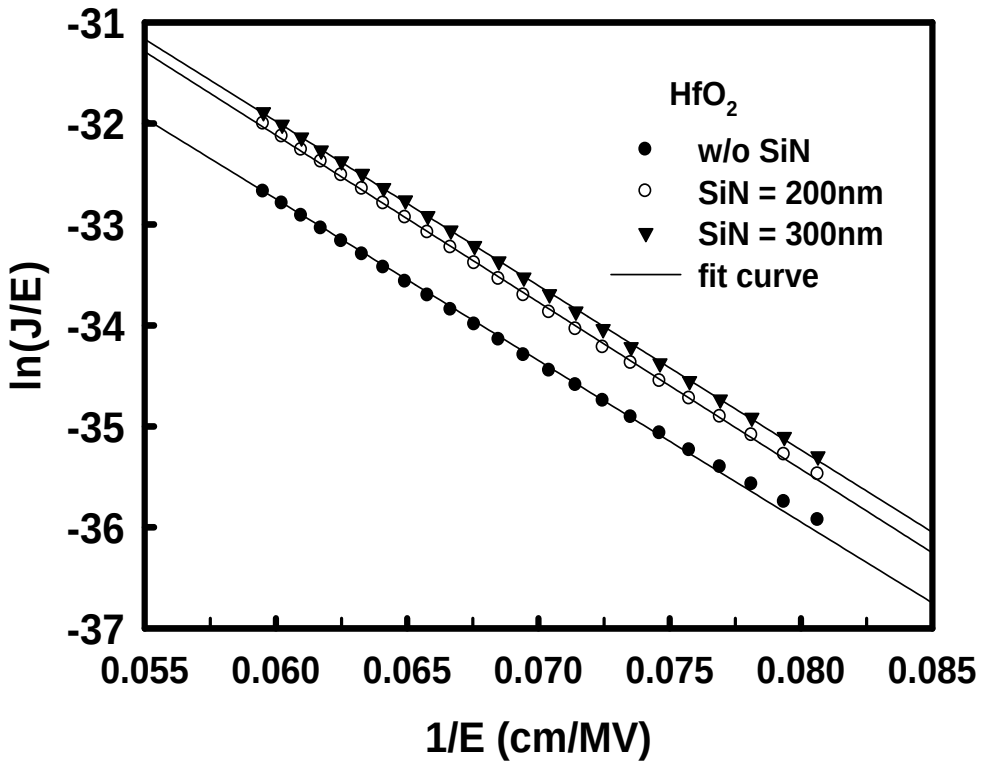


Fig. 2-8 $\ln(J_G/E_{eff})$ as a function of $E_{eff}^{1/2}$ in the unstrained and strained devices. The barrier heights can be obtained by the slopes.

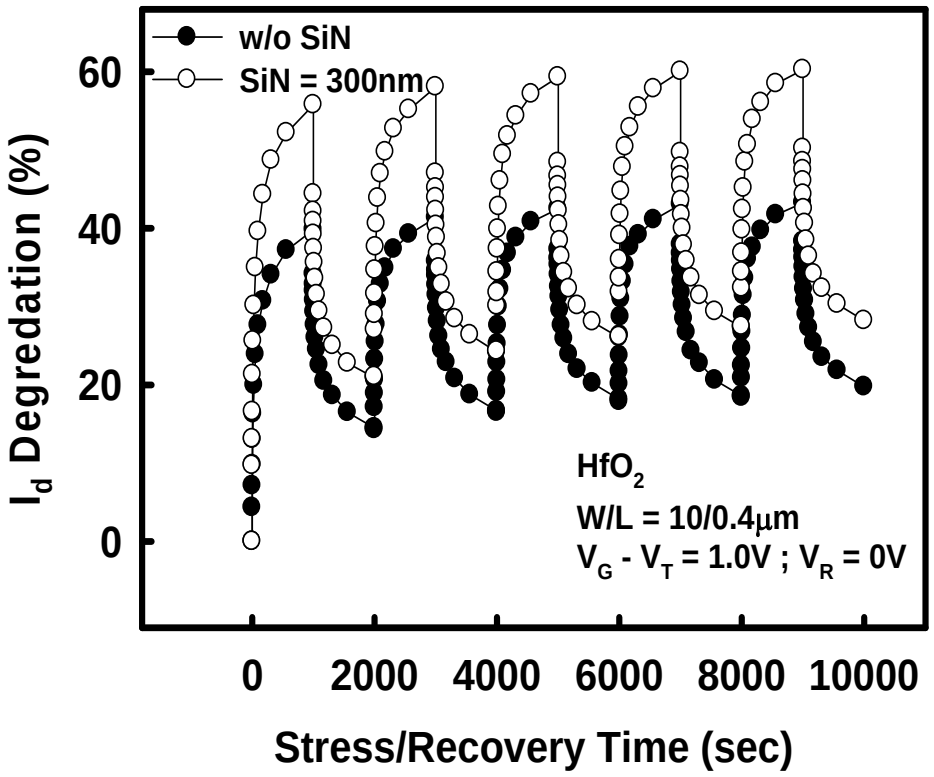


Fig. 2-9 The drain current degradation of nMOSFETs as a function of the stress/recovery time with a fixed stress/recovery voltage +2.0V/0V in difference thickness of capping nitride layers.

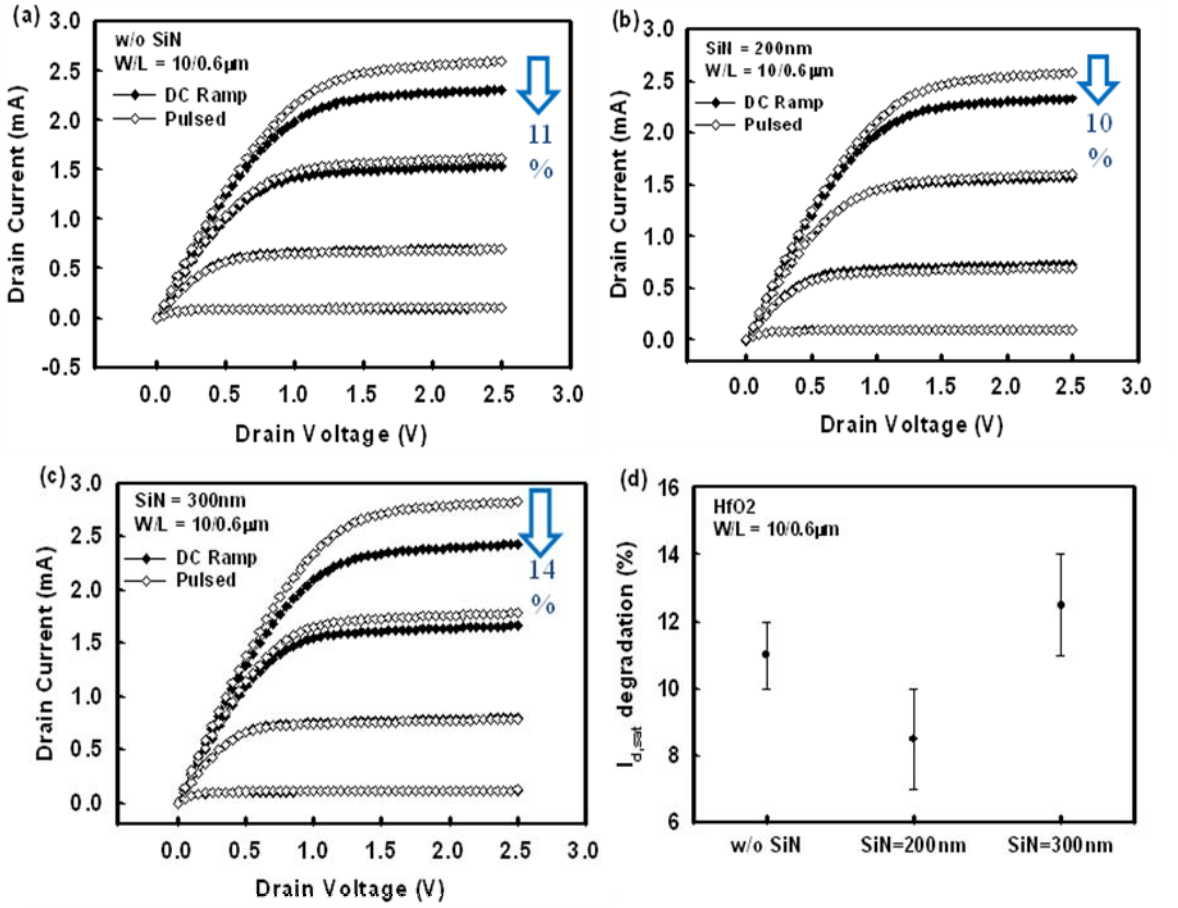


Fig. 2-10 I_d-V_d curves of (a) unstrained (b) SiN = 200nm (c) SiN = 300nm devices by two measurement methods: DC ramp and pulsed I-V and (d) the distribution of drain current degradation under different conditions.

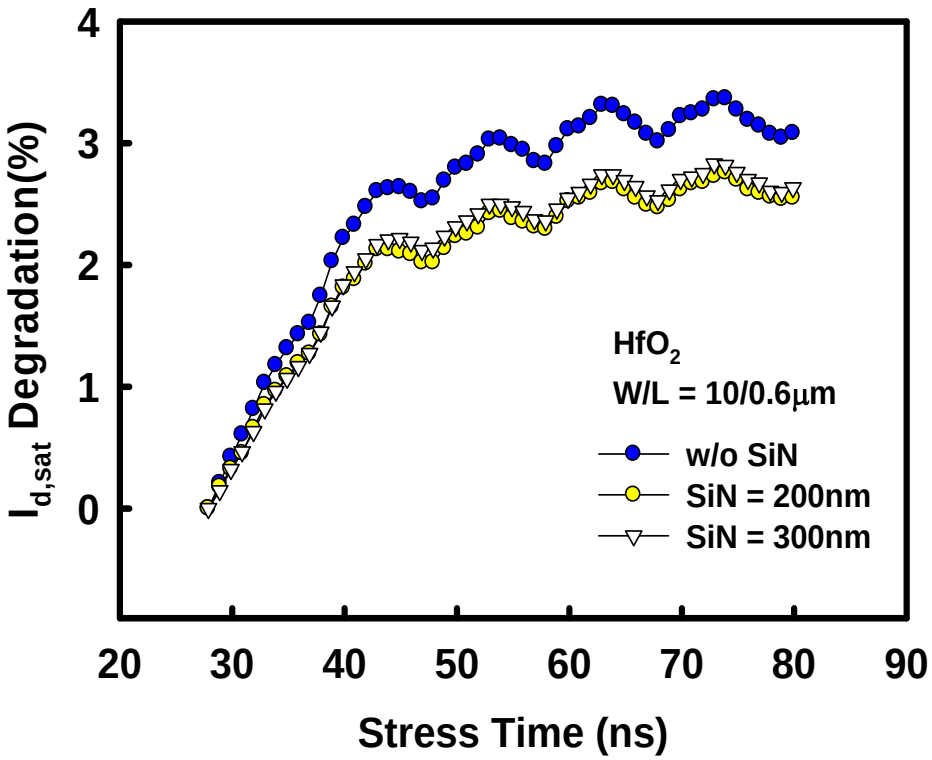


Fig. 2-11 $I_{d,sat}$ as a function of stress time ranging several nanoseconds to 100ns by single pulse measurement.

Chapter 3

Bias Temperature Instability in nMOSFETs with HfO_2/SiON High-k Gate Stacks

3.1 Introduction

Threshold voltage instability in Hf-based high-k gate dielectrics has been recognized as one of the most critical reliability issues that need to be solved urgently, especially for the nMOSFETs under substrate electron injection conditions (positive bias stress) [1]. The electrons in channel are injected into the pre-existing bulk traps of the HfO_2 high-k gate dielectric by tunneling through the thin interfacial oxide. The pre-existing traps of the HfO_2 high-k gate dielectric are positioned above the Si conduction band edge in energy and in the HfO_2 bulk layer in space. These pre-existing bulk traps are distributed in a wide range of space and energy [2], thus making the charge trapping model different from that of conventional SiO_2 or SiON. Furthermore, the high-k dielectrics are reversible by charge trapping and de-trapping. Thus, it is found that the trapped charge carriers could recover to the pre-stress condition after prolonged recovery time. According to results of the threshold voltage shift and the drain current degradation with stress/recovery time, the model could be built to fit the data with reasonable physical mechanism. However, since the charge carriers could be trapped/de-trapped quickly and easily by applying a forward/reverse bias voltage, the degradation may be underestimated due to the switching and measuring delays in the stress/measure cycles [3]. These so-called fast traps would be detected by transient measurement solving the underestimate of charge trapping in high-k gate dielectrics.

In this chapter, the charge trapping behavior under various voltages, temperature and

geometrics will be studied in detail to comprehend the physical model in section 3.3. In section 3.4, the charge de-trapping behavior under various stress voltages and recovery voltages will be investigated to build the physical model according to the charge trapping model. Finally, the transient charge trapping behavior will be analyzed by pulsed I-V measurement.

3.2 Device Fabrication

nMOSFET devices with the poly-Si/HfO_2/SiON high-k gate stacks were fabricated using the conventional CMOS process technology. The interfacial oxide (～1.0 nm) was formed by oxide rapid thermal anneal (RTA) at 800℃ in N_2O ambient with 30s, followed by the deposition of the HfO_2 (～3.0 nm) high-k gate dielectric using atomic layer deposition (ALD) technique. The 200 nm poly-Si was deposited by low pressure chemical vapor deposition (LPCVD). After gate definition, spacer formation, and S/D implantation, the capping layer was deposited by plasma chemical vapor deposition (PECVD). The equivalent oxide thickness of above mentioned high-k gate stack was extracted to be 2.0～2.5 nm by using C-V measurement.

3.3 Electron trapping behaviors during stress in high-k gate dielectric

Fig. 3-1 shows (a) the gate leakage current density and (b) the subthreshold slop as a function of stress time for nMOSFETs under static stress at various gate bias voltages. The gate leakage current density increases with stress voltage. The symbols in Fig. 3-1 (a) are the measurement data and the solid lines are power law fits to the results. Since J_g is observed to decrease with stress time, it implies that no new traps in the bulk are created during stressing. The subthreshold slope remains constant with stress time

regardless of stress voltage. Since interfacial trap density can be detected by subthreshold slope, it is concluded that no new interfacial traps are created during stressing. Therefore, creation of additional new traps during stressing is assumed to be negligible. Thus, it implies that the electron trapping and de-trapping behaviors are occurred in the pre-existing traps of the HfO_2 gate dielectric.

Fig. 3-2 shows the threshold voltage shift as a function of stress time for nMOSFETs under static stress at various gate bias voltages. The threshold voltage shift in this study is determined from the static I_d-V_g characteristics. The symbols in Fig.3-2 are measurement data and the solid lines are the fits to the results using the physical model proposed by Zafar et al. The model assumes that the injected charge carriers are captured with dispersive capture time constant in the pre-existing bulk traps of the high-k gate dielectrics without additional new traps generated during the static stress. The operation process of the model that is a little different from that by Zafar et al. is showed as followings:

$$\frac{dn_T}{dt} = \frac{(N_{tot} - n_T)}{\tau_c} \tag{3.1}$$

$$n_T = N_{tot}\left[1 - \int \frac{\rho(\tau_c)}{N_{tot}} \cdot \exp(-\frac{t}{\tau_c}) \cdot d\tau_c\right] = N_{tot}\left[1 - \exp(-(\frac{t}{\tau_{c0}})^{\gamma})\right] \tag{3.2}$$

$$\Delta V_T = \Delta V_{\max}\left[1 - \exp(-(\frac{t}{\tau_0})^{\gamma})\right] \quad where \quad \Delta V_{\max} = \frac{q \cdot N_{tot} \cdot x_{eff}}{\varepsilon \cdot area} \tag{3.3}$$

However, the modeling equation (3.3) of the model is the same with that of Zafar's model.

Where n_T is the trapped charge density, $\rho(\tau_c)$ is the trapped charge density per second with continuous capture time constant, N_{tot} is the total density of traps of the HfO_2 gate

dielectric, τ_c/τ_{c0} is the capture time constant/characteristic capture time constant, t is the stress time, γ is the distribution factor of $\rho(\tau_c)$ versus capture time constant, ΔV_{max} is the maximum threshold voltage shift, q is the magnitude of electronic charge, x_{eff} is the centroid of trapped charge, area is the gate area, and ε is the permittivity of the dielectric.

By Eq. 3.3, the three parameters (ΔV_{max}, γ, and τ_{c0}) that well describe the behavior of charge trapping would be obtained by fitting the symbols of Fig. 3-2. These parameters would be dependent on stress voltage with trends in Table 3-1. First, the maximum V_t shift dependent on N_{tot}, and x_{eff} (q, ε, and area are fixed values) increased with increasing stress voltage. However, N_{tot} had been assumed a fixed value in the original of the model used in SiO_2 [4]. Then, the ratio of ΔV_{max} of 3.0V to ΔV_{max} of 1.5V 8:1 would be equal to the ratio of x_{eff} of 3.0V to x_{eff} of 1.5V. This is inconsistent with physical principle because the maximum ratio of total thickness of the gate dielectrics to the thickness of SiON is smaller than 8:1. Thus, it could be assumed that the total density of traps (N_{tot}) would be a function of stress voltage and N_{tot} increased with increasing stress voltage. The total density of traps truly represents the maximum density of traps that can be filled by charge carriers under specific stress voltage. Next, it is inconsistent with Zafar's previous work in the γ factor which is only dependent on high-k materials. However, the decreasing γ factor with increasing stress voltage that is consistent with our results has been reported by using power law fitting method in [5]. Therefore it is probable that the γ factor is dependent not only on high-k materials but also on stress voltage. The smaller γ factor under higher stress voltage represents the wider distribution of the capture time. According to above mentions of N_{tot} and γ, the trapped charge density distribution versus capture time under different stress voltages could be predicted and roughly plotted in Fig. 3-4 [6]. In the first stage of the each curve in Fig. 3-4, the increasing charge density along increasing capture time would be due to

the capture time increasing with stress time. Then, the each curve of Fig. 3-4 would reach the maximum value and become decay with capture time because the trapped electrons could build an energy barrier that induced the electrons injecting to high-k gate dielectric harder. Finally, the maximum trap density would be fully filled by electrons and the V_t shift would reach a constant. At last, the characteristic capture time constant would decrease with increasing stress voltage in Fig. 3-3due to the increasing injected charge carriers. Thus, the "early trapped" (0～1s) charge carriers would increase with increasing stress voltage demonstrated in Fig. 3-5.

The same fitting model could be used in the drain current degradation under various stress voltages in Fig. 3-6 and the trends of the parameters would be the same with the results of threshold voltage shift. Moreover, Fig. 3-7 (a) shows the threshold voltage shift as a function of stress time for HfAlO high-k gate dielectric under static stress at various gate bias voltages. Fig. 3-7 (b) shows the characteristic capture time constant under various gate bias voltages. The results showed the same trends in the three parameters with the HfO_2 high-k gate dielectric and could be fitted by the same model. Comparing with the γ factor of the HfO_2 gate dielectric under the same voltage, γ varies with different high-k materials and that is consistent with the Zafar's previous work.

Fig. 3-8 shows the threshold voltage shift as a function of stress time for nMOSFETs under static stress at various temperatures. The V_t shift decreased with increasing stress temperature. The reason can be suggested that the de-trapping mechanism is dominant under higher stress temperature. Although the V_t shift seemed to slow down under higher stress temperature, the generated interface trap density measured by CP degraded more serious in Fig. 3-9. Fig. 3-10 shows the threshold voltage shift as a function of stress time for nMOSFETs under static stress at various dimensions. The V_t shift with stress time would be dependent on gate length, but independent on gate width. Moreover, the increasing gate length increased the V_t shift. The phenomenon can be

suggested that larger gate length with smaller source/drain overlap ratio induces more V_t shift because the electric field in the S/D overlap region smaller than that in the channel under the positive stress voltage.

3.4 Electron De-trapping Behavior during the Stress/Recovery Cycles in High-k Gate Dielectric

Fig. 3-12 shows the drain current degradation for nMOSFETs under static stress/recovery time with a fixed stress voltage V_g=+2.0V and various recovery voltages V_g =+1.4～-1.4V. Under strong recovery voltage such as V_g=-1.4V, almost all the trapped electrons in the HfO_2 traps could be de-trapped. As the recovery voltage was weaker, the residual electrons that couldn't be de-trapped become more. Fig. 3-13 (a) shows the recovery region of Fig. 3-12. The symbols are measurement data and the solid lines are the fits to the results using the physical model that is built according to Zafar's charge tapping model. The recovery model assumes that the trapped charge carriers emit with dispersive emission time constant in the pre-existing bulk traps of the high-k gate dielectrics. The operation process of the model is showed as followings:

$$\frac{dn_{de}}{dt} = \frac{(n_{de,MAX} - n_{de})}{\tau_e} \tag{3.4}$$

$$n_{de} = n_{de,MAX}\left[1 - \int \frac{\rho(\tau_e)}{n_{de,MAX}} \cdot \exp(-\frac{t}{\tau_e}) \cdot d\tau_e\right] = n_{de,MAX}\left[1 - \exp(-(\frac{t}{\tau_{e0}})^{\gamma})\right] \tag{3.5}$$

$$where \quad n_{de,MAX} = n_{de,MAX}(V_{G,stress}, V_{G,recovery})$$

$$\Delta V_T = \Delta V_{\max} - \Delta V_{de} = \Delta V_{residue} + \Delta V_{de,MAX} \cdot \exp\left[-(\frac{t}{\tau_{e0}})^{\gamma}\right]$$

$$where \quad \Delta V_{\max} = \frac{q \cdot n_{T,MAX} \cdot x_{eff}}{\varepsilon \cdot area}, \Delta V_{de,MAX} = \frac{q \cdot n_{de,MAX} \cdot x_{eff}}{\varepsilon \cdot area} \tag{3.6}$$

$$\Delta V_{residue} = \Delta V_{\max} - \Delta V_{de,MAX}$$

Where n_{de} is the de-trapped charge density, $\rho(\tau_e)$ is the de-trapped charge density per second with continuous emission time constant, $n_{de,MAX}$ is the maximum density of de-trappied charge carriers as a function of recovery and stress voltage, τ_e/τ_{e0} is the emission time constant/characteristic emission time constant, t is the stress time, γ is the distribution factor of $\rho(\tau_e)$ versus emission time constant, $n_{T,MAX}$ is the total density of trapped charge carriers after one thousand seconds stress under stress voltage Vg=2.0V, ε is the permittivity of the dielectric, and x_{eff} is the centroid of trapped charge during stressing.

$$\Delta I_{d,sat} / I_{d0,sat} \approx \Delta I_{residue} + \Delta I_{de,MAX} \cdot \exp\left[-(\frac{t}{\tau_{e0}})^{\gamma}\right] \tag{3.7}$$

The drain current degradation ($\Delta I_{d,sat}/ I_{d0,sat}$) can be linearly transformed with the threshold voltage shift (ΔV_T) from Fig. 3-11. Thus, the modeling equation can be obtained in Eq. (3.7). The four parameters ($\Delta I_{de,MAX}$, $\Delta I_{residue}$, γ, and τ_{e0}) that can well describe the behavior of charge de-trapping are obtained by fitting the symbols of Fig. 3-13 (b). First, the sum of $\Delta I_{de,MAX}$ and $\Delta I_{residue}$ under various recovery voltages would be a fixed value due to the same stress condition. $\Delta I_{de,MAX}$ increased with the stronger recovery voltage due to the $n_{de,MAX}$ as a function of recovery voltage and increasing with increasing recovery voltage that would be similar to N_{tot} of charge trapping model. Moreover, $\Delta I_{residue}$ decreased with the stronger recovery voltage due to the decreasing residual trapped electrons of HfO_2 gate dielectric. Next, the γ factor decreases with the stronger recovery voltage. The smaller γ factor under stronger recovery voltage represents the wider distribution of the emission time of the de-trapped charge carriers. According to above mentions of $n_{de,MAX}$ and γ, the de-trapped charge density distribution versus emission time under different recovery voltages could be also

predicted and roughly plotted in Fig. 3-14 which would be almost the same with Fig. 3-4 of charge trapping. At last, the characteristic emission time constant would decrease with stronger recovery voltage in Fig. 3-14. That's because the trapped electrons with energy above the Si conduction band become more under stronger recovery voltage and the trapped electrons with energy higher than Si conduction band can emit more quickly than those with energy lower than the Si conduction band [1].

Fig. 3-15 shows the drain current degradation for nMOSFETs under static stress/recovery time with various voltages V_g=+1.5～2.5V and a fixed recovery voltage V_g =0V. Under stronger stress voltage and the same recovery voltage, the residual electrons that couldn't be de-trapped become more. Fig. 3-16 (a) shows the recovery region of Fig. 3-15. The symbols are measurement data and the solid lines are the fits to the results using Eq. (3.7). The four parameters ($\Delta I_{de,MAX}$, $\Delta I_{residue}$, γ, and τ_{e0}) are also obtained by fitting the symbols of Fig. 3-16 (a). First, the sum of $\Delta I_{de,MAX}$ and $\Delta I_{residue}$ under the same recovery voltages would be not a fixed value due to the various stress condition. $\Delta I_{de,MAX}$ and $\Delta I_{residue}$ increased with the increasing stress voltage due to the increasing trapped electrons of HfO_2 gate dielectric. Thus, $n_{de,MAX}$ would be as a function of stress voltage and increasing with increasing stress voltage. Next, the distribution of the emission time constant is wider with increasing stress voltage due to the wider distribution of the time constant of trapped charge carriers. According to above mentions of $n_{de,MAX}$ and γ, the de-trapped charge density distribution versus emission time under different stress voltages could be showed in the same plot of Fig. 3-14. At last, Fig. 3-16 (b) shows the characteristic emission time constant (τ_{e0}) increasing with increasing stress voltage because of the more maximum density of de-trapped charge carriers ($n_{de,MAX}$). Then, the average emission time constant of the de-trapped charge is longer after higher stress voltage

Fig. 3-17 shows the drain current degradation for nMOSFETs under static

stress/recovery time with a fixed stress voltage V_g=+2.0V and various recovery voltages V_g =+0.7～-2.0V. The recovery voltage plays a significant role to clean up the trapped charge carriers before the next stress cycle. Under strong recovery voltage Vg=-2.0V, almost all the trapped electrons can be de-trapped immediately, and similar charge trapping/de-trapping behaviors can be observed during the five consecutive stress/recovery cycles. However, the charge trapping/de-trapping behaviors changed under weak recovery voltages since the trapped charge had not been completely removed at weak recovery voltages during previous recovery cycles.

3.5 Fast Electron Trapping Behavior in High-k Gate Dielectric

Fig. 3-18 shows I_d-V_d curves under (a) 25℃ (b) 50℃ (c) 75℃ (d) 125℃ by two measurement methods: DC ramp and pulsed I-V. The measurement time of the conventional DC ramp measurement is about several milliseconds to seconds. The pulse width of the pulsed I-V measurement we used is 100ns and raising/falling time is 20ns. Thus, the different of $I_{d,sat}$ by two methods could be the charge loss with the capture time ranging from 100ns to several milliseconds. In Fig. 3-18 (a), the charge loss would be more serious with increasing gate voltage. Moreover, the charge loss would be retarded with increasing the measurement temperature because of the de-trapping mechanism dominant. These results are consistent with the results of the slow traps.

3.6 Summary

In this chapter, electron trapping and de-trapping characteristics are investigated in the pre-existing traps of the HfO_2 high-k gate dielectric. During the PBTI stress, V_t shift and $I_{d,sat}$ degradation continue to grow and eventually become saturated, whereas the gate leakage decays with stress time and the subthreshold swing remains unchanged. According to the fitting results with the model proposed by Zafar et al., the total density of traps is not a fixed value but dependent on stress voltage and the distribution factor of capture time is dependent on not only high-k materials but also stress voltages. Moreover, the fitting results can build the distribution of the trapped charge density with capture time. The temperature effect and the geometric effect under stressing are discussed. Then, the recovery model can be built base on the charge trapping model. Our recovery model can well fit the measurement data. According to the fitting results with our model, the maximum density of de-trapped electrons is not a fixed value but dependent on stress voltage and the distribution factor of emission time is dependent on stress voltages. Moreover, the fitting results can also build the distribution of the de-trapped charge density with emission time. The fast traps can be detected by pulsed I-V measurement and the results are similar to those of slow traps.

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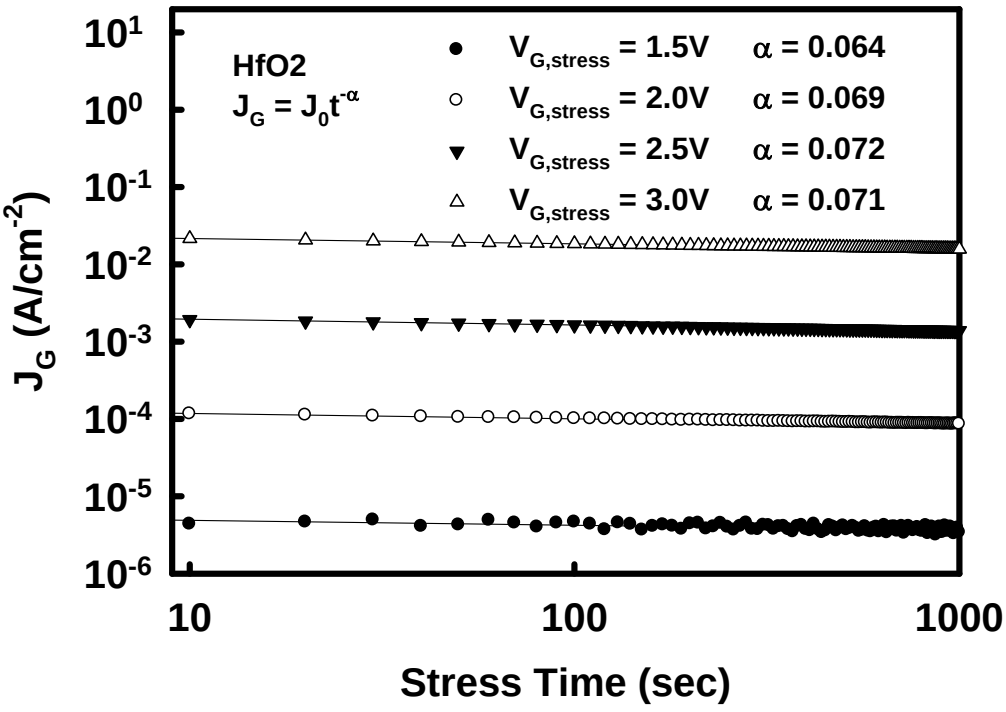
stress voltage / *Parameters*	$V_G = 1.5V$	$V_G = 2.0V$	$V_G = 2.5V$	$V_G = 3.0V$
ΔV_{max} *(V)*	*0.037*	*0.075*	*0.163*	*0.296*
τ_{c0} *(sec)*	*297.5*	*159.9*	*12.8*	*5.5*
γ	*0.41*	*0.36*	*0.28*	*0.24*

Table 3-1 The three parameters, ΔV_{max}, τ_{c0}, and γ, extracted by fitting under various stress voltages.



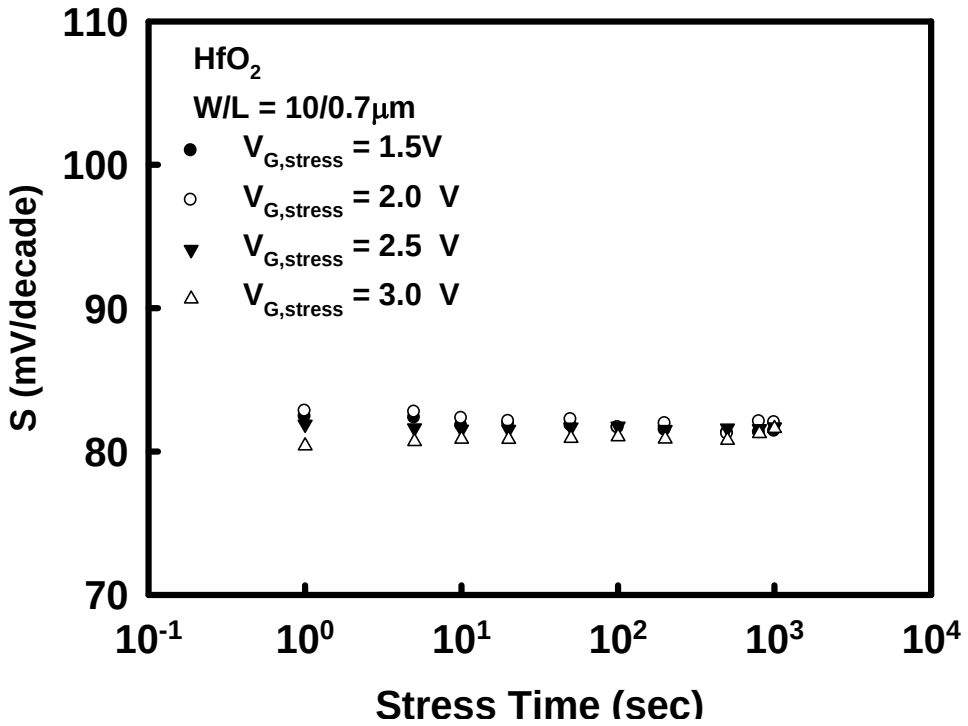


Fig. 3-1 (a) the gate leakage current density and (b) the subthreshold slop as a function of stress time for nMOSFETs under static stress at various gate bias voltages.

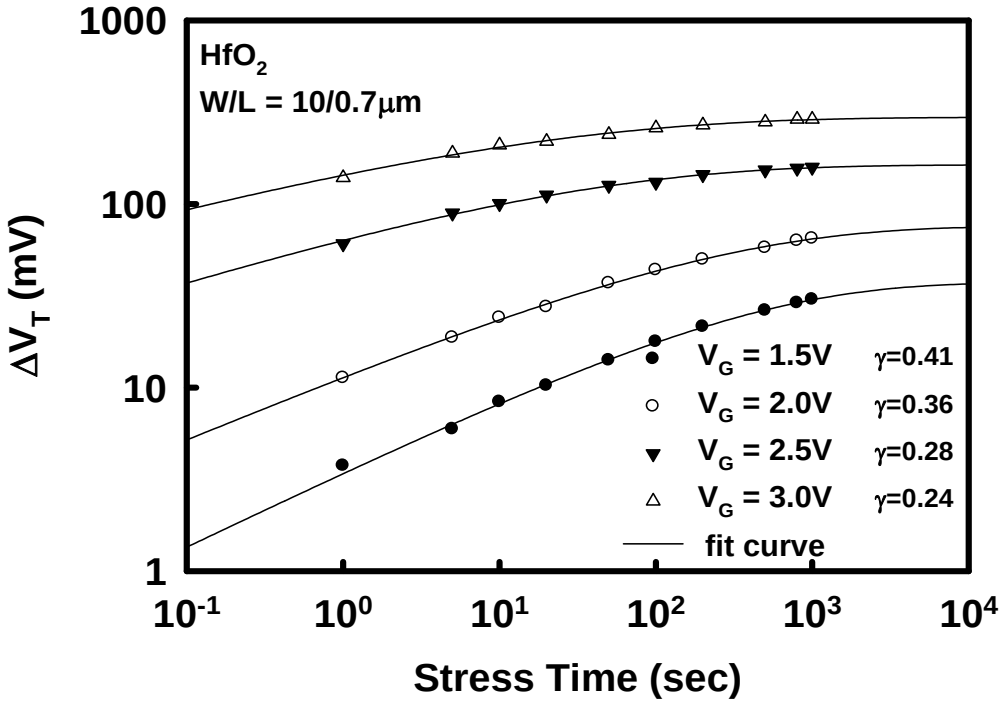


Fig. 3-2 The threshold voltage shift as a function of stress time for nMOSFETs under static stress at various gate bias voltages.

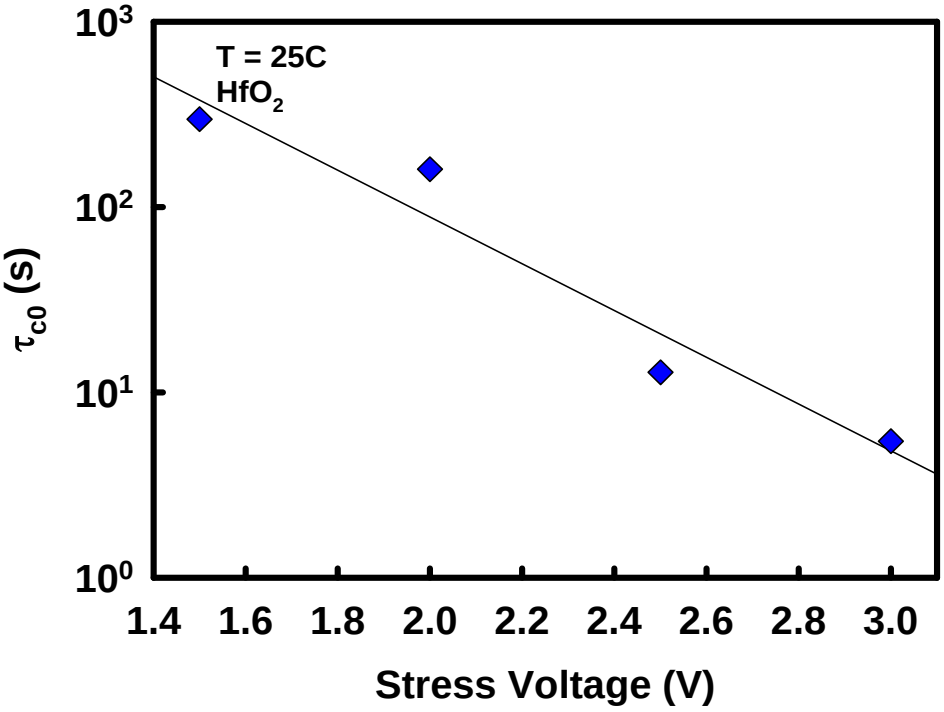


Fig. 3-3 The characteristic capture time constant under various gate bias voltages.

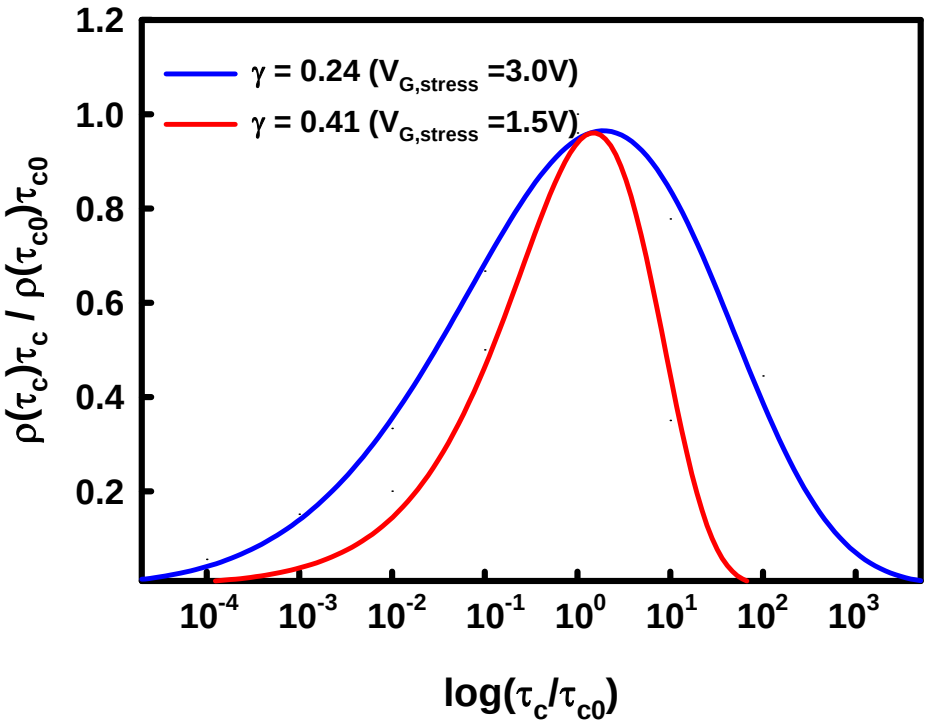


Fig. 3-4 The trapped charge density distribution versus capture time under different stress voltages.

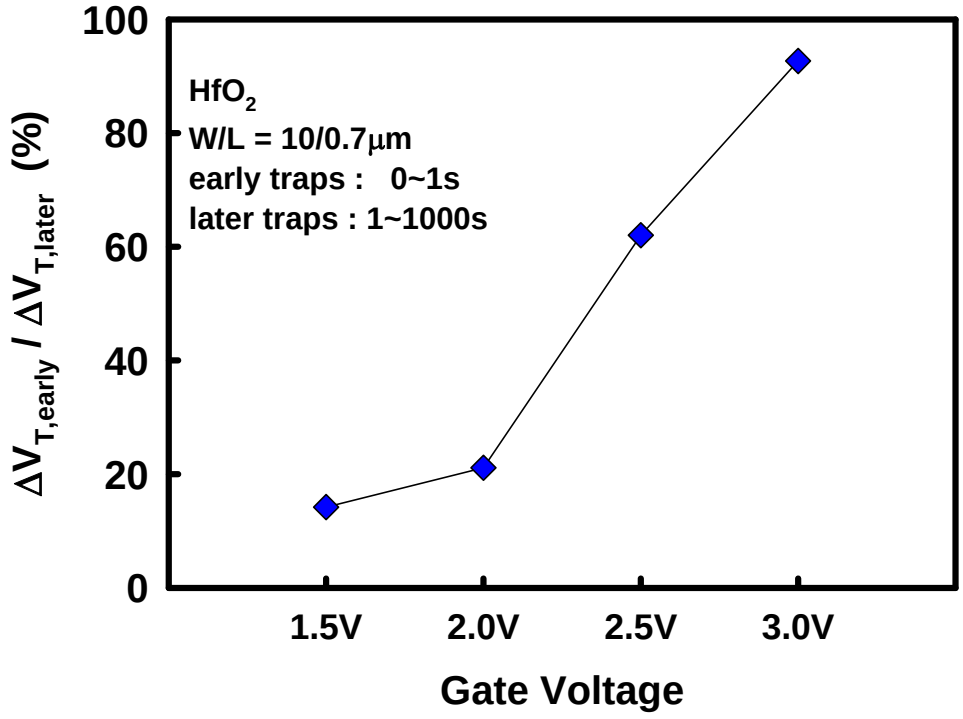


Fig. 3-5 The ratio of early traps to fast traps under various gate bias voltages.

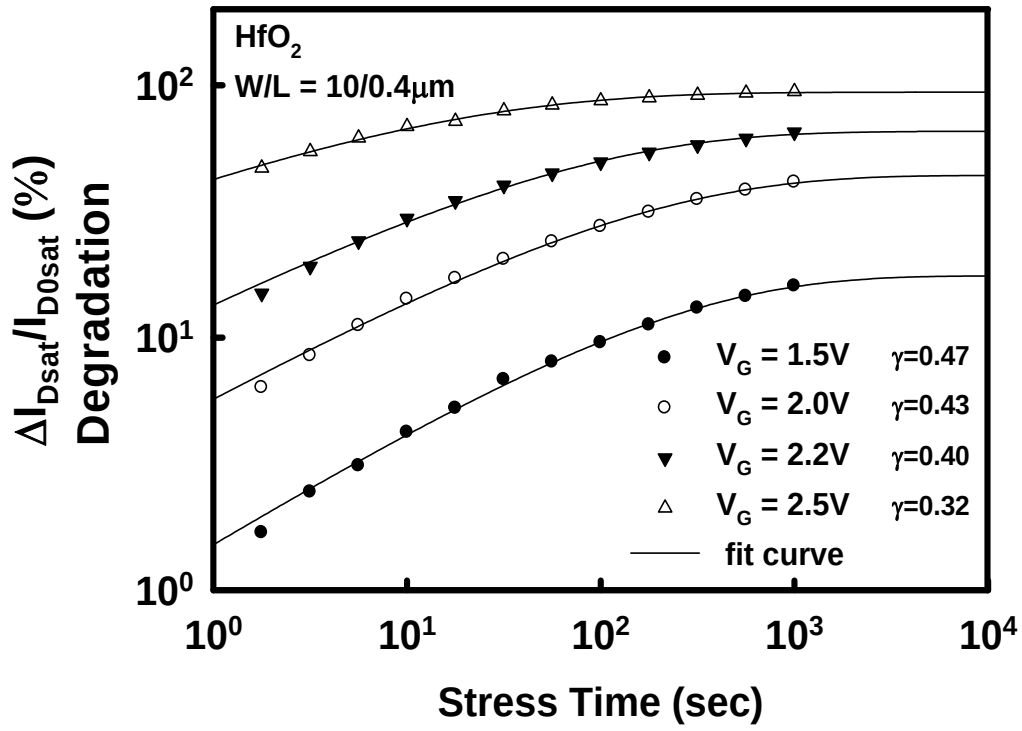
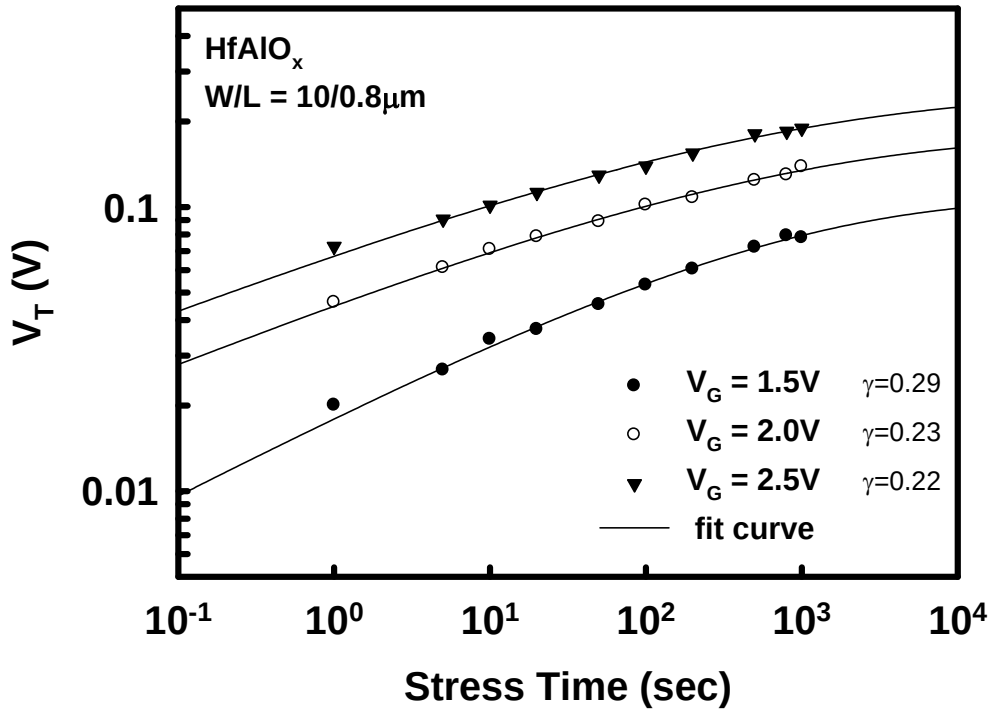


Fig. 3-6 The drain current degradation as a function of stress time for nMOSFETs under static stress at various gate bias voltages.



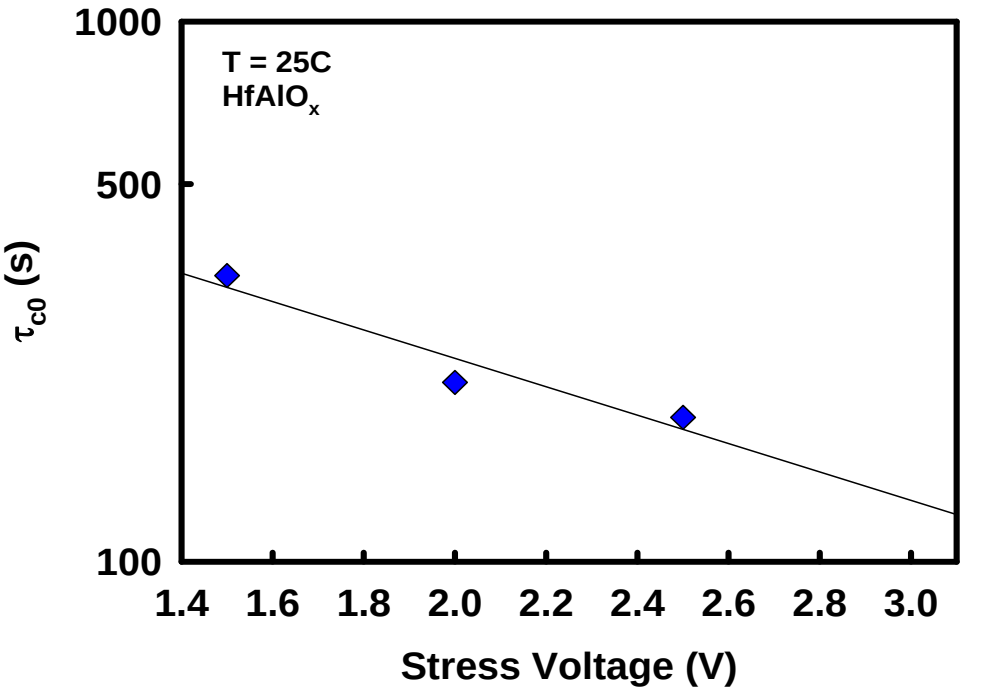


Fig. 3-7 (a) The threshold voltage shift as a function of stress time for HfAlO high-k gate dielectric under static stress at various gate bias voltages. (b) The characteristic capture time constant under various gate bias voltages.

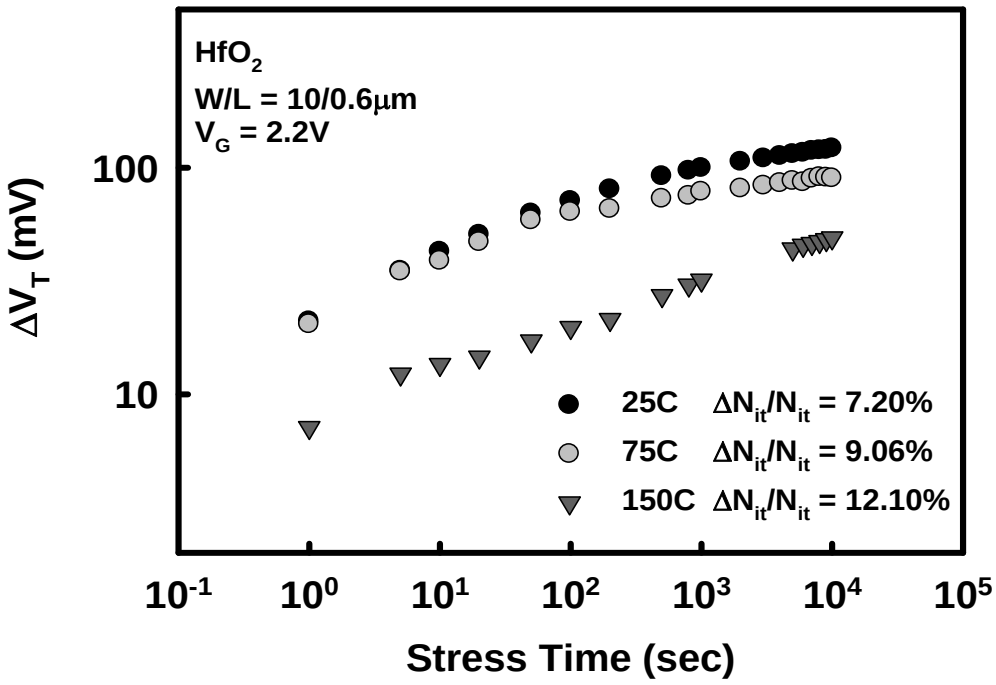


Fig. 3-8 The threshold voltage shift as a function of stress time for nMOSFETs under static stress at various temperatures.

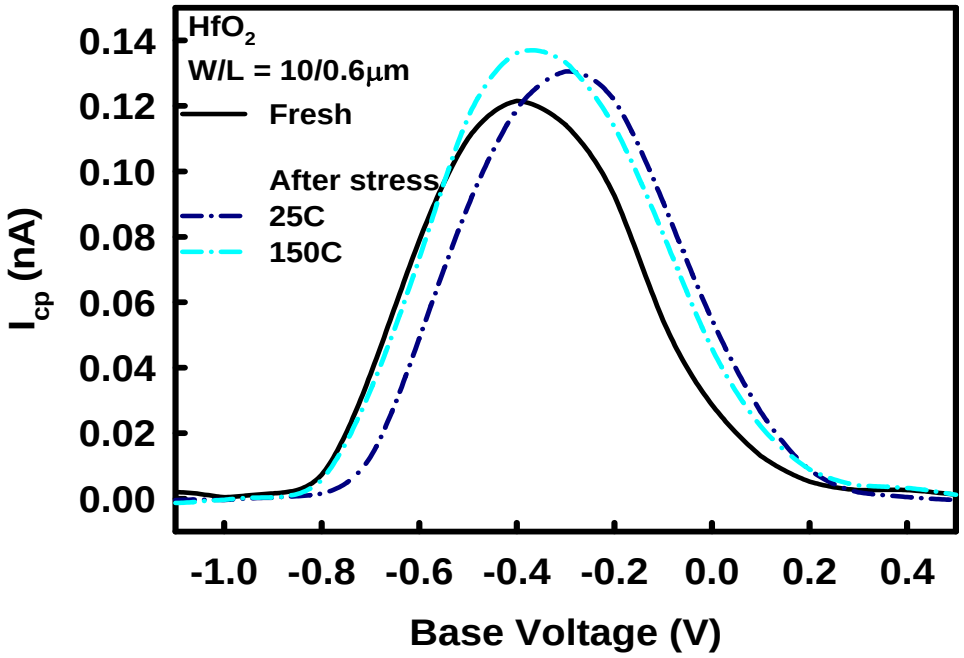


Fig. 3-9 The charge pumping current as a function of base voltage of fresh and stressed conditions under various stress temperatures.

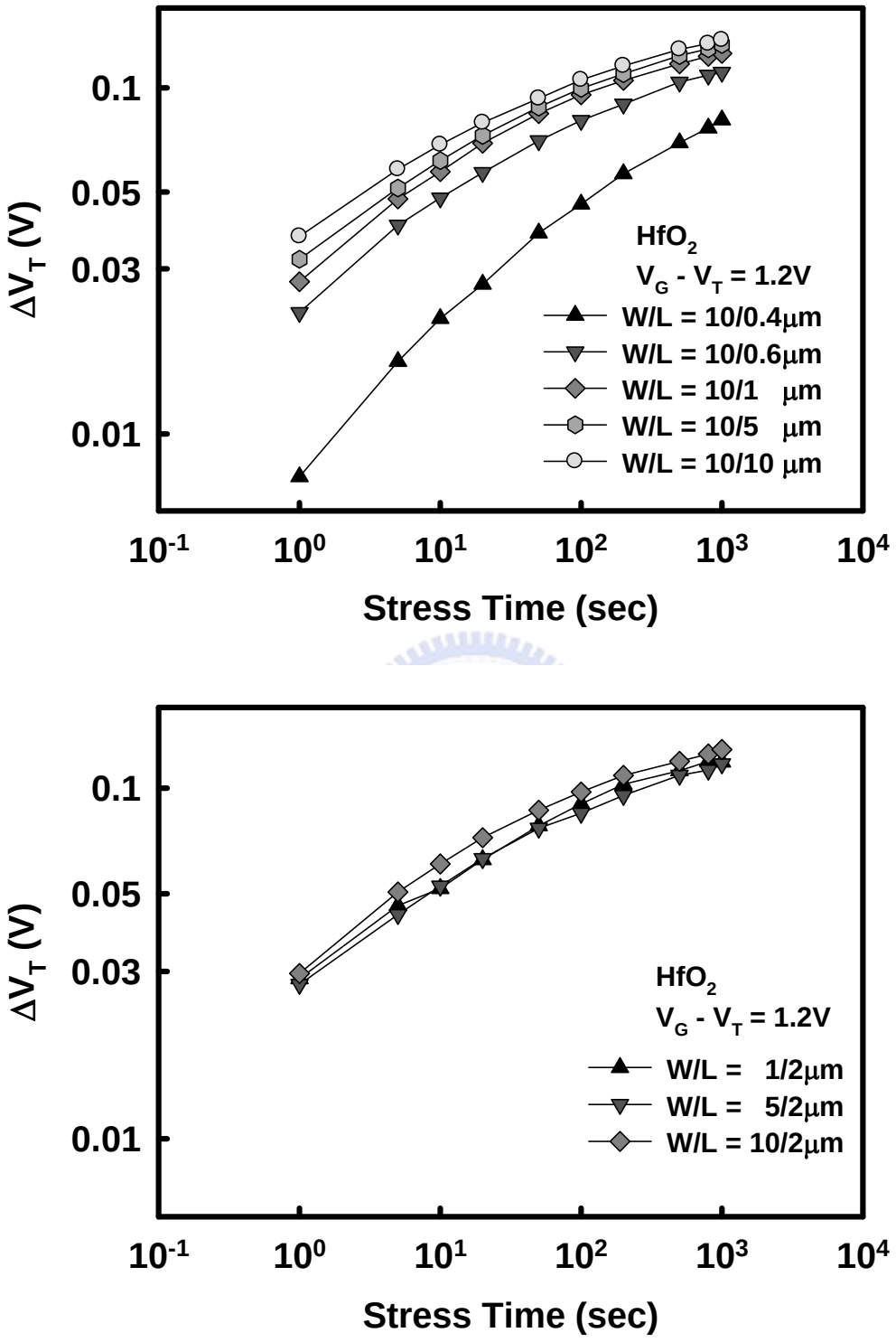


Fig. 3-10 The threshold voltage shift as a function of stress time for nMOSFETs under static stress at various dimensions.

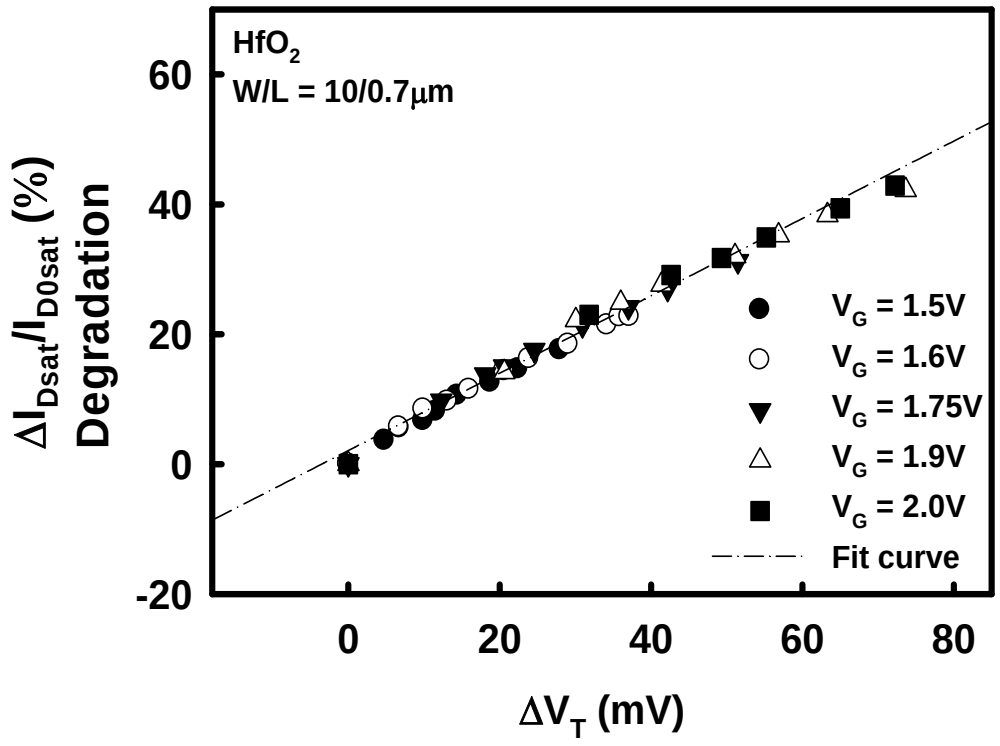


Fig. 3-11 The drain current degradation ($\Delta I_{d,sat}/ I_{d0,sat}$) can be linearly transformed with the threshold voltage shift (ΔV_T).

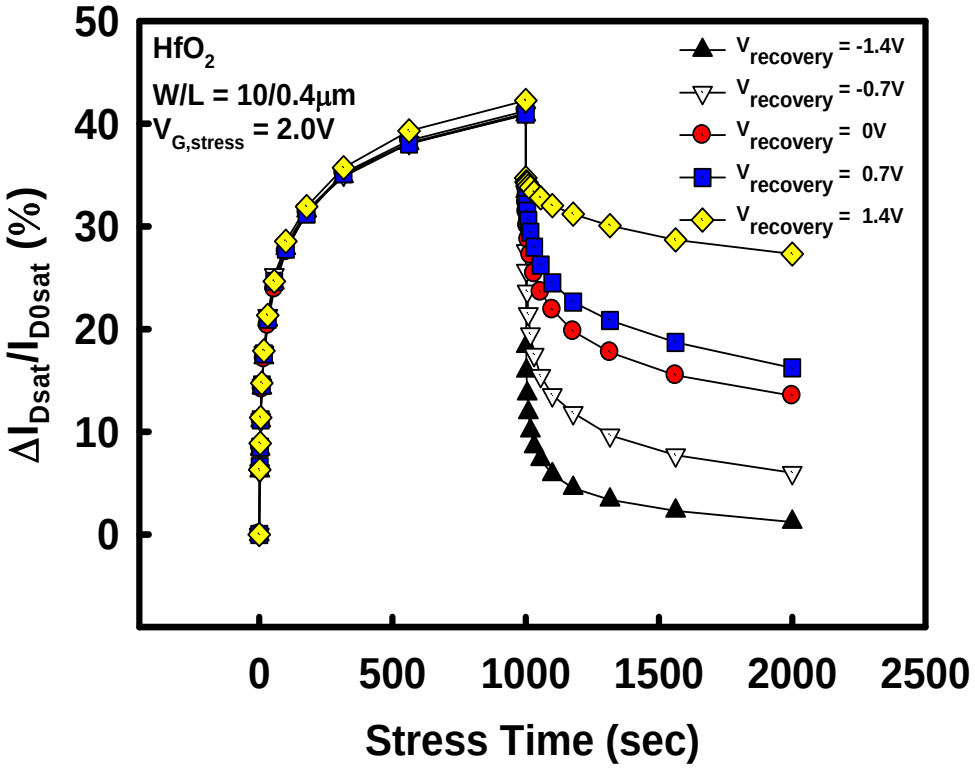
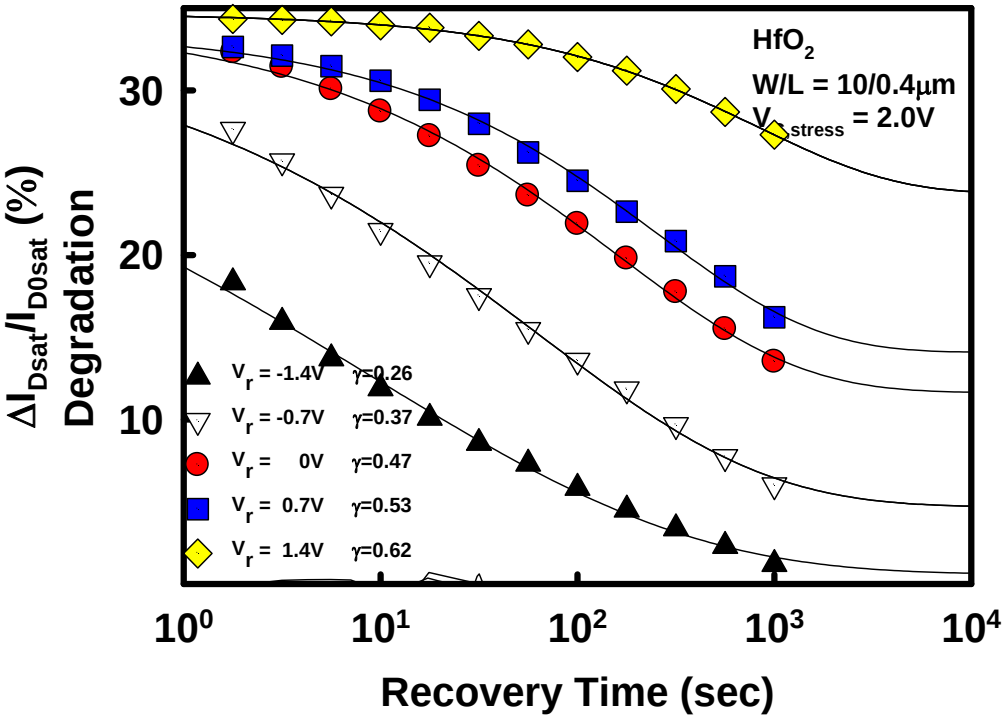


Fig. 3-12 The drain current degradation for nMOSFETs under static stress/recovery time with a fixed stress voltage Vg=+2.0V and various recovery voltages Vg =+1.4 ～-1.4V.



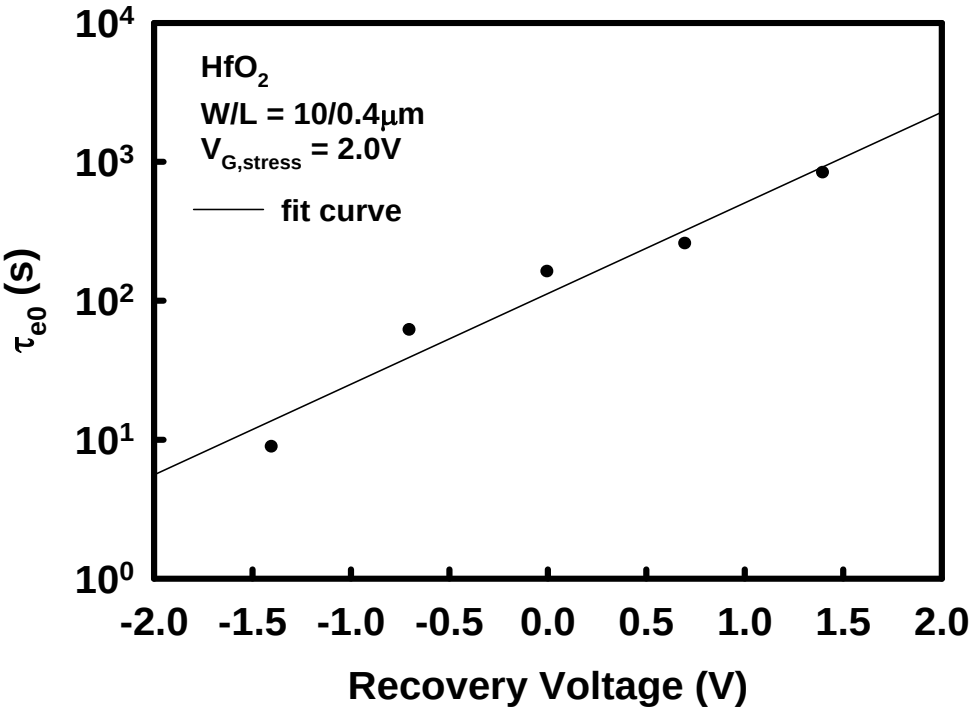


Fig. 3-13 (a) The threshold voltage shift as a function of stress time for HfO_2 high-k gate dielectric under recovery at various recovery voltages. (b) The characteristic emission time constant under various recovery voltages.

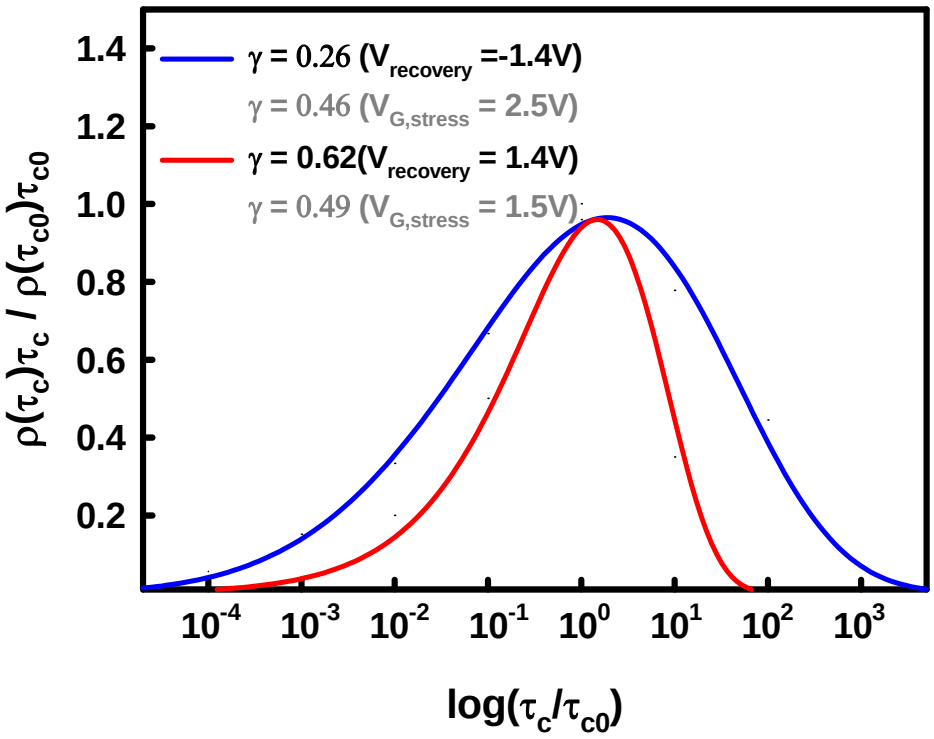


Fig. 3-14 The trapped charge density distribution versus capture time under different stress voltages.

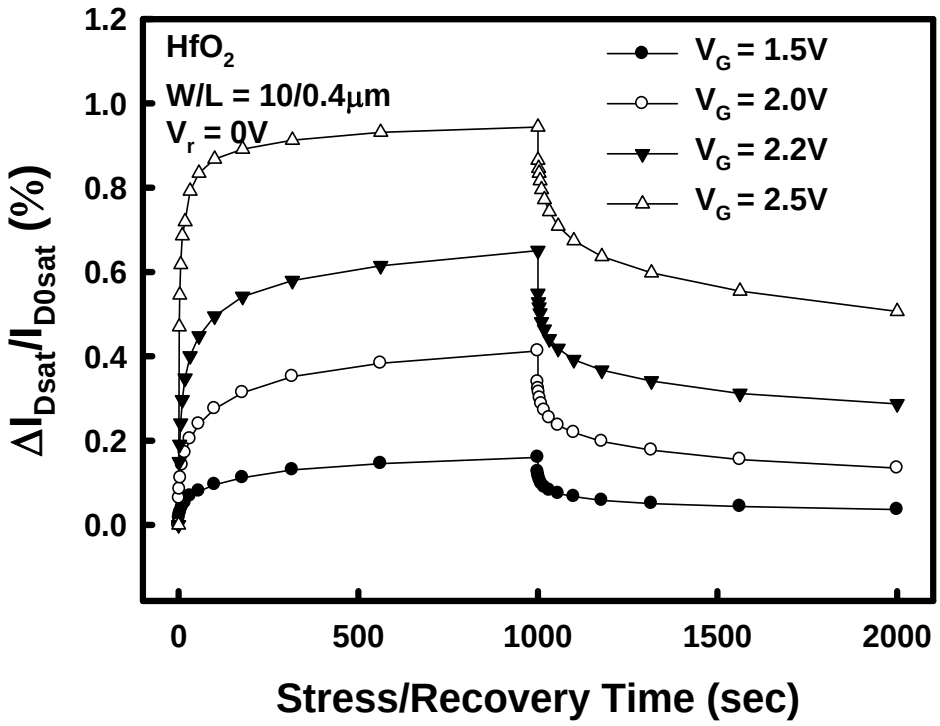


Fig. 3-15 The drain current degradation for nMOSFETs under static stress/recovery time with various voltages V_g=+1.5～2.5V and a fixed recovery voltage V_g =0V.

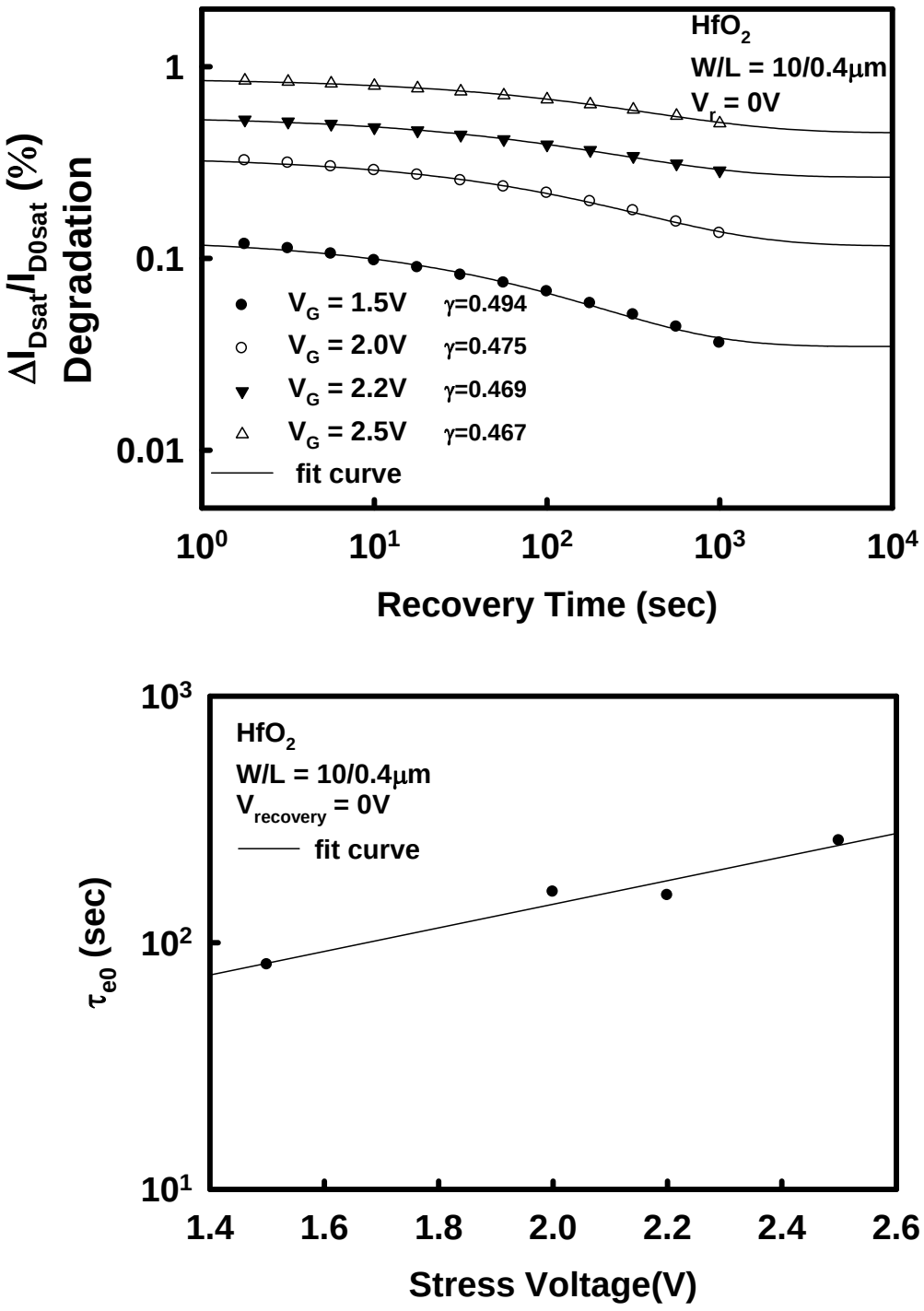


Fig. 3-16 (a) The threshold voltage shift as a function of stress time for HfO_2 high-k gate dielectric under recovery at various stress voltages. (b) The characteristic emission time constant under various stress voltages.

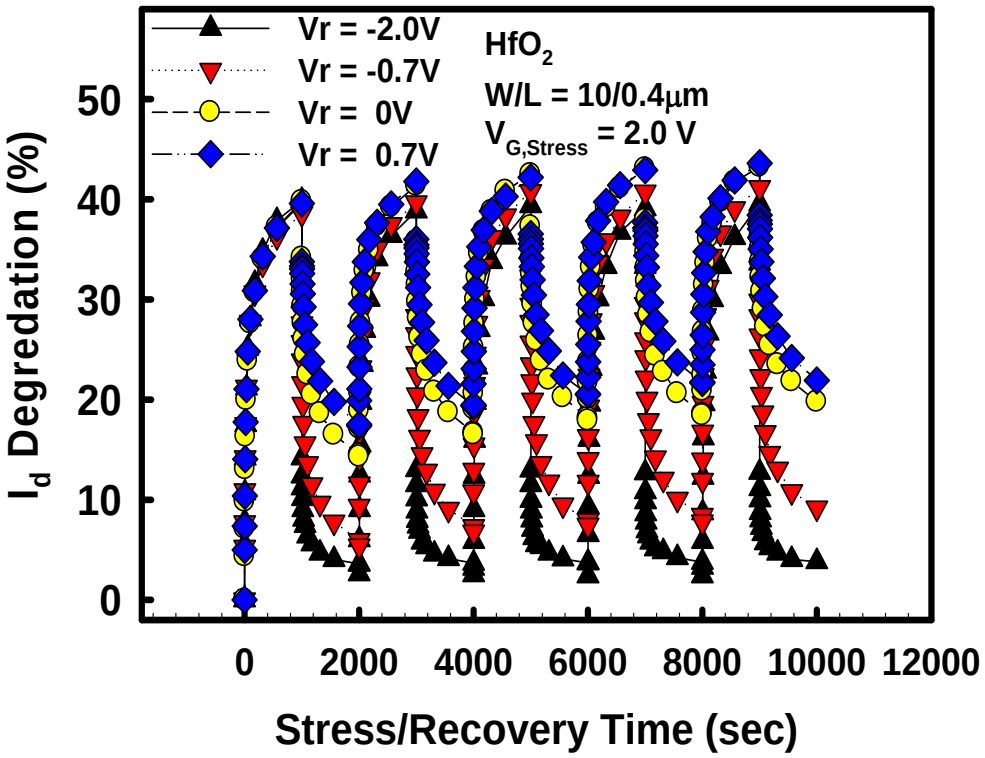


Fig. 3-17 The drain current degradation for nMOSFETs under static stress/recovery time with a fixed stress voltage V_g=+2.0V and various recovery voltages V_g =+0.7 ～-2.0V.

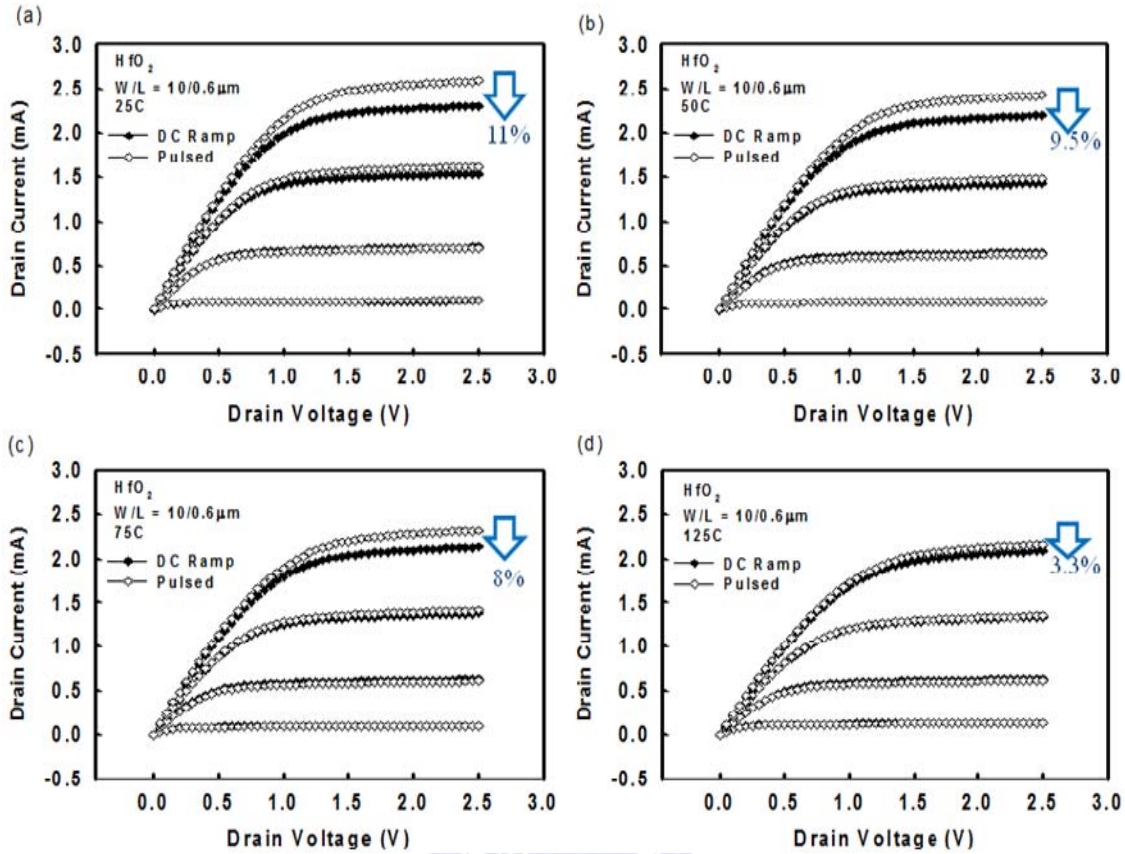


Fig. 3-18 I_d-V_d curves under (a) 25℃ (b) 50℃ (c) 75℃ (d) 125℃ by two measurement methods: DC ramp and pulsed I-V.

Chapter 4

Constant Voltage Stress and Negative Bias Temperature Insatiability Stress in pMOSFETs with HfO_2/SiON High-k Gate Stacks and the Effects of Fluorine incorporation

4.1 Introduction

Compared to nMOSFETs, limited works have focused on the physics of negative bias temperature instability (NBTI) in high-k pMOSFETs [1]-[3]. The model proposed by Zafar et al. the creation of positive oxide charge carriers to de-passivation of Si/SiO_2 interface [1]. As Si-H bonds break, hydrogen diffuses away and reacts with the oxide, thereby generating positive charge carriers in the interface and in the oxide. On the other hand, Houssa et al. presented the impact of forming gas annealing and of Hf content on NBTI [2], [3]. According to their study, the responsible defects are hydrogen-induced overcoordinated oxygen centers induced by the transport and trapping of H^+ in the gate dielectric stacks. Therefore, it is complicated that there are two mechanisms causing threshold voltage shift in high-k gate dielectrics under NBTI: (1) the de-passivation of Si-H bonds and (2) the charge trapping for pMOSFETs with high-k gate dielectric. Thus, the constant voltage stress (CVS) method that induces less degradation of Si/SiO_2 interface can be used to analyze the charge trapping and de-trapping mechanisms. The hole trapping is attributed to filling of pre-existing traps in the high-k dielectrics without the creation of additional traps. In order to suppress the degradation of pMOSFETs under NBT stress, fluorine incorporation used to retard the

degradation on the constant voltage stress and negative bias stress of pMOSFETs has been reported [4].

In this chapter, the charge trapping behavior under constant voltage stress and NBT stress will be studied in detail to realize the physical model in section 4.3. In section 4.4, the charge de-trapping behavior under various stress voltages and recovery voltages will be investigated by the charge de-trapping model proposed in chapter 3. The effect of fluorine incorporation will be investigate in section 4.5. Finally, the transient charge trapping behavior will be analyzed by pulsed I-V measurement.

4.2 Device Fabrication

pMOSFET devices with the poly-Si/HfO_2/SiON high-k gate stacks were fabricated using the conventional CMOS process technology. After conventional LOCOS isolation, some samples received fluorine ion implantations (F: 5E13 cm^{-2} and 5E14 cm^{-2}). Then, the interfacial oxide (～1.0 nm) was formed by oxide rapid thermal anneal (RTA) at 800℃ in N_2O ambient with 30s, followed by the deposition of the HfO_2 (～3.0 nm) high-k gate dielectric using atomic layer deposition (ALD) technique. The 200 nm poly-Si was deposited by low pressure chemical vapor deposition (LPCVD). After gate definition, spacer formation, and S/D implantation, the capping layer was deposited by plasma chemical vapor deposition (PECVD). The equivalent oxide thickness of above mentioned high-k gate stack was extracted to be 2.5～3.0 nm by using C-V measurement.

4.3 Hole Trapping Behaviors during Stress in High-k Gate Dielectric

Fig. 4-1 shows the charge pumping current as a function of top voltage of fresh and

stressed conditions. Under constant voltage stress, the interface states by charge pumping measurement seemed unchanged. Because of that, creation of additional new traps during stressing is assumed to be negligible. Thus, it implies that the hole trapping and de-trapping behaviors are occurred in the pre-existing traps of the HfO_2 gate dielectric under constant voltage stress.

Fig. 4-2 shows the threshold voltage shift as a function of stress time for pMOSFETs under static stress at various gate bias voltages. The threshold voltage shift in this study is determined from the static I_d-V_g characteristics. The symbols in Fig.4-2 are measurement data and the solid lines are the fits to the results using the physical model discussed in chapter 3. By Eq. 4.1, the three parameters (ΔV_{max}, γ, and τ_{c0}) that can well describe the behavior of charge trapping would be obtained in by fitting the symbols of Fig. 4-2 (a). The fitting results: ΔV_{max} increased, γ decreased , and τ_{c0} decreased with increasing stress voltage. The trends of the three parameters are the same with those of nMOSFETs in chapter 3. Thus, we can know that the hole trapping behavior is similar to the electron trapping behavior in slow traps. Compared to nMOSFETs, the values of smaller maximum threshold voltage shift, the wider distribution of capture time, and the longer characteristic time constant (Fig. 4-2 (b)) could be found in pMOSFETs. These differences can be assumed due to the intrinsic characteristics between electron and hole.

$$\Delta V_T = \Delta V_{\max}\left[1-\exp(-(\frac{t}{\tau_0})^{\gamma})\right] \tag{4.1}$$

Fig. 4-3 shows the threshold voltage shift as a function of stress time for pMOSFETs under static stress at various temperatures. In the first stage, the V_t shift decreased with increasing stress temperature. The reason can be suggested that the de-trapping

mechanism is dominant under higher stress temperature. Then, the V_t shift under higher stress temperature increasingly exceeded that under lower stress temperature because the generated traps became dominant. Moreover, the interface trap density measured by CP degraded more serious under higher stress temperature in Fig. 4-4.

4.4 Hole De-trapping Behavior during the Stress/Recovery Cycles in High-k Gate Dielectric

Fig. 4-5 shows the threshold voltage shift for pMOSFETs under static stress/recovery time with a fixed stress voltage V_g=-2.0V and various recovery voltages V_g =0～1.0V. Under strong recovery voltage such as V_g=1.0V, almost all the trapped holes in the HfO_2 traps could be de-trapped. As the recovery voltage was weaker, the residual holes that couldn't be de-trapped become more. Fig. 4-6 (a) shows the recovery region of Fig. 4-5. The symbols are measurement data and the solid lines are the fits to the results using the physical model that is built in chapter 3.

$$\Delta V_T = \Delta V_{\max} - \Delta V_{de} = \Delta V_{residue} + \Delta V_{de,MAX} \cdot \exp\left[-\left(\frac{t}{\tau_{e0}}\right)^{\gamma}\right] \quad (4.2)$$

By Eq. (4.2), the four parameters ($\Delta V_{de,MAX}$, $\Delta V_{residue}$, γ, and τ_{e0}) that can well describe the behavior of charge de-trapping are obtained by fitting the symbols of Fig. 4-6 (a). The fitting results: $\Delta V_{de,MAX}$ increased, $\Delta V_{residue}$ decreased, γ decreased, and τ_{e0} decreased (Fig. 4-6 (b)) with stronger recovery voltage. The trends of the four parameters are the same with those of nMOSFETs in chapter 3. Thus, we can know that the hole de-trapping behavior is similar to the electron de-trapping behavior under various recovery voltages in slow traps. However, the holes could be de-trapped only under reverse voltage but the electrons could be de-trapped under the recovery voltage

which is just smaller than stress voltage. Moreover, the electron trapping would happen as the recovery voltage is stronger in pMOSFETs.

Fig. 4-7 shows the threshold voltage shift for pMOSFETs under static stress/recovery time with various recovery voltages V_g=-2.0～-3.0V and a fixed stress voltage V_g =1.0V. The fitting results: $\Delta V_{de,MAX}$ increased, $\Delta V_{residue}$ increased, γ decreased, and τ_{e0} decreased with increasing stress voltage in Fig. 4-8 (a) (b). The trends of the four parameters are the same with those of nMOSFETs in chapter 3. Thus, the hole de-trapping behavior is similar to the electron de-trapping behavior under various stress voltages in slow traps.

4.5 Fluorine Incorporation

Fig. 4-9 (a) (b) show I_d-V_g and Gm-V_g curves of pMOSFETs with dual-layer HfO_2/SiON high-k gate stack in the devices with fluorine and without fluorine. From I_d-V_g curves, drain current would be larger in the device with fluorine. In Gm-V_g curve, the same phenomenon would also be occurred. Turn-on current which varies with gate voltage also represented larger in the device with fluorine in Fig. 4-10. Fig. 4-11 shows I_{cp}-V_{top} curves by charge pumping method of pMOSFETs with dual-layer HfO_2/SiON high-k gate stack in the devices with and without fluorine. From I_{cpmax} of I_{cp}-V_{top} curves, the interface trap density could be obtained. The interface state of with fluorine devices could be improved slightly.

Fig. 4-12 shows the threshold voltage shift as a function of stress time for pMOSFETs under NBT stress in the devices with and without fluorine. The result showed that fluorine incorporation could suppress the V_t shift under NBT stress. However, the improvement mechanisms of fluorine could be interface trap density of Si/SiON or the bulk traps of HfO_2. First, the interface state could be passivated by

fluorine. Thus, Si-H bonds could be replaced by Si-F bonds and the Si-F bonds would be stronger than the Si-H bonds. The Si-F couldn't so easy be broken that the fluorine passivation would suppress the V_t shift. Second, the bulk traps of HfO_2 could be passivated by fluorine and the V_t shift would be suppressed. Fig. 4-13 shows the charge pumping current under fresh and stressed conditions in the devices with and without fluorine. The interface states couldn't be protected under NBT stress by fluorine incorporation. Fig. 4-14 shows the normalized density from the two-frequency CP method in the devices with and without fluorine. The two-frequency CP method can be used to characterize high-k trap generation [5]. The high-k trap density is obtained from the difference between CP results at two frequencies.

$$N_{HK} = \frac{1}{W \cdot L \cdot q}\left[\frac{I_{CP}}{f} - \frac{I_{CP}@1MHz}{1MHz}\right] \tag{4.3}$$

The result of Fig. 4-14 can prove that the fluorine incorporation can suppress the bulk traps generation under NBT stress.

4.6 Fast Hole Trapping Behavior in High-k Gate Dielectric

Fig. 4-15 shows I_d-V_d curves under (a) 25℃ (b) 50℃ (c) 75℃ (d) 125℃ by two measurement methods: DC ramp and pulsed I-V. In Fig. 4-15 (a), the charge loss would be more serious with increasing gate voltage. Moreover, the charge loss would be retarded with increasing the measurement temperature because the de-trapping mechanism is dominant. Compared to nMOSFETs, the temperature effect inducing the de-trapping mechanism is less obvious in pMOSFETs. Fig. 4-16 shows I_d-V_d curves in the devices (a) without and (b) with fluorine by DC ramp and pulsed I-V measurement.

The less charge loss could be showed in the device with fluorine. Moreover, Fig. 4-16 shows I_d-V_d curves in the device (c) without fluorine and (d) with fluorine after stress by DC ramp and pulsed I-V measurement. The less increasing of the generation trap density could be detected in the device of fluorine. The behavior of the fast traps is similar to that of the slow traps in temperature effect and condition effect (with/without fluorine).

4.7 Summary

Hole trapping and de-trapping characteristics are investigated in the pre-existing traps of the HfO_2 high-k gate dielectric. During the constant voltage stress/recovery, V_t shift continues to grow/decay and eventually become saturated, whereas the interface trap density remains unchanged. According to the fitting results with the model discussed in chapter 3, we can find that the trends of the results are similar to that of nMOSFETs. Thus, we can know that the hole trapping and de-trapping behaviors are similar to the electron trapping and de-trapping behaviors in slow traps. The difference is just the intrinsic characteristics between electron and hole. From the temperature effect, the de-trapping mechanism is dominant in the first stage of the stress time and the mechanism of generation traps is dominant as the stress time is prolonged.

Fluorine incorporation can suppress the V_t shift due to many reasons. We can confirm that the improvement is due to the passivation in bulk traps of HfO_2 by our data. The fast traps can be detected by pulsed I-V measurement and the results are similar to those of slow traps in temperature effect and condition effect.

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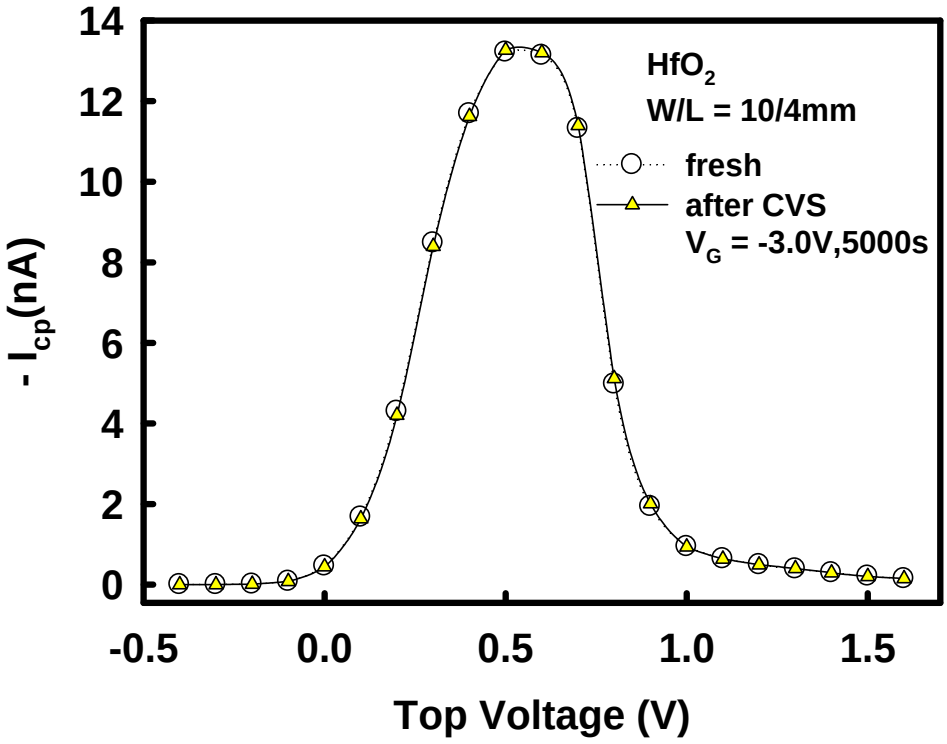


Fig. 4-1 The charge pumping current as a function of top voltage of fresh and stressed conditions.

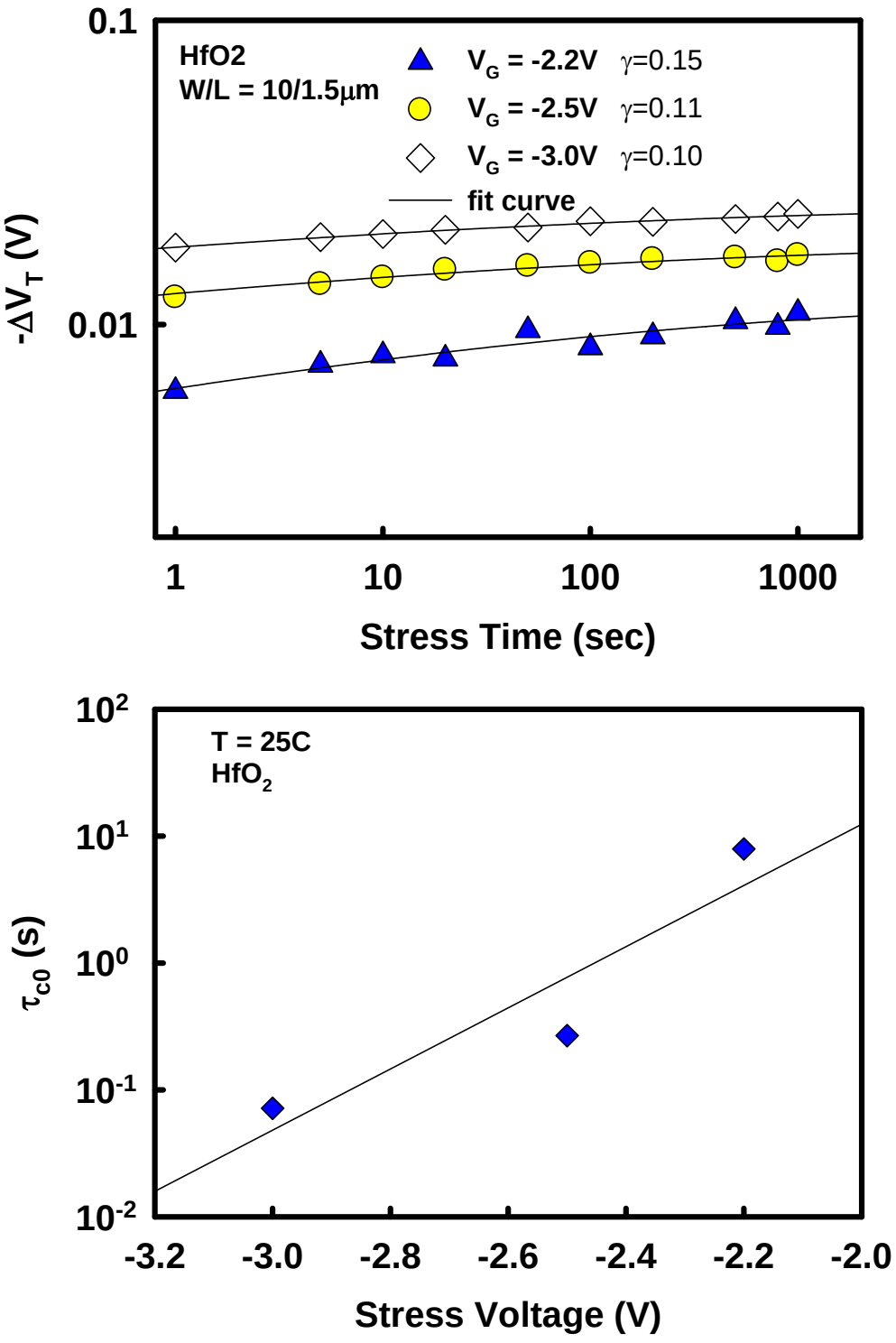


Fig. 4-2 (a) The threshold voltage shift as a function of stress time for HfO_2 high-k gate dielectric under static stress at various gate bias voltages. (b) The characteristic capture time constant under various gate bias voltages.

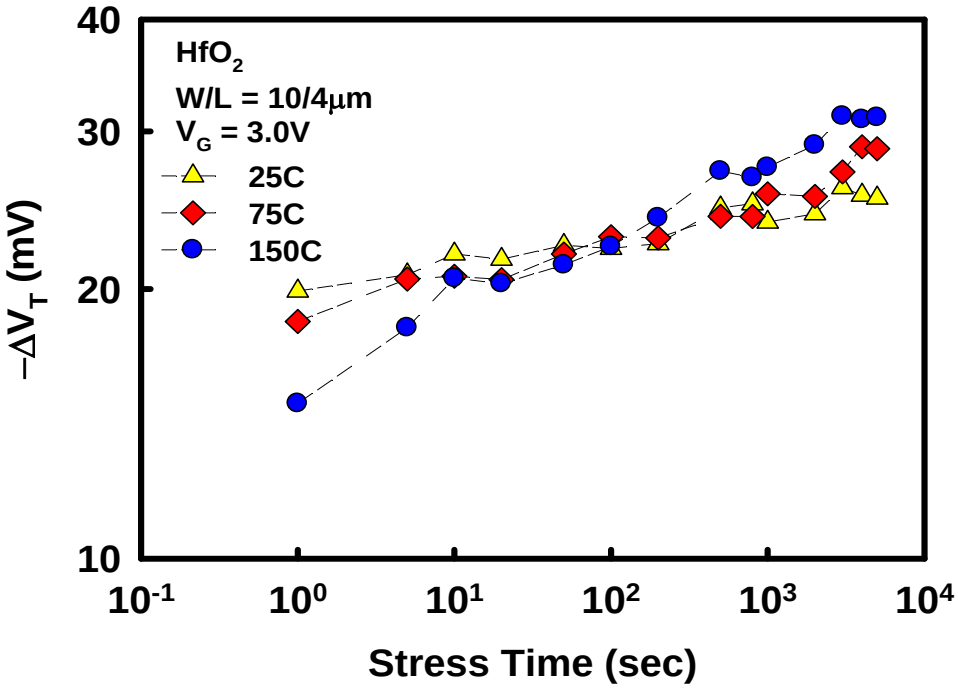


Fig. 4-3 The threshold voltage shift as a function of stress time for pMOSFETs under static stress at various temperatures.

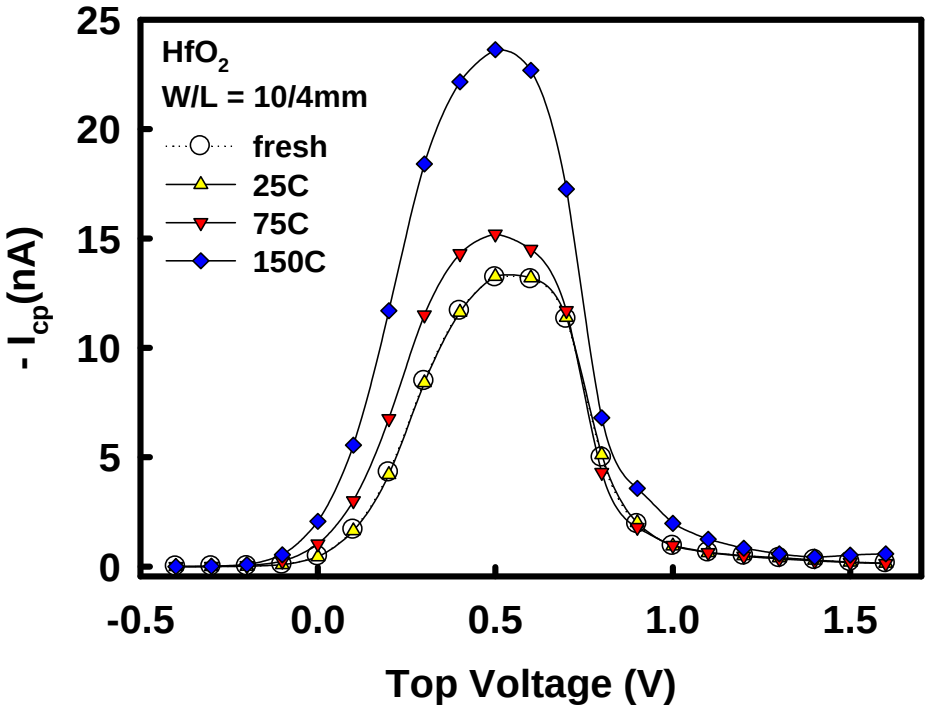


Fig. 4-4 The charge pumping current as a function of top voltage of fresh and stressed conditions under various stress temperatures.

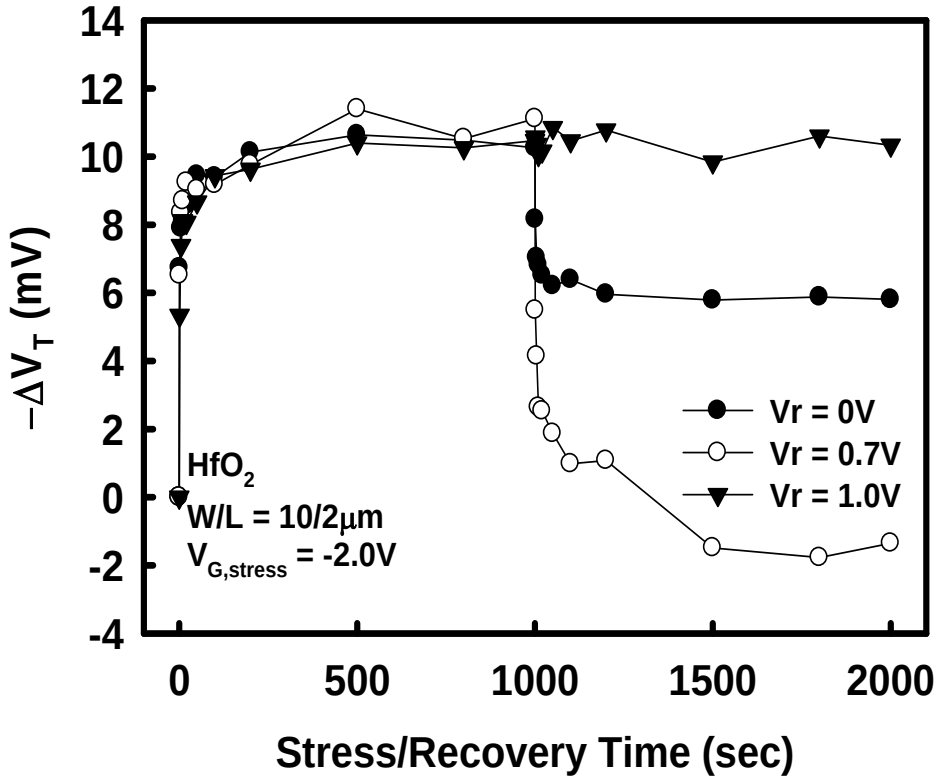


Fig. 4-5 The threshold voltage shift for pMOSFETs under static stress/recovery time with a fixed stress voltage V_g=-2.0V and various recovery voltages V_g =0～1.0V.

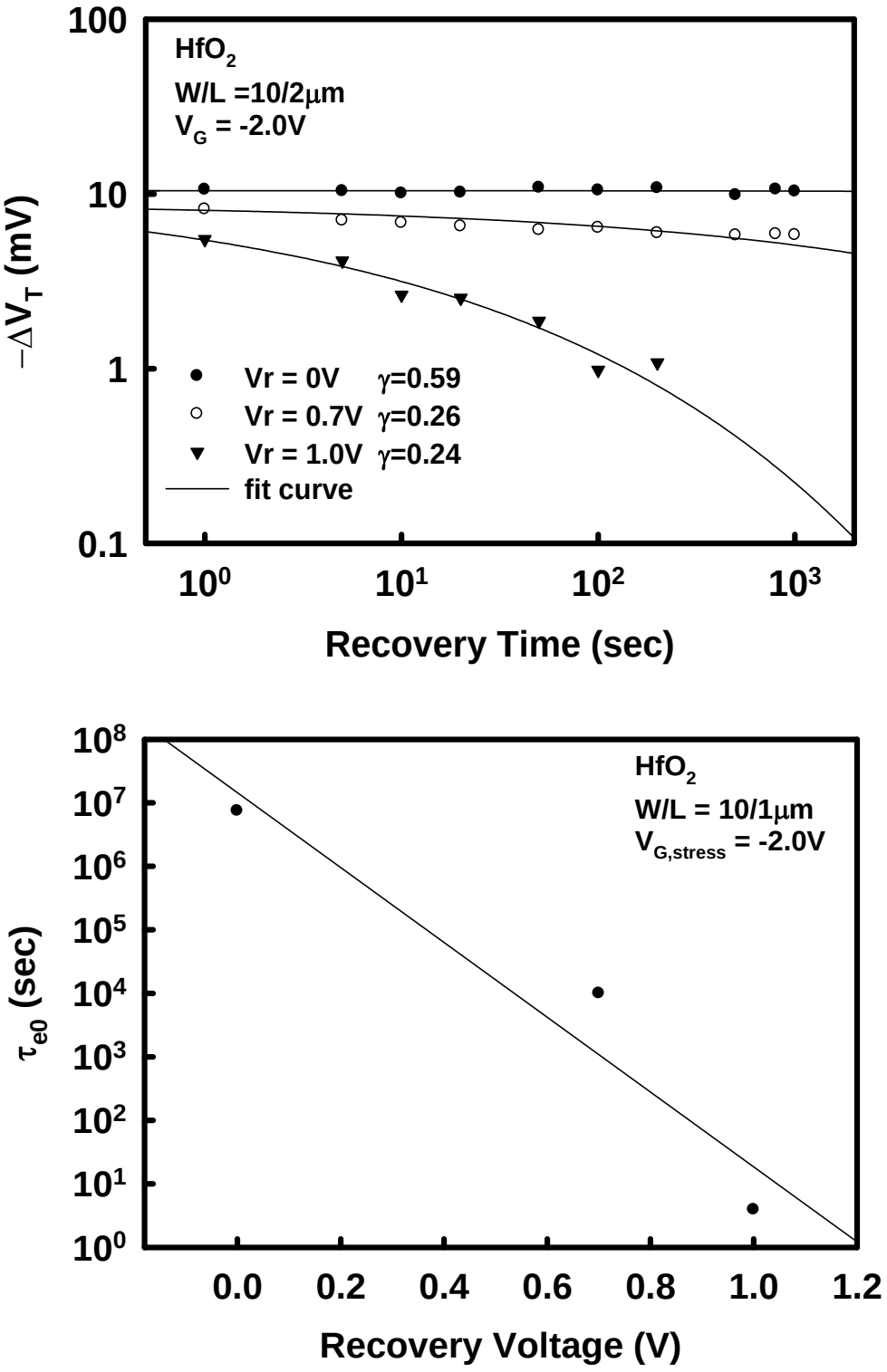


Fig. 4-6 (a) The threshold voltage shift as a function of stress time for HfO_2 high-k gate dielectric under recovery at various recovery voltages. (b) The characteristic emission time constant under various recovery voltages.

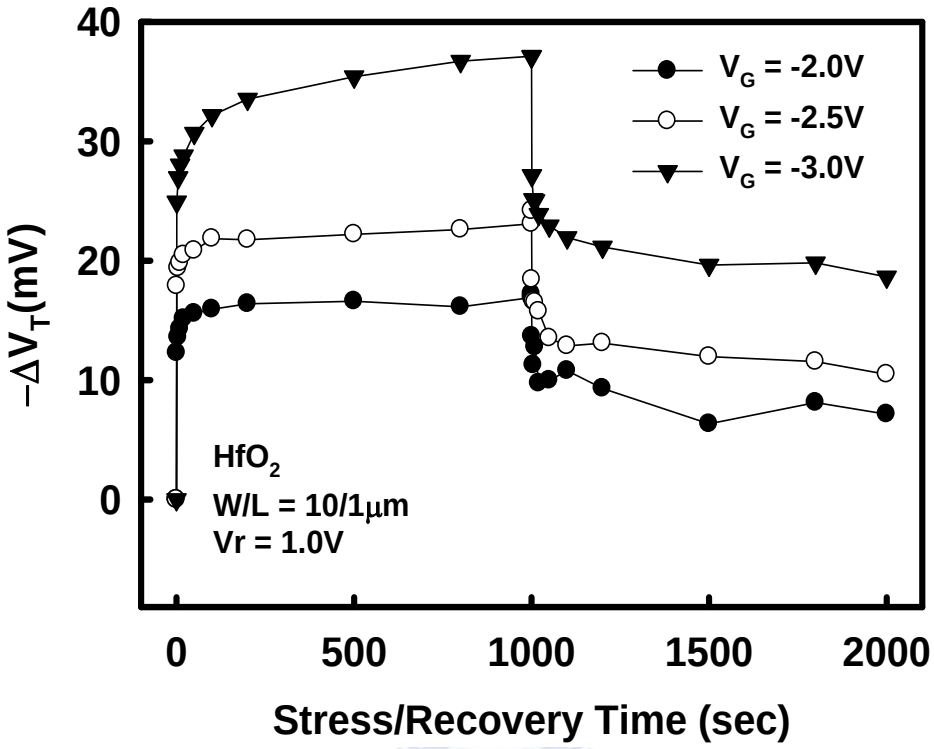


Fig. 4-7 The threshold voltage shift for pMOSFETs under static stress/recovery time with various recovery voltages V_g=-2.0～-3.0V and a fixed stress voltage V_g =1.0V.

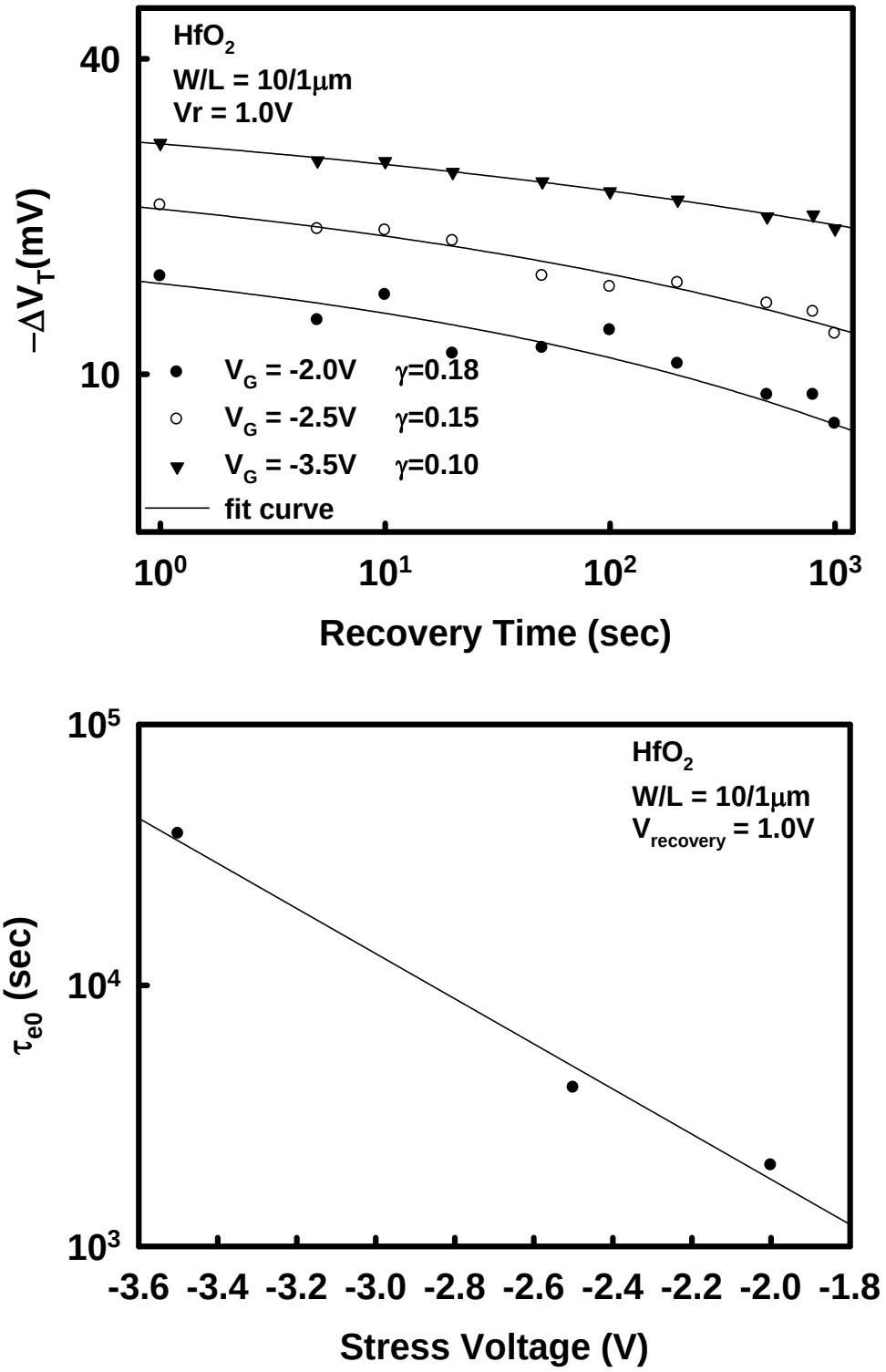
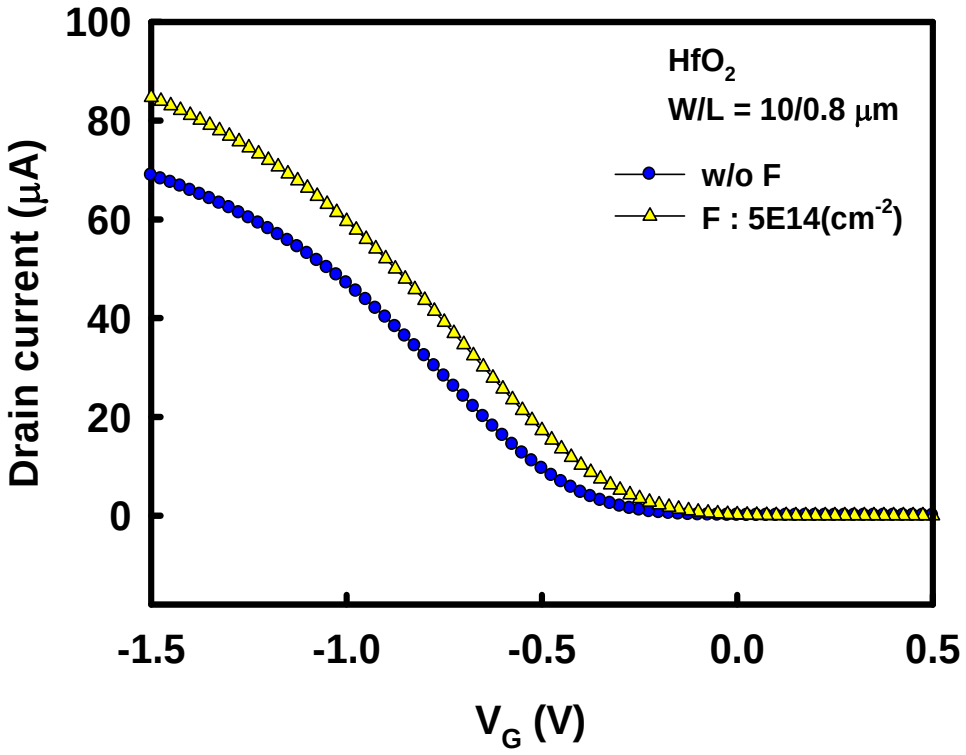


Fig. 4-8 (a) The threshold voltage shift as a function of stress time for HfO_2 high-k gate dielectric under recovery at various stress voltages. (b) The characteristic emission time constant under various stress voltages.



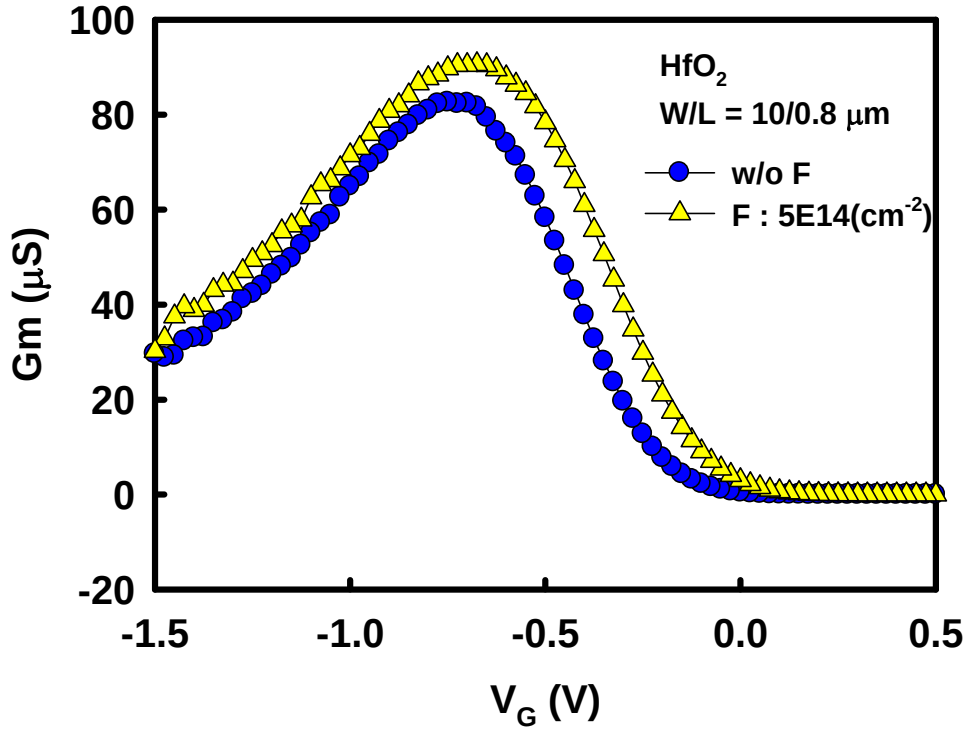


Fig. 4-9 (a) I_d-V_g and (b) Gm-V_g curves of pMOSFETs with dual-layer HfO_2/SiON high-k gate stack in the devices with fluorine and without fluorine.

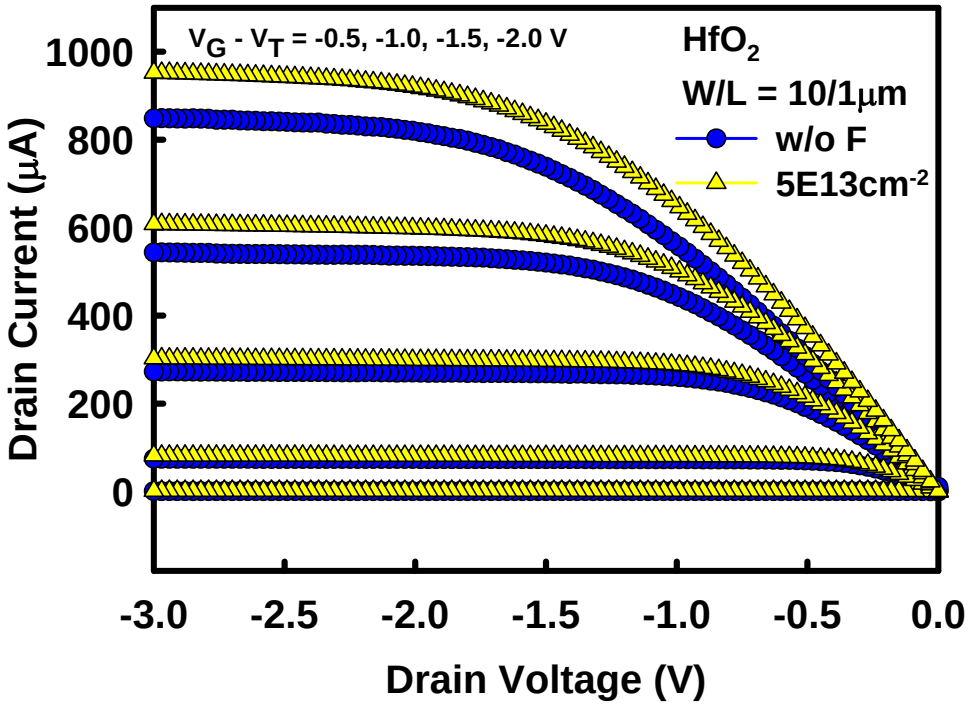


Fig. 4-10 I_d-V_d curves of pMOSFETs with dual-layer HfO_2/SiON high-k gate stack in the devices with and without fluorine.

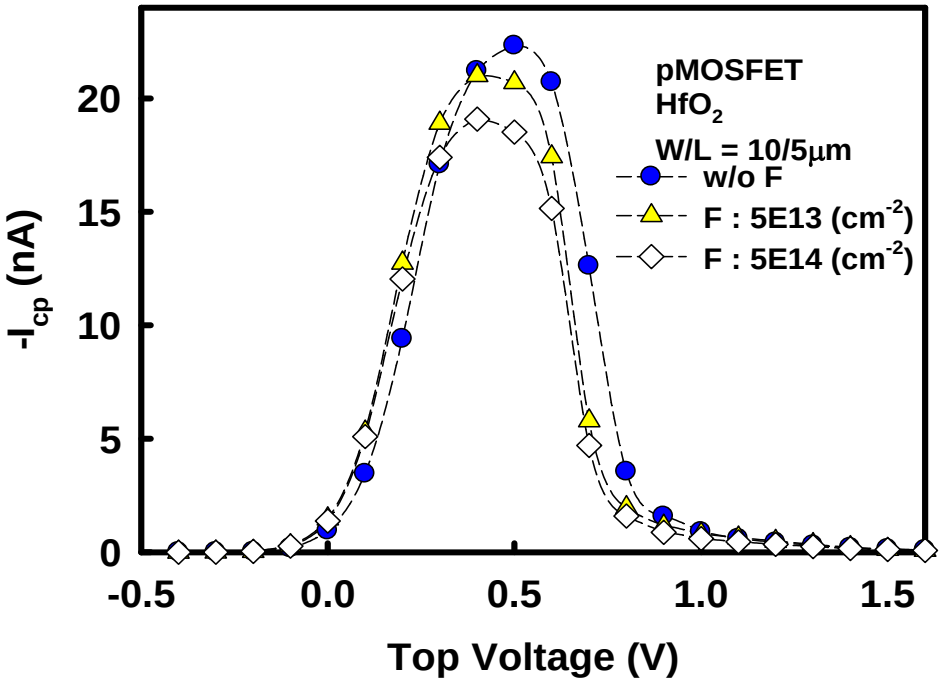


Fig. 4-11 I_{cp}-V_{top} curves of nMOSFETs with dual-layer HfO_2/SiON high-k gate stack in the devices with and without fluorine.

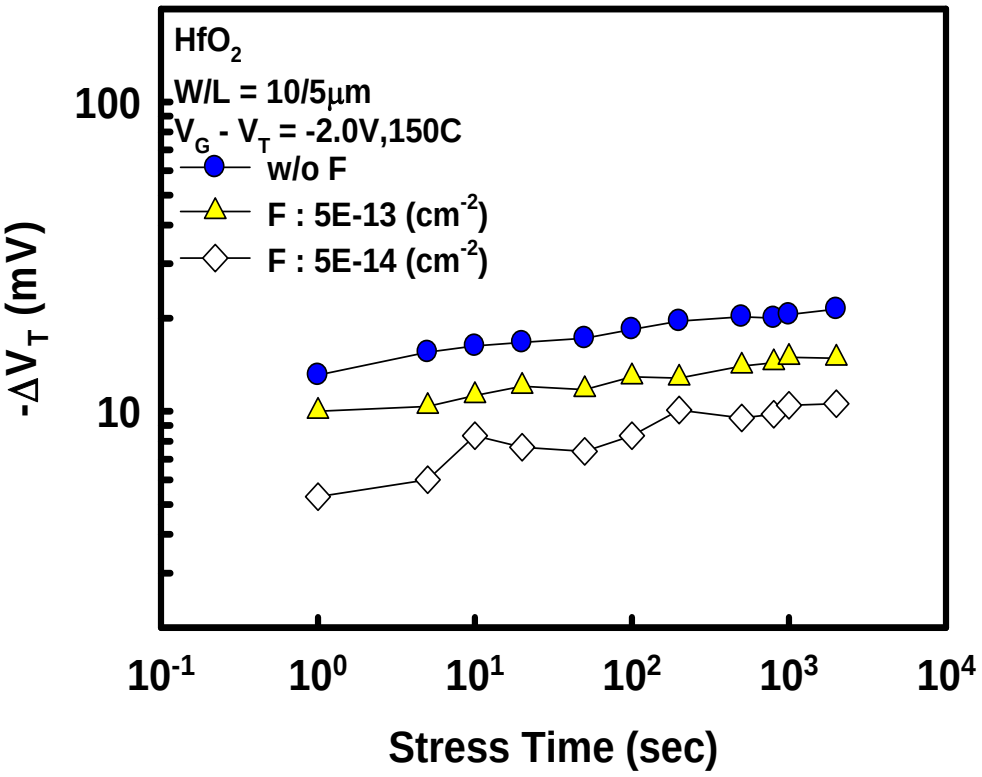


Fig. 4-12 The threshold voltage shift as a function of stress time for pMOSFETs under NBT stress in the devices with and without fluorine.

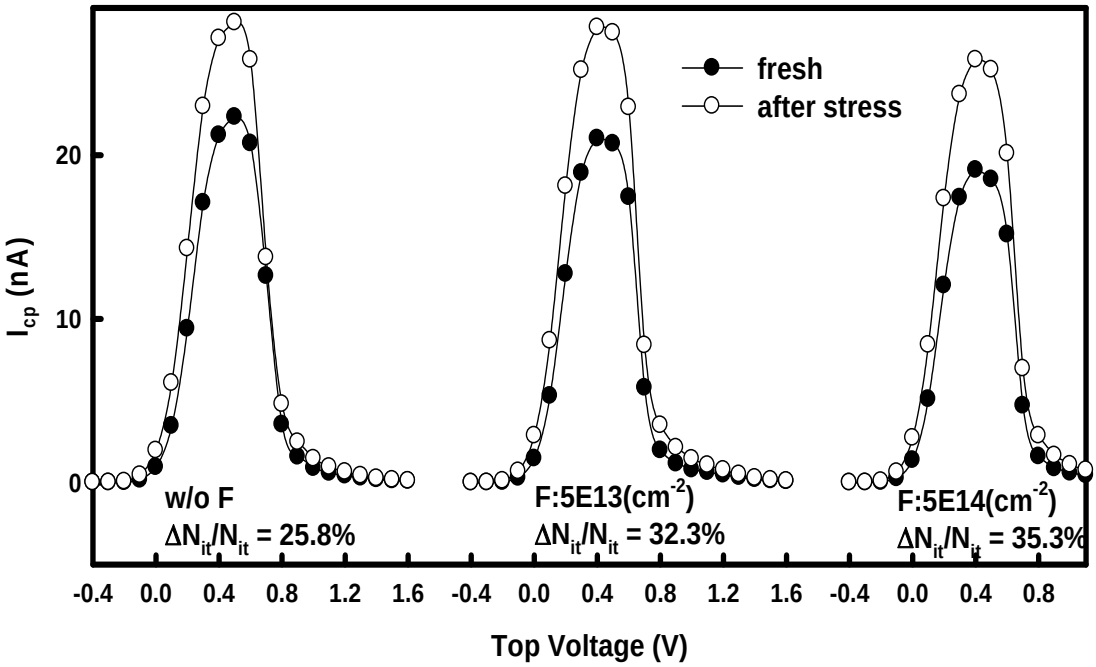


Fig. 4-13 The charge pumping current under fresh and stressed conditions in the devices with and without fluorine.

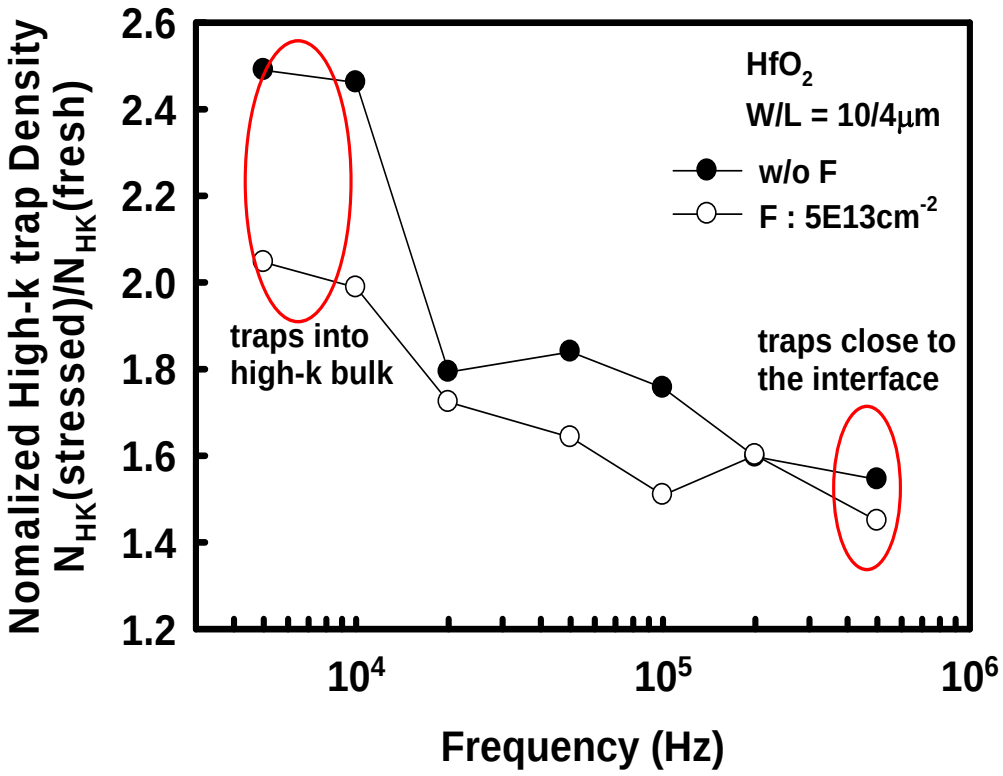


Fig. 4-14 Nonalized high-k trap density (N_{HK}(stressed)/ N_{HK}(fresh)) as a function of frequency in the devices with and without fluorine.

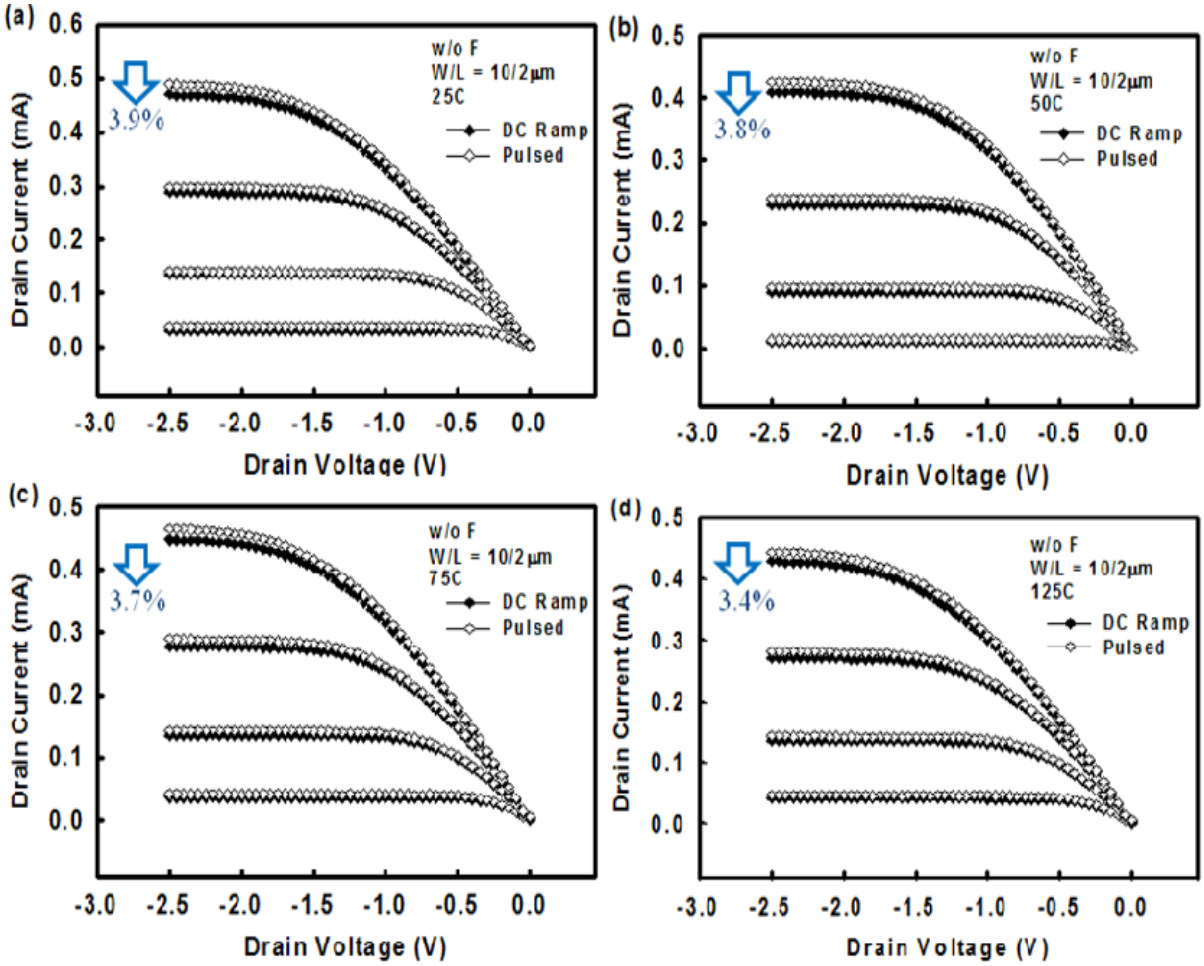


Fig. 4-15 I_d-V_d curves under (a) 25℃ (b) 50℃ (c) 75℃ (d) 125℃ by two measurement methods: DC ramp and pulsed I-V.

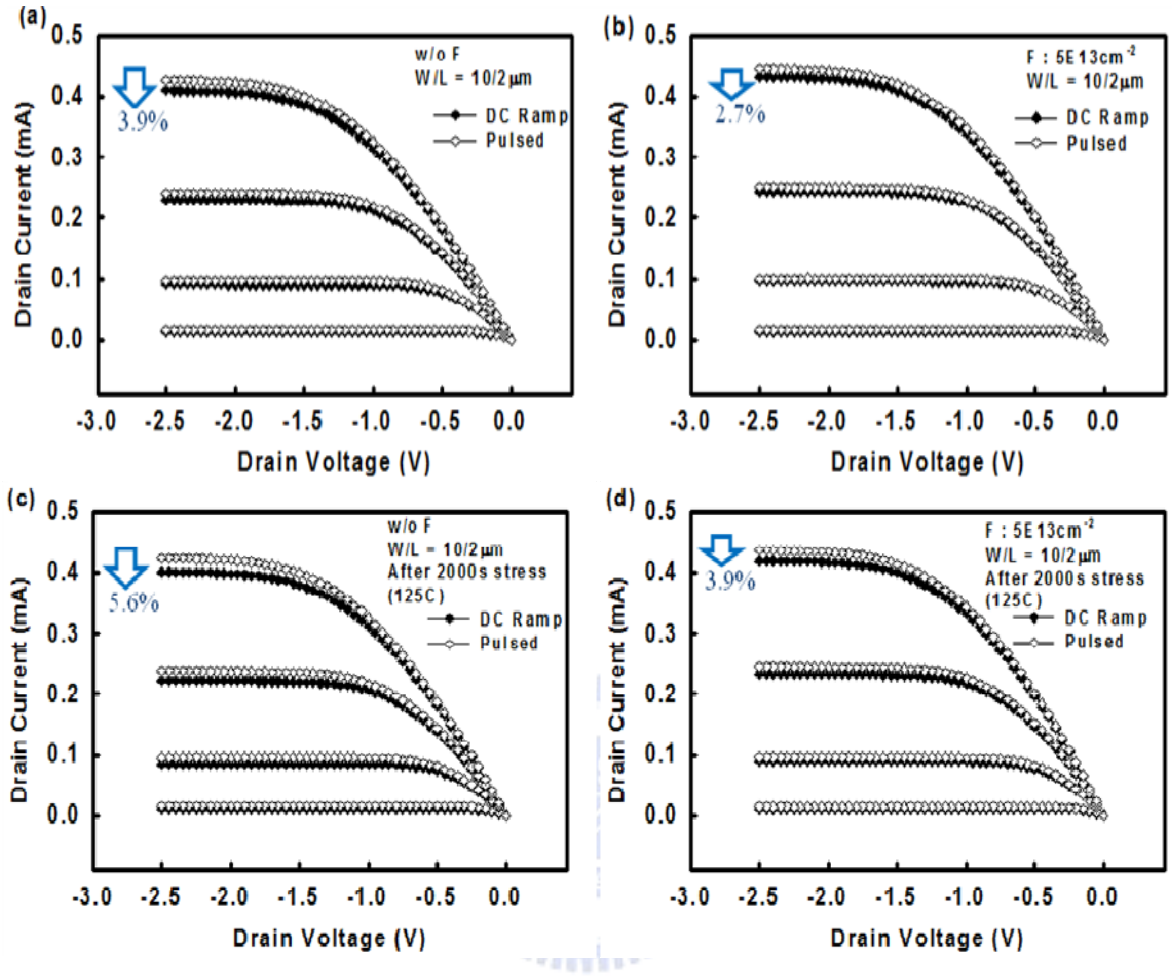


Fig. 4-16 I_d-V_d curves in the devices (a) without and (b) with fluorine by DC ramp and pulsed I-V measurement. I_d-V_d curves in the device (c) without fluorine and (d) with fluorine after stress by DC ramp and pulsed I-V measurement.

Chapter 5
Conclusions and Suggestions for Future Work

5.1 Conclusions

In this thesis, the fundamental characteristics and the physical mechanisms of charge trapping and de-trapping in the pre-existing traps in Hf-based high-k gate dielectrics have been studied. The basic electrical characteristics and the charge trapping behaviors of the strain effect in NMOS and the fluorine effect in PMOS also have been discussed completely.

In chapter 2, the strained devices could improve the electrical characteristics of NMOS, but they would induce more threshold voltage shift in high-k material. By F-P and F-N tunneling fitting, we conclude that the strain effect induces bulk traps generated in HfO_2. In chapter 3, according to the fitting results with the model proposed by Zafar et al., we can find that the total density of traps is not a fixed value but dependent on stress voltage and the distribution factor of capture time is dependent on not only high-k materials but also stress voltages. Moreover, the fitting results can build the distribution of the trapped charge density with capture time. The recovery model can be built base on the charge trapping model and the recovery model can well fit the measurement data. In chapter 4, According to the fitting results with the model discussed in chapter 3, we can know that the hole trapping and de-trapping behaviors are similar to the electron trapping and de-trapping behaviors in slow traps. The difference is just the intrinsic characteristics between electron and hole. Moreover, we can confirm that the improvement of the fluorine incorporation is due to the passivation in bulk traps of HfO_2 by our data.

5.2 Suggestions for Future Work

There are some works valuable for future researches:

1. The hydrogen passivation of the strain effect could be found in the electrical characteristics. Thus, we can research in the physical analysis to assist our inference from the electrical analysis.
2. The physical model could apply to our data suitably. However, the threshold voltage shift and the drain current degradation would be underestimated because the so-called fast traps couldn't be detected by conventional DC I-V measurement. Thus, the combination of the stress mode and the pulsed I-V measurement is necessary to obtain the actual data.
3. The fluorine passivation of the fluorine incorporation effect could be found in the electrical characteristics. Thus, we can research in the physical analysis to assist our inference from the electrical analysis.
4. The strain effect in PMOS and the fluorine effect in NMOS can also be investigated.

個人簡歷(Vita)

姓名: 詹効諭

性別: 男

生日: 09/19

籍貫: 台灣省苗栗縣

住址: 苗栗縣苗栗市建功里民族路 62 號

學歷: 國立中央大學機械工程學系

90 年 9 月 – 94 年 6 月

國立交通大學電子研究所碩士班

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在二氧化鉿為基底之高介電係數閘極介電層中的載子捕捉與逃逸的電性行為

Charge Trapping and De-trapping Behavior in Hf-Base High-k Gate Dielectrics