國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩　士　論　文

90 奈米互補式金氧半製程下之多功能輸入/輸出元件庫設計

Design of Configurable I/O Cell Library in 90-nm CMOS Process

研 究 生：陳世範　(Shih-Fan Chen)

指導教授：柯明道教授　(Prof. Ming-Dou Ker)

中華民國九十七年九月

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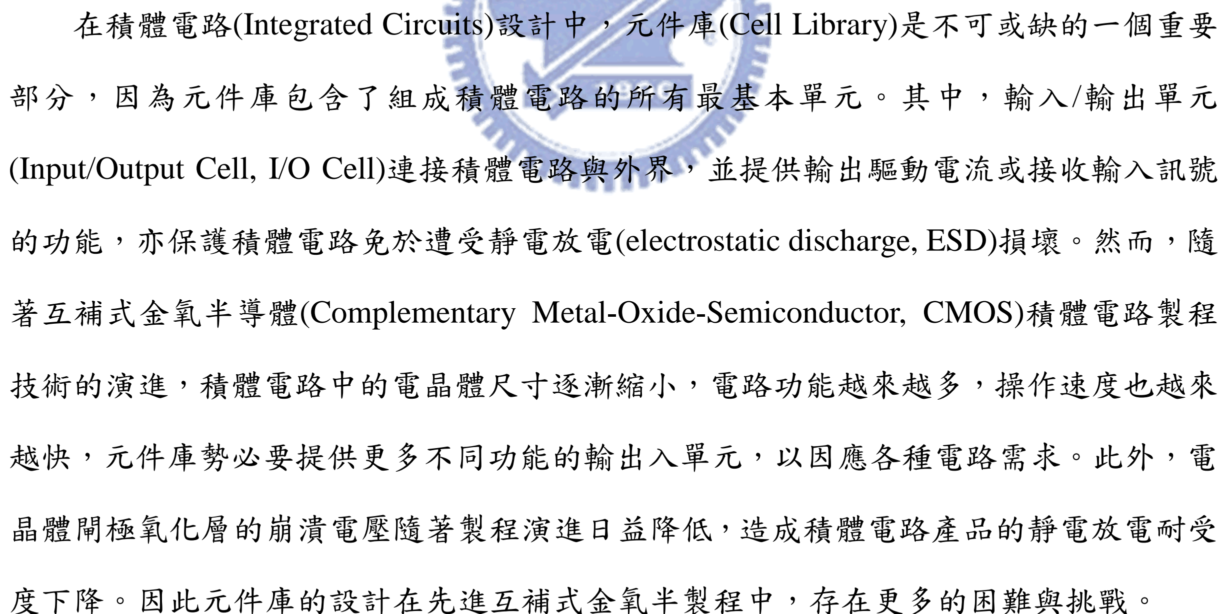
ABSTRACT (CHINESE)



在積體電路(Integrated Circuits)設計中，元件庫(Cell Library)是不可或缺的一個重要部分，因為元件庫包含了組成積體電路的所有最基本單元。其中，輸入/輸出單元(Input/Output Cell, I/O Cell)連接積體電路與外界，並提供輸出驅動電流或接收輸入訊號的功能，亦保護積體電路免於遭受靜電放電(electrostatic discharge, ESD)損壞。然而，隨著互補式金氧半導體(Complementary Metal-Oxide-Semiconductor, CMOS)積體電路製程技術的演進，積體電路中的電晶體尺寸逐漸縮小，電路功能越來越多，操作速度也越來越快，元件庫勢必要提供更多不同功能的輸出入單元，以因應各種電路需求。此外，電晶體閘極氧化層的崩潰電壓隨著製程演進日益降低，造成積體電路產品的靜電放電耐受度下降。因此元件庫的設計在先進互補式金氧半製程中，存在更多的困難與挑戰。

本論文在 90 奈米互補式金氧半製程中，設計並驗證一套輸入/輸出元件庫，此多功能輸入/輸出元件庫包含多功能輸入/輸出單元(Configurable I/O Cell)、電源單元(Power Cell)、類比輸入/輸出單元(Analog I/O Cell)和電源切斷單元(Power Break Cell)。輸出單元內可以控制電流驅動能力，並可在三態(Tri-State)時選擇是否具有拉高(Pull Up)至高邏輯

準位(Logic High)或拉低(Pull Down)至低邏輯準位(Logic Low)之功能。在輸入單元部分，可以選擇是否具有史密特觸發(Schmitt-Trigger)功能，以提升對輸入訊號的雜訊抵抗能力，這些功能皆由單一輸出入單元完成。此外，隨著瞬間輸出電流增加，接地電位彈跳現象(Ground Bounce)將越來越嚴重，使得電路可能發生功能錯誤的現象。本輸入/輸出單元亦提供一個具有電壓迴轉率控制(Slew-Rate Control)的多功能輸出入單元以抑制接地電位彈跳現象。靜電放電防護方面，本輸入/輸出元件庫提供了多組高效能靜電放電防護電路，以建構完整的全晶片(Whole-Chip)靜電放電防護。本論文以 90 奈米互補式金氧半製程設計並製作此輸入/輸出元件庫，實驗晶片的量測結果已成功驗證此輸入/輸出元件庫之所有功能，包含接收輸入訊號、傳送輸出訊號、電壓迴轉率控制與全晶片靜電放電防護。

Design of Configurable I/O Cell Library in 90-nm CMOS Process

Student: Shih-Fan Chen **Advisor: Prof. Ming-Dou Ker**

Department of Electronics Engineering and Institute of Electronics

National Chiao-Tung University

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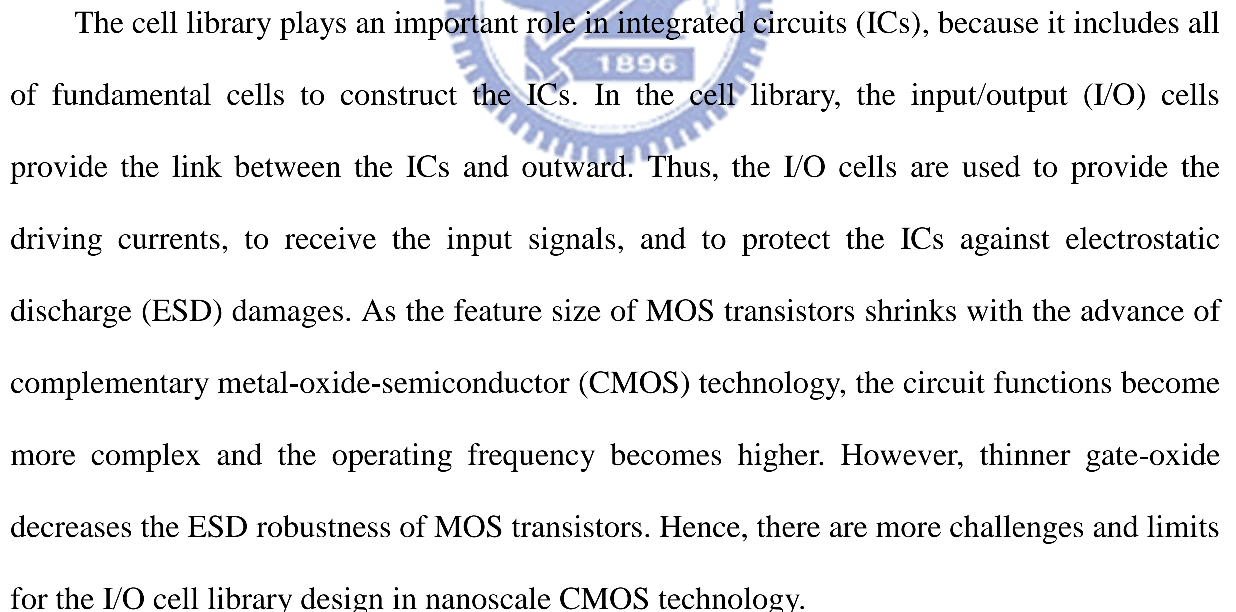

The cell library plays an important role in integrated circuits (ICs), because it includes all of fundamental cells to construct the ICs. In the cell library, the input/output (I/O) cells provide the link between the ICs and outward. Thus, the I/O cells are used to provide the driving currents, to receive the input signals, and to protect the ICs against electrostatic discharge (ESD) damages. As the feature size of MOS transistors shrinks with the advance of complementary metal-oxide-semiconductor (CMOS) technology, the circuit functions become more complex and the operating frequency becomes higher. However, thinner gate-oxide decreases the ESD robustness of MOS transistors. Hence, there are more challenges and limits for the I/O cell library design in nanoscale CMOS technology.

In this thesis, an I/O cell library is designed in 90-nm CMOS technology. The I/O cell library includes the configurable I/O cells, analog I/O cells, power cells, and power break cell. In the configurable I/O cell, the output stage is used to provide driving current. Besides, it can

pull the I/O pad up to logic high or pull the I/O pad down to logic low under the tri-state. In input stage, a schmitt-trigger is realized and can be turned on to increase the noise margin of input signal. All of the aforementioned functions have been integrated in a single configurable I/O cell proposed in this thesis. Moreover, the ground bounce issue becomes more critical as the instantaneous driving current becomes larger. In the proposed I/O cell library, the slew-rate-control unit is realized in another configurable I/O cell to mitigate the ground bounce issue. In addition, several effective ESD protection circuits are designed in this I/O cell library to provide whole-chip ESD protection. The proposed I/O cell library has been fabricated in 90-nm CMOS process. Experimental results have successfully verified all of the functions provided in the I/O cell library, including receiving input signals, transmitting output signals, slew-rate control, and whole-chip ESD protection.

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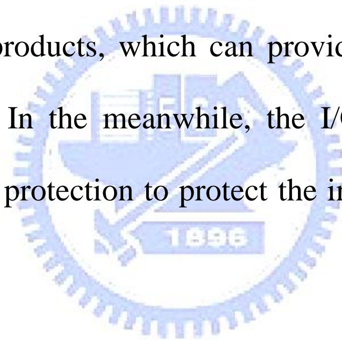
Chapter 1

Introduction

1.1 MOTIVATION

In the digital integrated circuits (ICs) or mixed-signal ICs designs of the system-on-a-chip (SoC) and VLSI system, the cell libraries are often used to accelerate the design process to achieve the time-to-market requirement. The I/O (input/output) cell is an essential element in the IC products, which can provide enough output driving currents or receive the external signals. In the meanwhile, the I/O cell also can provide a sufficient electrostatic discharge (ESD) protection to protect the internal circuits and I/O circuits inside the ICs.



1.1.1 Issue of I/O Interface

With new generations of CMOS technologies, the dimensions of transistors have been scaled down to reduce the silicon cost, and to increase circuit performance (ex., operating speed). However, since the thickness of gate-oxide becomes much thinner, several problems such as gate-oxide reliability [1] and hot-carrier degradation [2] will be faced. Thus, the core power supply voltage (VDD) must be correspondingly decreased to ensure the ICs lifetime. Since the power supply voltage has been reduced, it will decrease lower power consumption to achieve the purpose of low power. In order to increase the circuit performance and decrease the power consumption, generally the internal or core circuit is designed with thin-oxide

devices and lower power supply. But the I/O cell may receive or transmit a higher voltage level signal at the I/O interface. Therefore, in this thesis, the thick-oxide devices have been used to prevent the reliability issue. When such I/O cell receives a high voltage level signal, the signal will be transformed into a low voltage level signal and then it will be transmitted to the internal circuit. As a result, there is no need to concern the reliability issues while the internal circuit will be designed with the thin-oxide devices and operated with low voltage supply.

In high-speed interface, the output buffer is a major contributor to the pin-to-pin delays because of output loading as well as package and aboard parasitic. The channel widths of output buffer are always increased to achieve high driving capability and high speed, which results in large power/ground noise due to output drivers switching simultaneously. Since the input pads are connected to the same power/ground buses, power/ground noise must be well controlled to avoid any false switching. Even though the internal power/ground buses are separated from the external (I/O buffers) power/ground buses, they are connected through a VDD/VSS package plane in multilayer package. Therefore, the output buffer must be designed with considerations of power/ground noise to achieve high performance.

In this thesis, two configurable I/O cells are designed to provide different driving capacities, turn on/off the pull-up or pull-down mechanism, and switch on/off the function of schmitt-trigger when the I/O circuit operates in transmitting mode, tri-state, and receiving mode, respectively. Instead of providing different cells as general I/O cells, the configurable I/O cells combine most functions to meet different specification requirement. Beside, the difference between these two configurable I/O cells is the output buffer without or with slew-rate control mechanism. The configurable I/O cell with slew-rate control is designed with considerations of power/ground noise.

1.1.2 Issue of ESD

ESD has become the main reliability concern on semiconductor products, especially for the SoC implementation in nanoscale CMOS processes. The ESD specifications of commercial IC products are generally required to be higher than 2kV in human-body-model (HBM) and 200V in machine-model (MM) [3] ESD stress. Therefore, on-chip ESD protection circuits have to be added between the input/output pad and VDD/VSS to provide the desired ESD robustness in CMOS ICs [4]-[6]. ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode), as shown in Fig. 1.1(a) ~ 1.1(d), respectively. The typical design of on-chip ESD protection circuits in a CMOS IC is illustrated in Fig. 1.2. To avoid the unexpected ESD damage in the internal circuits of CMOS ICs [7]-[9], the turn-on-efficient power-rail ESD clamp circuit is placed between VDD and VSS power lines [10]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of PMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground as shown in Fig. 1.3. Consequently, the I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [10].

In this thesis, a new set I/O cell library is proposed to assist the digital or mixed-signal IC design with effective ESD protection circuits to enhance the ESD level in SoC implementations. The configurable I/O cell library has been fabricated and verified in UMC 90-nm salicide CMOS process.

1.2 INTRODUTION OF CONFIGURABLE I/O CELL LIBRARY

Table 1.1 lists the cell categories and functions of the configurable I/O cell library. This

I/O cell provides two configurable I/O cells named UCIONS (without slew-rate control mechanism) and UCIOS (with slew-rate control mechanism). While the configurable I/O cell operates in transmitting mode, 7 different output driving currents can be selected in the I/O cell. When the I/O cell operates in receiving mode, the I/O cell becomes an input cell and can be selected with or without the function of schmitt-trigger. When the configurable I/O cell operates in tri-state mode, the functions of pull-up and pull-down can be turned on or off separately. Thus, in this situation, the voltage level at the I/O PAD can be biased at high or low or floating. The analog signals can be transmitted by the analog I/O cell (UAIO25 or UAIO10) which is composed of ESD protection circuit only. The I/O cell library provides four power cells (UVDD25, UVSS25, UVDD10, and UVSS10). The UVDD25 and UVSS25 cells are used to provide the supply voltages for I/O ring, and the UVDD10 and UVSS10 are used to provide the supply voltages for pre-driver and internal circuits.

1.3 THESIS ORGANIZATION

In chapter 2, the DC specification of this configurable I/O cell will be listed, and the circuit design and the simulation results of the configurable I/O cell will be specified. The design of ESD protection circuits will be introduced in chapter 3. The whole layout implementation of the I/O cell library will be shown in chapter 4. Besides, in chapter 5, the test chip arrangement for function verification and ESD robustness tests will be illustrated. The experimental results will be shown in chapter 6. Finally, the last chapter ends with a few concluding statements pertaining to the research as well as recommendations for future work in the area.

Tabel 1.1

Configurable I/O cell library.

<table>
<tr><th colspan="3">I/O Cells</th></tr>
<tr><th>Cell Name</th><th>Function</th><th>Pins</th></tr>
<tr><td>UCIOS</td><td>Configurable I/O Cell with Slew-Rate Control</td><td>PAD, I, S0, S1, S2, PD, PU, SCH, C</td></tr>
<tr><td>UCIONS</td><td>Configurable I/O Cell without Slew-Rate Control</td><td>PAD, I, S0, S1, S2, PD, PU, SCH, C</td></tr>
<tr><td>UINPUT</td><td>Input Cell</td><td>PAD, C</td></tr>
<tr><td>UAIO25</td><td>Analog I/O for 2.5 V</td><td>PADwiR, PADwoR</td></tr>
<tr><td>UAIO10</td><td>Analog I/O for 1.0 V</td><td>PADwiR, PADwoR</td></tr>
<tr><th colspan="3">Power Cells</th></tr>
<tr><th>Cell Name</th><th>Function</th><th>Pins</th></tr>
<tr><td>UVDD25</td><td>Positive Power Source for I/O Ring</td><td>VDDIO</td></tr>
<tr><td>UVSS25</td><td>Ground Supply for I/O Ring</td><td>VSSIO</td></tr>
<tr><td>UVDD10</td><td>Positive Power Source for Pre-Driver and Core Circuit</td><td>VDD</td></tr>
<tr><td>UVSS10</td><td>Ground Supply for Pre-Driver and Core Circuit</td><td>VSS</td></tr>
<tr><td>UPBREAK</td><td>Power Bus Break Cell</td><td></td></tr>
<tr><th colspan="3">Other Cells</th></tr>
<tr><th>Cell Name</th><th colspan="2">Function</th></tr>
<tr><td>UFeederXX</td><td colspan="2">0.1, 0.3, 0.5, 1, 2, 5, 10, 15 and 20μm-Width of Filler Cells for Interconnection</td></tr>
<tr><td>UCorner</td><td colspan="2">Corner Cell</td></tr>
<tr><th colspan="3">Physical Dimension of Cells</th></tr>
<tr><td>Cell Pitch</td><td colspan="2">61.5μm per cell</td></tr>
<tr><td>Cell Hight</td><td colspan="2">101.9μm</td></tr>
<tr><td>Metal Layers</td><td colspan="2">Suitable for 4 ~ 9 layers</td></tr>
</table>

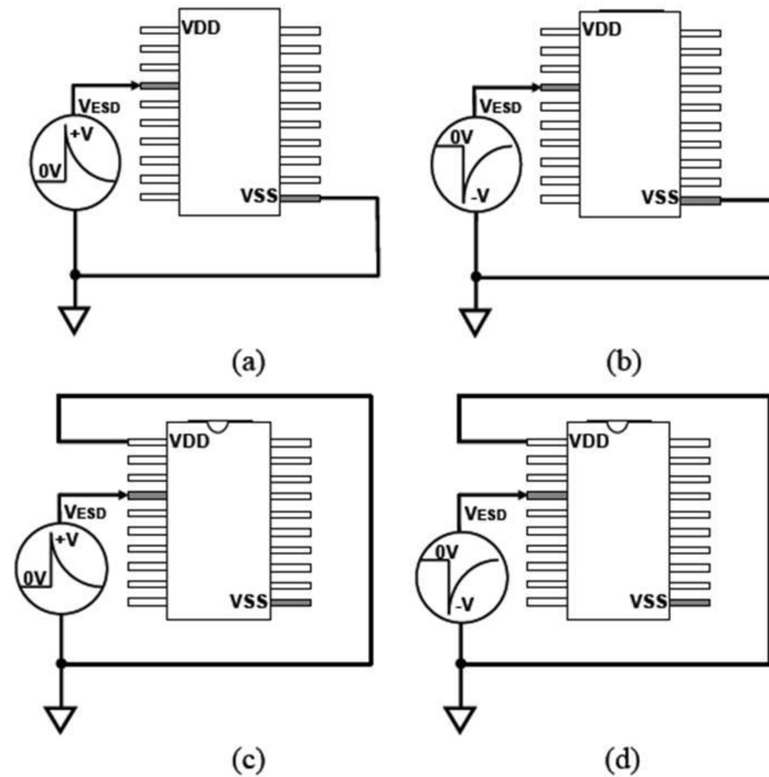


Fig. 1.1 The four pin-combination modes for ESD test on an IC product: (a) positive-to-VSS (PS-mode), (b) negative-to-VSS (NS-mode), (c) positive-to-VDD (PD mode), and (d) negative-to-VDD (ND-mode).

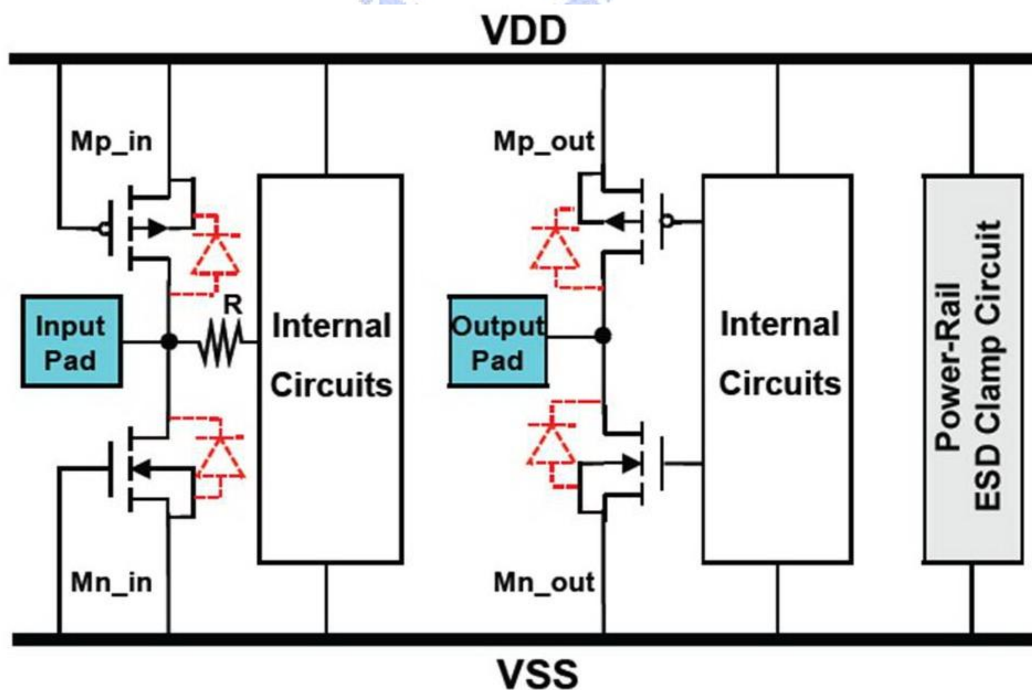


Fig. 1.2 Typical on-chip ESD protection circuits in a CMOS IC.

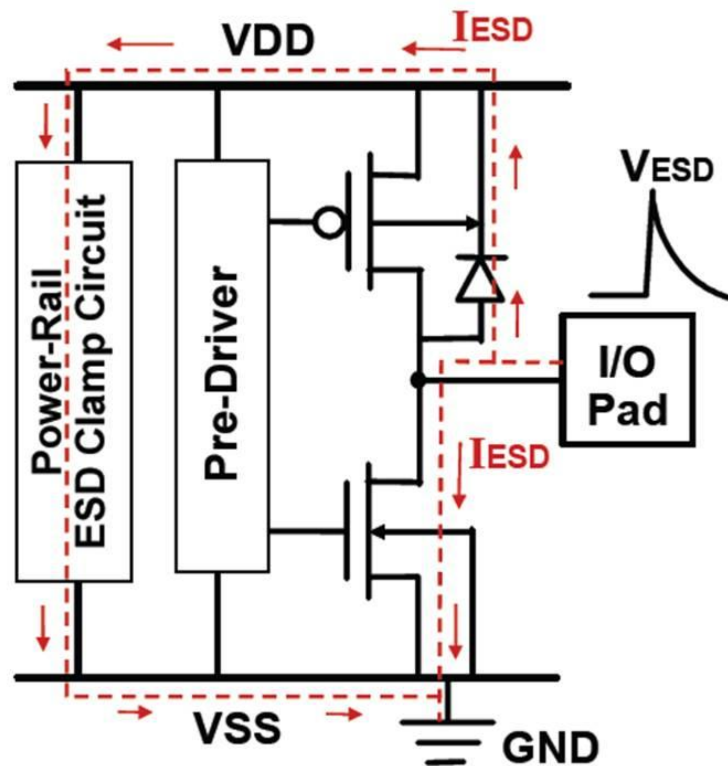


Fig. 1.3 The ESD current paths of the I/O pad with power-rail ESD clamp circuit under the positive-to-VSS (PS-mode) ESD stress. The ESD current paths are indicated by the dashed lines.

Chapter 2

Design and Simulation Results of Configurable I/O Cell

2.1 INTRODUCTION OF CONFIGURABLE I/O CELL

Fig. 2.1 shows the circuit block diagram of the configurable I/O cell and the function of each block circuit is defined as follows:

- Pre-driver: The driving select signals, S0, S1, and S2, are used to control the configurable I/O cell operating in transmitting mode or in receiving mode (tri-state input mode). When the configurable I/O cell operates in transmitting mode, the pre-driver generates pull up signals, P0, P1, and P2, and pull down signals, N0, N1, and N2. Therefore, the output transistors NMOS and PMOS can be turned on (off) separately to change the output driving capability.
- Level shifter: The voltage level of operation signal is shifted from low (VSS-to-VDD) to high (VSSIO-to-VDDIO).
- Output stage: When the configurable I/O cell operates in transmitting mode, the low voltage level (VSS-to-VDD) at the data input signal, I, will be transformed into the high voltage level (VSSIO-to-VDDIO) at the I/O PAD. Consequently, different amount of output transistors NMOS/PMOS turned on will result in different output driving capability.
- Input stage: When the configurable I/O cell operates in receiving mode, the

schmitt-trigger control signal, SCH, controls input stage to become normal input stage or schmitt-trigger input stage. Moreover, the configurable I/O cell in receiving mode receives VSSIO-to-VDDIO input signal at the I/O PAD and then transmits VSS-to-VDD output signal to core circuit through the input stage.

- Pull-up/Pull-down network: When the driving select signals S0, S1, and S2 are biased at 0V and the I/O PAD is floating, the configurable I/O cell operates in tri-state. In this situation, the mechanism of pull-up and pull-down can be turned on or off by the pull up signal PU and the pull down signal PD.

- Slew-rate control: When the output stage operates with slew-rate control circuit, the simultaneous switching noise (SSN) can be reduced significantly.

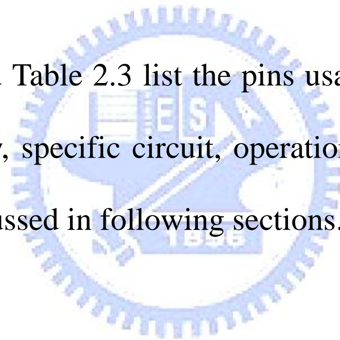


Table 2.1, Table 2.2, and Table 2.3 list the pins usage and functions of configurable I/O cell. Besides, the design flow, specific circuit, operation principle, and simulation results of configurable I/O cell are discussed in following sections.

2.2 BASIC SPECIFICATION

In this configurable I/O cell library, the typical core power supply voltage (VDD) and I/O output driver power supply voltage (VDDIO) are 1.0V and 2.5V. However, the library is also compatible with 1.8-V ~ 3.3-V design window of VDDIO. Therefore, the information of this library will be provided not only with 2.5-V VDDIO, but also with 1.8-V and 3.3-V VDDIO supply voltage in following introduction. Table 2.4, Table 2.5, and Table 2.6 list the DC specification of configurable I/O cell under 2.5-V, 1.8-V, and 3.3-V VDDIO supply voltage, respectively.

2.3 OUTPUT STAGE

2.3.1 Driving Capability

In order to design an output cell with variable driving capability, the transistors of output driver are distributed into three groups, MP0/MN0, MP1/MN1, and MP2/MN2 as shown in Fig. 2.1. The specification on dc driving currents of the configurable I/O cell are defined as 2mA, 8mA, 10mA, 14mA, 16mA, 22mA, and 24mA with different output MOS fingers. When the output driving current is 2mA, the finger number of the output driver is one. Similarly, when the output driving current is 24mA, the finger numbers of the output driver are 12 fingers.

The driving select signals, S2, S1, and S0, are used not only to control the operating mode, but also to choose the output driving capability in transmitting mode. In order to distribute the output driving current equally, 12 fingers of output drive are divided into three groups in parallel. The transistor MP0/MN0 is designed with only one finger, and MP1/MN1 and MP2/MN2 are composed of 4 fingers and 7 fingers, respectively. The relation between the driving capability and the driving select signals (S0, S1, and S2) has been mentioned in Table 2.2. Moreover, the design flow of output driver will be introduced in next paragraph. However, several parameters should be defined firstly in this section as follows:

- I_{OL}: The sink current at I/O PAD of configurable I/O cell when the voltage at I/O PAD of configurable I/O cell is biased at V_{OL} (= 0.4V), as shown in Fig. 2.2.
- I_{OH}: The source current at I/O PAD of configurable I/O cell when the voltage at I/O PAD of configurable I/O cell is biased at V_{OH} (= $VDDIO_{min}$ – 0.4V = 0.9 x VDDIO – 0.4V), as shown in Fig. 2.3.

- Duty cycle: The fraction time that the system in an active state can be expressed as following equation:

$$Duty\ Cycle = \frac{\tau}{T} \quad (1)$$

where τ is the duration that the function is non-zero; T is the period of the function.

First of all, the size of output NMOS with single finger (MN0) in Fig. 2.1 has to be determined in output driver design. The simulation setup for measuring size of MN0 is shown as Fig. 2.2(a). It has been simulated by SPICE in a 90-nm CMOS process with a simulated environment of 2.25-V (0.9 x 2.5V) VDDIO and the worst case (temperature of 125 °C and SS corner) which can result in the experience results to meet the design specification certainly. Table 2.7 lists the definition of simulated environment. As shown in Fig. 2.4, the MN0 size can be determined with the low level output current I_{OL} equaled to 2.32mA. While the simulated and measured values of I_{OH}/I_{OL} are larger than the definition value (2mA, 8mA, 10mA… 24mA), it can be described as design specification conformability in driving capability. Table 2.8 depicts the simulation results of the level output current I_{OL} in different simulation environments. The dimension of the NMOS is determined with 2.25-V VDDIO and the worst case simulation environment. After determining the size of MN0, a single-finger output PMOS, MP0, is combined with this output NMOS as an inverter to design output PMOS. In this thesis, there are two methods to design the output PMOS. The first method determines the size of output PMOS MP0 by the high level output current $I_{OH} \approx I_{OL}$ where I_{OL} was the simulated driving current under the worst case and 2.25-V VDDIO for output NMOS, as shown in Fig. 2.5. Fig. 2.6 shows the simulated result of output PMOS MP0 with the channel width of 45.4µm and the simulation environment is set in the worst case and 2.25-V VDDIO. As shown in Fig. 2.7, the second method to determine the size of output PMOS MP0 is to make that duty cycle of output signal near to 50% when a square wave with duty cycle of 50% is inputted. A loading capacitance of 10pF is added at I/O PAD in the second method for

simulating actual condition and setting the same simulation environment as the first method. The duty cycle of output signal could be more (less) than 50% due to too big (small) PMOS size, as shown in Fig. 2.8. Thus, the channel width of MP0 by second method is determined on 42μm and the simulated duty cycle is 50.7% as shown in Fig. 2.9. According to these two PMOS sizes from these two methods, the corresponding I_{OH} and duty cycle are compared in Table 2.9 with the same simulation environment. Since the output PMOS size in the second method is smaller than the first method, the output PMOS size is decided on 42μm.

The simulation results of pull high driving current (I_{OH}) and duty cycle with different simulation environments are listed in Table 2.10 and Table 2.11, respectively. In Table 2.11, the input signal V_{in} is set in 0 ~ VDDIO, $T_r = T_f = 0.1$ns, pulse width = 1.875ns, period = 3.75ns, frequency = 266MHz and the additional loading capacitance (C_{load}) is 10pF. Furthermore, Table 2.12, Table 2.13, and Table 2.14 list the simulation results of duty cycle with different output MOS fingers and operating frequencies under 2.5-V, 1.8-V, and 3.3-V VDDIO voltage supplies. Similarly, the input signal V_{in} is set in 0 ~ VDDIO, $T_r = T_f = 0.1$ns, pulse width = 1.875ns, period = 3.75ns, frequency = 266MHz, and C_{load} is 10pF but the simulation environment is set with pseudo worst case for close to actual condition.

2.3.2 Short-circuit Current Reduction

The circuit consumes unnecessary power due to short-circuit current. In order to reduce the short-circuit current at the output stage, the output NMOS/PMOS should be turned on slowly and turned off quickly to avoid DC paths flowed from VDDIO to VSSIO. Thus, the gate-controlled signals of output PMOS (NMOS) should be designed with a short (long) rise time and long (short) fall time. Fig. 2.10 shows the implementation of inverter with short-circuit current reduction. MP2/MN2 and MP3/MN3 are transmission gates as resistive elements to slow down the turn-on signal of output driver. In order to verify the effect of

transmission gates, the inverters with short-circuit current reduction are placed in front of the output driver as shown in Fig. 2.11. Fig. 2.12 shows the simulation results under different VDDIO supply voltage. When the gate-controlled signals (P_out and N_out) are pulled up to VDDIO, the signal of N_out is transmitted more slowly than P_out. On the contrary, the signal of P_out is transmitted more slowly than N_out when P_out/ N_out are pulled down to VSSIO. The inverter with short-circuit current reduction can be used to produce a delay of signal.

The inverters with short-circuit current reduction shown in Fig. 2.10 are added to the inverter chains to form the tapper buffers in front of the output driver (MN1~2/MP1~2) as shown in Fig. 2.1. Besides, since single-finger output drivers (MN0/MP0) have small amount of driving currents, the tapper buffers in front of it (MN0/MP0) can be composed of general inverters (without short-circuit reduction) to save layout area. In addition, each gate terminal of MP2-MP3 and MN2-MN3 shown in Fig. 2.10 has to be connected to power line (VDDIO or VSSIO) through a resistance individually to avoid the gate-oxide breakdown under ESD stress condition. However, in order to show the circuit clearly, the resistances are all omitted in this figure.

2.4 PRE-DRIVER

The pre-driver circuit uses thin-oxide (1.0-V) devices since the input data comes from internal core circuit with VSS-to-VDD (0V-to-1.0V) voltage level. Furthermore, the pre-driver circuit generates control signals of output drivers. Table 2.15 lists the truth table of pre-driver circuit, where the control signals (S2-S0), input signal (I), and gate-controlled signals (P2-P0 and N2-N0) correspond to that in Fig. 2.1. According to the table, the relation between the gate-controlled signals (P2P0 and N2-N0) and control/input signals (S2-S0 and I)

can be defined as the equation as follows:

$$Px = \overline{Sx \cdot I} \qquad x = 0,1,2$$
$$Nx = \overline{\left(\overline{Sx} + I\right)} \qquad x = 0,1,2 \tag{2}$$

Therefore, the logic diagram of pre-driver composed of a NAND gate and NOR gate is shown in Fig. 2.13. However, since parts of transistors can be used commonly to save layout area, the circuit is implemented as shown in Fig. 2.14. Fig. 2.15 shows the simulation waveforms under different frequencies of input signals. It depicts the pre-driver can be operated correctly under different input frequency.

2.5 LEVEL SHIFTER

Since the output stage receives VSS-to-VDD (low voltage level) input signals at control/input signal pin (I, S0, S1, and S2) and transmits VSS-to-VDDIO (high voltage level) output signals at I/O PAD, the I/O cell needs a level shifter circuit to shift the voltage level from VDD to VDDIO. Fig. 2.16 shows circuit implementation of level shifter. Two inverters connected to gate terminals of transistors MN1 and MN2 separately are comprised of 1.0-V devices, other transistors are 2.5-V devices. When the input (In) receives a DC signal of VDD (1.0V), the node Inb and node In_buff are biased at VSS and VDD. Thus, the transistor MN2 (2.5V device) is turned on weakly due to the $V_{GS,\,MN2}$ = 1.0V and MN1 is turned off. However, when the node I_invb is pulled down to logic low, the node I_inv will start to be pulled up to logic high through the transistor MP1. Therefore, the transistor MP2 will be switched off, and then the output (Out) will be biased at VDDIO due to the node I_invb is biased at 0V. On the contrary, when the input (In) receives a DC signal of VSS (0V), the level shifter will transmit a logic high output signal to output (Out). Fig. 2.17 and Fig. 2.18 show the simulation

waveforms of level shifter circuit. The duty cycles are simulated under different simulation conditions as listed in Table 2.16. A small amount of load capacitance (C_{load}) is added to simulate the parasitic capacitance while the output is connected to the input of inverter chain.

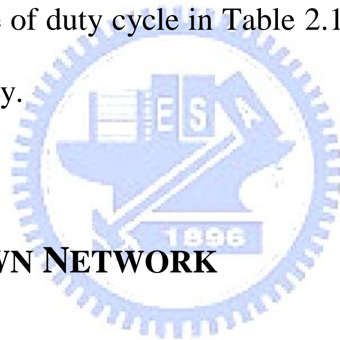
2.6 INPUT STAGE

The circuit diagram of schmit-trigger with an enable signal, SCH, is shown in Fig. 2.19, where the transistors MN4/ MP4 are 1.0-V devices, and the others are 2.5-V devices. While SCH receives logic high (1.0V) to trigger the function of schmitt-trigger, the node 1 and 2 are biased at VSS (0V) and VDD (1.0V) and then the noise margin will be enhanced. On the contrary, while SCH receives logic low to turn off the function of schmitt-trigger, the node 1 and 2 are floating points and then the circuit will become a inverter to form normal input stage.

In this configurable I/O cell, the I/O cell receives VSSIO-to-VDDIO (0V ~ 2.5V/1.8V/3.3V) input signal at I/O PAD and transmits VSS-to-VDD (0V ~ 1.0V) output signal at pin to internal circuit (C) as shown in Fig. 2.1. An inverter has been added to shcmitt-trigger circuit as shown in Fig. 2.20. The supply voltage VDD (1.0V) is used to transform the voltage level from VSSIO-to-VDDIO (high voltage level) to VSS-to-VDD (low voltage level). In order to overcome gate-oxide reliability [1] and hot-carrier degradation [2], this inverter is composed of thick-oxide devices. However, the inverter with thick-oxide devices causes a small $|Vgs|$ of the transistor MP when MP is turned on. Thus, in order to make a close 50-persentage duty cycle of output signal, MP has been designed in a big size to enhance the driving capability.

Fig. 2.21 shows the simulated voltage transform curve (VTC) of schmitt-trigger under

different simulation conditions, and Table 2.17 lists the corresponding threshold voltages (V_{T+}, V_{T-}, and V_{TH}). The waveforms of output signal, C, is simulated while the I/O PAD is swept from logic low to high and then return to its initial voltage level. The $V_{T+/-}$ is defined as the voltage level of I/O PAD while the voltage level of C is VDD/2 with the function of schmitt-trigger (SCH = 1). The V_{T+} is I/O PAD transmitted from low to high, and the V_{T-} is that from high to low. The V_{TH} is defined as the voltage level of I/O PAD while the voltage level of C is VDD/2 without the function of schmitt-trigger (SCHa = 0). Fig. 2.22-24 show the simulation waveforms of input stage when the I/O PAD is inputted a signal with 266-MHz frequency under different VDDIO supply voltage, and Table 2.18-19 list the duty cycle under different simulation conditions. Since the $|Vgs|$ of the transistor MN shown in Fig. 2.20 vary from 1.62V to 3.6V, the range of duty cycle in Table 2.18 and 3.19 are 45.72% ~ 56.65% and 44.85% ~ 61.79%, respectively.



2.7 PULL-UP/PULL-DOWN NETWORK

In this thesis, the pull-up and pull-down resistances are formed with a PMOS and NMOS operating in linear region, respectively. Besides, in order to prevent ESD stress, two 36k-Ω resistances are placed individually between the I/O PAD and the drain terminal of PMOS/NMOS as shown in Fig. 2.25. To avoid an undesired leakage current, the control signal PU (VSS-to-VDD) is shifted to high voltage level (VSSIO-toVDDIO) by level shifter mentioned in section 2.4 to turn the PMOS (MP1) off completely.

Since the equivalent resistance of the PMOS/NMOS (MP1/MN1) operating in linear region is nonlinear resistance, the rise/fall time of pull-up/pull-down network is near to that with the pull-up/pull-down resistances of design specification to determine the MP1/MN1

sizes. As shown in Fig. 2.26, to determine the size of the pull-up MOS (MP1), the gate terminals of MP1 and MN1 are biased at 0V to turn on the MP1 and turn off the MN1, respectively. Under the same additional load capacitance (C_{load}) of 12pF, MP1 and the 36k-Ω series resistance are replaced by an ideal resistance (R_{PU}) of 37kΩ. In order to make that these two simulated circuit have similar rise time, the device size of MP1 can be optimized with the typical simulation case and 2.5-V VDDIO. Therefore, the device size of MP1 can be determined and the corresponding ideal resistance can be defined as the equivalent pull-up resistance (R_{PU}) in simulated circuit, simultaneously. Similarly, the dimension of pull-down MOS (MN1) is determined as shown in Fig. 2.27. Hence, the size of MN1 can be determined and the corresponding ideal resistance is defined as the equivalent pull-down resistance (R_{PD}) in simulated circuit, simultaneously.

After determination of the MP1/MN1 size, Fig. 2.28 shows the simulation setup of the equivalent pull-up/pull-down resistances (R_{PU}/R_{PD}) in simulated circuits with different simulated conditions and load capacitance of 12pF. The R_{PU}/R_{PD} is modified to obtain the same rise/fall time of the pull-up/pull-down network. The simulation results are listed in Table 2.23 and Table 2.24. The variation of pull-up/pull-down resistance is listed in Table 2.25.

2.8 SLEW-RATE CONTROL

2.8.1 Introduction

Signal and power integrity are crucial issues in VLSI systems. Modern trends in deep sub-micron circuit designs, such as high operating frequencies, short rise/fall times, and lower supply voltage, exacerbate this problem. Output buffers provide an interface for driving mainly capacitive and inductive external loads. The capacitive load typically consists of the

bonding wire, the pin, the conductors on the PCB and the input capacitances of connected gates. The inductive load usually comprises the package parasitic series inductances of the power and ground lines supplying the output buffer, connected to the external power and ground rails on the PCB. A major component of the circuit noise is the inductive noise. Ground bounce, also known as simultaneous switching noise (SSN) or delta-I noise, is a voltage glitch induced at power/ground (P/G) distribution connections due to switching currents passing through either wire/substrate inductance or package lead inductance associated with power or ground rails. When the current flows through the inductance L, the voltage drop can be expressed as

$$V = L\frac{di}{dt} \tag{3}$$

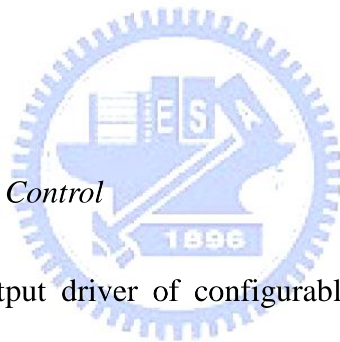
In the output buffer design, the transistors sizing is imposed by DC interfacing constraints. This leads to several problems [11]:

- Unacceptable high current peaks which occur with the simultaneous switching of many output buffers;
- Inductive power supply noise which results in large voltage drops;
- Electromagnetic interference (EMI) due to high output edge switching rates.

The results noise voltage can potentially cause spurious transitions at inputs of devices sharing the same power and ground rails. Therefore, controlling the output voltage variations is generally required to limit the crosstalk and reduce the inductive power supply noise to an acceptable value. Besides, the effect of ground bounce in output buffer can be simply modeled as an inductor shown in Fig. 2.29 [12].

2.8.2 *Concept of Slew-rate Control*

To solve these problems, a reduction of the slew rate in the output edges is preferred as far as the speed specification is satisfied [13]. A simple approach is to slow down the turn-on time of the output switching transistor through an access resistor to the transistor gate. Furthermore, the output driver can be divided into several parallel output drivers for ground bounce reduction and slew-rate control. An output buffer with slew-rate control, which is a three-step slew-rate control circuit, is shown in Fig. 2.30 [14]. The parallel output transistors of slew-rate controlled output buffer turn on progressive through delay elements implemented by resistors or transmission gates. This helps reduce the slew rate of output buffer and the ground/power bounce. However, the output transistors turn off step by step as output transistors turn on.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2.8.3 *Design of Slew-rate Control*

Fig. 2.31 shows the output driver of configurable I/O cell with slew-rate control to reduce ground/power bounce. The delay elements are implemented by transmission gate (MDN/MDP). The original MN1/MP1 (multiple=4) shown in Fig. 2.1 are divided into MN10/MP10 (m=2) and MN11/MP11 (m=2). The original MN2/MP2 (m=7) are divided into MN20/MP20 (m=2), MN21/MP21 (m=2), and MN22/MP22 (m=3). In order to reduce short-circuit current simultaneously, the gate-controlled signals of output NMOS have to be designed with longer rise times and shorter fall times. Thus, larger NMOS width and smaller PMOS width of transmission gates DN1 and DN2 are needed. On the contrary, larger PMOS width and smaller NMOS width of transmission gates DP1 and DP2 are needed.

The gate-controlled signals of output driver with slew-rate control are simulated as shown in Fig. 2.32, and the corresponding switching current on power and ground lines are

shown in Fig. 2.33. As a result, the ground bounce effects of output driver with slew-rate control were improved obviously. Fig. 2.34 shows the output waveforms of the configurable I/O cell with different VDDIO supply voltages. The rise times and fall times of output driver with slew-rate control are longer than those of output driver without slew-rate control. Table 2.23 and Table 2.24 list the simulation results of maximum switching current reduction on VDDIO and VSSIO power lines, respectively.

Tabel 2.1

Pin description.

Input Control Pins	Description
SCH	Schmitt-trigger enable
PU	Pull up enable
PD	Pull down enable
S0, S1, S2	Driving select
I	Data input
PAD	Bidirectional pin
C	Pin to internal circuit

Tabel 2.2

Configurable I/O cell with different output driving.

Operating Mode	Control Pins				Output Driving	Input Function
	S2	S1	S0	SCH		
Receive (PAD → C)	0	0	0	1		Schmitt-trigger input
	0	0	0	0		Normal input
Transmit (I → PAD)	0	0	1	x	2mA	
	0	1	0	x	8mA	
	0	1	1	x	10mA	
	1	0	0	x	14mA	
	1	0	1	x	16mA	
	1	1	0	x	22mA	
	1	1	1	x	24mA	

Tabel 2.3

State of I/O PAD in configurable I/O cell with different input signal.

<table>
<tr><th colspan="7">Input</th><th>Output</th></tr>
<tr><th>S2</th><th>S1</th><th>S0</th><th>I</th><th>PU</th><th>PD</th><th>PAD</th><th>PAD</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>0</td><td>0</td><td rowspan="5">No input</td><td>High-Z</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>1</td><td>0</td><td>Pull-up</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>x</td><td>0</td><td>1</td><td>Pull-down</td></tr>
<tr><td colspan="3" rowspan="2">Else</td><td>1</td><td>x</td><td>x</td><td>1</td></tr>
<tr><td>0</td><td>x</td><td>x</td><td>0</td></tr>
</table>

Tabel 2.4

DC specification of configurable I/O cell in 2.5-V VDDIO supply voltage.

Symbol	Parameter	Condition	Min.	Nom.	Max.
VDD	Core power supply		0.9V	1.0V	1.1V
VDDIO	I/O output driver power supply	2.5-V I/O	2.25V	2.5V	2.75V
T_J	Junction temperature		0°C	25°C	125°C
V_{IL}	Input low voltage				0.7V
V_{IH}	Input high voltage		1.8 V		
V_{T+}	Schmitt-trigger low to high threshold point		1.51V	1.63V	1.76V
V_{T-}	Schmitt-trigger high to low threshold point		0.76V	0.83V	0.92V
I_{IN}	Input leakage current	V_I = VDDIO or 0V			±10μA
I_{HIZ}	Output Tri-state leakage current				±10μA
R_{PU}	Pull-up resistor		27kΩ	37kΩ	49kΩ
R_{PD}	Pull-down resistor		24kΩ	37kΩ	60kΩ
V_{OL}	Output low voltage	I_{OL} = 2-24mA			0.4V
V_{OH}	Output high voltage	I_{OH} = 2-24mA	1.85V		
I_{OL}	Low level output current @ $V_{OL} = 0.4V$	2mA	2.34mA	4.06mA	5.31mA
		8mA	9.41mA	16.3mA	21.2mA
		10mA	11.7mA	20.3mA	26.5mA
		14mA	16.5mA	28.5mA	37.2mA
		16mA	18.8mA	32.5mA	42.5mA
		22mA	25.9mA	44.7mA	58.4mA
		24mA	28.2mA	48.8mA	63.7mA
I_{OH}	Low level output current @ $V_{OH} = 1.85V$	2mA	2.20mA	4.93mA	8.23mA
		8mA	8.94mA	19.8mA	33.0mA
		10mA	11.0mA	24.7mA	41.2mA
		14mA	15.5mA	34.7mA	57.8mA
		16mA	17.7mA	39.6mA	66.0mA
		22mA	24.3mA	54.4mA	90.8mA
		24mA	26.5mA	59.4mA	99.0mA

Tabel 2.5

DC specification of configurable I/O cell in 1.8-V VDDIO supply voltage.

Symbol	Parameter	Condition	Min.	Nom.	Max.
VDD	Core power supply		0.9V	1.0V	1.1V
VDDIO	I/O output driver power supply	1.8-V I/O	1.62V	1.8V	1.98V
T_J	Junction temperature		0°C	25°C	125°C
V_{IL}	Input low voltage				0.5V
V_{IH}	Input high voltage		1.5V		
V_{T+}	Schmitt-trigger low to high threshold point		1.21V	1.34V	1.46V
V_{T-}	Schmitt-trigger high to low threshold point		0.56V	0.59V	0.65V
I_{IN}	Input leakage current	V_I = VDDIO or 0V			±10μA
I_{HIZ}	Output Tri-state leakage current				±10μA
R_{PU}	Pull-up resistor		32kΩ	47kΩ	69kΩ
R_{PD}	Pull-down resistor		20kΩ	29kΩ	46kΩ
V_{OL}	Output low voltage	I_{OL} = 2-24mA			0.4V
V_{OH}	Output high voltage	I_{OH} = 2-24mA	1.22V		
I_{OL}	Low level output current @ $V_{OL} = 0.4V$	2mA	1.58mA	2.93mA	4.12mA
		8mA	6.34mA	11.7mA	16.4mA
		10mA	7.92mA	14.7mA	20.6mA
		14mA	11.1mA	20.6mA	28.9mA
		16mA	12.7mA	23.5mA	33.0mA
		22mA	17.5mA	32.3mA	45.4mA
		24mA	19.0mA	35.2mA	49.5mA
I_{OH}	Low level output current @ $V_{OH} = 1.22V$	2mA	1.46mA	3.06mA	5.08mA
		8mA	5.89mA	12.3mA	20.4mA
		10mA	7.35mA	15.4mA	25.4mA
		14mA	10.3mA	21.6mA	35.6mA
		16mA	11.8mA	24.6mA	40.7mA
		22mA	16.2mA	33.9mA	56.0mA
		24mA	17.7mA	37.0mA	61.1mA

Tabel 2.6

DC specification of configurable I/O cell in 3.3-V VDDIO supply voltage.

Symbol	Parameter	Condition	Min.	Nom.	Max.
VDD	Core power supply		0.9V	1.0V	1.1V
VDDIO	I/O output driver power supply	3.3-V I/O	3.0V	3.3V	3.6V
T_J	Junction temperature		0^oC	25^oC	125^oC
V_{IL}	Input low voltage				0.9V
V_{IH}	Input high voltage		2.2V		
V_{T+}	Schmitt-trigger low to high threshold point		1.78V	1.93V	2.07V
V_{T-}	Schmitt-trigger high to low threshold point		1.05V	1.13V	1.23V
I_{IN}	Input leakage current	V_I = VDDIO or 0V			±10μA
I_{HIZ}	Output Tri-state leakage current				±10μA
R_{PU}	Pull-up resistor		25kΩ	32kΩ	40kΩ
R_{PD}	Pull-down resistor		28kΩ	45kΩ	75kΩ
V_{OL}	Output low voltage	I_{OL} = 2-24mA			0.4V
V_{OH}	Output high voltage	I_{OH} = 2-24mA	2.6V		
I_{OL}	Low level output current @ $V_{OL} = 0.4V$	2mA	2.91mA	4.06mA	5.31mA
		8mA	11.7mA	16.3mA	21.2mA
		10mA	14.6mA	20.3mA	26.5mA
		14mA	20.4mA	28.5mA	37.2mA
		16mA	23.3mA	32.5mA	42.5mA
		22mA	21.0mA	44.7mA	58.4mA
		24mA	35.0mA	48.8mA	63.7mA
I_{OH}	Low level output current @ $V_{OH} = 2.6V$	2mA	2.81mA	6.55mA	11.0mA
		8mA	11.2mA	26.3mA	44.0mA
		10mA	14.1mA	32.8mA	55.0mA
		14mA	19.8mA	46.0mA	77.0mA
		16mA	22.6mA	52.6mA	88.0mA
		22mA	31.0mA	72.3mA	121mA
		24mA	33.8mA	78.9mA	132mA

Tabel 2.7

Simulation Environment

Simulation Case	Corner	Temperature (°C)	VDD (V)
Best	FF	0	1.1
Typical	TT	25	1.0
Pseudo Worst	TT	85	1.0
Worst	SS	125	0.9

Tabel 2.8

Simulation results of pull low driving current (I_{OL}) of output NMOS

in different simulation conditions.

Simulation Case	VDDIO		I_{OL}	I_{OL} (NMOS finger = 12)
Best	3.6V	(= typical VDDIO x 1.1)	5.5864mA	67.0370mA
	2.75V		5.1711mA	62.0533mA
	1.98V		4.0480mA	48.5758mA
Typical	3.3V		4.5462mA	54.5539mA
	2.5V		3.9819mA	47.7830mA
	1.8V		2.8925mA	34.7096mA
Worst	3V	(= typical VDDIO x 0.9)	2.8530mA	34.2365mA
	2.25V		2.3220mA	27.8638mA
	1.62V		1.5672mA	18.8059mA

Tabel 2.9

I_{OH} and duty cycle comparison between two methods of MP0 design.

Method	Device	Width	I_{OH} at V_{OH} = 1.85V	Duty Cycle
1	PMOS	45.4μm	2.3241mA	51.73%
1	PMOS m=12	544.8μm	27.8890mA	50.27%
2	PMOS	42μm	2.1472mA	50.7%
2	PMOS m=12	504μm	25.7661mA	50.15%

Tabel 2.10

Simulation results of high level output current (I_{OH}) of output PMOS designed with the second method in different simulation environments.

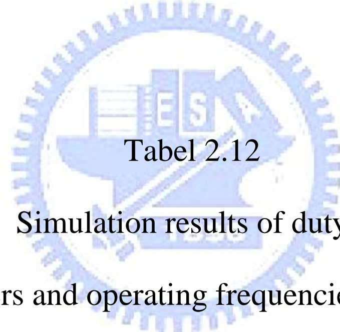
Simulation Case	VDDIO		V_{OH}	I_{OH} (mA)	I_{OH} (mA) (PMOS finger = 12)
Best	3.6V	(= typical VDDIO x 1.1)	2.6V	10.8172	129.8059
	2.75V		1.85V	8.1205	97.4457
	1.98V		1.22V	5.0575	60.6901
Typical	3.3V		2.6V	6.4671	77.6052
	2.5V		1.85V	4.8521	58.2257
	1.8V		1.22V	3.0462	36.5542
Worst	3V	(= typical VDDIO x 0.9)	2.6V	2.7828	33.3941
	2.25V		1.85V	2.1472	25.7661
	1.62V		1.22V	1.4484	17.3810

Tabel 2.11

Duty cycle in different simulation environment.

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	50.41%	50.50%	50.76%	51.17%
3.3	50.37%	50.42%	50.68%	51.07%
3.0	50.31%	50.34%	50.61%	50.95%
2.75	50.28%	50.28%	50.52%	50.89%
2.5	50.22%	50.20%	50.44%	50.86%
2.25	50.13%	50.16%	50.42%	50.79%
1.98	50.13%	50.14%	50.38%	50.78%
1.8	50.11%	50.09%	50.41%	50.80%
1.62	50.13%	50.11%	50.46%	50.88%

The range of duty cycle is 50.13% ~ ~51.17%.



Tabel 2.12

Simulation results of duty cycle

in different output MOS fingers and operating frequencies with 2.5-V VDDIO voltage supply.

Finger Number	1	4	5	7	8	11	12
Driving Current / Frequency	2mA	8mA	10mA	14mA	16mA	22mA	24mA
50 MHz	50.42%	50.15%	50.13%	50.11%	50.11%	50.09%	50.08%
66 MHz	50.47%	50.20%	50.18%	50.14%	50.14%	50.11%	50.11%
133 MHz	*	50.41%	50.36%	50.30%	50.28%	50.23%	50.22%
266 MHz	*	*	50.63%	50.58%	50.56%	50.45%	50.44%

(1) * Do not meet the design specification. (2) The range of duty cycle is 50.08% ~ ~50.63%.

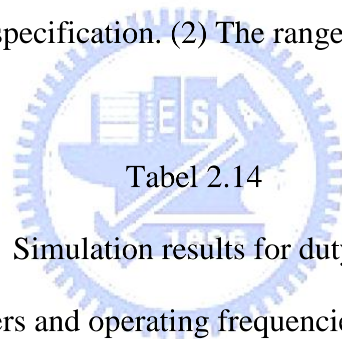
Tabel 2.13

Simulation results of duty cycle

in different output MOS fingers and operating frequencies with 1.8-V VDDIO voltage supply.

Finger Number	1	4	5	7	8	11	12
Driving Current / Frequency	2mA	8mA	10mA	14mA	16mA	22mA	24mA
50 MHz	50.23%	50.14%	50.13%	50.11%	50.11%	50.11%	50.10%
66 MHz	*	50.19%	50.17%	50.15%	50.14%	50.13%	50.13%
133 MHz	*	50.36%	50.34%	50.30%	50.29%	50.26%	50.26%
266 MHz	*	*	*	50.49%	50.52%	50.50%	50.51%

(1) * Do not meet the design specification. (2) The range of duty cycle is 50.1% ~ ~50.51%.



Tabel 2.14

Simulation results for duty cycle

in different output MOS fingers and operating frequencies with 3.3-V VDDIO voltage supply.

Finger Number	1	4	5	7	8	11	12
Driving Current / Frequency	2mA	8mA	10mA	14mA	16mA	22mA	24mA
50 MHz	50.96%	50.29%	50.25%	50.19%	50.18%	50.15%	50.14%
66 MHz	51.27%	50.39%	50.33%	50.26%	50.24%	50.20%	50.18%
133 MHz	*	50.78%	50.66%	50.52%	50.47%	50.39%	50.36%
266 MHz	*	51.51%	51.30%	51.03%	50.95%	50.78%	50.73%

(1) * Do not meet the design specification. (2) The range of duty cycle is 50.14% ~ 51.51%.

Tabel 2.15

Truth table of pre-driver.

Gate-controlled Signal			I	PMOS Gate-controlled Signal			NMOS Gate-controlled Signal		
S2	S1	S0		P2	P1	P0	N2	N1	N0
0	0	0	X	1	1	1	0	0	0
0	0	1	1	1	1	0	0	0	0
0	0	1	0	1	1	1	0	0	1
0	1	0	1	1	0	1	0	0	0
0	1	0	0	1	1	1	0	1	0
0	1	1	1	1	0	0	0	0	0
0	1	1	0	1	1	1	0	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	0	1	1	1	1	0	0
1	0	1	1	0	1	0	0	0	0
1	0	1	0	1	1	1	1	0	1
1	1	0	1	0	0	1	0	0	0
1	1	0	0	1	1	1	1	1	0
1	1	1	1	0	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1

Tabel 2.16

Duty cycle simulations under different VDDIO voltage supply

with input signal V_{in} = 0 ~ VDDIO, $T_r = T_f$ = 0.1ns, pulse width=1.875ns, period = 3.75ns,

frequency = 266MHz, and C_{load} = 20fF

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	51.2%	51.6%	51.6%	52.3%
3.3	51.2%	51.5%	51.6%	52.1%
3.0	51.3%	51.6%	51.7%	52.0%
2.75	51.5%	51.7%	51.9%	52.2%
2.5	51.6%	52.0%	52.1%	52.5%
2.25	51.9%	52.3%	52.5%	53.1%
1.98	52.2%	52.8%	53.0%	53.9%
1.8	52.5%	53.3%	53.5%	54.6%
1.62	52.9%	53.9%	54.2%	54.6%

*The range of duty cycle is 51.2% ~ 54.6%.

Tabel 2.17

Threshold voltages of schmitt-trigger under different simulation conditions.

Input Signal of SCHa	SCH = 1						SCH = 0		
VDDIO Supply Voltage	3.3V	2.5V	1.8V	3.3V	2.5V	1.8V	3.3V	2.5V	1.8V
Threshold Voltages / Simulation condition	V_{T+} (V)			V_{T-} (V)			V_{TH} (V)		
Best Case	2.065	1.755	1.455	1.225	0.915	0.645	1.91	1.366	0.955
Typical Case	1.925	1.625	1.335	1.125	0.825	0.585	1.723	1.235	0.876
Pseudo Worst Case	1.905	1.625	1.335	1.135	0.835	0.605	1.735	1.245	0.885
Worst Cast	1.775	1.505	1.205	1.045	0.755	0.555	1.568	1.128	0.815

Tabel 2.18

Duty Cycle of schmitt-trigger input stage

under different simulation conditions with input signal $V_{PAD} = 0 \sim VDDIO$, $T_r = T_f = 0.1ns$,

pulse width=1.875ns, period = 3.75ns, frequency = 266MHz, and $C_{load} = 0.1pF$

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	48.04%	46.91%	47.21%	45.72%
3.3	48.44%	47.42%	47.72%	46.42%
3.0	48.84%	47.97%	48.37%	47.11%
2.75	49.29%	48.46%	48.95%	47.87%
2.5	49.83%	48.92%	49.55%	48.92%
2.25	50.45%	49.89%	50.60%	50.21%
1.98	51.44%	51.14%	52.03%	52.10%
1.8	52.30%	52.32%	53.28%	53.79%
1.62	53.57%	54.16%	55.13%	56.65%

Tabel 2.19

Duty Cycle of normal input stage

under different simulation conditions with input signal $V_{PAD} = 0 \sim VDDIO$, $T_r = T_f = 0.1ns$,

pulse width=1.875ns, period = 3.75ns, frequency = 266MHz, and $C_{load} = 0.1pF$

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	47.53%	46.27%	46.54%	44.85%
3.3	47.96%	46.81%	47.13%	45.67%
3.0	48.57%	47.48%	47.91%	46.69%
2.75	49.15%	48.23%	48.75%	47.80%
2.5	49.88%	49.20%	49.81%	49.21%
2.25	50.87%	50.50%	51.20%	51.14%
1.98	52.35%	52.45%	53.34%	54.22%
1.8	53.72%	54.32%	55.33%	57.26%
1.62	55.53%	56.92%	58.14%	61.79%

Tabel 2.20

Equivalent pull-up resistance (R_{PU}) in simulated circuit under different simulation conditions.

Simulation Case	VDDIO (V)								
	3.6	3.3	3.0	2.75	2.5	2.25	1.98	1.8	1.62
Best	25kΩ	25kΩ	26kΩ	27kΩ	28kΩ	30kΩ	32kΩ	35kΩ	38kΩ
Typical	28kΩ	29kΩ	30kΩ	32kΩ	33kΩ	36kΩ	39kΩ	43kΩ	47kΩ
Pseudo Worst	30kΩ	32kΩ	33kΩ	35kΩ	37kΩ	40kΩ	44kΩ	47kΩ	53kΩ
Worst	36kΩ	38kΩ	40kΩ	42kΩ	45kΩ	49kΩ	56kΩ	61kΩ	69kΩ

Tabel 2.21

Equivalent pull-down resistance (R_{PD}) in simulated circuit under different simulation conditions.

Simulation Case	VDDIO (V)								
	3.6	3.3	3.0	2.75	2.5	2.25	1.98	1.8	1.62
Best	32kΩ	30kΩ	28kΩ	27kΩ	25kΩ	24kΩ	22kΩ	21kΩ	20kΩ
Typical	47kΩ	44kΩ	41kΩ	38kΩ	35kΩ	33kΩ	30kΩ	28kΩ	27kΩ
Pseudo Worst	49kΩ	45kΩ	42kΩ	39kΩ	37kΩ	34kΩ	31kΩ	29kΩ	28kΩ
Worst	75kΩ	69kΩ	64kΩ	60kΩ	55kΩ	50kΩ	46kΩ	43kΩ	40kΩ

Tabel 2.22

Variation of pull-up/pull-down resistance

VDDIO (V) (0.9xVDDIO~1.1xVDDIO)	R_{PU}			R_{PD}		
	Min.	Typ.	Max.	Min.	Typ.	Max.
3.3 (3 ~ 3.6)	25kΩ	32kΩ	40kΩ	28kΩ	45kΩ	75kΩ
2.5 (2.25 ~ 2.75)	27kΩ	37kΩ	49kΩ	24kΩ	37kΩ	60kΩ
1.8 (1.62 ~ 1.98)	32kΩ	47kΩ	69kΩ	20kΩ	29kΩ	46kΩ

Tabel 2.23

Reduction of the maximum switching current on VDDIO power line

under different simulation conditions.

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	14.5%	17.1%	17.2%	18.8%
3.3	16.7%	18.4%	18.7%	20.0%
3.0	17.8%	19.5%	20.5%	22.0%
2.75	20.5%	21.9%	21.8%	23.5%
2.5	22.0%	23.8%	23.3%	24.8%
2.25	25.1%	25.6%	25.4%	26.8%
1.98	26.6%	29.3%	27.4%	29.4%
1.8	29.6%	32.2%	29.4%	31.2%
1.62	30.7%	33.4%	31.2%	33.3%

Tabel 2.24

Reduction of the maximum switching current on VSSIO ground line

under different simulation conditions.

VDDIO (V)	Simulation Case			
	Best	Typical	Pseudo Worst	Worst
3.6	11.2%	12.4%	13.8%	16.2%
3.3	12.5%	14.2%	14.6%	17.7%
3.0	15.0%	16.3%	16.0%	19.2%
2.75	16.7%	17.8%	17.9%	21.0%
2.5	18.5%	20.5%	20.1%	22.8%
2.25	20.6%	23.1%	22.6%	25.8%
1.98	24.1%	27.7%	25.7%	29.3%
1.8	26.7%	31.1%	28.7%	33.0%
1.62	30.1%	35.5%	32.6%	37.7%

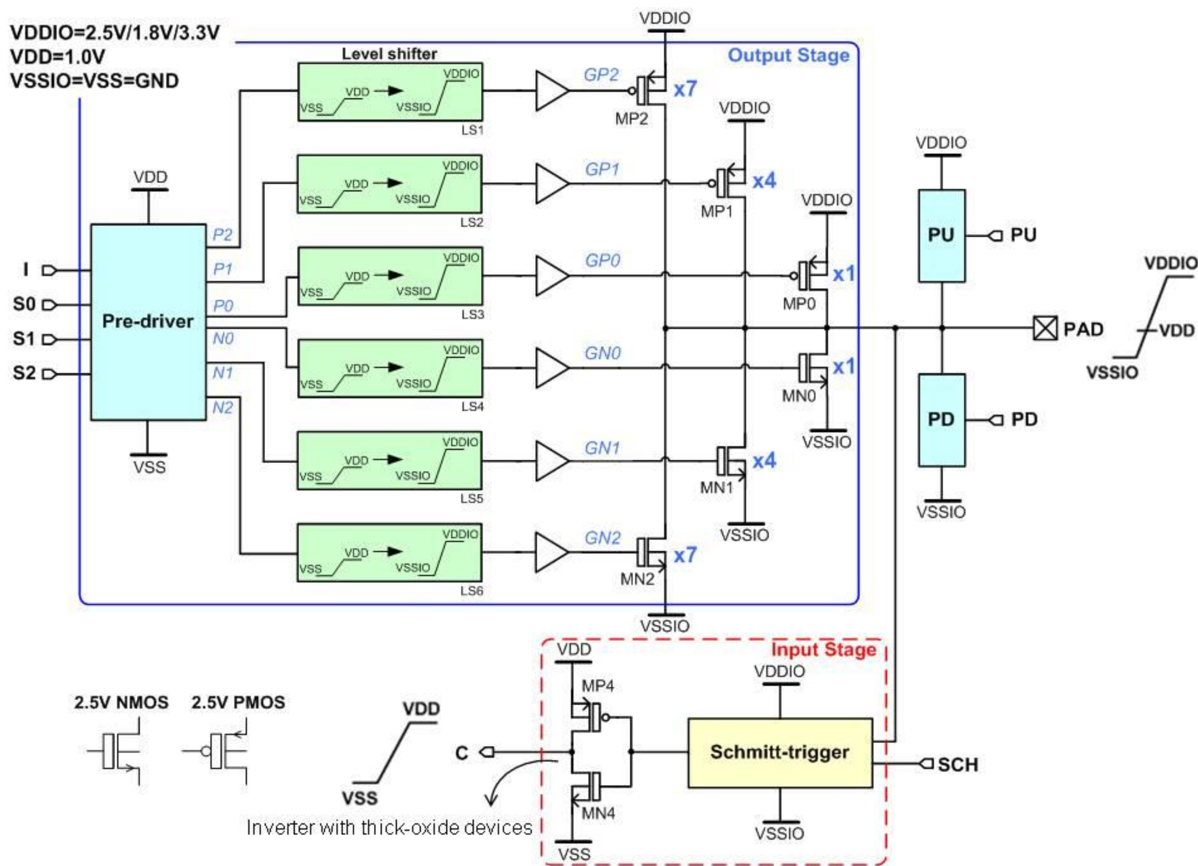


Fig. 2.1 Block diagram of 90-nm 1.0-V/2.5-V configurable I/O cell.

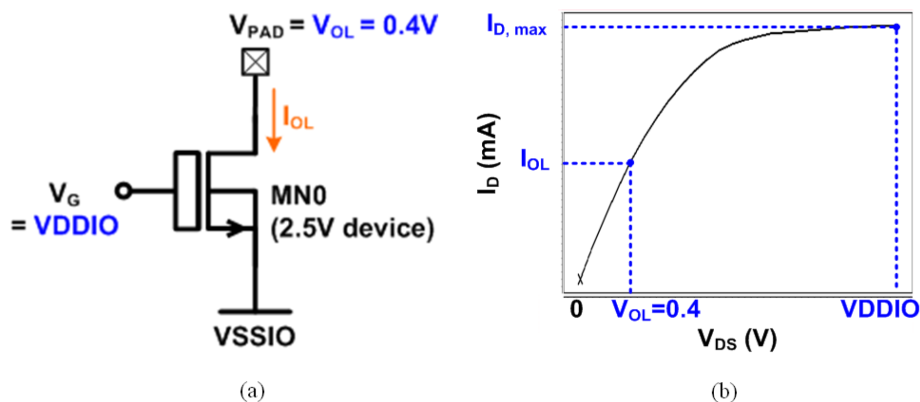


Fig. 2.2 Illustration of pull low driving current (I_{OL}) with (a) terminal condition and (b) I-V curve of output NMOS.

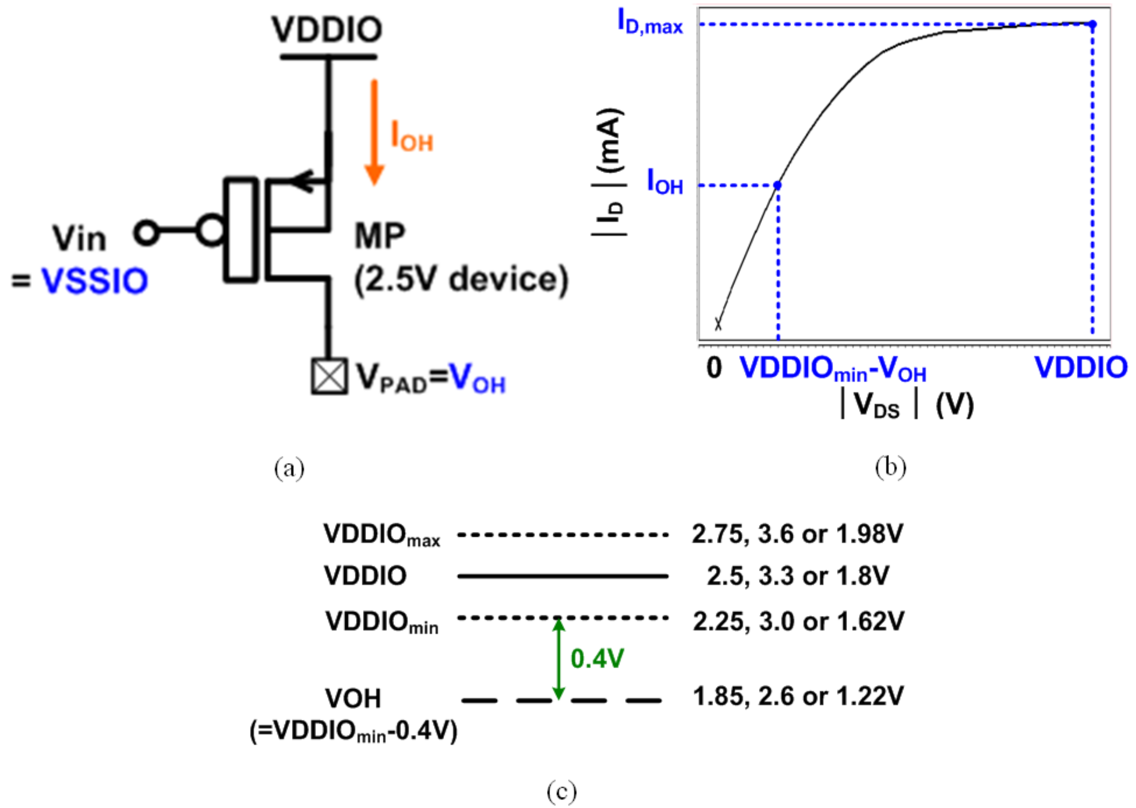


Fig. 2.3 Illustration of Pull high driving current (I_{OH}) with (a) terminal condition, (b) I-V curve of output PMOS and (c) corresponding V_{OH} in different VDDIO voltage supply.

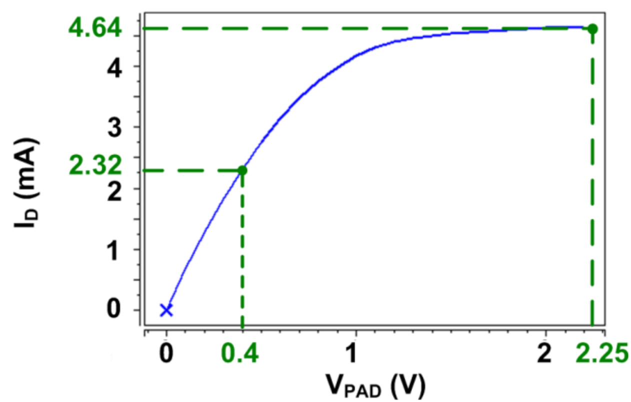


Fig. 2.4 Simulated result of single-finger output NMOS.

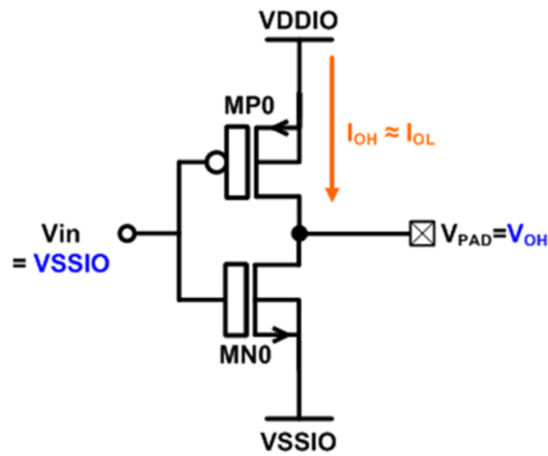


Fig. 2.5 The first method for designing single-finger output PMOS MP0.

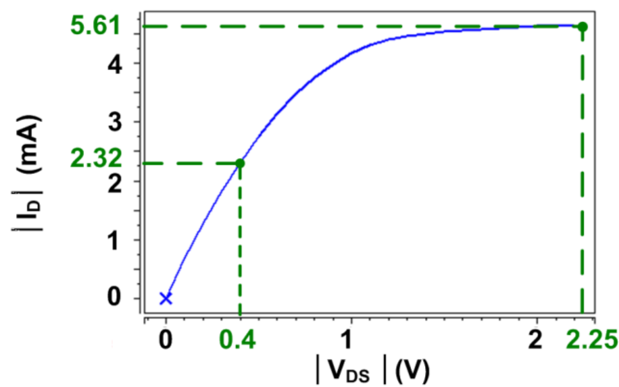


Fig. 2.6 Simulated results for single-finger output PMOS MP0 with the channel width of 45.4μm.

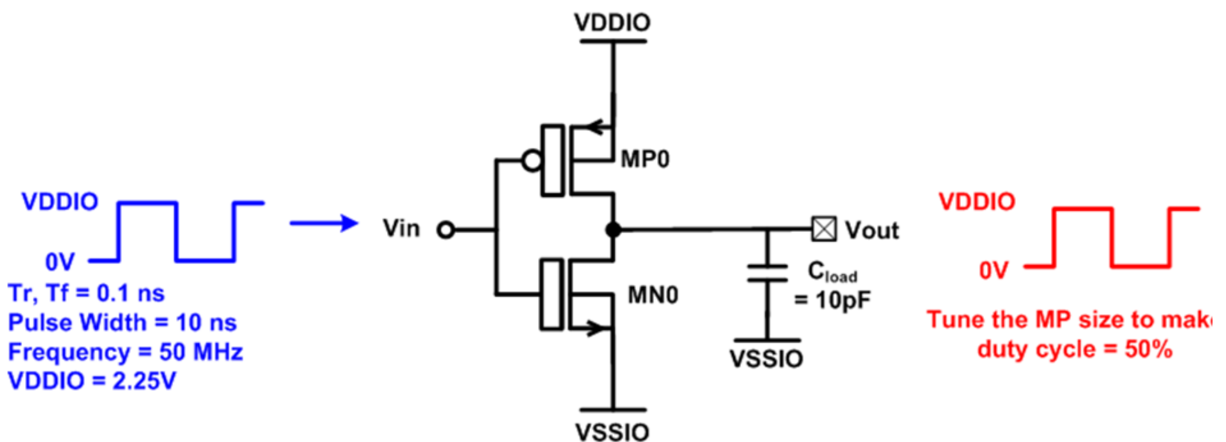


Fig. 2.7 The second method for designing single-finger output PMOS.

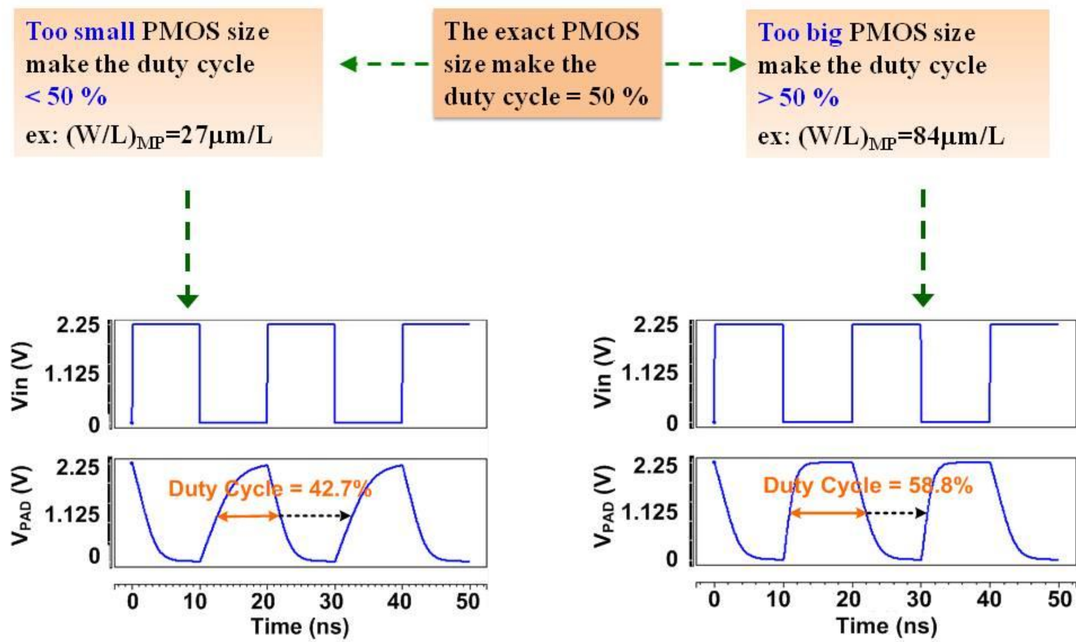


Fig. 2.8 Relation between PMOS Size and Duty Cycle.

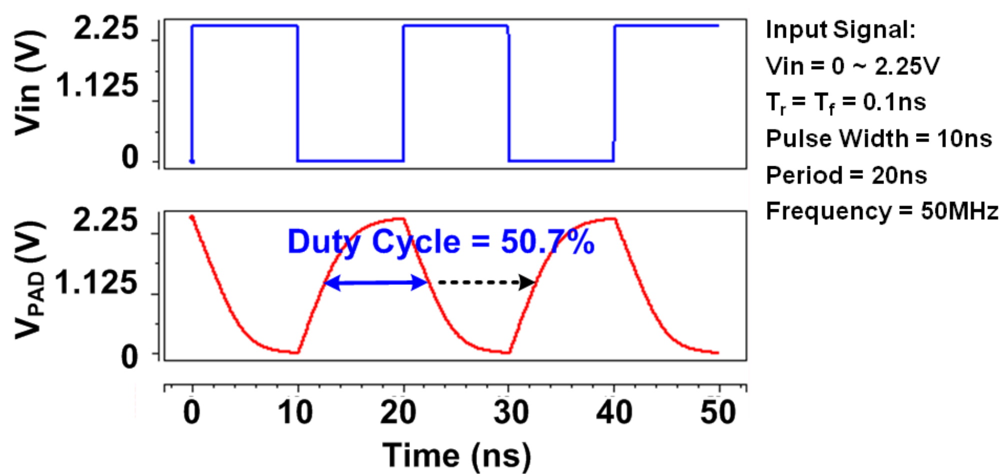


Fig. 2.9 Simulated waveform for determining size of single-finger output PMOS MP0.

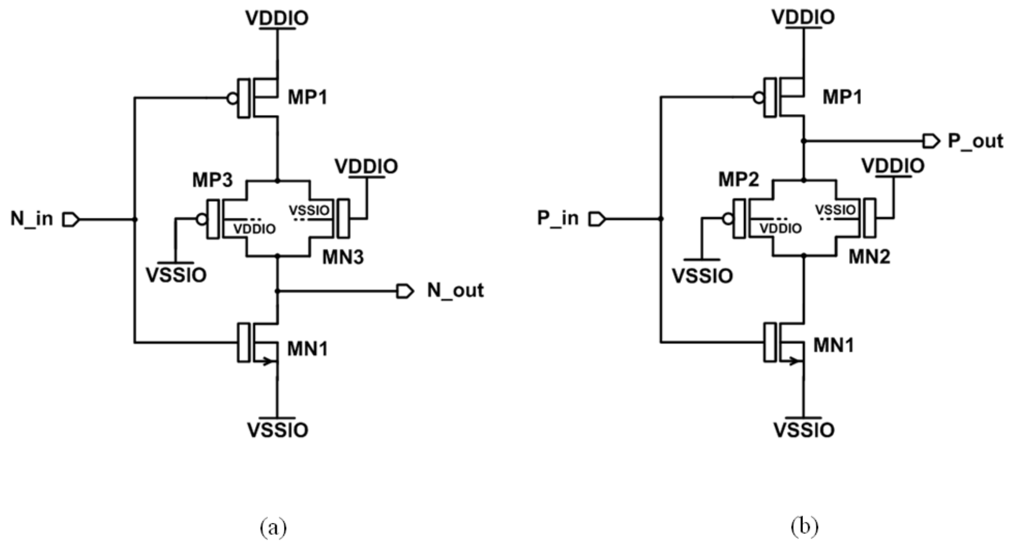


Fig. 2.10 The inverter with short-circuit reduction for (a) output NMOS and (b) output PMOS.

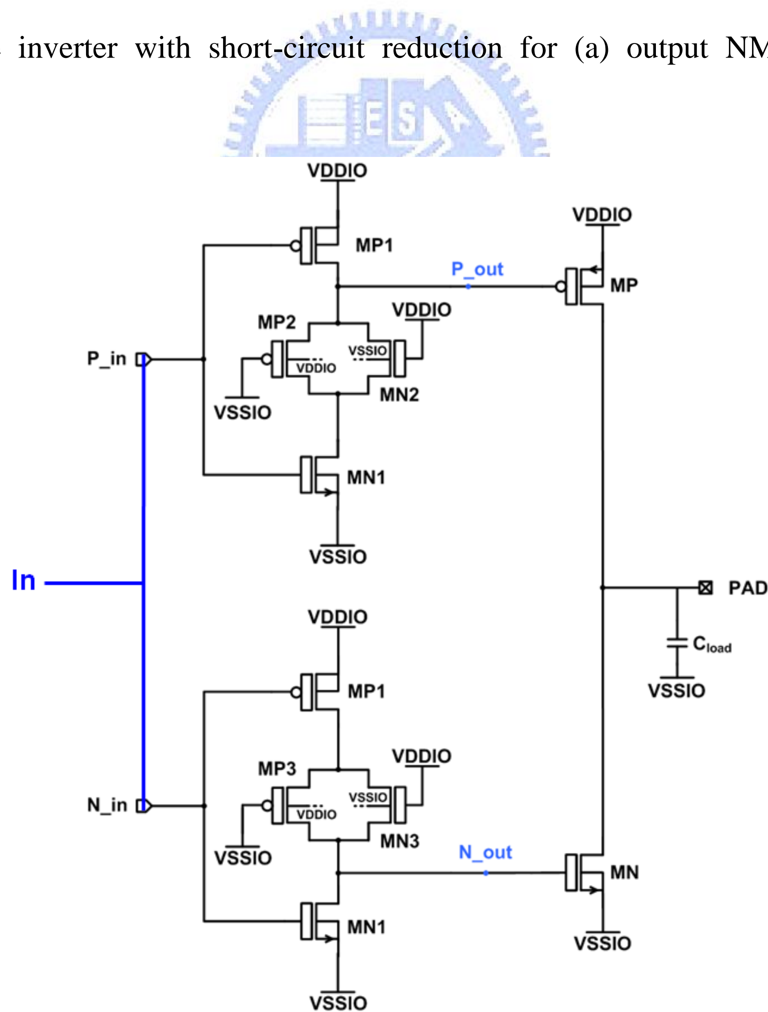


Fig. 2.11 Simulation setup of short-circuit current reduction.

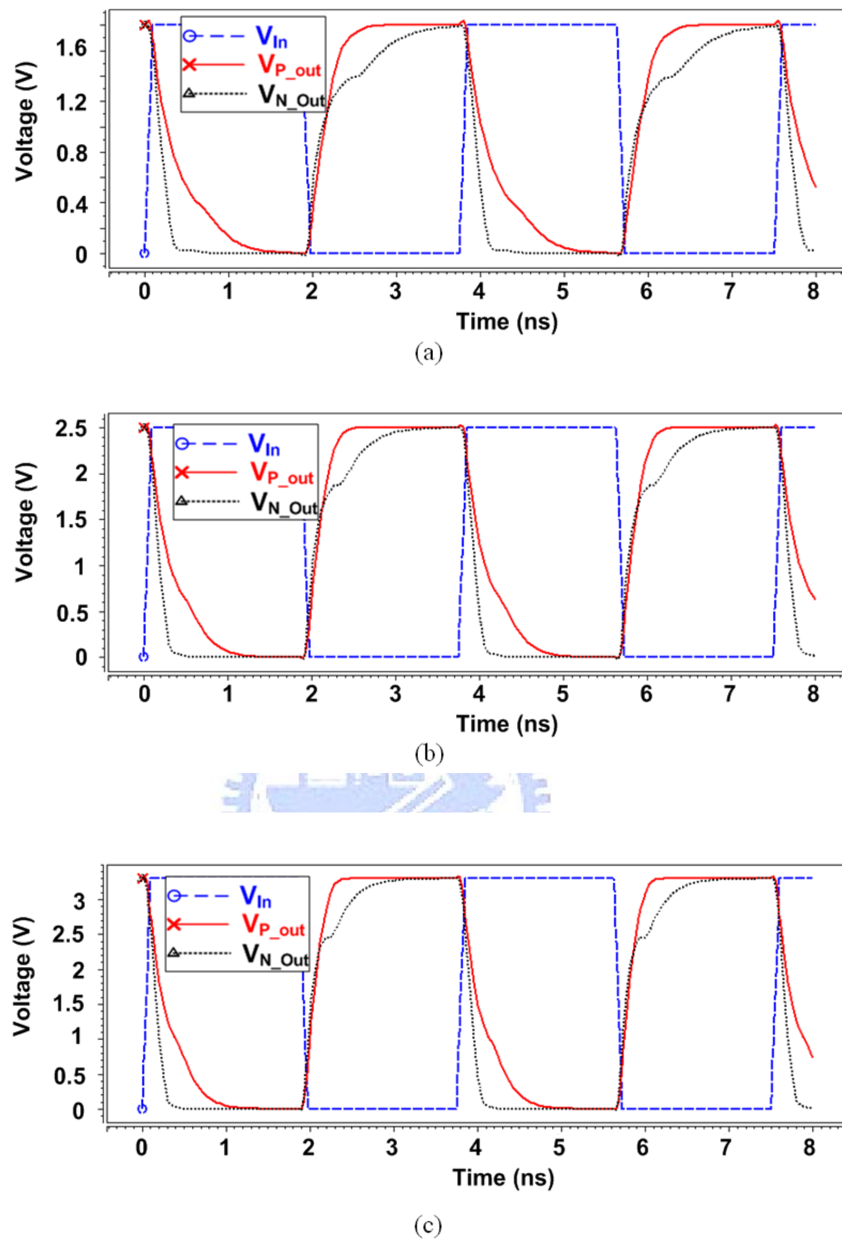


Fig. 2.12 Simulation results of short-circuit current reduction with the pseudo worst simulation case (85°C, TT corner), V_{in} = 0 ~ VDDIO, T_r = T_f = 0.1ns, Frequency = 266MHz, and C_{load} = 12pF, (a) 1.8-V VDDIO, (b) 2.5-V VDDIO, and (c) 3.3-V VDDIO.

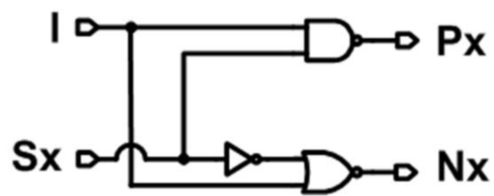


Fig. 2.13 Logic diagram of pre-driver.

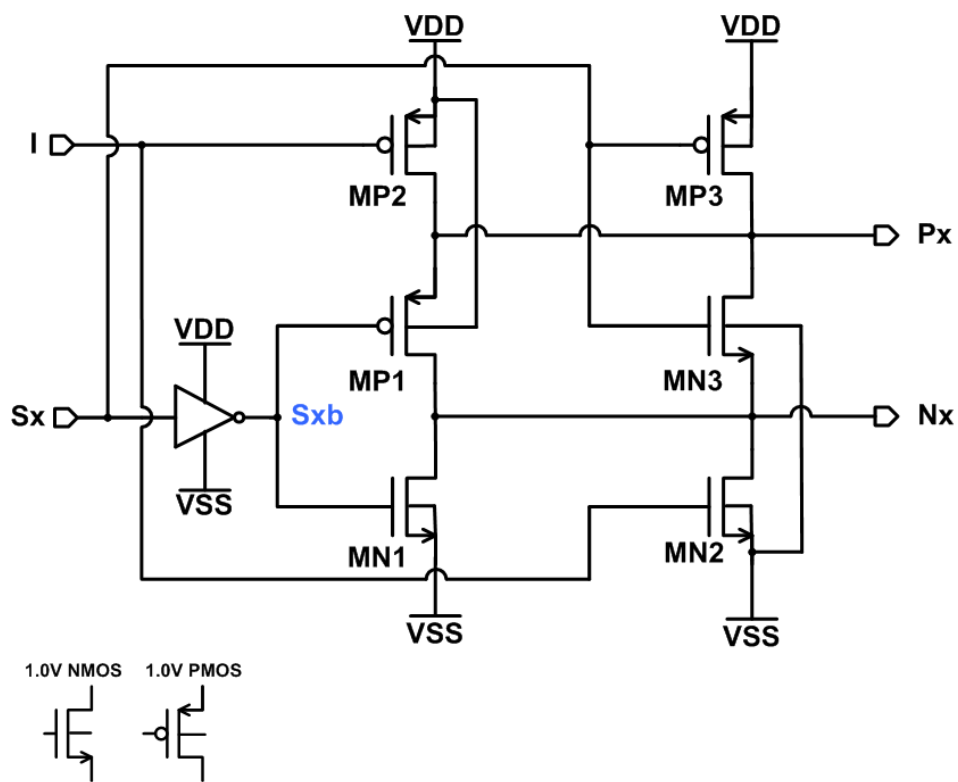
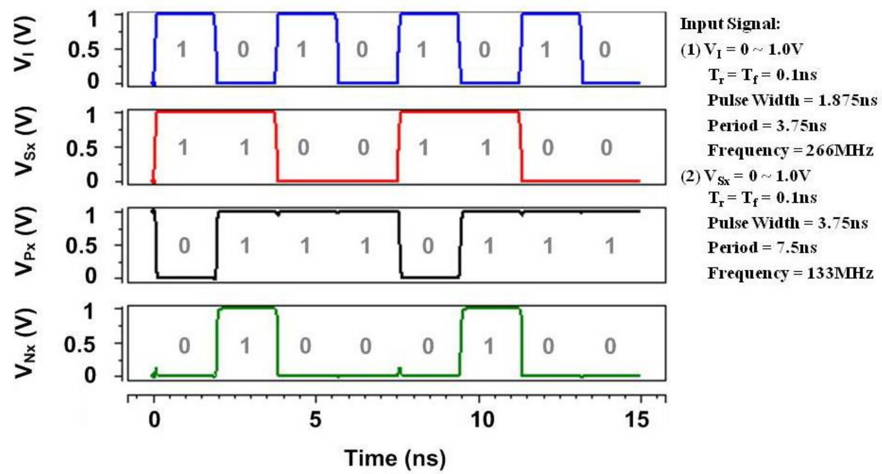
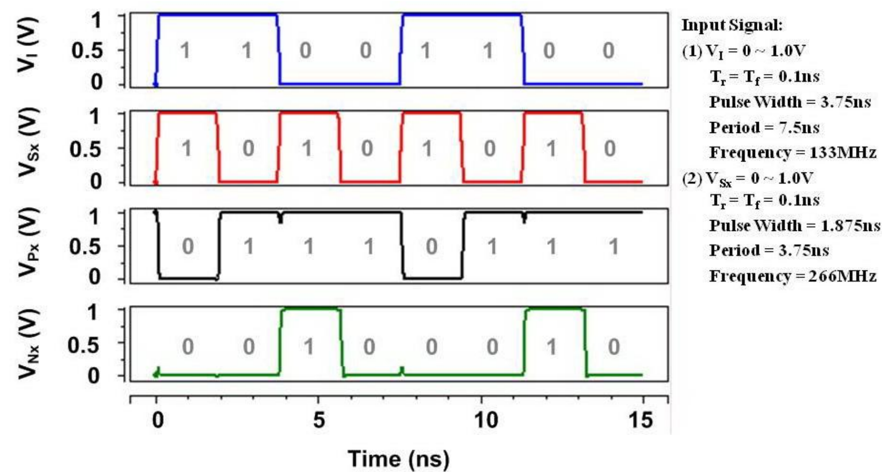


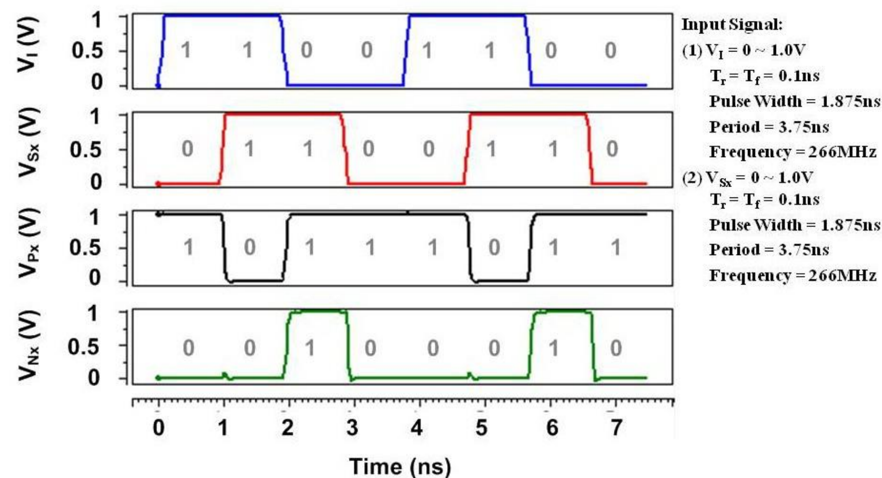
Fig. 2.14 Circuit implementation of pre-driver.



(a)



(b)



(c)

Fig. 2.15 Simulation waveforms of pre-driver with the pseudo worst case (85°C, TT corner), C_{load} = 0.9fF, (a) 266-MHz input signal V_I, 133-MHz input signal V_{Sx}, (b) 133-MHz input signal V_I, 266-MHz input signal V_{Sx}, and (c) 266-MHz input signals V_I and V_{Sx}.

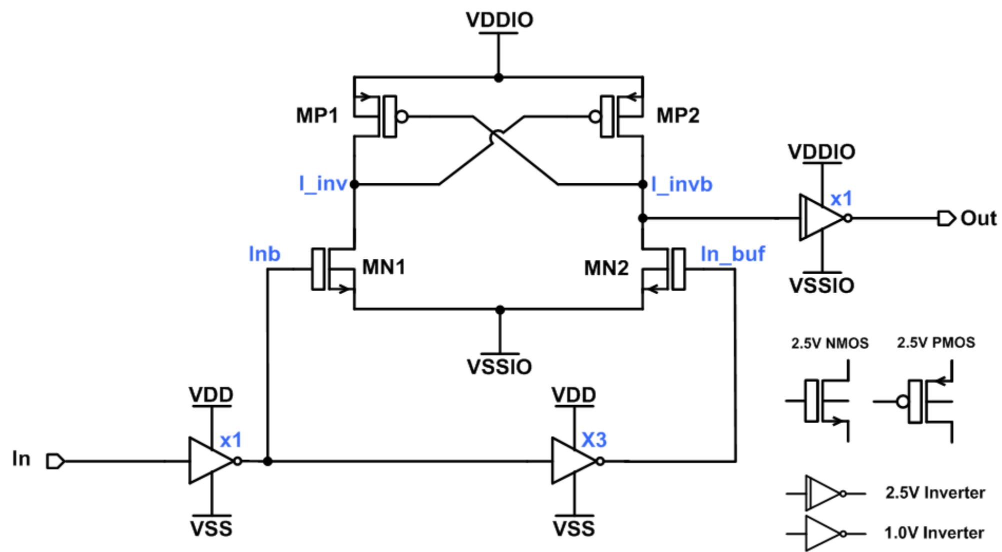


Fig. 2.16 Circuit diagram of level shifter.

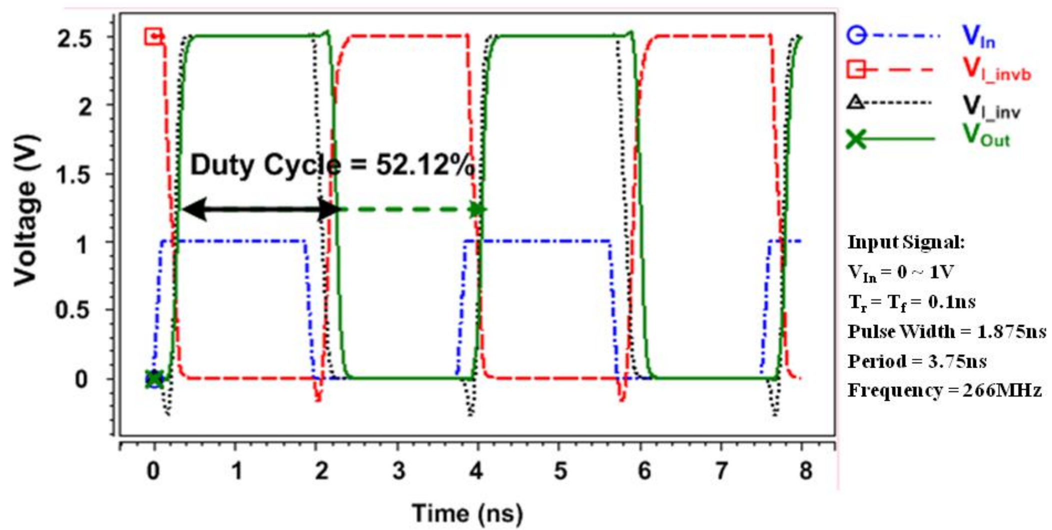


Fig. 2.17 Simulation waveforms of level shifter circuit with the pseudo worst case (85°C, TT), 1.0-V VDD, 2.5-V VDDIO, and C_{load} = 20fF.

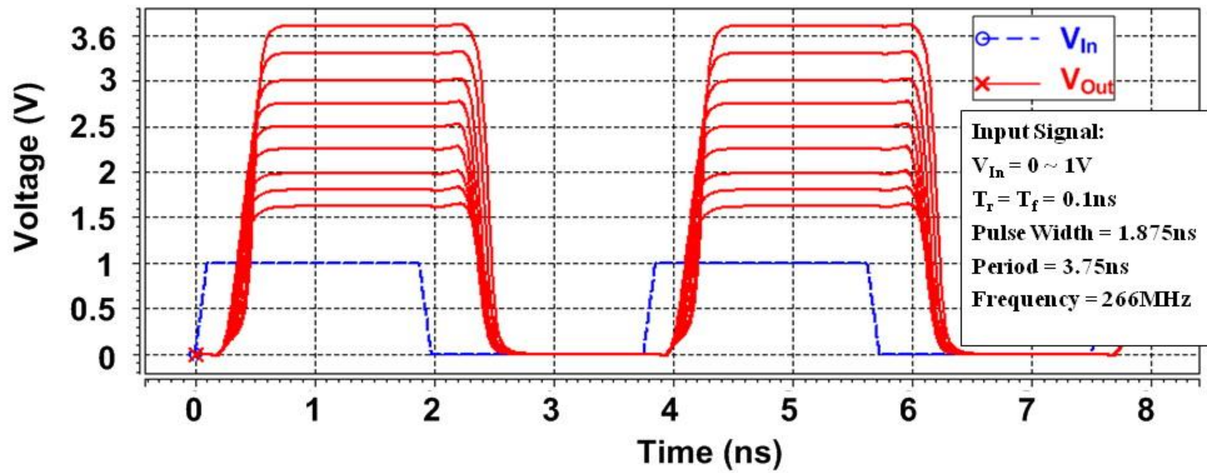


Fig. 2.18 Simulation waveforms of level shifter circuit operating in different VDDIO voltage supply with the pseudo worst case (85°C/TT), 1.0-V VDD, and C_{load} = 20fF.

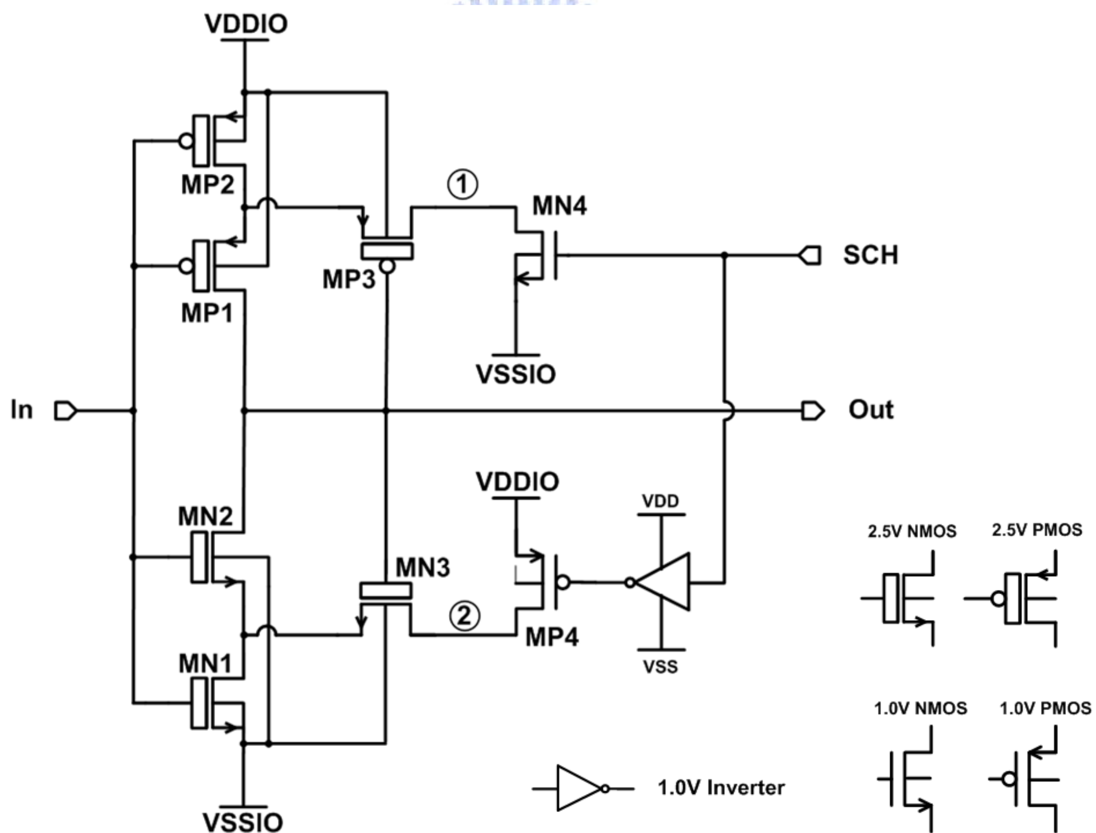


Fig. 2.19 Circuit diagram of schmitt-trigger with an enable signal (SCH).

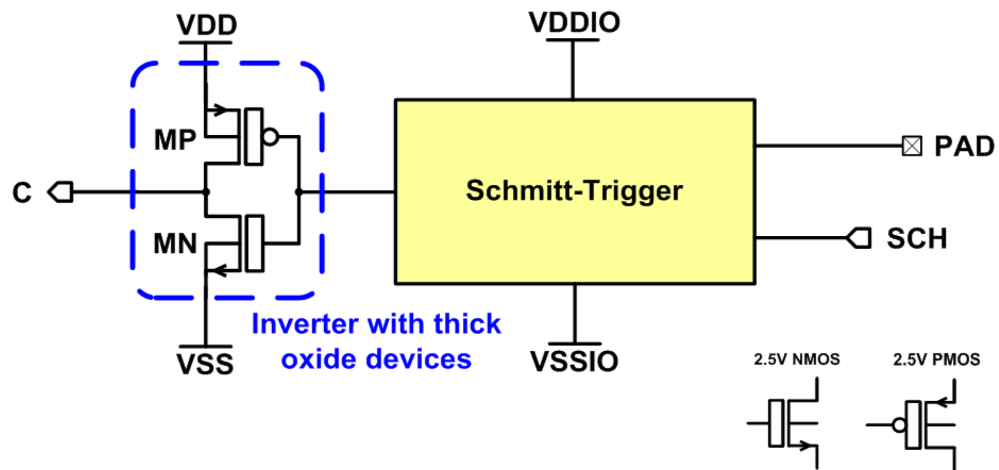
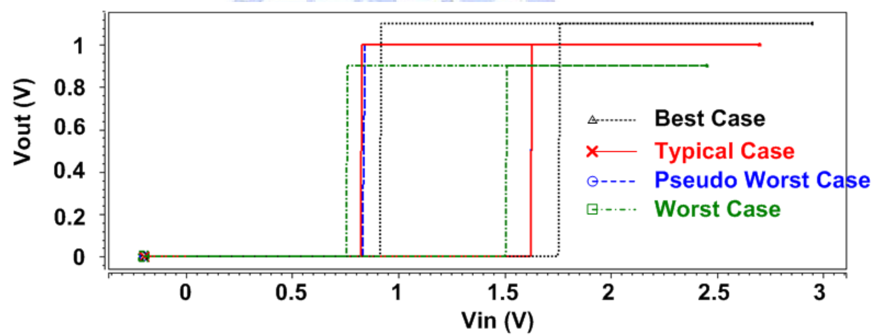
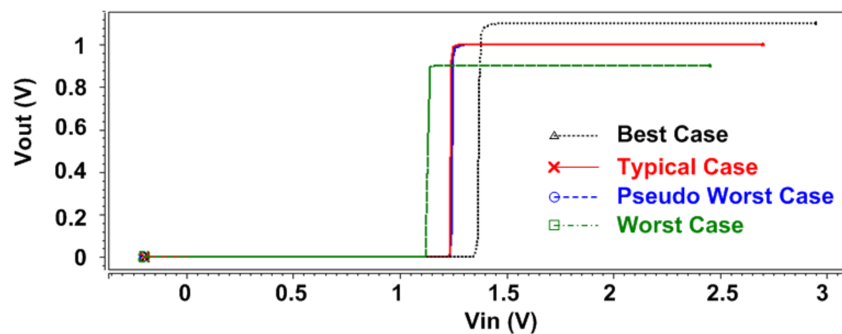


Fig. 2.20 Circuit diagram of input stage.



(a)



(b)

Fig. 2.21 Voltage transform curve (VTC) of input stage with (a) SCH = 1 and (b) SCH = 0.

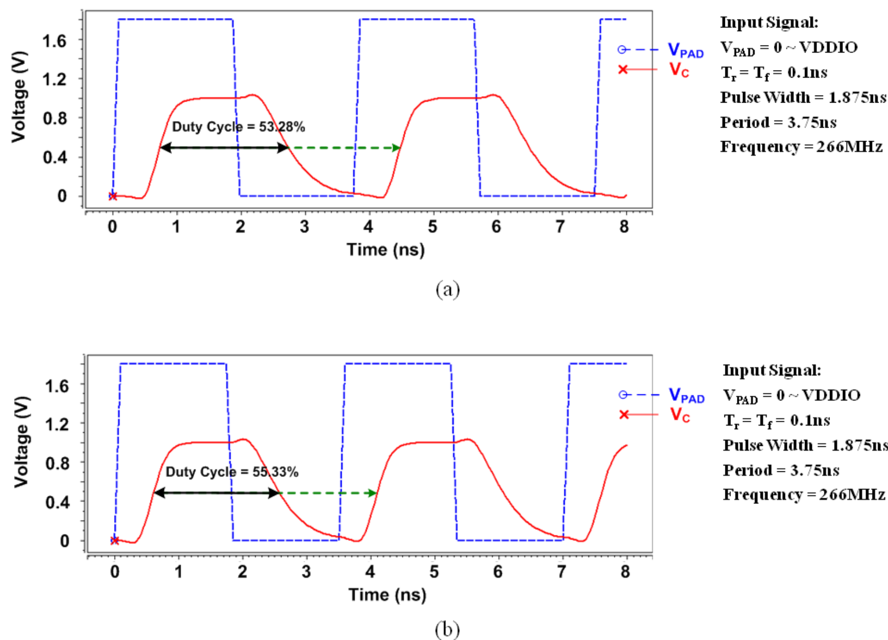


Fig. 2.22 Simulation waveforms of (a) schmitt-trigger input stage (SCH = 1) and (b) normal input stage (SCH = 0) with the pseudo worst case, C_{load} = 0.1pF, 1.0-V VDD, and 1.8-V VDDIO.

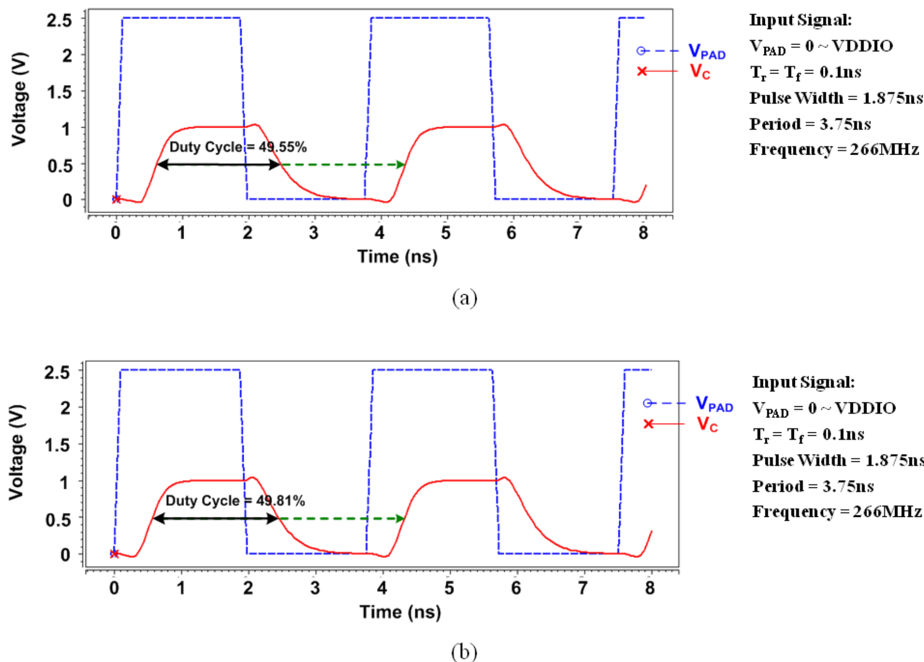
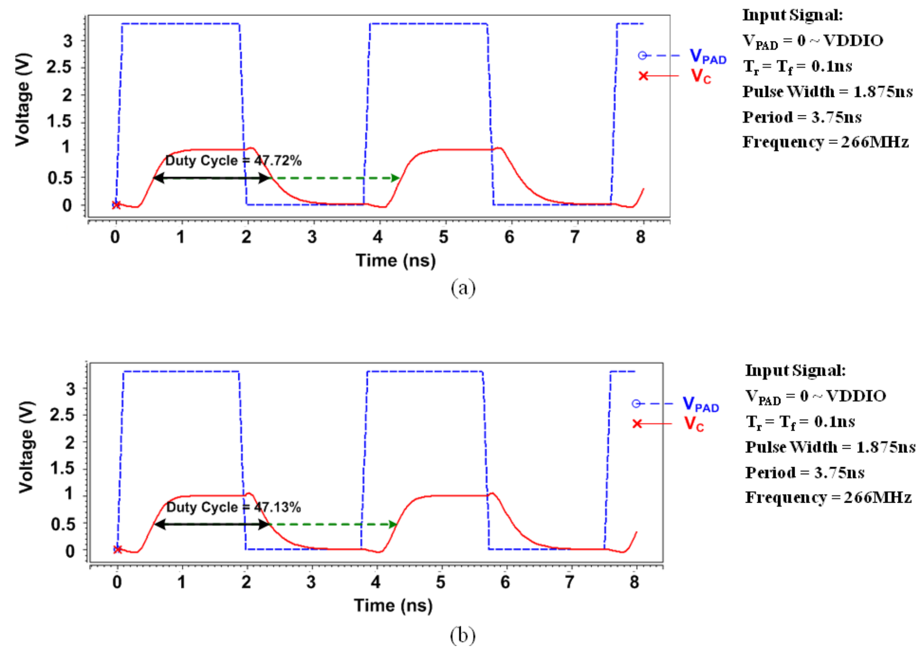


Fig. 2.23 Simulation waveforms of (a) schmitt-trigger input stage (SCH = 1) and (b) normal input stage (SCH = 0) with the pseudo worst case (85°C/TT), Cload = 0.1pF, 1.0-V VDD, and 2.5-V VDDIO.



(a)

(b)

Fig. 2.24 Simulation waveforms of (a) schmitt-trigger input stage (SCH = 1) and (b) normal input stage (SCH = 0) with the pseudo worst case (85°C/TT), C_{load} = 0.1pF, 1.0-V VDD, and 3.3-V VDDIO.

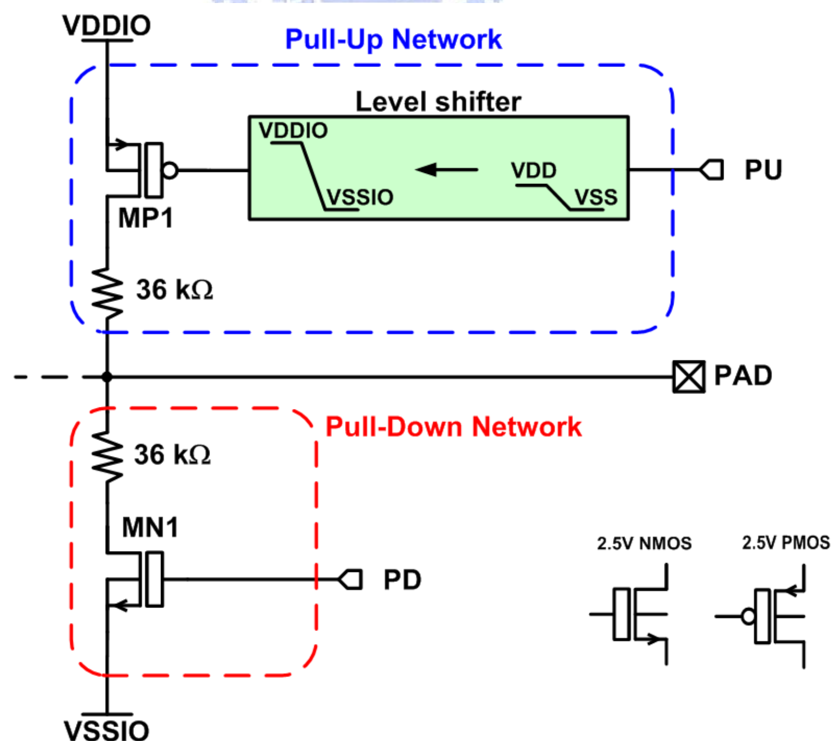
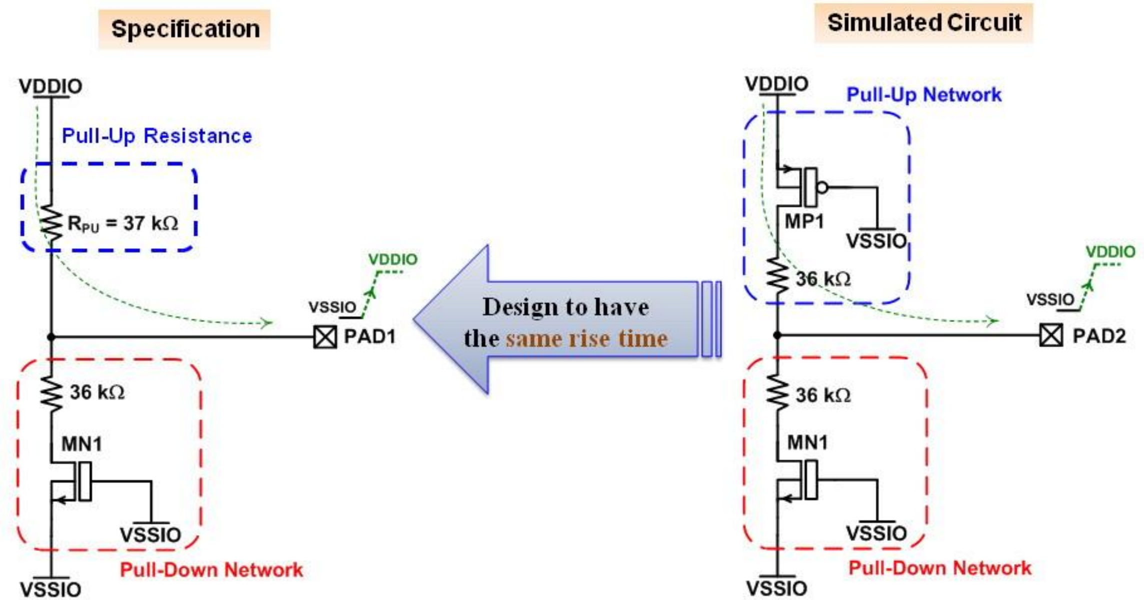
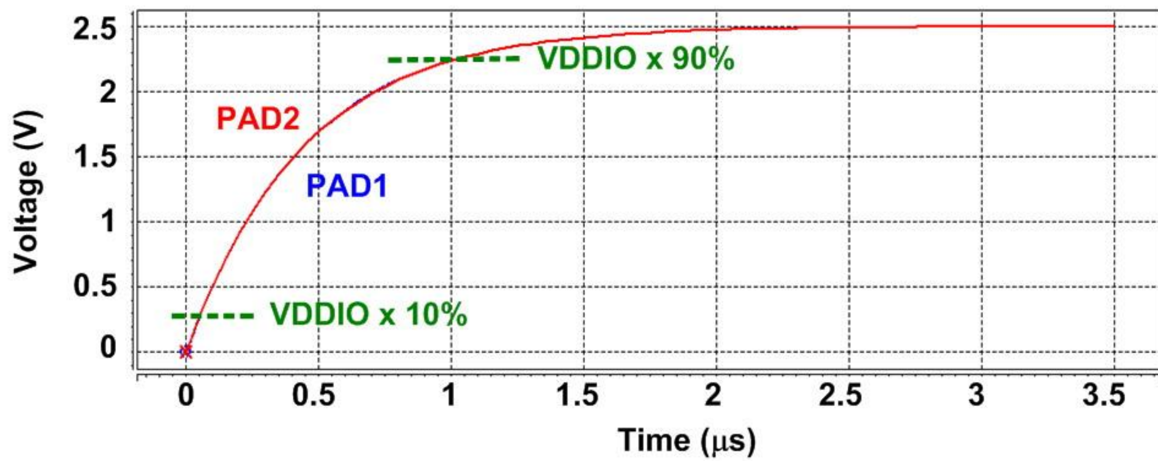


Fig. 2.25 Circuit implementation of pull-up and pull-down network.

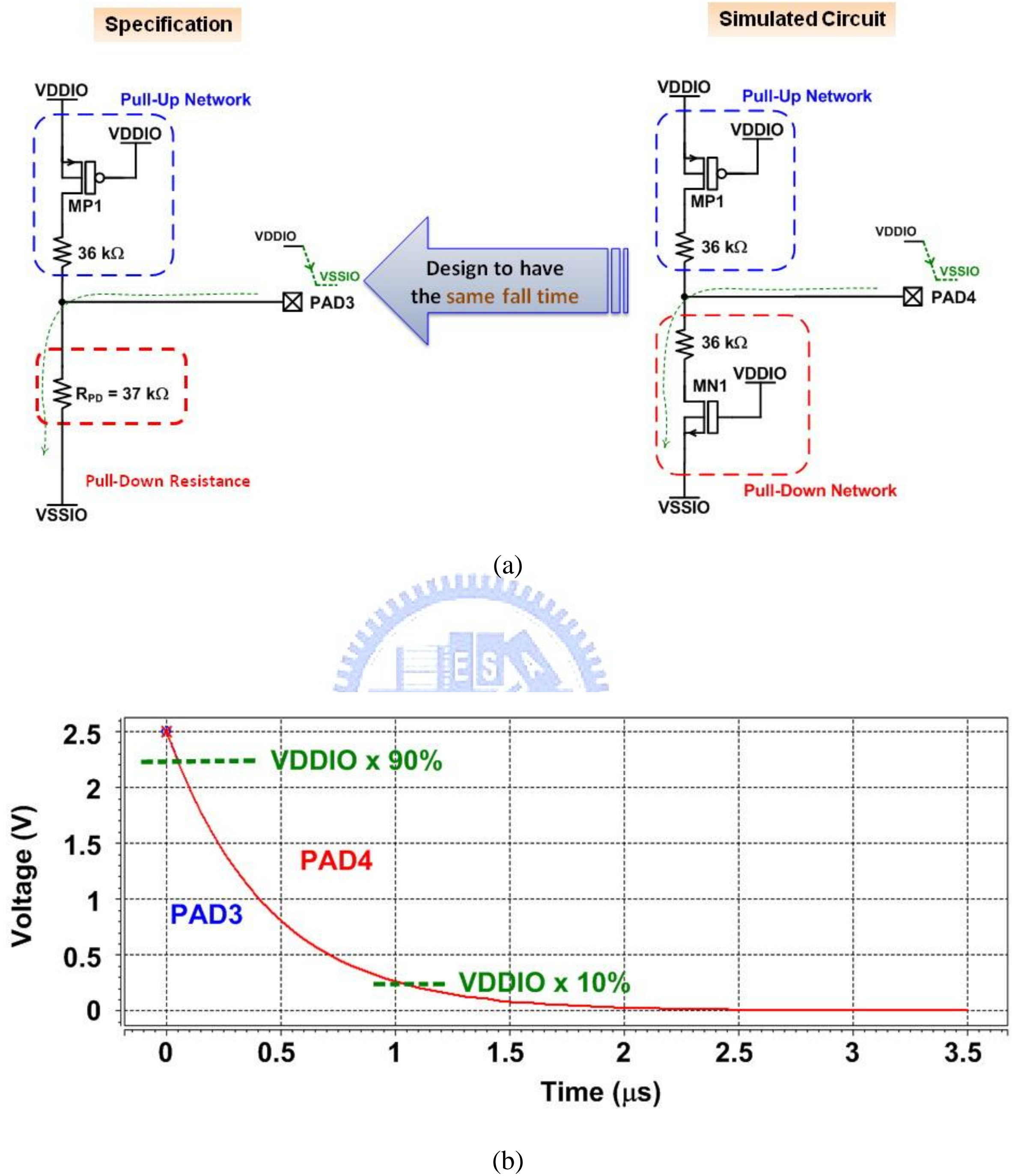


(a)



(b)

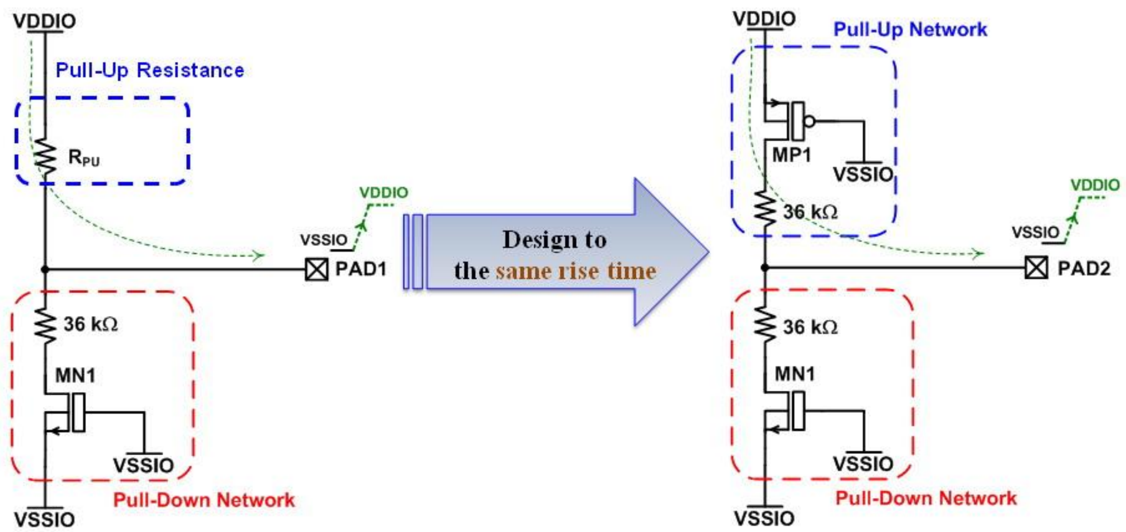
Fig. 2.26 Determination of pull-up MOS (MP1) size; (a) simulated method, and (b) simulated result.



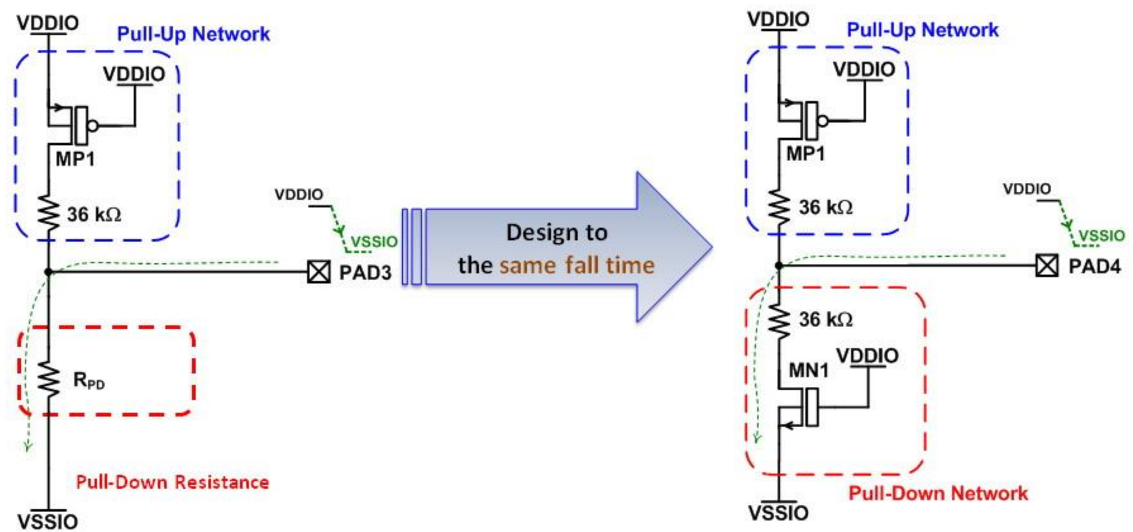
(a)

(b)

Fig. 2.27 Determination of pull-down MOS (MN1) size; (a) simulated method, and (b) simulated result.



(a)



(b)

Fig. 2.28 Simulation setup of equivalent (a) pull-up resistance and (b) pull-down resistance in pull-up/pull-down network.

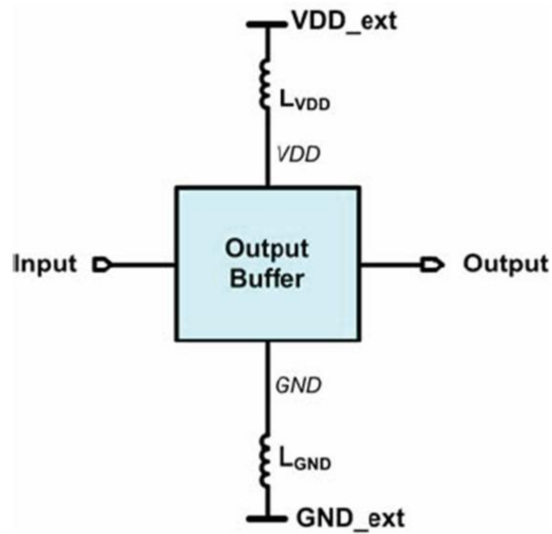


Fig. 2.29 The model for ground bounce effect.

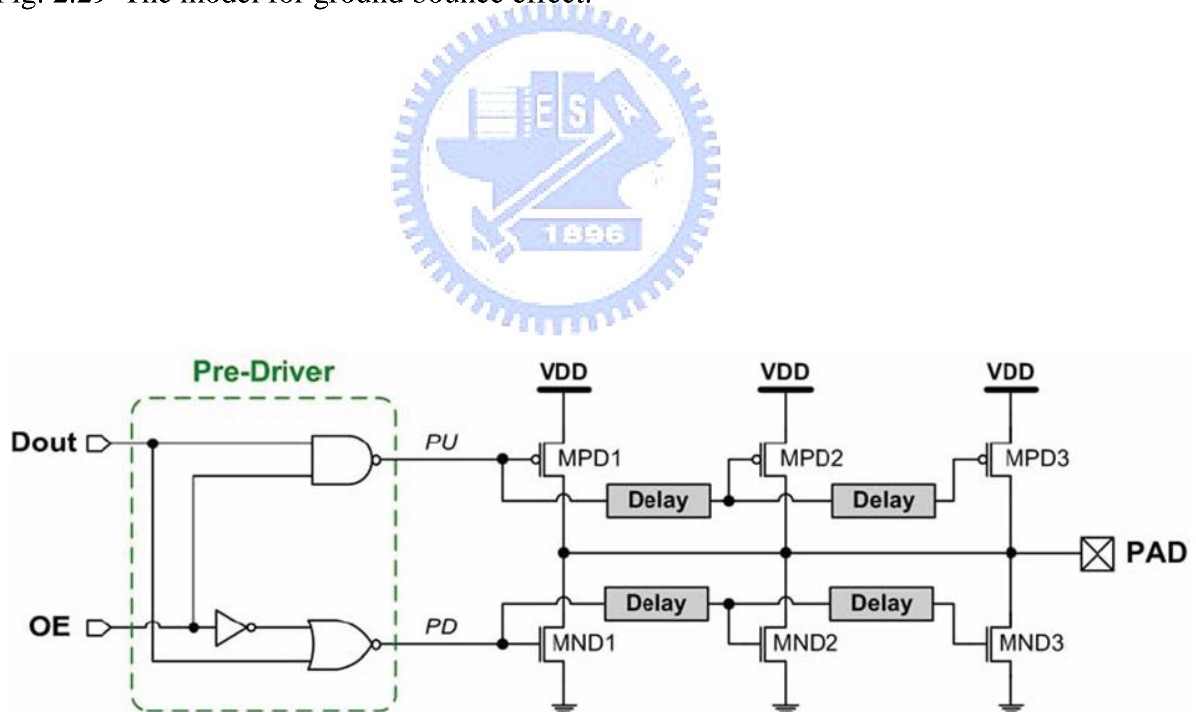


Fig. 2.30 Output buffer with slew-rate control.

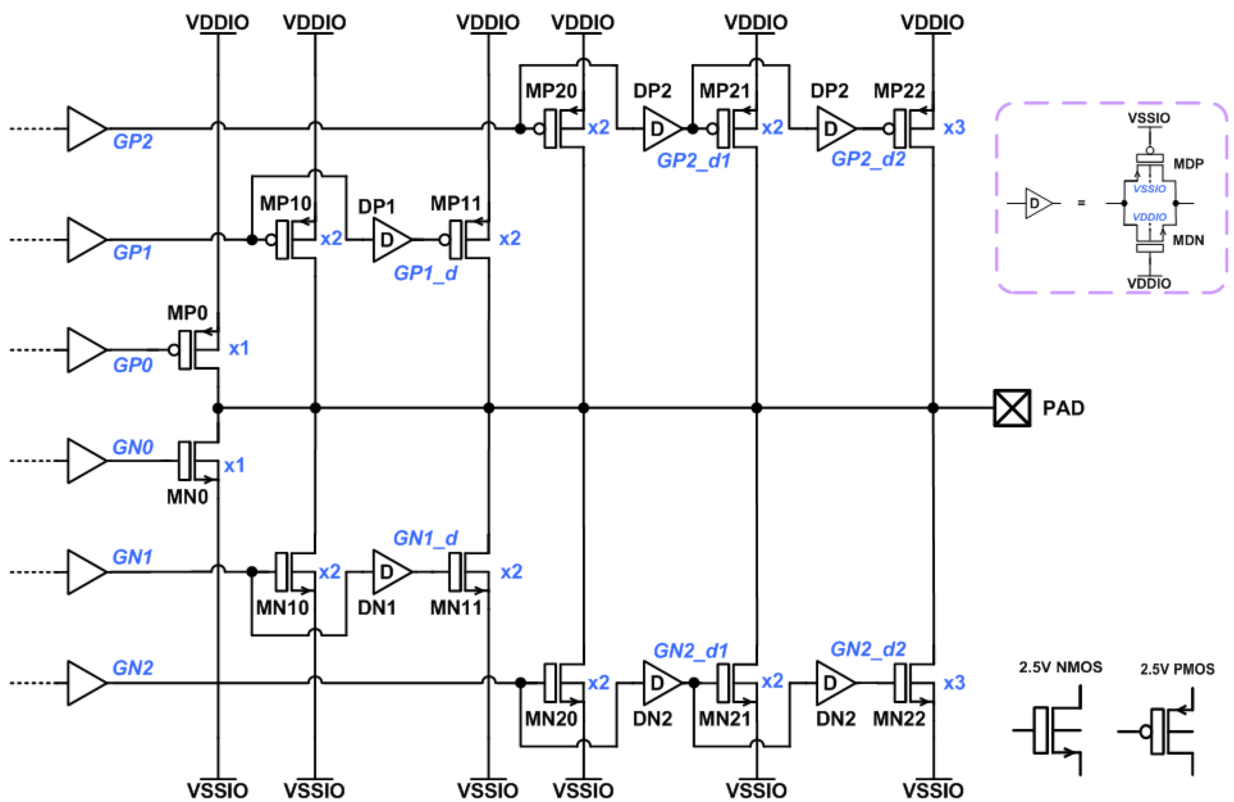


Fig. 2.31 Design for output driver of configurable I/O cell with slew-rate control.

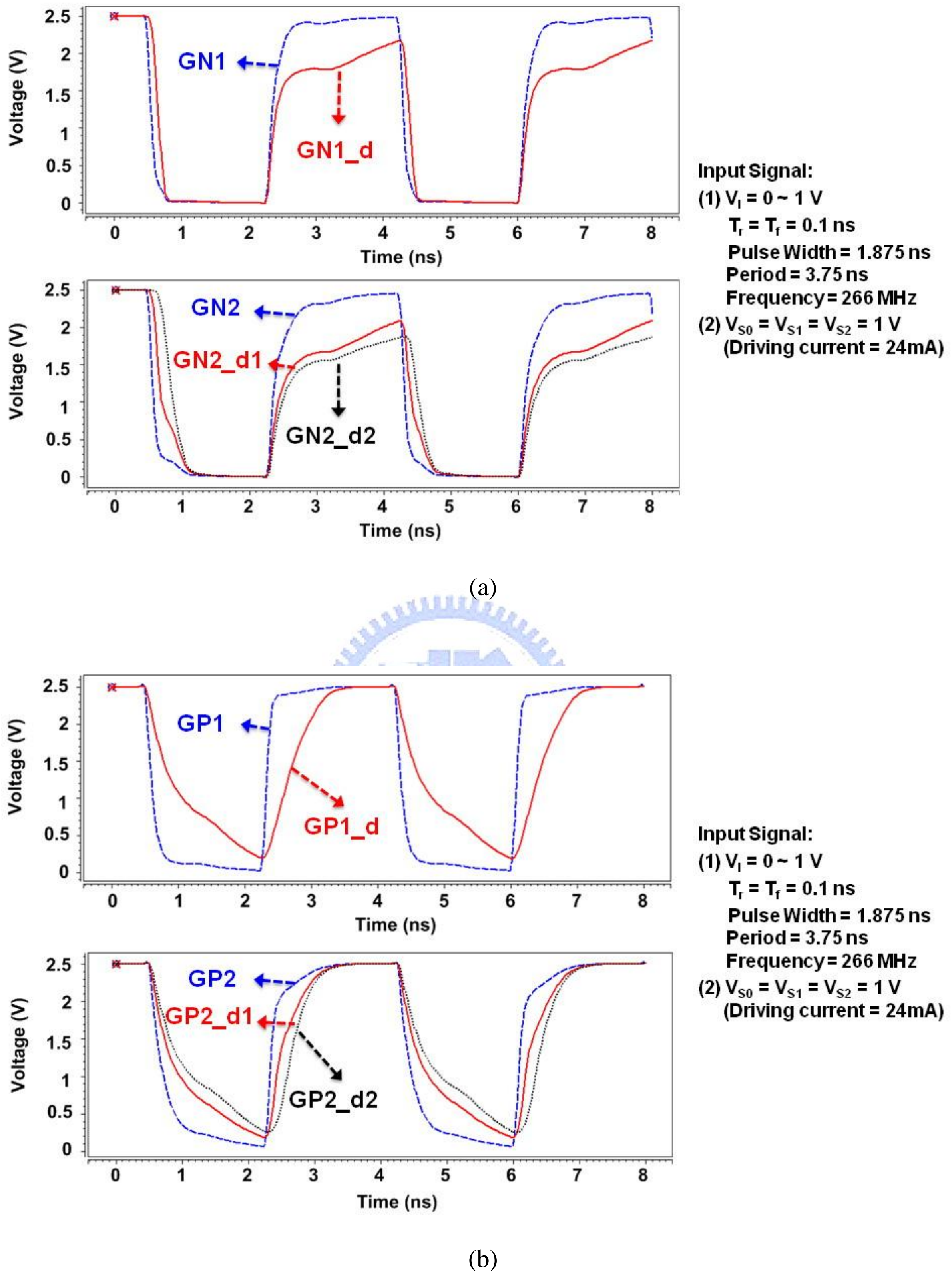
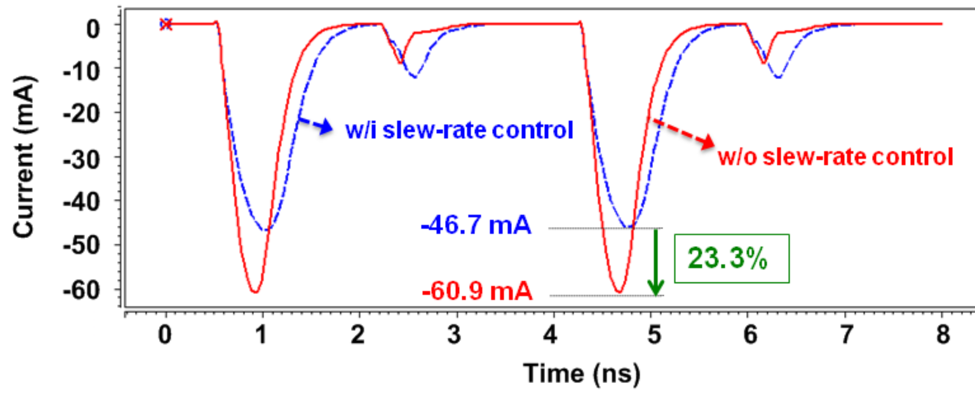
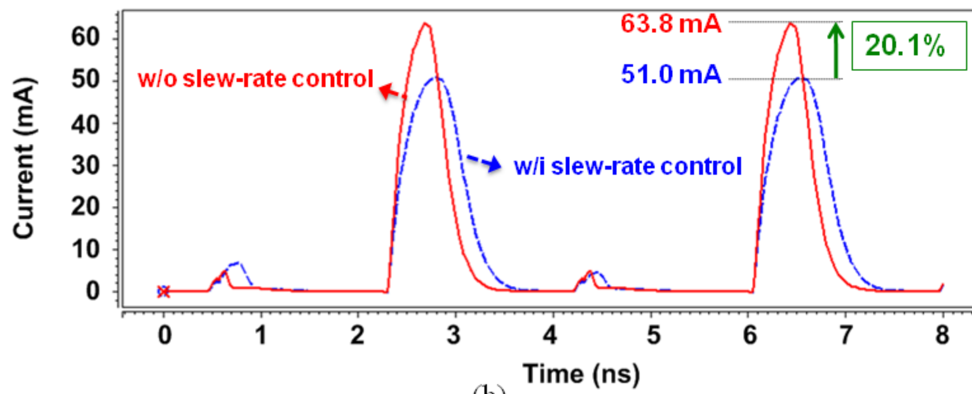


Fig. 2.32 Gate-controlled signals of (a) output NMOS and (b) output PMOS with slew-rate control under the pseudo worst case (85°C/TT),1.0-V VDD, 2.5-V VDDIO, and C_{load} = 12pF.

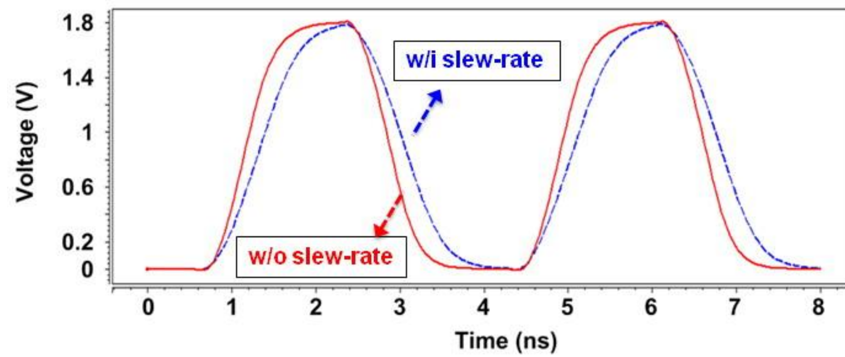


(a)

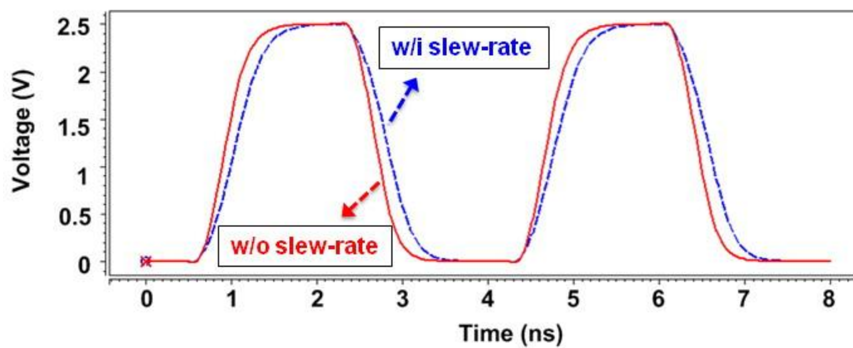


(b)

Fig. 2.33 Switching current on (a) VDDIO power line and (b) VSSIO ground line.



(a)



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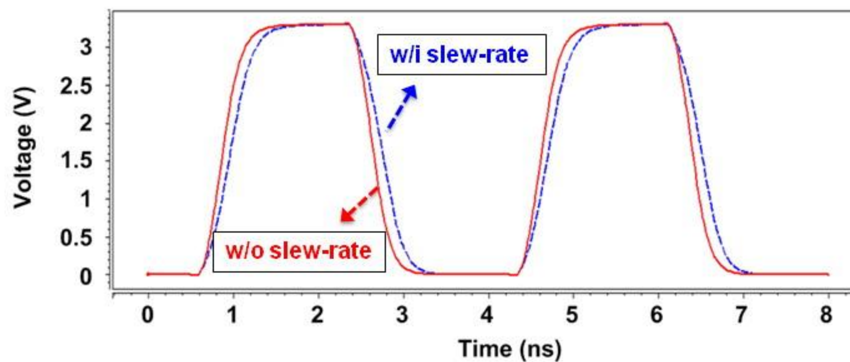


(c)

Fig. 2.34 Output waveforms of configurable I/O cell with the pseudo worst case (85°C/TT), 1.0-V VDD, C_{load} = 12pF, (a) 1.8-V VDDIO, (b) 2.5-V VDDIO, and (c) 3.3-V VDDIO.

Chapter 3

Design of ESD Protection Circuits

3.1 INTRODUCTION

To provide efficient ESD protection for CMOS ICs, the on-chip ESD protection circuits have to be designed and placed around the input, output, and power pads. In Fig. 3.1, the PMOS and NMOS are used as on-chip ESD protection devices for input and output pads. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of PMOS from I/O pad to VDD, and then through the VDD-to-VSS ESD clamp circuit to ground. However, due to the parasitic resistance and capacitance exist the VDD and VSS power lines, the efficiency of ESD protection is dependent on the pin location in a chip. To quickly bypass the ESD current during ESD-stress condition, the efficient VDD-to-VSS ESD clamp circuits are repeatedly inserted between VDD and VSS power lines in the appropriate distance to provide a low-impedance path between the VDD and VSS power lines [10].

Therefore, this 90-nm 1.0-V/2.5-V I/O cell library provides not only configurable I/O cells (UCIOS, UCIONS, and UINPUT), but also has power/ground cells (UVDD25, UVSS25, UVDD10, and UVSS10), analog I/O cells (UAIO25 and UAIO10), and power break cell (UPBREAK). The circuit design concepts of these cells are investigated in followings.

3.2 POWER/GROUND CELLS

As listed in Table 1.1, this 90-nm configurable I/O cell library provides five power/ground cells denoted as UVDD25, UVSS25, UVDD10, and UVSS10. UVDD25 and UVSS25 cells are supply voltages of I/O ring, and UVDD10 and UVSS10 cells are that of pre-driver and core circuits. Fig. 3.2 shows the block diagram of the whole-chip ESD protection circuit.

Power clamp ESD protection circuits should keep off and prevent the undesirable leakage current or malfunction during normal circuit operating condition. Under ESD stress condition, power clamp ESD protection circuits should be turned on quickly to provide effective ESD protection for internal and I/O circuits. Fig. 3.3 shows the circuit design of UVDD25 and UVDD10 cells which are designed by gate-driven technique. The gate-driven technique has been reported that it can effectively improve ESD reliability in submicron CMOS technology [15]-[18]. MOS-based, RC-triggered power clamps use a large NMOS drawn without consideration ESD rule (often referred to as a “BigFET”) to provide a low impedance path for discharge current [19]-[21]. The advantage of using the BigFET device is not needed to rely on junction avalanche breakdown phenomena and can thus be easily simulated using SPICE at an early design stage, enabling circuit optimization while maintaining technology independence [22]. To ensure that the ESD device is fully-on for the duration of the ESD event, the RC timer needs to have a time constant greater than or equal to the ESD pulse width – usually 1μs is selected to allow for process variations. Fig. 3.4 shows the simulated results of UVDD25 and UVSS25 cell under power-on condition and ESD stress condition. Under the power-on condition, the point Vg maintains a ground voltage level. As shown in Fig. 3.4(b), when the power VDDIO is rising up to 5-V voltage, the point Vg is pulled up to 5-V voltage closely. Hence, the large NMOS MN2 can be turn on to discharge the

ESD current.

The circuit diagrams of UVSS25 and UVSS10 cells are shown in Fig. 3.5. These two cells have a set of bidirectional diode to connect the VSS and VSSIO ground lines. Under the normal circuit operating condition, UVSS25 and UVSS10 provide the ground voltage supply for the VSSIO and the VSS ground lines, respectively. Thus, the noise of the VSSIO ground line will not affect the VSS ground line. Under the ESD stress condition, the bidirectional diode can provide paths between VSSIO and VSS ground lines to discharge the ESD current.

For layout consideration, a gate-couple technique is used in UVSS25 cell as shown in Fig. 3.5(a). This technique has been reported to effectively improve ESD reliability in submicron CMOS technology [15]-[16], [23]. The UVSS25 cell is designed with the NMOS (MN1) drain snapback breakdown to discharge the ESD current. Note that the MN1 has to draw with consideration of ESD rule in topological layout. Furthermore, the ESD protection ability of using NMOS drain snapback breakdown is stronger than that of using BigFET, but the trigger time of NMOS drain snapback breakdown is slower than the turn on time of BigFET under ESD stress condition. Therefore, The UVSS25 cell is used as the secondary protection to clamp ESD voltage between the VDDIO and VSSIO power lines. As shown in Fig. 3.6, the point Vc is pulled up enough to trigger the MN1 drain snapback breakdown under ESD stress condition.

The ESD protection element is implemented by STSCR (substrate-triggered silicon-controlled rectifier) shown in Fig. 3.5(b), which has been reported to effectively protect the thin gate oxide devices [24]. In the I/O cells, double guard rings have been often inserted between input (or output) PMOS and NMOS devices to avoid the latchup issue [25]. The layout view and device structures of traditional I/O cell are shown in Fig. 3.7(a) and (b), respectively. However, the maximum supply voltage is only 1.0V in 90-nm CMOS

technology with thin gate oxide of 22.5Å. If the holding voltage of parasitic SCR device is greater than the power supply voltage, latchup issue will not occur in such nanoscale CMOS process. Therefore, the STSCR can be used as on-chip ESD protection device without latchup concern in nanosacle CMOS process.

3.3 ANALOG I/O CELLS

As listed in Table 1.1, this configurable I/O cell library provides two analog I/O cells (UAIO25 and UAIO10). Fig. 3.8 shows the circuit diagram of the UAIO25 and the UAIO10 cells. The UAIO25 cell is designed with a BigFET as ESD element, and the UAIO10 is designed with a STSCR mentioned in section 3.2. The pins PADwiR or PADwoR are used to connect the input or output end of core analog circuit. When the PS-mode ESD stress occurs at I/O PAD, the ESD current can be discharge through the diode (D2) from I/O PAD to VDDIO(or VDD), and then through the VDDIO-to-VSSIO (or VDD-to-VSS) power clamp ESD protection circuit. When the ND-mode ESD stress occurs at I/O PAD, the ESD current can be discharge through the diode (D1) from I/O PAD to VSSIO (or VDD), and the through the power clamp ESD protection circuit.

3.4 POWER BREAK CELL

To overcome the unexpected ESD damage located at the internal circuit, adding the bi-directional diode between the separated power lines of the CMOS IC has been reported [26]-[28]. The design of such bi-directional diode in this thesis is defined as UPBREAK cell and shown in Fig. 3.9, where the bi-directional diodes are used to connect the

VDD1/VDDIO1 and VDD2/VDDIO2, or the VSS1/VSSIO1 and VSS2/VSSIO2, power lines of the CMOS IC. The UPBREAK cell is designed to conduct the ESD current between the separated power lines to avoid the ESD damage located at the internal circuits under the ESD stress condition. When the IC is in the normal operating condition, the UPBEAK cell is designed to block the noise between the separated power lines.

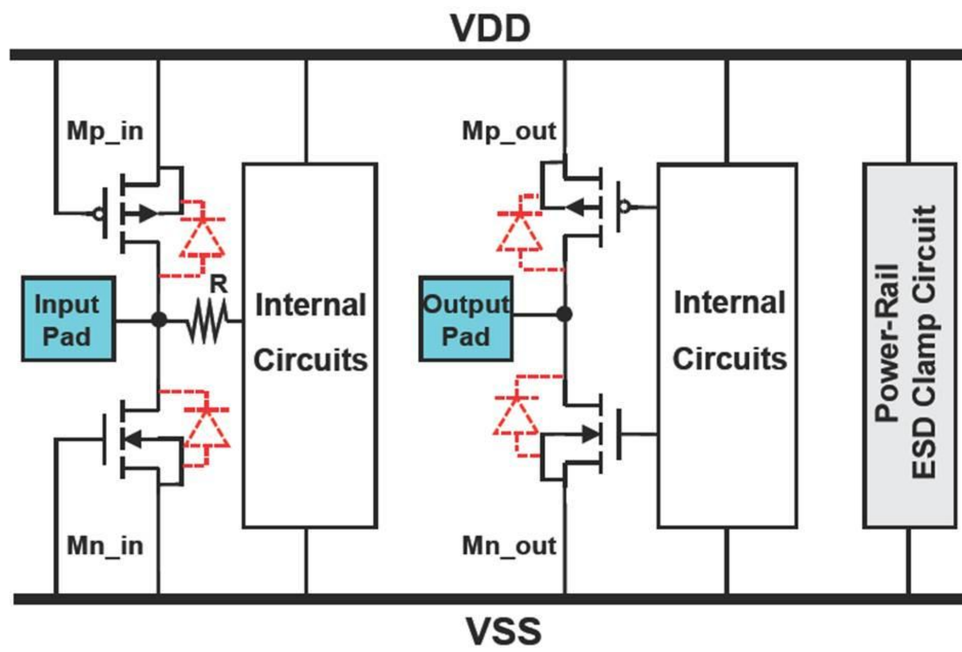


Fig. 3.1 Typical on-chip ESD protection circuits in a CMOS IC.

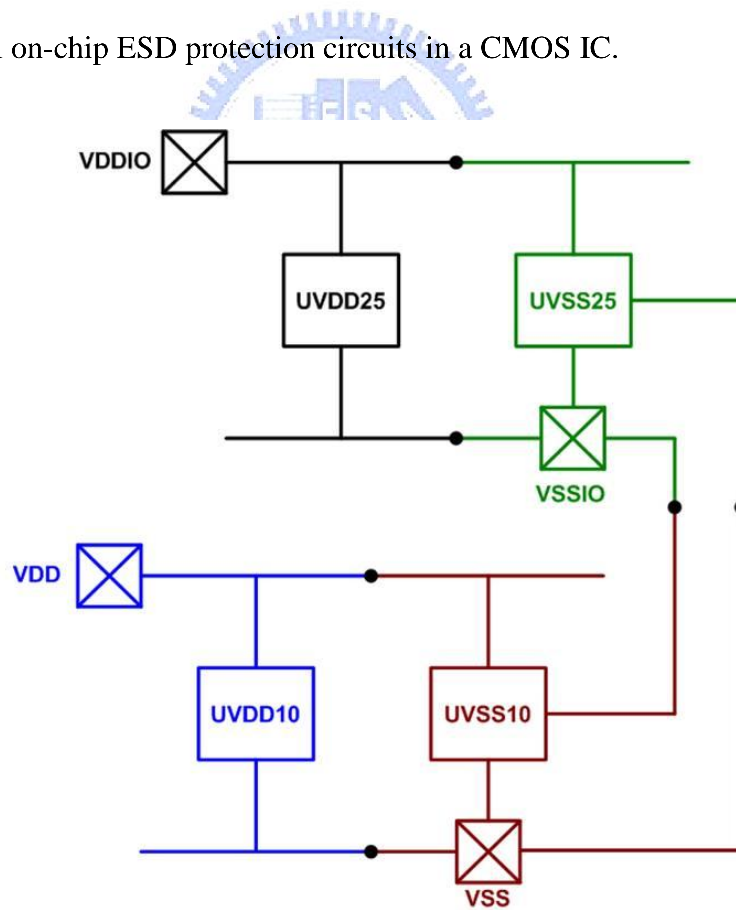
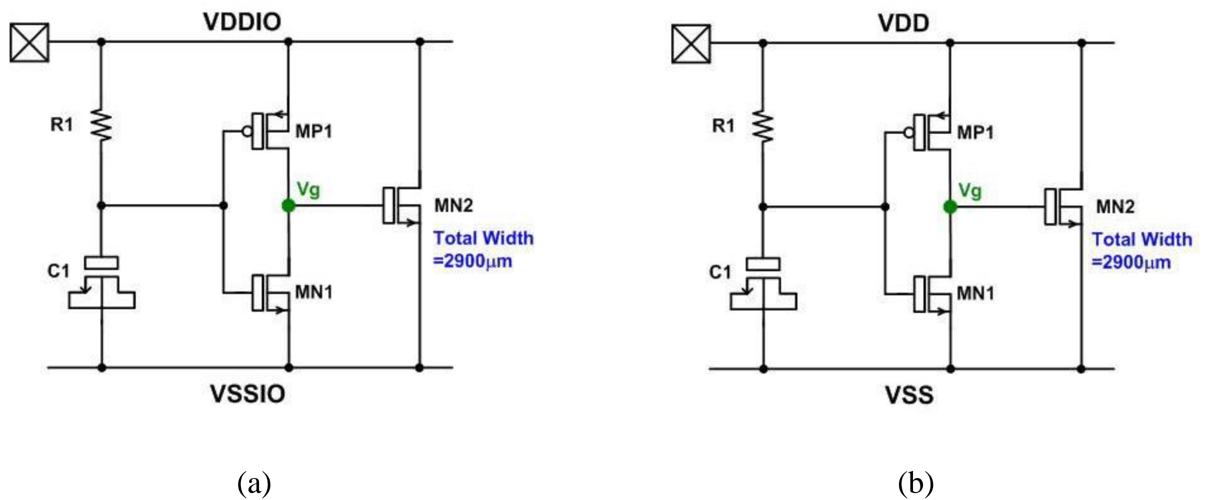
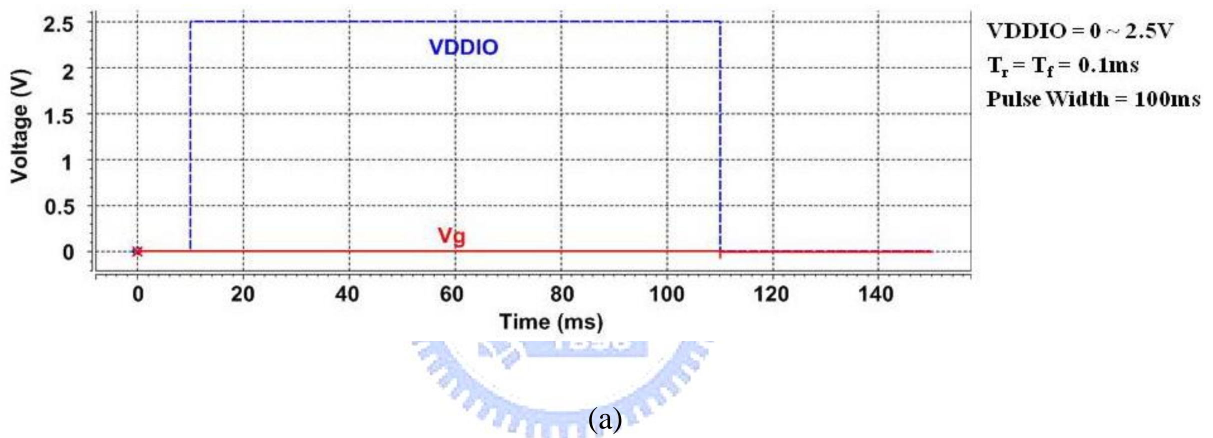


Fig. 3.2 Whole-chip ESD protection scheme.

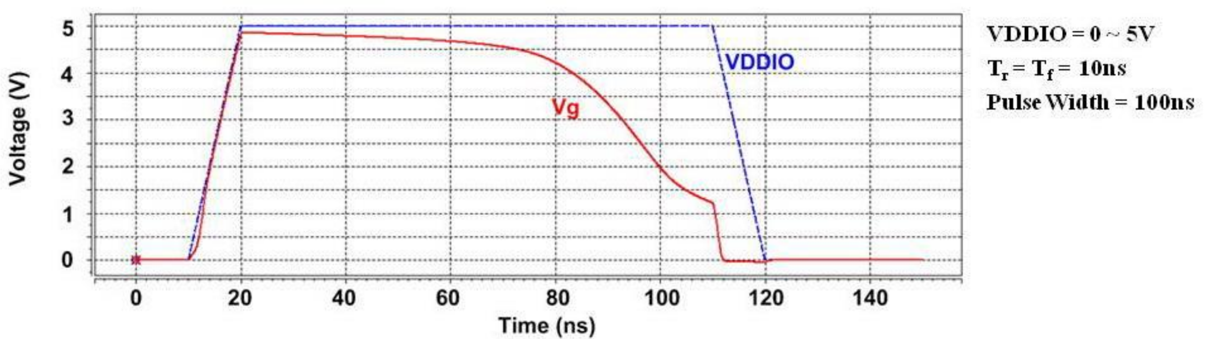


(a) (b)

Fig. 3.3 Circuit diagram of (a) UVDD25, (b) UVDD10 cells.

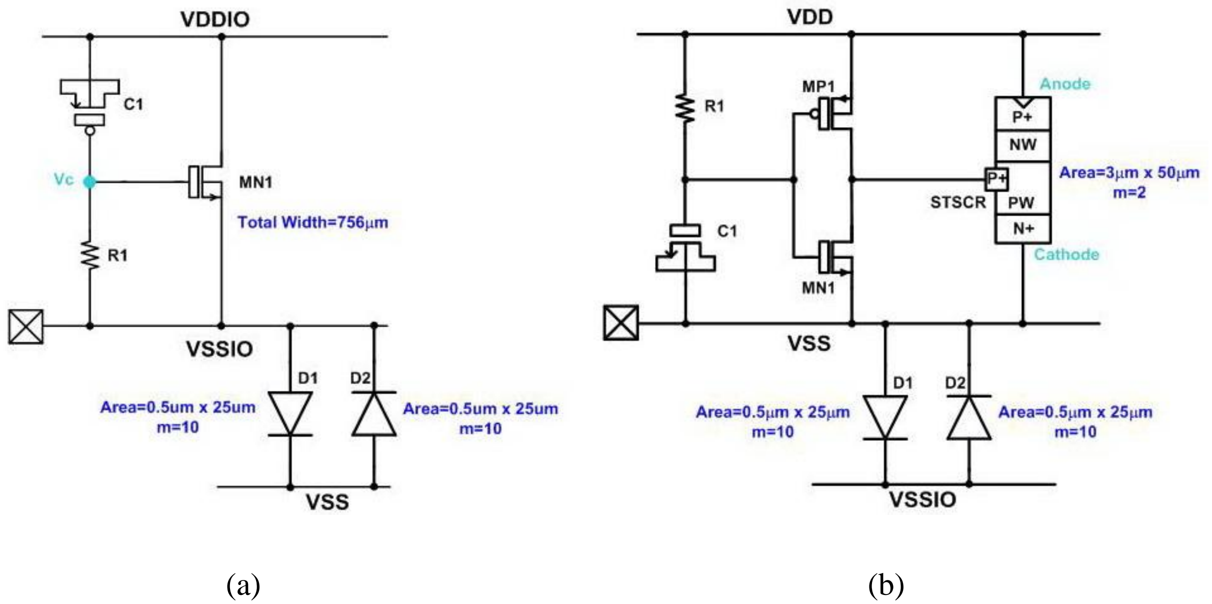


(a)



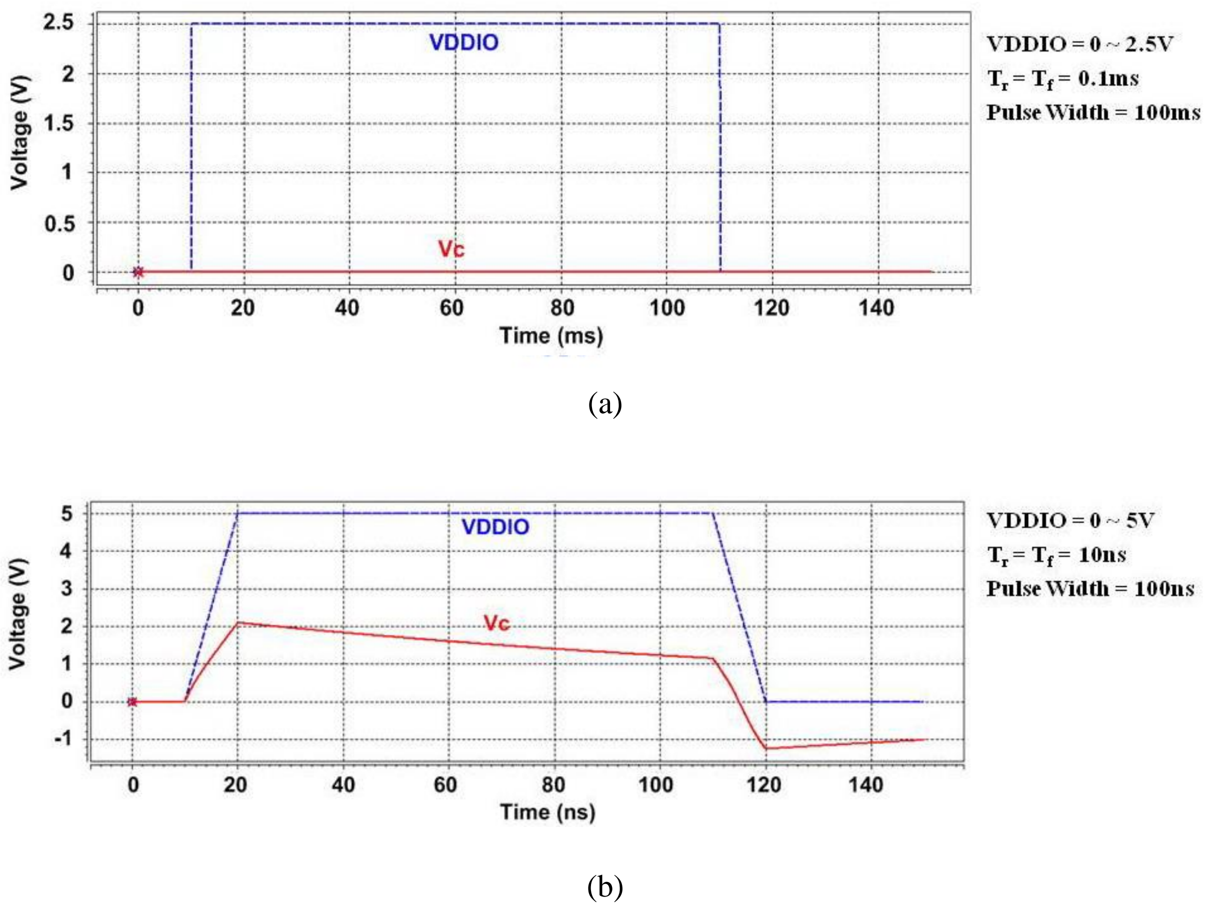
(b)

Fig. 3.4 Simulated results of UVDD25 and UVSS25 cells under (a) power-on condition and (b) ESD stress condition.



(a) (b)

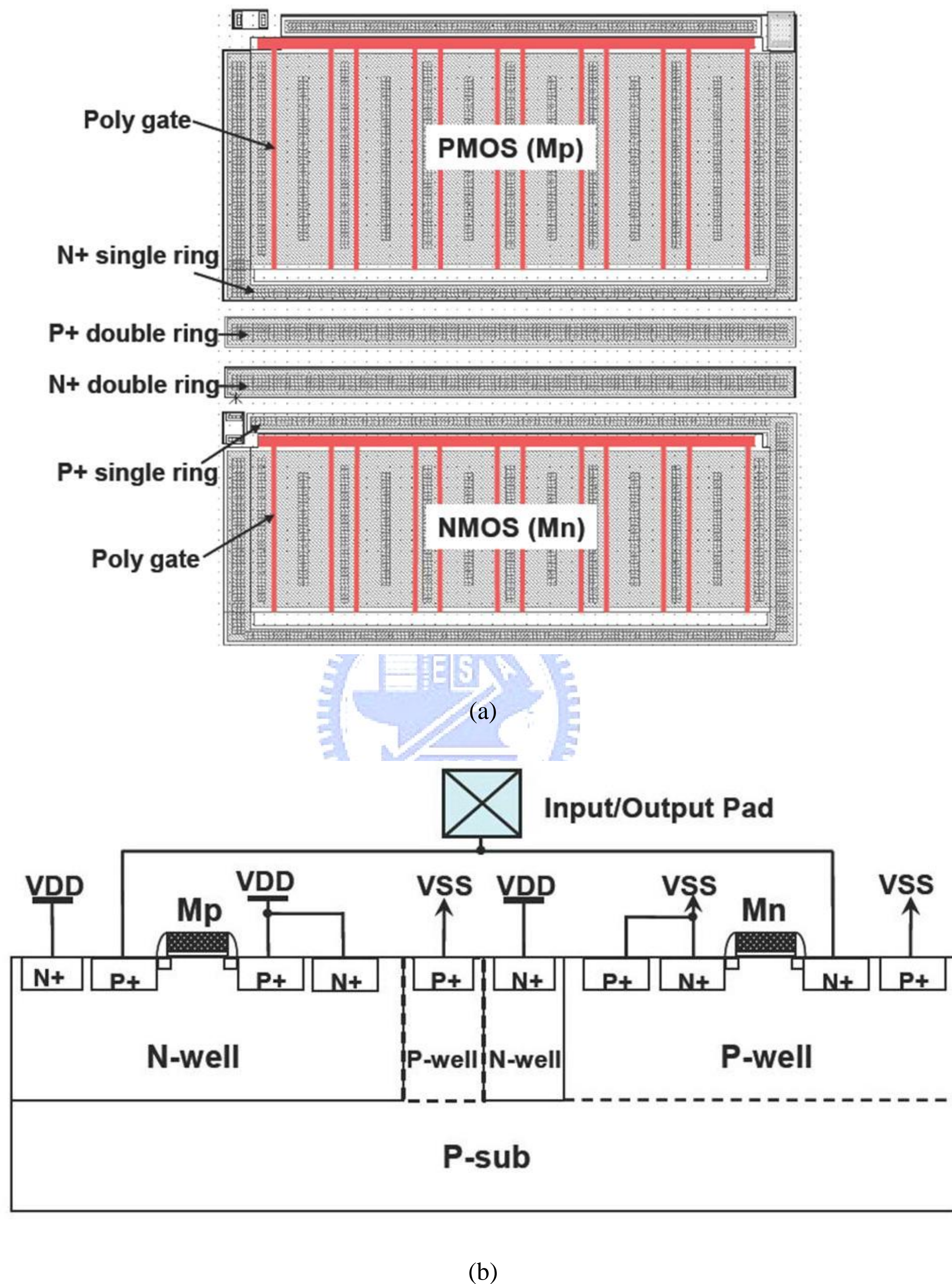
Fig. 3.5 Circuit diagram of (a) UVSS25, and (b) UVSS10 cells.



(a)

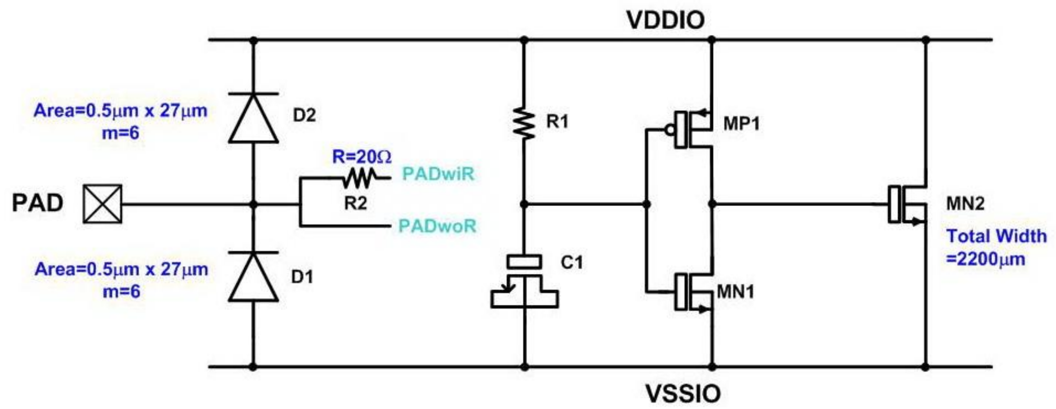
(b)

Fig. 3.6 Simulated results of UVSS25 cell under (a) power-on condition and (b) ESD stress condition.

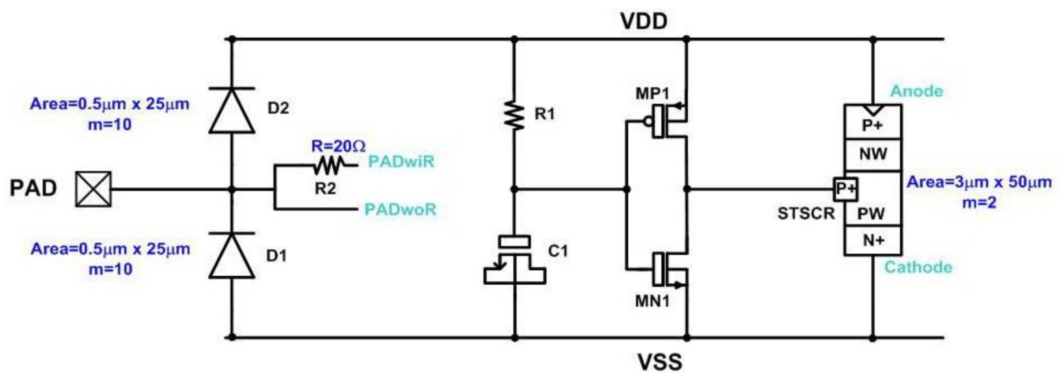


(b)

Fig. 3.7 (a) Layout view and (b) device structures of the I/O cell with double guard rings inserted between input (or output) PMOS and NMOS devices.



(a)



(b)

Fig. 3.8 Circuit diagram of (a) UAIO25 and (b) UAIO10 cells.

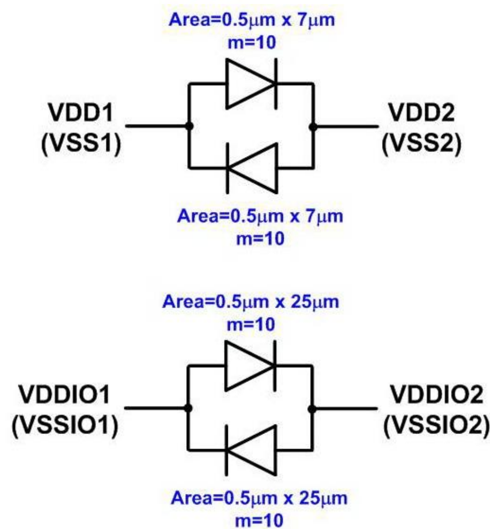


Fig. 3.9 Circuit diagram of power break cell.

Chapter 4

Physical Layout of Configurable I/O Cell Library

4.1 CONFIGURABLE I/O CELL WITH SLEW-RATE CONTROL

Fig. 4.1 shows layout implementation of the configurable I/O with slew-rate control cell (UCIOS) and the power line. The power line is drawn with from metal 4 (M4) to top metal (M9). Fig. 4.2 shows the cross section view of bond pad which is used with BOAC (bond over active circuit) structure. And the corresponding layer names are listed in Table 4.1. Furthermore, the particular block layout views of the UCIOS cell are shown in Fig. 4.3. The difference in physical layout between configurable I/O without slew-rate control cell (UCIONS) and with slew-rate control cell (UCIOS) is the drawing of slew-rate control. As shown in Fig. 4.4, the drain and source terminals of transmission gates are all connected to VSSIO. The gates of NMOS are connected to VSSIO through a resistance, and that of PMOS are connected to VDDIO through a resistance. Thus, the function of the slew-rate control can be turned off when the UCIONS is in normal operation.

4.2 POWER/GROUND CELLS AND ANALOG I/O CELLS

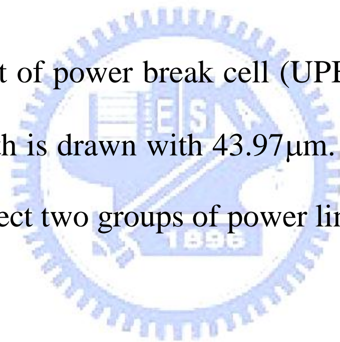
Fig. 4.5(a) shows the layout implement of the UVDD25 cell. In this layout view, only layers below the layer via3 (including the layer via3) are shown, and the other layers not shown are the routing of the power line. The cell width and hight are as same as the I/O cells.

The layout structure of the UVDD10 cell is similar to the UVDD25 cell, and metal routing is only different between two cells. Fig. 4.5(b) and (c) show the layout implements of the UVSS25 and UVSS10 cells which are designed in gate-couple and STSCR technique, respectively. The layout-top-views of the UAIO25 and UAIO10 cells are shown in Fig. 4.6.

Furthermore, the device layout of STSCR drawn in UVSS10 and UAIO10 cells is shown in Fig. 4.7. The STSCR structure is formed with construction between P+ diffusion of Anode and N+ diffusion of Cathode.

4.3 POWER BREAK CELL

Fig. 4.8 shows the layout of power break cell (UPBREAK). Its cell height is as same as the I/O cells, but the cell width is drawn with 43.97μm. The power break cell is composed of bidirectional diode to disconnect two groups of power lines.



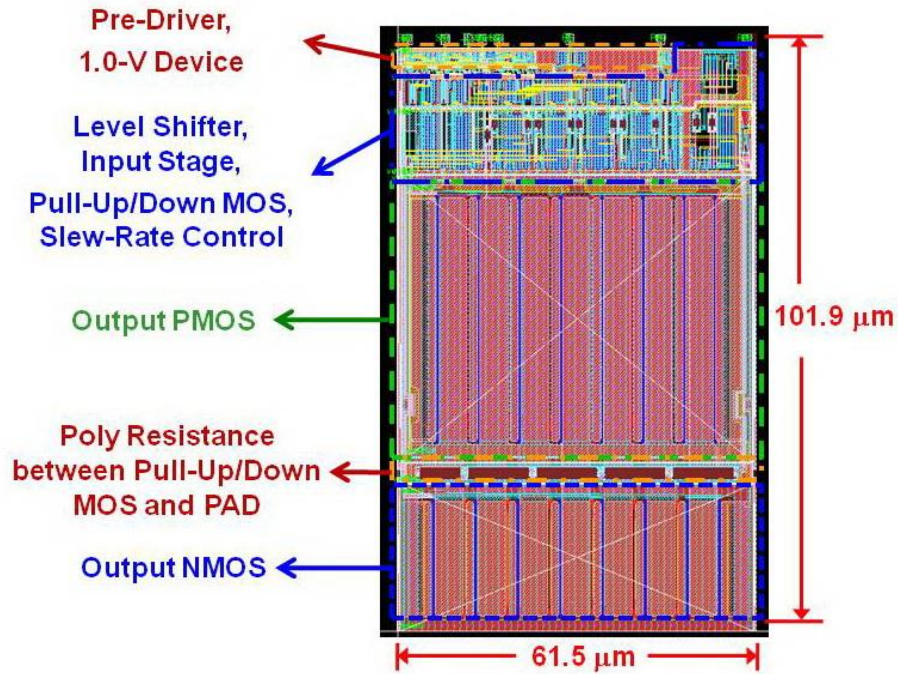
4.4 FILLER AND CORNER CELLS

Fig. 4.9 shows the layout-top-view of the filler cells (UFeederXX). The filler cells are used to fill the empty space between the I/O cells. It would connect the power lines to provide a continuous power supply. There are nine different sizes (0.1-μm, 0.3-μm, 0.5-μm, 1-μm, 2-μm, 5-μm, 10-μm, 15-μm, and 20-μm) of the filler cells provided in the I/O cell library. And Fig. 4.10 shows the layout-top-view of the corner cell (UCorner). It provides a connection between the power and ground rails in die corner areas.

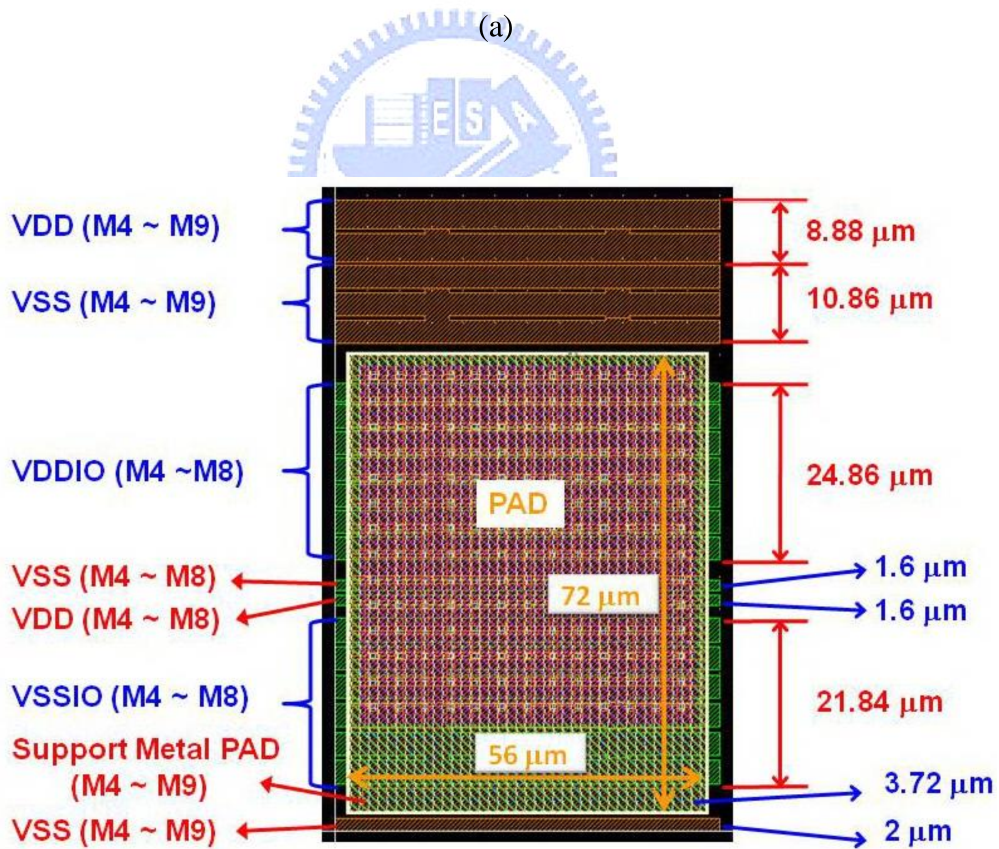
Tabel 4.1

Layer name definition of bond pad.

Layer Name	Description
Metal 9	Define 9th Cu metal
TMV_RDL (L1)	Define top-metal-and-Al-pad-contacts
AL_RDL (L2)	Define Al pad
PASV_RDL (L3)	Define Al pad window region

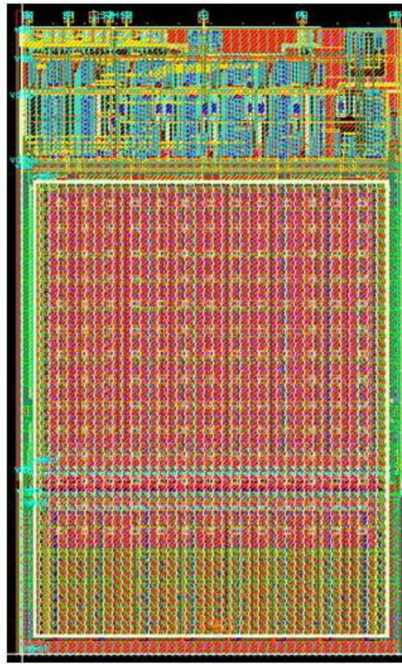


(a)



(b)

(continue to next page, Fig. 4.1)



(c)

Fig. 4.1 (a) Layout implementations of configurable I/O with slew-rate control cell (UCIOS) and power line. (a) Configurable I/O cell, (b) power line and (c) complete layout implementation.

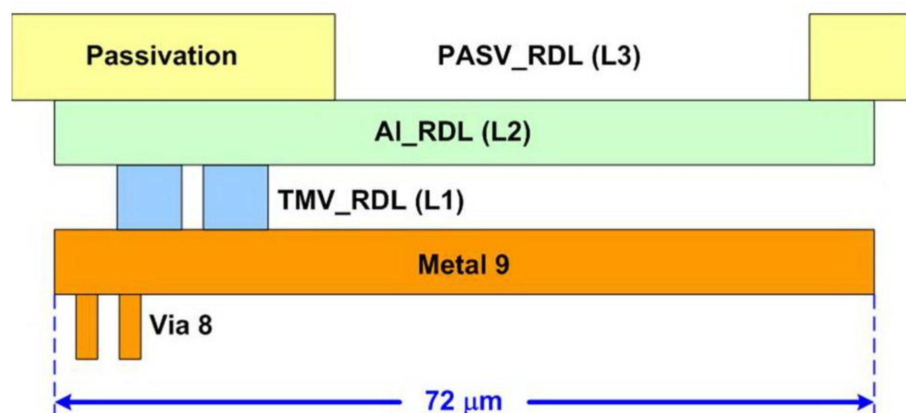
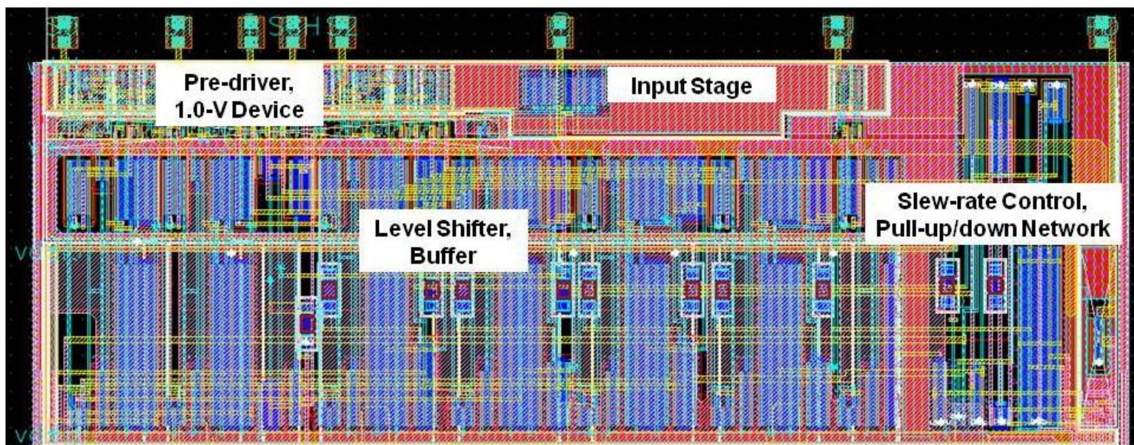
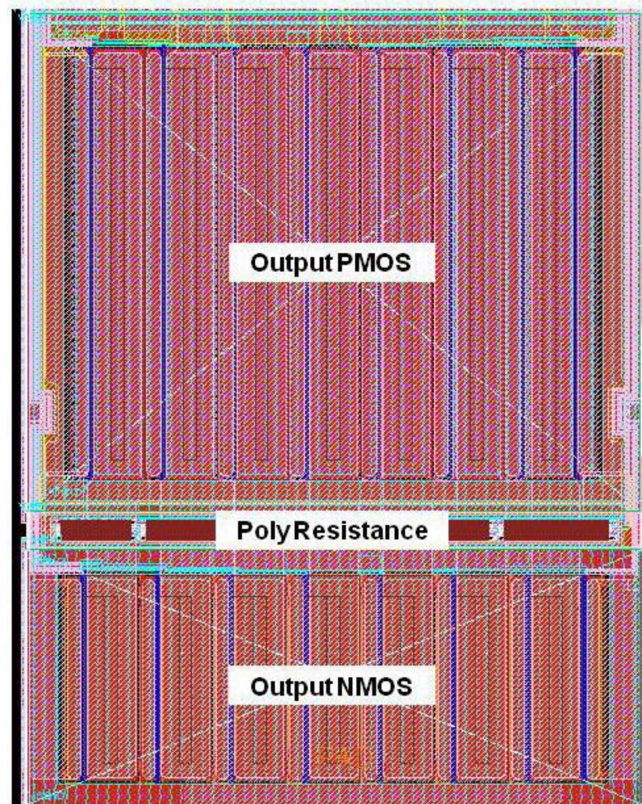


Fig. 4.2 Cross section view of bond pad.



(a)



(b)

Fig. 4.3 Block layout views of configurable I/O with slew-rate control cell (UCIOS).

(a) Pre-driver, level shifter, input stage, pull-up/pull-down network and slew-rate control;

(b) Output driver and poly resistance between pull-up/pull-down MOS and I/O PAD.

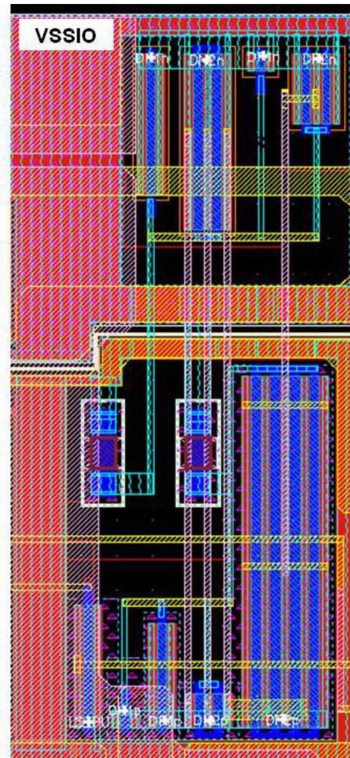


Fig. 4.4 Slew-rate control circuit layout of configurable I/O without slew-rate control cell (UCIONS).

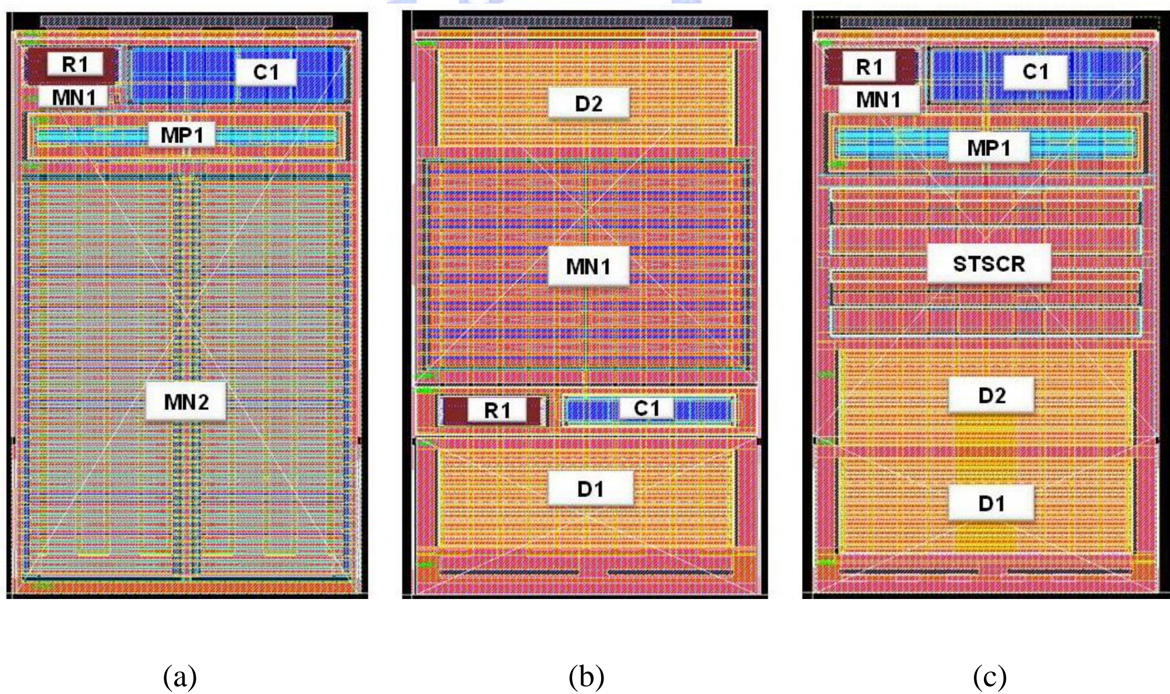


Fig. 4.5 Layout-top-view of (a) UVDD25, (b) UVSS25, and (c) UVSS10 cells.

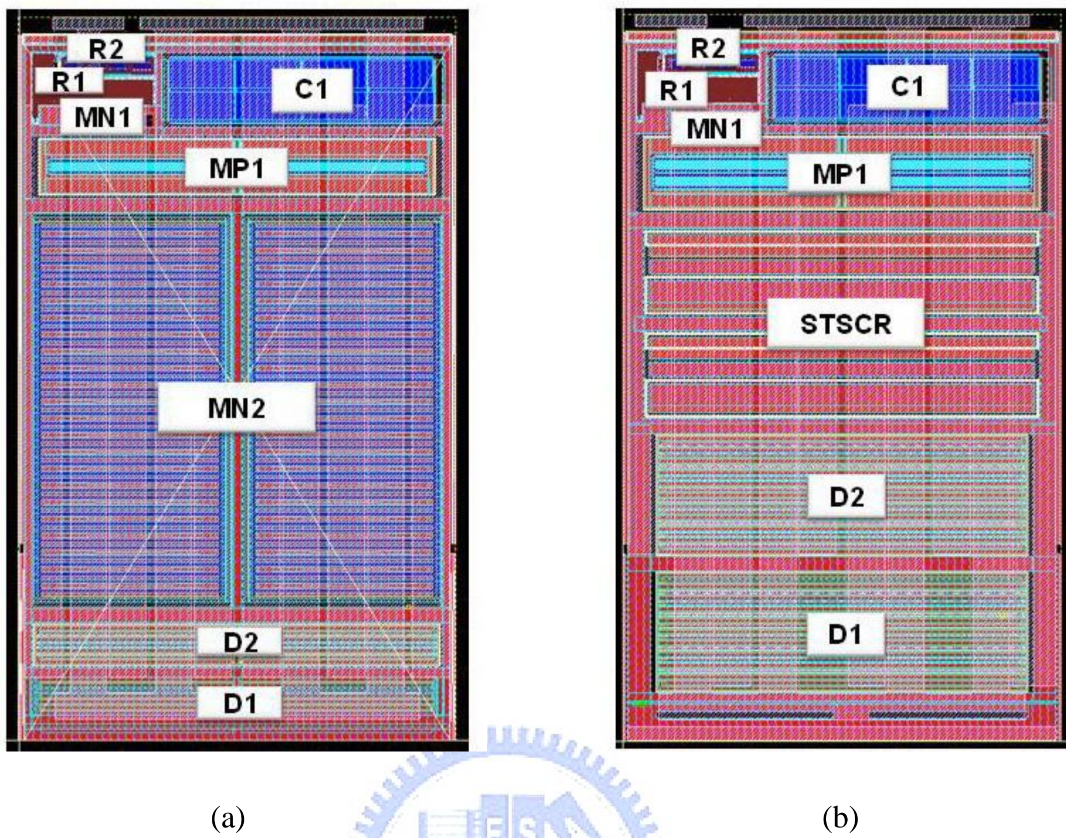


Fig. 4.6 Layout-top-view of (a) UAIO25 and (c) UAIO10 cells.

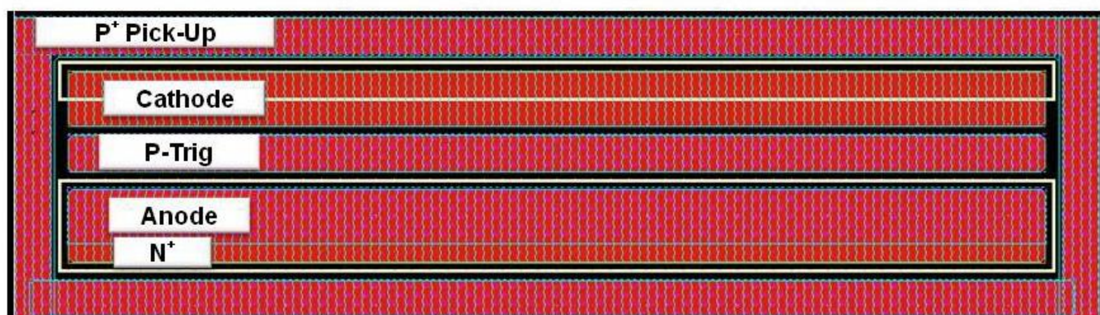


Fig. 4.7 Layout-top-view of STSCR drawn in UVDD10 and UAIO10 cells.

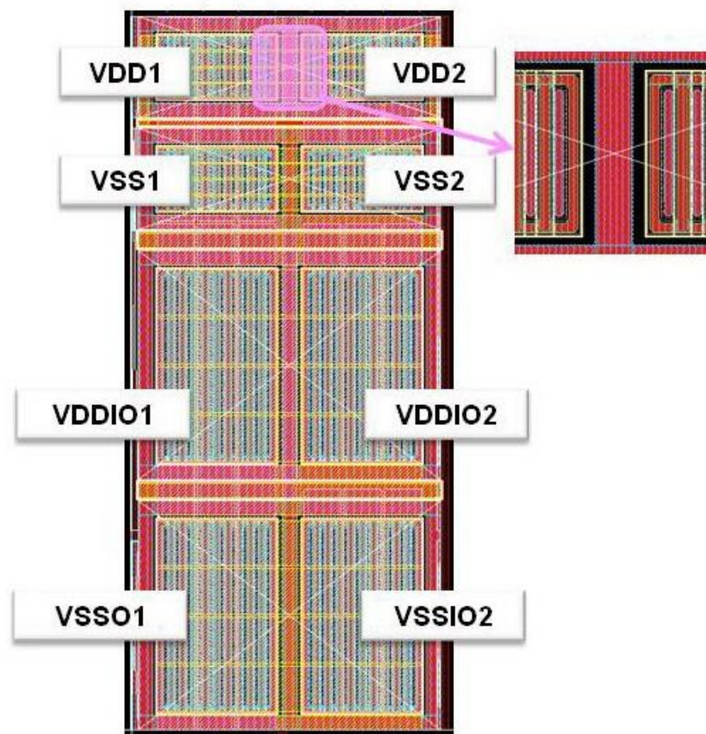


Fig. 4.8 Layout-top-view of UPBREAK cell.

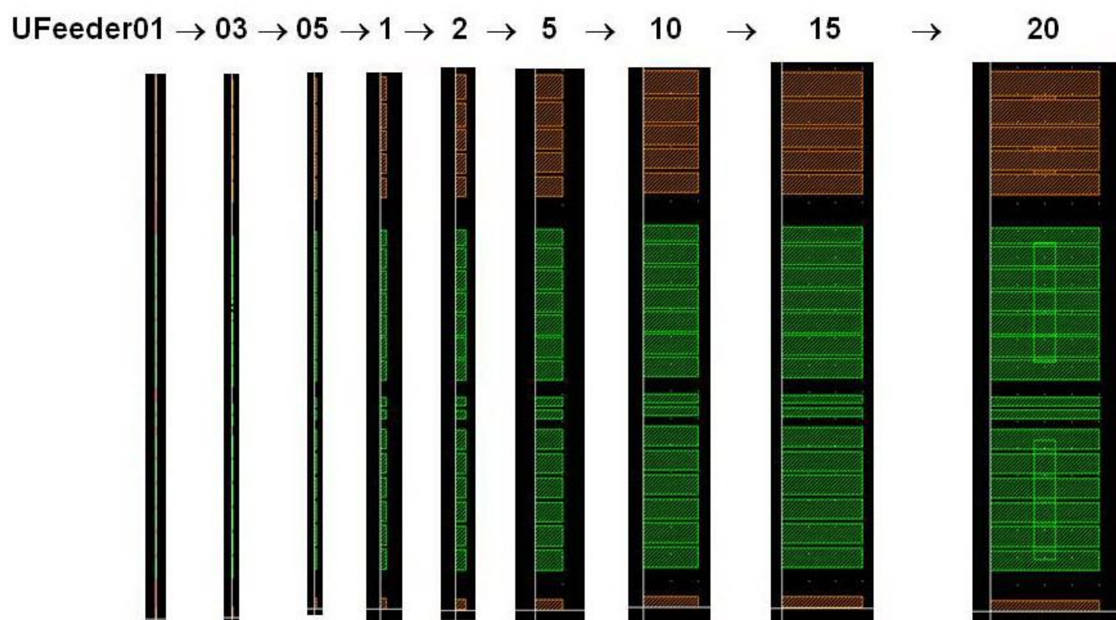


Fig. 4.9 Layout-top-view of UFeeder01, UFeeder03, UFeeder05, UFeeder1, UFeeder2, UFeeder5, UFeeder10, UFeeder15, and UFeeder20 cells.

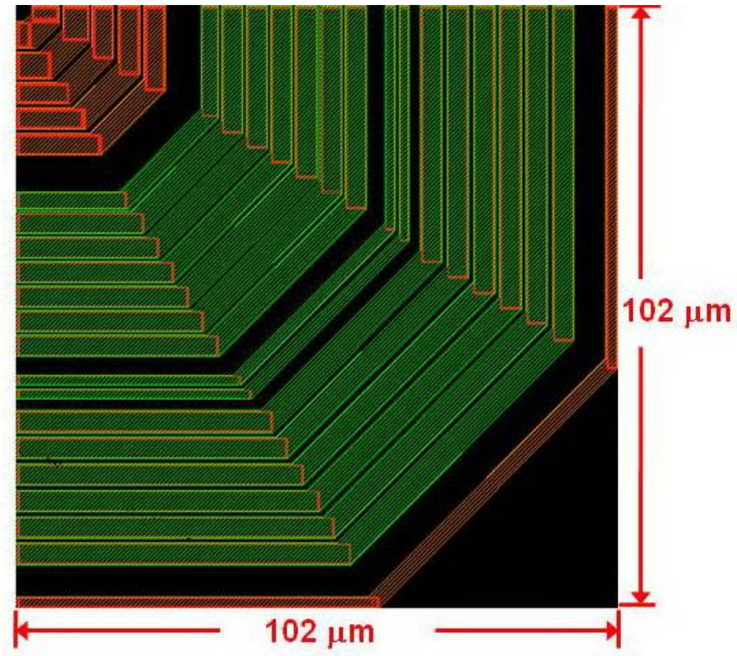


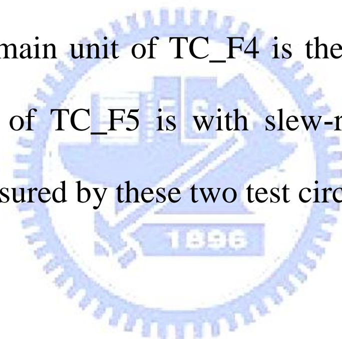
Fig. 4.10 Layout-top-view of corner cell (UCorner).

Chapter 5

Test Chip Arrangement of Configurable I/O Cell Library

5.1 VERIVICATION ON CONFIGURABLE I/O CELL

The definitions of test circuits for function verification are listed in Table 5.1. The function test circuit function 1 (TC_F1) is used to verify the pull-up/pull-down resistance. The TC_F2 and TC_F3 are used to verify the threshold points of schmitt-trigger and driving capability, respectively. The main unit of TC_F4 is the configurable I/O cell with slew-rate control (UCIONS), and that of TC_F5 is with slew-rate control (UCIOS). The SSN and propagation delay can be measured by these two test circuits.



5.1.1 Pull-Up/Pull-Down Resistance (TC_F1)

The test circuit of pull-up/pull-down resistance of configurable I/O cell is shown in Fig. 5.1. Five input cells (UINPUT) are placed between the input signal pins (Ia, Sa, PUa, PDa, and SCHa) and control-signal pins (I, S2, S1, S0, PU, PD, and SCH) to enhance the ESD robustness significantly. Fig. 5.2 depicts the input cell (UINPUT) defined as configurable I/O with slew-rate cell (UCIOS) biased all control-signal pins (I, S2, S1, S0, PU, PD, and SCH) at 0V. In Fig. 5.1, the control-signal pins S2, S1, and S0 are connected commonly to become an enable signal. The UCIOS cell will be in tri-state while the pin Sa receives a logic-0 signal and in transmitting mode while the pin Sa receives a logic-1 signal. When PUa, PDa, and SCHa are set to a high voltage level, the functions of pull-up, pull-down, and schmitt-trigger

will be switched on, respectively. On the contrary, when PUa, PDa, and SCHa are set to a low voltage level, the functions will be switched off. Note that the functions of pull-up and pull-down should not be turned on at the same time, because it will make a short circuit in the test circuit.

Fig. 5.3 shows the simulated waveforms of pull-up and pull-down resistance. In Fig. 5.3(a), the input signal Sa receives the input signal of 0-to-1.8V, 0-to-2.5V, and 0-to-3.3V with the corresponding VDDIO supply voltages, respectively, and the input signal I receives a DC signal of 0V. The I/O PADa is biased at 0V when the input signal Sa receives the logic high level, and the configurable I/O (UCIOS) cell is in transmitting mode simultaneously. When the input signal Sa receives a 0V signal to trigger the pull-up network, the UCIOS cell is in tri-state causing the I/O PADa at logic high with a rise time (T_r) of 1.03μs closely. Besides, in Fig. 5.3(b), the input signal Sa receives the same input signal waveform, but the input signal I is biased at logic high level. When the input signal Sa receives the logic high level, the UCIOS cell operates in transmitting mode so that the I/O PADa is biased at the same voltage level as input signal Sa. While the input signal, Sa, receives a 0V input signal to trigger the pull-down network, the UCIOS cell is in tri-state causing the I/O PADa at 0V with a fall time (T_f) of 1.03μs closely.

5.1.2 Schmitt-trigger Threshold Points (TC_F2)

To save layout area, the test circuit shown in Fig. 5.1 is used to measure not only pull-up/pull-down resistance, but also low-to-high/high-to-low threshold voltages (V_{T+}/V_{T-}) of schmitt-trigger input stage in configurable I/O cell. The input signal pin SCHa is used to control the function of schmitt-trigger switching on (off) with a high (low) level voltage. In order to enhance ESD robustness, the output signal pin, C, of the configurable I/O cell (UCIOS) is connected to the pin PADwoR of the analog for 1.0V I/O cell (UAIO10), which

not only can make a stronger capability of ESD protection, but also has a small parasitic capacitance that will not affect pin C.

Fig. 5.4, Fig. 5.5, and Fig. 5.6 shows simulation results for voltage-transfer curve (VTC) of configurable I/O cell under different VDDIO supply voltages. The waveforms of output signal pin, C, is simulated while the I/O PADa is swept from logic low to high and then return to its initial voltage level. According to the simulation waveforms shown in Fig. 5.4, Fig. 5.5, and Fig. 5.6, the threshold voltages are listed in Table 5.1. The $V_{T+/-}$ is defined as the voltage level of I/O PADa while the voltage level of C is VDD/2 with the function of schmitt-trigger (SCHa = 1). The V_{T+} is I/O PADa transmitted from low to high, and the V_{T-} is that from high to low. The V_{TH} is defined as the voltage level of I/O PADa while the voltage level of C is VDD/2 without the function of schmitt-trigger (SCHa = 0).

5.1.3 Driving Capability (TC_F3)

Test circuit for driving capability of configurable I/O cell is shown in Fig. 5.7. Ib, S0b, S1b, and S2b are input signal pins. The pull-up, pull-down, and schmitt-trigger functions are turned off in this test circuit. To save layout area, the control-signal pins I, S0, S1, and S2 are connected to the points Ia_in, Sa_in, PUa_in, and PDa_in shown in Fig. 5.1. The input cells (UINPUT) are used commonly in test circuits TC_F1 and TC_F3.

Table 5.3, Table 5.4, and Table 5.5 list the simulation results of driving capability in different VDDIO supply voltages. In this simulation, the input signal S2b, S1b, and S0b are changed from 001, 010, 011……to 111 to transform driving current from 2mA, 8mA, 10mA……to 24mA. While the input signal Ib receives logic low level, a sink current is produced at I/O PADb. Furthermore, when the voltage at I/O PADb is biased at V_{OL} = 0.4V, the sink current is defined as I_{OL}. Oppositely, while Ib receives logic high level, the source

current is produced at I/O PADb. When the voltage at I/O PADb is biased at V_{OH} = $VDDIO_{(min)}$ – 0.4V, the source current is defined as I_{OH}.

5.1.4 Simultaneous Switching Noise (SSN) and Propagation Delay (TC_F4 & TC_F5)

In actual application, when a lot of I/O cells are switched simultaneously with a joint set of power cells, it will cause serious simultaneous switching noise (SSN). As a result, the comparisons of SSN and delay time between configurable I/O cells with and without slew-rate control (UCIOS and UCIOINS) have to be measured. From the measured results, the ability of slew-rate control in SSN issue reduction can be verified. Fig. 5.8 shows the method of SSN measurement, the noise on the power lines can be measured from pure VDDIO and VSSIO cells while 17 cells switched simultaneously. The I/O pad name of pure VDDIO and VSSIO cells are denoted $VDDIO_{chip}$ and $VSSIO_{chip}$, respectively.

Since the delay time of single I/O cell is too short, it cannot be measured accurately. Hence, the multiple-stage I/O cells consisted of I/O cell chain are also used to analyze the delay of single-stage I/O cell as shown in Fig. 5.9. There is no mechanism to turn on or off the input stage of configurable I/O cell. Thus, when these I/O cells is operating in transmitting mode, the signal at the pin I (VSS-to-VDD) will be transmitted to I/O PAD (VSSIO-to-VDDIO) through the output stage. Then the signal will be transmitted to output signal C (VSS-to-VDD) through the input stage. Besides, the output signal C of a configurable I/O cell is associated with the input signal I of the next configurable I/O cell as an input signal pin. Then, an I/O chain (17 I/O cells) can be constructed. Therefore, the data of the PADn1/PADs1 will be transmitted to the PADn17/PADs17 through the I/O cell chain progressively when these I/O cells are operating in transmitting mode. Moreover, an inverter is inserted between the last configurable I/O cell and the first one to form a ring-oscillator. Besides, all the control-signal pins, SCH, PD, and PU, of the configurable I/O cells in the

ring-oscillator are connected to 0-V voltage to switch off the functions of schmitt-trigger, pull-up, and pull-down. And all the signal, S2, S1, and S0, are connected to input cells individually and denoted the input signal pins as Sn2/Ss2, Sn1/Ss1, and Sn0/Ss0, which control the driving capability to change the oscillatory frequency. When the input signal Sn2/Ss2, Sn1/Ss1, and Sn0/Ss0 are received 0V input signal simultaneously, the ring-oscillator will be turned off and make no output signal at all the I/O PAD of configurable I/O cells. Thus, to measure the delay time from PADn1/PADs1 to PADn17/PADs17 can infer the propagation delay of single I/O cell. Consequently, such test circuit show in Fig. 5.9 can measure the SSN and the propagation delay.

In order to verify the reduction of ground bounce by slew-rate control, a model for ground bounce effects is shown in Fig.5.10. The inductances of wire bonds vary from 3nH to 9nH in the simulation for pseudo worst case with 24mA driving capability and a load capacitance of 12pF which can result in close results to actual conditions in this part. Since the switching currents of configurable I/O cells in transmitting mode are much larger than that in receiving mode, the ground bounce effects are simulated in transmitting mode for clear illustration. The simulation waveforms of ground bounce effects on power lines are shown in Fig. 5.11 and several parameters are defined as follows:

- $VDDIO_{ext}/VSSIO_{ext}$: External power supply;
- $VDDIO_{chip_max}/VDDIO_{chip_min}$: maximon/minimum value of $VDDIO_{chip}$ power line;
- $VSSIO_{chip_max}/VSSIO_{chip_min}$: maximon/minimum value of $VSSIO_{chip}$ power line;
- $\Delta V_{VDDIOchip_over}$: overshoot on $VDDIO_{chip}$ power line ($VDDIO_{chip_max}$ - $VDDIO_{ext}$);
- $\Delta V_{VDDIOchip_under}$: undershoot on $VDDIO_{chip}$ power line ($VDDIO_{ext}$ - $VDDIO_{chip_min}$);
- $\Delta V_{VSSIOchip_over}$: overshoot on $VSSIO_{chip}$ power line ($VSSIO_{chip_max}$ - $VSSIO_{ext}$);

- $\Delta V_{VSSIOchip_under}$: undershoot on $VSSIO_{chip}$ power line ($VSSIO_{ext}$ - $VSSIO_{chip_min}$);

The $\Delta V_{VDDIOchip_under}$ and $\Delta V_{VSSIOchip_over}$ among these parameters are the major concerns since these two terms may result in increasing timing delay and even logic errors on transmitted signals.

The simulation waveforms of UCIOS cells (configurable I/O with slew-rate control cells) which are operated in transmitting mode with the additional parasitic inductances of 5nH and a 2.5-V VDDIO voltage supply are shown in Fig. 5.12. The signal on I/O PADs1 has some glitch due to the ground bounce effect. The simulation results with variation of wire bond inductance on $VDDIO_{chip}$ and $VSSIO_{chip}$ power lines are shown in Fig. 5.13, Fig. 5.14, and Fig. 5.15. Since the current supplied from VDD_{chip} is much smaller than that from $VDDIO_{chip}$, only ground bounce effect on $VDDIO_{chip}$ is shown. As shown in Fig. 5.13, Fig. 5.14, and Fig.5.15, the configurable I/O cell with slew-rate control (UCIOS) improves the ground bounce effects greatly.

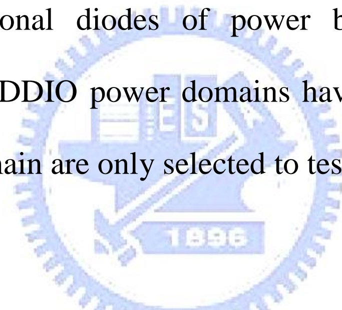
Moreover, the simulation waveforms of configurable I/O cells without slew-rate control (UCIONS) which are operated in transmitting mode with the additional parasitic inductances of 5nH, 2.5-V VDDIO voltage supply, and 24-mA driving current are shown in Fig. 5.16. The desired propagation delay of single I/O cell can be estimated as following equation:

$$\text{Propagation delay of single I/O cell} = \frac{\Delta T\text{-Delay}_{(INV)}}{17} \quad (4)$$

Where the ΔT is the time delay from the first I/O cell to the chosen I/O cell, $Delay_{(INV)}$ is the delay time of the inverter (INV). The simulated comparison between the propagation delays of UCIONS and UCIOS are listed in Table 5.6. As a result, the timing specifications of the UCIOS are somewhat larger than those of the UCIONS.

5.2 VERIFICATION ON THE ESD ROBUSTNESS OF EACH CELL

Fig. 5.17 depicts the testkeys for verifying the ESD robustness of power/ground cells. Each power/ground cell is associated with a pure ground/power pad. Fig. 5.18 depicts the testkeys of analog I/O cells. In order to test the ESD robustness on the diode and the power clamp circuit of the analog I/O cell, the power and ground line are connected to pure power and ground pad individually. Actually, the I/O pad of analog I/O cell may directly join the gate terminal of MOS transistor, so the pin I/O pad with poly resistance, PADwiR, of the analog I/O cells UAIO25 and UAIO10 are connected to the input end of 2.5-V and 1.0-V inverters respectively as shown in Fig. 5.19. Fig. 5.20 depicts the testkeys for verifying the ESD level of the bidirectional diodes of power break cell (UPBREAK). Since the VSS/VSSIO and the VDD/VDDIO power domains have the same diode size, the diodes of VDD and VDDIO power domain are only selected to test the ESD robustness.



5.3 VERIFICATION ON WHOLE-CHIP ESD PROTECTION

Fig. 5.21 shows the simplified scheme of whole-chip protection circuit. In this structure, the ground supply for core circuits and pre-driver are provided by UVSS10 cell, and the ground supply for I/O ring is provided by UVSS25 cell. Furthermore, Fig. 5.22 shows the test circuit of whole-chip protection with power break cell. The purpose is the ESD robustness test on two set of power through a power break cell. The layout-top-view of the test chip in UMC 90-nm process is shown in Fig. 5.23.

Tabel 5.1

Definition of function test circuit.

Test Circuit	Measured Function	Pins
TC_F1	Pull-Up/Pull-Down Resistance (R_{PU} and R_{PD})	PAD, I, S, PD, PU
TC_F2	Schmitt-Trigger Threshold Voltage (V_{T+} and V_{T-})	PAD, C, SCH
TC_F3	Driving Current (I_{OH} and I_{OL})	PAD, I, S0, S1, S2
TC_F4	Simultaneous Switching Output Noise (SSO or SSN) and Delay Time of Configurable I/O Cell without Slew-Rate Control	S0, S1, S2, PAD1, PAD3, PAD5, ….., PAD15, PAD17, pure VDDIO, pure VSSIO
TC_F5	Simultaneous Switching Output Noise (SSO or SSN) and Delay Time of Configurable I/O Cell with Slew-Rate Control	S0, S1, S2, PAD1, PAD3, PAD5, ….., PAD15, PAD17, pure VDDIO, pure VSSIO

Tabel 5.2

Threshold voltages of input stage under different simulation conditions.

Input Signal of SCHa	SCHa = 1						SCHa = 0		
VDDIO Supply Voltage	3.3V	2.5V	1.8V	3.3V	2.5V	1.8V	3.3V	2.5V	1.8V
Threshold Voltages / Simulation condition	V_{T+} (V)			V_{T-} (V)			V_{TH} (V)		
Best Case	2.065	1.755	1.455	1.225	0.915	0.645	1.91	1.366	0.955
Typical Case	1.925	1.625	1.335	1.125	0.825	0.585	1.723	1.235	0.876
Pseudo Worst Case	1.905	1.625	1.335	1.135	0.835	0.605	1.735	1.245	0.885
Worst Cast	1.775	1.505	1.205	1.045	0.755	0.555	1.568	1.128	0.815

Tabel 5.3

Driving capability of configurable I/O cell in 1.8-V VDDIO supply voltage.

Parameter / Simulation Case			Worst	Pseudo Worst	Typical	Best
VDD	Core Power Supply		0.9V	1.0V		1.1V
VDDIO	I/O Power Supply		1.62V	1.8V		1.98V
T	Temperature		125 °C	85 °C	25 °C	0 °C
I_{OL}	Low Level Output Current @ V_{OL} = 0.4V	2mA	1.58mA	2.40mA	2.93mA	4.12mA
		8mA	6.34mA	9.62mA	11.7mA	16.4mA
		10mA	7.92mA	12.0mA	14.7mA	20.6mA
		14mA	11.1mA	16.8mA	20.6mA	28.9mA
		16mA	12.7mA	19.2mA	23.5mA	33.0mA
		22mA	17.5mA	26.5mA	32.3mA	45.4mA
		24mA	19.0mA	28.9mA	35.2mA	49.5mA
I_{OH}	High Level Output Current @ V_{OH} = 1.22V	2mA	1.46mA	2.71mA	3.06mA	5.08mA
		8mA	5.89mA	10.9mA	12.3mA	20.4mA
		10mA	7.35mA	13.6mA	15.4mA	25.4mA
		14mA	10.3mA	19.1mA	21.6mA	35.6mA
		16mA	11.8mA	21.8mA	24.6mA	40.7mA
		22mA	16.2mA	30.0mA	33.9mA	56.0mA
		24mA	17.7mA	32.7mA	37.0mA	61.1mA

Tabel 5.4

Driving capability of configurable I/O cell in 2.5-V VDDIO supply voltage.

Parameter \ Simulation Case			Worst	Pseudo Worst	Typical	Best
VDD	Core Power Supply		0.9V	1.0V		1.1V
VDDIO	I/O Power Supply		2.25V	2.5V		2.75V
T	Temperature		125 °C	85 °C	25 °C	0 °C
I_{OL}	Low Level Output Current @ V_{OL} = 0.4V	2mA	2.34mA	3.33mA	4.06mA	5.31mA
		8mA	9.41mA	13.3mA	16.3mA	21.2mA
		10mA	11.7mA	16.7mA	20.3mA	26.5mA
		14mA	16.5mA	23.3mA	28.5mA	37.2mA
		16mA	18.8mA	26.7mA	32.5mA	42.5mA
		22mA	25.9mA	36.6mA	44.7mA	58.4mA
		24mA	28.2mA	40.0mA	48.8mA	63.7mA
I_{OH}	High Level Output Current @ V_{OH} = 1.85V	2mA	2.20mA	4.36mA	4.93mA	8.23mA
		8mA	8.94mA	17.5mA	19.8mA	33.0mA
		10mA	11.0mA	21.9mA	24.7mA	41.2mA
		14mA	15.5mA	30.6mA	34.7mA	57.8mA
		16mA	17.7mA	35.0mA	39.6mA	66.0mA
		22mA	24.3mA	48.1mA	54.4mA	90.8mA
		24mA	26.5mA	52.5mA	59.4mA	99.0mA

Tabel 5.5

Driving capability of configurable I/O cell in 3.3-V VDDIO supply voltage.

Parameter \ Case			Worst	Pseudo Worst	Typical	Best
VDD	Core Power Supply		0.9V	1.0V		1.1V
VDDIO	I/O Power Supply		3.0V	3.3V		3.6V
T	Temperature		125 °C	85 °C	25 °C	0 °C
I_{OL}	Low Level Output Current @ V_{OL} = 0.4V	2mA	2.91mA	3.88mA	4.65mA	5.74mA
		8mA	11.7mA	15.5mA	18.6mA	23.0mA
		10mA	14.6mA	19.4mA	23.2mA	28.7mA
		14mA	20.4mA	27.2mA	32.6mA	40.2mA
		16mA	23.3mA	31.1mA	37.2mA	45.9mA
		22mA	21.0mA	42.7mA	51.2mA	63.2mA
		24mA	35.0mA	46.6mA	55.8mA	68.9mA
I_{OH}	High Level Output Current @ V_{OH} = 2.6V	2mA	2.81mA	5.86mA	6.55mA	11.0mA
		8mA	11.2mA	23.5mA	26.3mA	44.0mA
		10mA	14.1mA	29.4mA	32.8mA	55.0mA
		14mA	19.8mA	41.2mA	46.0mA	77.0mA
		16mA	22.6mA	47.0mA	52.6mA	88.0mA
		22mA	31.0mA	64.7mA	72.3mA	121mA
		24mA	33.8mA	70.5mA	78.9mA	132mA

Tabel 5.6

Comparisons of propagation delays.

$VDDIO_{ext}$	Cell Name	ΔT	$Delay_{(INV)}$	Propagation Delay
1.8V	UCIONS	19.29ns	0.1566ns	1.13ns
	UCIOS	21.56ns		1.26ns
2.5V	UCIONS	16.07ns		0.94ns
	UCIOS	17.90ns		1.04ns
3.3V	UCIONS	15.60ns		0.91ns
	UCIOS	17.32ns		1.01ns

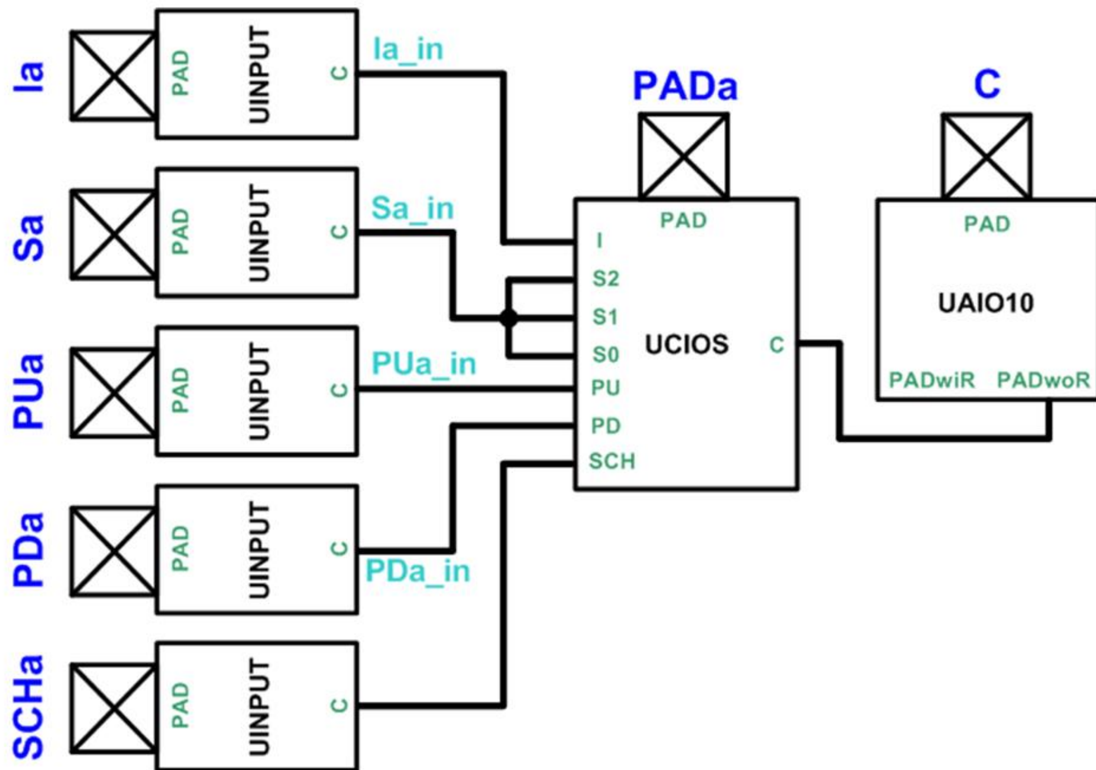


Fig. 5.1 Test circuit for measuring pull-up/pull-down resistance and Schmitt-trigger threshold points.

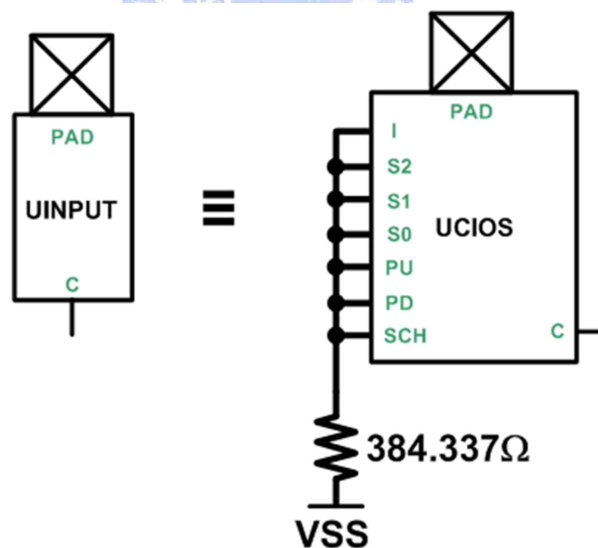
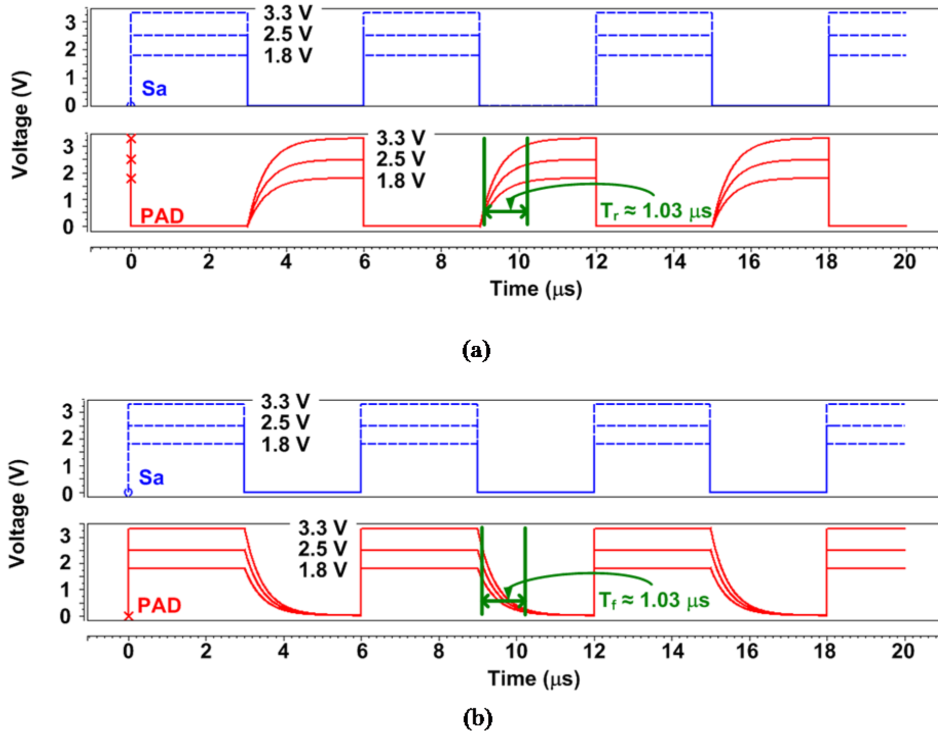


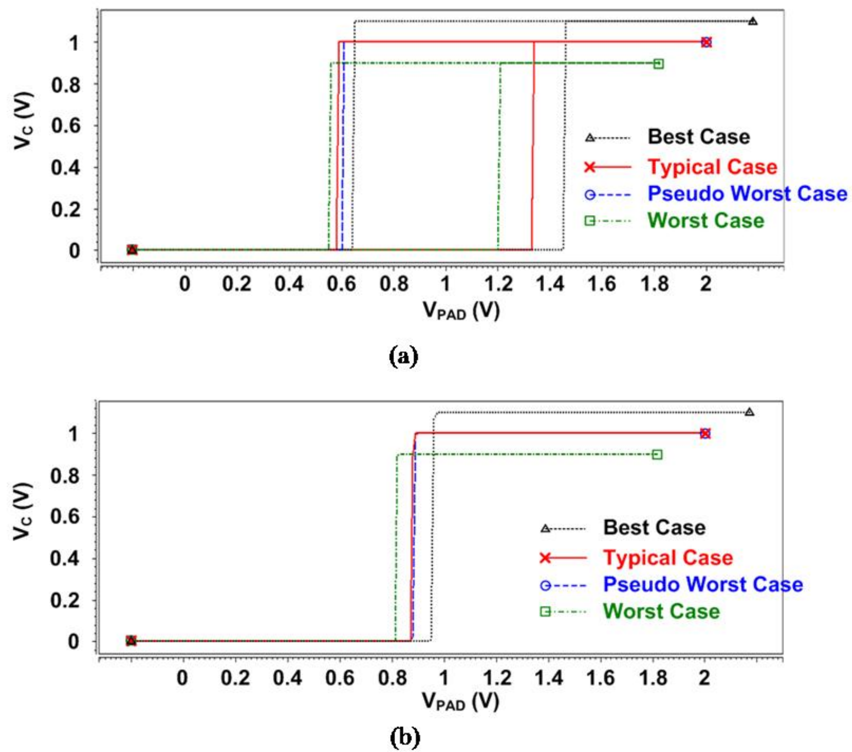
Fig. 5.2 The implementation of the input cell by making from configurable I/O with slew-rate control cell.



(a)

(b)

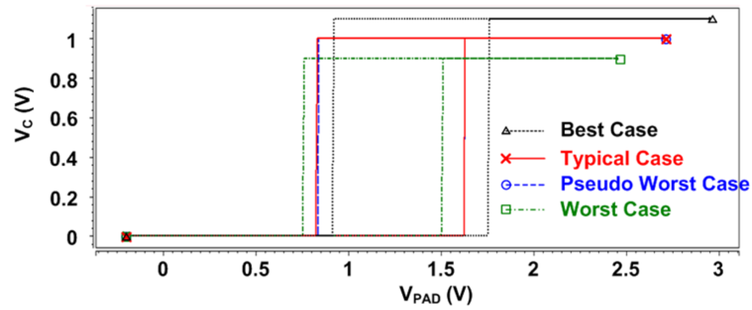
Fig. 5.3 Simulated results of (a) pull-up and (b) pull-down resistance.



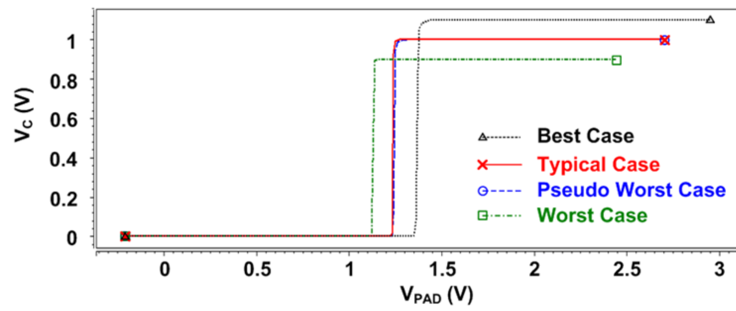
(a)

(b)

Fig. 5.4 Voltage-transfer curve of configurable I/O with (a) SCHa receiving a 1.8-V voltage and (b) SCHa receiving a 0-V voltage in 1.8-V VDDIO supply voltage.

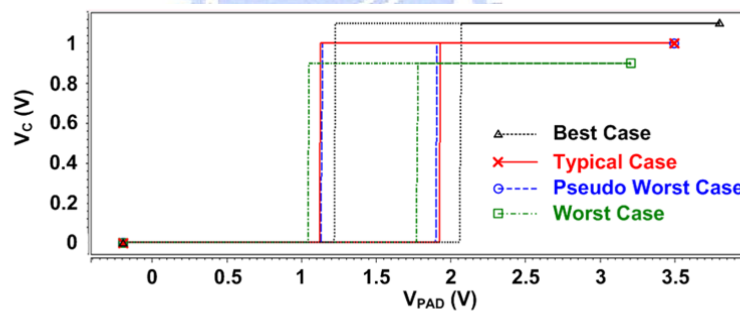


(a)

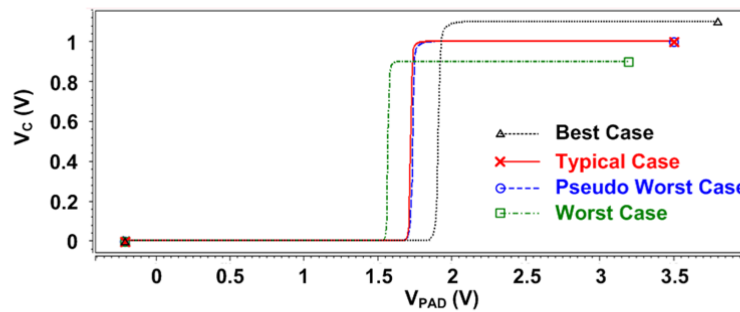


(b)

Fig. 5.5 Voltage-transfer curve of configurable I/O with (a) SCHa receiving a 2.5-V voltage and (b) SCHa receiving a 0-V voltage in 2.5-V VDDIO supply voltage.



(a)



(b)

Fig. 5.6 Voltage-transfer curve of configurable I/O with (a) SCHa receiving a 3.3-V voltage and (b) SCHa receiving a 0-V voltage in 3.3-V VDDIO supply voltage.

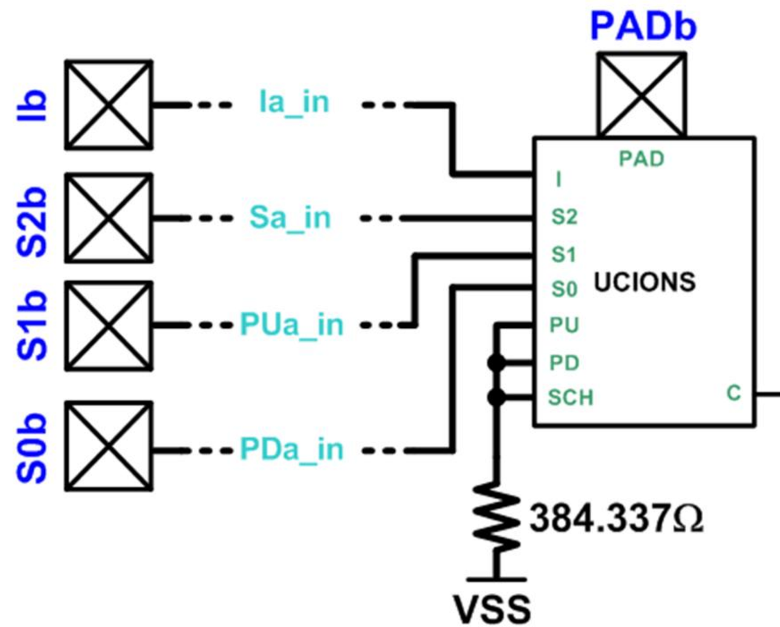


Fig. 5.7 Test circuit of configurable I/O driving capability.

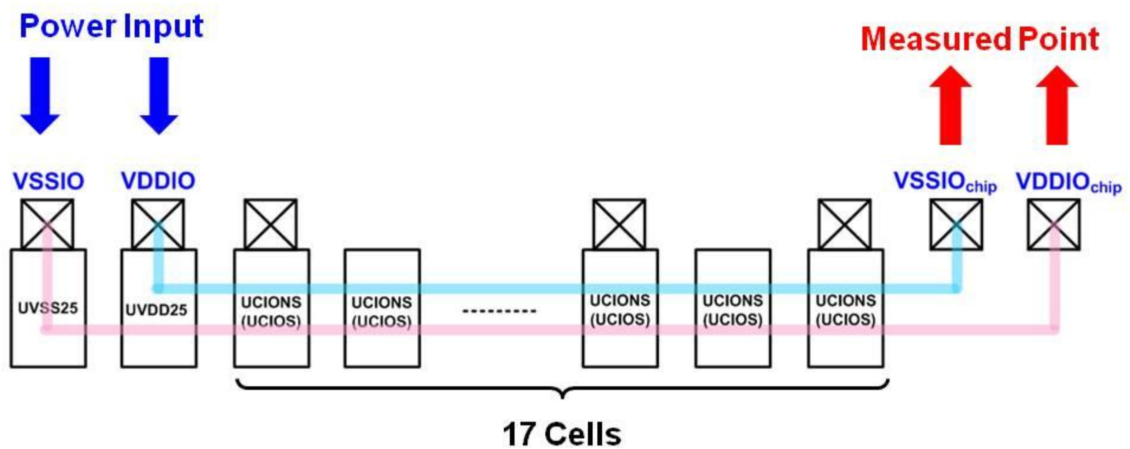


Fig. 5.8 Method for measuring SSN (simultaneous switching noise) of UCIOS and UCIONS.

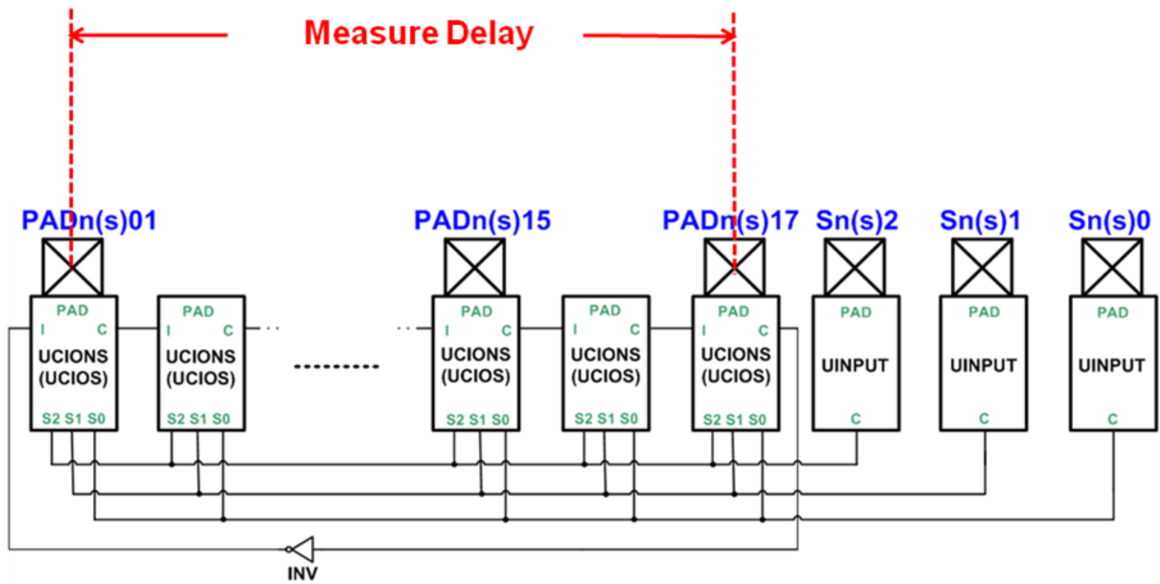


Fig. 5.9 Test circuit for measuring SSN and propagation delay of configurable I/O cells.

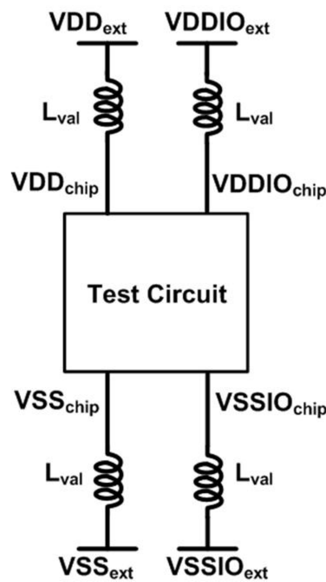


Fig. 5.10 Simulated model of ground bounce.

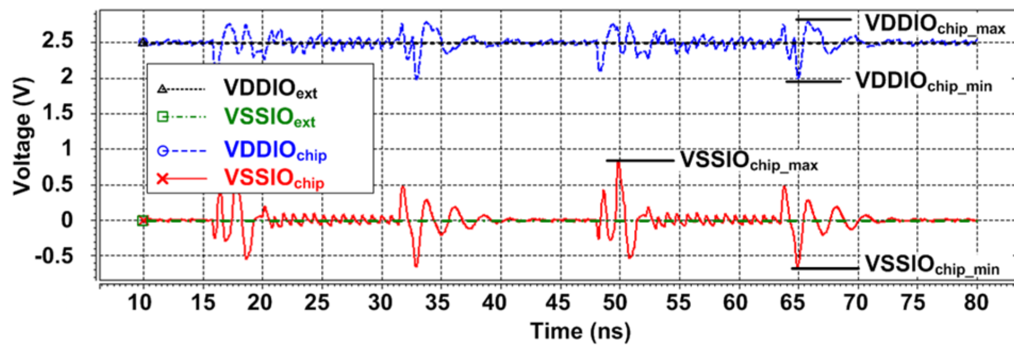


Fig. 5.11 Simulation waveforms of ground bounce effects on power lines.

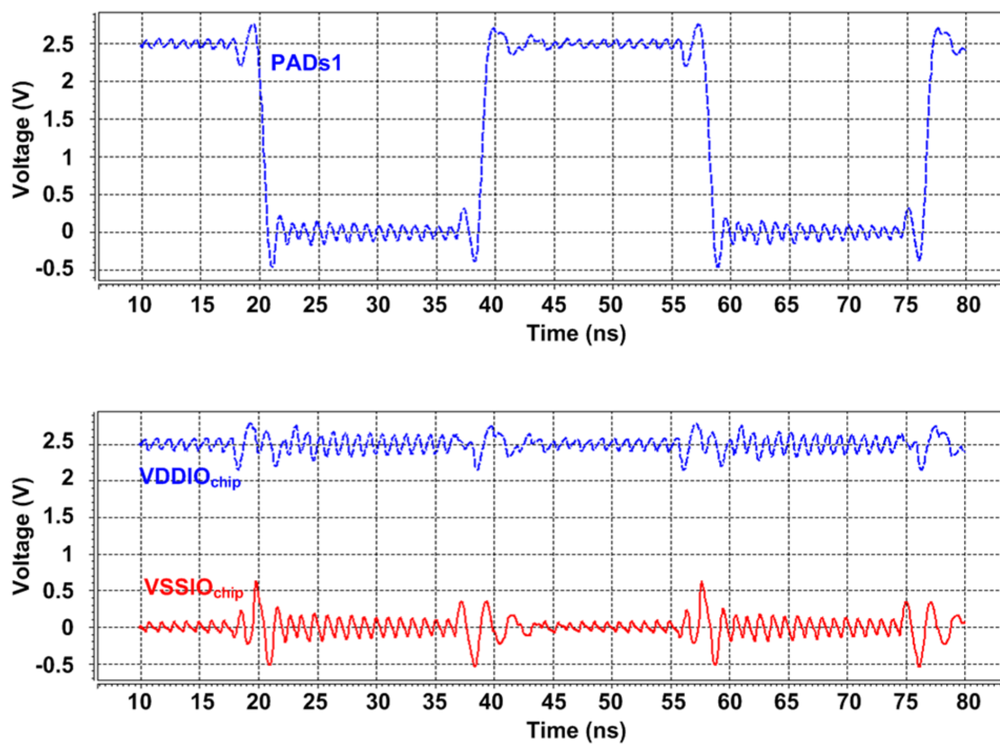
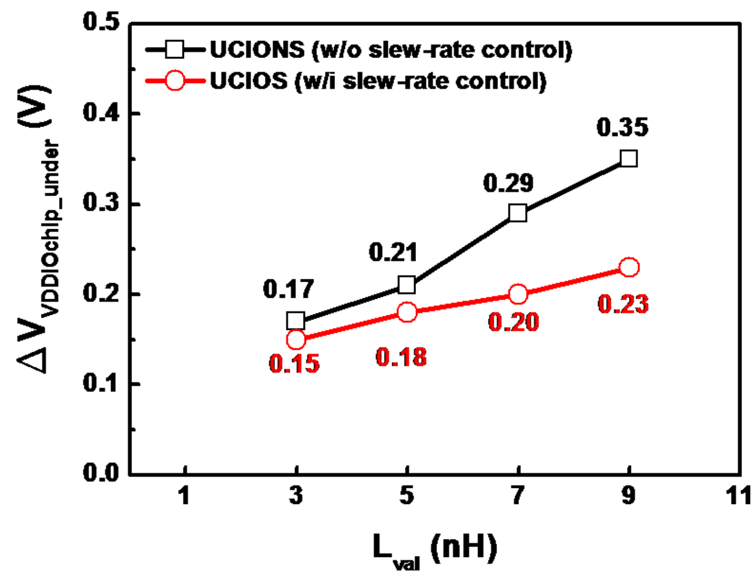
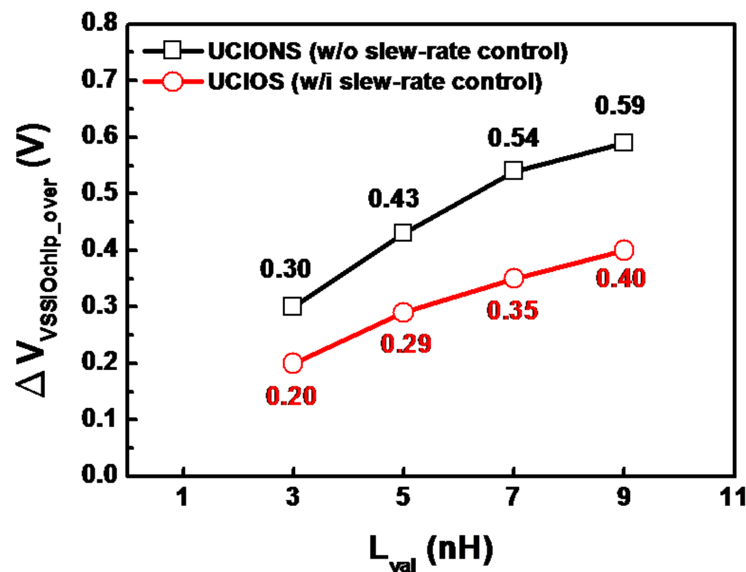


Fig. 5.12 Simulation waveforms of the UCIOS (configurable I/O cell with slew-rate control) with ground bounce effect in transmitting mode.

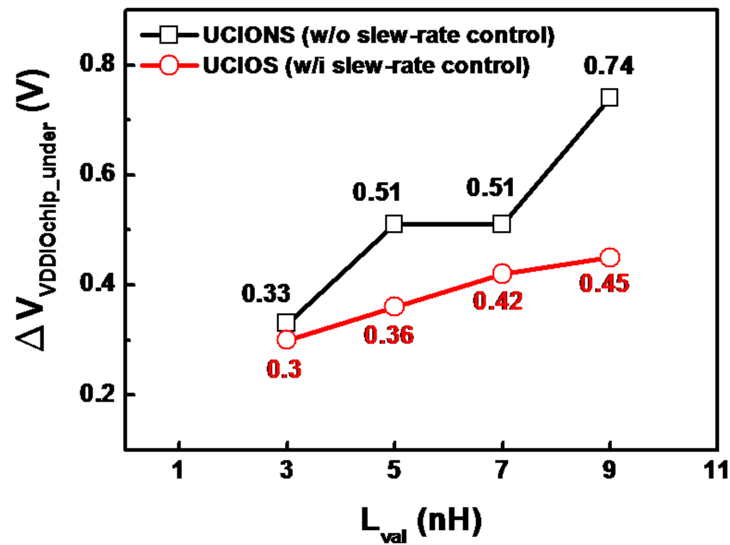


(a)

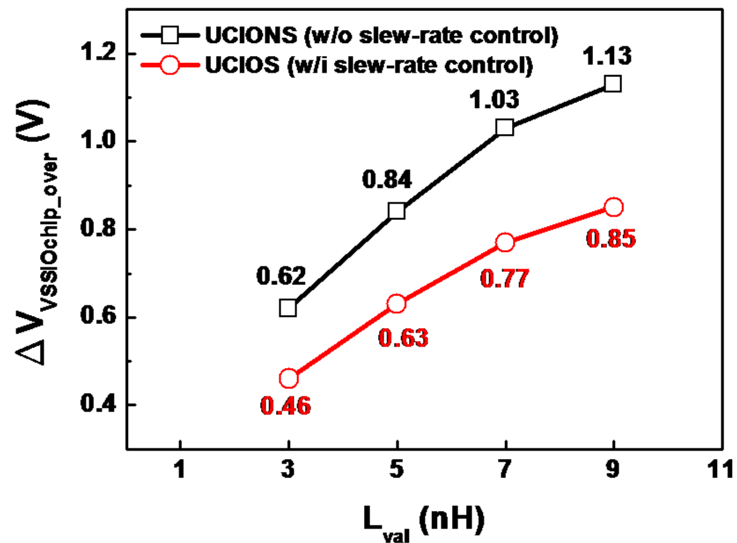


(b)

Fig. 5.13 The relation between ground bounce on $VDDIO_{chip}/VSSIO_{chip}$ power line and wire bond inductance on the UCIONS and UCIOS with 1.8-V $VDDIO_{ext}$ voltage supply. (a) The undershoot on $VDDIO_{chip}$ power line and (b) the overshoot on $VSSIO_{chip}$ power line.

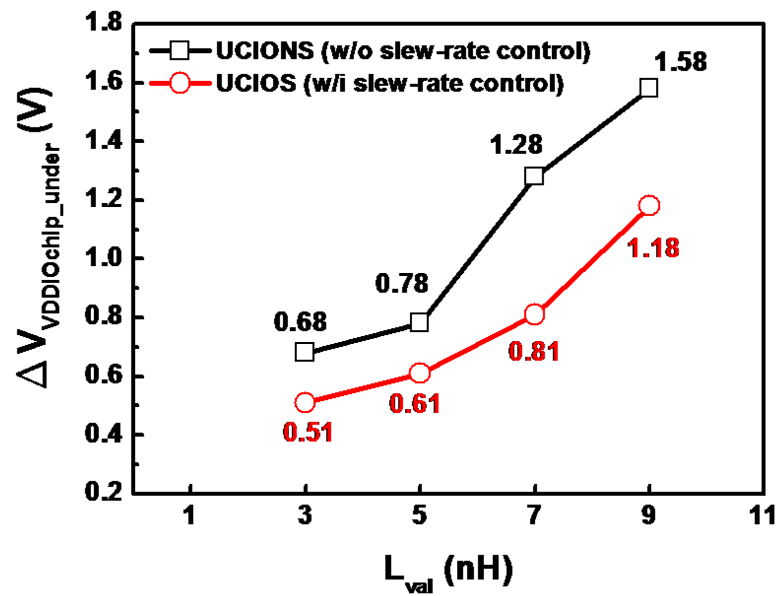


(a)

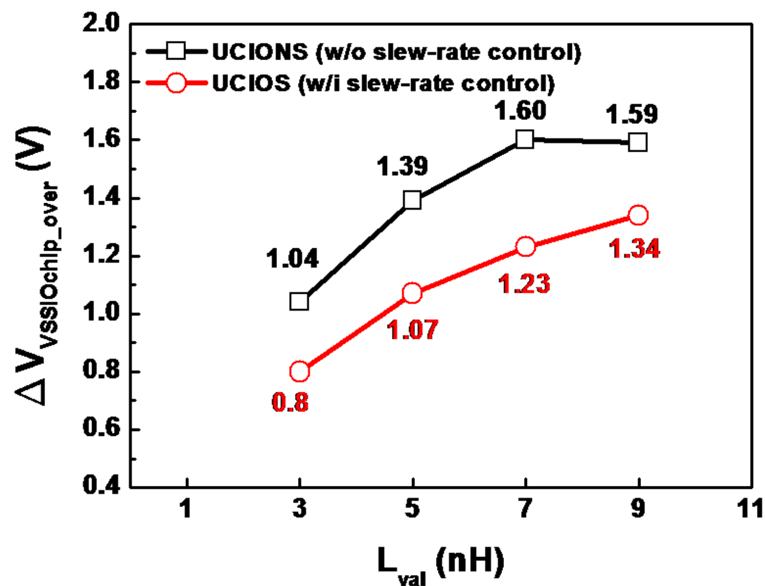


(b)

Fig. 5.14 The relation between ground bounce on $VDDIO_{chip}$/$VSSIO_{chip}$ power line and wire bond inductance on the UCIONS and UCIOS with 2.5-V $VDDIO_{ext}$ voltage supply. (a) The undershoot on $VDDIO_{chip}$ power line and (b) the overshoot on $VSSIO_{chip}$ power line.



(a)



(b)

Fig. 5.15 The relation between ground bounce on $VDDIO_{chip}$/$VSSIO_{chip}$ power line and wire bond inductance on the UCIONS and UCIOS with 3.3-V $VDDIO_{ext}$ voltage supply. (a) The undershoot on $VDDIO_{chip}$ power line and (b) the overshoot on $VSSIO_{chip}$ power line.

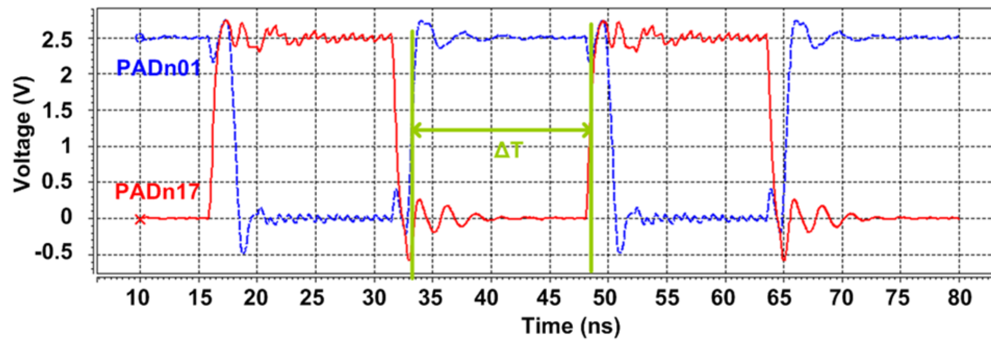


Fig. 5.16 Simulation waveforms for propagation delay of I/O cell with operating in transmitting mode.

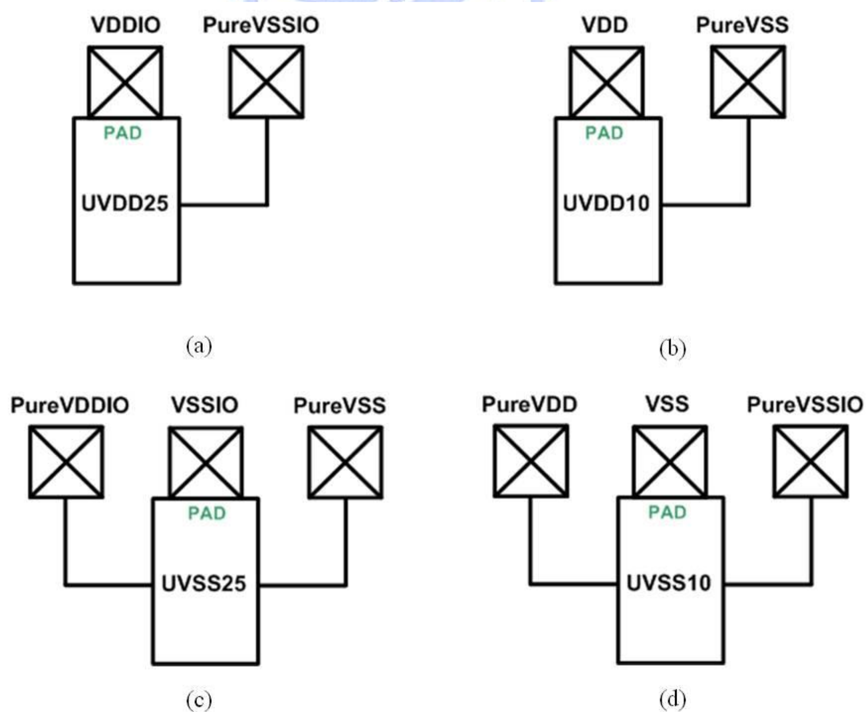


Fig. 5.17 Testkeys of power/ground cells, (a) UVDD25, (b) UVDD10, (c) UVSS25, and (d) UVSS10.

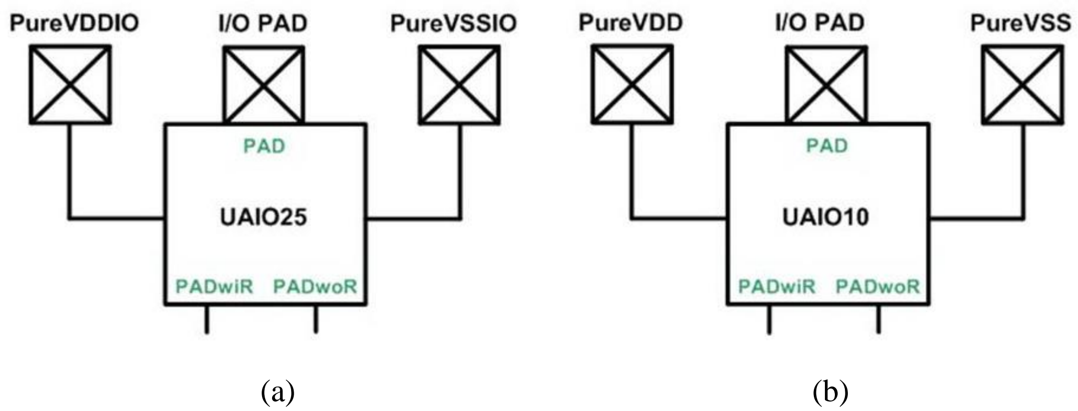


Fig. 5.18 Testkeys of analog I/O cells, (a) UAIO25 and (b) UAIO10.

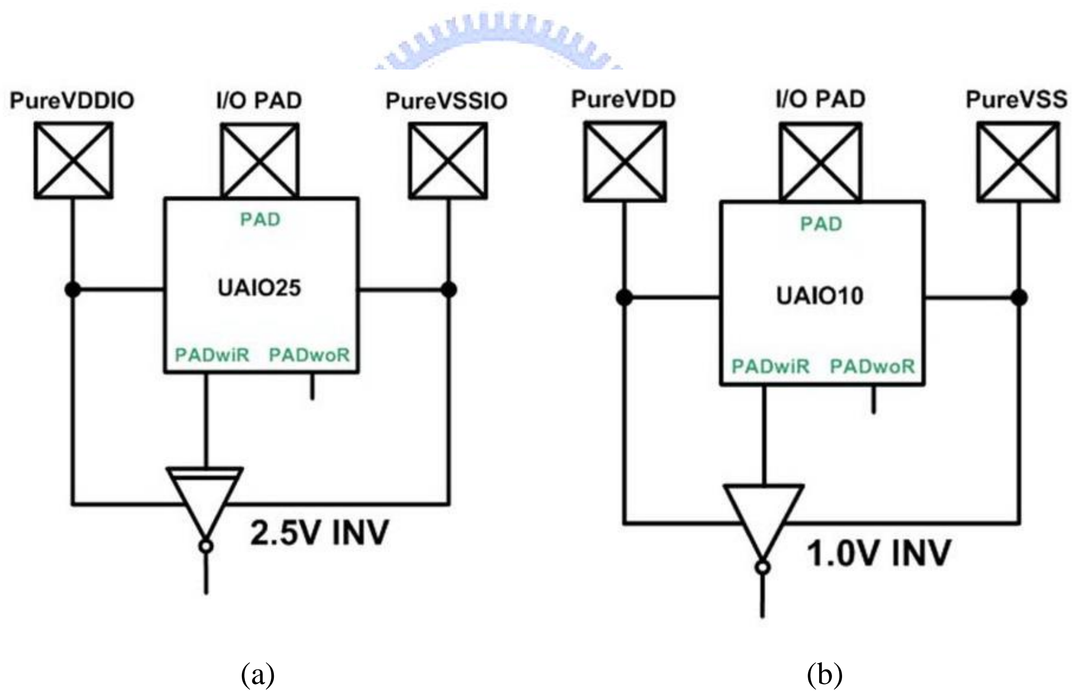


Fig. 5.19 Testkeys of analog I/O cells, (a) UAIO25 and (b) UAIO10 with inverter stage.

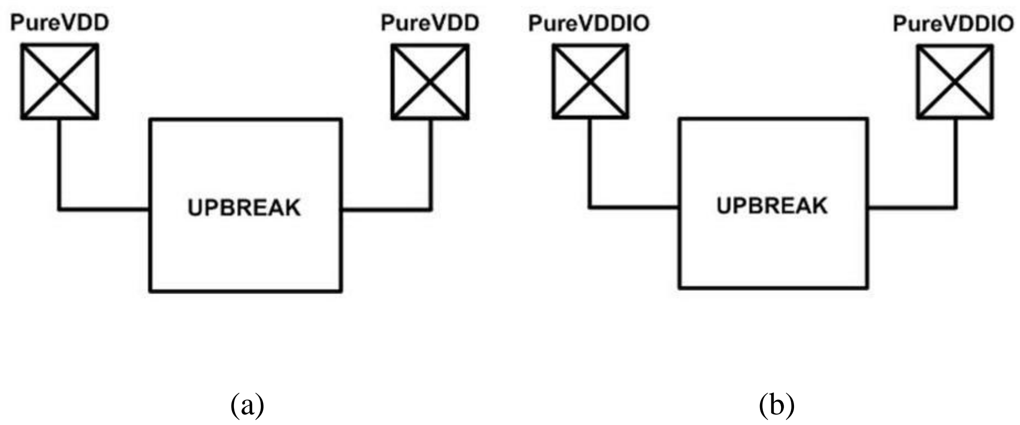


Fig. 5.20 Testkeys of power break cell for (a) 1.0-V power domain and (b) 2.5-V power domain.

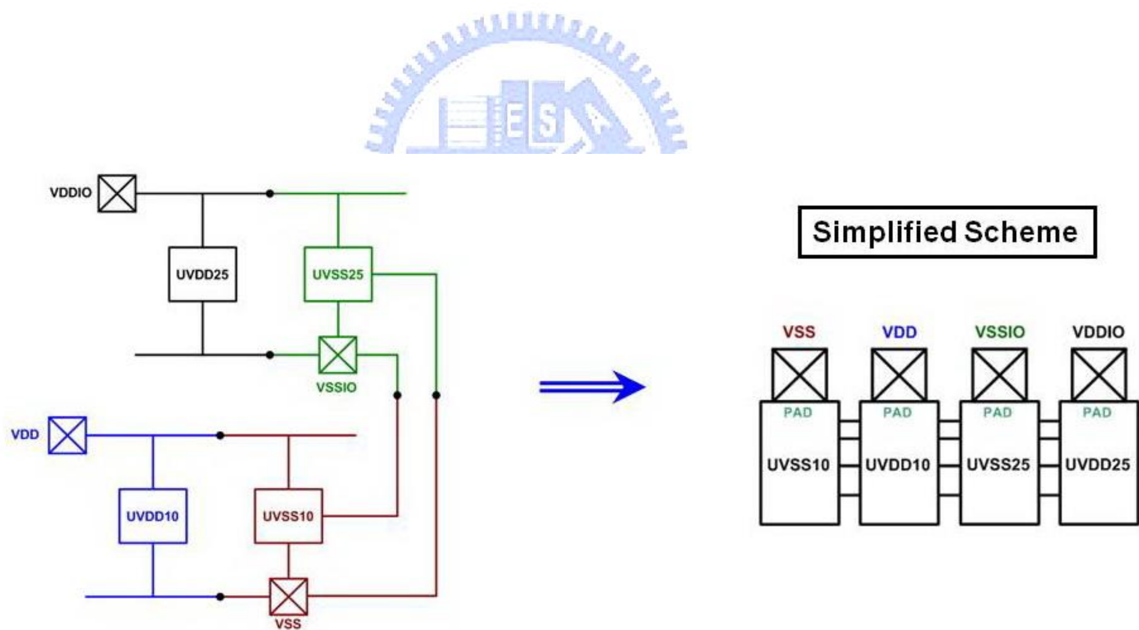


Fig. 5.21 Simplified scheme of whole-chip protection circuit.

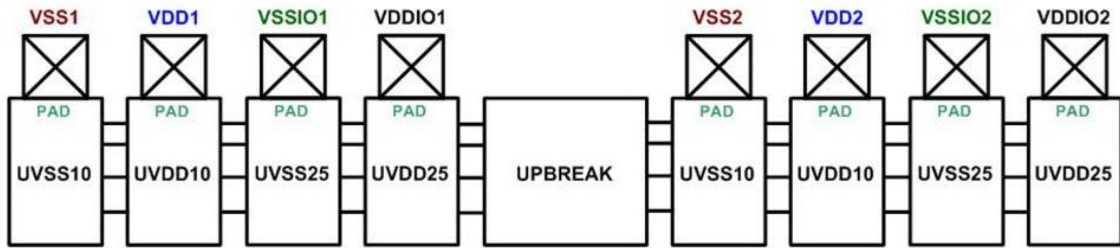


Fig. 5.22 Whole-chip protection scheme with power break cell.

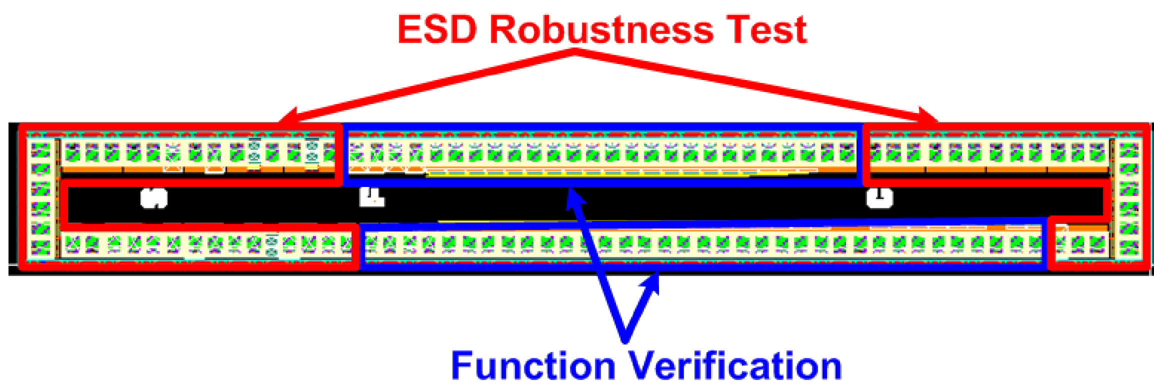


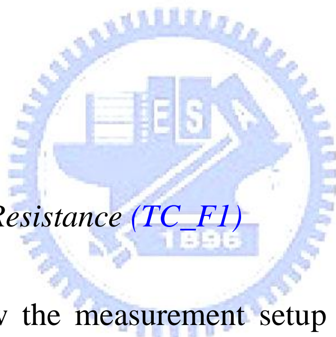
Fig. 5.23 Layout-top-view of test chip in UMC 90-nm CMOS process.

Chapter 6

Experimental Results

6.1 FUNCTION VERIFICATION

The test chip of the configurable I/O cell library in this thesis has been fabricated in UMC 90-nm CMOS process. Fig. 6.1 shows the die photo of the fabricated test chip with layout area is 3585.09μm × 425.39μm. The printed circuit board (PCB) of the test chip is shown in Fig. 6.2.



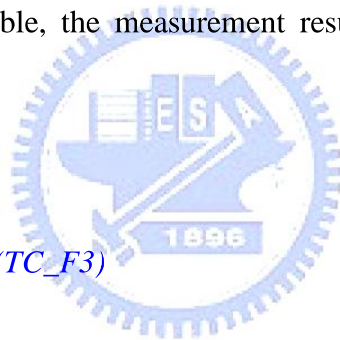
6.1.1 Pull-up/Pull-down Resistance (TC_F1)

Fig. 6.3(a) and (b) show the measurement setup to verify the pull-up and pull-down resistance, respectively. In this measurement, the function of pull-up/pull-down network has been measured with the test circuit TC_F1 only. The signals at Sa are generated by a pulse generator and the pull-up/pull-down signals at I/O PADa can be observed by a digital phosphor oscilloscope.

Fig. 6.4, Fig. 6.5, and Fig. 6.6 show the measured waveforms of the pull-up/pull-down network with 2.5-V, 1.8-V, and 3.3-V VDDIO supply voltage, respectively. The signals of the I/O PADa can be pulled up (down) to logic high (low) successfully. Moreover, the simulation and measurement results of the pull-up/pull-down network are summarized in Table 6.1. The compared simulation results are simulated with additional loading capacitance of 12pF under pseudo worst case (TT/85°C). The measurement results are close to the simulation results.

6.1.2 Schmitt-trigger Threshold Point (TC_F2)

Fig. 6.7(a) and Fig. 6.7(b) show the measurement setup to verify the threshold voltages of the schmitt-trigger input stage and normal input stage, respectively. In this measurement, since the output stage, pull-up network and pull-down network of configurable I/O cell should be turned off to use the input stage only, the pins Sa, Ia, PUa, and PDa are biased at 0V. The output voltage can be measured by a parameter analyzer while the I/O PADa is swept from low to high and then returned to its initial voltage. Fig. 6.8, Fig. 6.9, and Fig. 6.10 show the measurement waveforms of the input stage threshold points with 2.5-V, 1.8-V, and 3.3-V VDDIO supply voltage, respectively. Table 6.2 lists the threshold voltages of the simulation and measurement results. The compared simulation results are simulated with pseudo worst case (TT/85°C). From the table, the measurement results are also close to the simulation results.



6.1.3 Driving Capability (TC_F3)

Fig. 6.11(a) and Fig. 6.11(b) show the measurement setup to verify the low level output current (I_{OL}) and the high level output current (I_{OH}), respectively. According to the different driving current, the pins S0b, S1b, and S2b should be biased at the corresponding logic high or low. In order to measure the low level output current (I_{OL}) as shown in Fig. 6.11(a), the pin Ib is biased at 0V, and the I/O PADb is biased at a 0.4-V V_{OL} simultaneously to measure the current capability at PADb by a parameter analyzer. In order to measure the high level output current (I_{OH}) as shown in Fig. 6.11(b), the pin Ib is biased at logic high, and the I/O PADb is biased at a V_{OH} simultaneously to measure the I_{OH} by a parameter analyzer. Table 6.3, Table 6.4, and Table 6.5 list the measurement results of the driving capability. The measurement results show the configurable I/O cell can provide sufficient driving currents successfully to meet the driving currents specification.

6.1.4 Simultaneous Switching Noise (SSN) (TC_F4 & TC_F5)

The measurement setup to verify SSN issue is shown in Fig. 6.12. In common with the measurement of the driving capability, the pins S0b, S1b, and S2b can be biased at the logic high or low individually to select the corresponding driving current. The output waveforms can be measured at pins PADn(s)01, $VDDIO_{chip}$, and $VSSIO_{chip}$ by a digital phosphor oscilloscope. Fig. 6.13(a) and Fig. 6.13(b) show the measured waveforms of SSN with UCIONS (without slew-rate control) and UCIOS (with slew-rate control) cells, respectively. In this measurement, the VDDIO supply voltage is biased at 2.5V and the driving current is set in 24mA (S0b = S1b = S2b = 1). From these two figures, the $\Delta V_{VDDIOchip_under}$ can be decreased from 1.3V to 1.06V and the $\Delta V_{VSSIOchip_over}$ can be reduced from 1.64V to 1.32V with slew-rate control mechanism. Fig. 6.14(a) and Fig. 6.14(b) show the measurement results of the ground bounce effects with variation of the driving current. Since this measurement is measured to verify the impression of the slew-rate control mechanism, the VDDIO supply voltage is biased at 2.5V only to observe the ground bounce effects. From the Fig. 6.14(a) and Fig. 6.14(b), the $\Delta V_{VDDIOchip_under}$ and $\Delta V_{VSSIOchip_over}$ can be obviously reduced with the UCIOS cell. Thus, the UCIOS cell can improve the ground bounce effects efficiently.

6.1.5 Propagation Delay (TC_F4 & TC_F5)

The measurement setup to test the propagation delay of the UCIONS and UCIOS cells is shown in Fig. 6.15. The output waveforms can be observed at the I/O PADn(s)01 and PADn(s)17 by a digital phosphor oscilloscope. Fig. 6.16(a) and Fig. 6.16(b) show the measured waveforms of the UCIONS and UCIOS cells with 2.5-V VDDIO and 24-mA driving current, respectively. The ΔT of the UCIONS cell is 23.87ns, and that of the UCIOS cell is 26.05ns. After the calculations by the equation (4), the propagation delay of the UCIONS and UCIOS cells are 1.39ns and 1.52ns, respectively. The UCIONS cell operating in

transmitting mode is faster than the UCIOS cell. Fig. 6.17 shows the comparison between measurement and simulation results of the propagation delay when the UCIONS and UCIOS operating with 2.5-V VDDIO and different driving current. The simulation results are simulated with additional loading capacitances of 12pF at the I/O PADn(s)01 and PADn(s)17 under pseudo worst case (TT/85°C) and. Since all results of the propagation delay are in the order of nano-second (ns), the measured results are very close to simulated results. In Fig. 6.18, the propagation delay comparison between the measurement and simulation results with different VDDIO supply voltages and the driving currents is shown. The simulated environment in Fig. 6.18 is the same as that in Fig. 6.17.

6.1.6 Operating Frequency

The measurement setup to test the operating frequency at the output stage of the configurable I/O cell is shown in Fig. 6.19. The measurement is measured with the test circuit TC_F3 only. The signals at Ib, which are generated by a pulse generator, are transmitted to I/O PADb, and can be observed by a digital phosphor oscilloscope. Fig. 6.20(a), Fig. 6.20(b), and Fig. 6.20(c) show the measured waveforms of the configurable I/O cell to transmit the 266-MHz signals with voltage swings of 0-to-VDDIO from the pin Ib to the I/O PADb in 24-mA driving current under 2.5-V, 1.8-V, and 3.3-V VDDIO supply voltages, respectively. The signals at Ib can be successfully transmitted to the I/O PADb with the same voltage swing. The input signals at Ib and I/O PADb are like sinusoidal waves due to the constraint of the driving ability in the pulse generator. From the measured results in Fig. 6.4 ~ Fig. 6.6, Fig. 6.8 ~ Fig. 6.10 and Fig. 6.20, the configurable I/O cell can be correctly operated in receiving mode, transmitting mode, and tri-state. Table 6.6 lists the operating frequency of the configurable I/O cell with different VDDIO supply voltage and driving current.

6.2 ESD ROBUSTNESS

6.2.1 Each Power Cell

Table 6.7 lists the human-body-model (HBM) and machine-model (MM) ESD robustness of the UVDD25 and UVDD10 cells under positive or negative VDDIO(VDD)-to-VSSIO(VSS) ESD stress. The circuit design and testkey arrangement of each power/ground cell is mentioned in Chapter 3 and section 5.2. The test voltage of the HBM ESD stress is from ±0.5kV to ±5kV with step of ±0.5kV and the test voltage of the MM ESD stress is from ±50V to ±500V with step of ±50V. The failure criterion is defined as the measured voltage at the current level of 1μA shifted ±30% from its original voltage value. The aforementioned test method in the HBM and MM ESD stresses and the failure criterion are also used to following ESD test in this chapter. From shown in Table 6.7, the ESD level are all higher than 5k-V HBM and 500-V MM ESD stresses. Table 6.8 and Table 6.9 list the HBM and MM ESD robustness of the UVSS25 and UVSS10 cells, respectively. The HBM and MM ESD level of UVSS10 are 4.5kV and 350V, which are dominated by the VDD power line under positive VDD-to-VSS(VSSIO) ESD stresses. However, these ESD levels of such power/ground cells are high enough for safe IC production and field applications.

The HBM and MM ESD robustness of the 2.5-V and 1.0-V analog I/O cells under different pin combinations are listed in Table 6.10 and Table 6.11, respectively. The UAIO25+INV and UAIO10+INV cells are testkeys to verify the actual protection as shown in Fig. 5.19. From the Table 6.11, the HBM and MM ESD level of the UAIO and UAIO+INV cells are 4kV and 350V, which are dominated by the VDD power line under positive VDD-to-VSS ESD stresses. However, the ESD levels of the I/O PADs under other modes of ESD stresses are near to or even over 5-kV HBM and 500-V MM ESD stresses. With such ESD levels in a small layout area, such analog I/O cells are very suitable for analog I/O circuit

applications. To further improve ESD level, the increase of the STSCR effective area is a design suggestion.

Table 6.12 lists the HBM and MM ESD robustness of the power break cell. The ESD levels of the HBM and MM ESD stresses are 2.5kV and 200V, respectively, which are dominated under positive VDD1(VSS1)-to-VDD2(VSS2) ESD stress. It implies that the diode sizes of the 1.0-V power domain are too small to discharge the ESD currents. However, such ESD levels of the power break cell in a small layout area can pass the requirement of the ESD specification (2-kV HBM and 200-V MM ESD stresses), and achieve ESD level high enough to protect IC productions. To further improve ESD level, the increase effective area of the diode of the 1.0-V power domain is a design suggestion.

6.2.2 Whole-Chip ESD Protection Structure

The HBM and MM ESD robustness of the whole-chip protection circuit with the power break cell under different pin combinations are listed in Table 6.13. The ESD levels of the HBM and MM ESD stresses are 3kV and 300V, respectively, which are dominated under both positive VSS1-to-VSS2 and VDD1-to-VDD2 ESD stresses. It implies that the 1.0-V power domain of the power break cell dominates the ESD robustness. However, the all ESD levels under other modes of ESD stresses are over 5-kV HBM and 500-V MM ESD stresses.

Fig. 6.21 shows the teskey to test the ESD robustness of the configurable I/O cell with the whole-chip protection circuit. The whole-chip protection circuit is part of the function test circuit TC_F4. Table 6.14 lists the HBM and MM ESD robustness of the configurable I/O cell with the whole-chip protect circuit under different pin combinations. As a result, all ESD levels of the measured results are higher than 5-kV HBM and 500-V MM ESD stresses. Thus, the whole-chip protection has a great ability to protect the internal and I/O circuits

simultaneously. Moreover, to test the protective extend of the whole-chip protection circuit, the function test circuits TC_F1, TC_F2, TC_F3, and TC_F4 are used to verify it as shown in Fig. 6.22 and the longest distance of the measured region is 1801.05μm. According to the test method in Table 6.14, the HBM and MM ESD stresses are zapped step by step from the first I/O PAD to the last I/O PAD. The test result is that all ESD levels of the HBM and MM ESD stress are over 5kV and 500V, respectively. Therefore, the whole-chip protection circuit can sustain over 5-kV HBM and 500-V MM ESD stress successfully within the distance of 1801.05μm.

6.3 SUMMARY

The configurable I/O cell library has been designed and successfully fabricated in UMC 90-nm salicided CMOS process. The functions of the pull-up/pull-down, driving capacities, schmitt-trigger, and slew-rate control have been measured to verify its effectiveness. The ground bounce effects can be reduced greatly with the slew-rate control mechanism. The analog I/O and power cells have been verified its ESD robustness and it can effectively protect the core circuits and I/O output driver in UMC 90-nm CMOS technology for system-on-a-chip (SoC) applications.

Tabel 6.1

The simulation and measurement results of pull-up/pull-down network.

Parameters			Simulation Results	Measurement Results
VDDIO	2.5V	T_r (with Pull-up Network)	1.029μs	1.043μs
	1.8V		1.032μs	0.994μs
	3.3V		1.026μs	1.061μs
	2.5V	T_f (with Pull-down Network)	1.026μs	1.017μs
	1.8V		1.039μs	1.023μs
	3.3V		1.019μs	0.920μs

Tabel 6.2

The simulation and measurement results of input stage threshold points.

Parameters				Simulated Results		Measured Results	
SCH	1/0: Schmitt-trigger Enable/Disable	1	0	1	0	1	0
VDDIO	2.5V	V_{T+} (V)	V_{TH} (V)	1.625	1.245	1.625	1.280
		V_{T-} (V)		0.835		0.885	
	1.8V	V_{T+} (V)	V_{TH} (V)	1.335	0.885	1.295	0.905
		V_{T-} (V)		0.605		0.635	
	3.3V	V_{T+} (V)	V_{TH} (V)	1.905	1.735	1.935	1.795
		V_{T-} (V)		1.135		1.255	

Tabel 6.3

Measurement results of the driving capability under 2.5-V VDDIO supply voltage.

Parameters			Measured Results
I_{OL}	Low Level Output Current @ V_{OL} = 0.4V	2mA	3.68mA
		8mA	13.98mA
		10mA	17.02mA
		14mA	22.83mA
		16mA	25.50mA
		22mA	33.00mA
		24mA	35.24mA
I_{OH}	High Level Output Current @ V_{OH} = 1.85V	2mA	4.73mA
		8mA	17.53mA
		10mA	21.56mA
		14 mA	29.03mA
		16mA	32.65mA
		22mA	42.55mA
		24mA	45.72mA

Tabel 6.4

Measurement results of the driving capability under 1.8-V VDDIO supply voltage.

Parameters			Measured Results
I_{OL}	Low Level Output Current @ V_{OL} = 0.4V	2mA	2.67mA
		8mA	10.41mA
		10mA	12.71mA
		14mA	17.27mA
		16mA	19.38mA
		22mA	25.51mA
		24mA	27.34mA
I_{OH}	High Level Output Current @ V_{OH} = 1.62V	2mA	2.96mA
		8mA	11.19mA
		10mA	13.83mA
		14 mA	18.81mA
		16mA	21.26mA
		22mA	28.10mA
		24mA	30.29mA

Tabel 6.5

Measurement results of the driving capability under 3.3-V VDDIO supply voltage.

Parameters			Measured Results
I_{OL}	Low Level Output Current @ $V_{OL} = 0.4V$	2mA	4.28mA
		8mA	16.03mA
		10mA	19.42mA
		14mA	25.89mA
		16mA	28.83mA
		22mA	36.99mA
		24mA	39.39mA
I_{OH}	High Level Output Current @ $V_{OH} = 2.6V$	2mA	6.34mA
		8mA	23.13mA
		10mA	28.35mA
		14 mA	37.86mA
		16mA	42.44mA
		22mA	54.71mA
		24mA	58.58mA

Tabel 6.6

The operating frequency of the configurable I/O cell operating in transmitting mode with different driving current and VDDIO supply voltage.

VDDIO	Driving Current						
	2mA	8mA	10mA	14mA	16mA	22mA	24mA
2.5V	>66MHz	>133MHz	>266MHz	>266MHz	>266MHz	>266MHz	>266MHz
1.8V	>10MHz	>133MHz	>133MHz	>266MHz	>266MHz	>266MHz	>266MHz
3.3V	>66MHz	>266MHz	>266MHz	>266MHz	>266MHz	>266MHz	>266MHz

Tabel 6.7

HBM and MM ESD robustness of the UVDD25 and UVDD10 cells.

ESD Stress / Cell Name	HBM		MM	
	VDDIO(VDD) -to- VSSIO(VSS) (+)	VDDIO(VDD) -to- VSSIO(VSS) (-)	VDDIO(VDD) -to- VSSIO(VSS) (+)	VDDIO(VDD) -to- VSSIO(VSS) (-)
UVDD25	> 5kV		> 500V	
UVDD10	> 5kV		> 500V	

*ESD level: maximum pass voltage before the chip failing

Tabel 6.8

HBM and MM ESD robustness of the UVSS25 cell.

ESD Stress / Cell Name	HBM		MM	
	VDDIO -to- VSSIO(VSS) (+)	VDDIO -to- VSSIO(VSS) (-)	VDDIO -to- VSSIO(VSS) (+)	VDDIO -to- VSSIO(VSS) (-)
UVSS25	> 5kV		> 500V	

Tabel 6.9

HBM and MM ESD robustness of the UVSS10 cell.

ESD Stress / Cell Name	HBM		MM	
	VDD -to- VSS(VSSIO) (+)	VDD -to- VSS(VSSIO) (-)	VDD -to- VSS(VSSIO) (+)	VDD -to- VSS(VSSIO) (-)
UVSS10	4.5kV	> 5kV	350V	> 500V

Tabel 6.10

HBM and MM ESD robustness of the 2.5-V analog I/O cells.

ESD Event	ESD Stress / Cell Name	PS-Mode VSSIO (+)	NS-Mode VSSIO (-)	PD-Mode VDDIO (+)	ND-Mode VDDIO (-)	VDDIO -to- VSSIO (+)	VDDIO -to- VSSIO (-)
HBM	UAIO25	> 5kV					
MM		> 500V					
HBM	UAIO25+INV	> 5kV					
MM		> 500V					

Tabel 6.11

HBM and MM ESD robustness of the 1.0-V analog I/O cells.

ESD Event	ESD Stress / Cell Name	PS-Mode VSS (+)	NS-Mode VSS (-)	PD-Mode VDD (+)	ND-Mode VDD (-)	VDD -to- VSS (+)	VDD -to- VSS (-)
HBM	UAIO10	> 5kV				4kV	> 5kV
MM		400V	> 500V		450V	400V	> 500V
HBM	UAIO10+INV	> 5kV				4kV	> 5kV
MM		450V	> 500V		450V	350V	> 500V

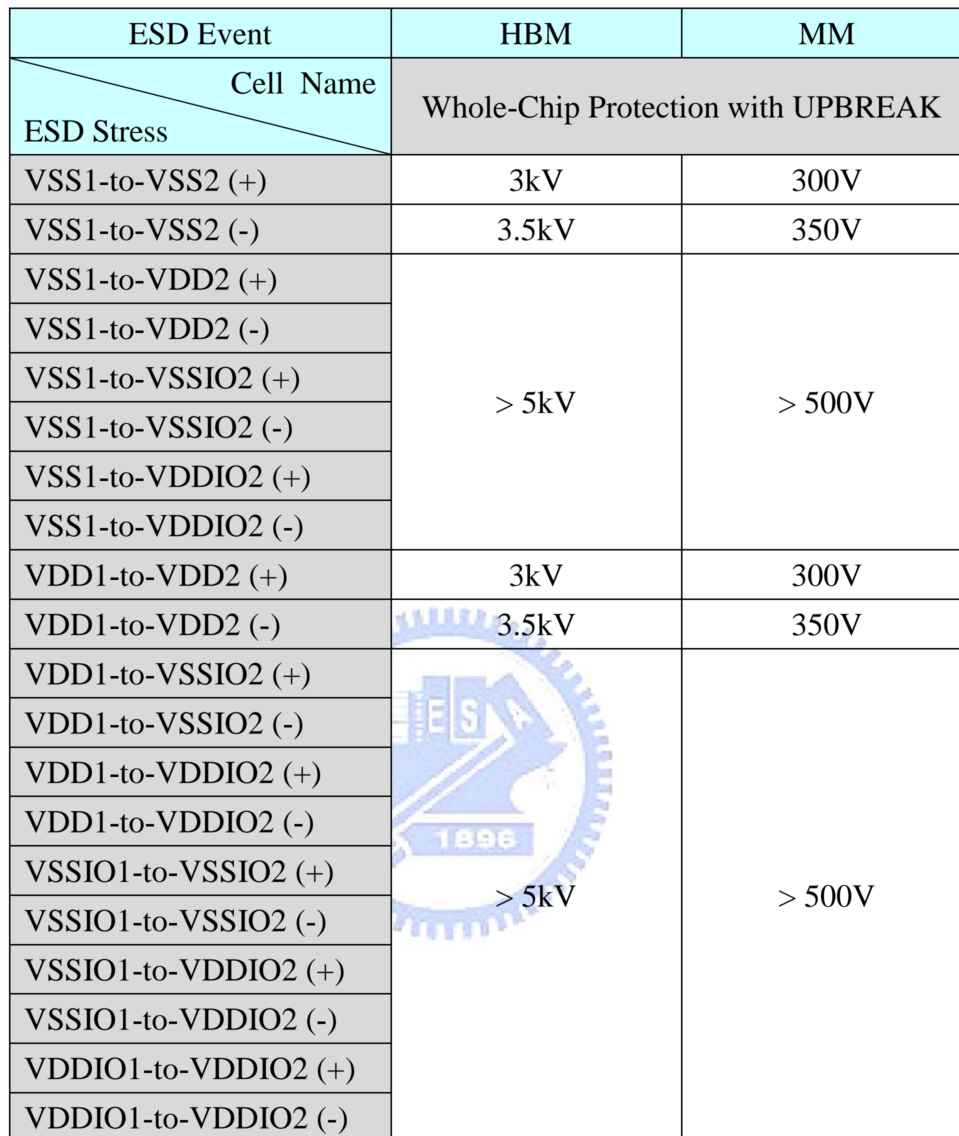
Tabel 6.12

HBM and MM ESD robustness of the power break cell.

ESD Event	ESD Stress / Cell Name	VDD1(VSS1) -to- VDD2(VSS2) (+)	VDD1(VSS1) -to- VDD2(VSS2) (-)	VDDIO1(VSSIO1) -to- VDDIO2(VSSIO2) (+)	VDDIO1(VSSIO1) -to- VDDIO2(VSSIO2) (-)
HBM	UPBREAK	2.5kV	3kV	> 5kV	> 5kV
MM		200V	250V	> 500V	> 500V

Tabel 6.13

HBM and MM ESD robustness of whole-chip protection with power break cell.



<table>
<tr><th>ESD Event</th><th>HBM</th><th>MM</th></tr>
<tr><td>Cell Name
ESD Stress</td><td colspan="2">Whole-Chip Protection with UPBREAK</td></tr>
<tr><td>VSS1-to-VSS2 (+)</td><td>3kV</td><td>300V</td></tr>
<tr><td>VSS1-to-VSS2 (-)</td><td>3.5kV</td><td>350V</td></tr>
<tr><td>VSS1-to-VDD2 (+)</td><td rowspan="6">> 5kV</td><td rowspan="6">> 500V</td></tr>
<tr><td>VSS1-to-VDD2 (-)</td></tr>
<tr><td>VSS1-to-VSSIO2 (+)</td></tr>
<tr><td>VSS1-to-VSSIO2 (-)</td></tr>
<tr><td>VSS1-to-VDDIO2 (+)</td></tr>
<tr><td>VSS1-to-VDDIO2 (-)</td></tr>
<tr><td>VDD1-to-VDD2 (+)</td><td>3kV</td><td>300V</td></tr>
<tr><td>VDD1-to-VDD2 (-)</td><td>3.5kV</td><td>350V</td></tr>
<tr><td>VDD1-to-VSSIO2 (+)</td><td rowspan="10">> 5kV</td><td rowspan="10">> 500V</td></tr>
<tr><td>VDD1-to-VSSIO2 (-)</td></tr>
<tr><td>VDD1-to-VDDIO2 (+)</td></tr>
<tr><td>VDD1-to-VDDIO2 (-)</td></tr>
<tr><td>VSSIO1-to-VSSIO2 (+)</td></tr>
<tr><td>VSSIO1-to-VSSIO2 (-)</td></tr>
<tr><td>VSSIO1-to-VDDIO2 (+)</td></tr>
<tr><td>VSSIO1-to-VDDIO2 (-)</td></tr>
<tr><td>VDDIO1-to-VDDIO2 (+)</td></tr>
<tr><td>VDDIO1-to-VDDIO2 (-)</td></tr>
</table>

Tabel 6.14

HBM and MM ESD robustness of configurable I/O cell with whole-chip protection.

<table>
<tr><th>ESD Event</th><th colspan="3">HBM</th><th colspan="3">MM</th></tr>
<tr><th>Cell Name / ESD Stress</th><th>UCIONS</th><th>UCIOS</th><th>UINPUT</th><th>UCIONS</th><th>UCIOS</th><th>UINPUT</th></tr>
<tr><td>I/O PAD-to-VSS (+)</td><td rowspan="8">> 5kV</td><td rowspan="8">> 5kV</td><td rowspan="8">> 5kV</td><td rowspan="8">> 500V</td><td rowspan="8">> 500V</td><td rowspan="8">> 500V</td></tr>
<tr><td>I/O PAD-to-VSS (-)</td></tr>
<tr><td>I/O PAD-to-VDD (+)</td></tr>
<tr><td>I/O PAD-to-VDD (-)</td></tr>
<tr><td>I/O PAD-to-VSSIO (+)</td></tr>
<tr><td>I/O PAD-to-VSSIO (-)</td></tr>
<tr><td>I/O PAD-to-VDDIO (+)</td></tr>
<tr><td>I/O PAD-to-VDDIO (-)</td></tr>
</table>

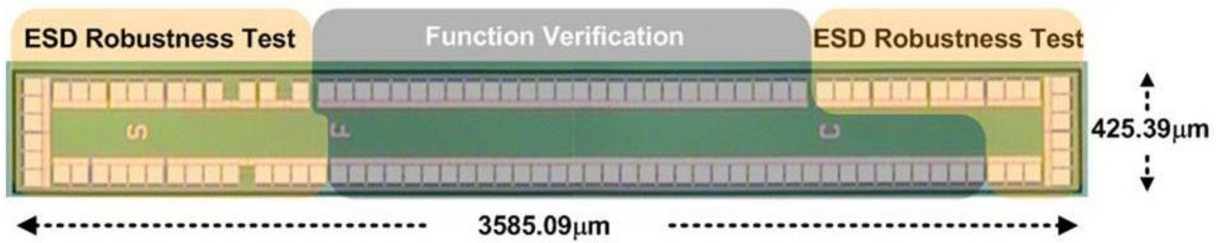


Fig. 6.1 The test chip photograph of the configurable I/O cell library in UMC 90-nm CMOS process.

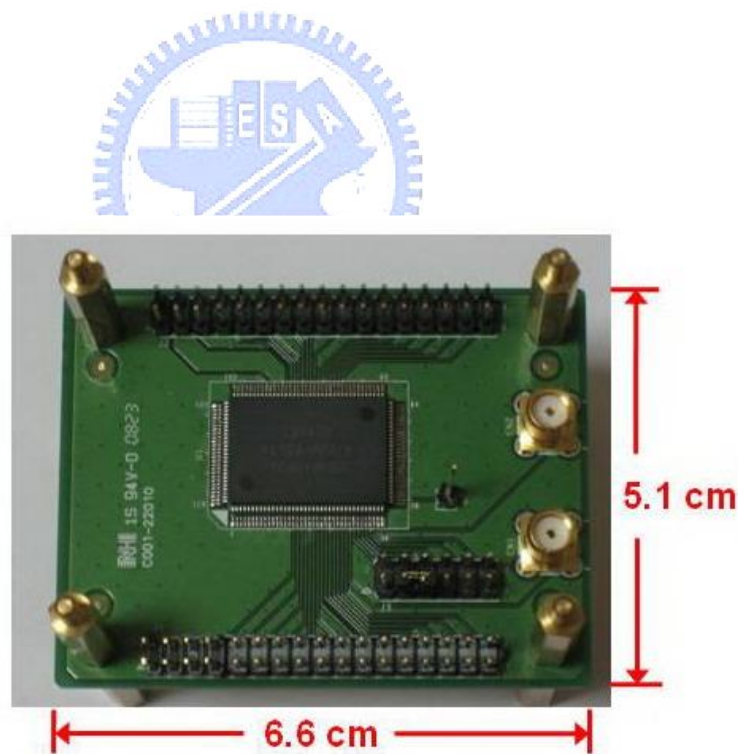


Fig. 6.2 The PCB view of tested chip.

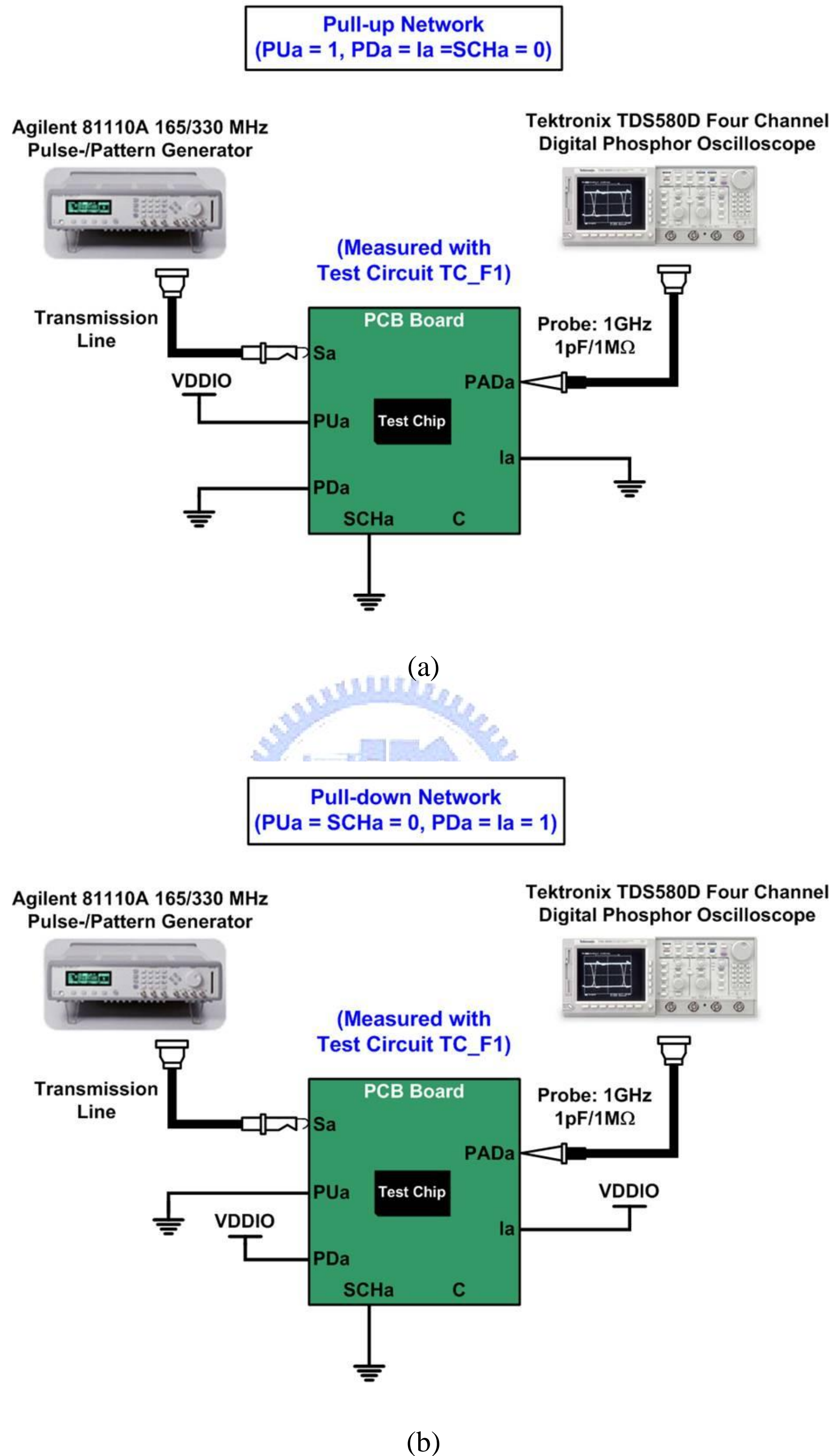
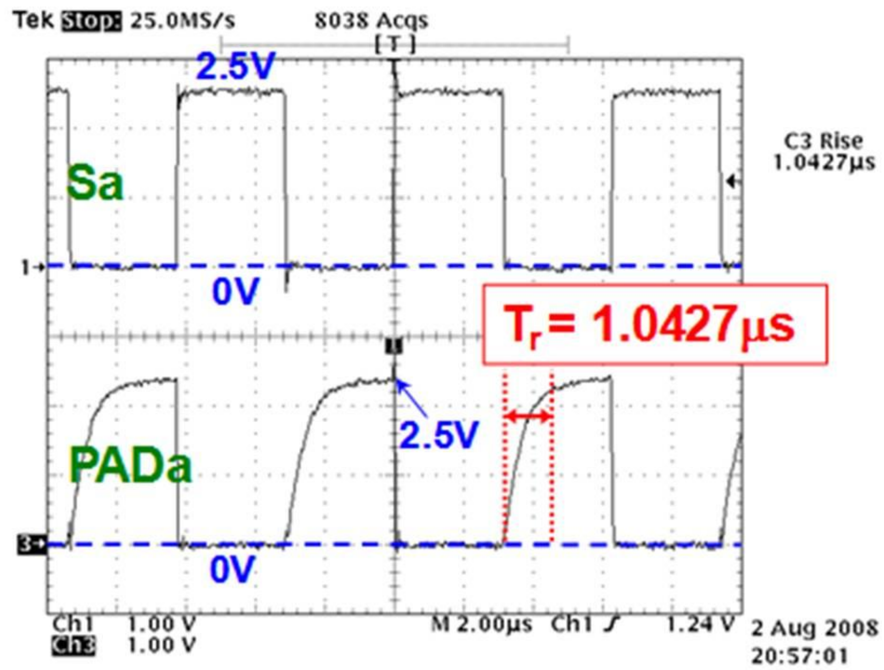
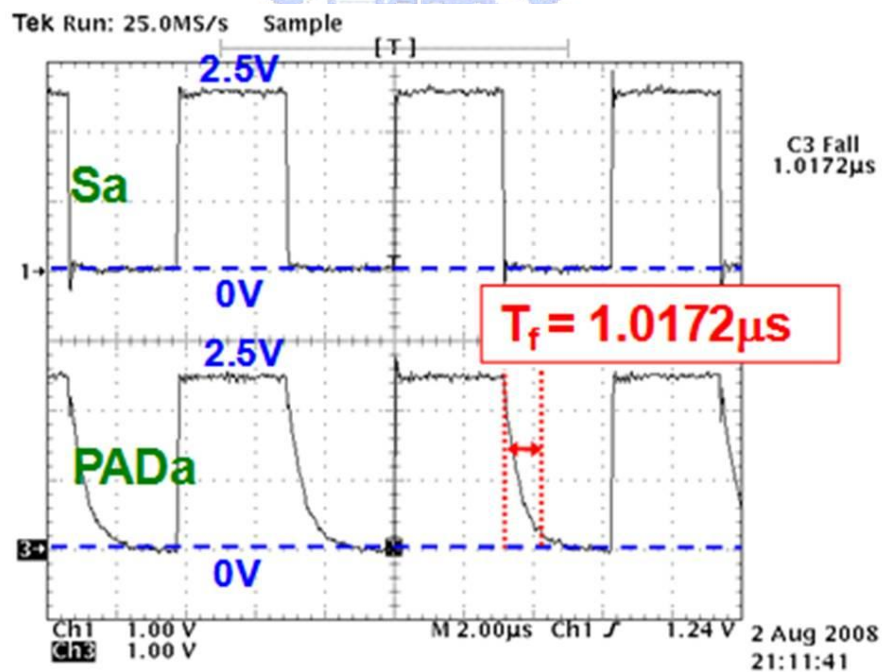


Fig. 6.3 Measurement setup to verify the (a) pull-up resistance and (b) pull-down resistance.

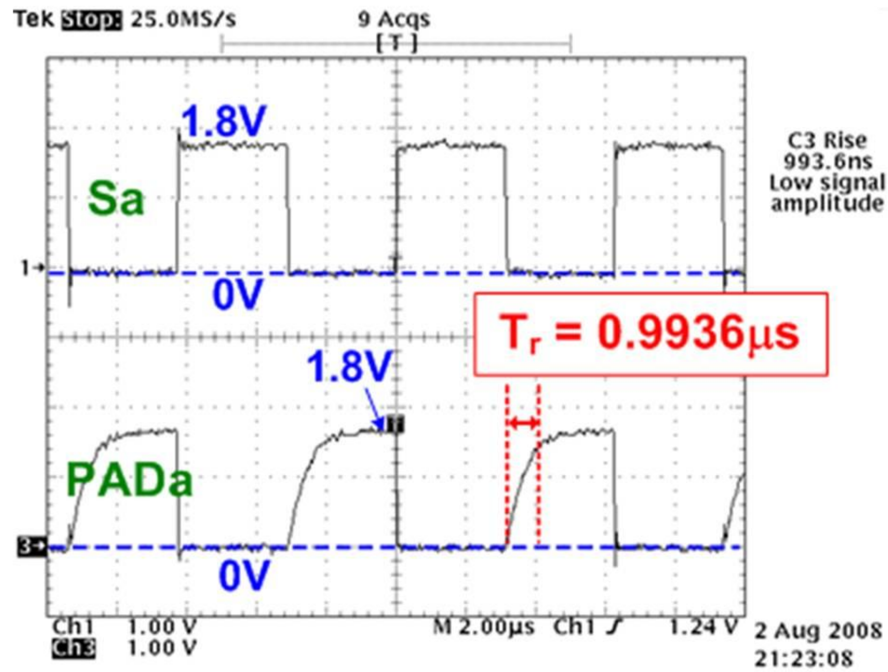


(a)

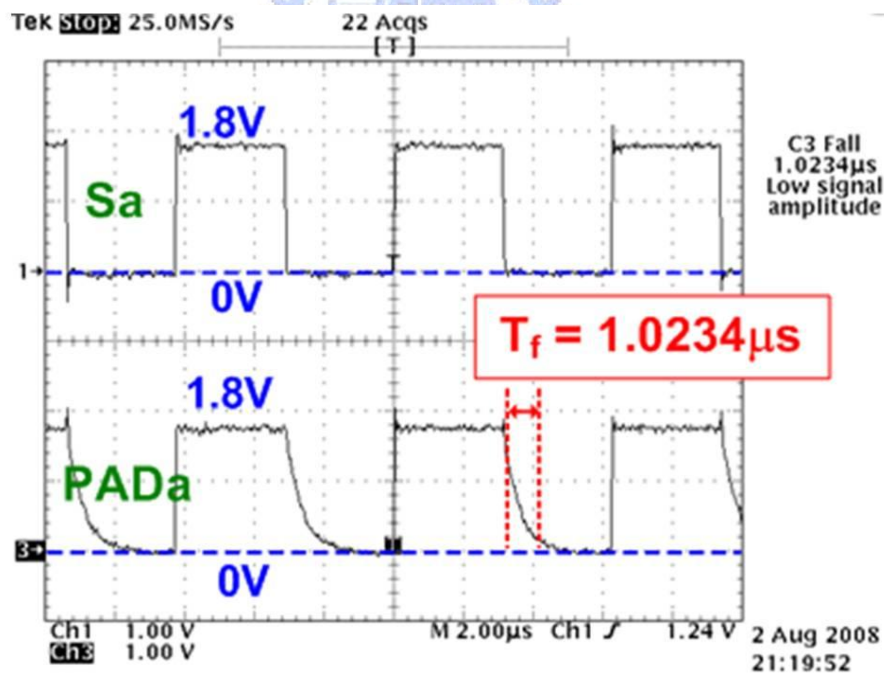


(b)

Fig. 6.4 Measured waveforms of the (a) pull-up network and (b) pull-down network with 2.5-V VDDIO voltage supply.

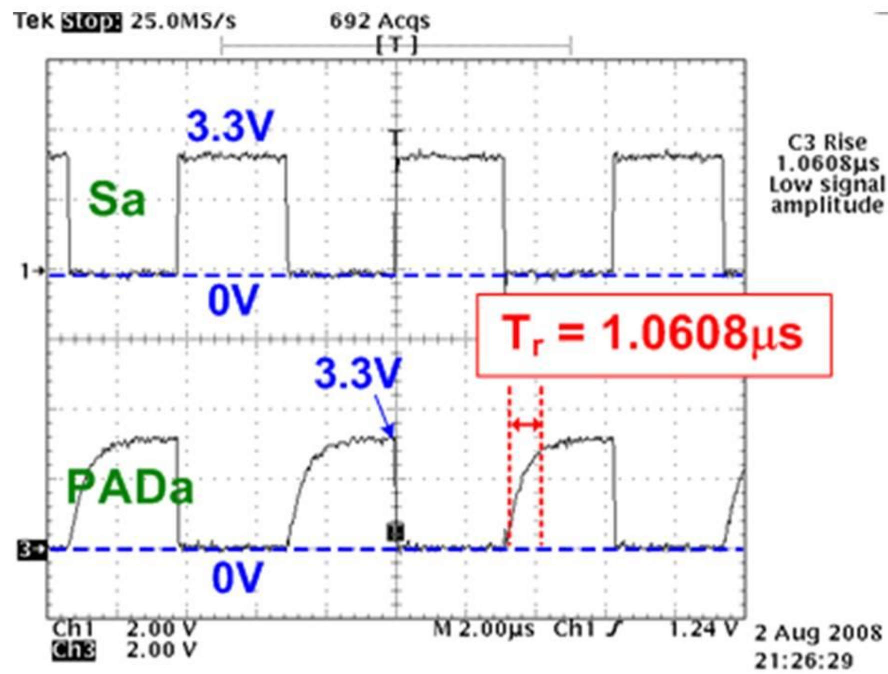


(a)

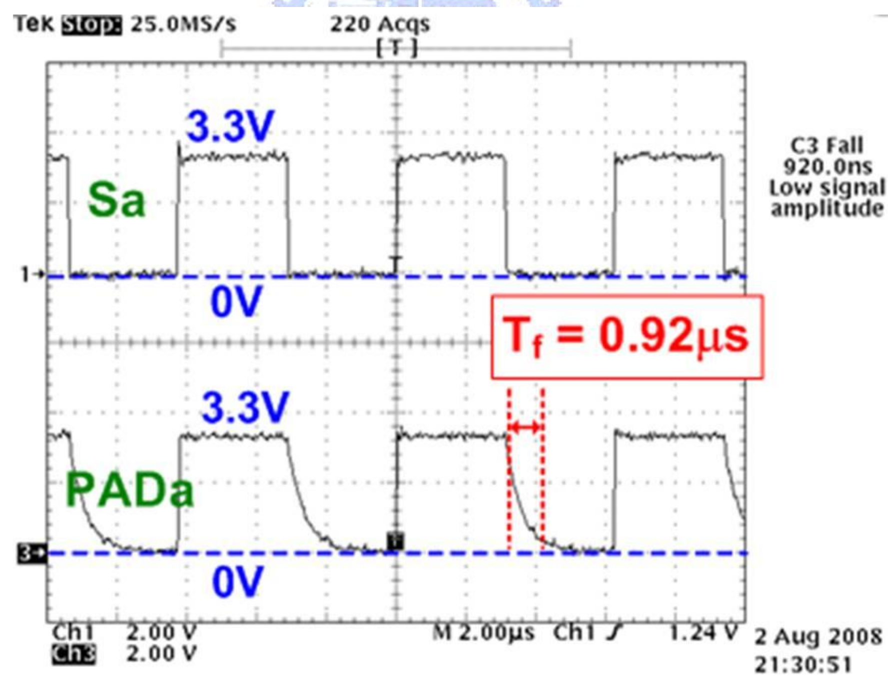


(b)

Fig. 6.5 Measured waveforms of the (a) pull-up network and (b) pull-down network with 1.8-V VDDIO voltage supply.



(a)



(b)

Fig. 6.6 Measured waveforms of the (a) pull-up network and (b) pull-down network with 3.3-V VDDIO voltage supply.

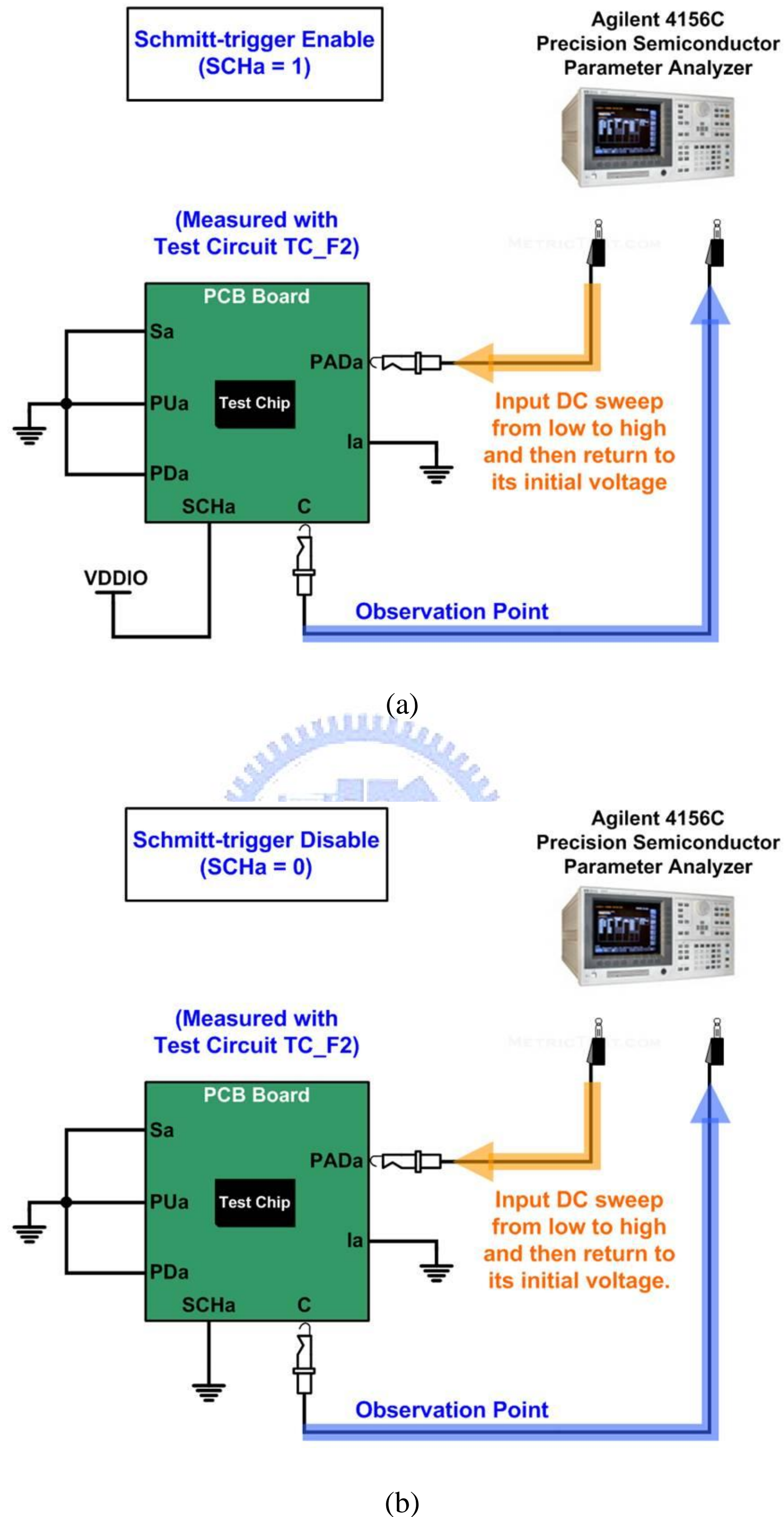
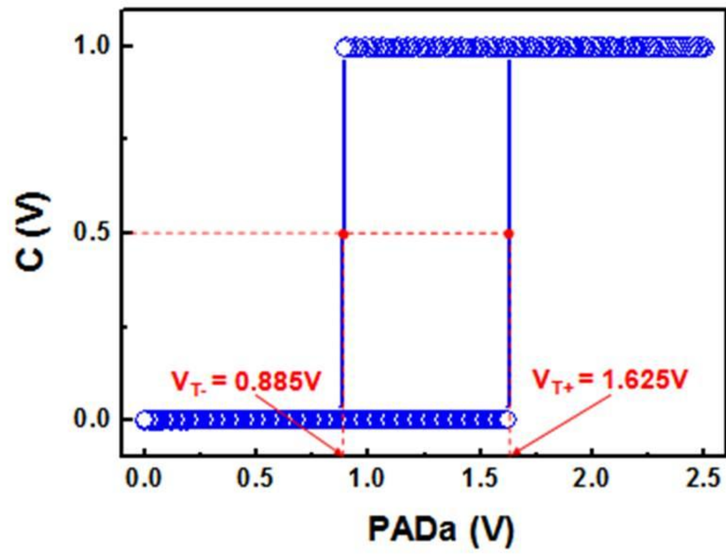
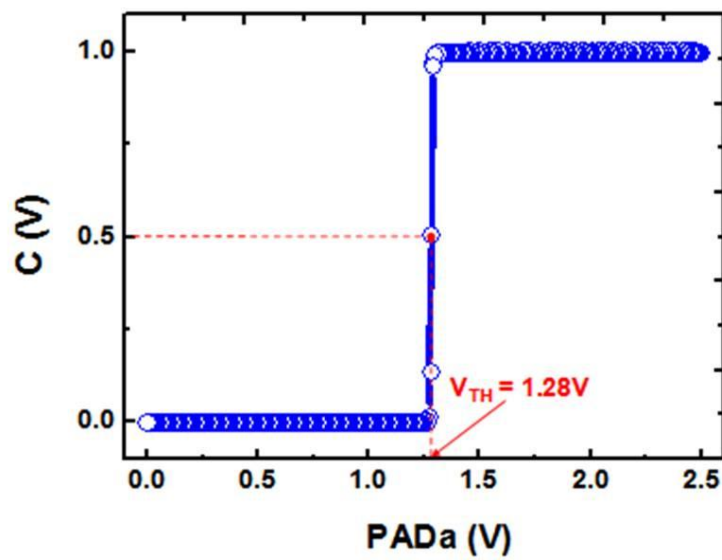


Fig. 6.7 Measurement setup to verify input stage threshold points with (a) schmitt-trigger enable (SCHa = 1) and (b) schmitt-trigger disable (SCHa =0).

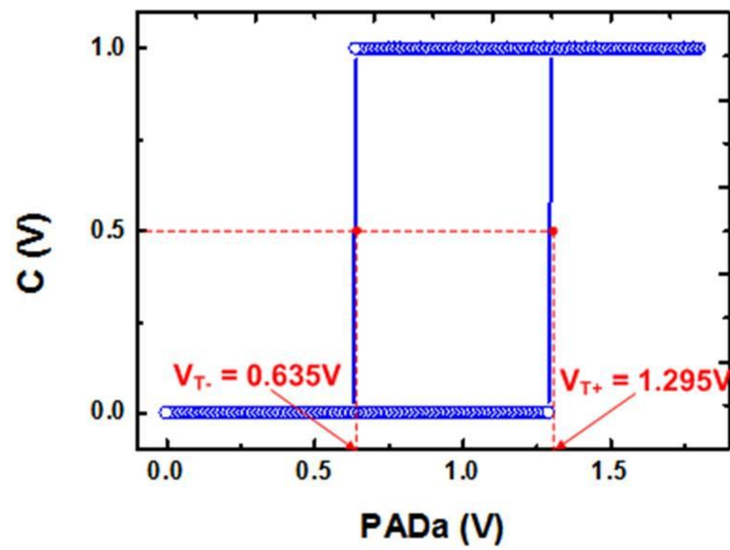


(a)

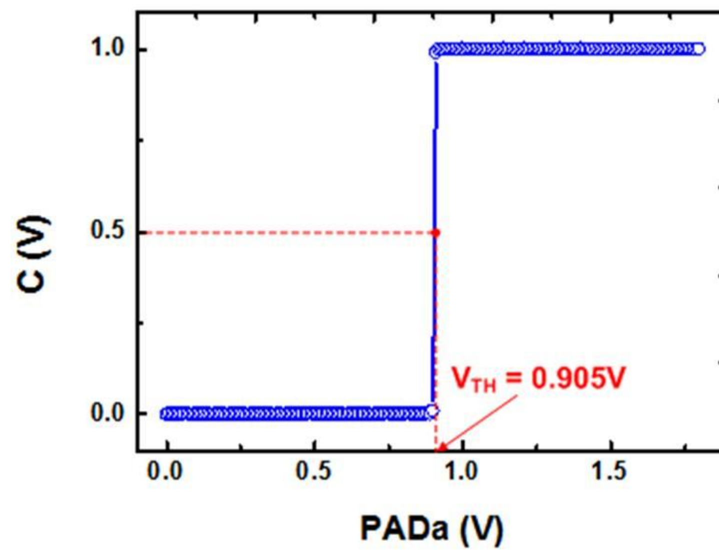


(b)

Fig. 6.8 Measured result of input stage with (a) schmitt-trigger enable (SCHa = 1) and (b) schmitt-trigger disable (SCHa =0) under 2.5-V VDDIO.

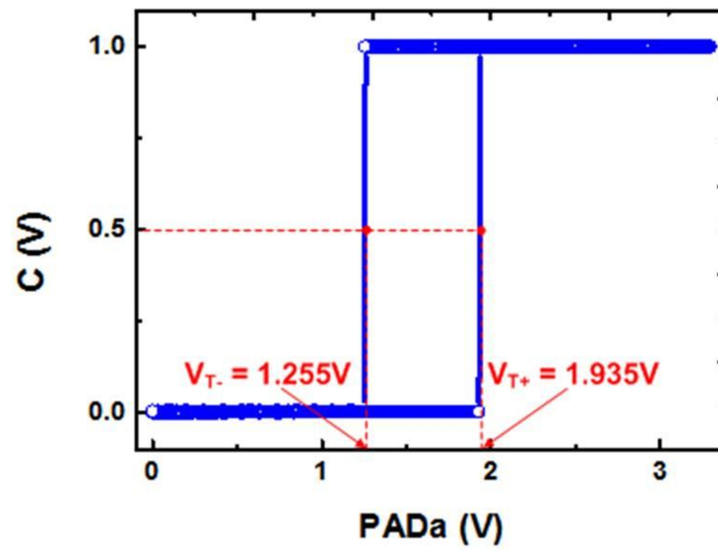


(a)

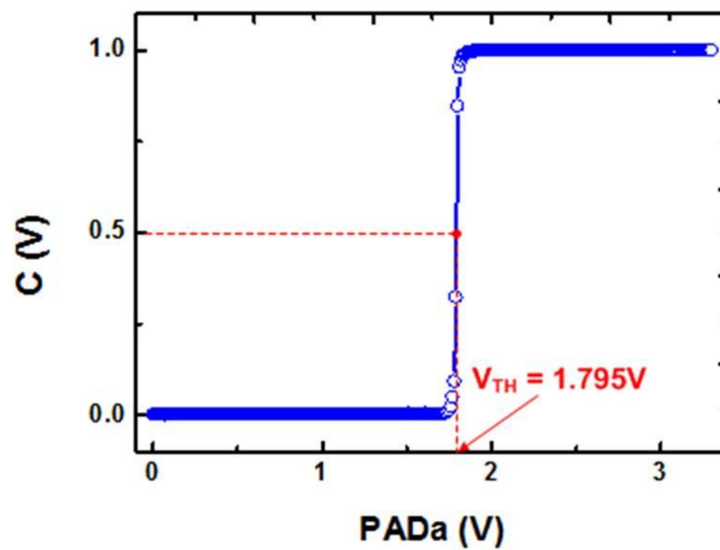


(b)

Fig. 6.9 Measured result of input stage with (a) schmitt-trigger enable (SCHa = 1) and (b) schmitt-trigger disable (SCHa =0) under 1.8-V VDDIO.

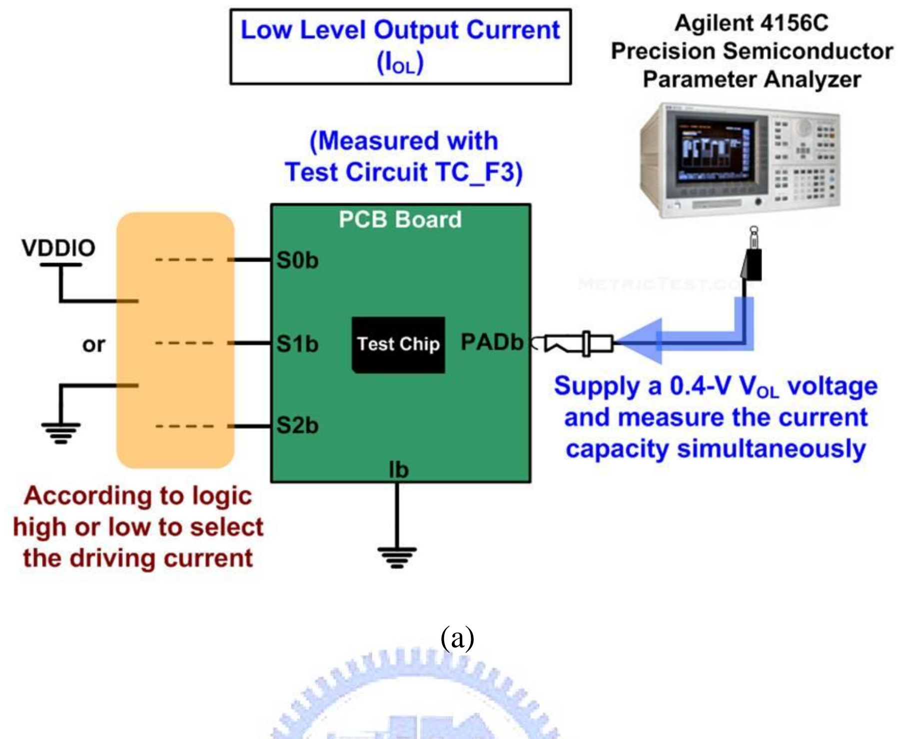


(a)

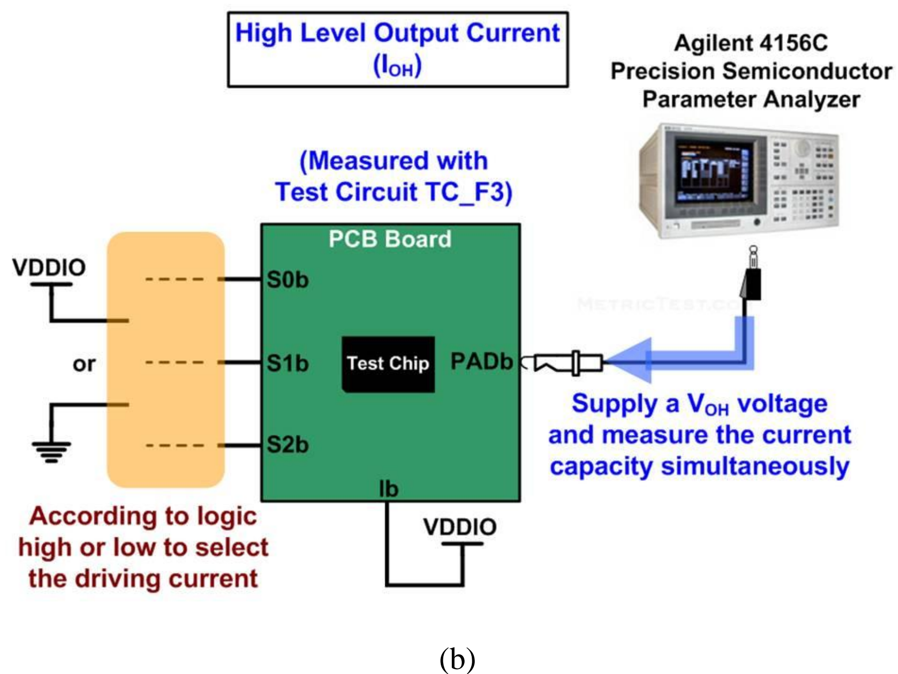


(b)

Fig. 6.10 Measured result of input stage with (a) schmitt-trigger enable (SCHa = 1) and (b) schmitt-trigger disable (SCHa =0) under 3.3-V VDDIO.



(a)



(b)

Fig. 6.11 Measurement setup to verify (a) low level output current (I_{OL}) and (b) high level output current (I_{OH}).

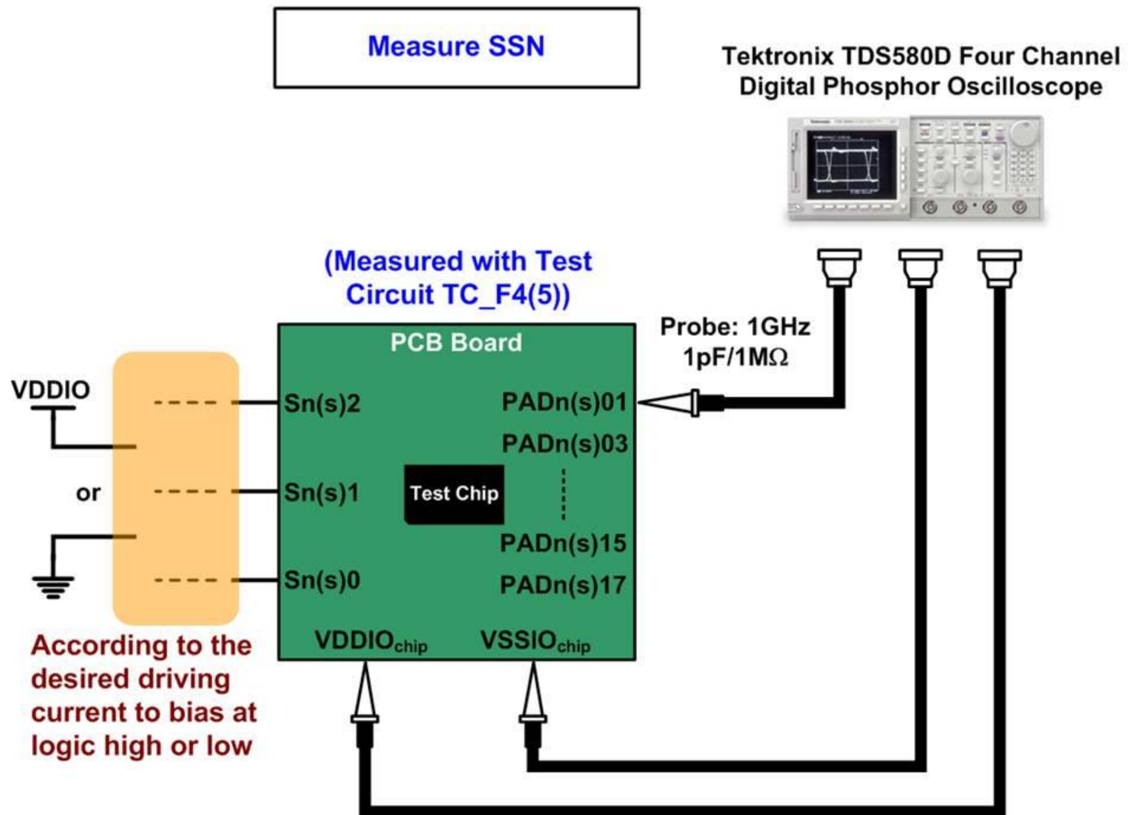
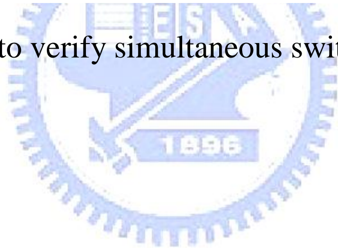
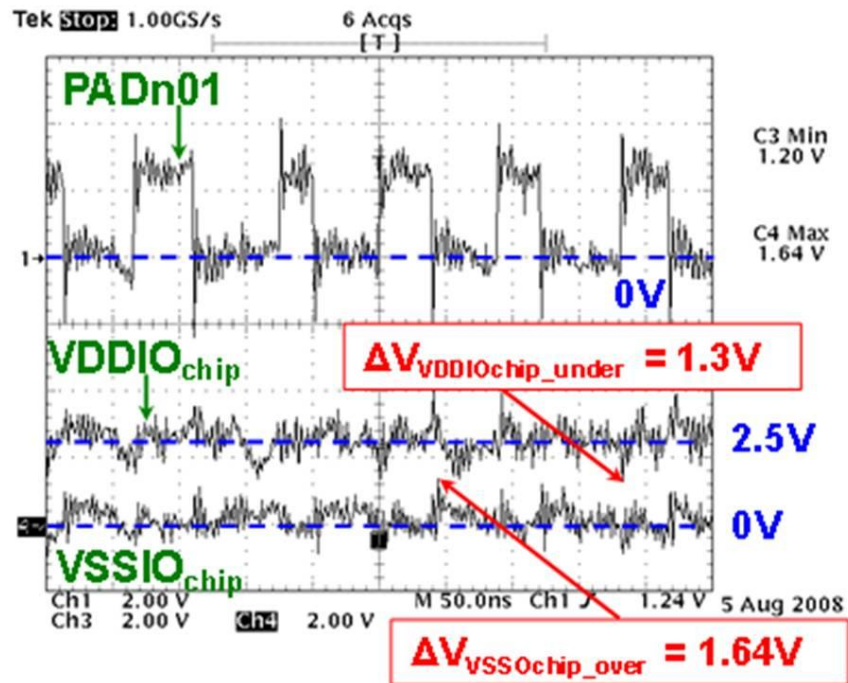
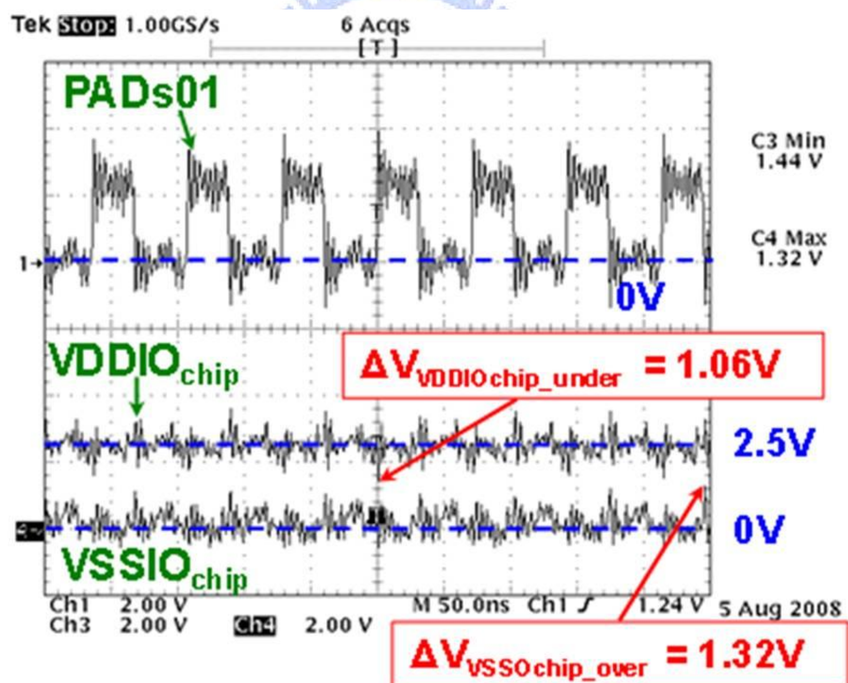


Fig. 6.12 Measurement setup to verify simultaneous switching noise (SSN).



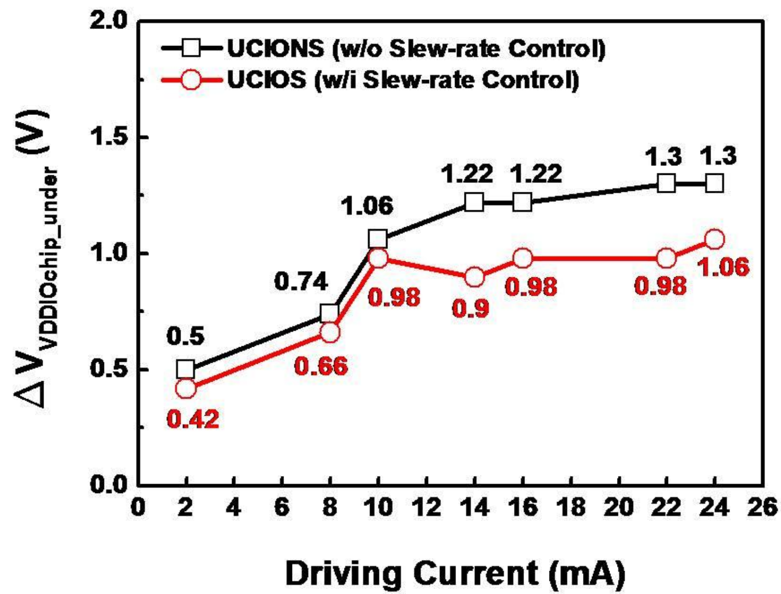


(a)

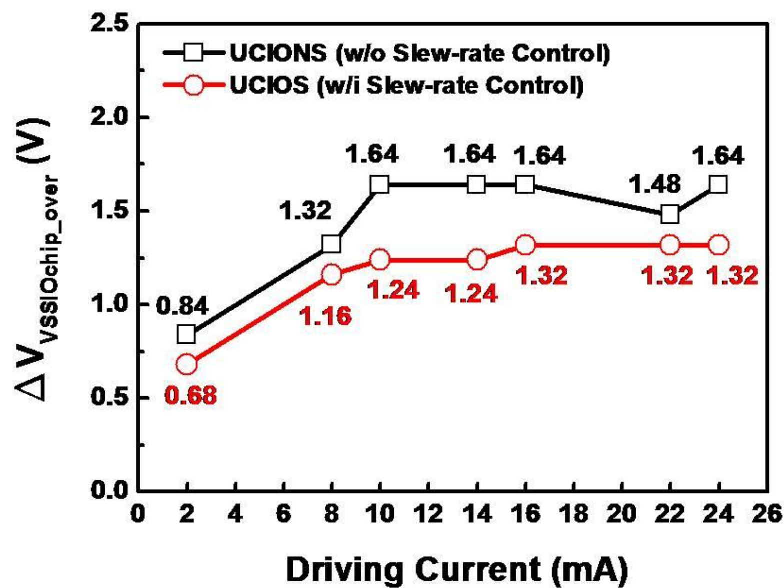


(b)

Fig. 6.13 Measured waveforms of simultaneous switching noise (SSN) issue when the configurable I/O cell operating (a) without slew-rate control (UCIONS) and (b) with slew-rate control (UCIOS).



(a)



(b)

Fig. 6.14 The relation between ground bounce on the power/ground line and driving current with the UCIONS and UCIOS. (a) The undershoot on $VDDIO_{chip}$ power line and (b) the overshoot on $VSSIO_{chip}$ ground line.

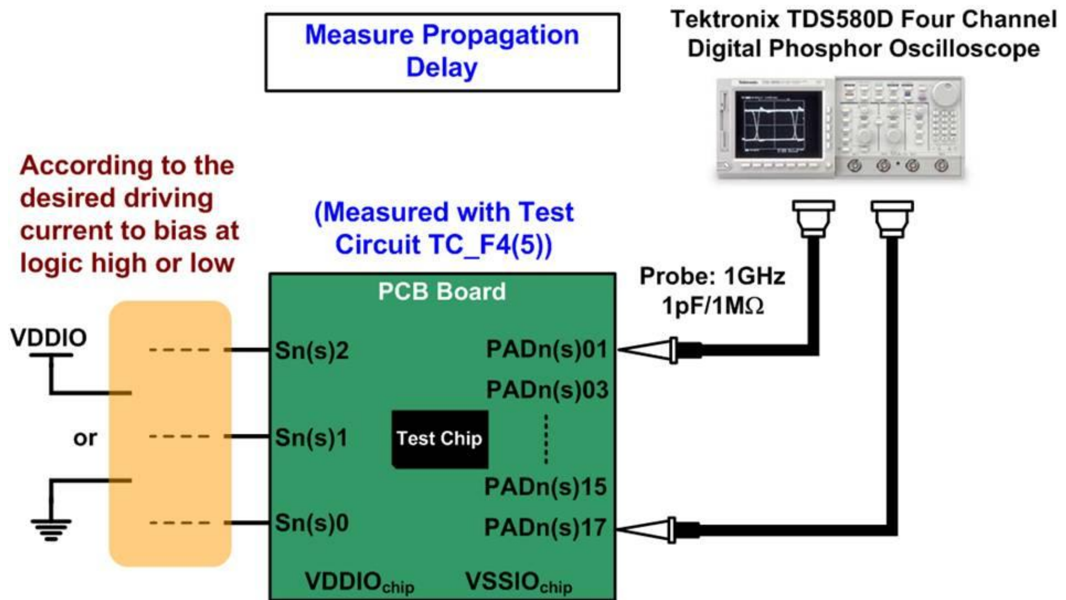
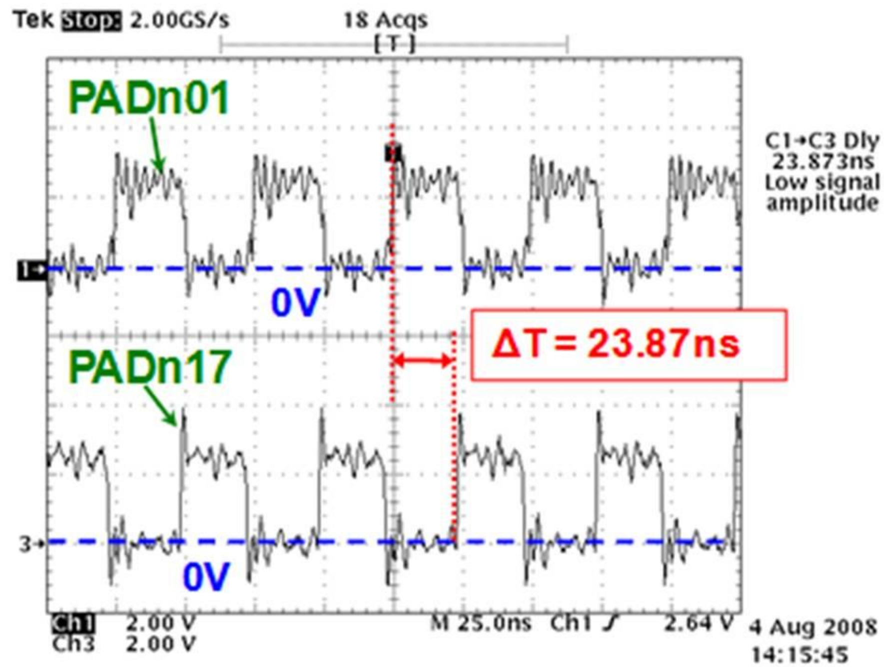
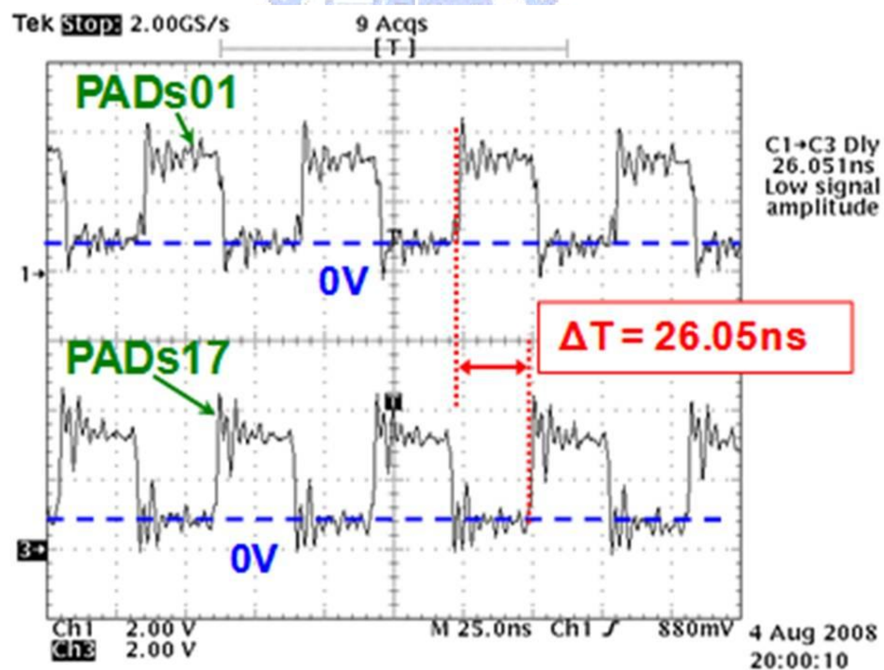


Fig. 6.15 Measurement setup to test the propagation delay of the UCIONS (UCIOS) cell.



(a)



(b)

Fig. 6.16 Measured waveforms to test the propagation delay when the configurable I/O cell operating (a) without slew-rate control (UCIONS) and (b) with slew-rate control (UCIOS) under 2.5-V VDDIO supply voltage.

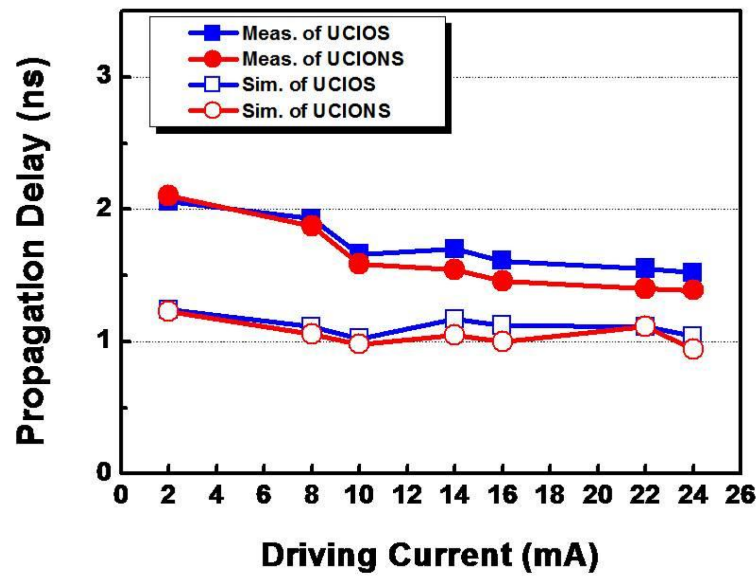


Fig. 6.17 Propagation delay comparison between measurement and simulation results of the propagation delay with 2.5-V VDDIO and different driving current.

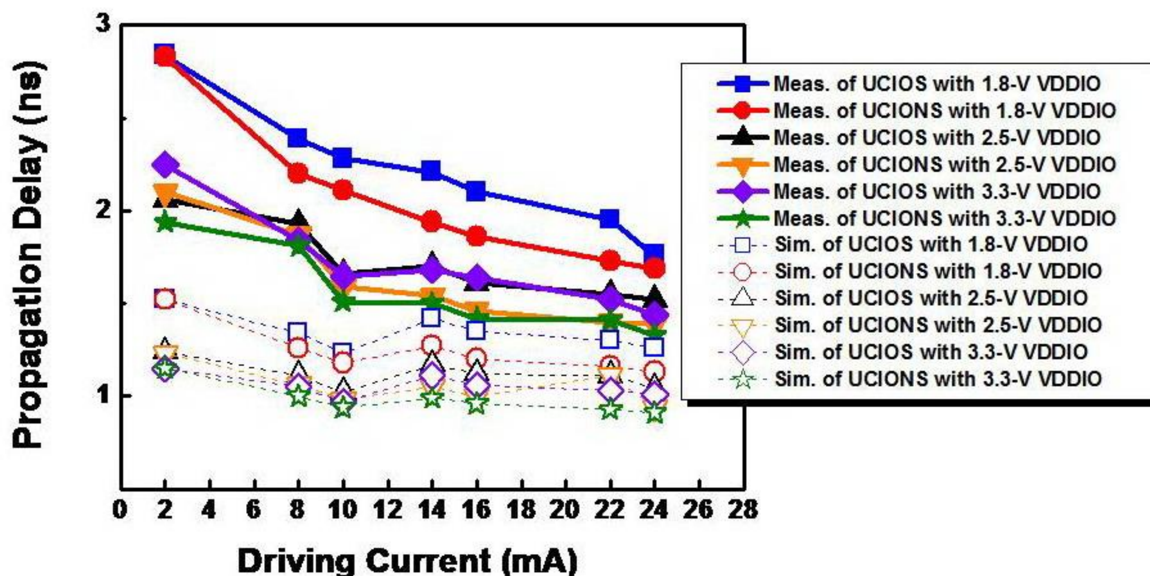


Fig. 6.18 Propagation delay comparison between measurement and simulation results in different driving current and VDDIO supply voltage.

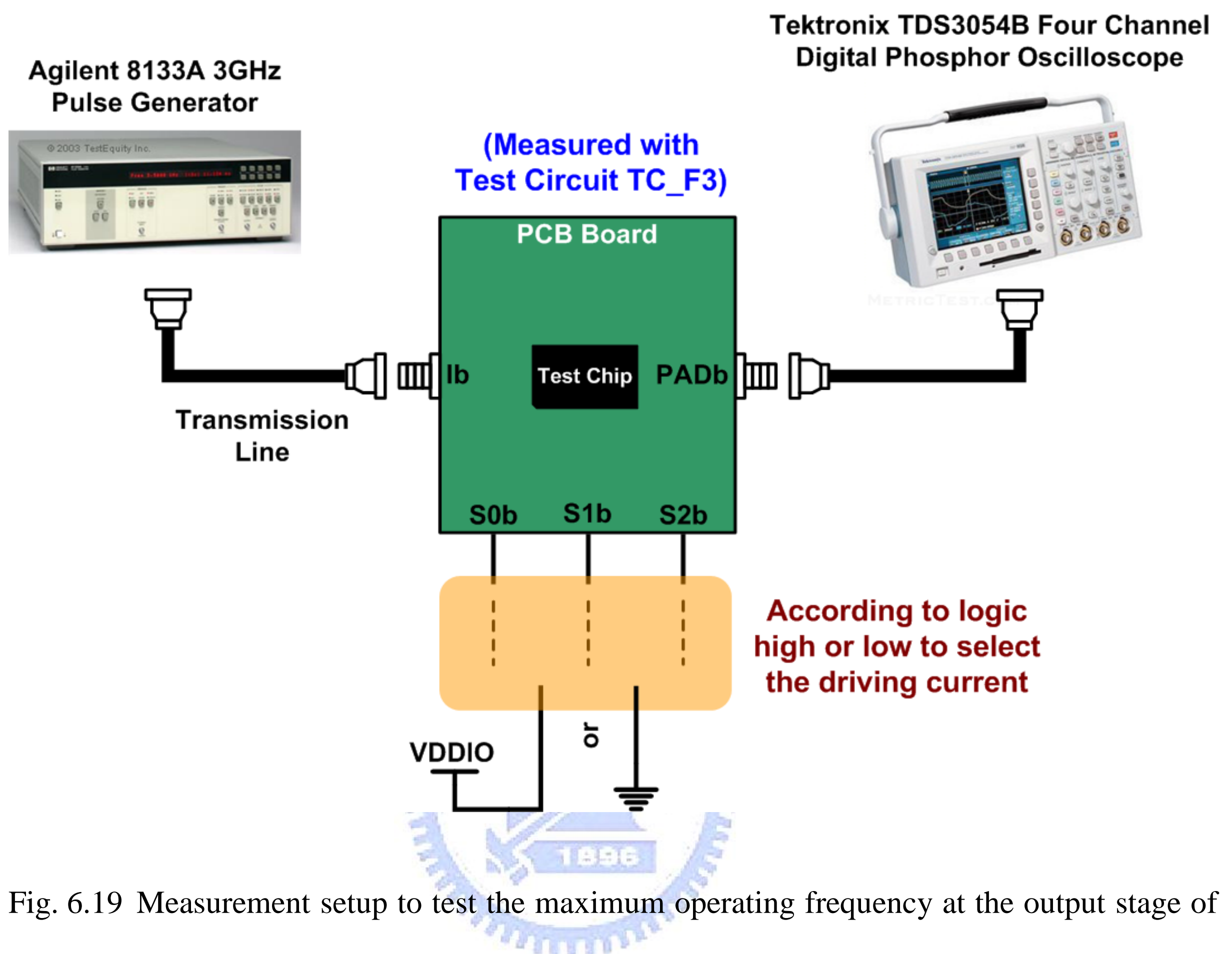
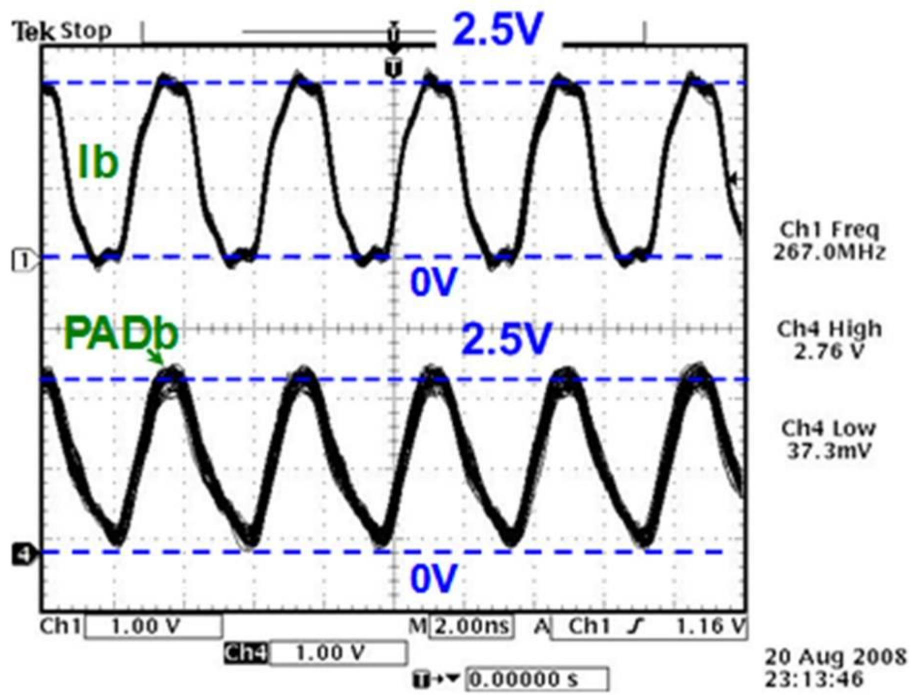
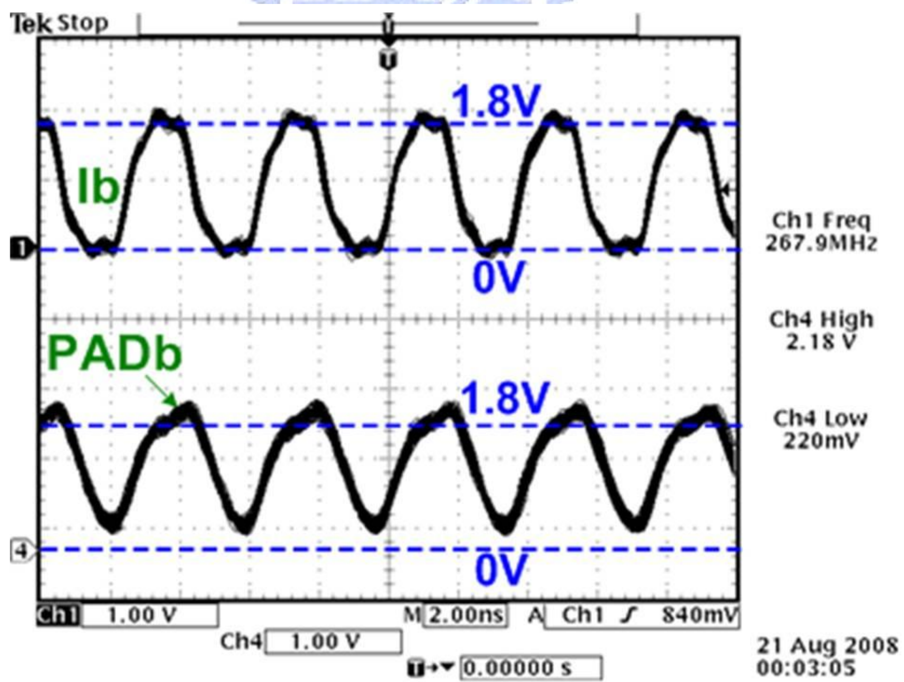


Fig. 6.19 Measurement setup to test the maximum operating frequency at the output stage of the configurable I/O.

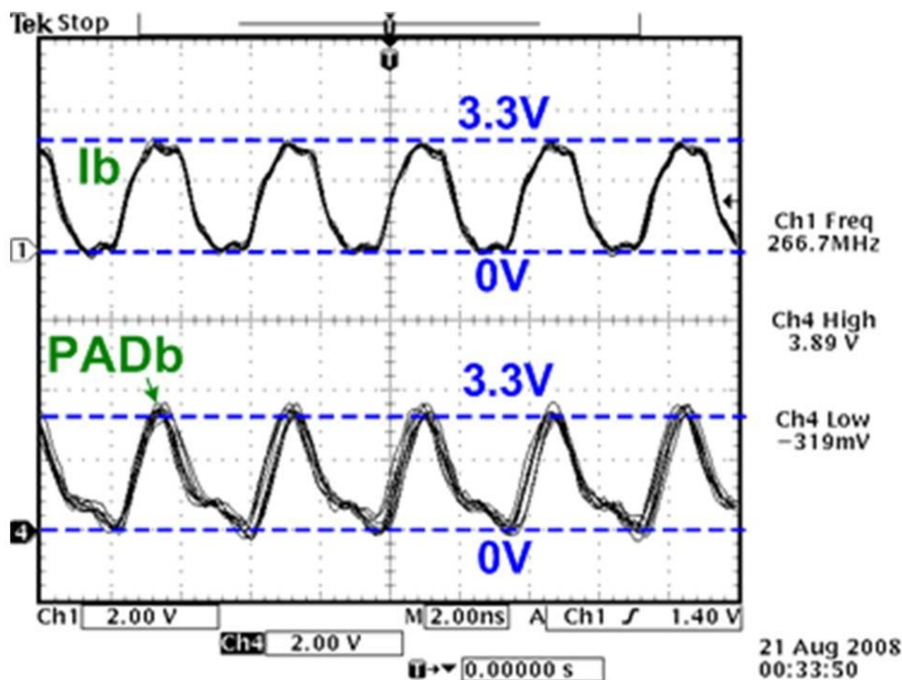


(a)



(b)

(continue to next page, Fig. 6.20)



(c)

Fig. 6.20 Measured waveforms of the configurable I/O cell operating at 266M-Hz operating frequency and 24-mA driving current when receiving 0V-to-VDDIO input signals at pin Ib with (a) 2.5-V, (b) 1.8-V, and (c) 3.3-V VDDIO supply voltage.

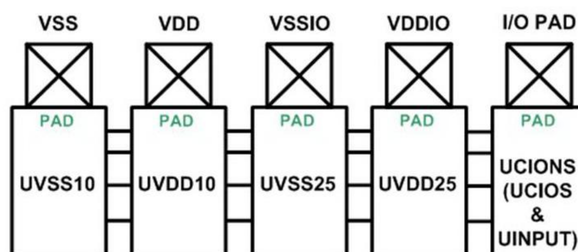


Fig. 6.21 Testkey of configurable I/O cell with whole-chip protection circuit.

Fig. 6.22 Protective extend test of whole-chip protection circuit.

Chapter 7

Conclusions and Future Works

7.1 CONCLUSIONS

In this thesis, a set of configurable I/O cell library has been designed to accelerate the design process to achieve the time-to-market requirement, and has been successfully verified in UMC 90-nm salicide CMOS process. The proposed I/O cell library can be applied in the 1.0-V core power supply voltage, 2.5-V/1.8-V/3.3-V I/O output driver power supply voltage with the operating speed of up to 266MHz. The configurable I/O cell of this library can provide 7 different selective driving currents in transmitting mode, an input stage with or without the function of the schmitt-trigger in receiving mode, and function of the pull-up or pull-down in tri-state. The configurable I/O cell with slew-rate control can effectively reduce the ground bounce effects. Furthermore, each of the ESD protection circuit has been successfully verified its ESD robustness in the test chip. Under the normal circuit operating condition, the I/O cells with the whole-chip protection circuit can be operated correctly. Under the ESD stress conditions, the whole-chip ESD protection circuit can effectively protect the core circuits. Thus, this I/O cell library can be applied in the CMOS ICs inside the microelectronic products successfully.

7.2 FUTURE WORKS

Since the configurable I/O cell is designed with an operating speed of up to 266MHz, the transmission line effect should be considered. Thus, the transmission model should be added into simulation to achieve more accurate results. Beside, the dimensions of ESD protection diodes in the 1.0-V power domain should be enlarged to further improve ESD level of the power break cell.

REFERENCES

[1] T. Furukawa, D. Turner, S. Mittl, M. Maloney, R. Serafin, W. Clark, L. Longenbach, and J. Howard, "Accelerated gate-oxide breakdown in mixed-voltage I/O buffers," in *Proc. IEEE Int. Reliability Physics Symp*., 1997, pp. 169-173.

[2] I.-C. Chen, J. Y. Choi, and C. Hu, "The effect of channel hot-carrier stressing on gate-oxide integrity in MOSFETs," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2253-2258, Dec. 1988.

[3] *ESD Test Standard*, ESD Association, ESD STM5.1, 1998.

[4] A. Wang, *On-Chip ESD Protection for Integrated Circuits*, Boston, Kluwer, 2001.

[5] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, 2nd Edition, John Wiley & Sons, Ltd., England, 2002.

[6] S. Voldman, *ESD Physics and Devices*, John Wiley & Sons, Ltd., England, 2004.

[7] C. Duvvury, R. Rountee, and O. Adams, "Internal chip ESD phenomena beyond the protection circuit," *IEEE Trans. Electron Devices*, vol. 35, no. 12, pp. 2133-2139, Dec. 1988.

[8] C. Johnson, T. J. Maloney, and S. Qawami, "Two unusual HBM ESD failure mechanisms on a mature CMOS process," in *Proc. EOS/ESD Symp*., 1993, pp. 225-231.

[9] V. Puvvada and C. Duvvury, "A simulation study of HBM failure in an internal clock buffer and the design issue for efficient power pin protection strategy," in *Proc. EOS/ESD Symp*., 1998, pp. 104-110.

[10] M.-D. Ker, "Whole-chip ESD protection design with efficient VDD-to-VSS ESD clamp

circuits for submicron CMOS VLSI," *IEEE Trans. Electron Devices*, vol. 46, no. 1, pp. 173-183, Jan. 1999.

[11] F. Garcia, P. Coll, and D. Auvergne, "Design of a slew rate controlled output buffer," in *Proc. IEEE Int. ASIC Conf.*, 1998, pp. 147-150.

[12] M. S. Haydt, R. Owens, and S, Mourad, "Modeling the effect of ground bounce on noise margin," in *Proc. IEEE International Test Conf.*, 1994, pp. 279-285.

[13] B. Deutschmann and T. Ostermann, "CMOS output drivers with reduced ground bounce and electromagnetic emission," in *Proc. European Solid-State Circuits Conf.*, 2003, pp. 537-540.

[14] S. Dabral and T. Maloney, *Basic ESD and I/O Design*, John Wiley & Sons, 1998.

[15] C. Duvvury, C. Diaz, and T. Haddock, "Achieving uniform nMOS device power distribution for submicron ESD reliability," in *Tech. Dig. of IEDM*, 1992, pp. 131-134.

[16] C. Duvvury and C. Diaz, "Dynamic gate coupling of nMOS for efficient output ESD protection," in *Proc. IEEE Int. Reliability Physics Symp.*, 1992, pp. 141-150.

[17] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Syst.*, vol. 4, no. 3, pp. 307-321, Mar. 1996.

[18] J. Chen, A. Amerasekera, and C. Duvvury, "Design methodology and optimization of gate-driven nMOS ESD protection circuits in submicron CMOS processes," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2448-2456, Dec. 1998.

[19] R. Merrill and E. Issaq, "ESD design methodology," in *Proc. EOS/ESD Symp.*, 1993, pp. 233-237.

[20] E. R. Worley, R. Gupta, B. Jones, R. Kjar, C. Nguyen, and M. Teenyson, "Sub-micro chip ESD protection schemes which avoid avalanching junctions," in *Proc. EOS/ESD Symp.*, 1995, pp. 13-20.

[21] T. J. Maloney and W. Kan, "Stacked PMOS clamps for high voltage power supply protection," in *Proc. EOS/ESD Symp.*, 1999, pp. 70-77.

[22] J. Li, R. Gauthier, and E. Rosenbaum, "A compact, timed-shutoff, MOSFET-based power clamp for on-chip ESD protection," in *Proc. EOS/ESD Symp.*, pp. 273-279, 2004.

[23] S. Ramaswamy, C. Duwury, and S.-M. Kang, "EOS/ESD reliability of deep submicron NMOS protection devices," in *Proc. IRPS,* 1995, pp.284-291.

[24] M.-D. Ker, T.-Y. Chen, and T.-H. Tang, "Method of forming a substrate-triggered SCR device in CMOS technology," US patent pending.

[25] M.-D. Ker and W.-Y. Lo, "Methodology on extracting compact layout rules for latchup prevention in deep-submicron bulk CMOS technology," *IEEE Trans. Semiconductor Manufacturing*, vol. 16, no. 2, pp. 319-334, May 2003.

[26] S. Dabral, R. Aslett, and T. Maloney, "Designing on-chip power supply coupling diodes for ESD protection and noise immunity," in *Proc. EOS/ESD Symp.*, 1993, pp. 239-249.

[27] T. Maloney and S. Dabral, "Novel clamp circuits for IC power supply protection," in *Proc. EOS/ESD Symp.*, 1995, pp. 1-12.

[28] M.-D. Ker, C.-Y. Wu, H.-H. Chang, and T.-S. Wu, "Whole-chip ESD protection schme for CMOS mixed-mode IC's in deep-submicron CMOS technology," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1997, pp. 31-34.

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