國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

浮停閘極快閃記憶體之可靠度改善

Study on Reliability Improvement for Nonvolatile Floating Gate Flash Memory

研 究 生：黃國洲　　Guo-Zhou Huang

指導教授：羅正忠　博士　　Dr. Jen-Chung Lou

中 華 民 國 九 十 七 年 八 月

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摘要

非揮發性記憶體的製作，是採用整層的複晶矽的浮停閘(Floating gate)結構，利用此層來當電子的儲存層，當電子由通道注入到這層浮停閘之後，會影響到元件的臨界電壓值(Threshold voltage)，藉由判別臨界電壓的電壓值大小，即可定義邏輯的 “0” 與 “1” 狀態。但是因為這種浮停閘結構為整層的半導體薄膜，在電子反覆的從穿隧氧化層進出這層浮停閘，會使得穿隧氧化層劣化以至於出現缺陷，當缺陷一產生之後，所有儲存的電子將會隨著這層缺陷而有了漏電路徑，導致所寫入的電子全部流失掉，無法達到記憶的效果。然而在不久的將來，會因為成本的考量，將元件尺寸縮小，在尺寸微縮的同時，穿遂氧化層的厚度也會隨之減少，以至於記憶體可靠度不佳。為了應付未來高密度記憶體的需

求，科學家努力研發各種可以取代的非揮發性記憶體如 PCM、FeRAM、MRAM 等…，但沒有人能確定那個種結構可以取代浮停閘記憶體。

如何利用現有的技術，帶領快閃記憶體在繼續的走下去。我們採用了高含氮量氧化層(oxynitride)來代替傳統的熱氧化層當穿隧氧化層，首先把晶片浸泡於雙氧水中，形成化學氧化層 接著在低壓的環境下用氨氣去執行氮化，最後通氧氣來完成氧化動作。如此就可以在介面上形成高氮含量的氧化層，此法製程簡單，跟目前的製程技術是相容的，而且可以提高記憶體的可靠度。

Study on Reliability Improvement for Nonvolatile Floating Gate Flash Memory

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Abstract

Manufacture the nonvolatile memory uses poly-silicon layer treated as election storage layer named floating gate (FG). Electron injection to this layer from channel will influence the threshold voltage. Two states threshold voltage constitute logic “0” and “1”. For FG structure, the oxide has a defect because of electron impact repetitively during the write/erase cycles. Then all of the charge stored in FG layer will be loss. In the near future, the device will be scaling down for the cost. At the same time, the thickness of tunneling oxide will decrease. It causes the reliability of the memory to be worse. In order to deal with demand for high density memory in the future, the scientists make great efforts to research and develop various kinds of nonvolatile memory to replace FG memory. For instance PCM , FeRAM , MRAM ,etc. But nobody can confirm that what kind of structure can replace FG memory.

How can we use existing technology to lead Flash memory continuously scale-down. We use the oxynitride to replace the traditional thermal oxide as the tunneling oxide. First, chemical oxide as a starting oxide can provide a better controllability in film thickness. Following that, the chemical oxide was nitrided using a furnace in low-pressure NH_3 ambient to transfer high-nitrogen oxynitride. The nitrided chemical oxide was then placed in atmospheric O_2 ambient to form a robust oxynitride. The process proposed here is simple and fully compatible with current process technology and improve the reliability of the memory.

致謝

在二年的碩士生涯下，終於完成了碩士論文，這要感謝很多人的幫忙。首先，我要感謝我的指導教授羅正忠博士，讓我學習許多做研究的方法與為人處事的態度。接下來要感謝實驗室的學長姊們，常常關心大家生活狀況的柏村學長、瓊惠學姊，每個星期都會特地來幫大家Meeting 的永裕學長，處理實驗室大小事的智仁學長，還有世璋學長、信智學長、大峰學長、正凱學長、德安學長、忠樂學長、建宏學長、一桀學長、小天學長、阿類學長…，因為你們的教導，使得我能更進步。同學們裡，有做事很有魄力的信富，對朋友超熱心的佳樺，實驗室型男小鄭，直衝博班的冠良，凌晨一起回宿舍的梁文彥，來自高手實驗室的羅正愷，台北三劍客小陸、岳展、嘉宏，晨修…，因為你們，讓這二年的碩士生活更加豐富。實驗室學弟們，侑廷、介銘、翊裳、哲輔，感謝你們在實驗上的幫忙。還有各時期的同學與朋友們，感謝你們的出現，讓我的生活增添了色彩。感謝 NDL 與奈米中心所提供的儀器設備。最後我要感謝我的爸爸黃機博先生、媽媽高梅碧女士，感謝你們這些年來的支持與付出，因為有你們的支持，讓我可以在求學的路途中無後顧之憂的往前邁進。祝大家平安、順利。

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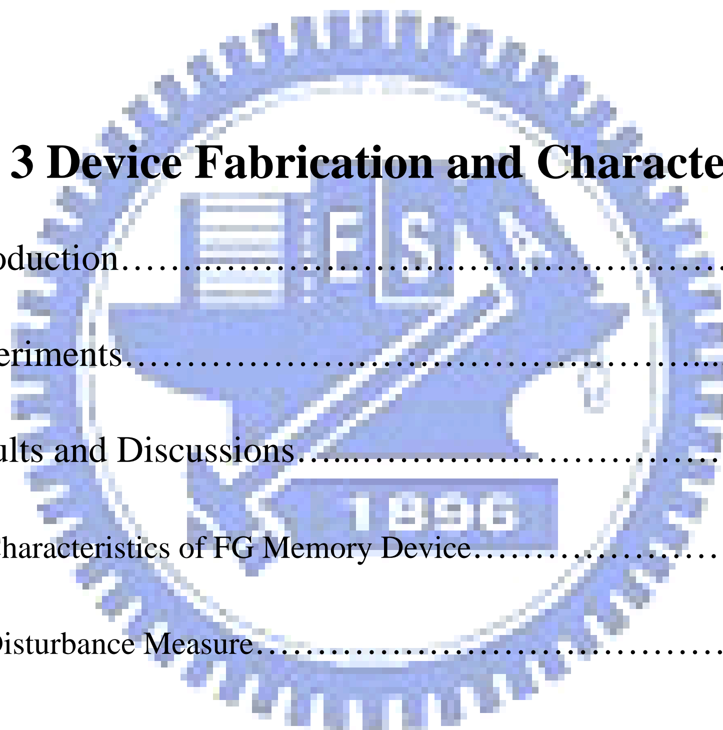

Table Captions

Table 3-1 **The actual thickness of the tunneling oxide.**

Figure Captions

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Fig. 1-3 The charges are stored in the FG

Fig. 1-4 The charges are lost from the tunneling oxide. Then the data will be lost.

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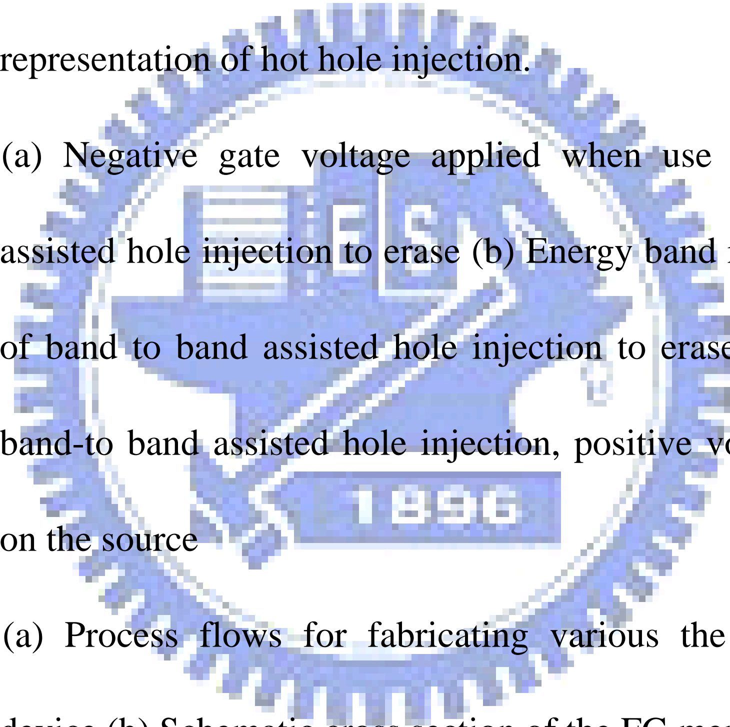
Fig. 3-3 I_D-V_G curves of the FG memory. A memory window about 2.5V can be achieved with programmed V_G = 7V, V_D =6V and erased V_G = -7.7V operation.



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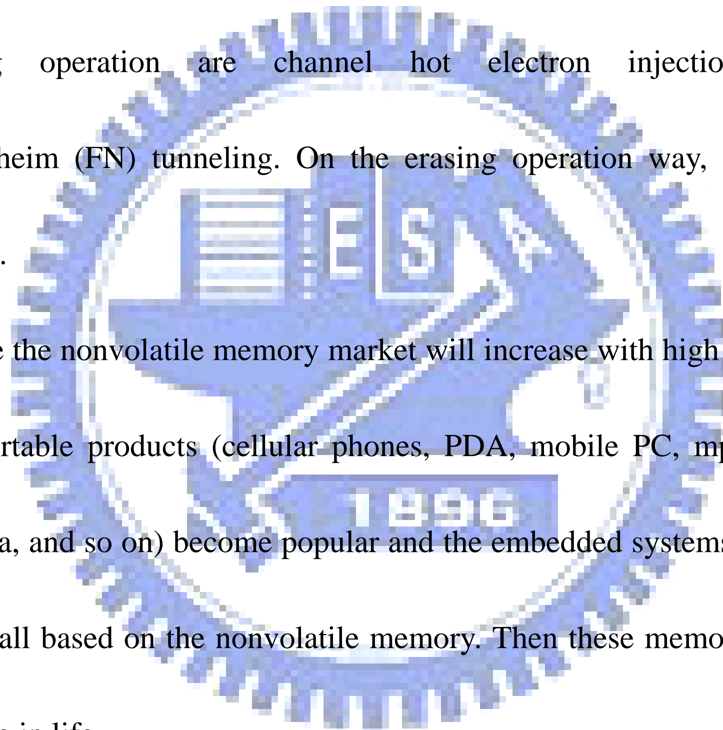
Chapter 1
Introduction

1.1 General Background

In recent years, the semiconductor market has been continuously growing. About 28% of this market is semiconductor memory market in 2007. These memories approximately divided into two categories : random access memories (RAM's) and read-only memories (ROM's). See Fig. 1-1. These two kinds of memories are the most different in data retention. If power turn off, the data will be lost. These memories will be called volatile memories or RAM. The volatile memories are like SRAM and DRAM. These memories have fast speed in programming and reading. RAM is massive applied in computer industry. For ROM's, like EPROM, EEPROM, or Flash, are able to balance the less-aggressive programming and reading performance with nonvolatile character.

In 1967, D. Kahng and S. M. Sze invented the floating-gate (FG) nonvolatile semiconductor memory at Bell Labs [1]. A Flash memory cell is based on a floating-gate MOS transistor (Fig. 1-2). It has a gate completely surrounded by dielectric. The floating gate is electrically governed by a capacitive couple control gate (CG). Fig. 1-2 shows the cross-section of an industry-standard Flash cell. This

cell structure was presented by Intel in 1988 and named ETOX (EPROM Tunnel Oxide). The operation principal is using the poly-silicon layer as FG to storage the charge. After the charge injection into the FG from the channel, the threshold voltage will change. There are two kinds of threshold voltage on memory. The logical “0” and “1” are defined by the difference of threshold voltage. Several physical mechanisms are available to accomplish this charge transfer, but in common use method of programming operation are channel hot electron injection (CHEI) or Fowler-Nordheim (FN) tunneling. On the erasing operation way, FN tunneling is often be used.



In future the nonvolatile memory market will increase with high speed due to the electronic portable products (cellular phones, PDA, mobile PC, mp3 audio player, digital camera, and so on) become popular and the embedded systems develop. These products are all based on the nonvolatile memory. Then these memories will play an important role in life.

1.2 Motivation

FG memory is central memory in the nonvolatile memory market now. As the memory device is scaled down, tunneling oxide thickness will decrease. The thin tunneling oxide had fast program/erase speed. The storage layer is conduction material. If there is a defect chain in the tunneling oxide, the charge that store in the FG layer will flow away through the tunneling oxide. See Fig. 1-3, Fig. 1-4. The date will be lost. This signal is an error. When tunneling oxide thickness is continuously scaled down, the reliability of memory will be decreased. Then, there are a lot of structure of the memories be published to replace the FG memory, such as SONOS, nanocrystal memory, FeRAM [2], MRAM [3], phase change memory (PCM) [4], and so on. But what kind of memory will replace the FG memory device, no one know the answer.

We will improve the tunneling oxide, let the FG memory can scale down continuously. We use the oxynitride (SiON) to replace the conventional dry oxide to improve reliability of the tunneling oxide on the FG memory.

1.3 Organization of the thesis

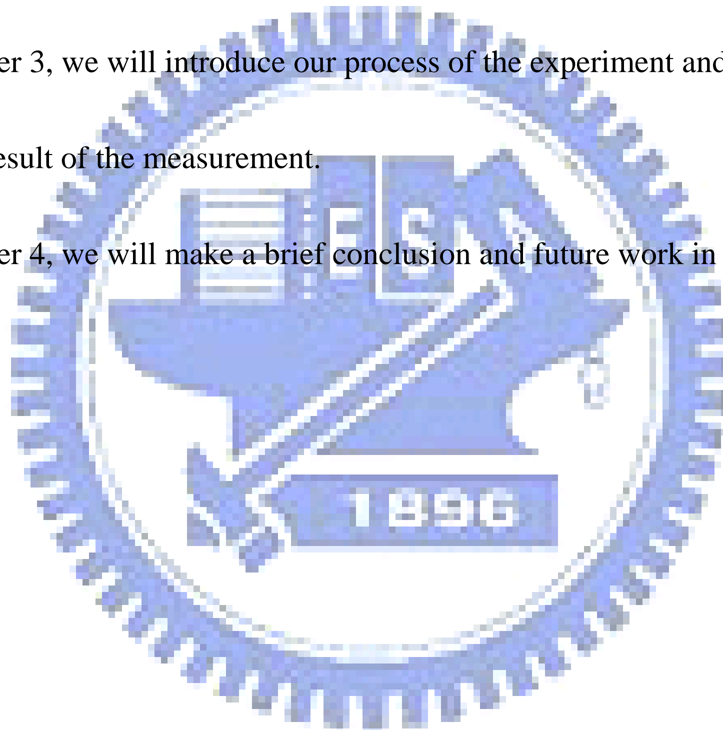
This thesis can be divided into four parts. The detail contents in each chapter are described as follow.

In chapter 1, we introduce the memory market and memory type, and then we speak our motivation.

In chapter 2, we will introduce the basic principles of flash memory device.

In chapter 3, we will introduce our process of the experiment and discuss and analyze the result of the measurement.

In chapter 4, we will make a brief conclusion and future work in the last chapter.



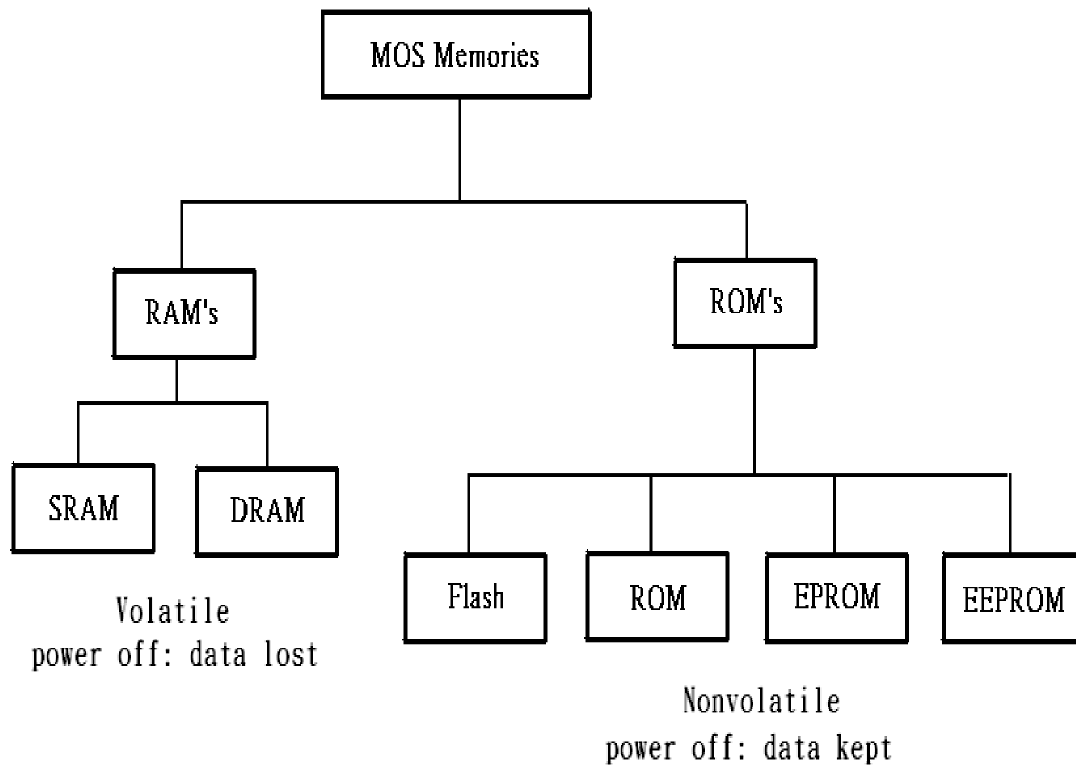


Fig. 1-1 MOS Memory tree

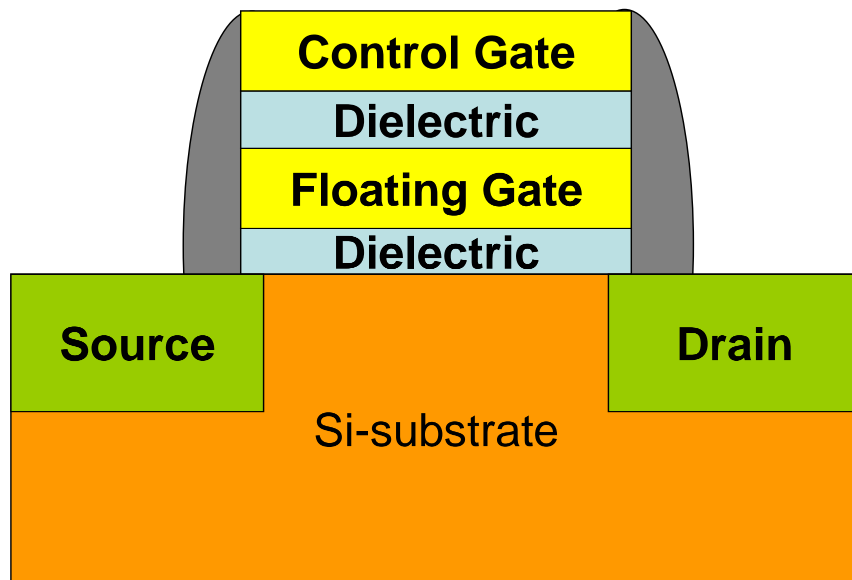
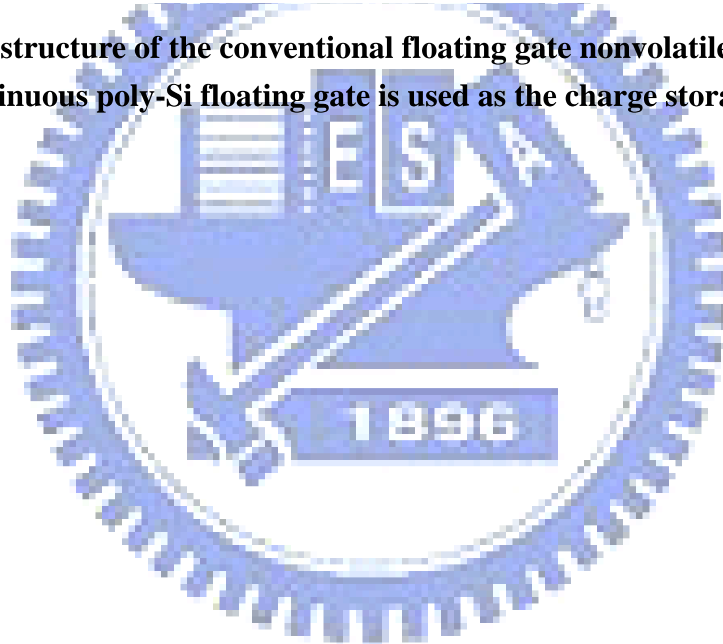


Fig. 1-2 The structure of the conventional floating gate nonvolatile memory device. Continuous poly-Si floating gate is used as the charge storage element.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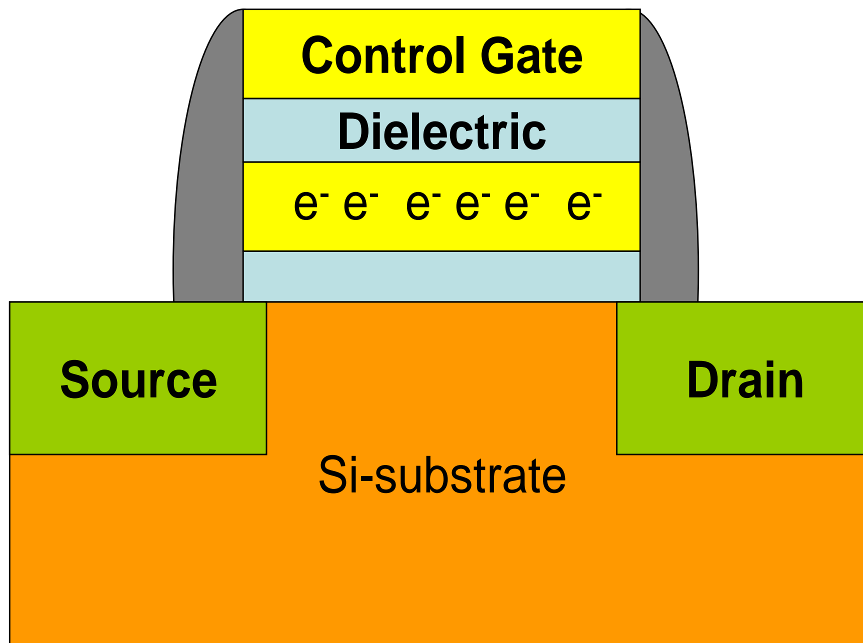


Fig. 1-3 The charges are stored in the FG.

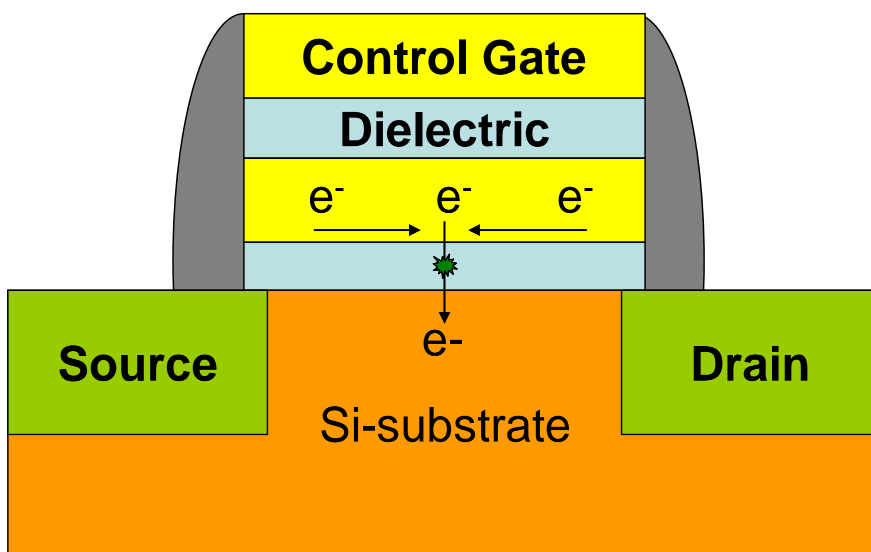


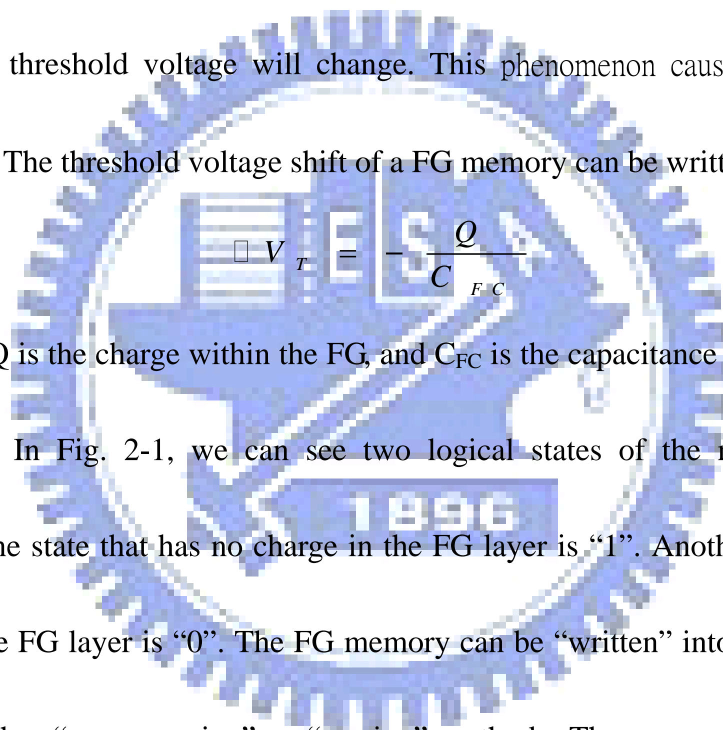
Fig. 1-4 The charges are lost from the tunneling oxide. Then the data will be lost.

Chapter2

Basics Principle of Nonvolatile Memory

2.1 Introduction

Novel nonvolatile memories, such as SONOS and nanocrystal memories are based on the concept of floating gate memory. If the data store in the FG layer of the memory, the threshold voltage will change. This phenomenon causes the threshold voltage shift. The threshold voltage shift of a FG memory can be written as [5] [6]:



$$\Delta V_T = -\frac{Q}{C_{FC}}$$

Where Q is the charge within the FG, and C_{FC} is the capacitance between FG and control gate. In Fig. 2-1, we can see two logical states of the memory reading operation. One state that has no charge in the FG layer is “1”. Another state that has charges in the FG layer is “0”. The FG memory can be “written” into either state “0” or “1” by either “programming” or “erasing” methods. There are many methods to achieve “programming” or “erasing”.

It is necessary to have good “programming” and “erasing” ability in the memory. In Fig. 2-2, C_{FC} , C_S, C_B, and C_D are the capacitance between FG and control gate, source, bulk regions and drain, respectively. The total capacitance C_1 between FG and substrate can be written as:

$$C_S + C_B + C_D = C_1$$

If C_{FC}>>C_1, V_{FG} will have higher potential. High potential can help the more electrons inject into FG layer. So we can add C_{FC} to increase "programming" and "erasing" ability.

In this chapter, we will discuss programming and erasing mechanisms from relation between bias and energy band bending. Fowler-Nordheim tunneling, hot electron injection, band to band assisted holes injection, channel holes injection will be discussed. In addition to programming and erasing mechanisms, we also discuss the reliability.

2.2 Basic Program Mechanisms

2.2.1 Fowler-Nordheim tunneling

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism [7], when a large positive voltage is applied across a FG transistor, its band structure will be influenced as indicated in fig. 2-3. Due to high electrical field, the tunneling oxide barrier will become triangular energy barrier. As sufficient high field, the width of barrier becomes small enough to tunnel through the barrier from the Si-substrate conduction band into FG layer.

2.2.2 Hot Electron Injection

At large drain bias, the minority carriers that flow in the channel are heated by the large electric field occurred at the drain side of the channel and their energy distribution is shifted higher. This phenomenon gives rise to impact ionization at the drain, by which both minority and majority carriers are generated. The highly energetic majority carriers are normally collected at the substrate contact and from the so-called substrate current. The minority carries heating occurs when some of the minority carries gain enough energy to allow them to surmount the SiO_2 energy barrier. If the oxide field favors injection, these carriers injected over the barrier into the gate insulator and give rise to the so-called hot-carrier injection gate current [8] [9]. Fig. 2-4 shows the phenomenon of hot injection. This mechanism is schematically represented for the case of an n-channel nonvolatile memory. In Mos devices, the drain voltage should increase beyond the saturation voltage V_{dsat} ($V_d > V_{dsat}$) the mode can named hoe carrier effect. To distinguish from Fowler-Nordheim tunneling the definition of hot carrier injected in this study is the only condition that the drain is applied bias.

2.3 Basic Erases Mechanisms

2.3.1 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling is a field-assisted carrier tunneling mechanism,

when a large negative voltage is applied across a FG transistor, its band structure will be influenced as indicated in fig. 2-5. Due to high electrical field, the tunneling oxide barrier will become triangular energy barrier. As sufficient high field, the width of barrier becomes small enough to let holes tunnel through the barrier from the Si-substrate valance band into FG layer, or electron can tunnel through the barrier from the FG layer into Si-substrate conduction band.

2.3.2 Hot Hole Injection

The mechanism of hot hole injection in p-channel is like to hot electron injection. Fig.2-6 (a) shows the phenomenon of hot injection. It's reported that hole injection is an erase operation in p-channel devices [10].

2.3.3 Band to Band Assisted Hole Injection

Fig. 2-7 shows the phenomenon of band to band assisted holes injection. In N-channel, when a negative gate voltage and a positive drain voltage are applied to the cell, electron-hole pairs are generated by BTBT in the drain region [11] [12]. The holes are accelerated by a lateral electric field toward the channel region and some of them obtain high energy. The injection of such hot holes [13], into FG layer through the tunneling oxide is used for a new erase operation in N-channel. Another hot hole injection method is applied a positive voltage on source, in Fig. 2-7(c).

2.4 Basic Reliability of Nonvolatile Memory

For a nonvolatile memory, the important concern is distinguishing the state in cell. However, in many times operation and charges storage for a long term, the state is not obvious with charges loss. Endurance and retention experiments are performed to investigate Flash-cell reliability.

2.4.1 Retention

Any nonvolatile memory technology, Flash memory are specified to retain data for over ten years. This means the loss of charge stored in the memory must be as minimal as possible. In updated Flash technology, due to the small cell size, the capacitance is very small and an operative programmed threshold voltage shift of 2V corresponds a number of electrons in the order of $10^3$to 10^4. A loss of 20% in this number (around 2-20 electron lost per month) can lead to a wrong read of the cell and then to a data loss. Possible causes of charge loss are: 1) defects in the tunneling oxide; 2) defects in the interpoly dielectric; 3) mobile ion contamination; 4) detrapping of charge from insulating layers surrounding the FG [14].

2.4.2 Endurance

Flash products are specified for 10^5 write/erase cycles. Cycling is known to cause a fairly uniform wear-out of cell performance, mainly due to the tunnel oxide degradation, which eventually limits the endurance characteristics. The oxide defect

will increase stress induce leakage current (SILC), that let electrons store in memory will be lost. Threshold voltage gradually recovery the initial value that before writing, the memory window will be close. Data retention after cycling is the issue that definitely limits the tunneling oxide thickness scaling. For very thin oxide, below 8-9nm, the number of leaky cells becomes so large that even error-correction techniques cannot fix the problem.

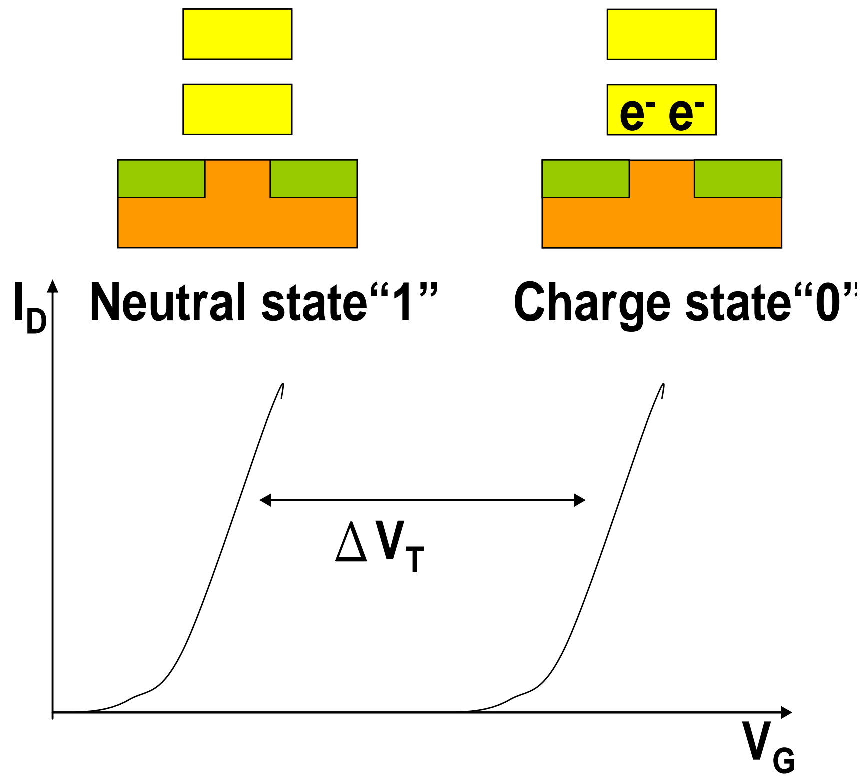
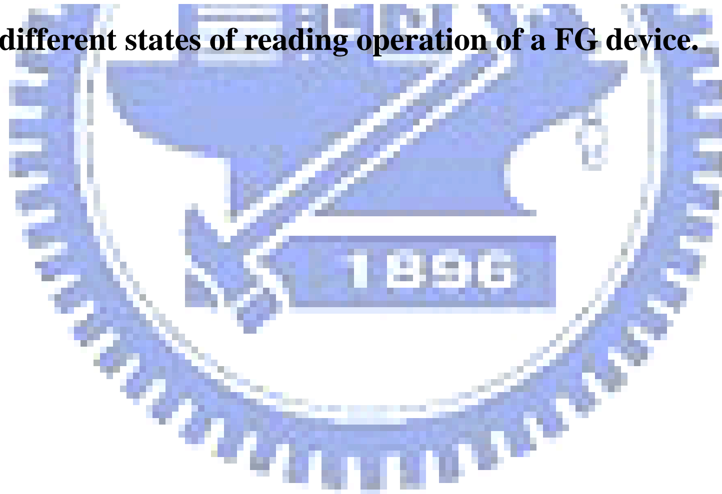
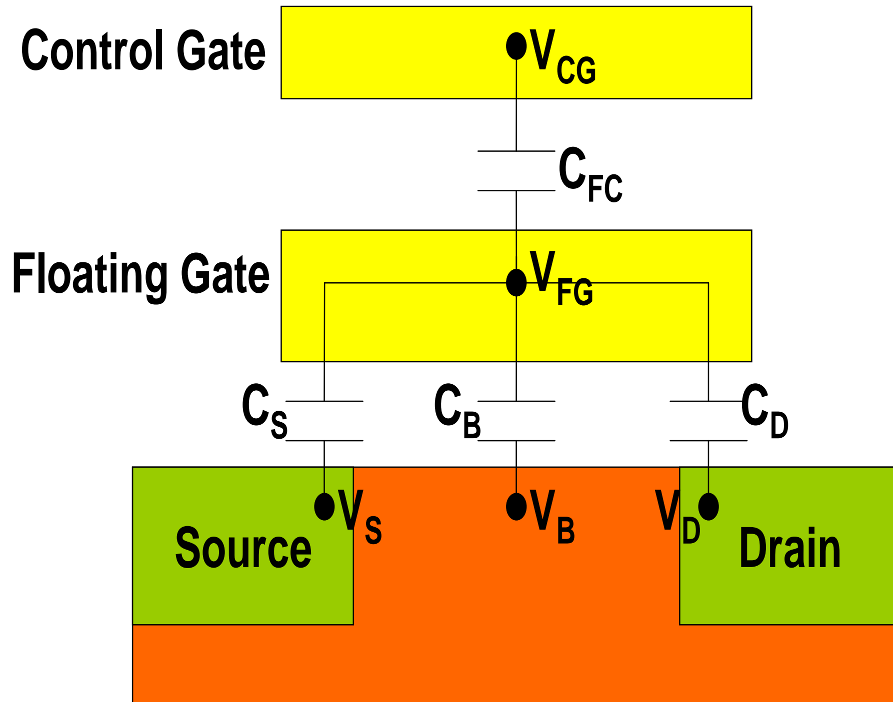


Fig. 2-1 The different states of reading operation of a FG device.





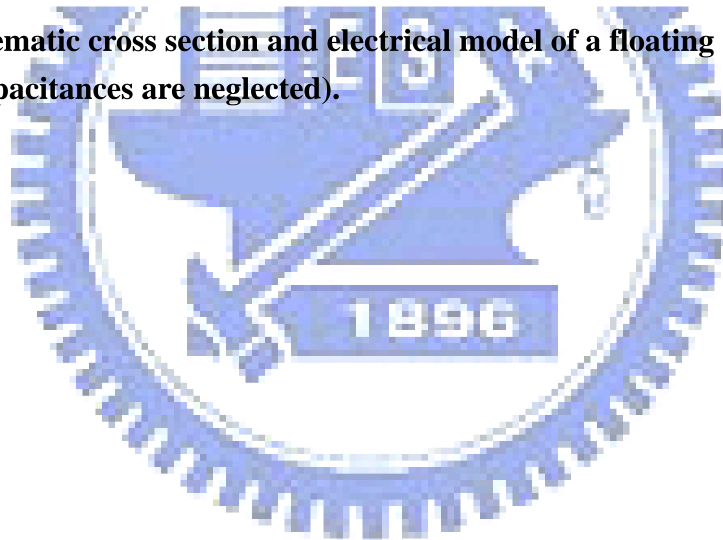
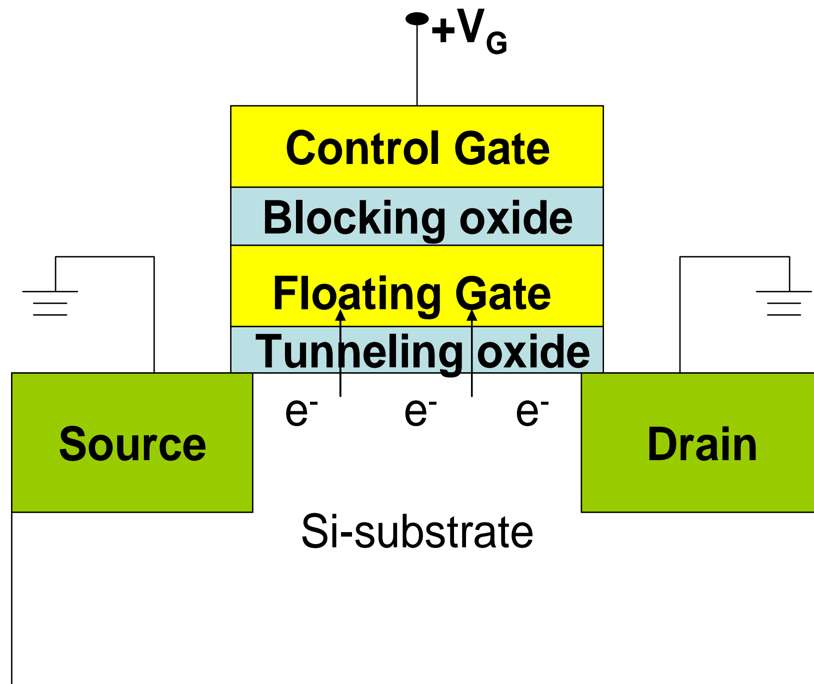
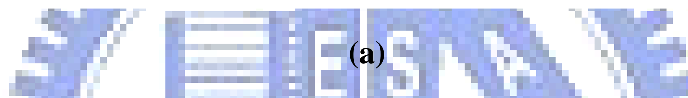


Fig. 2-2 Schematic cross section and electrical model of a floating gate device (junction capacitances are neglected).





(a)

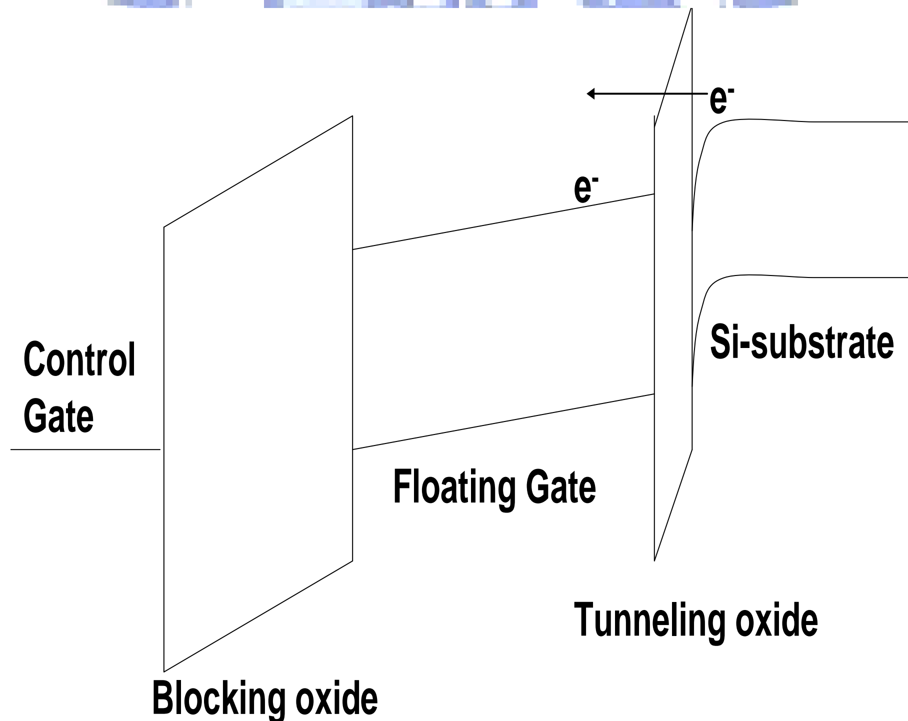


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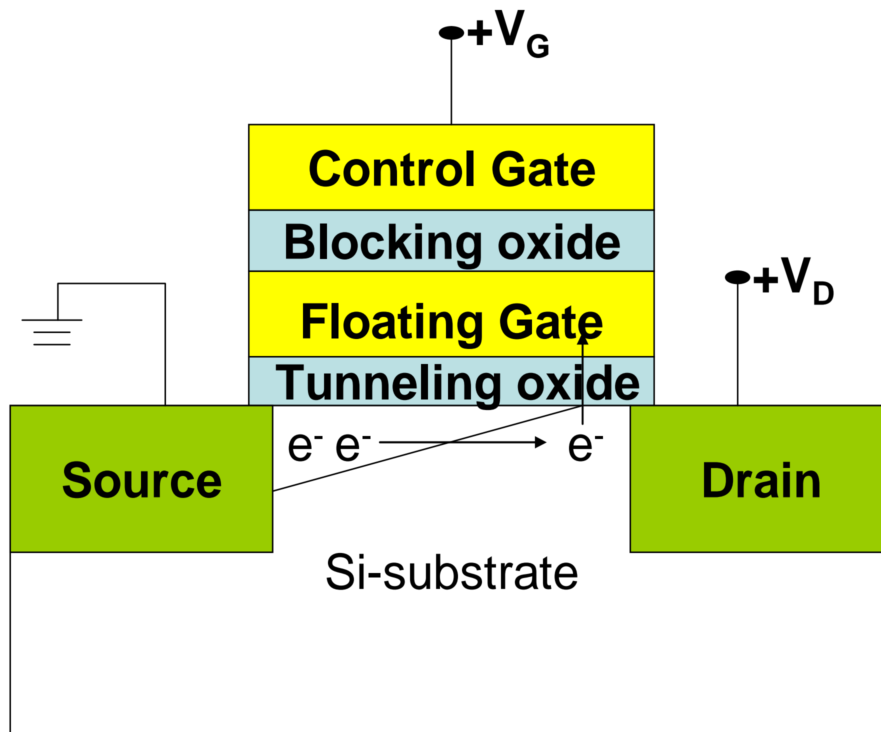
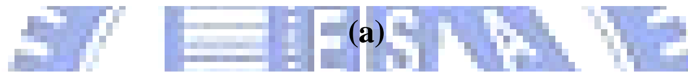
Fig. 2-3 (a) Positive voltage applied on the gate when use Fowler-Nordheim tunneling to program (b) Energy band representation of Fowler-Nordheim tunneling . Electron in Si-subtrate conduction band tunneling into the Floating Gate.





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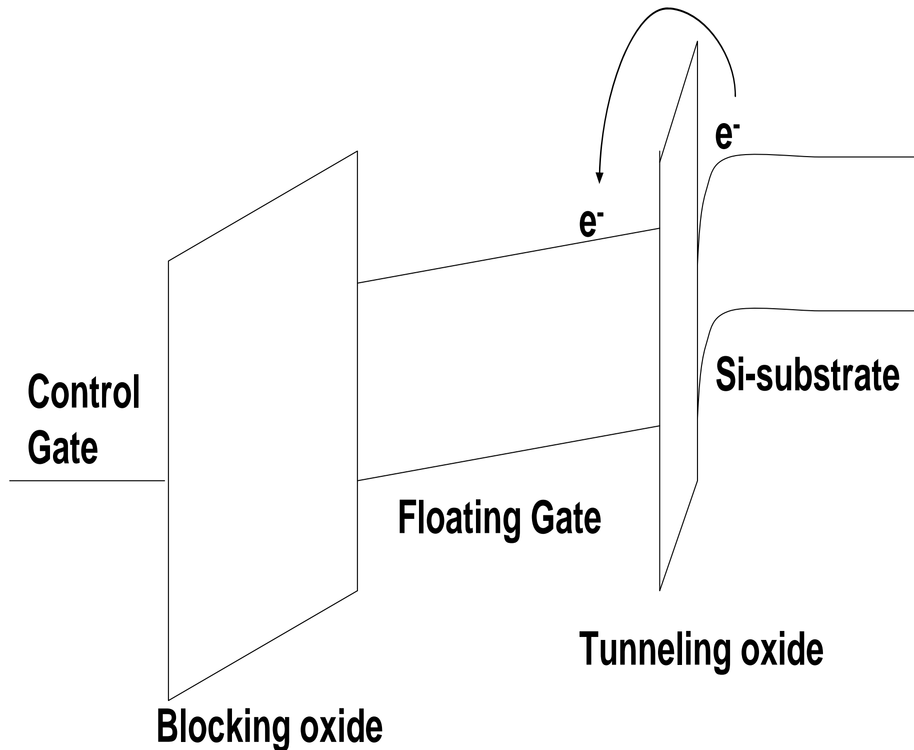

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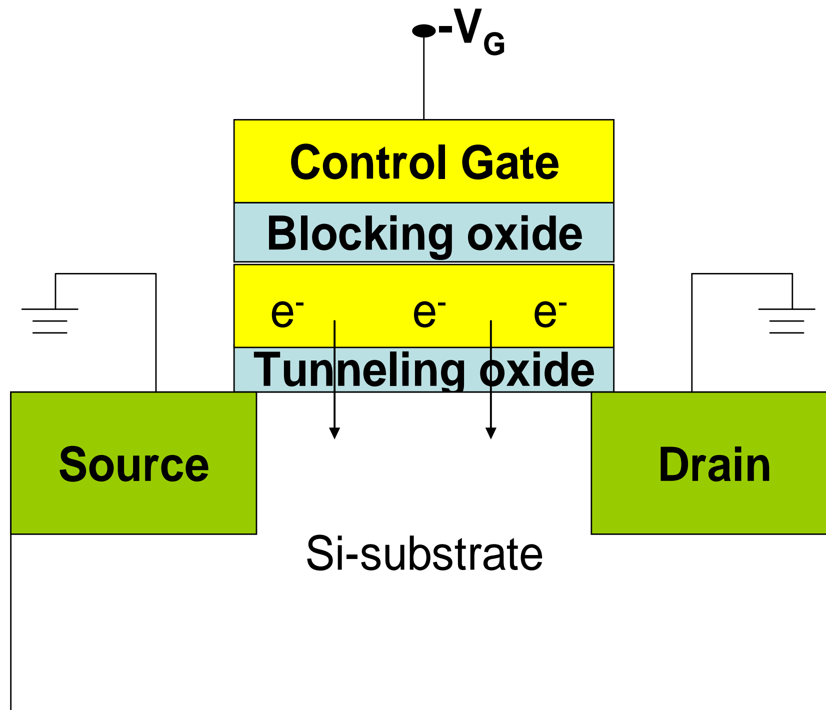
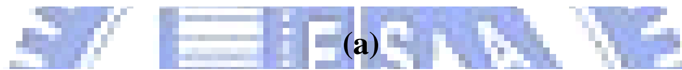
Fig. 2-4 (a) Positive gate voltage and positive grain voltage applied when use hot carrier injection to program. (b) Energy band representation of hot carrier injection.





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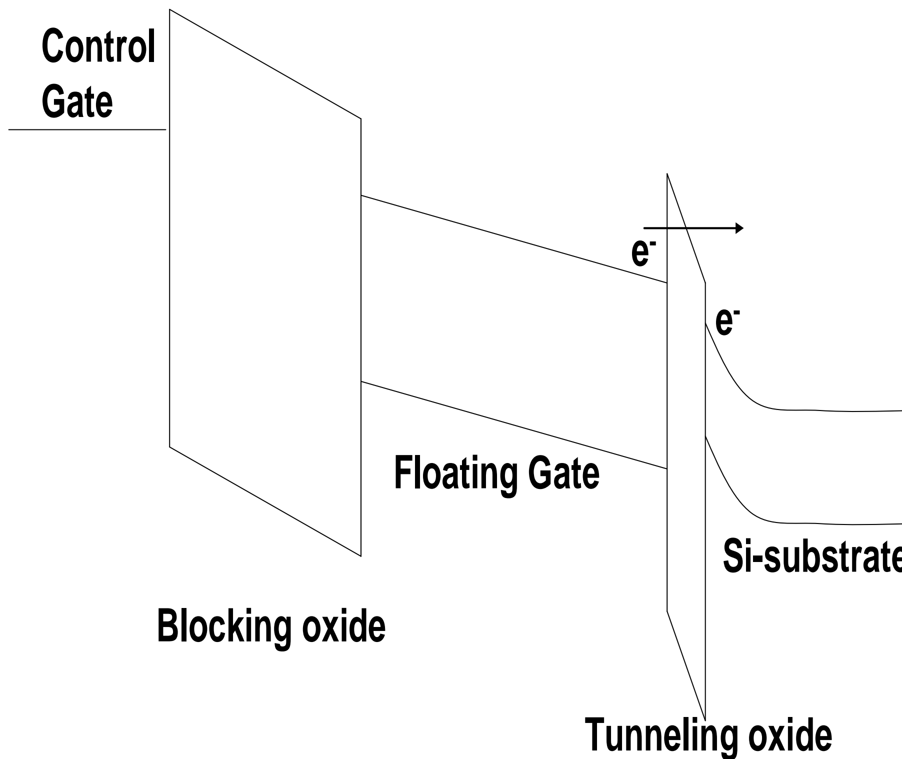
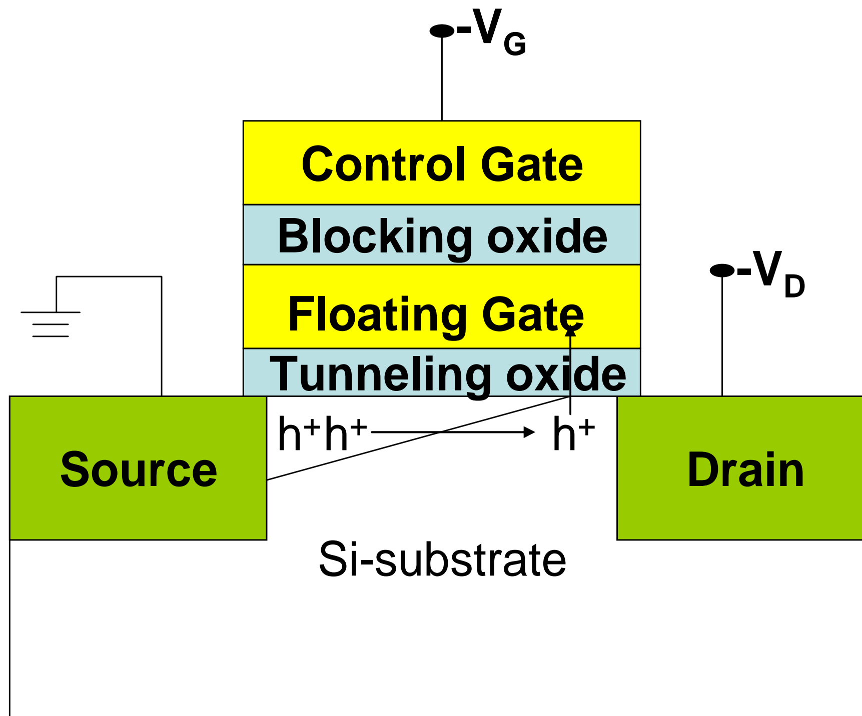
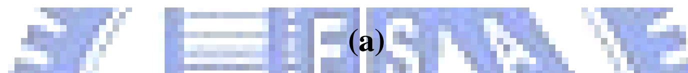


(b)

Fig. 2-5 (a) Negative voltage applied on the gate when use Fowler-Nordheim tunneling to erase (b) Energy band representation of Fowler-Nordheim tunneling . Electron in Floating Gate tunneling into the Si-subtrate conduction band





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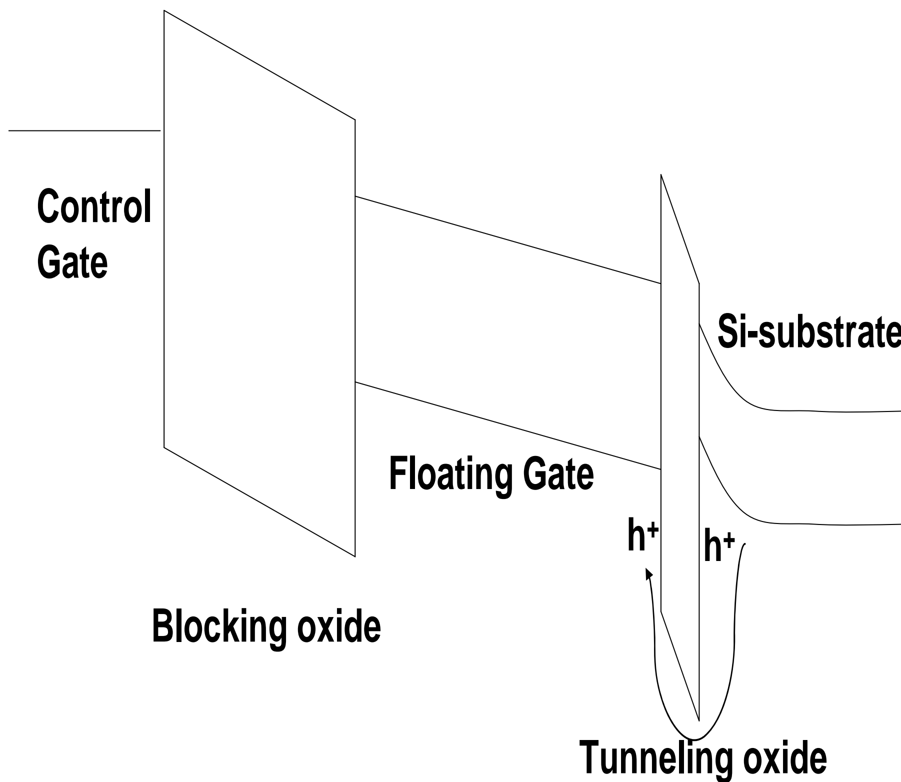

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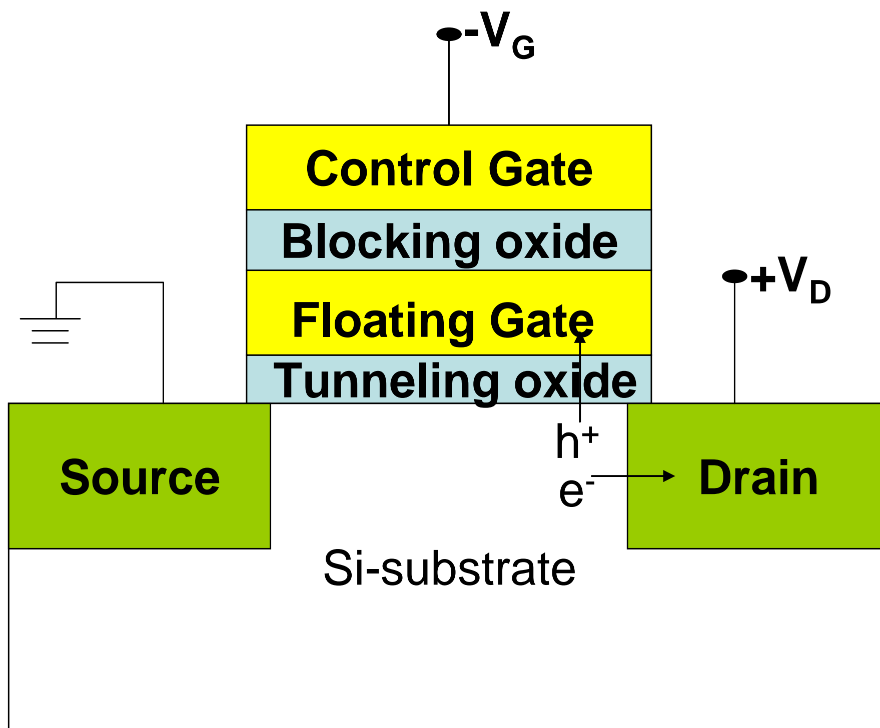
Fig. 2-6 (a) Negative gate voltage and negative grain voltage applied when use hot hole injection to erase. (b) Energy band representation of hot hole injection.



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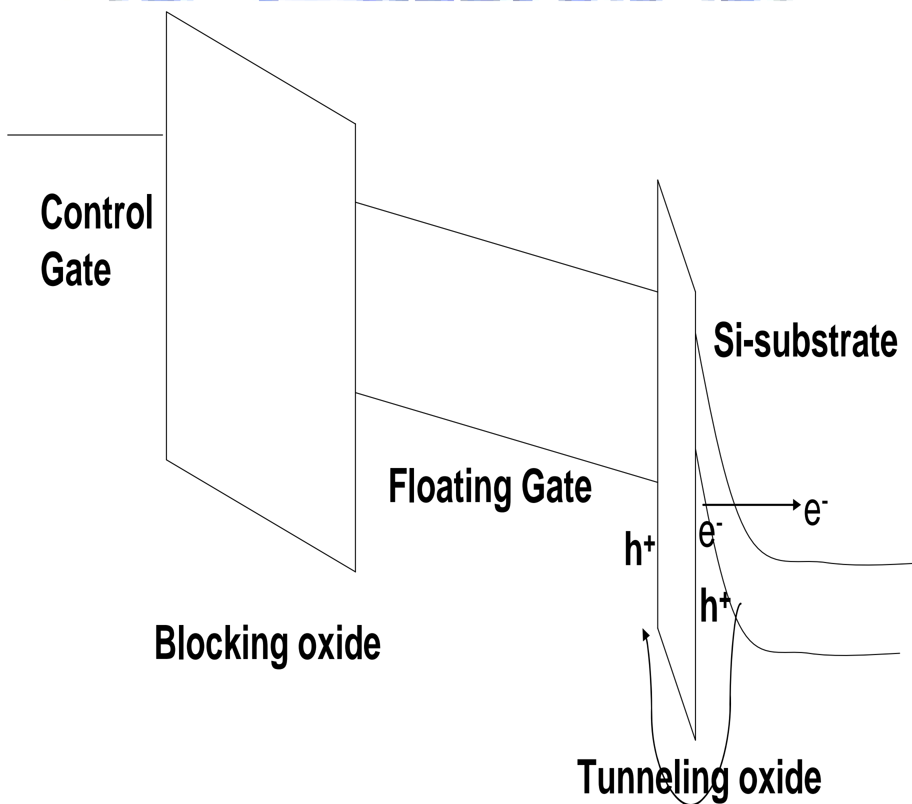


(b)

Fig. 2-7 (a) Negative gate voltage applied when use band-to band assisted hole injection to erase (b) Energy band representation of band to band assisted hole injection to erase.

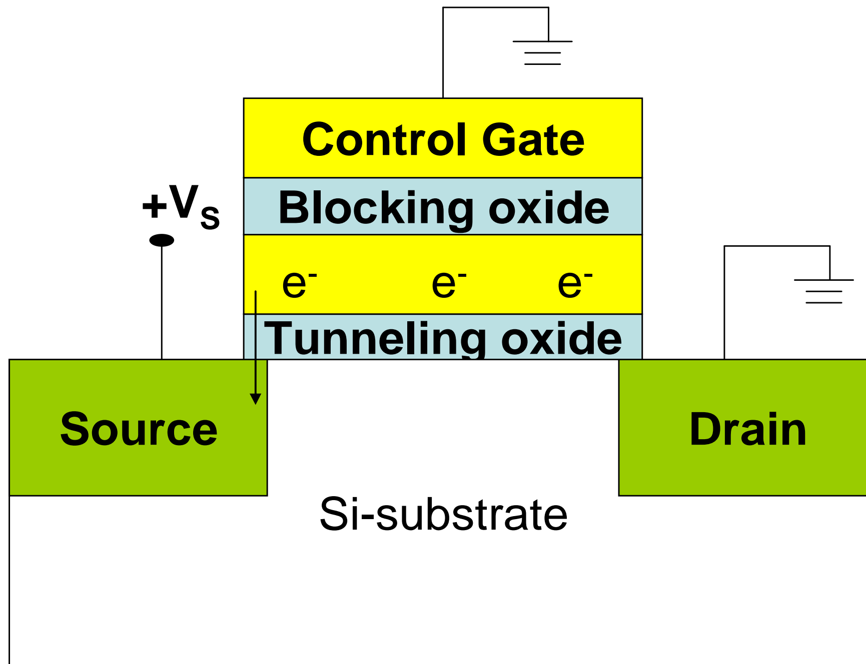


Fig. 2-7 (c) Another band-to band assisted hole injection, positive voltage applied on the source.

Chapter 3
Device Fabrication and Characterization

3.1 Introduction

When the FG device is scaling down, tunneling oxide thickness will be decrease. It can let FG memory increase write/erase speed and decrease the operation voltage, but the data retention will be worse. So the main challenging of the FG memory is reliability as device scaling down. Although there are many structure of the memory be published to replace the FG memory, but the technology of the other memory structure is not enough mature to manufacture. Such as nanocrystal memory device, nanocrystal size and density will influence electron trapped capability. But we can not accurately control the nanocrystal size and density. In the SONOS memory way, the memory has leakage problem, so they can not be manufacture. No one known that what kind of memory structure can replace FG memory device. So we tried to solve the problem let FG memory can be continuously scaled down.

In order to scale down FG memories, we use the oxynitride film to replace the conventional thermal oxide. The oxynitride film has the small charge trapping amount and low stress-induced leakage current [15] [16]. In the oxynitride, we can obtain Si – rich at the bottom and N – rich at the top. The nitrogen accumulates at the oxynitride

surface to reduce the concentration of strained Si – O band and the creation of hot electrons as many as three orders of magnitude. Thinner oxynitride films are preferred in ULSI technology.

In this chapter, we proposed a novel approach for forming an oxynitride tunneling dielectric with high nitrogen content and applied in FG memory. Then we will compare characteristics of oxynitride and thermal oxide for tunneling oxide in FG memory.

3.2 Experiments

Fig. 3-1 schematically describes the process flow of the FG memory. The fabrication process of this memory device was started with LOCOS isolation process on a p-type, 5-10 Ω・cm, (100) 150 nm silicon substrate. We dipped in HF about seven minutes to remove the sacrificial oxide layer. Then standard RCA clean was used to remove organic, particle and metal contamination. First we grow oxynitride layer. At the oxynitride growth step, first we dipped into H_2O_2 solution at room temperature in 20 minutes to grow 1 nm chemical oxide. Then we use a furnace in low - pressure (l20 mTorr) NH_3 ambient at 780℃ about 15 minutes, let the chemical oxide was nitrided. The nitrided chemical oxide was placed in atmospheric O_2 ambient at 923℃ to form the oxynitride. We respectively grew 5 nm, 7nm oxynitride and 7nm Dry oxide to compare

their electrical characteristics. Now the tunneling oxide is completed. After completed tunneling oxide layer, we deposited 80 nm poly-Si by low pressure chemical vapor deposition (LPCVD). Then FG implant, rapid thermal anneal (RTA) was performed at 950 ℃ for 20 sec in N_2 ambient to activate dopants. We deposited 15 nm TEOS as blocking oxide by low pressure chemical vapor deposition (LPCVD). Final we deposited 200nm poly-Si. Subsequently, gate electrode was defined by I-line lithography stepper and etched by RIE etching system. To continue patterning and S/D implant. Then, rapid thermal anneal (RTA) was performed at 950℃ for 20 sec in N_2 ambient to activate dopants. Afterwards, TEOS capping layer (500nm) was deposited by low pressure chemical vapor deposition (LPCVD). Subsequently I-line lithography stepper and RIE used to define contact hole. Al-Si-Cu (900nm) metallization were sputtered by PVD system. Subsequently I-line lithography stepper and metal etcher used to define metal pattern.

3.3 Results and Discussions

In this thesis, all devices described had dimensions of L/W = 1/10 μm, and the threshold voltage is defined when the I_D current reach 10^{-7} A in I_D-V_G curves. If it don't show temperature, that means room temperature (T=25℃). The Table 3-1 shows the actual thickness of the tunneling oxide of the FG memory.

3.3.1 Characteristics of FG Memory Device

In Fig. 3-2, we show the I_D-V_D curve and I_D-V_G curve of the FG memory device to confirm that the device can be used. We use channel hot-electron (CHE) injection to program and Folwer-Nordheim tunneling (FN tunneling) to erase. The programming and erase time are both 10ms, and window of about 2.5V can be clearly observed in Fig. 3-3. During programming, a small fraction of electrons in the substrate obtain enough energy from applied to V_D surmount the barrier between oxide and silicon conduction band edges. These electrons can be trapped in the FG layer and threshold voltage shift to right. When erasing, we applied a negative gate voltage to generate FN tunneling to erase these electron in the FG layer. It reduces the threshold voltage and causes the I_D-V_G curve shift to left. We use this mechanism of adjust threshold voltage by different applied voltages to obtain memory characteristics.

In Fig. 3-4, we show the change of threshold voltage with different temperature. We can find that the threshold voltage decrease as temperature increase. Because at high temperature lattice oscillation create a lot of electron hole pair. The threshold voltage will be decreased.

The "$\triangle V_t$" is defined as threshold voltage difference between the program state or erase state. The program speed is shown in Fig. 3-5. Gate and drain terminals

were biased equally from 5 to 8V. Both source and substrate terminals were biased at 0V. As shown in Fig. 3-5 (a) (b) (c), program characteristics as a function of pulse width. With V_G and V_D increasing, the V_{th} shift increase and the program speed becomes faster. Then in Fig. 3-5 (d) shows that program characteristics as a function of pulse width and the thin tunneling oxide will have fast program speed. But we can see that the 5nm oxynitride is not faster a lot than others. Because we use CHE injection to program then the CHE was influenced by barrier high. In erasing way, we choose to use FN tunneling. The erase speed is shown in Fig. 3-6. Gate terminal was biased from -5 to -8V. The source, drain, and substrate terminals were biased at 0V. As shown in Fig. 3-6 (a) (b) (c), erase characteristics as a function of pulse width. With $|V_G|$ increasing, the V_{th} shift increase and the erase speed becomes faster. Then in Fig. 3-6 (d) shows that erase characteristics as a function of pulse width and the thin tunneling oxide will have fast erase speed. Because we use FN tunneling to erase, the thin tunneling oxide have fast erase speed was obvious.

Fig. 3-7 shows the retention characteristics of FG memory device. We let the memory windows about 2.55V, then measure the retention. We can find that FG memory devices have good retention ability even if the thickness of the tunneling oxide reduces to 5nm in Fig. 3-7 (a). In Fig. 3-7 (b), the retention go worst as the temperature increase [17] [18] [19] [20]. The quality of the tunneling oxide plays an

important role in charge retention. If the oxide has a defect because of electron repeat impact during the write/erase cycles, all of the charge stored in FG layer will be loss.

Fig. 3-8 shows the endurance characteristics after 10^4 P/E cycles of the FG memory devices. We use channel hot-electron injection to program and Folwer-Nordheim tunneling to erase. Let the memory windows of about 2.2V can be keep. From the Fig. 3-8 we can see that the thinner tunneling oxide will have the better endurance characteristics and 7nm dry oxide and 7nm oxynitride is similar. The increase of threshold voltage of erase state can be observed. This is due to the injection electron not completely eliminated. The accumulation caused to increase the threshold voltage in erase state over P/E cycles [21]. Another reason for this, it may be the stress-induced election traps generated in the tunneling oxide during P/E cycles [22].

We measure the retention after 10^4 P/E cycles of the FG memory devices to confirm the damage of the tunneling oxide. We can see that the 7nm oxynitride still have good retention after 10^4 P/E cycles in 10^8 seconds Fin Fig. 3-9 (a). In the conventional dry oxide, we can find that the charge loss behavior of the devices is more serious. Retention became worse then before, even the retention of 5nm oxynitride is better then the retention of 7nm conventional dry oxide in Fig. 3-9 (b). This means the conventional tunneling oxide was damaged during 10^4 P/E cycles.

Thus the number of electron trapped in the tunneling oxide increase and ability of the charge storage decrease. We can find that oxynitride has better endurance.

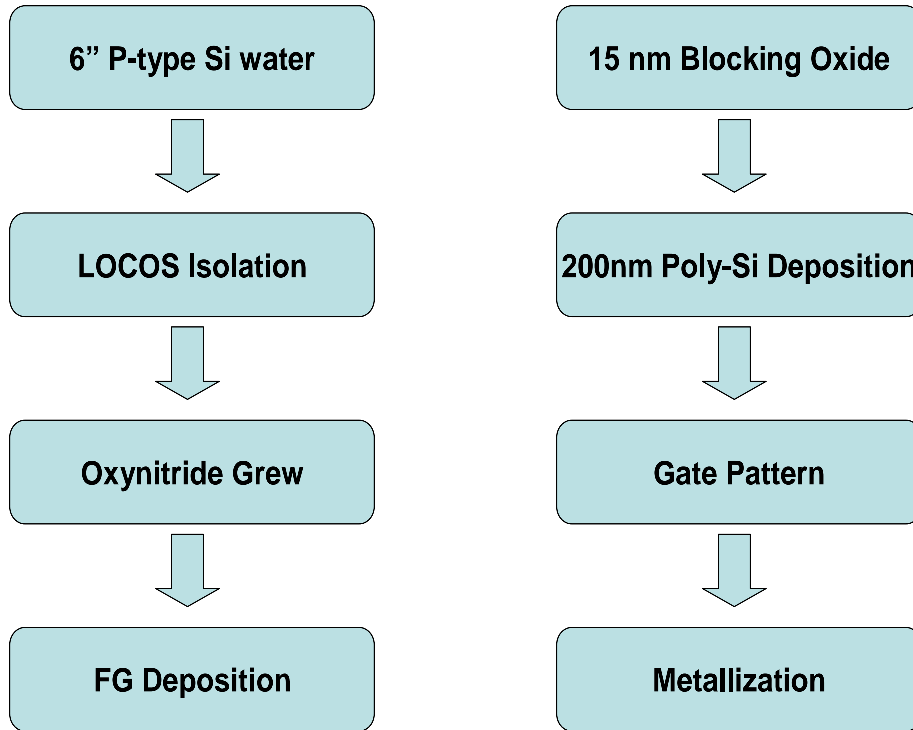
3.3.2 Disturbance Measurement

Gate disturbance may occur the cells sharing a common word line as a cell is been programmed. The applied gate voltage attract electron into the FG layer from the substrate, thus induce the threshold voltage arise. Finally, the cell will from erase state transfer to program state. The data is error. Fig. 3-10 shows the gate disturbance characteristics in the erase state. We use V_G=6V and V_D=V_S=V_B=0V in the erase state of the FG memory for 1000s. We can find that the threshold voltage shift is not enough 0.2V. It means that gate disturbance can be neglected.

Drain disturbance may occur the cells sharing a common bit line as a cell is been programmed. The applied drain voltage attract hole into the FG layer from the substrate, thus induce the threshold voltage degradation. Finally, the cell will from program state transfer to erase state. The data is error. Fig. 3-11 shows the gate disturbance characteristics in the program state. We use V_D=6V and V_G=V_S=V_B=0V in the program state of the FG memory for 250s. The data loss is very serious. We can see that the oxynitride have better result of the data loss duo to drain disturbance.

3.4 Summary

In this chapter, we have investigated the memory effects and performance of the FG memory device with oxynitride. The FG memory with oxynitride can improve the retention, endurance, and drain disturbance without decrease program/erase speed is obvious, and the process is compatible with CMOS process. The oxynitride as tunneling oxide will be a candidate for the flash memory in the future.



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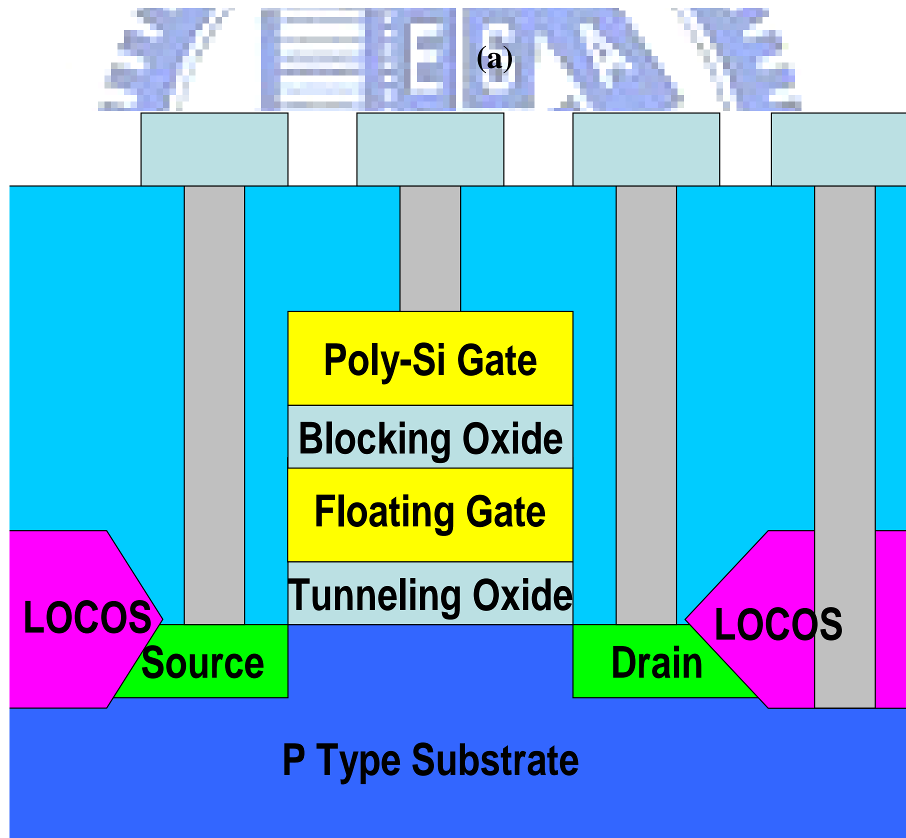
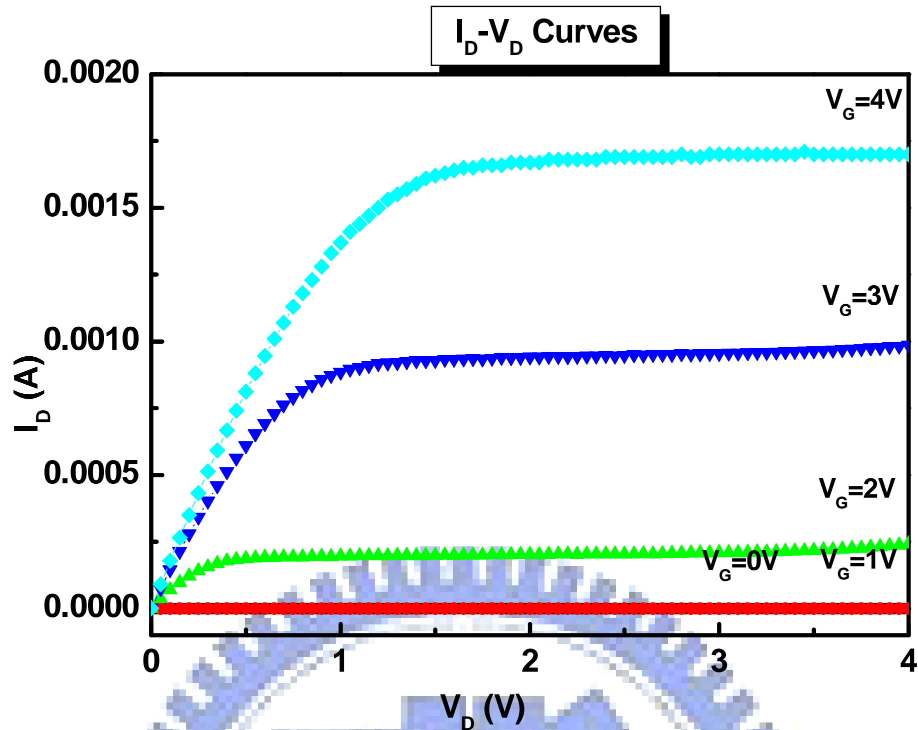


(b)

Fig. 3-1 (a) Process flows for fabricating various the FG memory device (b) Schematic cross section of the FG memory device.

	Expectant	Actuality
5nm Oxynitride	5 nm	5.5 nm
7nm Dry Oxide	7 nm	6.7 nm
7nm Oxynitride	7 nm	7 nm

Table 3-1 The actual thickness of the tunneling oxide.



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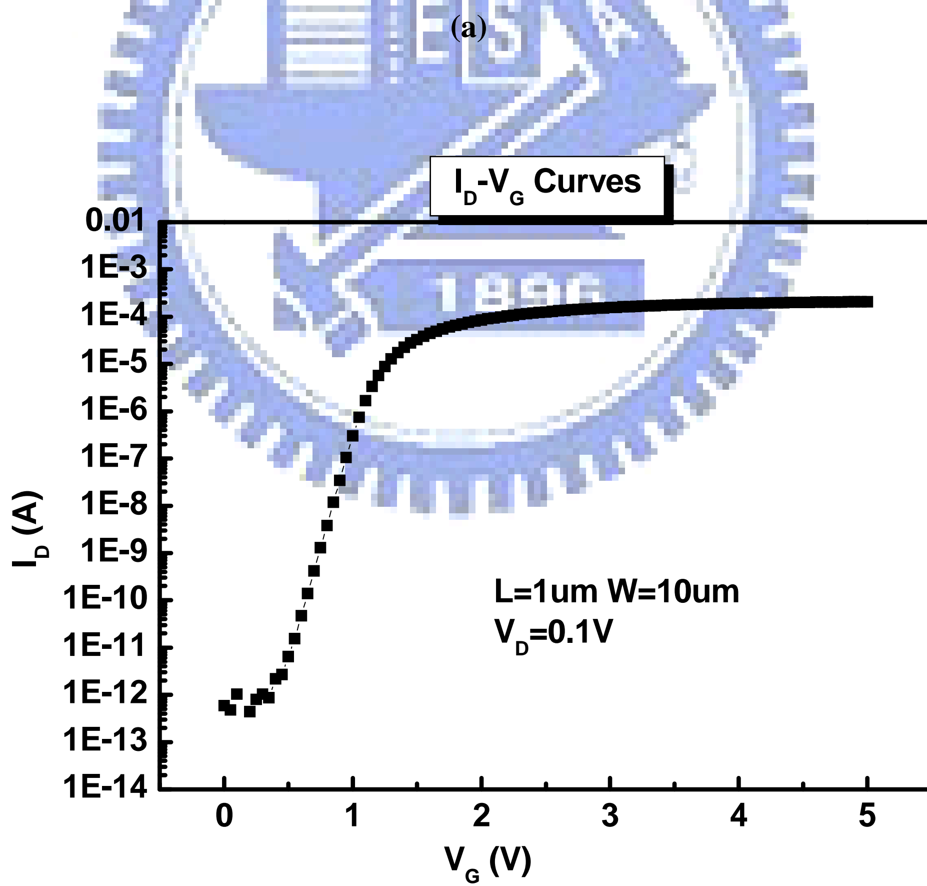


(b)

Fig. 3-2 (a) I_D-V_D curves of the FG memory. (b) I_D-V_G curves of the FG memory.

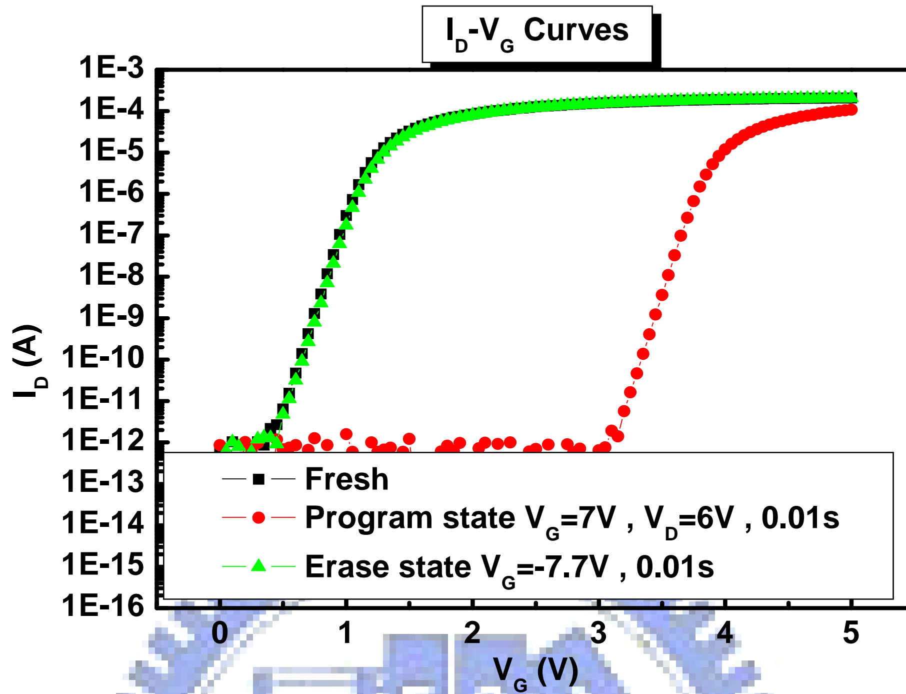
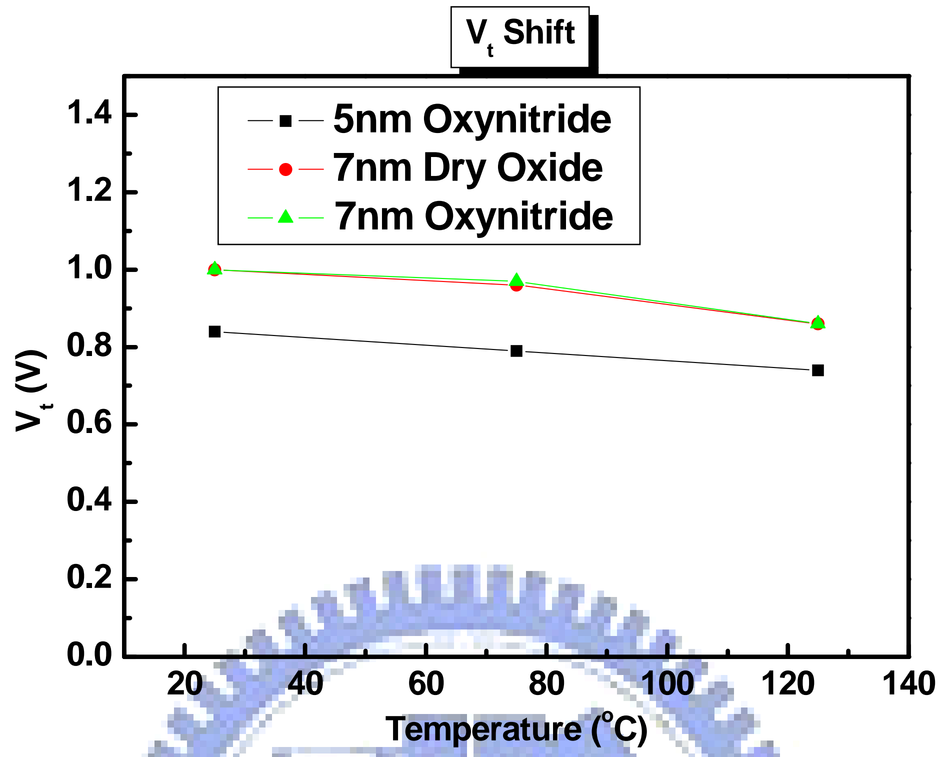


Fig. 3-3 I_D-V_G curves of the FG memory. A memory window about 2.5V can be achieved with programmed V_G = 7V, V_D =6V and erased V_G = -7.7V operation.



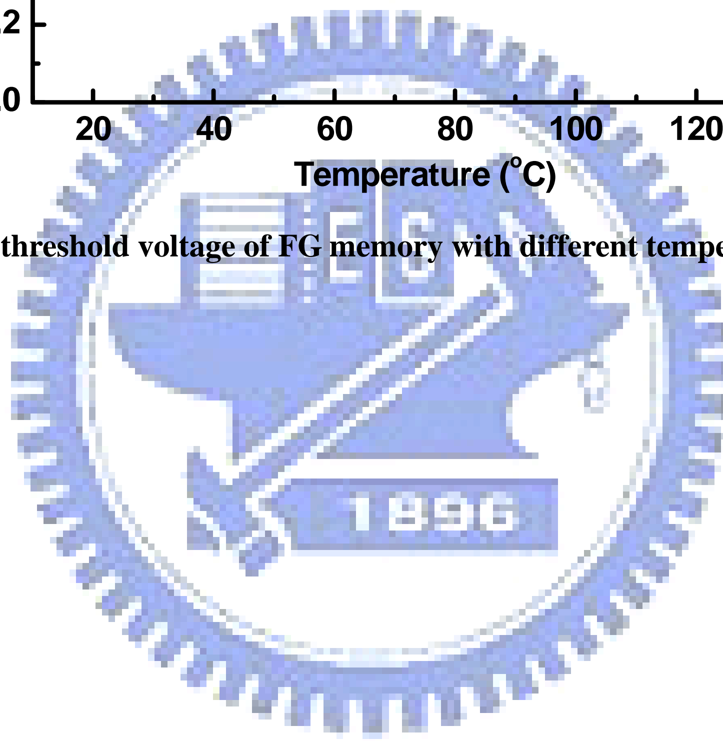
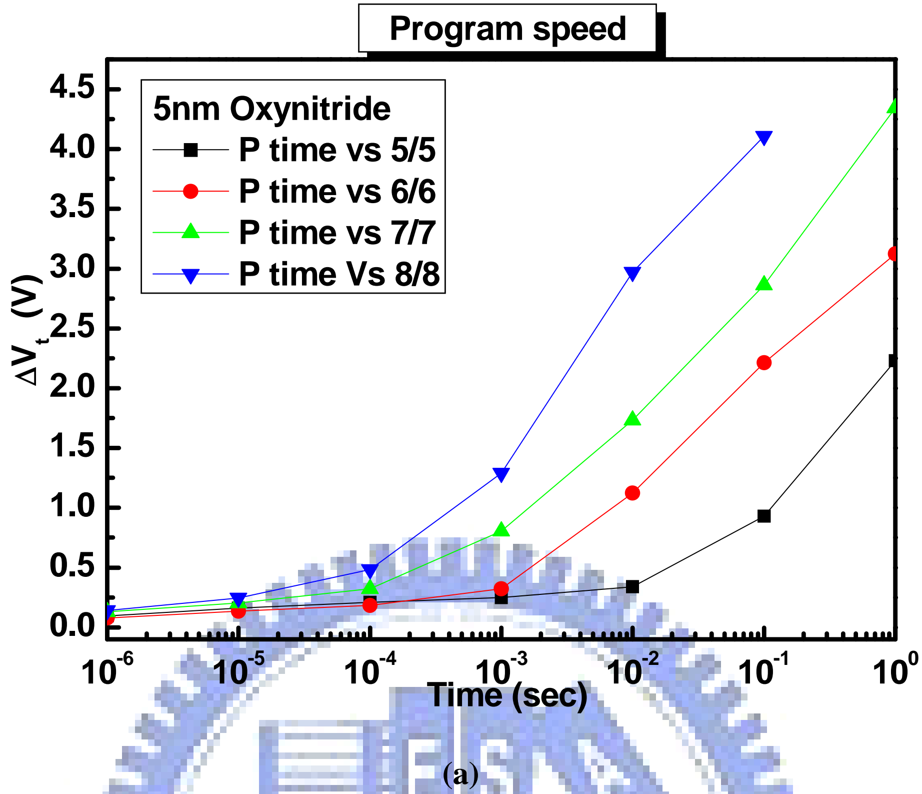


Fig. 3-4 The threshold voltage of FG memory with different temperature.



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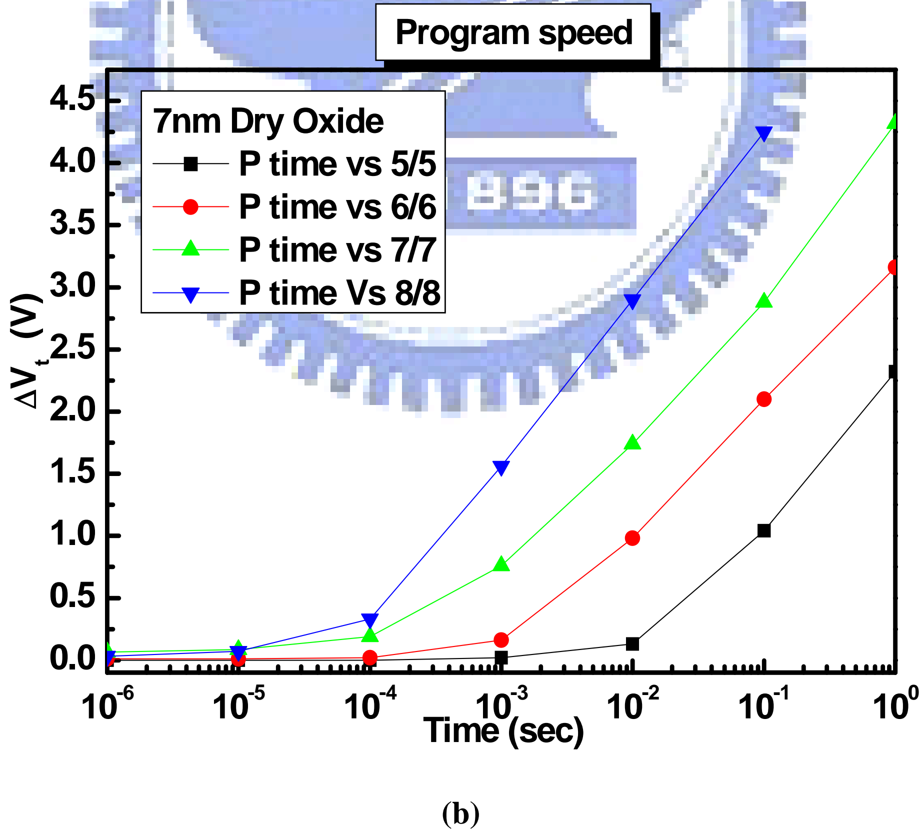
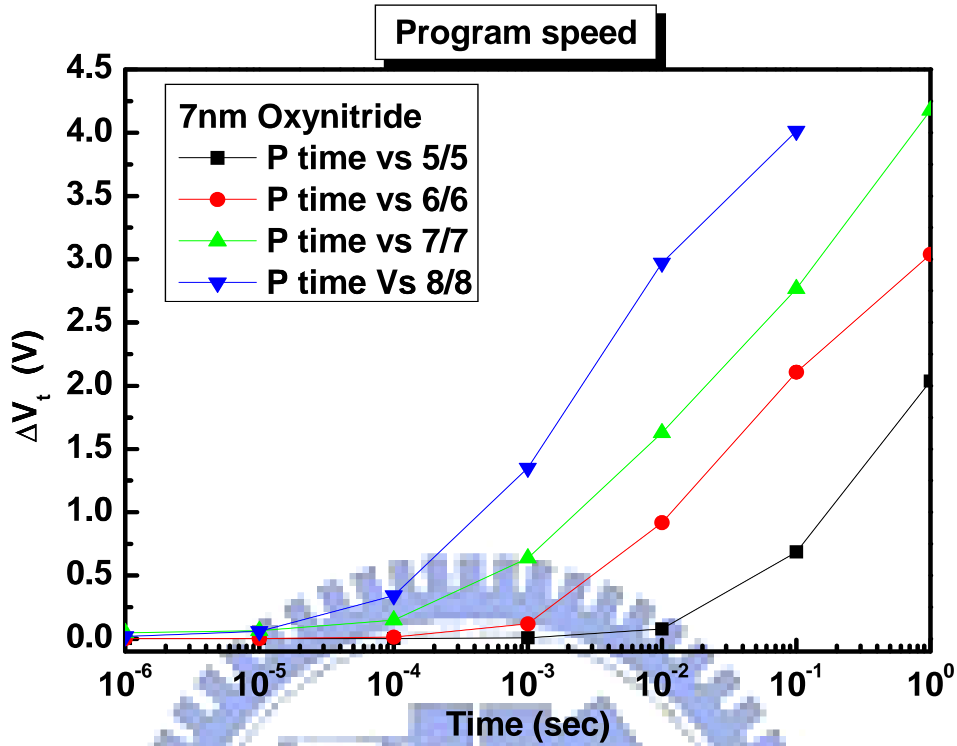


(b)

Fig. 3-5 (a) The program speed of 5nm oxynitrid with $V_G = V_D = 5\sim8V$. (b) The program speed of 7nm dry oxide with $V_G = V_D = 5\sim8V$.



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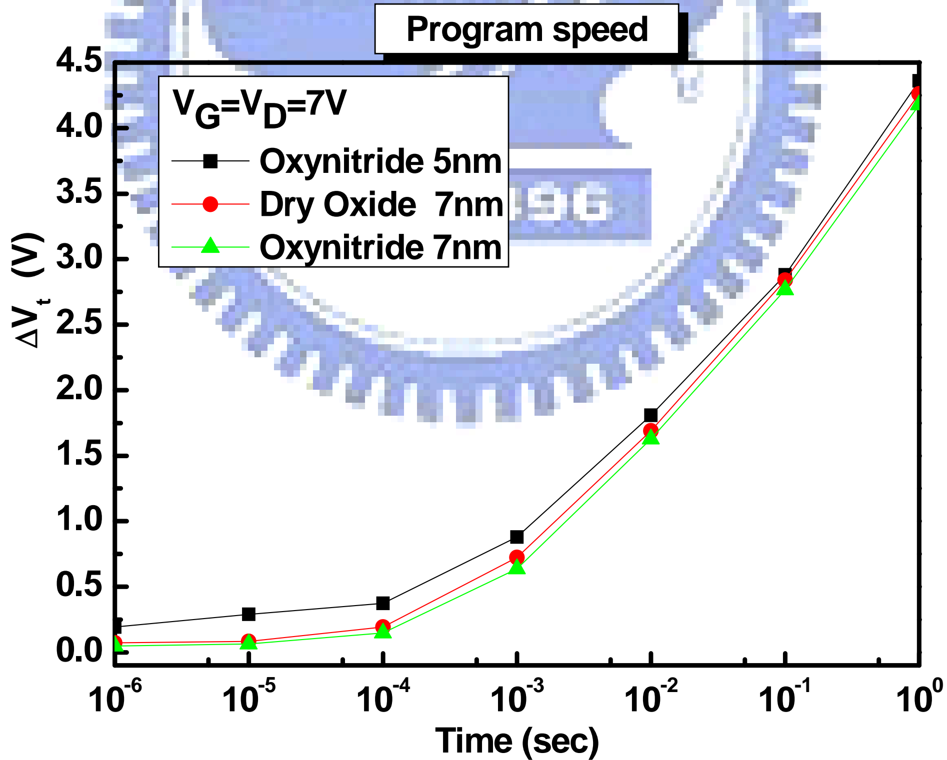
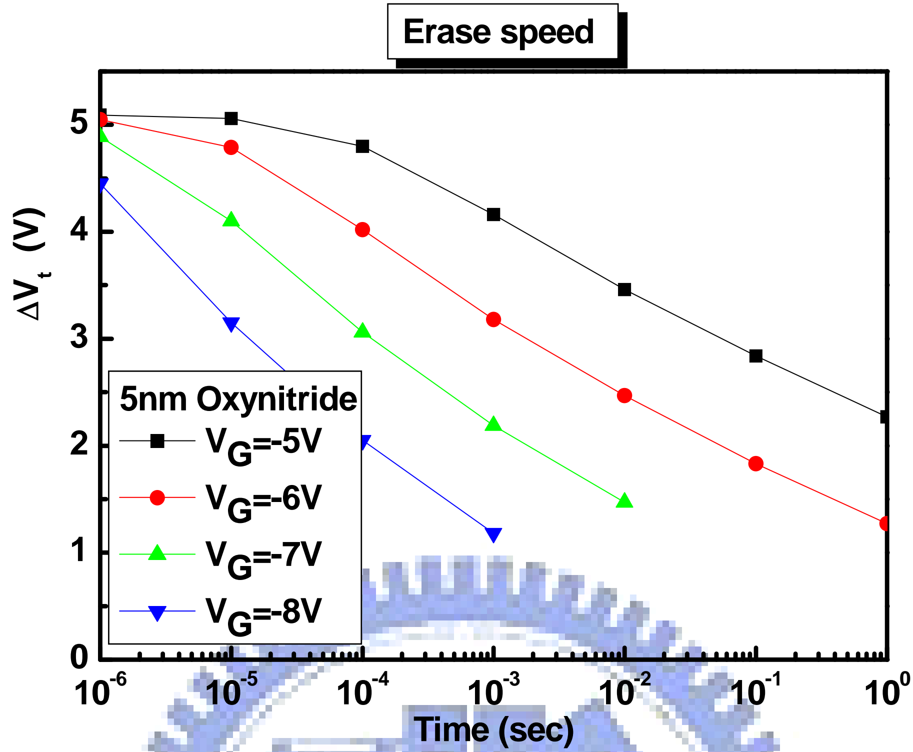


(d)

Fig. 3-5 (c) The program speed of 7nm oxynitrid with $V_G = V_D = 5\sim8V$. (d) The program speed of the different tunneling oxide with $V_G = V_D = 7V$.



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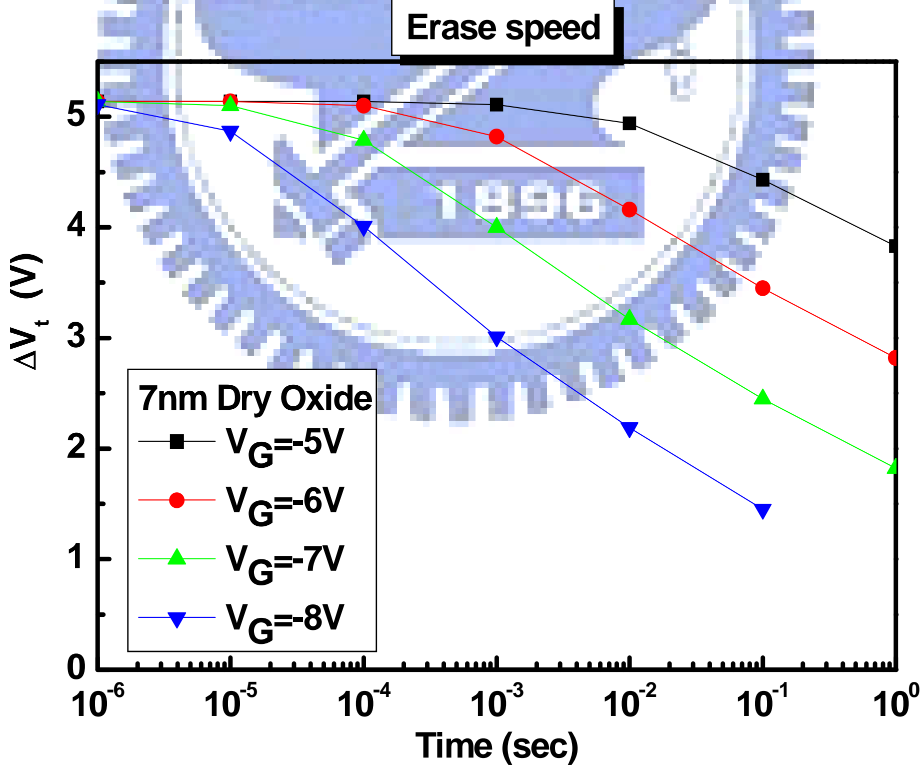
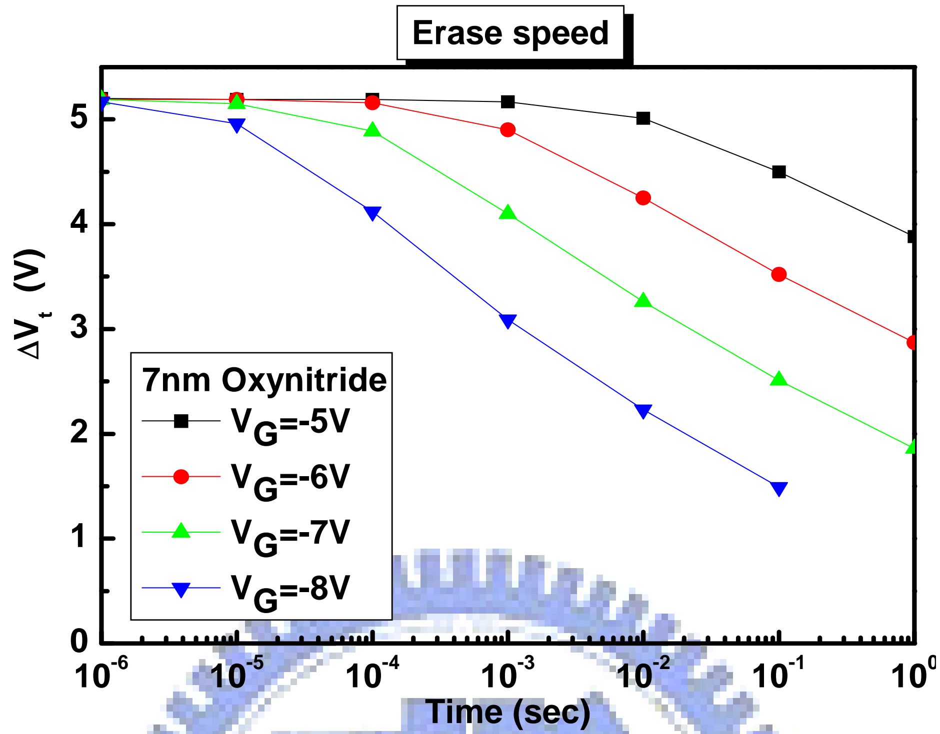


(b)

Fig. 3-6 (a) The erase speed of 5nm oxynitrid with V_G = -5 ~ -8V. (b) The erase speed of 7nm dry oxide with V_G = V_D = -5 ~ -8V.



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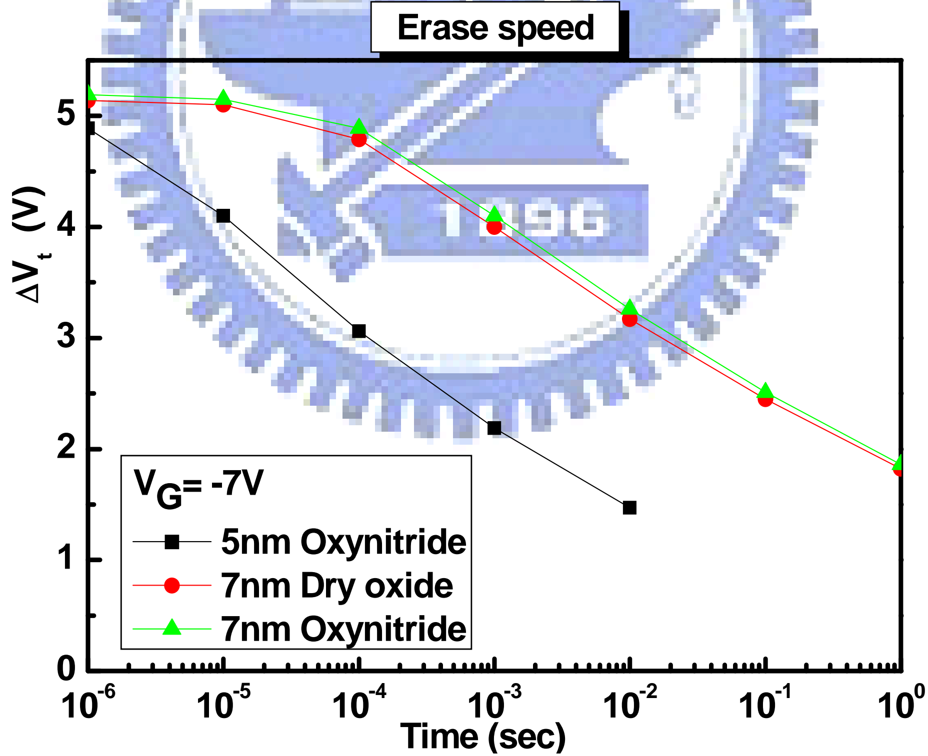

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Fig. 3-6 (c) The erase speed of 7nm oxynitrid with V_G = -5 ~ -8V. (d) The erase speed of the different tunneling oxide with V_G = -7V.

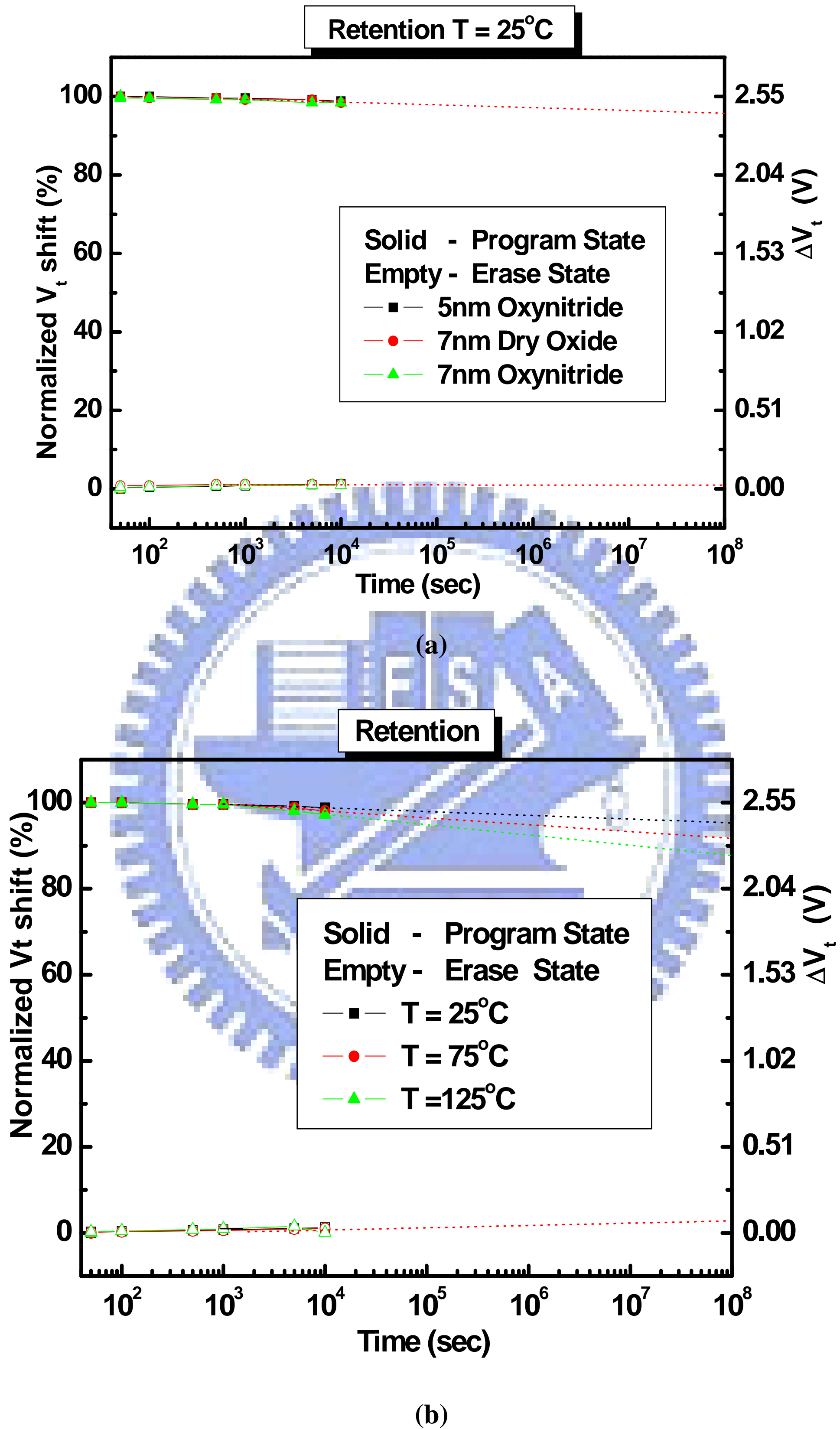
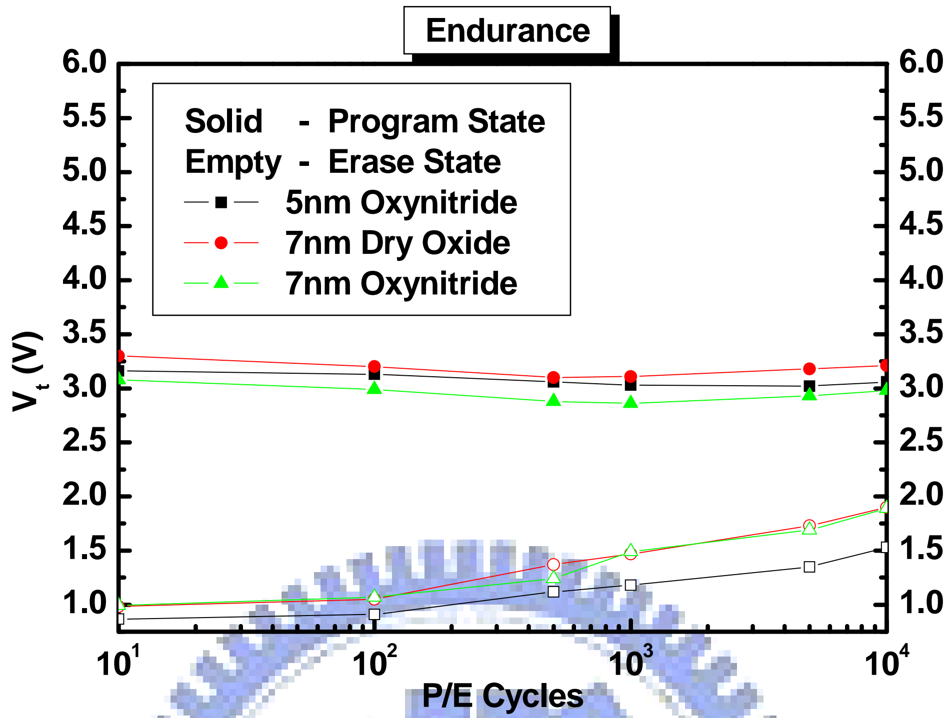


Fig. 3-7 (a) Retention characteristics of the different tunneling oxide. (b) Retention characteristics of the different temperature.



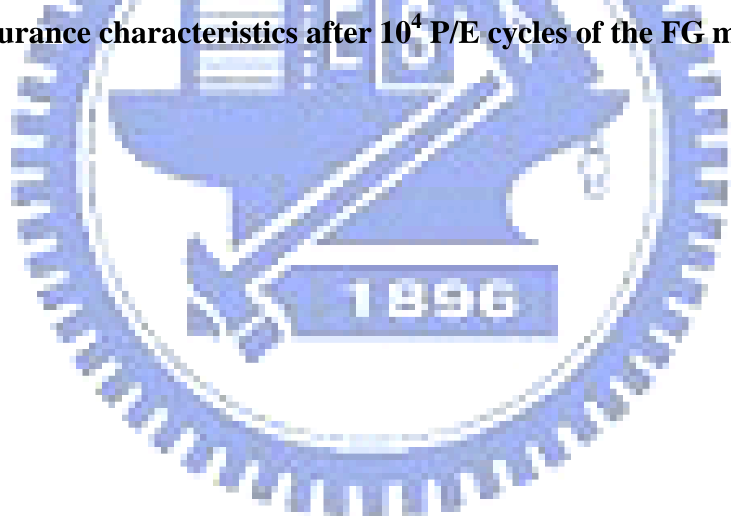
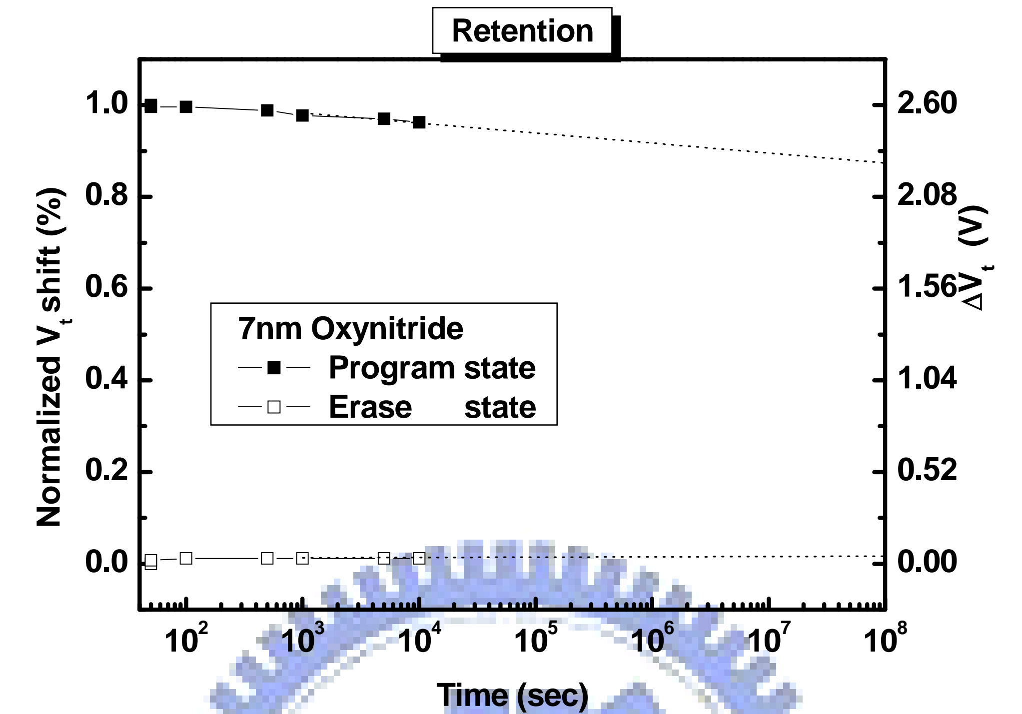
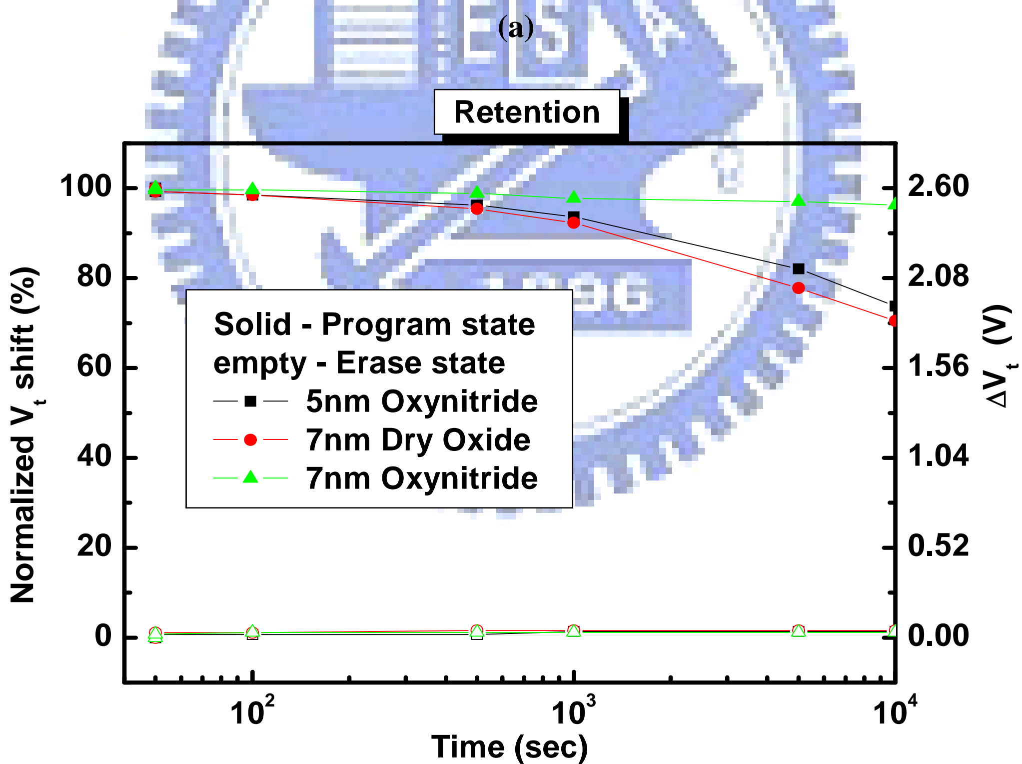


Fig. 3-8 Endurance characteristics after 10^4 P/E cycles of the FG memory devices.



(a)



(b)

Fig. 3-9 (a) Retention characteristics of 7nm oxynitride after 10^4 P/E cycles. (b) Compared retention characteristics of different tunneling oxide after 10^4 P/E cycles.

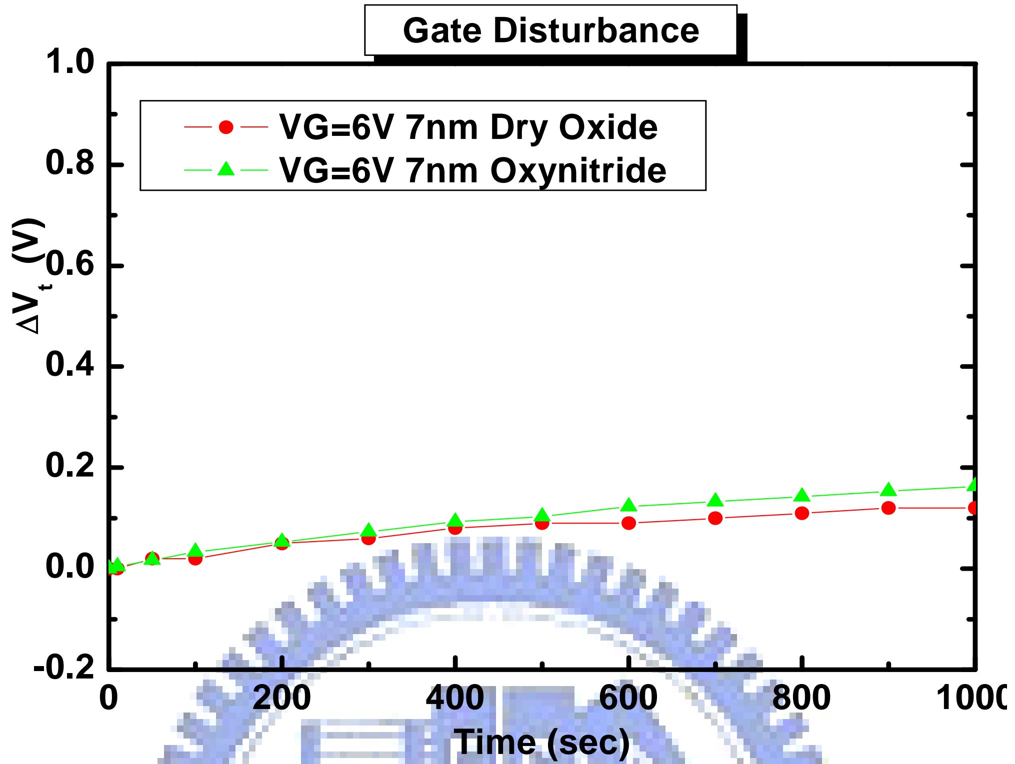


Fig. 3-10 Gate disturbance of the FG memory devices.

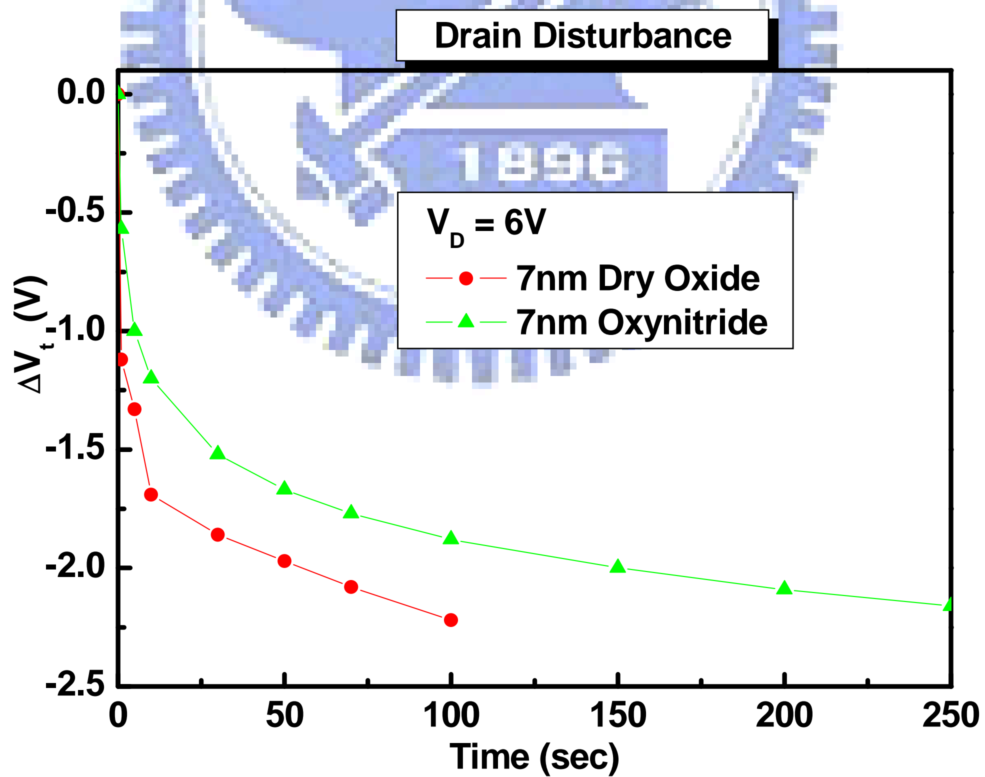


Fig. 3-11 Drain disturbance of the FG memory devices.

Chapter 4
Conclusions and Recommendations for Future Work

4.1 Conclusion

The FG memory is central memory in the nonvolatile memory market. These memory devices have very mature technology. From the data of the measuring, we can find that the FG memory device has extremely good ability of retention even through it is at high temperature. If the device has the path of electron loss, the extremely good ability of retention will not exist. The quality of the tunneling oxide plays an important role in FG memory.

In this thesis, we use the oxynitride to replace conventional dry oxide as the tunneling oxide. We can get the better reliability without decrease program/erase speed. Because our blocking oxide is TEOS oxide without densify, it may cause the program/erase cycles can not reach to 10^5. We can not obviously compare oxynitride better than dry oxide in endurance. The oxynitride has better reliability than traditional dry oxide is not suspect. It has potential that leading FG came to next generation.

4.2 Recommendations for Future Work

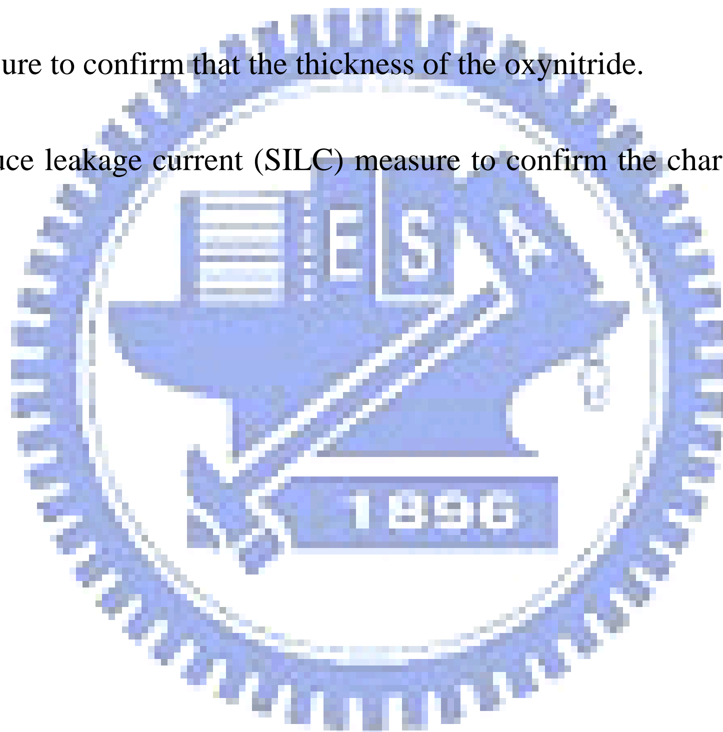
1. SIMS measure to prove that the distribution of the atoms in the tunneling oxide

2. Using the ONO to replace the TEOS oxide of blocking oxide,and then measure the endurance effect whether the program/erase cycles can reach to 10^5.

3. We can try the different temperature and time for nitridation whether the device will have better characteristic.

4. TEM measure to confirm that the thickness of the oxynitride.

5. Stress induce leakage current (SILC) measure to confirm the characteristics of the endurance.



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