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碩 士 論 文

以鉿為基底之高介電常數閘極介電層之N通道金氧半電晶體可靠度探討

Investigation of Reliability in Advanced Hf-Based High-*k* Gate Dielectrics nMOSFETs

研 究 生 ：曾友良

指導教授 ：莊紹勳 博士

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摘要

當元件氧化層持續微縮時，以二氧化矽為基底做為 CMOS 元件因為閘極漏電流過高，無法滿足低功率電路的要求，故以高介電係數材料取代二氧化矽是一個重要的課題。近年來在研究氮氧化鉿矽上，指出可提高介電層物理厚度且有效降低閘極漏電流。與傳統的二氧化矽或氮氧化矽閘極氧化層相比，以鉿為材料的高介電常數閘極介電層具有相當嚴重的可靠度問題：臨界電壓漂移和操作電流的不穩定性，起因於高介電材料層中有大量的缺陷，導致電荷捕捉與逃逸現象。所以發展一套完整且可靠的方法去分析電荷捕捉的特性顯得相當重要。

本論文中，將以已發展成熟的「電荷幫浦」方法做為基礎，利用操作頻率的不同來定性並定量的研究在介電層中缺陷分布的情形。通道電子能穿隧的深度會隨著不同操作頻率而改變，因此可由電荷幫浦電流對應到頻率便能得知在閘極介電層中不同深度的缺陷密度。

此方法用來觀察由製程造成閘極介電層缺陷，另外我們也研究在

高介電層中嚴重的N通道元件正壓高溫破壞後的不穩定性。在不同操作破壞條件下觀察缺陷產生情形，並將此結果與電性有效對應，如臨界電壓、汲極電流等。藉由電荷幫浦方法，我們可以了解在不同製程以及不同操作條件下介電層的良好程度，電路操作的可靠度問題，並且對其物理機制有更深入的了解。

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ABSTRACT

With the aggressive scaling of CMOS devices, SiO_2-based gate dielectrics can't conform the demand of low power application due to large gate leakage and high-k materials as the alternative of SiO_2-based gate dielectrics has attracted a lot of interest. Recently, the studies indicate that HfSiON dielectric significantly reduces gate leakage by increasing physical thickness. Compared to the conventional SiO_2 or SiO_xN_y gate dielectrics, Hf-based gate dielectrics are well known to suffer from the serious reliability concern of threshold voltage shifts and operation current instability due to the fast charge trapping and de-trapping in the pre-existing bulk traps in high-k bulk layer. Therefore, it is very important to develop a integrated and reliable method to quantitatively characterize charge traps in high-k dielectrics.

In this thesis, proposed "Charge Pumping" approach is well developed and we will utilize it basically to study the traps distribution in dielectrics qualitatively and measurably. The available tunneling depth of channel carriers is dependent of frequency. Hence traps density in opposition to dielectric depth is extracted by charge pumping current and frequency.

This method will be used to profile gate dielectrics traps induced by different process. Besides, positive bias temperature instable (PBTI) in high-k gate dielectric nMOSFETs is a critical issue and we will study it. In distinct stress condition, the traps generation will be powerfully related to characteristic in circuit level, such as threshold voltage and drain current. By charge pumping method, the quality and reliability of dielectrics in different process and distinct operation is distinguished and the physics behind is more understood.

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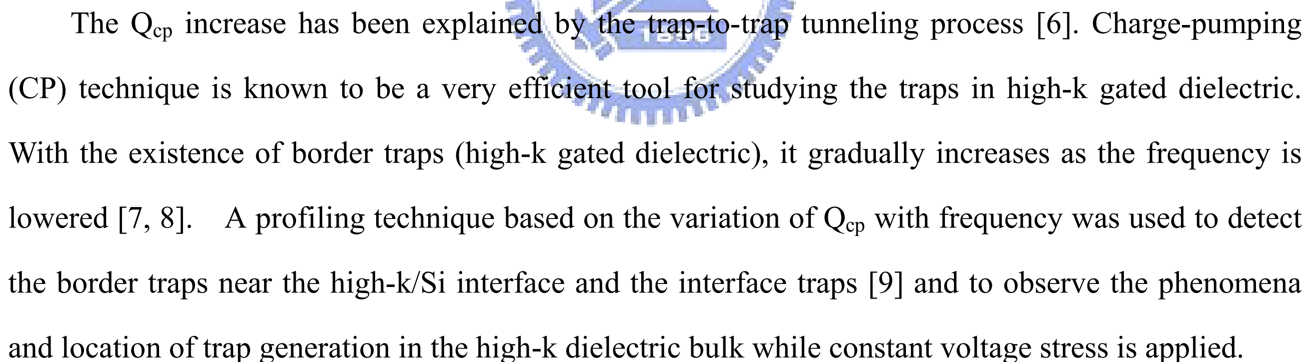
Chapter 1
Introduction

1.1 The Motivation of This work

As the minimum feature size of CMOS devices continues to scale down, the SiO_2 gate dielectric meets its fundamental physical limits. To reduce the large gate leakage and maintain a low equivalent oxide thickness (OET), the gate dielectric materials with high dielectric constant (high-k) have been proposed to replace SiO_2. [1,2]. However, most reports have shown that the use of high-k gate dielectrics is apt to generate large number of interface traps at the surface channel and oxide trap charges in the gate dielectric bulk of MOS transistors, which would result in the degradation of device electrical characteristic [3–5].



The Q_{cp} increase has been explained by the trap-to-trap tunneling process [6]. Charge-pumping (CP) technique is known to be a very efficient tool for studying the traps in high-k gated dielectric. With the existence of border traps (high-k gated dielectric), it gradually increases as the frequency is lowered [7, 8]. A profiling technique based on the variation of Q_{cp} with frequency was used to detect the border traps near the high-k/Si interface and the interface traps [9] and to observe the phenomena and location of trap generation in the high-k dielectric bulk while constant voltage stress is applied.

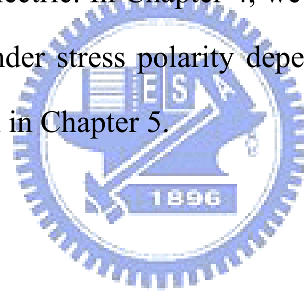
Furthermore, during measurement, we need to overcome the induced leakage current using any of the above methods. It has been demonstrated successfully an IFCP (Incremental Frequency Charge Pumping) method for the interface characterization.

In this thesis, traps at various location of a stacked dielectric have been characterized by charge-pumping (CP) technique combined with multiple frequency measurement. Then we will

compare different halo implants devices by positive constant stress and negative constant stress. The excellent correlation of all types of traps to process conditions makes this method very promising for the applications in high-k dielectrics development.

1.2 Organization of this thesis

This thesis has been divided into five chapters. Chapter 2 describes the devices used in this work and experimental setup. The low leakage IFCP method for high-K dielectrics will be used to determine interface traps and the traps in high-K dielectrics. At the same time, the evaluation will be described. In Chapter 3, we will use the method of Chapter 2 to discuss varied channel length NMOSFETs with a polysilicon gate and HfSiON gate dielectric. In Chapter 4, we also use the same method to investigate the effect of halo implants species under stress polarity dependent constant voltage stress. Finally, a summary and conclusion will be given in Chapter 5.



Chapter 2
Device Fabrication and Experimental Measurements

2.1 Introduction

To reduce the high gate leakage, current major efforts are focused on replacing SiO_2 and SiON with high-k gate dielectrics. If a material with a dielectric constant larger than 3.9 of SiO_2 is used, the same equivalent oxide thickness (EOT) can be reached with a physically thicker layer. This ultimately leads to a reduction of the gate leakage current and allows further scaling of the gate oxide. The most promising candidate with sufficient high k-value is currently HfO_2, but unfortunately there is an interaction with the poly-Si gate, leading to Fermi level pinning, and large defect densities as well as V_T instabilities are reported [4]. Only when metal gate electrodes are used, most of the unwanted effects disappear and the poly-Si depletion can be eliminated. From integration point of view, poly-Si electrodes are still preferred and be used to speed up the introducing of high-k dielectrics. Hf-silicates (HfSiON) most likely will be the first to be introduced in integrated CMOS. Hf-silicates proved compatibility with poly-Si gate processing while maintaining good electrical characteristics. HfSiON can only be introduced if reliability is guaranteed [11]. However, the direct tunneling leakage is still large under EOT scaling down to below 16Å.

In order to analyze the reliability property of NMOSFET's in thin HfSiON in the following chapters, we use a simple charge pumping method. As a result, the measurement setup and basic theory used are listed here. This chapter is divided into several sections. In the first section, the devices used in this study are examined. Then, the experimental analysis methods used in thesis will be introduced, including the low leakage IFCP method for high-k dielectrics.

2.2 Experimental Setup

The experimental setup for the I-V measurement of MOSFET's is illustrated in Fig. 2.1. Based on the PC controlled instrument environment, the complicated and long-term characterization procedures for analyzing the intrinsic and degradation behavior in MOSFET's can be easily achived. As shown in fig.2.1, the characterization equipment, including semiconductor parameter analyzer (HP4156C), dual channel pulse generator (HP8110A), low leakage switch mainframe (HP E5250A), cascade guarded thermal probe station and thermal controller, provides an adequate capability for measuring the device I-V characteristics. Besides, the PC program used to control all the measurement process is VEE and HT-basic.

2.3 Device Fabrication

MOS devices were fabricated based on advanced 90nm CMOS technology. The high K film deposited by ALD (atomic layer deposition) is HfSiON, while HfSiON films received post-deposition NH_3 annealing. A given interfacial layer film was formed on a Si(100) wafer prior to high K film deposition. Interfacial layer film used in this work is nitrogen-incorporated SiON. All wafers received HF cleaning prior to growing interfacial layer film. Halo B and halo BF_2 are two different implant species for light AMU and heavy AMU, respectively. Fig.2.2 shows the device fabrication process.

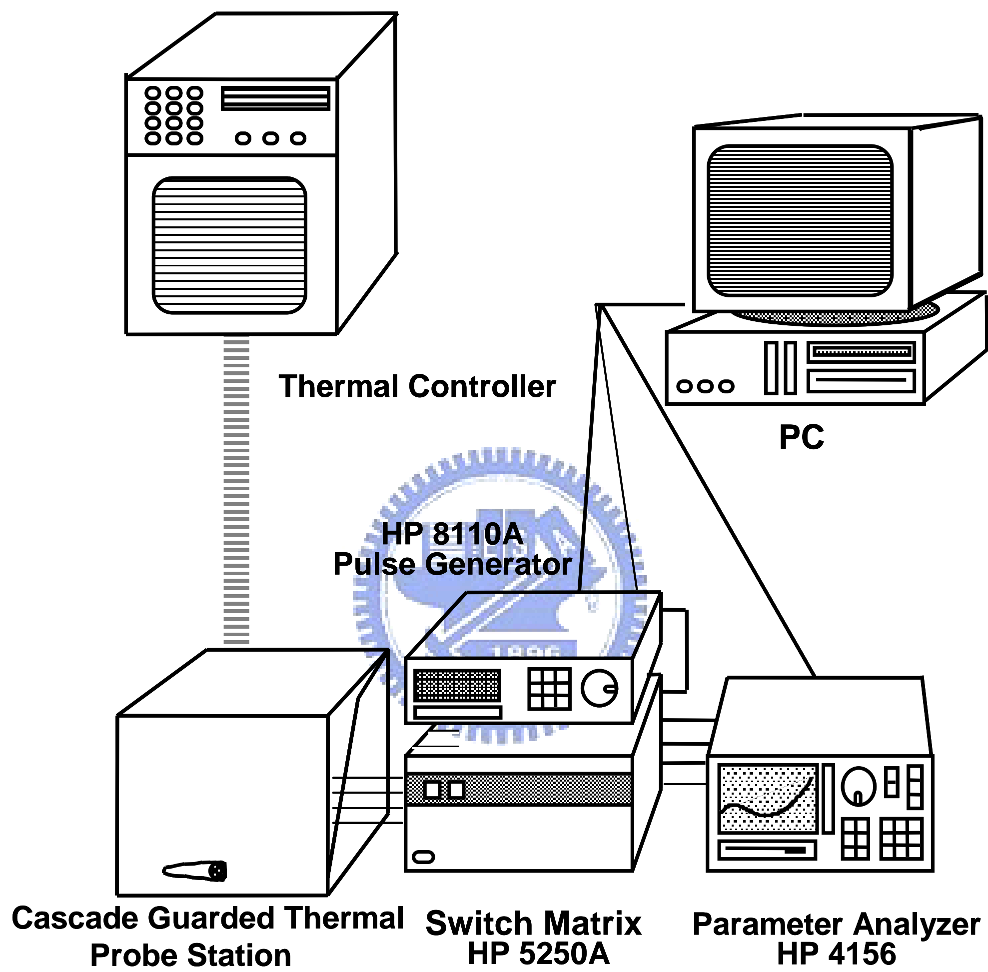


Fig.2.1 The experimental setup and environment for basic I-V measurement of MOSFET's.

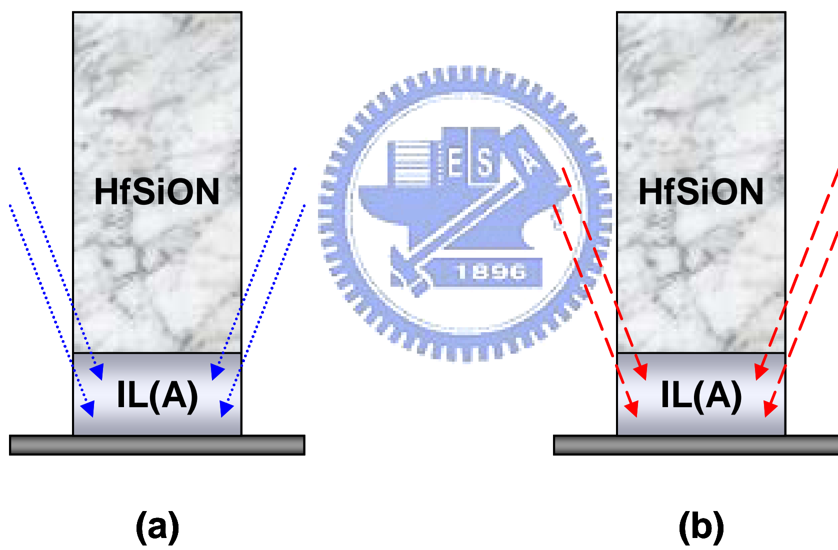


Fig. 2.2 Schematic illustrations of device with different halo implant species. (a) Using light atomic mass unit implant in halo B. (b) Using heavy atomic mass unit implant in halo BF_2.

2.4 The Low Leakage IFCP Technique

2.4.1 Basic Theory

The charging pumping principle for MOSFET's has been applied to characterize the fast interface traps in MOSFET's. The original charge pumping method was introduced by Brugler and Jespers, and the technique was developed by Heremans [12]. This technique is based on a recombination process at the Si/SiO_2 interface involving the surface traps. It consists of applying a constant reverse bias at the source and drain, while sweeping the base level of the gate pulse train from a low accumulation level to a high inversion level. The frequency and the rise/fall time are kept constant. When the base level is lower than that flat-band voltage while the top level of the pulse is higher than the threshold voltage, the maximum charge pumping current occurs. This means that a net amount of charge is transferred from the source and drain to the substrate via the fast interface traps each time the device is pulsed from inversion toward accumulation. The charge pumping current is caused by the repetitive recombination at interface traps. As a result, the recombination current measured from the bottom (substrate) is the so-called charge pumping current [13]. The CP current can be given by:

$$I_{CP} = q \cdot f \cdot W \cdot L \cdot N_{IT}. \quad (2.1)$$

According to this equation, the current is directly proportional to the interface trap density in the channel, the frequency, and the area of the device. However, when the top level of the pulse is lower than the flat-band voltage or the base level is higher than the threshold voltage, the fast interface traps are permanently filled with holes in accumulation or the electrons in inversion in n-MOSFET's, which no holes reach the surface at the time, respectively. As a result, there is no recombination current and then the charge pumping current cannot be discovered.

Charge pumping measurements can be performed with several different ways. For our experimental requirement, we perform the charge pumping measurement by applying a gate pulse with the fixed base voltage (V_{gl}) and increasing the pulse amplitude. While the channel operates between accumulation and inversion as the fixed base voltage lower than flat-band voltage and high voltage above the threshold voltage respectively; this gives rise to the charge pumping current (I_{CP}) from the bulk and reaches saturation situation. If we use another method which changes base voltage with fixed pulse amplitude, the current saturation region is not extensive enough for research because of the limit that the saturation current happens only when the gate pulse train from a low accumulation level to a high inversion level.

2.4.2 Experimental Setup of Charge Pumping Measurement

The basic setup of charge pumping measurement is shown in fig.2.3. The source, drain and bulk electrodes of tested devices are grounded. A 1MHz square pulse waveform provided by HP8110A with fixed base level (V_{gl}) is applied to NMOS gate, or with fixed top level (V_{gh}) is applied to PMOS gate. We keep V_{gl} at –1.0V while increase V_{gh} from –1.0V to 1.0V by step 0.1V, or keep V_{gh} at 1.0V while decrease V_{gl} from 1.0V to –1.0V by step –0.1V.

With a smaller voltage step, we get a higher profiling resolution. The parameter analyzer HP4156C is used to measure the charge pumping current (I_{CP}).

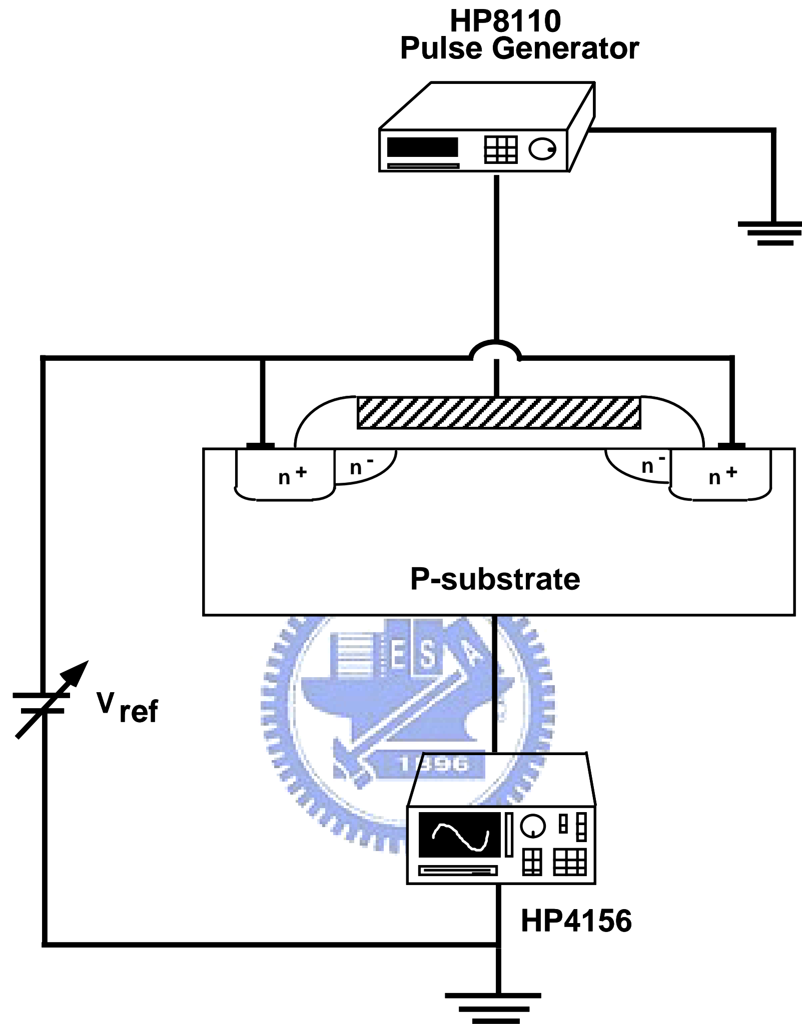


Fig.2.3 The experimental setup of charge pumping method.

2.4.3 Principle of the Low Leakage IFCP Method

Figures 2.4 (a) and (b) show the schematic of a low leakage IFCP measurement for CMOS developed by [14]. With both S/D grounded and by applying a gate pulse with a fixed base level (V_{gl}) and a varying high level voltage (V_{gh}) for NMOS, the channel will operate between accumulation and inversion. This gives rise to the charge pumping current I_{CP} (=I_B) measured from the bulk. However, leakage current I_G is unavoidable, as we see from Fig. 2.4 (a), the leakage of I_{CP} is very small when t_{ox} >30Å. However, it was revealed in Fig. 2.5 that the leakage current increases curves (1) and curves (2), for tested sample. From the measured I_{CP} at two frequencies, f_1 and f_2, can be expressed as :

$$I_{CP,\ f1\ \text{with-leakage}} = I_{CP,\ f1\ \text{correct}} + I_{CP,\ \underline{\text{leakage}@f1}} \qquad (2.2)$$

and

$$I_{CP,\ f2\ \text{with-leakage}} = I_{CP,\ f2\ \text{correct}} + I_{CP,\ \underline{\text{leakage}@f2}}. \qquad (2.3)$$

When the frequency is sufficiently high, the leakage components in these two frequencies are almost the same ($I_{CP,\ \text{leakage}@f1} \approx I_{CP,\ \underline{\text{leakage}@f2}}$). We then take the difference of I_{CP} ($\Delta I_{CP,\ f1-f2}$) between two frequencies. From equations (2.2) and (2.3), the difference of these two CP curves gives :

$$\Delta I_{CP,\ f1-f2} = I_{CP,\ f1\ \text{with-leakage}} - I_{CP,\ f2\ \text{with-leakage}}. \qquad (2.4)$$

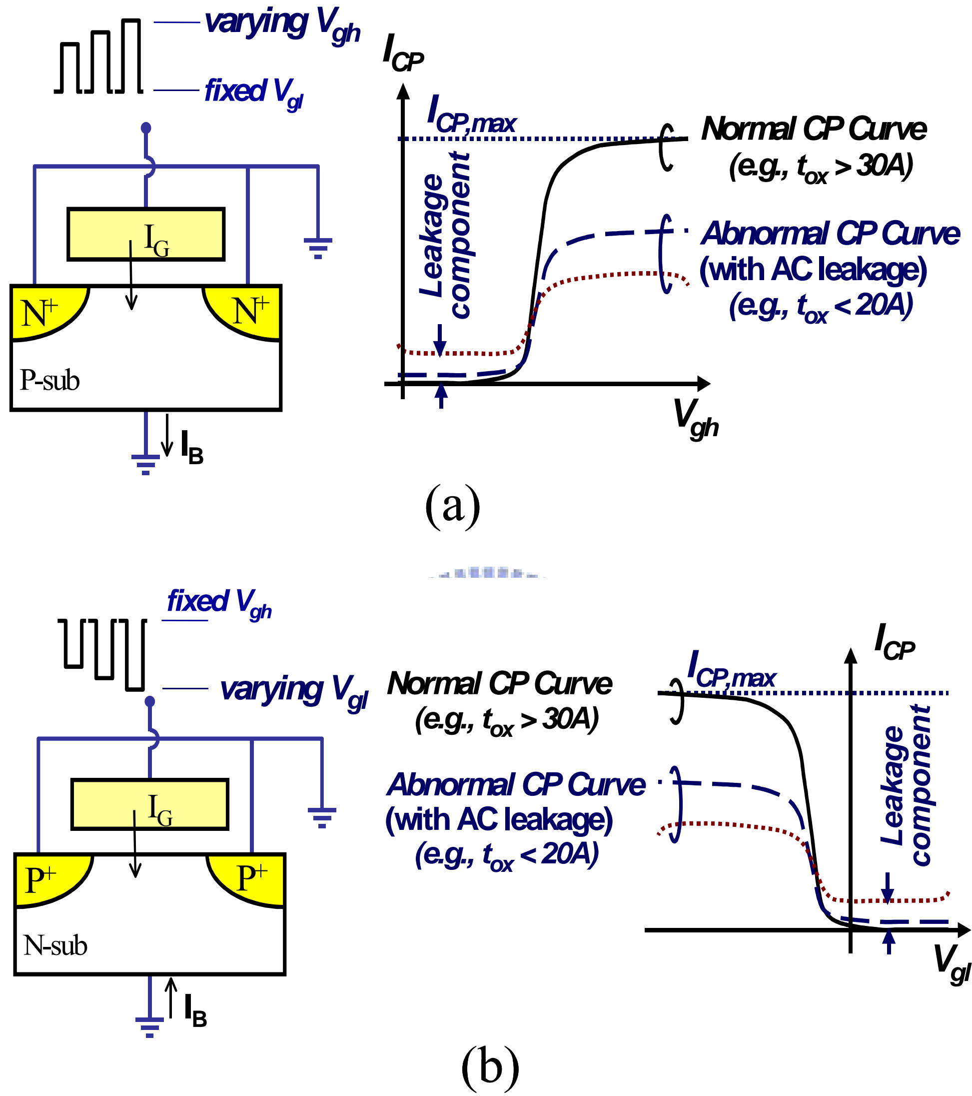


Fig.2.4 The schematic of charge pumping for (a) nMOSFET measurement, (b) pMOSFET measurement. Induced leakage current (I_G) occurs when t_{ox}< 20A.

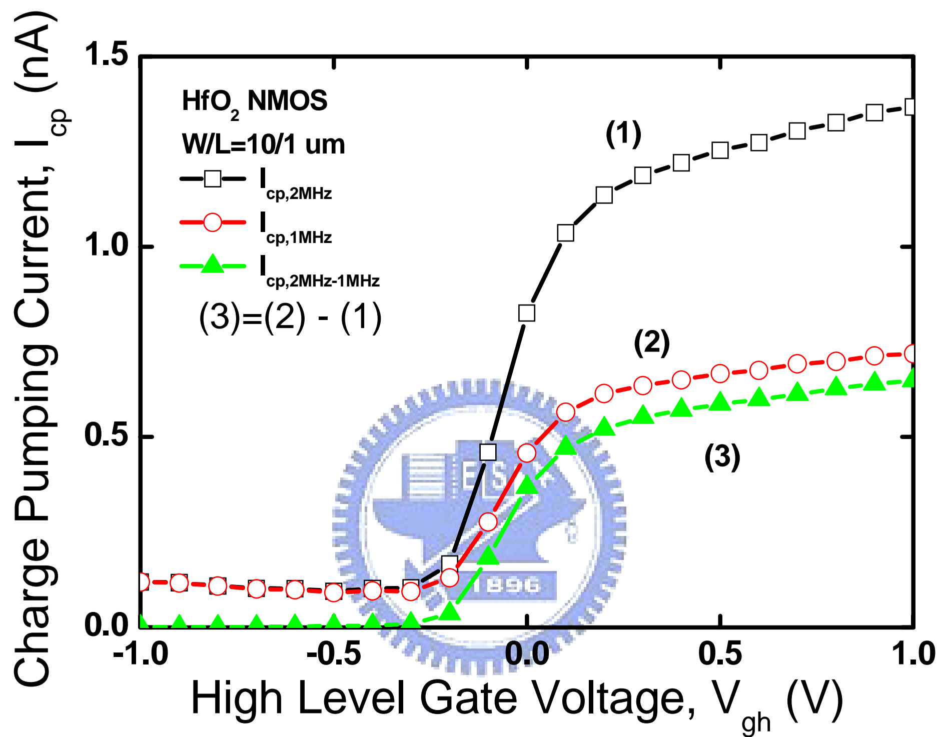


Fig.2.5 Measurement of I_{CP} at two different frequencies. The low leakage IFCP method is achieved by subtracting their respective I_{CP}'s at two successive frequencies.

Since the correct CP curve is directly proportional to the frequency, it will be equal to the difference of two CP curves. Therefore, in the IFCP method, the correct CP curve at frequency ($f1- f2$) can be given by

$$I_{CP, f1-f2} = \Delta I_{CP, f1-f2}. \qquad (2.5)$$

For example, $I_{CP(2MHz)} - I_{CP(1MHz)}$ is regarded as the I_{CP} at their difference frequency, 1MHz. The correct result is shown in curve (3).

2.4.4 Application of the IFCP Measurement for High–K Dielectrics

We mentioned that low leakage IFCP measurement can reduce the leakage component and extract interface state density accurately. Unfortunately this excellent method can not be applied to high K devices due to fast oxide traps. When a low frequency is applyied to gate, the I_{CP} includes two component which are $I_{CP,Nit}$ and $I_{CP,Not}$. On the other hand, a high frequency applying to gate, the composition of charge pumping current is almost N_{it}. This phenomenon has already been described by R. Degraeve and A. Kerber [15]. Fig. 2.5 shows the charge pumping measurement at 1MHz and 2MHZ. We could found unreasonable results since I_{CP} has two components at low frequency, if we applied the IFCP measurement to high K device. In the meanwhile, we also find that high frequency CP measurement is more sensitive in gauging the interface state density. Using this characteristic, we improve IFCP for high K device.

2.5 Extraction of the Effective Channel Length

Figure 2.6 shows the non-uniform interface trap distribution for the extraction of effective channel

length. Using two different channel lengths, the interface traps can be represented by

$$N_{it,\,1,\,total} = N_{it,\,11}(edge) + N_{it,\,12}(center) \qquad (2.6)$$

and

$$N_{it,\,2,\,total} = N_{it,\,21}(edge) + N_{it,\,22}(center). \qquad (2.7)$$

Since the mechanical stress in the edge region is more critical than the center region, the interface traps in the edge is larger than that in the center region and the mechanical stress in two different channel devices are almost the same, $N_{it,\,11}$ is approximately equal to $N_{it,\,21}$. To eliminate the traps generated at the edge region, the difference of these two interface traps can be used, which is directly proportional to the ΔL. Hence, we have

$$\Delta I_{CP,\,max} \propto \Delta N_{it,\,total} = N_{it,\,1,\,total} - N_{it,\,2,\,total} = N_{it,\,12} - N_{it,\,22} \propto \Delta L. \qquad (2.8)$$

Figure 2.5 (a) shows the definitions of ΔL_1, ΔL_2, and ΔL_0, which can be expressed as

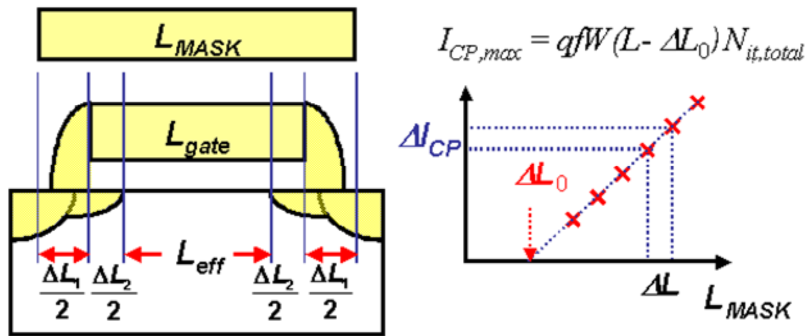
$\Delta L_1 = L_{MASK} - L_{gate}$,

$\Delta L_2 = L_{gate} - L_{eff}$,

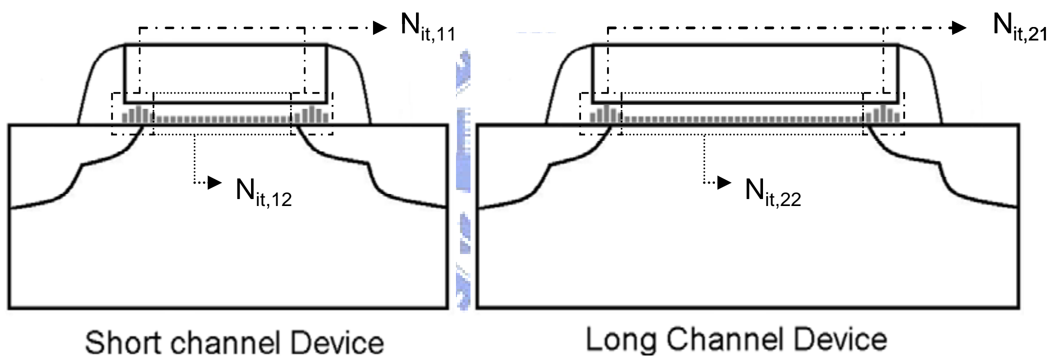
and

$$\Delta L_0 = L_{MASK} - L_{eff} = \Delta L_1 + \Delta L_2. \qquad (2.9)$$

Figures 2.7 show the calculated interface traps, N_{it}, per unit width and offset length, $\Delta L_0 = L_{MASK} - L_{eff}$, from the measured 10 devices with two nMOSFETs in this work. Finally, we can get ΔL_0=48nm and that will help us calculate accurate data to analyze short channel device characteristic.

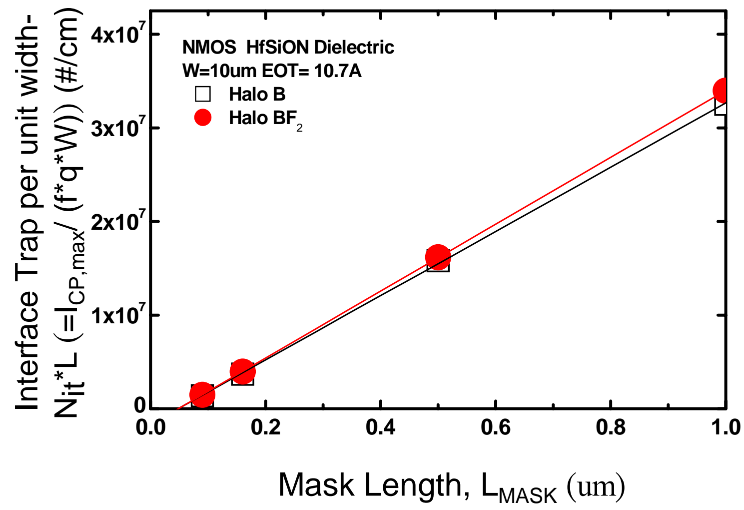


(a)



(b)

Fig.2.6 Illustration of ΔL_0 extraction from C-P data. (a) Parameter definition and extraction method. (b) Interface traps distribution in short and long channel length devices.



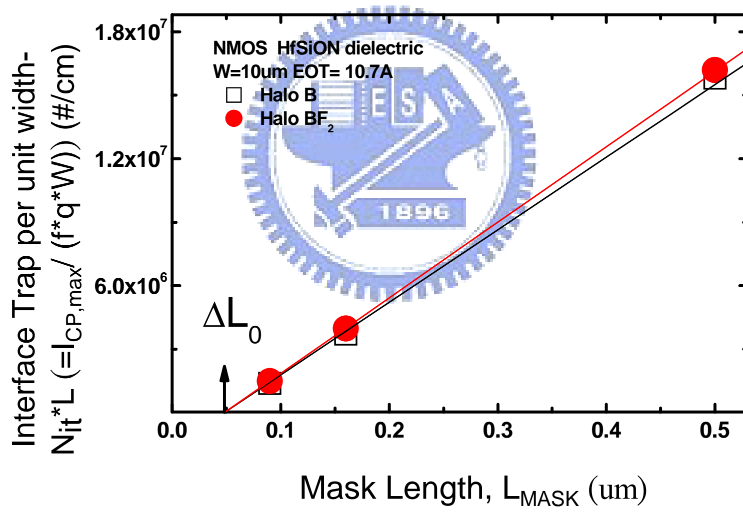


Fig. 2.7 (a) Non-uniform interface trap distribution for the extraction of effective channel length.

(b) To enlarge the figure to calculate $\Delta L_0 \approx 0.048\mu m$.

2.6 Geometry Effect in Charge-Pumping Measurement

The charge pumping method is suitable for interface trap measurements on small geometry MOSFETs instead of large-diameter MOS capacitors. The MOSFET source and drain are tied together and slightly reverse biased with voltage V_R. The time varying gate voltage is of sufficient amplitude for the surface under the gate to be driven into inversion and accumulation. The charge pumping current is measured at the substrate, at the source-drain tied together, or at the source and drain separately. The interface traps, continuously distributed through the band gap, are represented by the four small horizontal lines at the semiconductor surface with the filled circles representing electrons occupying interface traps. When the gate voltage changes from positive to negative potential, the surface changes from inversion to accumulation. However, the important processed take place during the transition from inversion to accumulation and from accumulation to inversion.

When the gate pulse falls from its high to its low value during its finite transition time, electrons in the inversion layer shift to both source and drain. In addition, electrons captured by those interface traps near the conduction band are thermally emitted into the conduction band and also drift to source and drain. Those electrons on interface traps deeper within the band gap do not have sufficient time to be emitted and will remain captured on interface traps. Once the hole barrier is reduced, holes flow to the surface where some are captured by those interface traps still filled with electrons. Holes are indicated by the open circles on the band diagrams. Finally, most traps are filled with holes. Then, when the gate returns to its positive voltage, the inverse process begins and electrons flow into the interface to be captured. That meets a part of electrons flow into the inversion layer from the source and drain will not flow back into the source-drain. They would recombine with holes to generate charge pumping current. Nevertheless, under high frequency measurement, amount of carriers in channel center has not enough time to flow back into the source-drain as the channel is too long. That would induce a large current by recombine with holes through next state, accumulation mode. It will blight

wrong measured result. Fig.2.8 and fig.2.9 show the short and long channel SiO_2 gate dielectric NMOS in charge-pumping measurement. As the figures, long channel device has geometry effect to lead Icp to grow dramatically.

2.7 Summary

In this chapter, experiment analysis methods have been described. In the latter discussions, we will use these experimental techniques to discuss the traps in the gate dielectrics and interface trap in Si/IL (interfacial layer) for nMOSFET under stress polarity dependent constant voltage stress. By using the IFCP method and the method of separating N_{it} and N_{ot}, the difference between halo(B) and halo(BF_2) samples will also be studied.

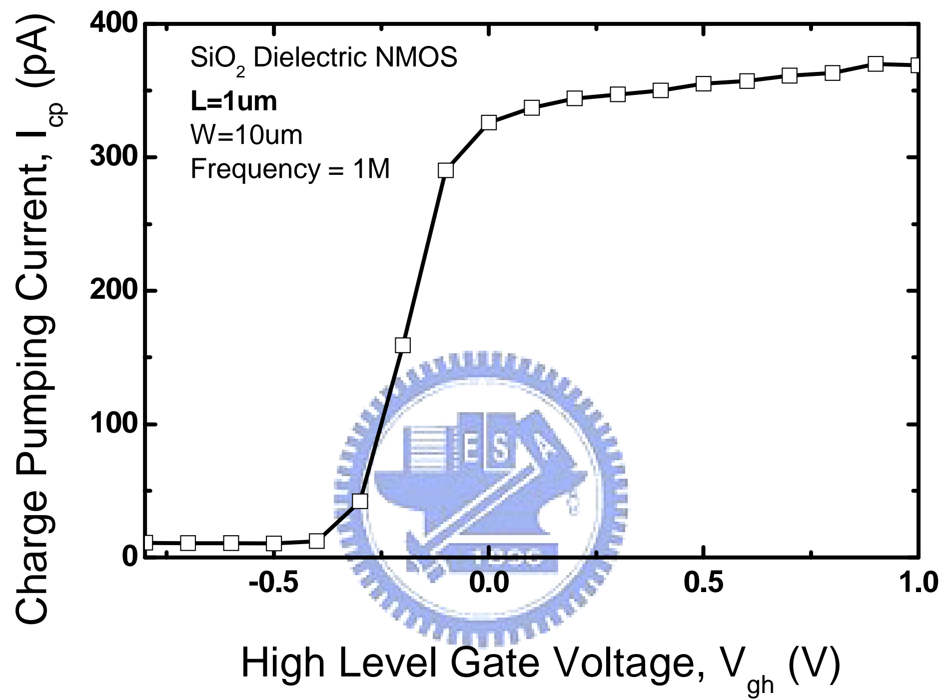


Fig.2.8 Charge-pumping measurement in short channel SiO_2 gate dielectric NMOS device.

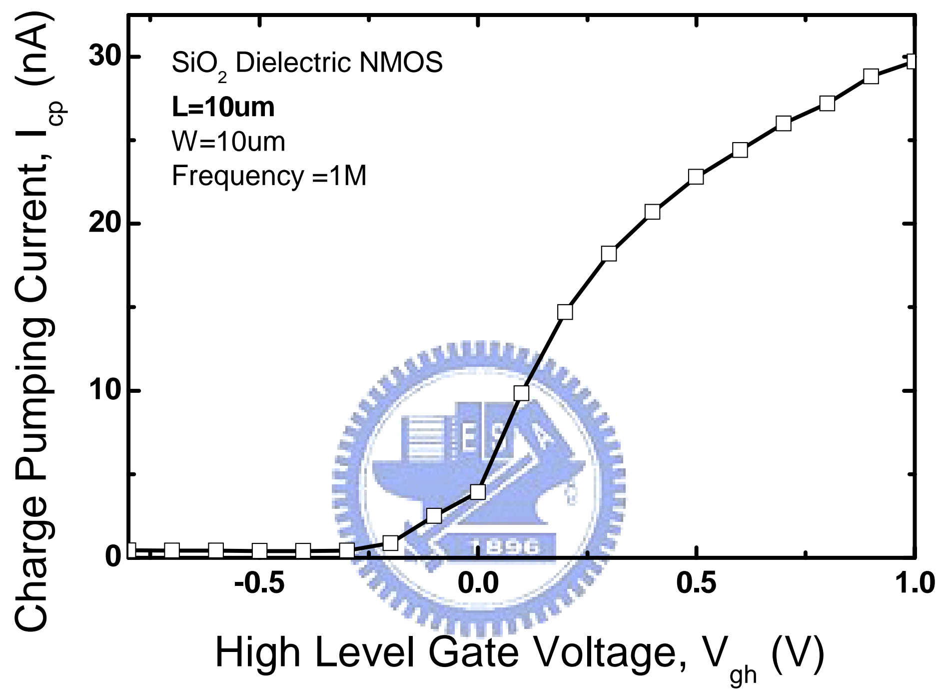


Fig.2.9 Charge-pumping measurement in long channel SiO_2 gate dielectric NMOS device.

Chapter 3

Investigation of the Properties in HfSiON Film

3.1 Introduction

Device scaling is a driving force of semiconductor industry in productivity and performance as predicted by Moor's law. Nano-scale MOSFET transistor and MOS capacitor have reached their fundamental limits and the introduction of new gate dielectric materials has been surveyed and investigated for a continued scaling. As a trade-off for very short channel device length, ultra-thin and high quality gate oxide is strongly needed. Among them, high-K materials as a gate stack has attracted great interest. Recently, HfSiON has been successfully integrated into CMOS as gate dielectrics for low power applications, with good reliability and comparable mobility.

Threshold voltage (V_t) instability induced by charge trapping has been recognized as one of the critical reliability issue in Hf-based high-k gate dielectrics, especially for nMOSFETs under positive bias stress [16]. In general, a defect band filled with plenty of pre-existing high-k traps is positioned above the Si conduction band edge in energy and in the HfSiON bulk layer in space [17]. In other words, these pre-existing high-k traps are distributed in a wide range of space and energy, thus making the charge trapping model different from that of SiO_2. The high-k traps located at deep energy levels are believed to responsible for the C-V hysteresis or V_t instability determined by static I_D-V_G characteristics [3], [18]. And the high-k traps located at shallow energy levels are indicated as the physical origins of stress-induced leakage current (SILC) in HfSiON/IL high-k gate stacks [19]. In addition, the initial high-k bulk trap density has been demonstrated to be highly associated with the event of dielectric breakdown in HfSiON high-k gate dielectrics, thus influencing the device reliability and yield [15].

As reported in literatures, Si atoms could be in corporate into the HfSiON high-k gate dielectric to suppress the dielectric re-crystallization during high temperature rapid thermal annealing (RTA) and to reduce the high-k bulk trap density [20], [21]. Moreover, the thickness of base oxide (IL) plays a significant role in the charging and discharging dynamics of threshold voltage instability, and the tunneling time constant decreases exponentially with the decrease of base oxide thickness [22]. Although thin base oxide thickness is preferred for the continuous scaling of equivalent oxide thickness (EOT) below 1.0nm, this may further degrade the problem of threshold voltage instability due to fast charge trapping, Both the composition of high-k bulk layer and base oxide thickness are being modified to obtain the appropriate high-k gate stack structure with required EOT value and reduce threshold voltage instability.

Although, high-k dielectrics increase the physical thickness, the direct tunneling leakage still exists with EOT (equivalent oxide thickness) scaling down to below 16Å. Therefore, the leakage current will induce measurement error for ultra-thin gate dielectrics CMOS devices. To investigate the properties of HfSiON correctly, we need to eliminate the leakage current during the measurement by the IFCP method. The traps in the HfSiON and interface will be evaluated.

3.2 Device Fabrication

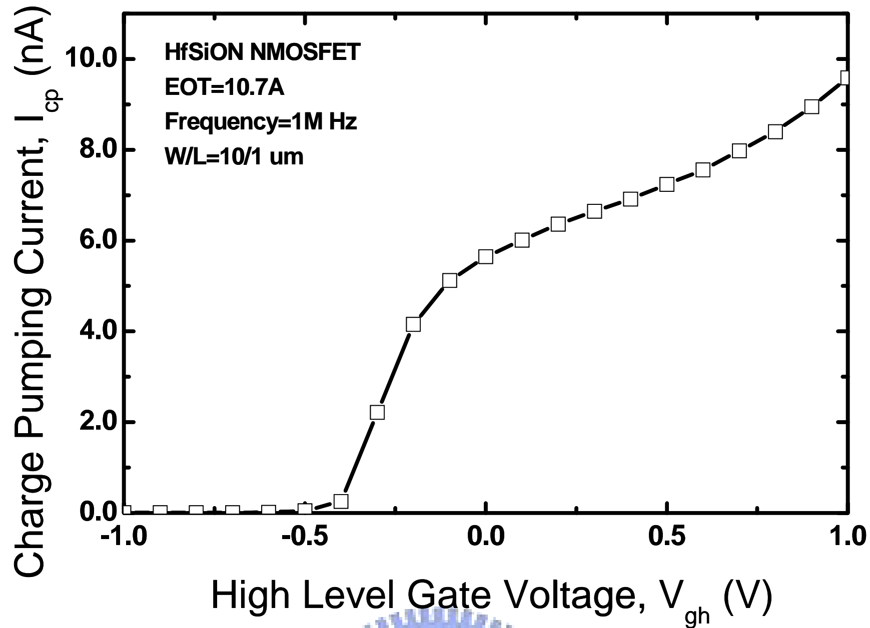
The devices used in this work were fabricated using 90nm CMOS technology. Test samples is nMOSFET which has halo implant with SiO_2 and the effective oxide thickness is 10.7Å. Furthermore, both of the high-k films is HfSiON with different halo implant species including light AMU and heavy AMU.

3.3 Extraction of the Traps in High-K Dielectrics

The technique of charge pumping is frequently used in the study of interface traps by applying a square wave to the gate of the device and measuring the resulting current through the source and drain. The interface traps charge and discharge with a charge pumping current (I_{CP}) directly proportional to frequency f; however, the charge recombined per cycle ($Q_{CP} = I_{CP}/f$ remains the same irrespective of the measurement frequency [10]. In a device, with traps located spatially near Si/IL (interfacial layer) interface, is held in inversion for a period of time longer than the tunneling time constant, then communication may occur between the interface traps and traps in the high-K film. This results in an additional current component and gives rise to an increase of the charge recombined per cycle. In this work, devices fabricated with the HfSiON film are characterized by a high concentration of traps in the high-k film with a well-defined trapping distance, corresponding to the interfacial layer.

Because I_{cp} is proportional to frequency so gate leakage would affect that at lower frequency. In order to gat the accurate product, fig.3.1 shows the lowest (10k Hz) and biggest (1MHz) frequency Charge-Pumping measurements. Fig.3.2 shows the charge pumped per cycle (Q_{cp}) as a function of frequency ranging from 10k Hz to 1MHz. The objective of the latter definition is to eliminate the effects caused by the gate leakage and the tunneling dc currents from source/drain-to-gate overlap [23]. As can be seen in the figure, when the frequency is lower than 500k Hz (this frequency can be regarded as the break-point frequency), Q_{cp} increases clearly with decreasing frequency.

The increase in Q_{cp} can be attributed to the trap-to-trap tunneling of the border-trapped charges close to the HfSiON/ interfacial layer and HfSiON bulk. As the frequency decreases to 10k Hz and lower, data does not show due to the large derivative disturbance resulted from noise signal.



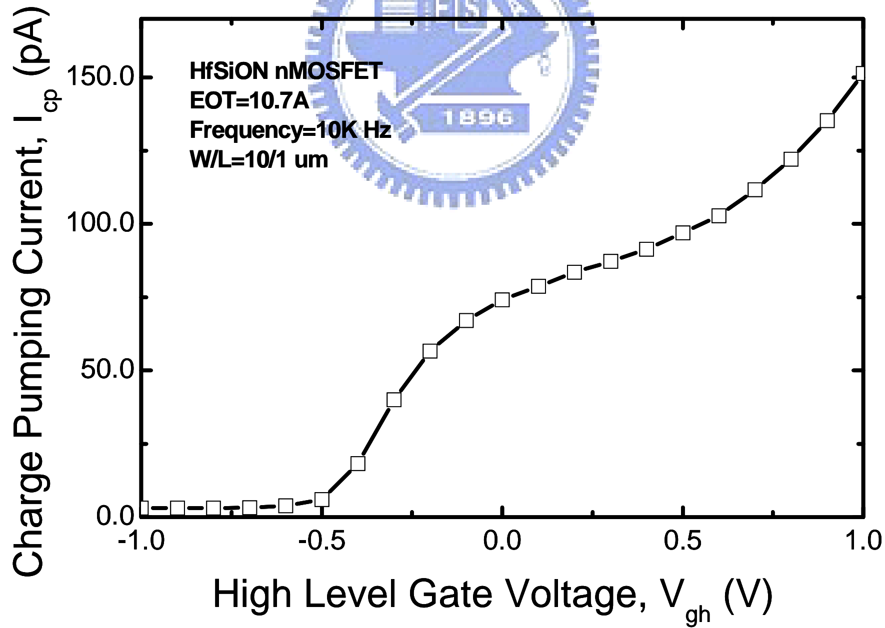


Fig. 3.1 (a) F=1MHz Charge-Pumping measurements. (b) F=10k Hz Charge-Pumping measurements

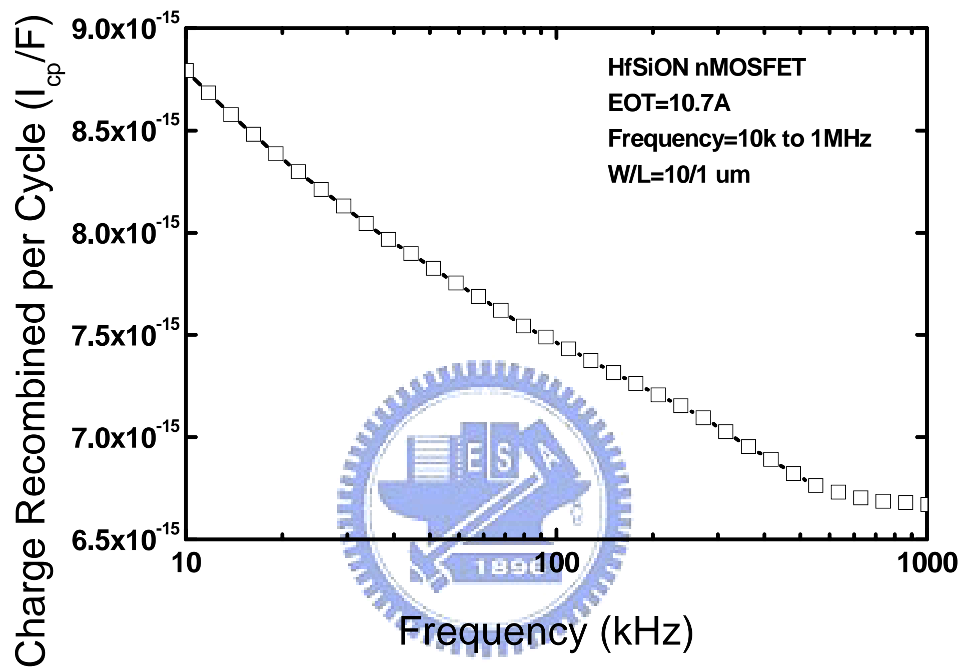


Fig.3.2 The recombined charge per cycle (Q_{cp}) for the high-k device. The charge-pumping current is seen to increase for lower frequencies indicating that the charge pumping current is the sum of an interface trap component and a bulk trap in high-k dielectric.

Beside, at low frequency, nMOS exhibits significantly higher N_t. Such charge trapping in nMOS not only reduces the amount of free carriers in the channel but also serves as additional coulomb scattering centers to lower the electron mobility. N_t of nMOS can be divided into two parts based on its dependence on frequency: one is frequency independent part named as interface traps (N_{it}), which locates at Si/IL interface next to channel with very short time constant. Another is frequency dependent part, which is referred to as oxide traps (N_{hk}) of the HfSiON layer. In this thesis, we will separate the influence of the traps in HfSiON from the influence of interface traps on the charge recombined per cycle in a charge-pumping experiment. Since, by varying the charge-pumping frequency we can sense different fractions of the trap density. Therefore, using the above skill and the time constant of the electron trap-to-band tunneling detrapping process, it will help us to obtain the trap density in the HfSiON away from the interfacial layer.

3.4 Depth Profiling of Traps in MOSFET with High-k Gate Dielectric

3.4.1 Basic Theory

According to the model in [24], the extracted depth profile of border traps in the gate dielectric can be calculated by

$$N_{Hk}(x_m) = -\frac{1}{q\lambda_n A\Delta E_t}\frac{dQ_{cp}}{d\ln(f)} \tag{3.1}$$

where A is the gate area, Q_{cp} the charge pumped per cycle, f the measurement frequency, $\lambda_n = \hbar/2\sqrt{2m_n\Phi_n}$ the attenuation coefficient, Φ_n the potential barrier, and m_n the effective mass of electrons. The factor ΔE_t represents the energy gap in which traps will be allocated by electrons. The rise/fall times of gate pulse in the CP technique of this paper are 10 ns. Such a transient time scans an energy gap of $\Delta E_t = 0.8eV$ [25]. In order to obtain the tunneling distance, x_m as a function of gate frequency was calculated as follows [8], [26]:

$$x_m = \frac{1}{\kappa_0} \ln(t_m \sigma_n \bar{v} n) \qquad (3.2)$$

where κ_0 is the decay constant; $\kappa_0 = 2\lambda_n$, $t_m \approx 1/2f$ the tunneling time, σ_n the capture cross section, $\bar{v}$ the thermal velocity, and n the carrier density. Table 3.1 lists the needed constants.

Fig. 3.3 shows the variation in the volume densities of bulk traps (N_{hk}) along the track of the distance from Si surface. It can be seen that the N_{hk} density in the native oxide ($\approx$1.5–3.7A) varied rapidly near the HfSiON/IL. This is probably caused by the in-complete bonding near the interface [4], [27], [28]. We find a special point ($x_m \approx 3A$) that has the lowest trap density because it is center of IL. A lot of studies have reported that traps in SiO_2 are less than traps in HfSiON can prove above phenomenon. In deeper depth (about 4–6.5 A), a uniform distribution of trap densities about $5*10^{20}/cm^3$ is observed in the HfSiON bulk layer. This indicates that the bulk trap related reliability issues of high-k gated MOSFETs are the same as the formation of the HfSiON/IL interface.

3.4.2 Investigate Short Channel Effect in H-k Dielectric

Fig.3.4 shows the interfacial traps distribution in short channel and long channel length devices. Since the mechanical stress in the edge region is more critical than the center region, the interface traps in the edge is larger than that in the center region. The relation can be distribute as $N_{it,11} \approx N_{it,21}$, $N_{it,12} >> N_{it,11}$, $N_{it,22} >> N_{it,21}$. Fig.3.5(a) shows the trap densities of different channel length devices at varied frequencies. At lower frequencies, C-P measurement senses higher N_t. The flat region, higher frequencies can be as Si/IL interfacial trap density. It is the same as we know that show channel length device has larger interface traps. The Si/IL interface traps of short channel devices (L=0.5 um and L=0.16 um) are more than long channel device (L=1 um). The increase amount of interface traps compared with L=1um are 14% and 20% in L=0.5um and L=0.16um respectively. Than we investigate high-k dielectric traps by N_{cp} minus N_{it}, it is the same as above concept. Fig.3.5(b) shows that. Fig.3.6

shows depth profiling of dielectric traps in different channel length devices. The lager N_{hk} occurs in (IL/HfSiON) interface no matter different channel length. And all the points of lowest N_{hk} are about 3A. It lets us believe that the point is interfacial layer center.

3.5 Dielectric Degradation Phenomenon in nMOS High-k Devices under Static PBTI Stress

3.5.1 Basic Theory

Bias Temperature Instability (BTI) is a degradation phenomenon in MOS Field Effect Transistors (MOSFETs), known since the late sixties on SiO_2 dielectrics. Even though the root causes of the degradation are not yet well understood, it is now commonly admitted that under a constant gate voltage and an elevated temperature a build up of charges occurs either at the interface Si/SiO_2 or in the oxide layer leading to the reduction of MOSFET performances.

As a consequence of both the nitridation process step and the use of surface-channel devices, many researchers ascribed an accelerated BTI-like degradation of pMOSFETs under negative bias and elevated temperatures, the so-called NBTI (Negative Bias temperature Instabilities) effect [29], [30]. Unlike SiO_2, the high-K dielectrics such as Hf-based dielectrics present serious instabilities for negative and positive bias, after NBT and PBT (Positive Bias Temperature) stresses. The trapped charges are sufficiently high to represent one of the high-K integration's most critical showstopper. The instability is worrying, especially in the case of nMOS PBTI. In this section we present a review of process optimizations found in the literature. A new experimental methodology is also presented in order to asses with accuracy the real degradation and allows us to argue on possible PBTI mechanisms.

	Value
Φ_n	3.1 (eV)
m_n	4.6E-31 (Kg)
ΔE_t	0.8 (eV)
κ_0	5E-9
σ_n	5E-18 (cm^2)
$\overline{v}$	1E6 (cm/s)
n	6E18 (1/cm^3)
$\hbar$	1.05E-34 (kg*m^2/s)
λ_n	7.8E-11

Table 3.1 Parameters of constant and physical in depth profiling of traps.

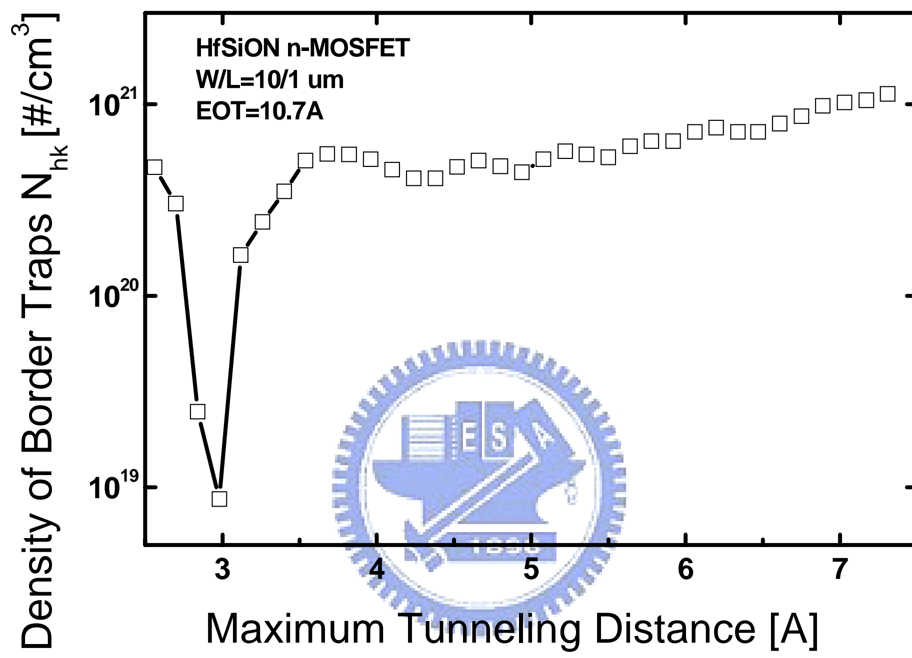


Fig 3.3 Volume densities of bulk traps in gate dielectric as a function of the distance from Si surface.

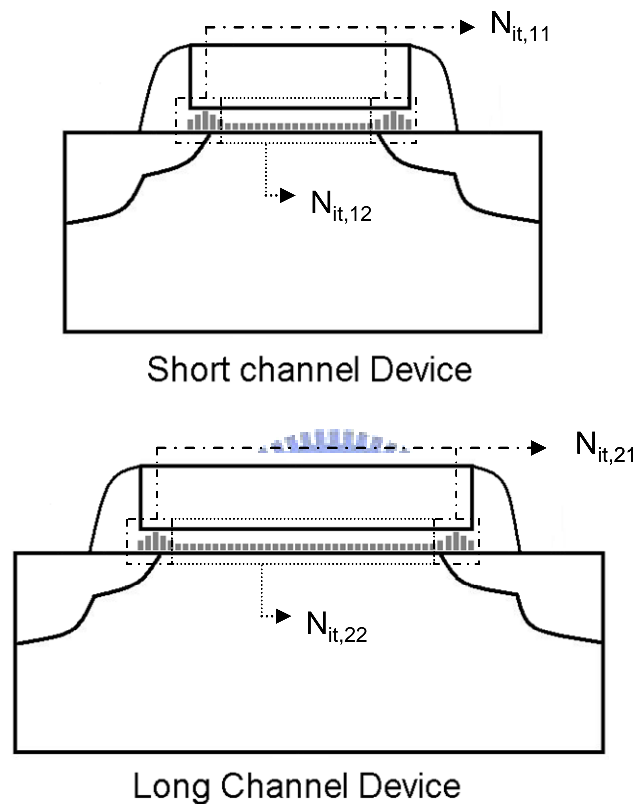
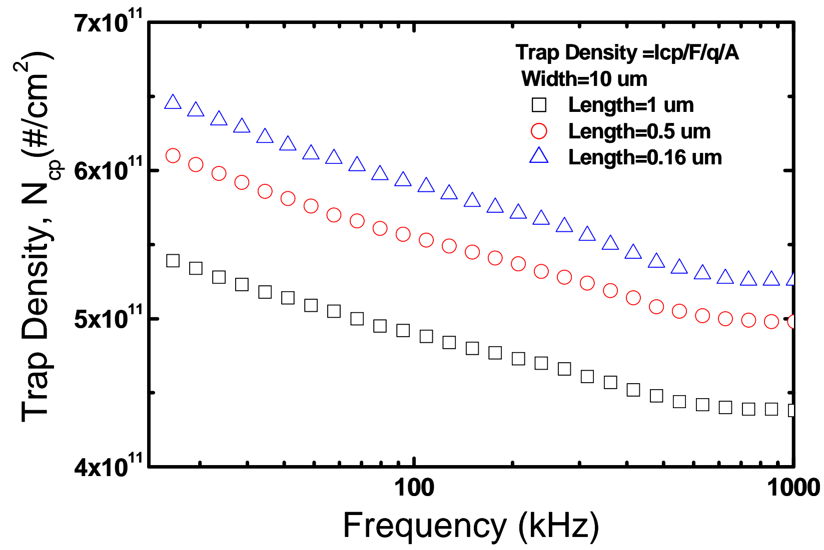
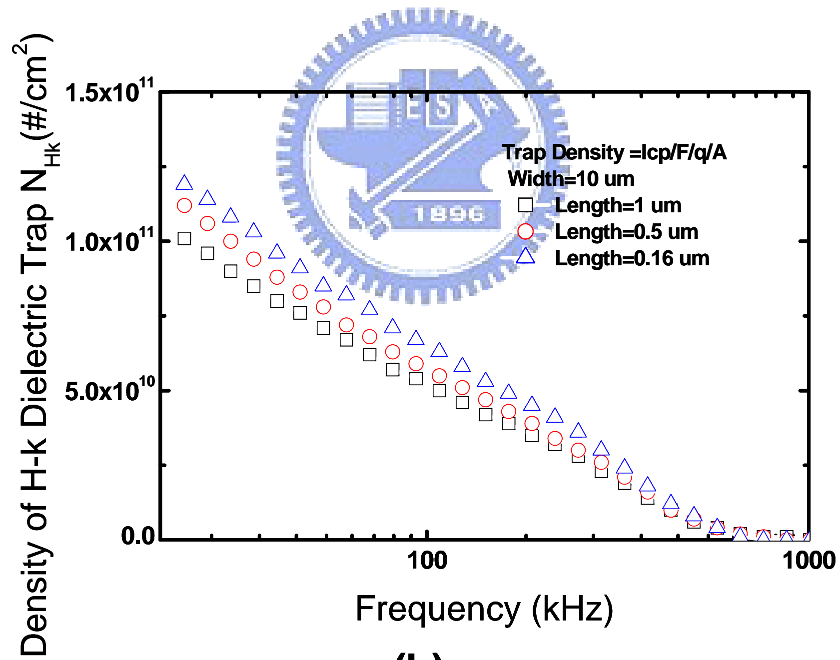


Fig. 3.4 Interface traps distribution in short and long channel length devices.



(a)



(b)

Fig. 3.5 (a) The trap densities of different channel length devices at varied frequencies. (b) The H-k dielectric trap densities of different channel length devices at varied frequencies.

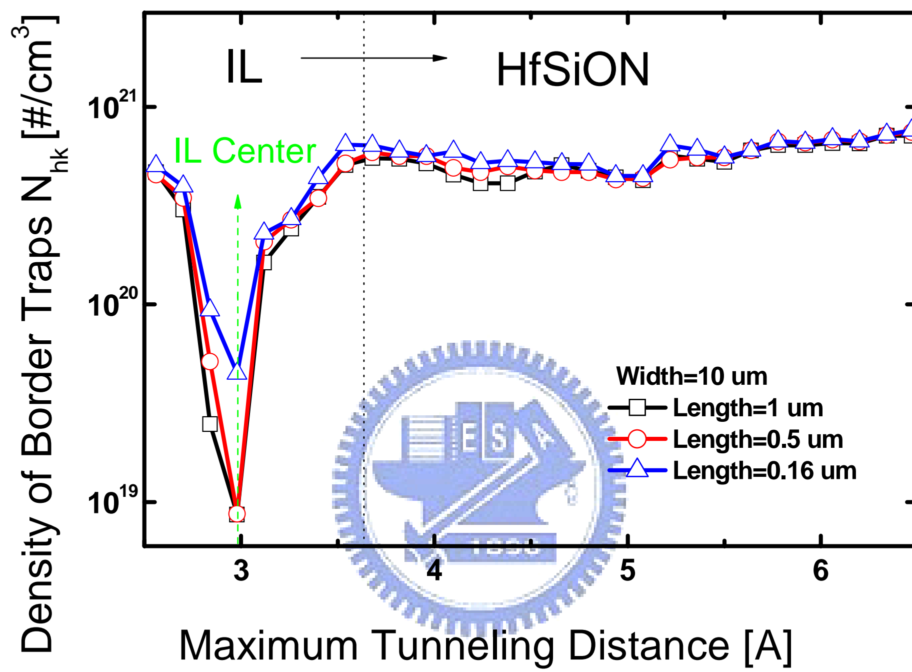


Fig 3.6 Volume densities of bulk traps in gate dielectric of different lengths as a function of the distance from Si surface.

3.5.2 Charge Trapping and De-trapping Behaviors during Static PBTI Stress

Fig. 3.7 shows the nMOS band diagram after stress, and the traps in HfSiON dielectric will capture electrons to induce more traps in HfSiON dielectric. However some electrons with lower energy may recover back into the cahnnel naturally. This would affect the measured result. In charge pumping measurement, too large gate voltage may increase trapping electrons and the negative low level bias may cause de-trapping. That would induce experimental error. Therefore we use one point charge pumping measurement to measure the traps change with stressing devices. In classic I_{cp} curve, we choose one point that high level gate voltage is higher than threshold voltage and low level gate voltage is lower than flat-band voltage to measure charge pumping current. This method can avoid the above issues in measurement. On the other hand, after stress we should de-trap by negative bias for ultra-small time. It can let the lower energy electrons de-trap more quickly.

Fig.3.8 shows the difference of stress process with de-trapping and without de-trapping. Charge pumping current of process with de-trapping is larger because the step lets electrons leave and produce more vacant traps to sense I_{cp}.

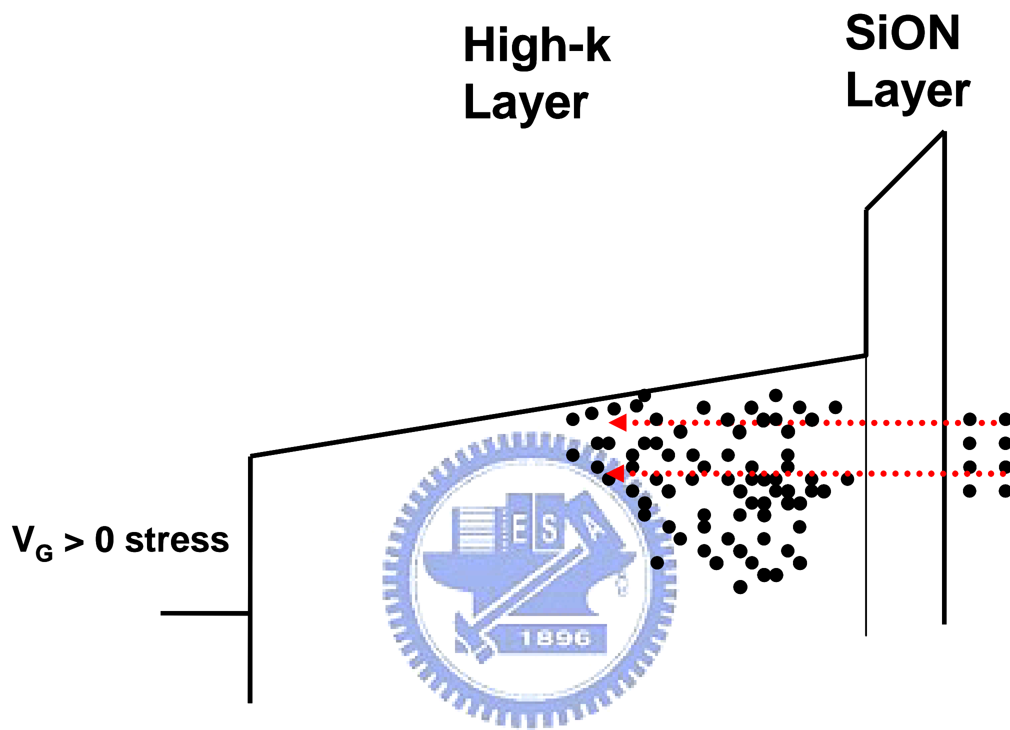
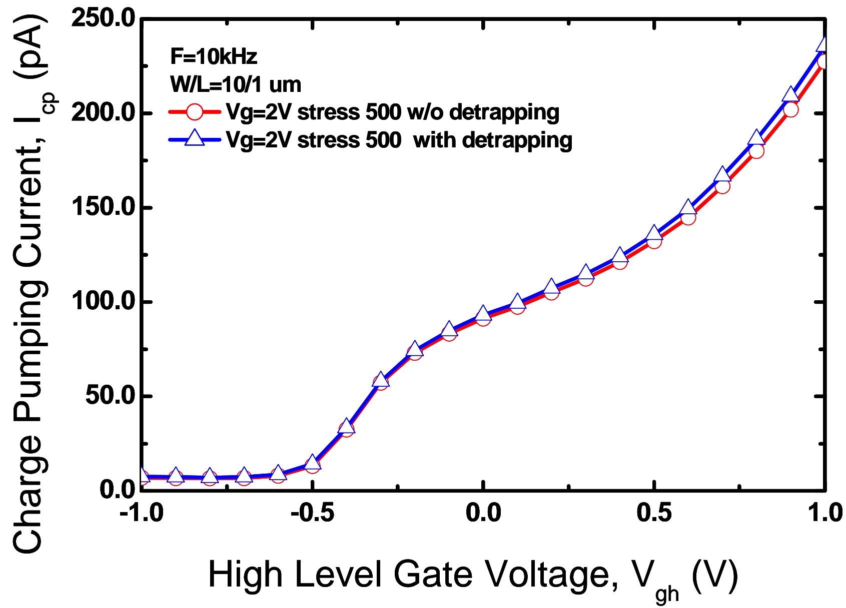
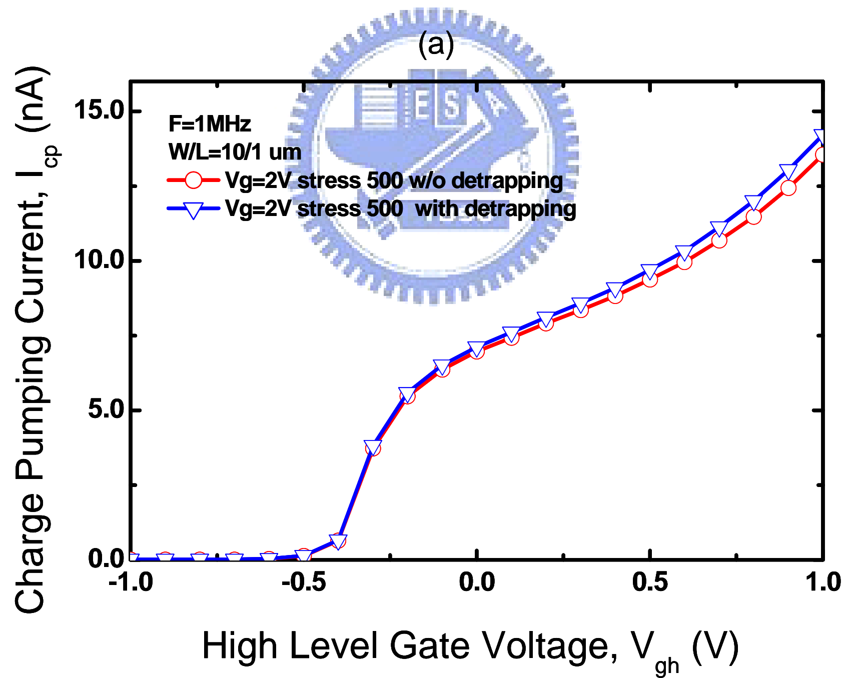


Fig.3.7 Schematic band diagram of SiON/HfSiON gate stack for substrate injection. High energetic electrons arrive at the anode.



(a)



(b)

Fig.3.8 (a) Low frequency (10kHz) I_{cp} of with de-trapping and without de-trapping. (b) High frequency (1MHz) I_{cp} of with de-trapping and without de-trapping.

3.5.3 Result and Discussion

The schematic diagram of the stress and measurement sequence is shown in Fig.3.9. And fig.3.10 shows one point charge-pumping current varied after different PBTI stress. Charge pumping current is proportional to frequency high and low. No matter any frequencies, we can find the higher temperature has the large charge pumping current. That is because the higher temperature stress will induce more electrons to have enough energy to be charged in traps and bring more and more traps in high-k dielectric.

Fig.3.11 shows the trap densities as function of frequency measured on the original MOS device, after PBTI stress of different temperatures. The break point frequency found for original and after stressing devices, which is about 700kHz. Furthermore, the amount of trap density obtained for device after stressing is apparently higher than the original device. This indicates that a number of weak bounds hidden near the Si/high-k interface can be induced as border traps after stressing. And higher stress temperature would induce more trap density increase.

Fig.3.12 shows the volume densities of bulk traps in gate dielectric as a function of distance from Si surface, extracted from the trap densities versus frequency curves before and after different temperatures of PBTI stress. It can be seen that N_{hk} density in the dielectric bulk (~2.5-7.5A) has an apparent increase after stress. However, the stress-induced bulk traps would more and more as stressing and burning stressing.

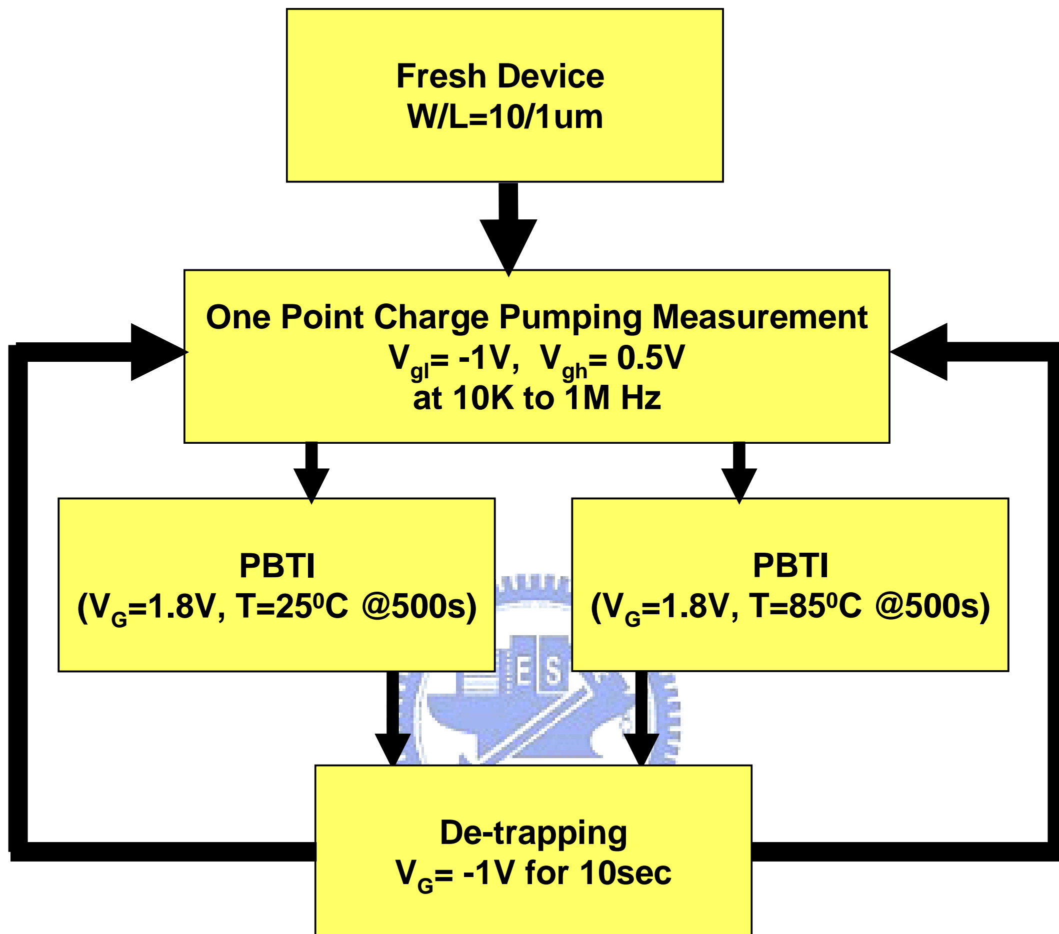


Fig. 3.9 The measurement flow used to monitor the trap generation. Before each set of charge-pumping measurements, a short non-stressing negative voltage is applies.

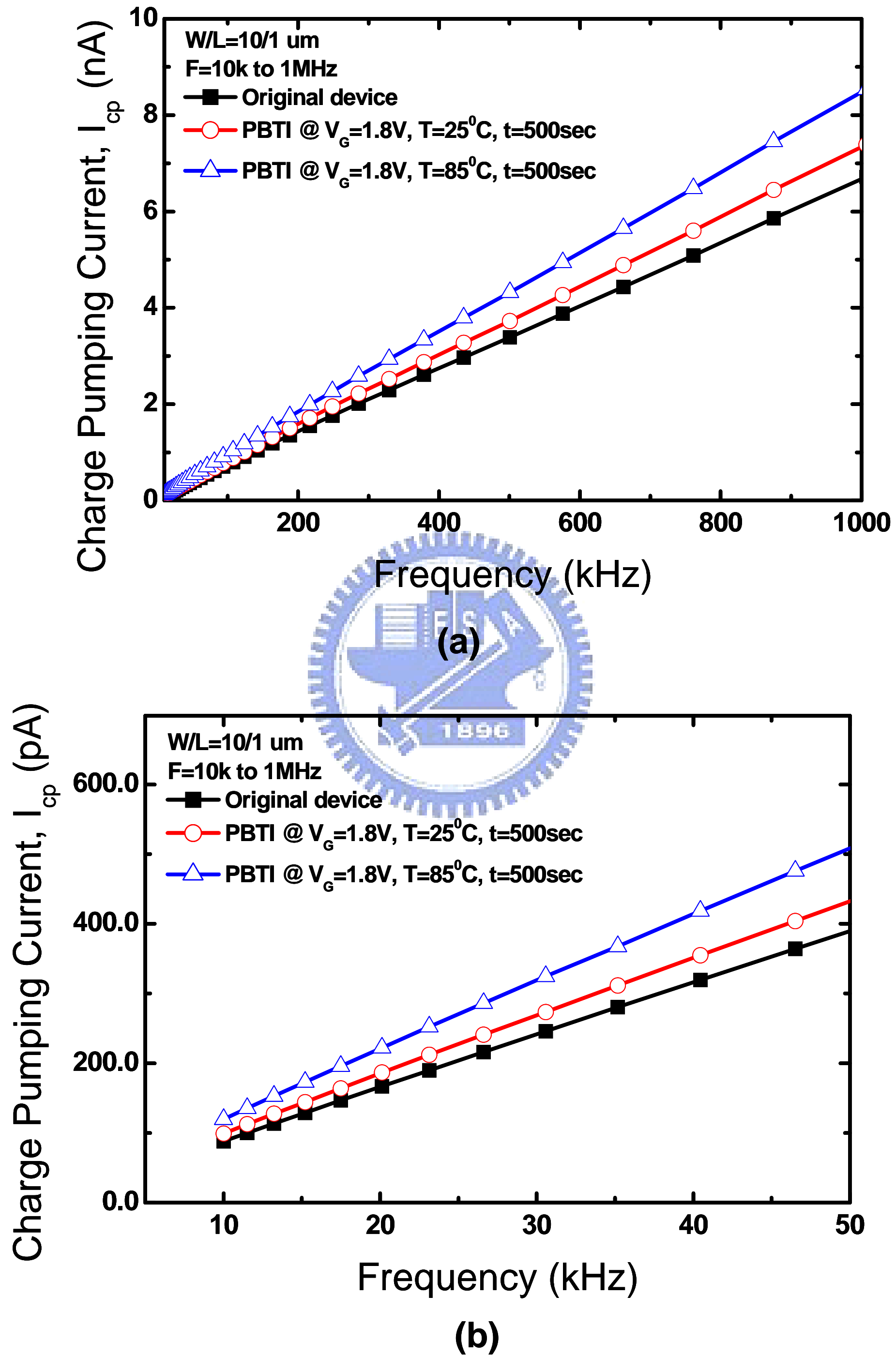
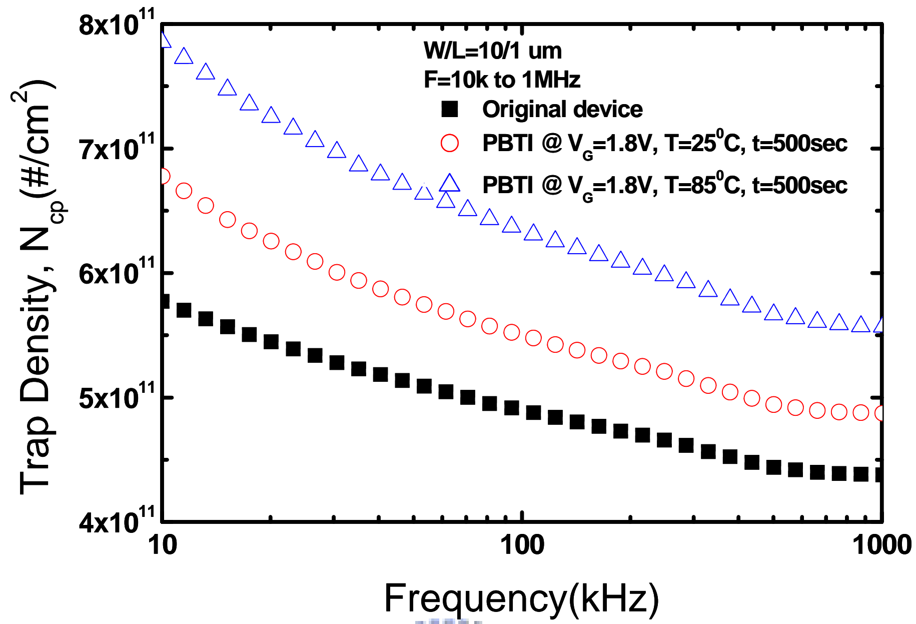


Fig. 3.10 (a) PBTI stress induces charge-pumping current varied. (b) Amplify the lower frequencies charge-pumping current.



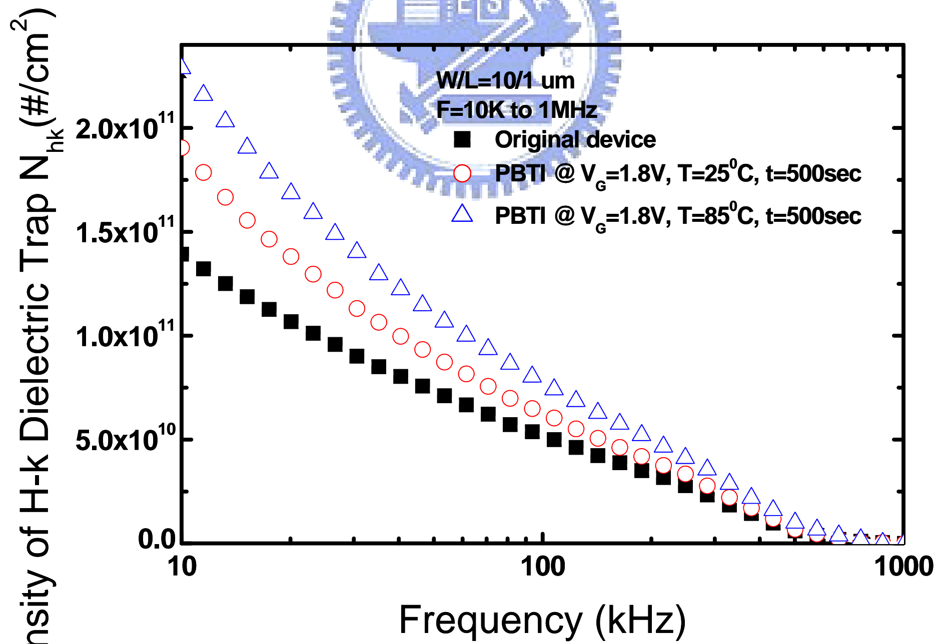


Fig. 3.11 (a) The trap densities of different temperature stress at varied frequencies. (b) The high-k dielectric trap densities of different temperature stress at varied frequencies.

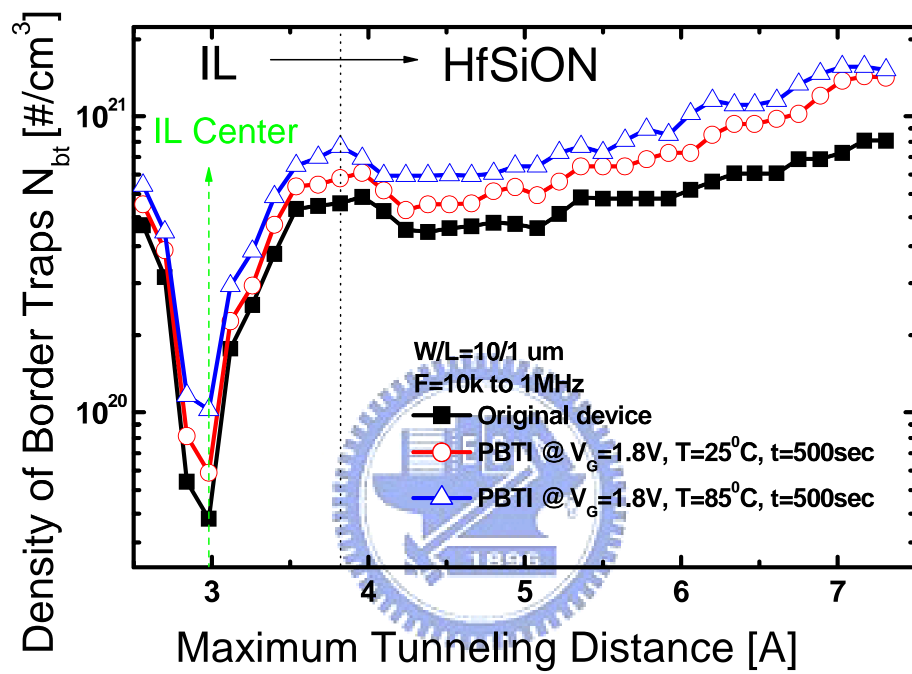


Fig.3.12 Volume densities of bulk traps in gate dielectric of different temperature stress as a function of the distance from Si surface.

3.6 Summery

In this chapter, we combine IFCP method and trap-to-band tunneling time constant to obtain trap position in the HfSiON. The IFCP method improves traditional charge pumping measurement by eliminating direct tunneling leakage current in ultra-thin gate dielectric films for MOS devices, and helps us to calculate more accurate traps in the HfSiON. On the other hand, we successfully separate N_{it} and N_{hk} with IFCP method for high-k dielectrics.

Using this method to investigate N_{hk} in different channel length devices and in different stress condition, we find the break point frequency is similar at trap density versus frequency chart and IL center is fixed to the same point at N_{hk} versus the distance of trap position away from Si surface chart.

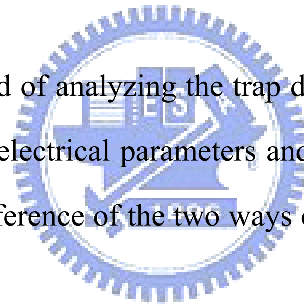
The results in this chapter show that there are more bulk traps existing in the high-k gate dielectric than in the SiO_2 one. Experimental results indicate that the weak bonds present in high-k gate dielectric are easily trapped by charges after stressing; thus, stress results in a large V_{th} shift. In addition, a novel CP extraction technique has been proposed to measurement the spatial of the near-interface traps in the gate dielectric of high-k gated MOSFETs.

Chapter 4

Stress Voltage Polarity Dependence of Trap Generation

4.1 Introduction

The reliability of nMOS has been investigated in the past using PBTI stress method. With the continuous shrinking of the transistor dimension, new reliability issues emerge. During the operation of a n-MOSFET in a CMOS inverter, the applied gate bias (input signal) is switching between “high” and “low” voltages, while the drain bias (output signal) is alternating between “low” and “high” voltages, correspondingly. Therefore, it is critically important to investigate stress voltage polarity dependence of trap generation in transistor.



Thus, in this chapter, the method of analyzing the trap density is the same as before: under 1.8V of operating voltage, the variation of electrical parameters and reliability during positive and negative stress of the device. Moreover, the difference of the two ways of stress is compared for the problems in circuit systems.

4.2. The Devices under Test

The devices used in this work were fabricated using 0.09μm CMOS technology. In this section, we use the devices with gate dielectric thickness (EOT= 10.2Å) to investigate the positive and negative bias stress with different halo implant species with halo B and halo BF_2, respectively.

4.3 Results and Discussion

4.3.1 Comparison of halo B device before and after stress

The change of threshold voltage with positive and negative stress is shown in Fig.4.1. When the

device is under positive stress, the nMOS is in inverse mode. The electrons in the channel would be captured by the traps located at the interface and the high-k gate dielectric, and the threshold voltage would be increased by the accumulation of the electrons. In negative stress mode, the nMOS is in the accumulation state, and therefore the threshold voltage would be decreased by the holes captured by the traps at the interface and in the high-k dielectric. As a result, the absolute value of ΔV_t would get larger with the stressing time, and makes a direct proportion in the logarithmic axis.

The plot of drain current versus gate voltage under different positive stress time is shown in Fig.4.2. We could see that the there is a right shift of the drain current with the stress time, and the magnitude of the shift is equal to the V_t shift. Fig.4.3 shows the drain current under stress time of 2000 seconds after a left shift of 0.088V, and we found out that this curve is the same as the original curve so it could be proved that the drain current shift caused by the positive stress is the V_t shift.

The change of drain current versus gate voltage under different negative stress time is shown in Fig.4.4, and it could be seen that the slope of the former half of the drain current has changed. It could be used to calculate the subthreshold swing by the slope. Fig.4.5 shows the subthreshold swing under different stressing time. With the stress time increasing, the subthreshold swing would also get increased and thus makes the device turned on more slowly.

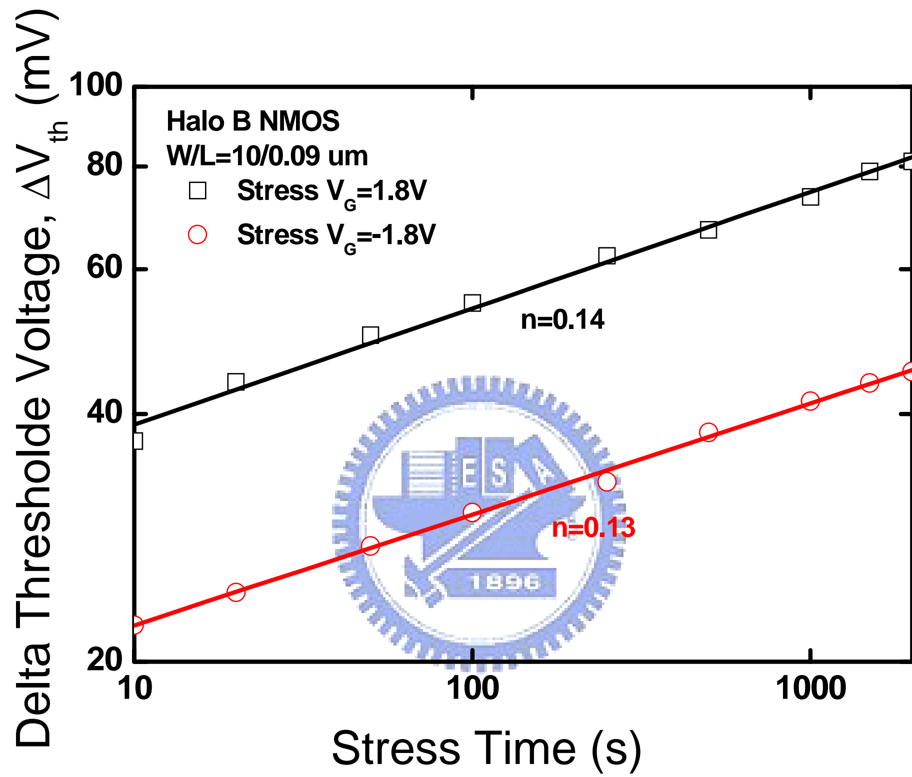


Fig.4.1 Delta threshold voltage of halo B device with positive and negative stress.

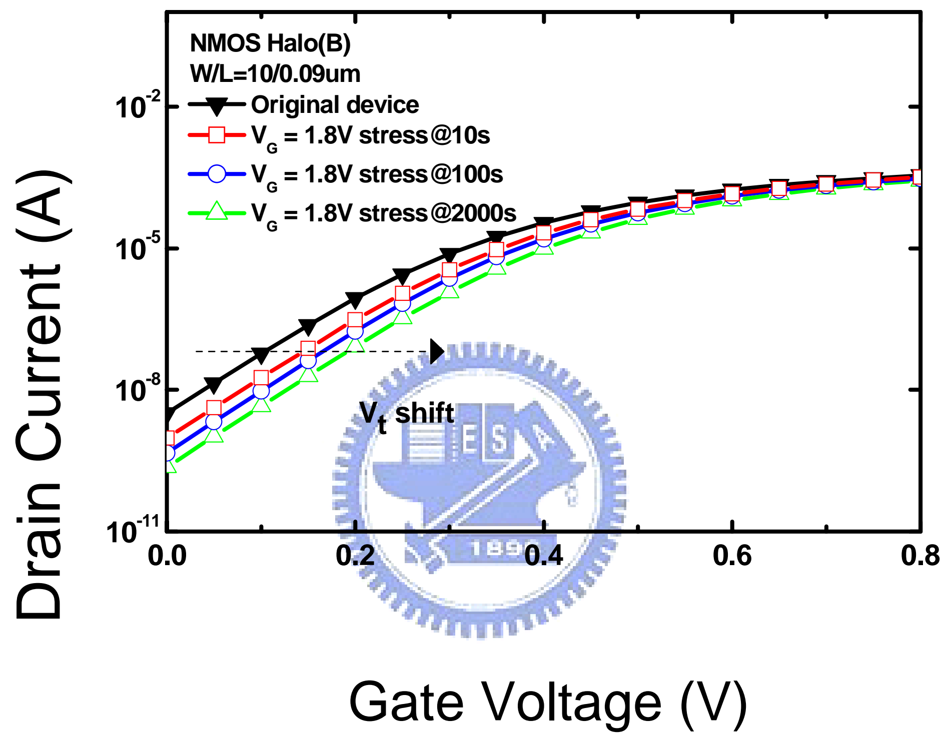


Fig.4.2 Drain current of halo B device versus gate voltage under different positive stress time.

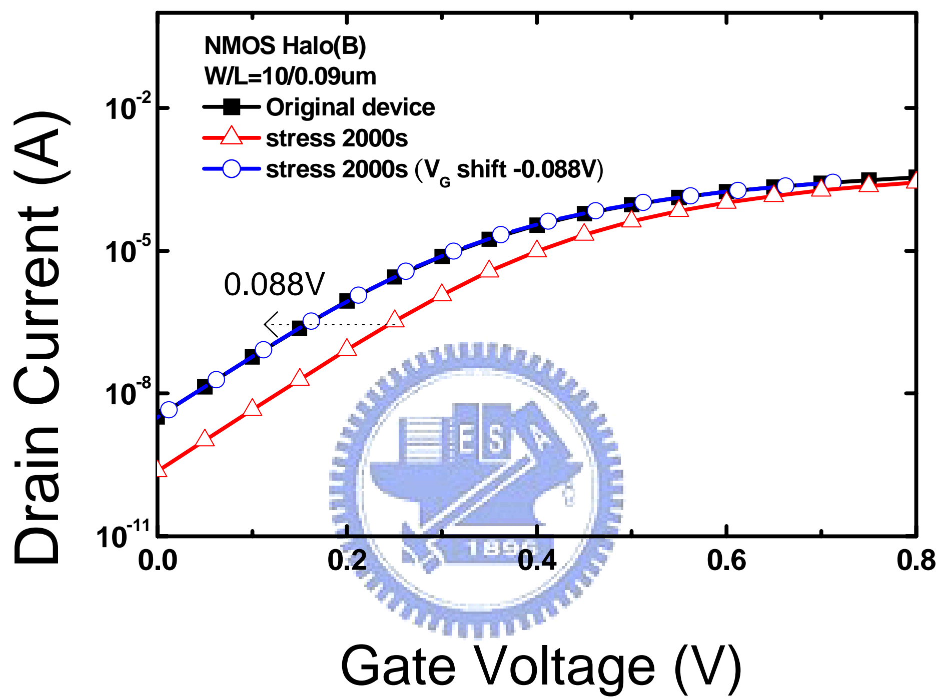


Fig.4.3 The drain current of halo B device under stress time of 2000 seconds after a left shift of 0.088V will coincide with the curve of original device.

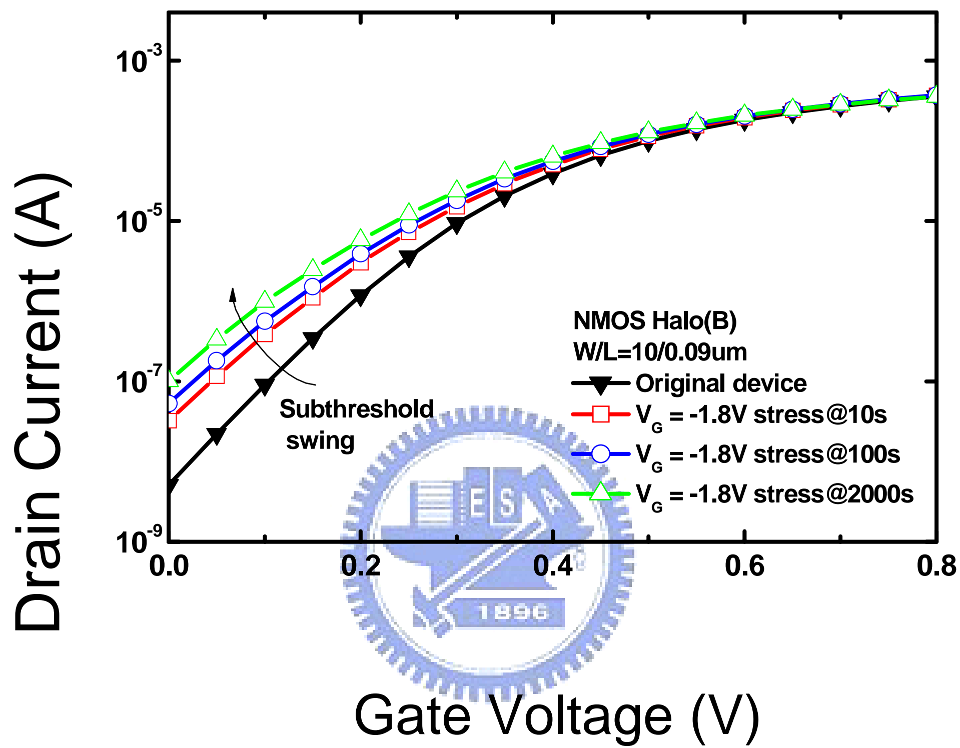


Fig.4.4 The change of drain current of halo B device versus gate voltage under different negative stress time.

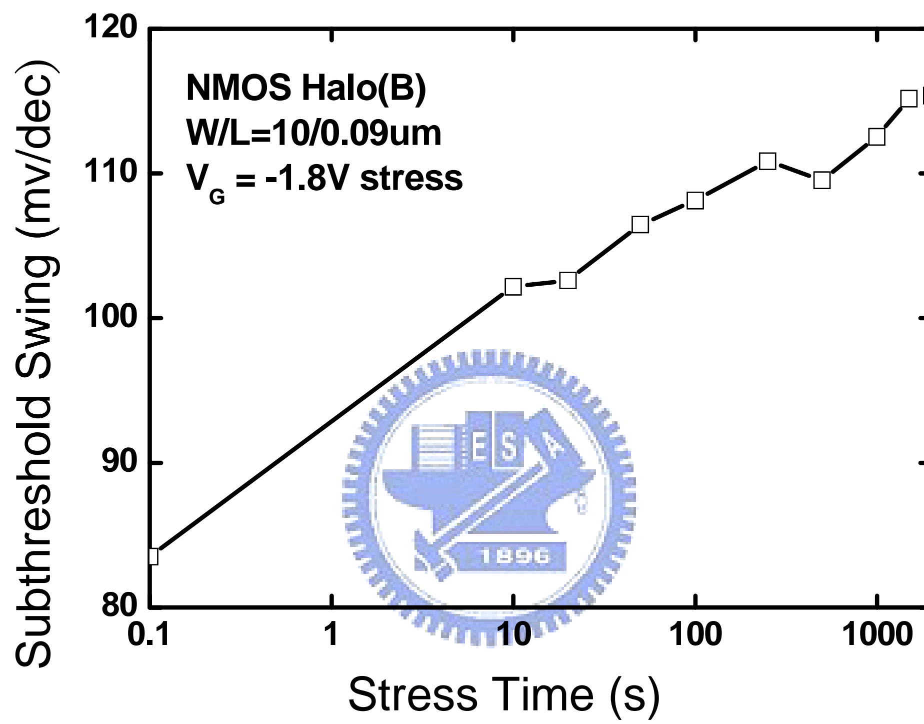


Fig.4.5 The subthreshold swing calculated by the slope of drain current curve in halo B device.

Next we utilize the method mentioned of CP measurement in chapter 3 to observe the variation of trap located at different depths. The trap density close to the Si interface could be detected by using higher frequency, and the lower frequency could be used to detect the trap density from the interface to the high-k gate dielectric. Thus, 1MHz was chosen as a high frequency to measure the Si/IL interface trap density, and 10kHz was for the Si interface to the high-k gate dielectric trap density. At last, the trap density in the high-k bulk only is calculated by the trap density from 10K Hz subtracted by the one from 1MHz.

Fig.4.6 shows the variation of interface trap density in positive and negative stress modes under different stress time. It is discovered that more damages occurred at the Si/IL interface by the negative stress mode, and more traps are generated. The change of high-k gate dielectric trap density in both stress modes under different stress time is shown in Fig.4.7, and it could be seen that a larger amount of damage would be produced under positive stress so the number of traps generated are much larger.

When V_D is small, $I_D=(\frac{W}{L})\,\mu C_{ox}(V_g-V_t)V_D$ and $G_m=\frac{\partial I_D}{\partial Vg}=\mu C_{ox}\frac{W}{L}V_D \Rightarrow G_m \propto \mu$. Gm could be used to obtain the change of mobility during stressing. Fig.4.8 shows the change of $G_{m,max}$ in positive and negative stress under different stress time. Apparently, the negative stress mode would impose a large decrease on the mobility. Consequently, according to the experimental results, the damage to the device from negative stress is far more than what we've imagined, which is a new discovery for us.

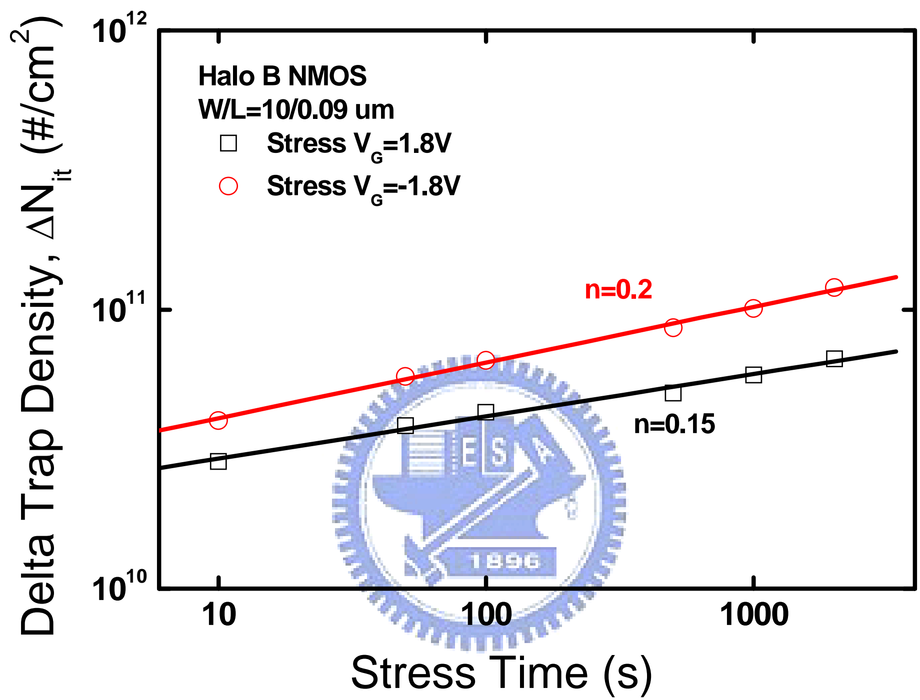


Fig.4.6 The variation of interface trap density of halo B device in positive and negative stress modes under different stress time.

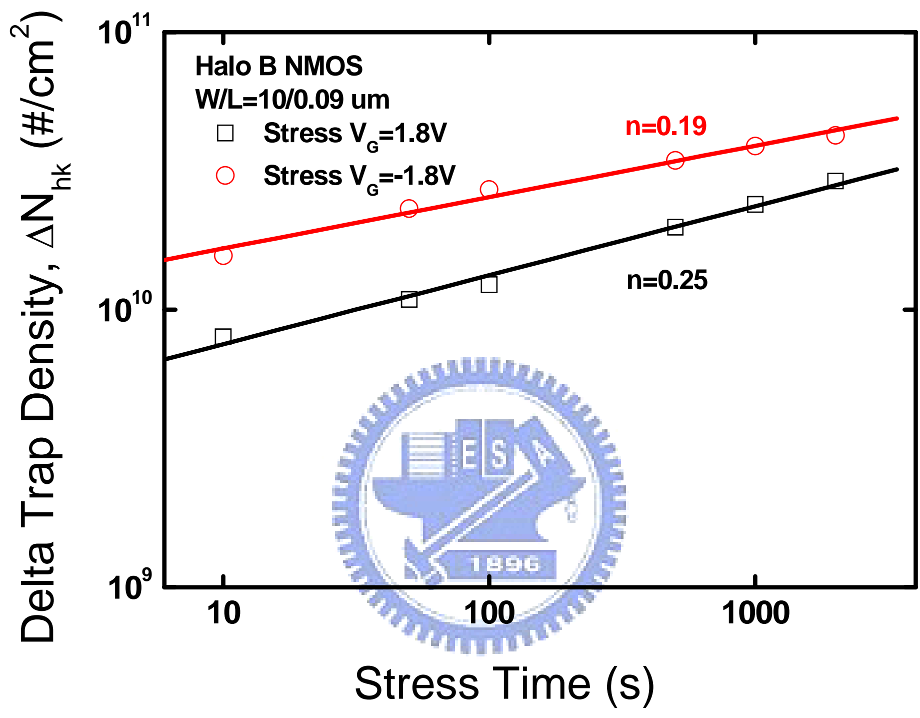


Fig.4.7 The change of high-k gate dielectric trap density of halo B device in both stress modes under different stress time.

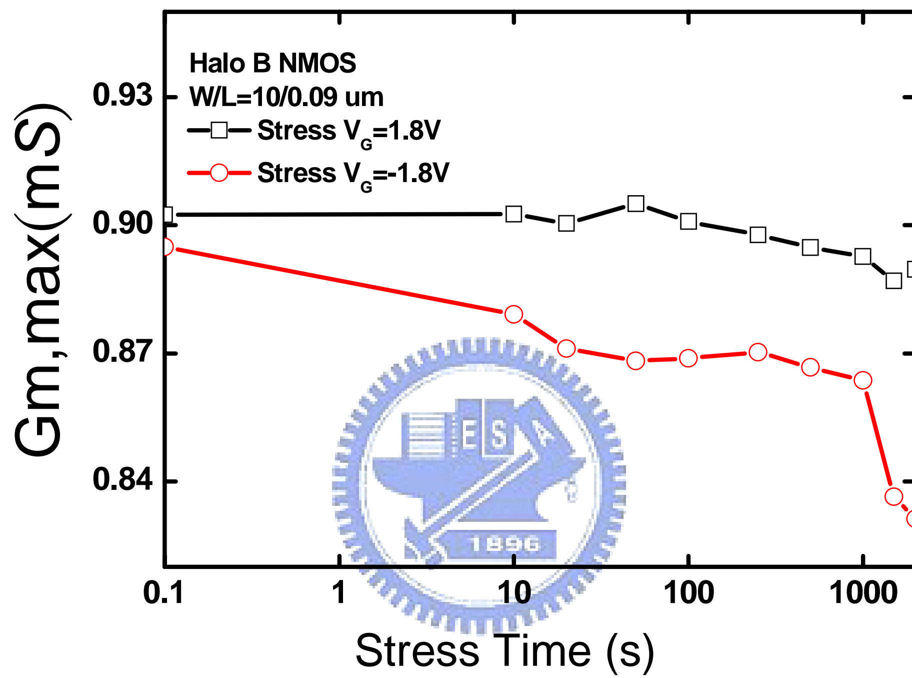


Fig.4.8 The change of $G_{m,max}$ of halo B device in positive and negative stress under different stress time.

4.3.2 Comparison of halo BF_2 device before and after stress

The change of threshold voltage with positive and negative stress is shown in Fig.4.9 When the device is under positive stress, the nMOS is in inverse mode. The electrons in the channel would be captured by the traps located at the interface and the high-k gate dielectric, and the threshold voltage would be increased by the accumulation of the electrons. In negative stress mode, the nMOS is in the accumulation state, and therefore the threshold voltage would be decreased by the holes captured by the traps at the interface and in the high-k dielectric. As a result, the absolute value of ΔV_t would get larger with the stressing time, and makes a direct proportion in the logarithmic axis.

The plot of drain current versus gate voltage under different positive stress time is shown in Fig.4.10. We could see that the there is a right shift of the drain current with the stress time, and the magnitude of the shift is equal to the V_t shift. Fig.4.11 shows the drain current under stress time of 2000 seconds after a left shift of 0.1V, and we found out that this curve is the same as the original curve so it could be proved that the drain current shift caused by the positive stress is the V_t shift.

The change of drain current versus gate voltage under different negative stress time is shown in Fig.4.12, and it could be seen that the slope of the former half of the drain current has changed. It could be used to calculate the subthreshold swing by the slope. Fig.4.13 shows the subthreshold swing under different stressing time. With the stress time increasing, the subthreshold swing would also get increased and thus makes the device turned on more slowly.

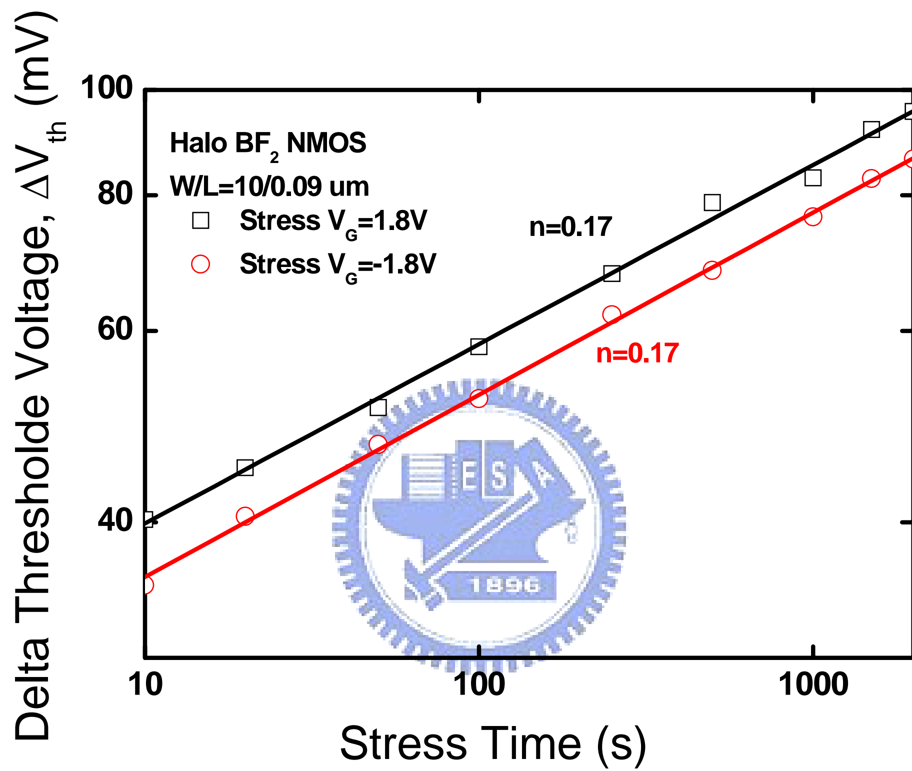


Fig.4.9 Delta threshold voltage of halo BF_2 device with positive and negative stress.

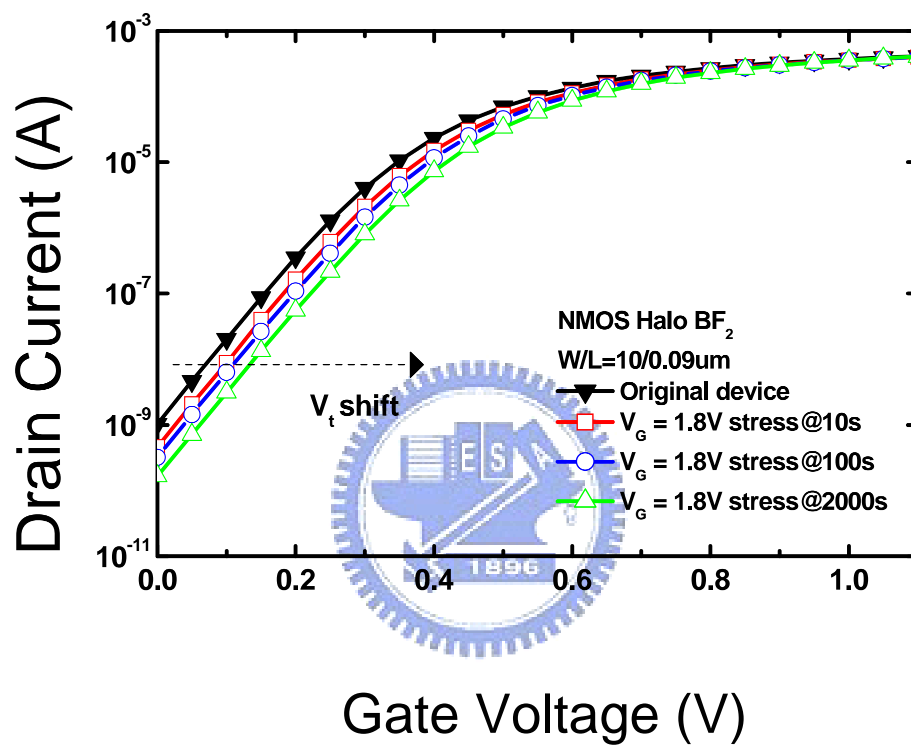


Fig.4.10 Drain current of halo BF_2 device versus gate voltage under different positive stress time.

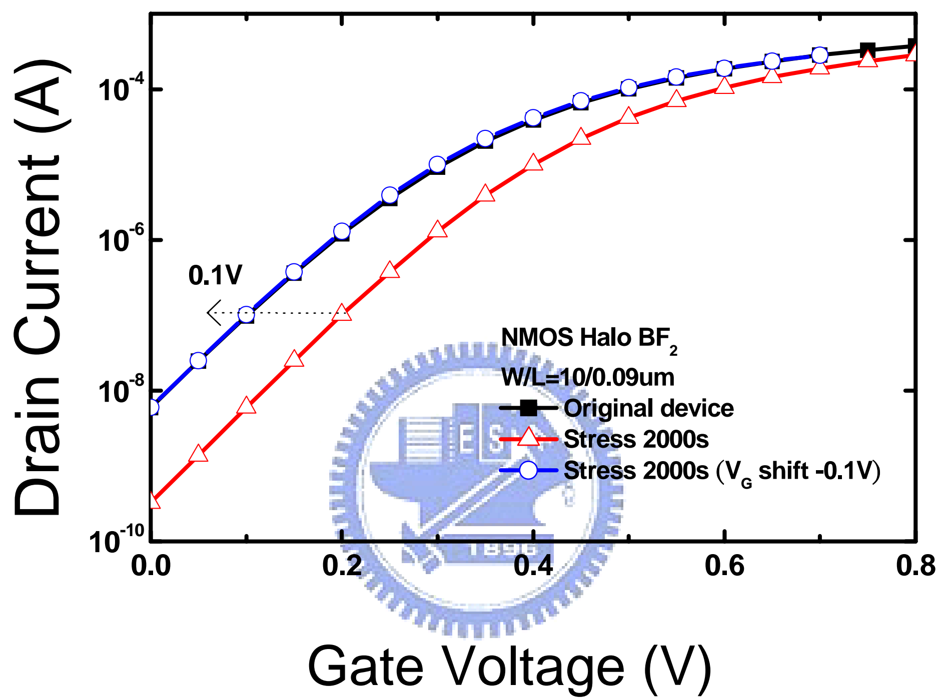


Fig.4.11 The drain current of halo BF_2 device under stress time of 2000 seconds after a left shift of 0.088V will coincide with the curve of original device.

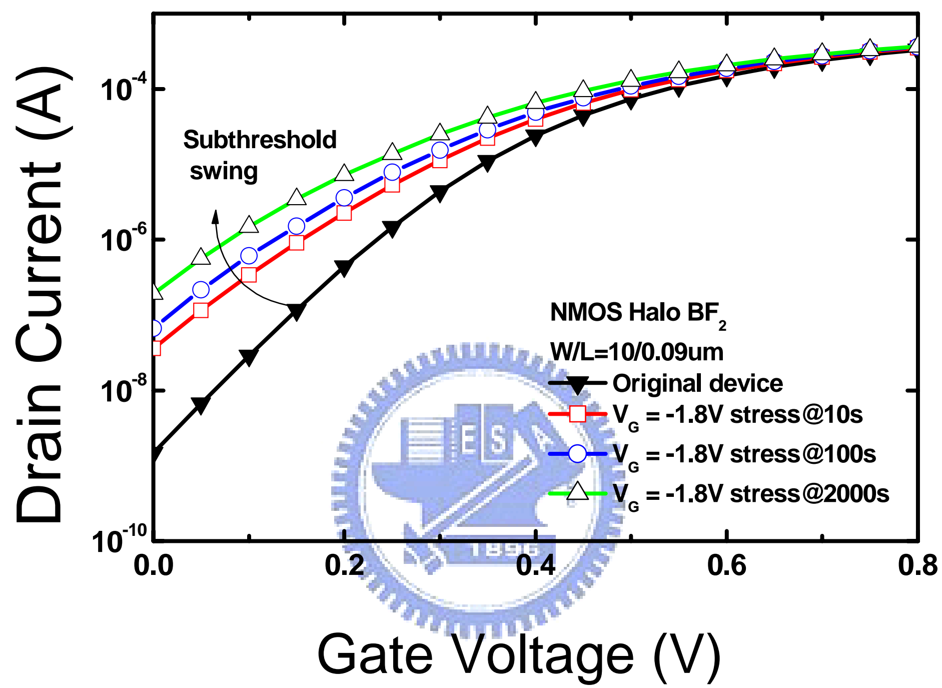


Fig.4.12 The change of drain current of halo BF_2 device versus gate voltage under different negative stress time.

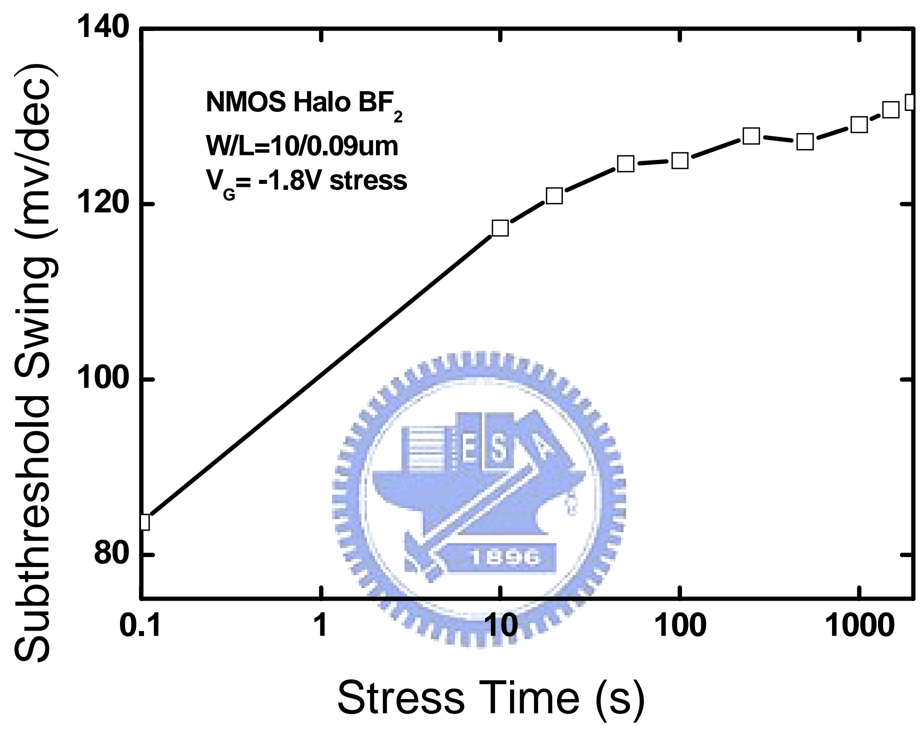


Fig.4.13 The subthreshold swing calculated by the slope of drain current curve in halo BF_2 device.

Next we observe the variation of trap located at different depths utilize the method mentioned of CP measurement in chapter 3 to. Fig.4.14 shows the variation of interface trap density in positive and negative stress modes under different stress time. It is discovered that more damages occurred at the Si/IL interface by the negative stress mode, and more traps are generated. The change of high-k gate dielectric trap density in both stress modes under different stress time is shown in Fig.4.15, and it could be seen that a larger amount of damage would be produced under positive stress so the number of traps generated are much larger. This is the point which is different from Si/IL interface trap density generation. Fig.4.16 shows the change of $G_{m,max}$ in positive and negative stress under different stress time. Apparently, the negative stress mode would impose a large decrease on the mobility. The same result is obtained from both kinds of devices after positive and negative stress. That is, the damage to the device from negative stress is far more than what we have imagined, which is a new discovery for us.

4.3.3 Difference between halo B device and halo BF_2 device

Accompanied with the progress of VLSI device scaling techniques, the importance of the short channel effect could not be ignored, which is caused by the ultra-short channel length, and a channel current is generated when the device is in its off state. Halo implantation is often applied to suppress this phenomenon. In this section, different materials of halo implantation are compared. Fig.4.17 shows the off-state drain current of two different halo devices in different channel lengths under V_G=0V, V_D=1.5V. The I_{off} would get larger when the length is getting shorter. The I_{off} of halo BF_2 would be smaller than the one of halo B, and this may be due to the bigger molecular volume of BF_2 which makes the pocket closer to the junction and decreases I_{off} more effectively.

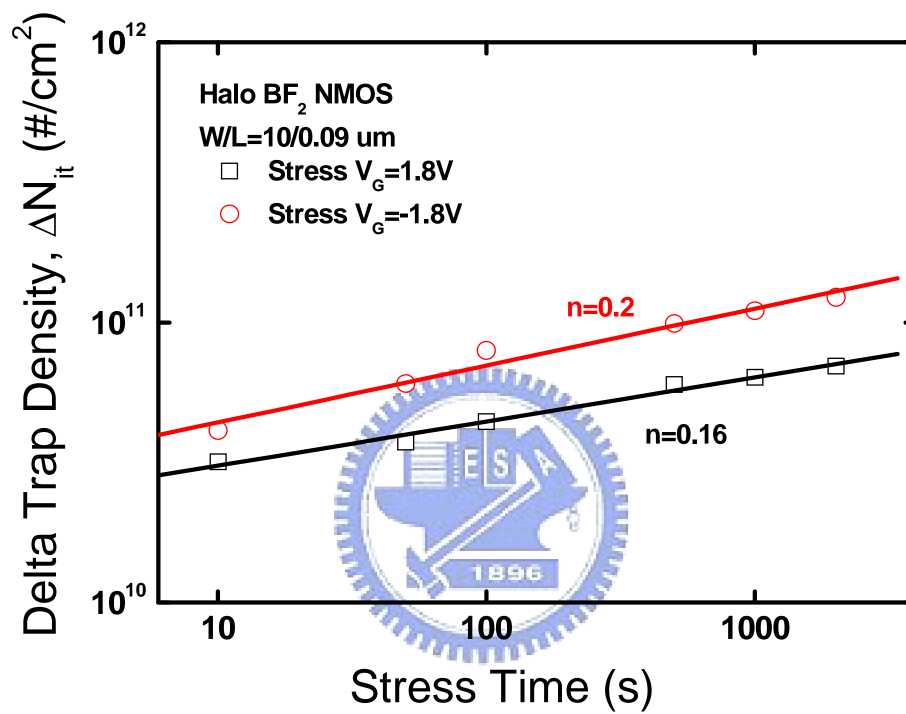


Fig.4.14 The variation of interface trap density of halo BF_2 device in positive and negative stress modes under different stress time.

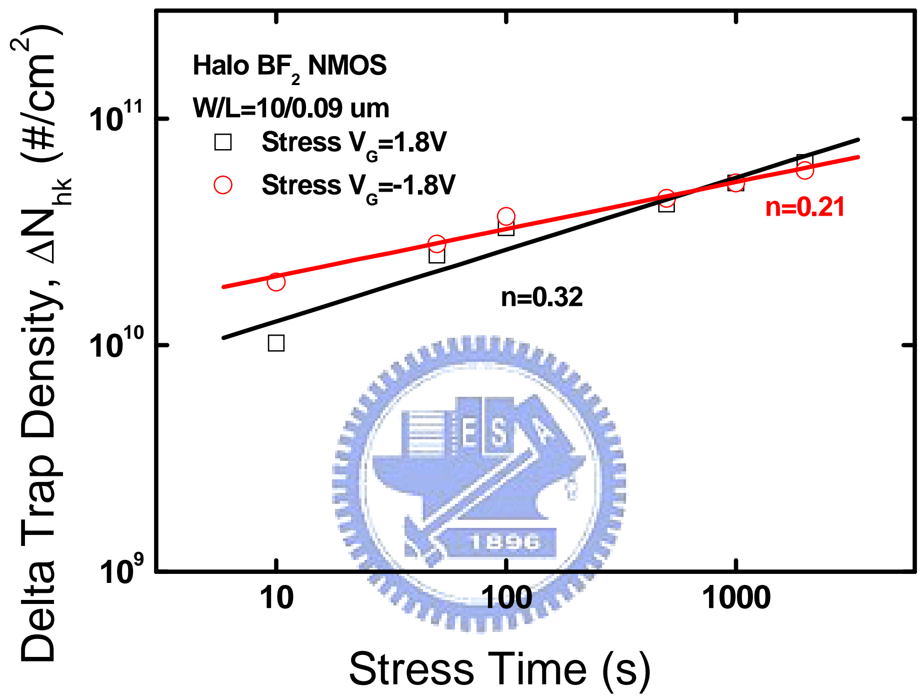


Fig.4.15 The change of high-k gate dielectric trap density of halo BF_2 device in both stress modes under different stress time.

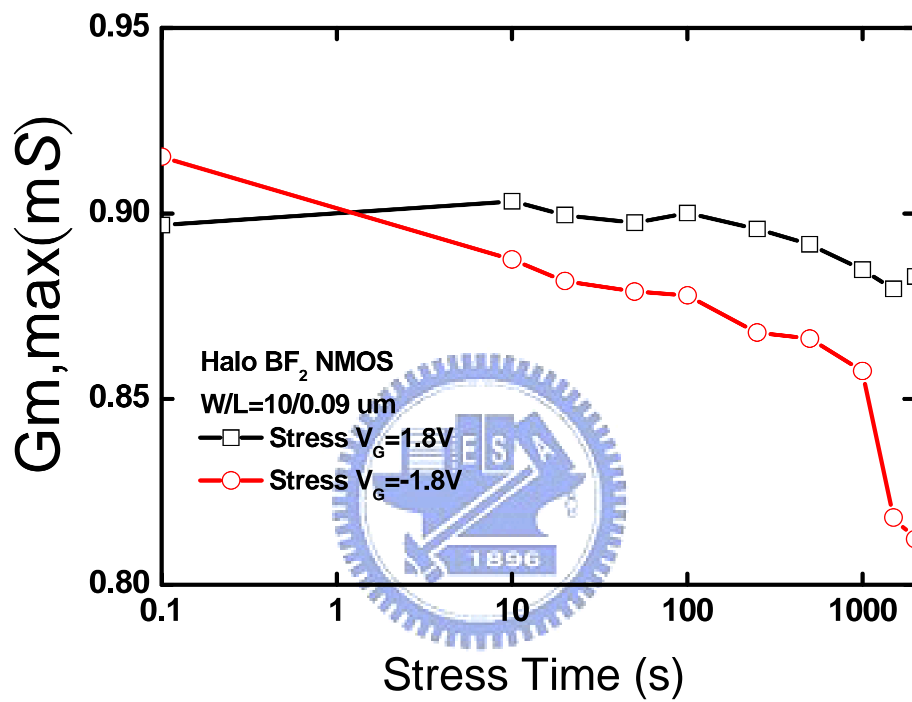


Fig.4.16 The change of $G_{m,max}$ of halo BF_2 device in positive and negative stress under different stress time.

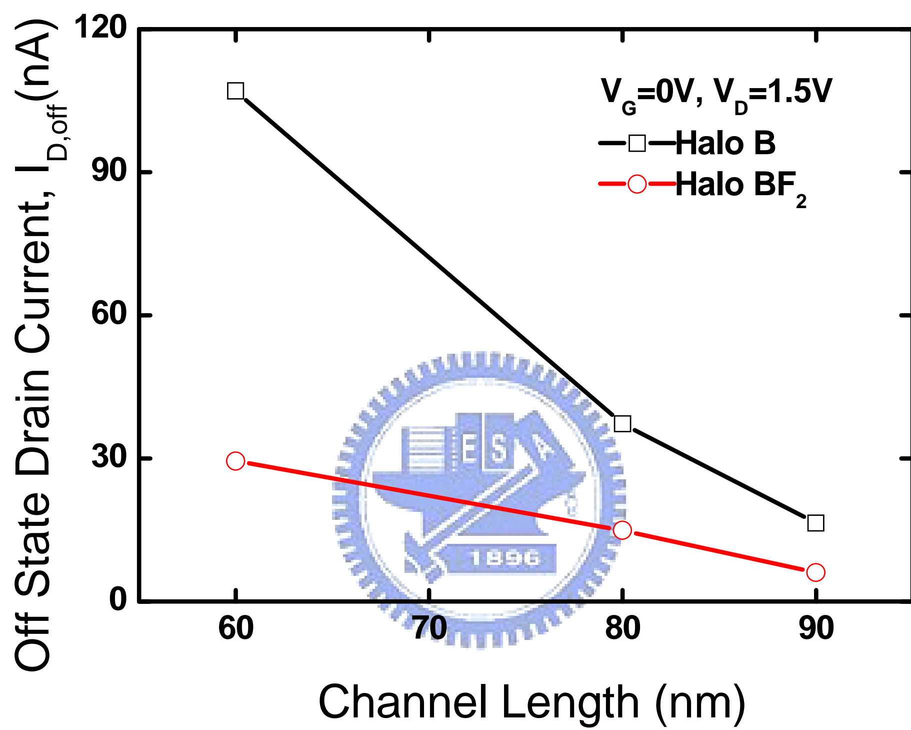


Fig.4.17 The off-state drain current of two different halo devices in different channel lengths under V_G=0V, V_D=1.5V.

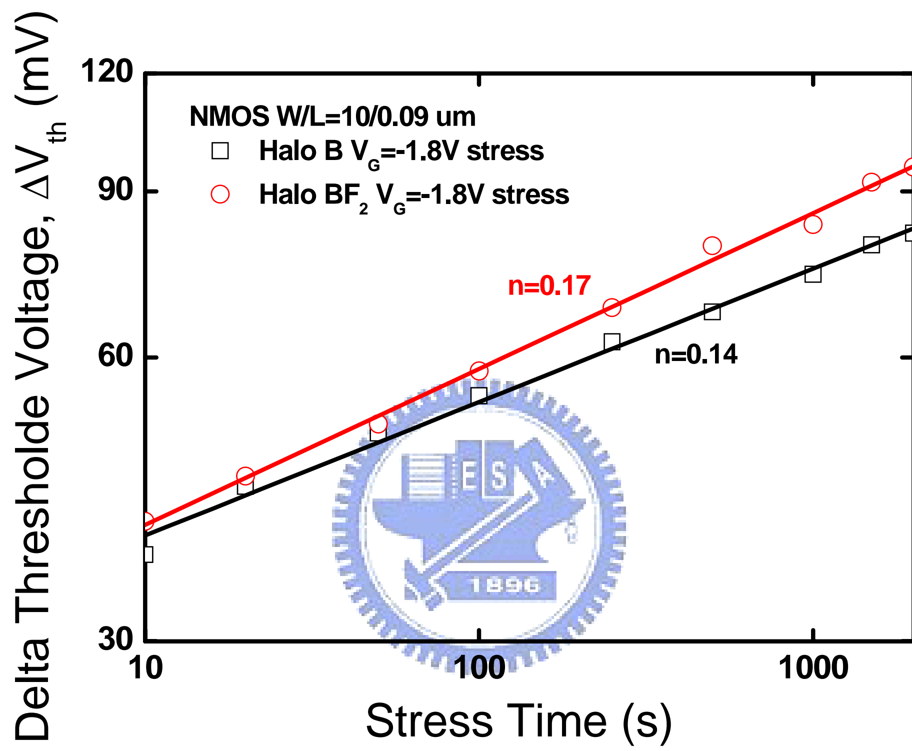


Fig.4.18 Negative stressing induce delta V_t shift of the different halo implant.

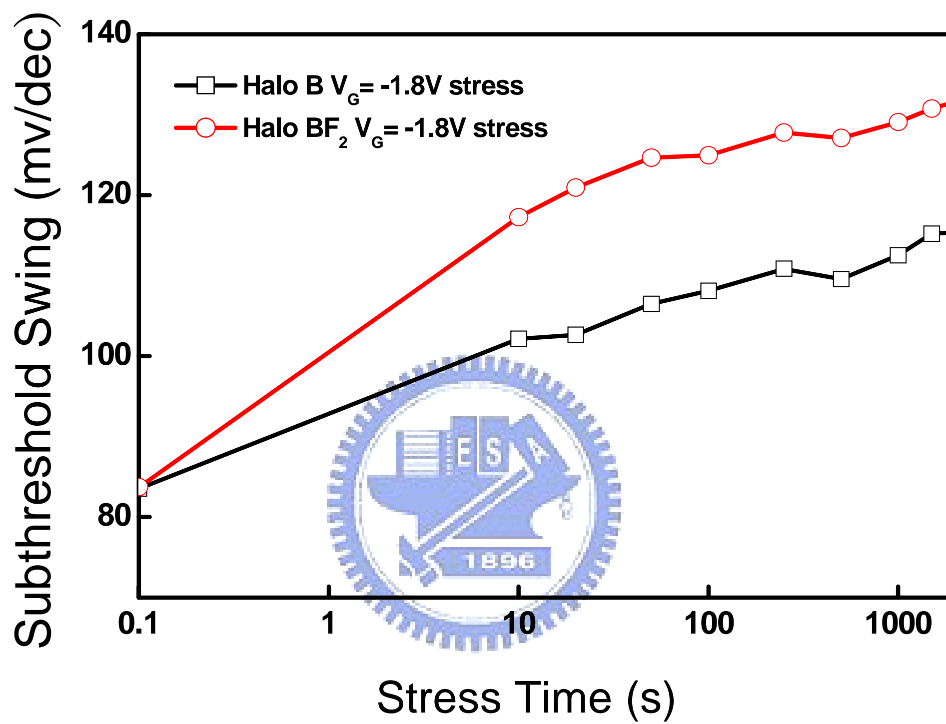


Fig.4.19 The subthreshold swing of different halo implant by negative stress under different stress time.

Fig.4.18 shows delta V_t shift of the different halo implant by negative stress. The V_t degradation of halo BF_2 device is severer than halo B after constant voltage stress. The subthreshold swing of different halo implant by negative stress under different stress time is shown in Fig.4.19. With the stressing time, the subthreshold swing would get larger and make the device turn on more slowly. Besides, the variation of halo BF_2 is more obvious than halo B. From Fig.4.18 and Fig.4.19, the concept of more damage from halo BF_2 is known. The reason might be that more defects are generated at the dielectric and interface of Si/IL during implantation of larger molecules.

4.4 Summary

In this chapter, the nMOS of an inverter under positive and negative stress is simulated, and the comparison of both stress modes to the device is done. The difference of positive and negative stress is discovered. Both stress modes would cause V_t shift, but the degradation of subthreshold swing could only be detected under negative stress. Different frequencies are utilized to compare the variation of traps at different location. We find that the traps are mostly generated at high-k gate dielectric during positive stress and at the Si/IL interface by negative stress. Fig.4.20 shows the band diagram during positive stress. With V_G=1.8V, the device is in inversion state, and therefore the electrons in the channel would be captured by the traps in HfSiON, which may cause more trap generation in this region. Thus the degradation in high-k dielectric is severer than Si/IL interface. The band diagram under negative stress is shown in Fig.4.21. The device is in its accumulation state under V_G=-1.8V, and the holes would be captured by the traps at the Si/IL interface. Consequently, more damage is generated at the Si/IL interface than the high-k dielectric. On the other hand, due to the negative stress on the poly-Si gate, a large number of electrons would be captured by the traps in high-k dielectric, and thus numerous defects would be induced in the device.

A same result is obtained by CP measurement with different frequencies. According to Fig.4.2,

Fig.4.3, Fig.4.10, and Fig.4.11, the traps created by positive stress are mainly located inside of HfSiON and could capture the electrons to make V_t varied. From Fig.4.4, Fig.4.5, Fig.4.12, and Fig.4.13, it is known that under the negative stress mode, the traps originated are generally at the Si/IL interface, and the threshold voltage and subthreshold swing would change due to the capture of the holes. Comparing the positive and negative stress, it could be known that the traps produced closer to the channel (Si/IL interface) would impose a larger effect on the electrical properties, and this could be shown by Fig.4.8 and Fig.4.16 (mobility of negative stress goes down more rapidly than positive stress).

On the other hand, though a bigger molecular halo (BF_2) device could suppress I_{off} more effectively, it would do more damage to the device itself. This is what should be considered when choosing the materials in the area of integration.

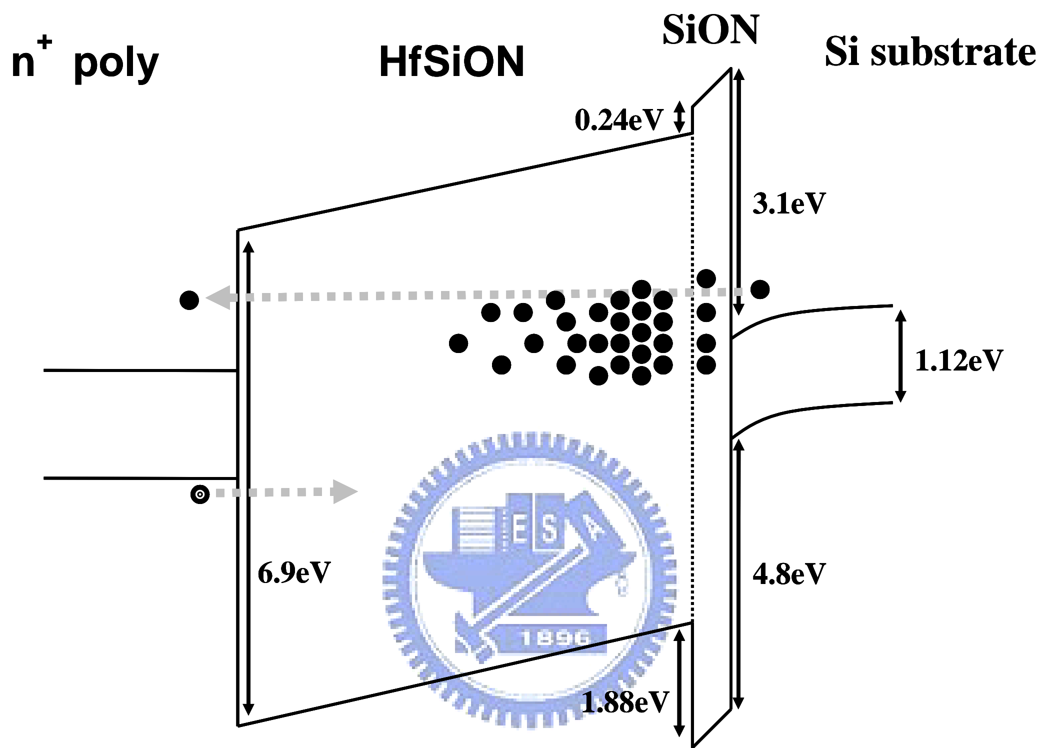


Fig.4.20 The band diagram during positive stress.

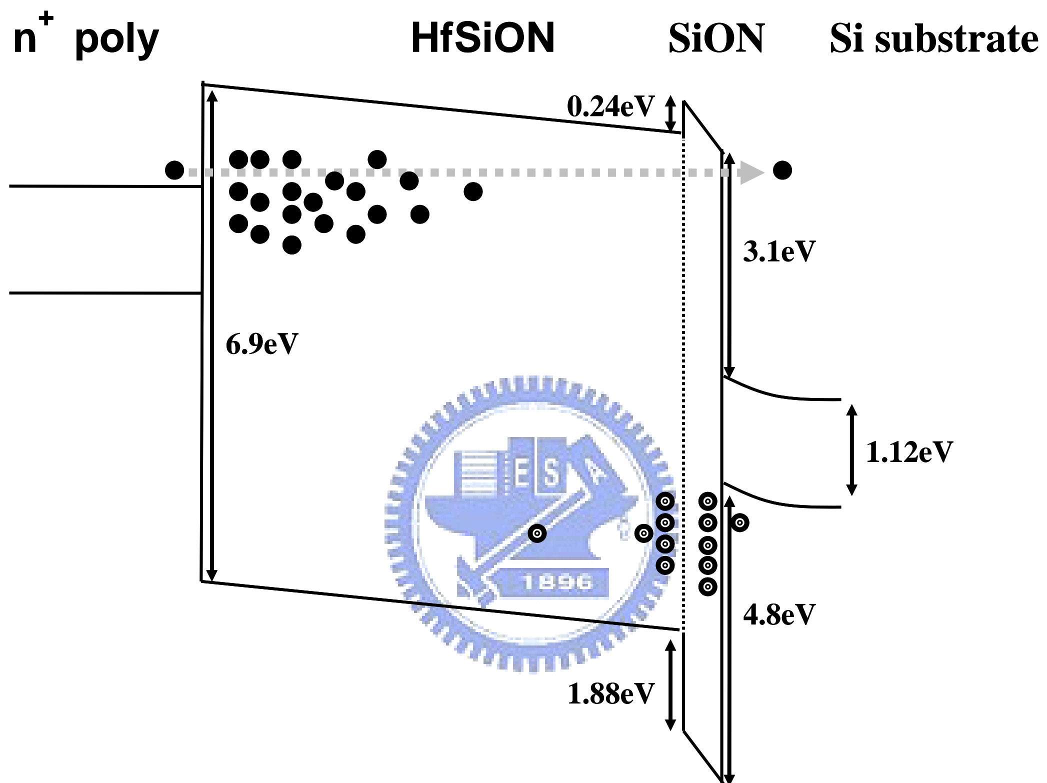


Fig.4.21 The band diagram during negative stress.

Chapter 5

Conclusion

Alternative gate oxide material is a trend for the scaling of oxide thickness in CMOS device technology. Hafnium based dielectrics are among the most promise candidates as a replacement for SiO_2 in conventional CMOS process. Interfacial layer and halo implant are mandatory for high-k and sub-65nm CMOS devices.

.In this dissertation, the basic principle of the CP measurement has been introduced briefly, and the trap density at different depths could be measured by different frequencies. Subsequently, the variation of the traps is investigated using this method after the device is stressed by positive and negative voltage. It has been shown that the traps created by the positive stress are mainly generated by the capture of electrons into the traps in the high-k dielectric and thus produces the defects. Nevertheless, the mechanism of trap generation under the negative stress is more complicated. The device is in its accumulation state under a negative voltage, and the holes in the channel would be captured by the defects located at the Si/IL interface, which may damage the device. The gate poly-Si, which is n-type, would cause the electrons to be trapped into the dielectric due to the negative bias at the gate side, and more traps are created inside the device. For the electrons are captured in the dielectric under the positive stress, the electrical properties changed is essentially about the variation of the threshold voltage. However, in the situation of the negative stress, the electrons would be trapped in the dielectric, and besides the holes would be captured at the Si/IL interface. Because where the holes are trapped is closer to the channel, the variation of electrical properties would be much more obvious, and this could be seen by the degradation of the subthreshold swing under negative stress and the change of $G_{m,max}$ during positive and negative stress. The result is not found in related researches so far,

and it is the primary contribution of this thesis.

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