國 立 交 通 大 學

電子工程學系　電子研究所

碩 士 論 文

高功函數矽化銥金屬閘極之高溫穩定氮氧化鉿鑭P型金氧半場效電晶體研究

The Research of High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir_3Si Gate

研究生: 周坤億

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中華民國九十七年六月

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電子工程學系　電子研究所碩士班

碩士論文

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摘要

本論文研究高溫穩定矽化鉿金屬閘極之氮氧化鉿鑭 P 型金氧半場效電晶體元件，此等效氧化層厚度為 1.6 奈米的元件在平帶電壓上一伏時有著 $1.8\times10^{-5}A/cm^2$ 的低漏電流，並且擁有高達 5.08 電子伏特的高功函數和 $84cm^2\cdot S$ 的高移動率。此閘極優先的 P 型金氧半場效電晶體製程是利用自我對準的離子布植技術和 1000℃快速高溫退火的方式來製作，而這些方法都相容於現在大尺寸製程整合的生產線。

The Research of High-Temperature Stable HfLaON p-MOSFETs With High-Work-Function Ir_3Si Gate

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Abstract

We research a novel 1000℃ stable HfLaON p-MOSFET with Ir_3Si gate. Low leakage current of 1.8×10^{-5} A/cm^2 at 1 V above flat-band voltage, good effective work function of 5.08 eV, and high mobility of 84 cm^2/V · s are simultaneously obtained at 1.6 nm equivalent oxide thickness. This gate-first p-MOSFET process with self-aligned ion implant and 1000 ℃ rapid thermal annealing is fully compatible to current very large scale integration fabrication lines.

誌　謝

本論文得以完成,首先要感謝我的指導老師 荊鳳德 教授，在兩年的碩士研究生涯裡，給予我豐富的指導與照顧，不論是研究上與生活裡都讓我在這兩年裡獲得許多的收穫。

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Contents

Figure Captions

Chapter 1 Introduction

Chapter 2 Experimental Steps and Measurement

Chapter 3 Result and Discussion

Chapter 1

Introduction

1.1 Motivation to study high-k dielectrics

With the improvement of the semiconductor processing technology, the scaling trend of MOSFETs devices will produce the large gate leakage current due to thinner gate oxide [1]-[2]. The MOSFETs exhibit significant leakage current more than 1 A/cm^2 when the thickness of ultra-thin silicon gate oxide (SiO_2) is less than 2 nm. The gate leakage current through the gate oxide increases significantly because the direct tunneling is the primary conduction mechanism in down-scaling CMOS technologies. To reduce the leakage current related higher power consumption in highly integrated circuit and overcome the physical thickness limitation of silicon dioxide, the conventional SiO_2 will be replaced with high dielectric constant (high-κ) materials as the gate dielectrics beyond the 0.1 μm technology node [3]-[8]. Therefore, the engineering of high-κ gate dielectrics have attracted great attention and played an important role for VLSI. Although high-κ materials often exhibit smaller bandgap and higher defect density than conventional silicon dioxide, using the high-κ gate dielectric can efficiently increase the physical thickness in the same effective oxide thickness (EOT) that shows lower leakage characteristics than silicon dioxide by several orders without the reduction of capacitance density [4]-[7]. Recently, some

high-κ materials have been widely studied and successfully intergraded in advanced MOSFETs or semiconductor devices, such as DRAMs or Flash memory and RF metal-insulator-metal (MIM) capacitors [9]-[10].

According to the ITRS (International Technology Roadmap for Semiconductor) [11] ,the suitable gate dielectrics must have value more than 8 for 50-70 nm technology nodes and that must be more than 15 when the technology dimension less than 50 nm. Figure 1-1 shows the evolution of CMOS technology requirements.

Oxy-nitrides (SiO_xN_y) have been introduced to extend the use of SiO_2 in production but eventually it has to be replaced by a high-κ material, such as Ta_2O_5, TiO_2, HfO_2, ZrO_2, Al_2O_3, La_2O_3 or mixtures of them or metal-oxide-silicates of the mentioned compounds. However, most metal oxides will have the characteristics of crystallization at elevated temperature which cause devices generate non-uniform leakage distribution and give large statistical variation for nanometer devices across the chip. Therefore, replacement gate strategies have been proposed to prevent crystallization and deleterious effects of mass along grain boundaries. Figure 1-2 shows the summaries of the κ value and band offset for popular high-K dielectric candidates. To predict the M-N thermal stability, in Figure 1-3 we show the bond enthalpy for various metal/dielectric combinations. In general the bond strength is that M-O> M-N> M-C.

1.2 Motivation to study metal gate

As traditional poly-silicon (poly-Si) gated metal-oxide semiconductor field effect transistors (MOSFETs) scale down, the additional series capacitance due to poly-Si depletion becomes an increasingly large fraction of the total gate capacitance. Besides, diffusion of boron penetrates from the poly-Si gate will also degrade the performance of the transistors. To overcome these problems, using metal gate electrodes will be a practical way to eliminate poly gate depletion and boron penetration. In addition, metal gates also show the potential of reduced sheet resistance. Metal electrodes with suitable work functions and sufficient physical and electrical stability are being investigated to address these problems. In addition, thermal stability of the effective metal electrode and metal diffusion are also important considerations. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced CMOSFET's, such as TiN, TaN, Pt, Mo and Ir. Tantalum (Ta) has a work-function close to *n*+ poly-Si. Tantalum nitride (TaN) is quite stable (to maintain thermal stability up to a 1000℃ RTA) because the activation energy of metal and nitrogen is relatively low. Tantalum is bonded tightly within nitride and no obvious diffuse was observed in fabricated devices. However, TaN gate on high-κ HfO_2 shows a significant shift of flat band voltage (V_{FB}) toward the mid-gap of Si due to the interface reaction between the TaN and HfO_2 at the high temperature. This is

called the “Fermi-level pinning effect.” Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced MOSFETs.

Therefore, metal-gate/high-κ CMOSFETs show undesired high threshold voltages (V_t), which is opposite to the VLSI scaling trend. The increasing $|V_t|$ in both metal-gate/high-k n- and p-MOS may be due to the interface dipole and charged defects formed by MN-MO reaction or [poly-Si]-MO reaction at high temperature, which altered the band diagram in Figure 1-4. Fermi level pinning of poly-Si and metal electrodes on HfO_2 has been investigated. From Figure 1-5 the schematic HfO_2 bond diagram, the metal accumulation at HfO_2 surface may screen the surface dipole and un-bonded defect states, to reduce Fermi-level pinning. Furthermore, it has been shown that dosing surfaces with intra-layers can modify the interface dipole and band alignment, a phenomenon exploited in the fabrication of MOS gas sensors.

The work functions (Φ_m) of metal shown in Figure 1-6 play an important role for metal-gate/high-κ CMOSFETs. The preferred work function of the metals are ~5.2 eV for p-MOSFETs and ~4.1 eV for n-MOSFETs. Recently, lots of metal or metal-nitride materials have been widely researched and successfully intergraded in advanced CMOSFETs, such as TiN, TaN, Pt, Mo and Ir. However, it has been found that thermal annealing of the metal gates at temperatures above 900℃ results in

mid-gap values for almost all metal gate candidates. Therefore, the Fermi-level pinning effect needs to be avoided by selecting suitable metal gate and high-κ materials for advanced CMOS technologies.

1.3 Introduce of this work

According to the International Technology Roadmap for Semiconductors, the metal-gate/high-κ is the required technology for the future generation complementary MOSFETs to reduce the undesired large gate leakage current and continue the gate oxide scaling [12-22]. Currently, the HfSiON is a promising candidate beyond SiON with merits of high-κ value, low gate leakage current, and similar amorphous structure after 1000℃ rapid thermal annealing (RTA) for self-aligned process. However, the lack of a high-work-function gate for HfSiON p-MOSFETs is the challenge since only Ir (5.27 eV) and Pt (5.65 eV) in the periodic table [19] have the needed work function larger than the target 5.2 eV. The other problem of HfSiON is the relative lower κ of 10–14 that causes limited scaling capability. In this letter, we developed the high temperature stable Ir3Si/HfLaON p-MOSFET to address the aforementioned issues. The novel HfLaON dielectric can preserve the amorphous structure after 1000 ◦C RTA and is similar to HfSiON but with significantly higher κ value. Using high work- function Ir3Si gate electrode [19], [20], the p-MOSFETs show good device integrity of low leakage current of 1.8×10^{-5} A/cm^2 at 1 V above flat-band voltage

V_{fb}, high effective work function $\varphi_{m\text{-}eff}$ of 5.08 eV, high hole mobility of 84 $cm^2/V \cdot s$, and good 1000℃ RTA thermal stability at equivalent oxide thickness (EOT) of 1.6 nm. These results are compatible with or better than the best reported metal gate/high-κ p-MOSFETs [12-18].

		2003	2005	2007	2009	2012	2015	2018
Gate Length (nm)		107	80	65	50	30	25	18
EOT (nm)	High Speed	1.3	1.2	0.9	0.8	0.7	0.6	0.5
	Low Power	1.6	1.4	1.2	1.0	0.9	0.8	0.7
S/D Junction Depth (X_j, nm)*		49.5	35.2	27.5	NA	NA	NA	NA
Interconnect Levels		9	11	11	12	12	13	14
Logic V_{DD} (V)	High Speed	1.2	1.1	1.1	1.0	0.9	0.8	0.7
	Low Power	1.0	0.9	0.8	0.8	0.7	0.6	0.5

Source: International Technology Roadmap for Semiconductor (ITRS 2003)

Fig. 1-1 The evolution of MOS technology requirement.

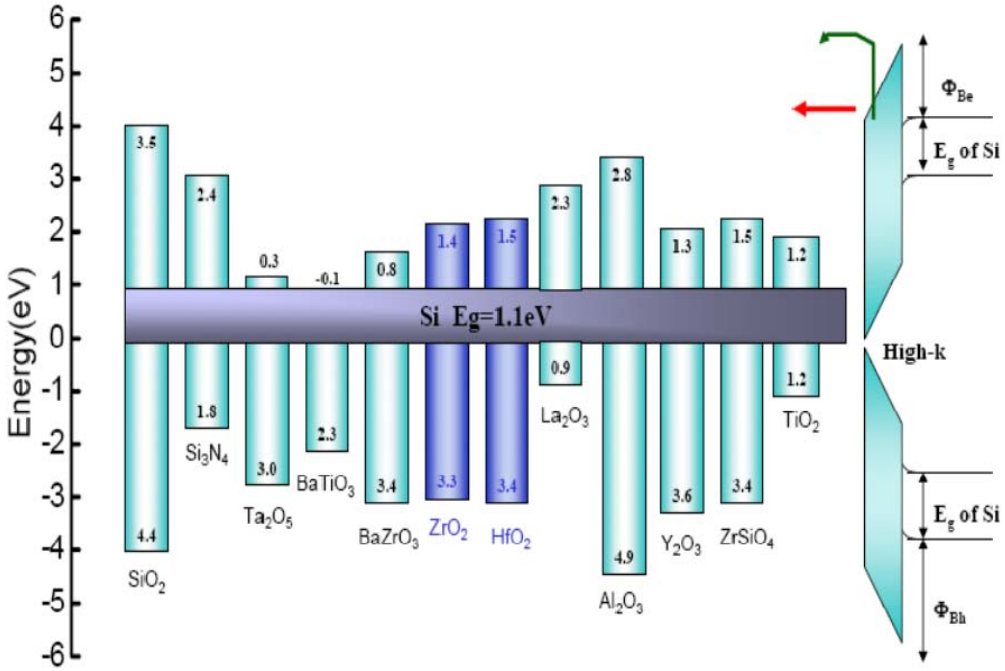

Fig. 1-2 The band offset of popular high-materials.

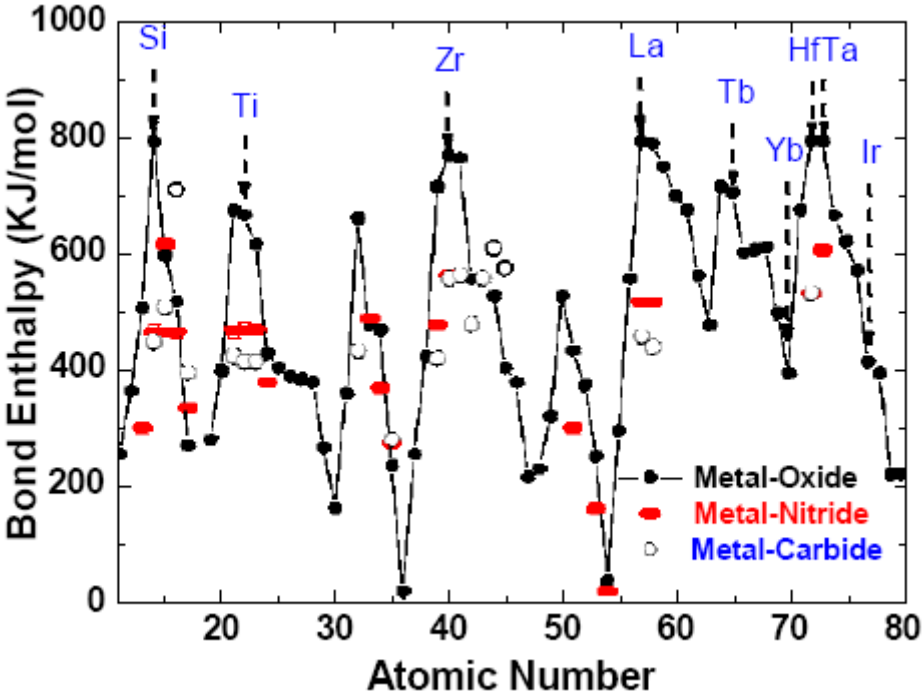

Fig. 1-3 Bond enthalpy for M-O, M-N and M-C in the Periodic Table for thermal stability prediction, with M-O>M-N>M-C in general . The bond enthalpy peaked at La, Hf and Ta.

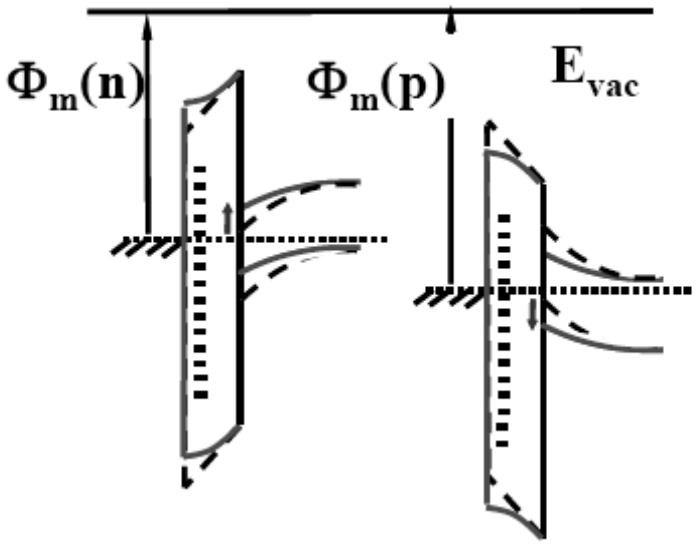

Fig. 1-4 Energy band diagram to show the increasing $|V_t|$ in both n- and p-MOS.

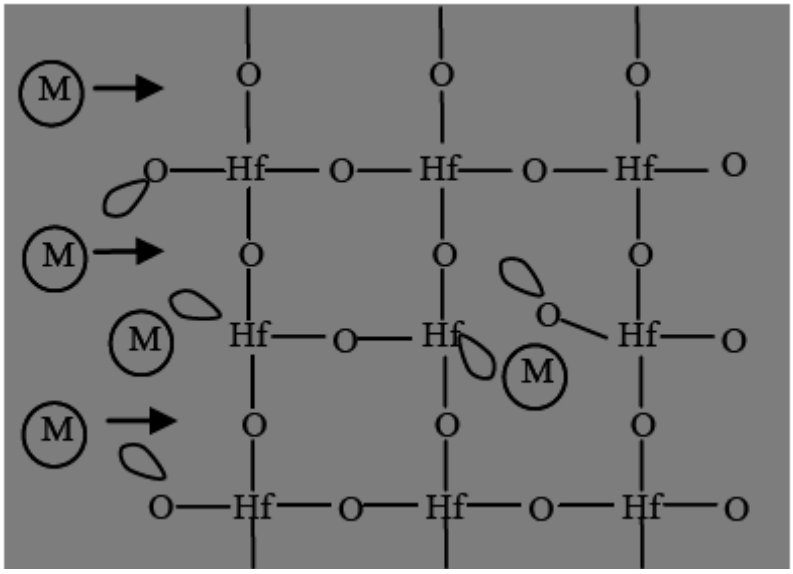

Fig. 1-5 The schematic HfO_2 bond diagram.

Chapter 2

Experimental Steps and Measurement

2.1 Fabrication of MOSFET

Standard N-type Si wafers with resistivity 1~10 Ω-cm (10^{15}-10^{16} cm^{-3} doping level) were used in this study, and following RCA clean processes. The detail steps of RCA clean is shows in Fig. 2-1. After standard RCA clean, the HfLaO was deposited on N-type Si wafers by PVD and post deposition anneal (PDA). The HfLaON was formed by applying NH_3 plasma surface nitridation on HfLaO. Then 5 nm amorphous Si and 20 nm Ir was subsequently deposited on HfLaON and RTA annealed at 400~1000℃ for 30~5 sec to form the MOS capacitors. For comparison, Ir/HfSiON devices were also fabricated, where the HfSiON was formed by atomic layer deposition (ALD) of HfSiO and followed by surface plasma nitridation. The low temperature deposited Al gate on 1000℃ RTA-annealed HfLaON capacitors were also formed for $\varphi_{m\text{-}eff}$ reference. For p-MOSFETs, additional thick TaN capping layer is added on Ir/Si/HfLaON to prevent subsequent ion implantation penetration, where the Ir_xSi gate was formed during RTA. After patterning, self-aligned B^+ implantation was applied at 25 KeV and source-drain doping was activated at 1000℃ RTA for 5 sec.

The fabricated p-MOSFETs were characterized by C-V and *I-V* measurements, and the processes of MOSFET is shown in Fig. 2-1 ~ Fig. 2-13.

2.2 The measurement of MOS capacitors

To investigate the electrical characteristics of devices, we measured the I_g-V_g curves for gate leakage current by using HP 4156C semiconductor parameter analyzer. Besides, HP4284A precision LCR meter was used to evaluate the gate capacitance and the conductance ranging from 100 kHz to 1 MHz.

A. DI water rinse, 5 min.
B. H_2SO_4 : H_2O_2 = 3:1, (10 min, 75~85℃)
C. DI water rinse, 5 min.
D. HF : H_2O = 1:100
E. DI water rinse, 5 min.
F. NH_4OH : H_2O_2 : H_2O = 1:4:20 (SC1), (10 min,75~85℃)
G. DI water rinse, 5 min.
H. HCl : H_2O_2: H_2O = 1:1:6 (SC2), (10min, 75~85℃)
I. DI water rinse, 5 min.
J. HF : H_2O = 1:100
K. DI water rinse.
L. Spinner

Fig.2-1 The RCA clean steps.

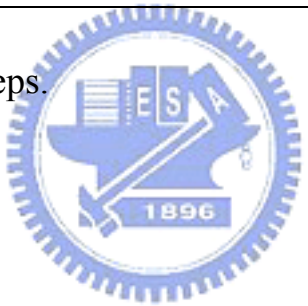

Fig. 2-2 Silicon substrate.

RCA Clean

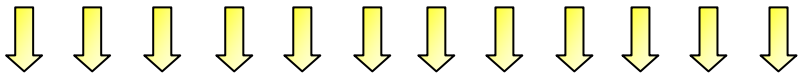

Fig.2-3 RCA Clean.

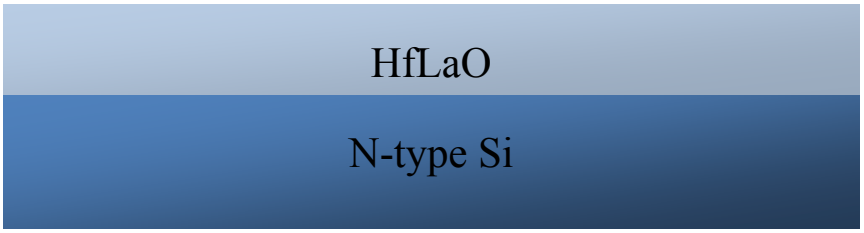

Fig.2-4 Deposited HfLaO dielectric.

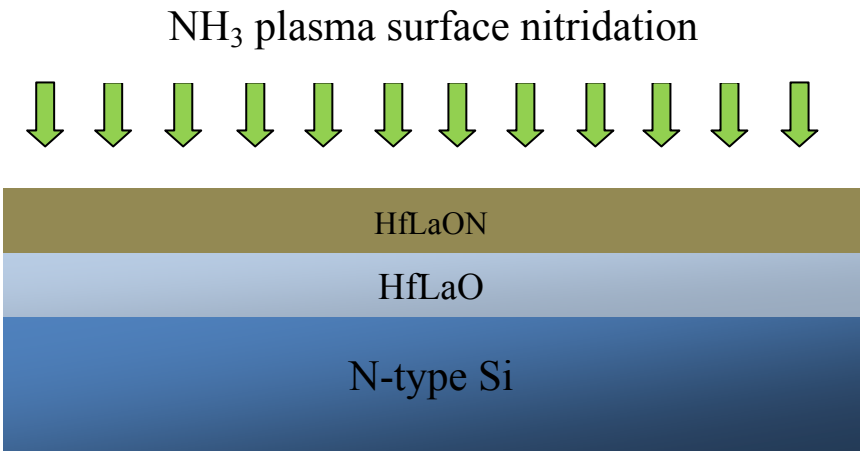

Fig.2-5 NH_3 plasma surface nitridation on HfLaO.

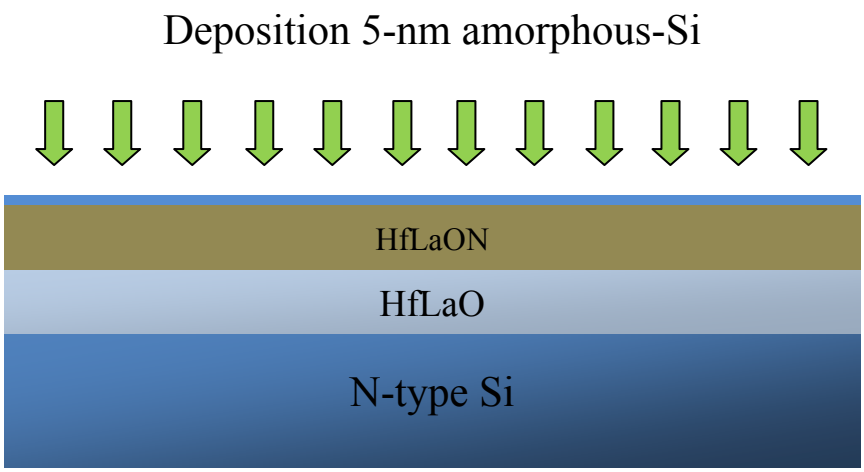

Fig.2-6 Deposition 5-nm amorphous-Si.

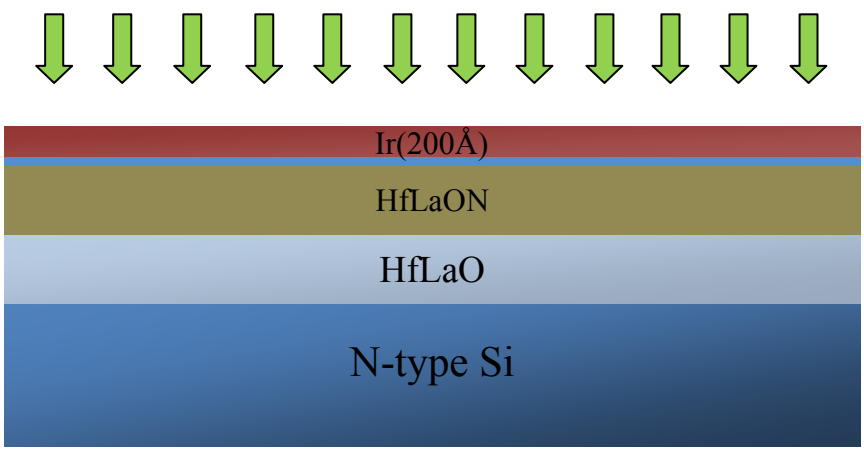

Fig.2-7 Deposition 20-nm Ir.

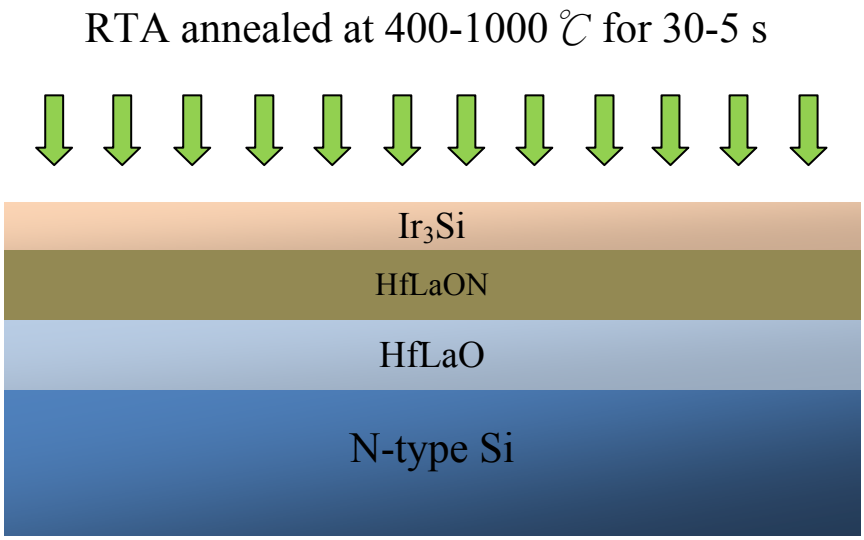

Fig.2-8 Formation of Ir_3Si.

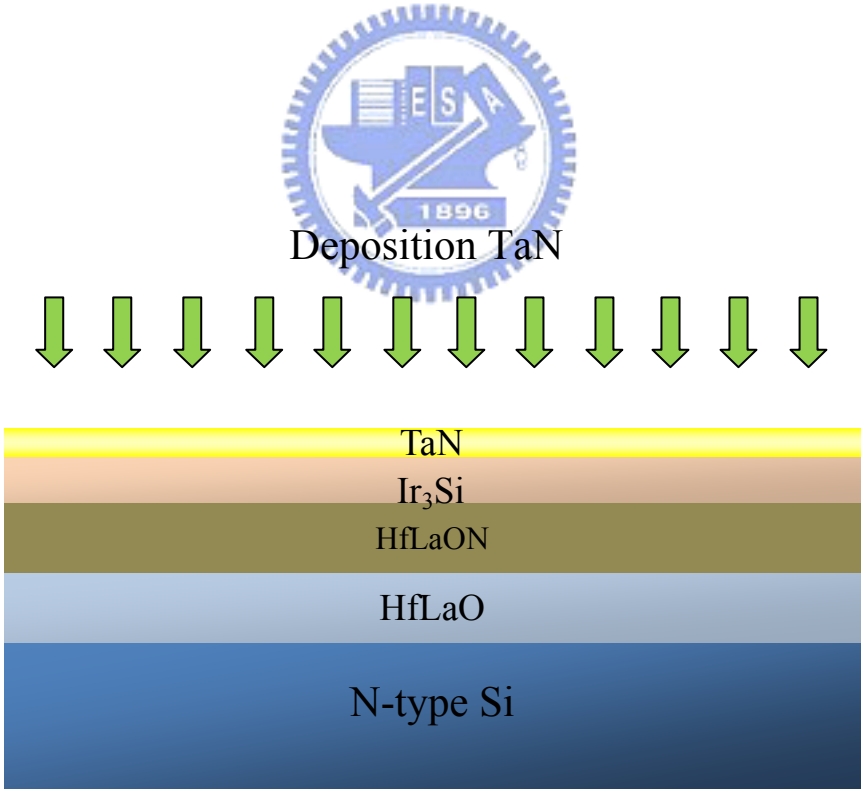

Fig.2-9 Deposition TaN capping layer to prevent ion implantation penetration.

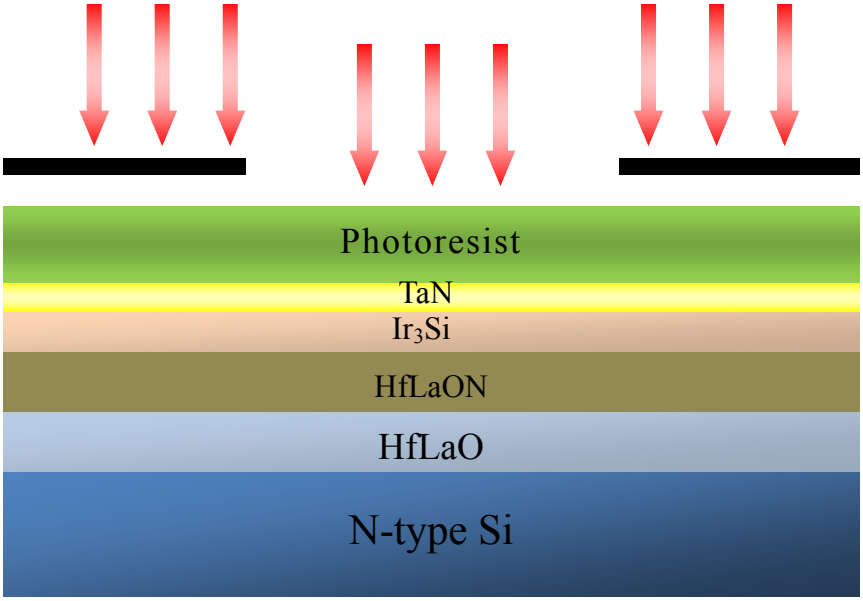

Fig.2-10　Photoresist and Lithography.

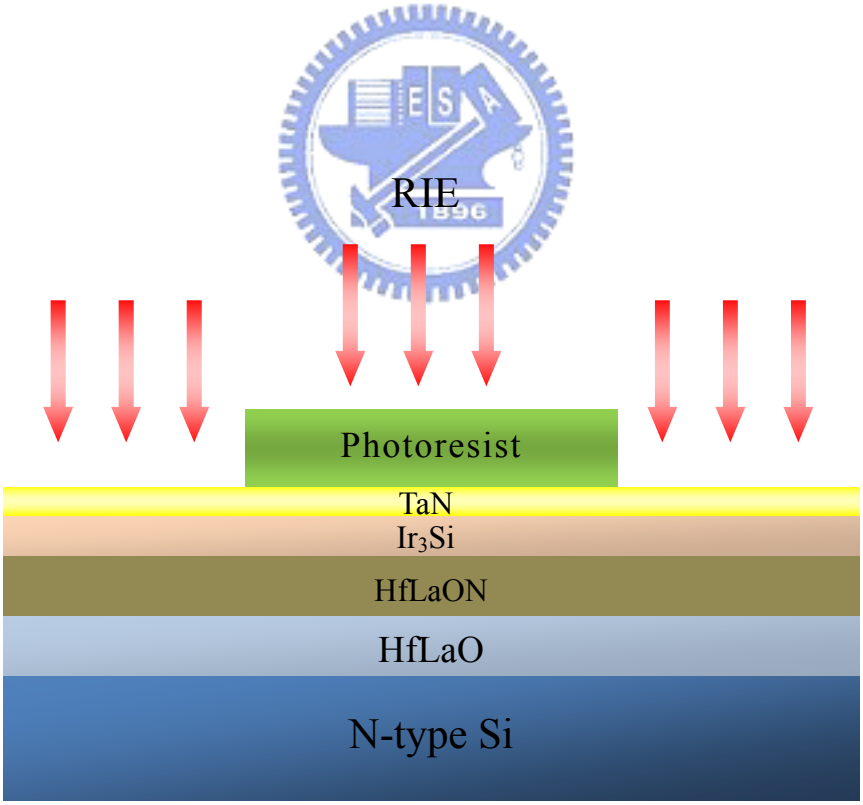

Fig.2-11　RIE etching.

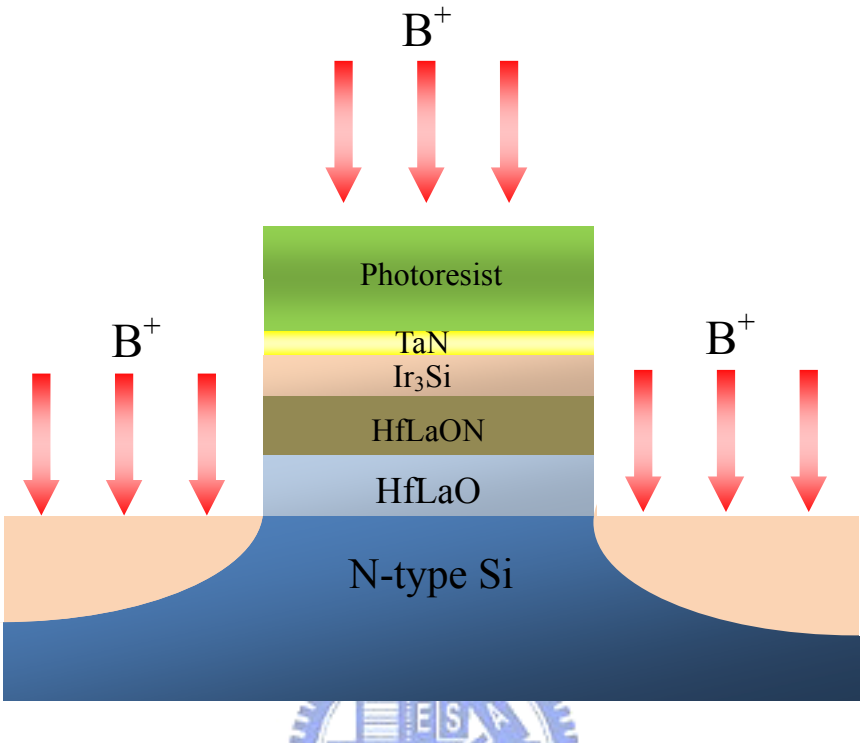

Fig. 2-12 Self-aligned B^+ implantation.

RTA

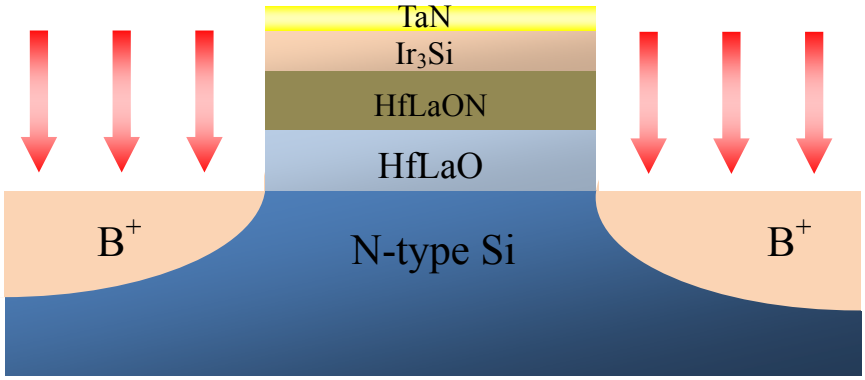

Fig. 2-13 source-drain doping activation at 1000℃ RTA for 5s

Chapter 3

Result and Discussion

Figures 3-1 and 3-2 show the XRD comparison of HfLaO and HfLaON with different RTA temperature. After 1000℃ RTA, strong undesired crystallization in HfLaO is clear measured, but in sharp contrast, the HfLaON still preserves the amorphous state. The existence of Hf, La, O and N in HfLaON is confirmed by XPS in Figure 3-3. The metal-gate Ir3Si on HfLaON are further analyzed by AES. As shown in Figure 3-4, such good device characteristic is due to the nitridation on thick high-κ that prevents Ir3Si metal diffusion through HfLaON. The high φm-eff is due to the Ir3Si accumulated toward HfLaON interface to un-pin the Fermi-level. Figure 3-5 shows the J-EOT plot, where much improved leakage current than SiO2 is obtained at 1.7 nm EOT. In addition, high κ of 20 is still preserved even after 1000oC RTA and much better than HfO2. Figures 3-6 and 3-7 show the C-V and J-V characteristics respectively, for different RTA temperature annealed IrxSi/HfLaON capacitors. The Ir/HfSiON and Al/1000oC-annealed-HfLaON devices are also shown for comparison. An increasing *Vfb* trend with increasing RTA annealing temperature is measured, which is attributed to IrxSi reaction toward high-κ interface [19]-[20]. The Ir on HfSiON shows the highest Vfb, but the capacitor failed after 1000℃ RTA.

In contrast, the Ir_xSi/HfLaON have good 1000℃ thermal stability by converting

the Ir to Ir_xSi by inserting ~5 nm amorphous Si; however, the better thermal stability is traded off the slightly lower V_{fb}. From the C-V shift to control Al gate on 1000℃ RTA annealed HfLaON, the extracted φm-eff of Ir3Si/HfLaON is 5.08 eV. Here the Al gated capacitor was chosen as a reference because low temperature deposited pure metal has little Fermi-level pinning on high-κ dielectric [15]-[16], [19]-[20] and the same 1000℃ RTA ensures the similar oxide charge in HfLaON to Ir_3Si-gated devices. The using Al control gate is to avoid oxide charge difference on thickness introduced by nitrogen-plasma treatment and process variation. Anyway, the fixed charge density should be small from the good mobility shown following. The merit of using HfLaON rather than HfSiON is clearly seen by the orders of magnitude leakage current improvement. Very low leakage current of 1.8×10^{-5} A/cm^2 at 1V above V_{fb} are measured in Ir_xSi/HfLaON at 1.6 nm EOT. Such low leakage current is attributed the high κ value of 20 and amorphous structure after 1000℃ RTA from cross-sectional TEM measurement in Figure 3-8. The decreasing stretch of C-V curves with increasing RTA temperature suggests the improving oxide quality annealing out the defects at high temperatures. Therefore, high $\varphi_{m\text{-}eff}$ of 5.08 eV, low gate leakage current of 1.8×10^{-5} A/cm^2 (Vfb+1V) and good thermal stability of 1000℃ RTA can be achieved at the same time in Ir_xSi/HfLaON MOS capacitors at 1.6 nm EOT. The decreasing capacitance density with increasing RTA temperature is related to slight

decreasing κ value reduction shown in Figure 3-9, but the amount of reduction is significantly less than HfO_2.

We have further used the X-Ray Diffraction (XRD) measurements to characterize the Ir_xSi. As shown in Figure 3-10, the Ir-rich Ir_xSi with x=3 was formed with distinct 2θ angle to residual Ir peak. The x=3 in Ir_xSi was determined by comparing the measured peak XRD pattern with published data . The amorphous structure of HfLaON was also confirmed by glazing angle XRD measurements even after 1000℃ RTA .Figure 3-11 shows the transistor Id-Vd characteristics as a function of Vg-Vt for 1000℃ RTA annealed Ir_3Si/HfLaON p-MOSFETs and good transistor characteristics are obtained. Here the Vt is -0.1 V as obtained from the linear Id-Vg plot and consistent with the large $\varphi_{m\text{-}eff}$ of 5.08 eV from C-V curves.

Figure 3-12 shows the hole mobility plot as a function of gate electric field of Ir_3Si/HfLaON p-MOSFETs. High hole mobility of 84 and 63 cm^2/V-s are obtained at peak value and 1 MV/cm effective field for Ir_3Si/HfLaON p-MOSFETs, respectively. This result is comparable with the reported HfSiON p-MOSFET in the literature [12]-[18] with advantages of process compatible to current VLSI line.

In Figures 3-13 and 3-14, a large 2.6 V operation voltage for 10-years is obtained from the t_{BD} plot. Further reliability study is from the BTI shown in Figure 3-15, where <20 mV shift are measured for CMOS at 10 MV/cm stress and 85℃ for 1 hr.

Table 3-1 summarizes the comparison among various metal-gate/ high-κ CMOS.

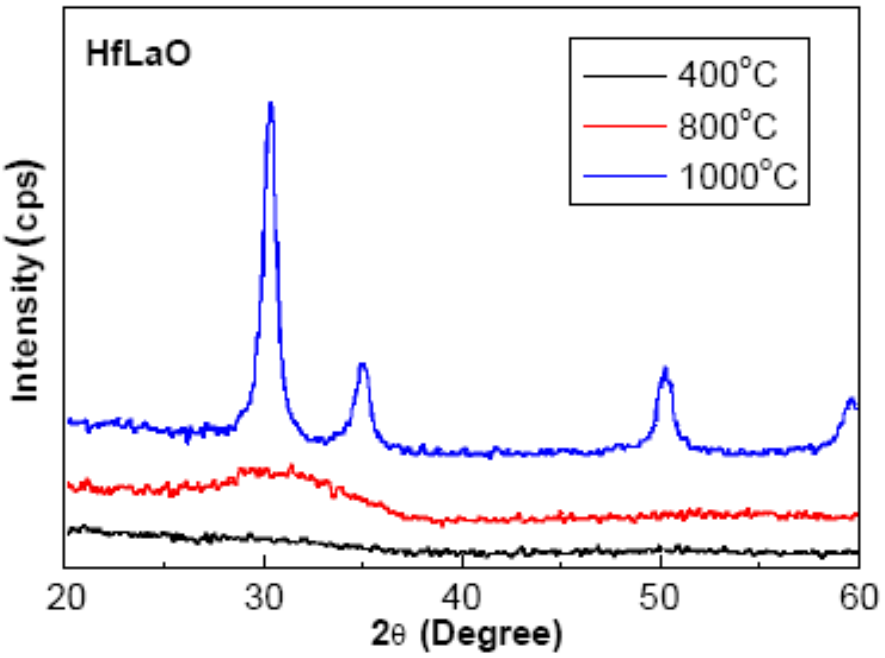

Fig. 3-1 Grazing incident XRD spectra of HfLaO after different RTA annealing.

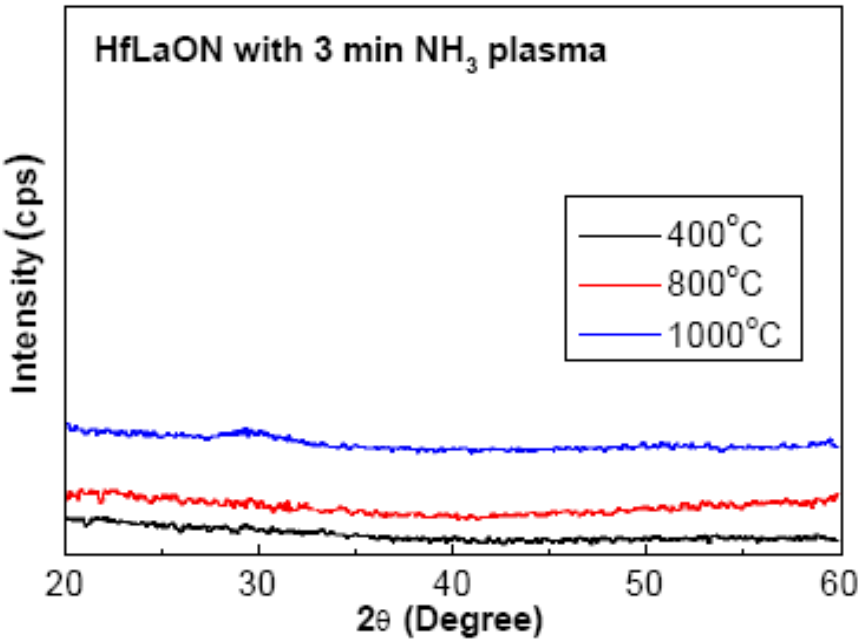

Fig. 3-2 Grazing incident XRD spectra of HfLaON with NH3 plasma after different RTA annealing. In contrast to the HfLaO case, the HfLaON stays amorphous state after 1000oC RTA

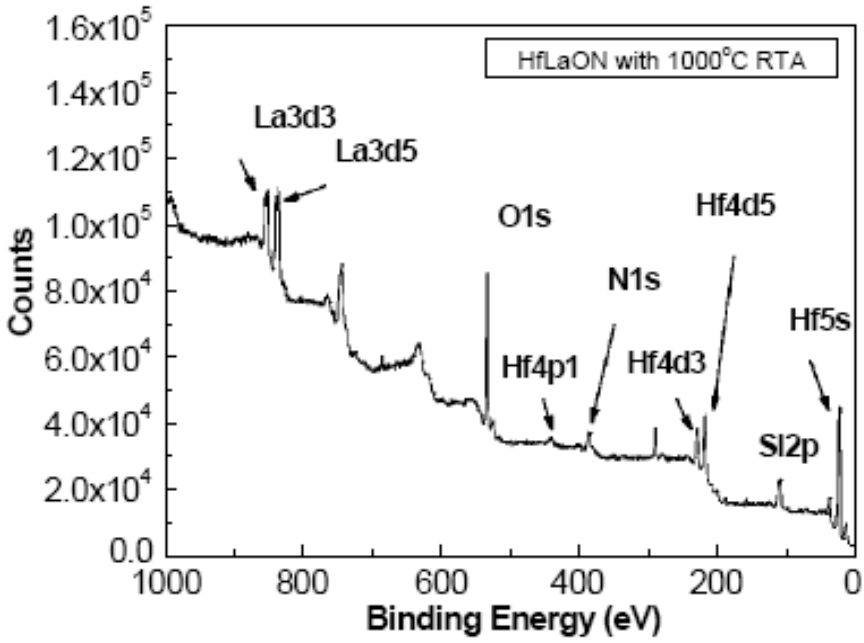

Fig. 3-3 XPS spectra of HfLaON after 1000℃ RTA. The existence of Hf, La, O, and N are clearly seen.

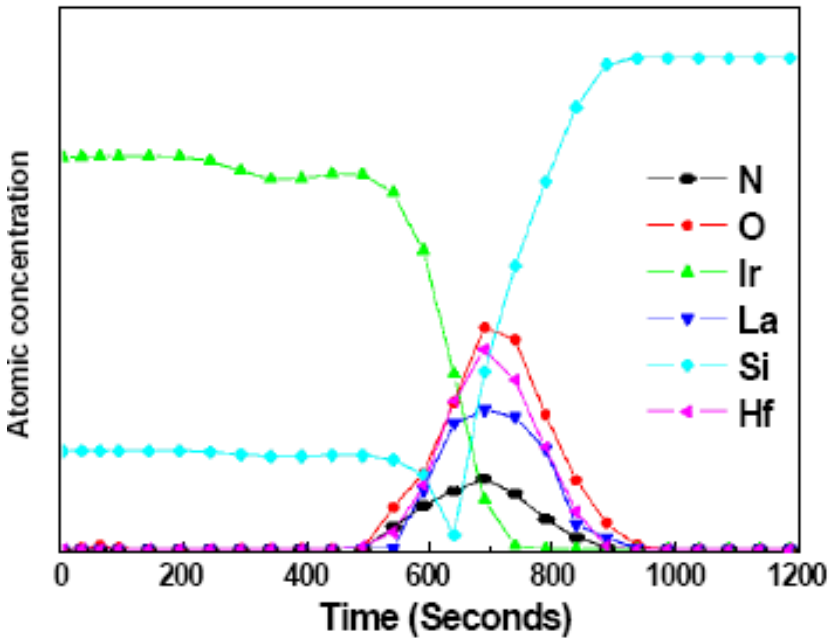

Fig. 3-4 AES profile of Ir_3Si/HfLaON/n-Si MOS structure after 1000℃ RTA. The Ir_3Si accumulated toward HfLaON interface is found to un-pin the Fermi-level.

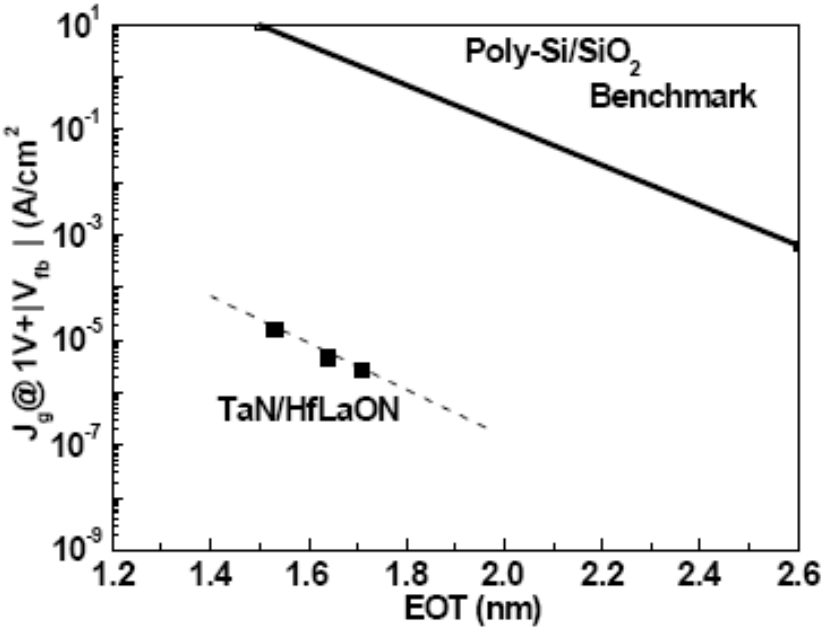

Fig. 3-5 The comparison of gate leakage current density for MOS devices with SiO_2 and HfLaON gate dielectrics.

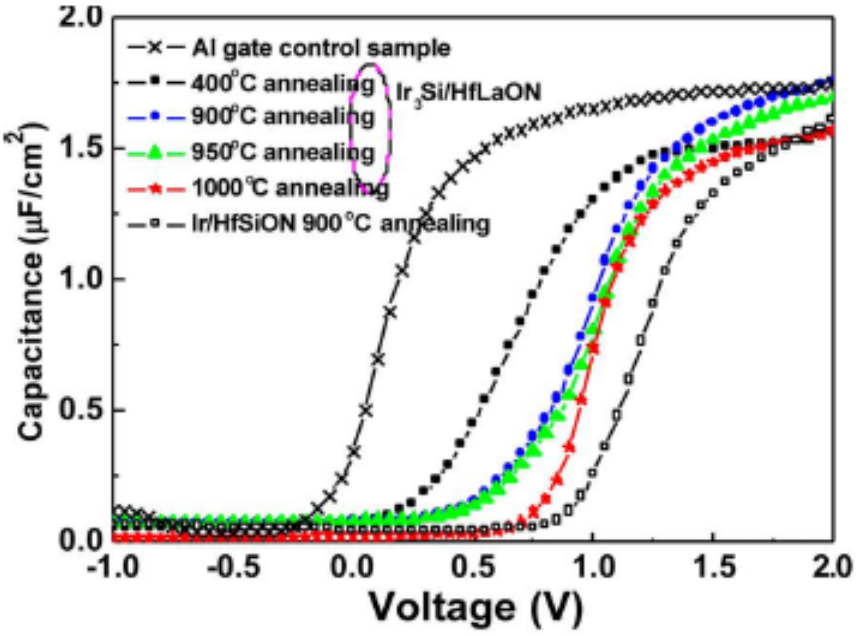

Fig. 3-6 C-V characteristics of Ir_xSi/HfLaON, Ir/HfSiON, and Al/1000℃-annealed-HfLaON capacitors measured under accumulation. The device area is 100 μm×100 μm.

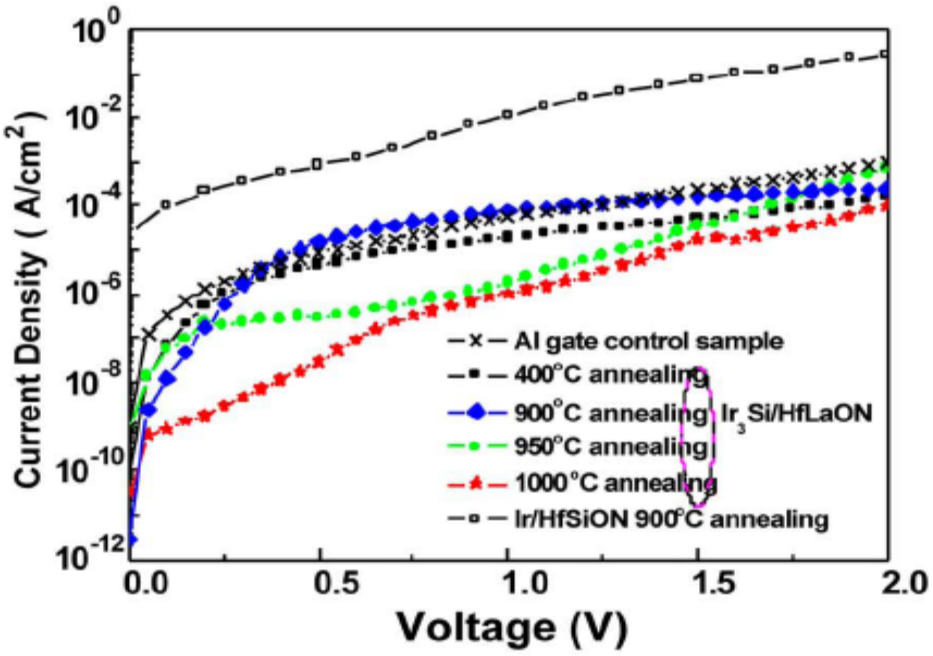

Fig. 3-7 J-V characteristics of Ir_xSi/HfLaON, Ir/HfSiON, and Al/1000℃-annealed-HfLaON capacitors measured under accumulation. The device area is 100 μm×100 μm.

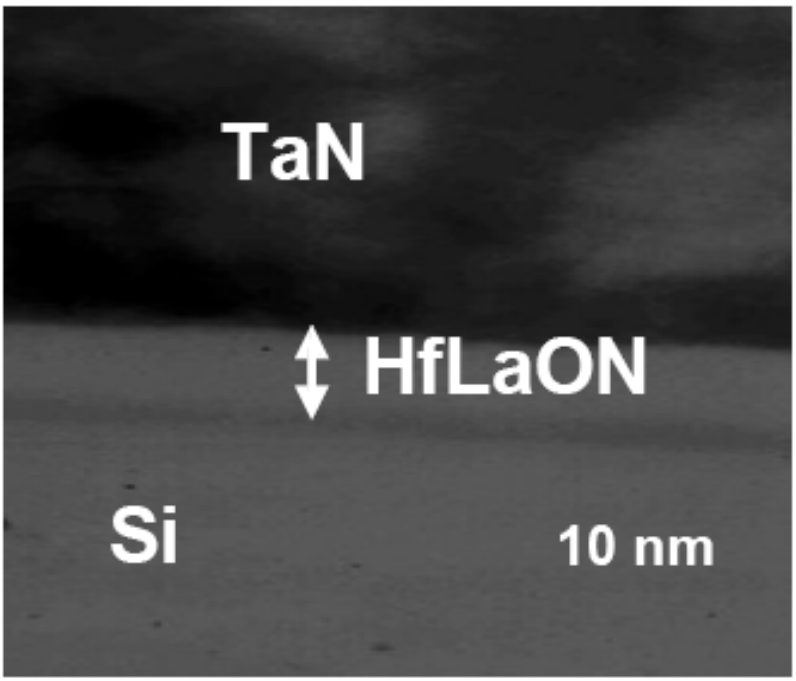

Fig. 3-8 TEM image of TaN/HfLaON/Si after 1000℃ RTA. Good interface property is observed with very thin interfacial layer.

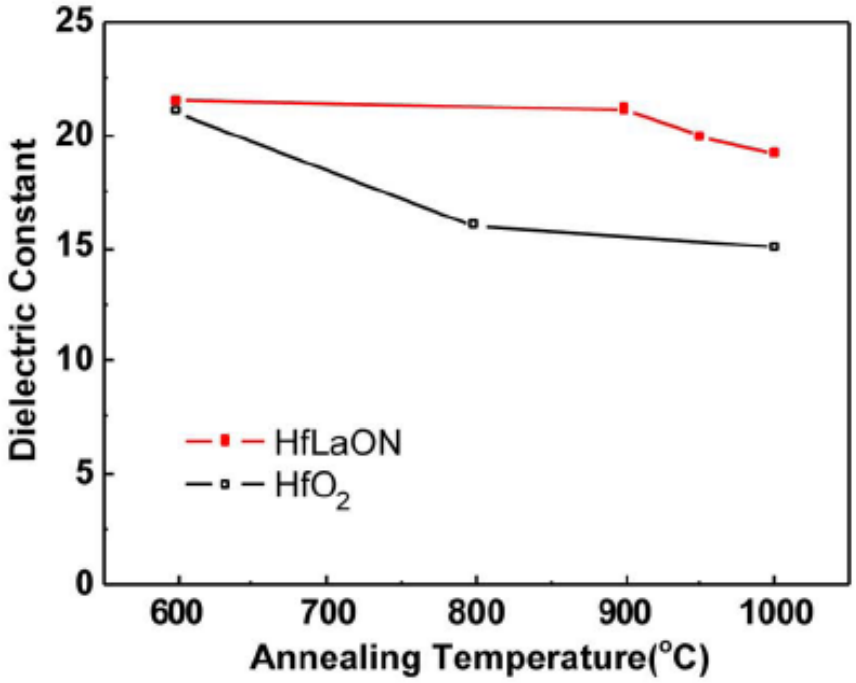

Fig. 3-9 The dielectric constant of HfLaON and HfO_2 at different RTA temperatures.

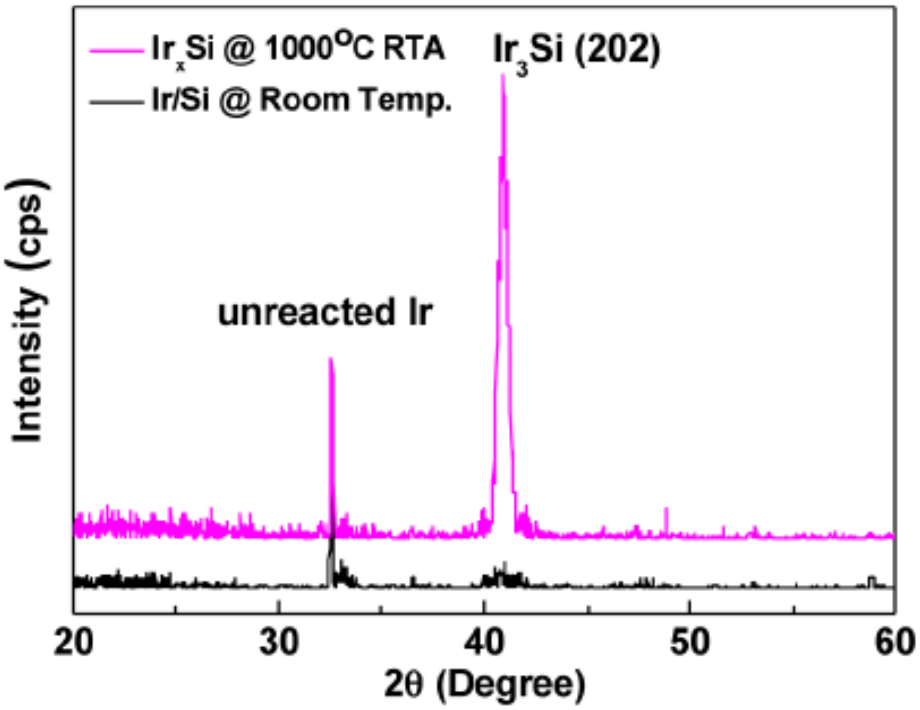

Fig. 3-10 XRD profiles of Ir3Si/HfLaON structure.

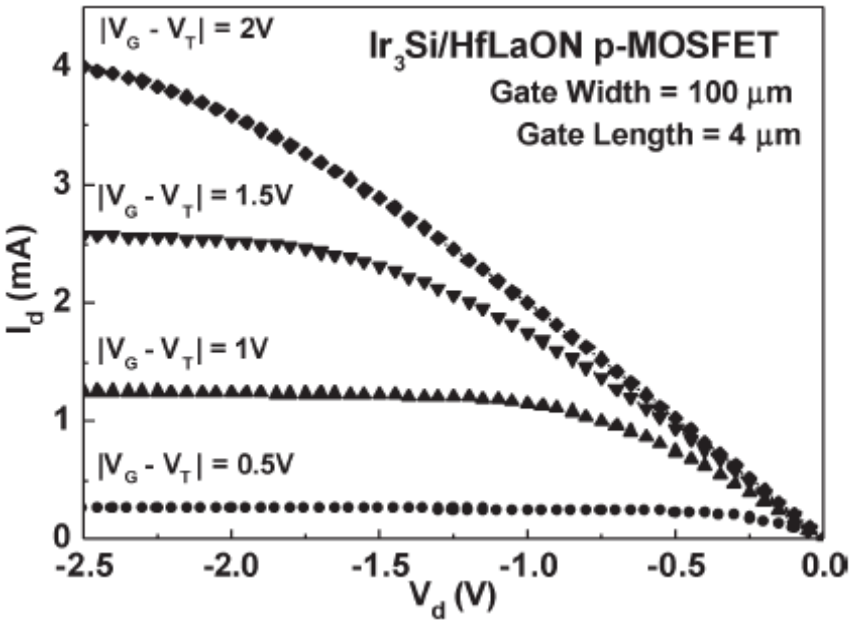

Fig. 3-11 The *Id-Vd* characteristics of Ir_3Si/HfLaON p-MOSFETs. The gate length is 4 μm

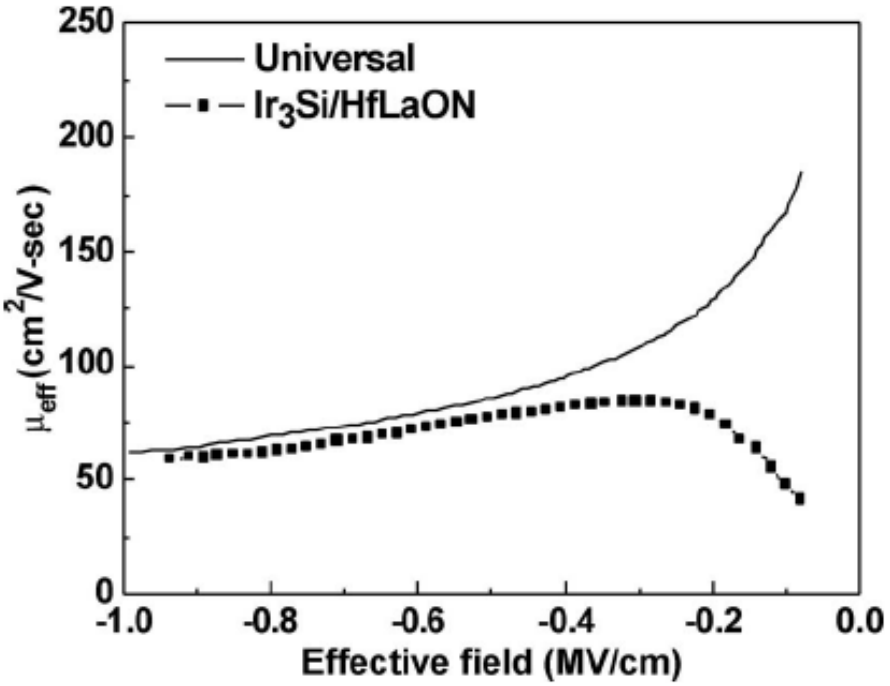

Fig. 3-12 The hole mobility as a function of gate electric field of Ir_3Si/HfLaON p-MOSFETs.

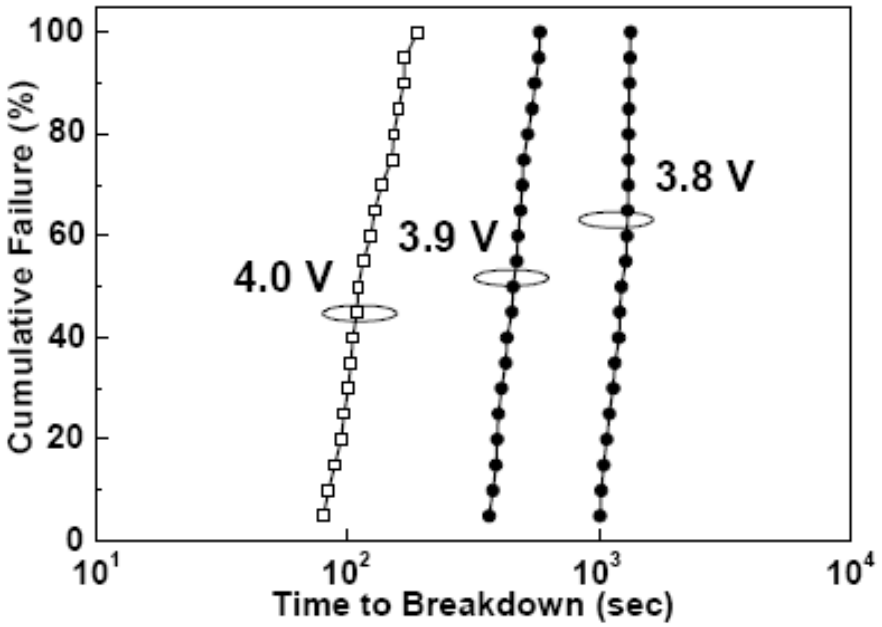

Fig. 3-13 The accumulative failure vs. time-to-breakdown of HfLaON PMOS after 1000℃ RTA.

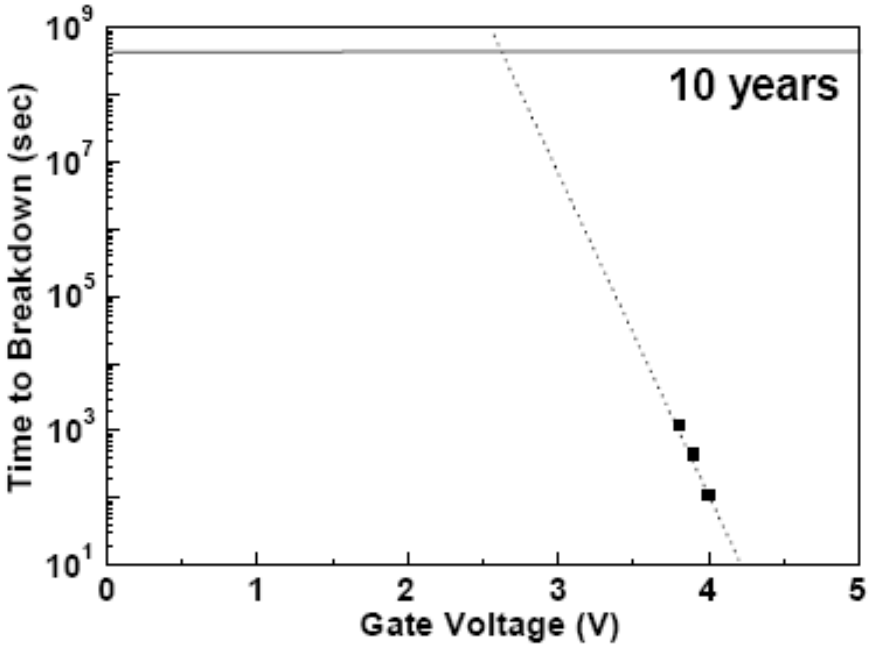

Fig. 3-14 The maximum 10-year operation voltage plot from MTTF-tBD plot in Figure 3-13. Large extrapolated voltage of 2.6 V is obtained for 10 years operation.

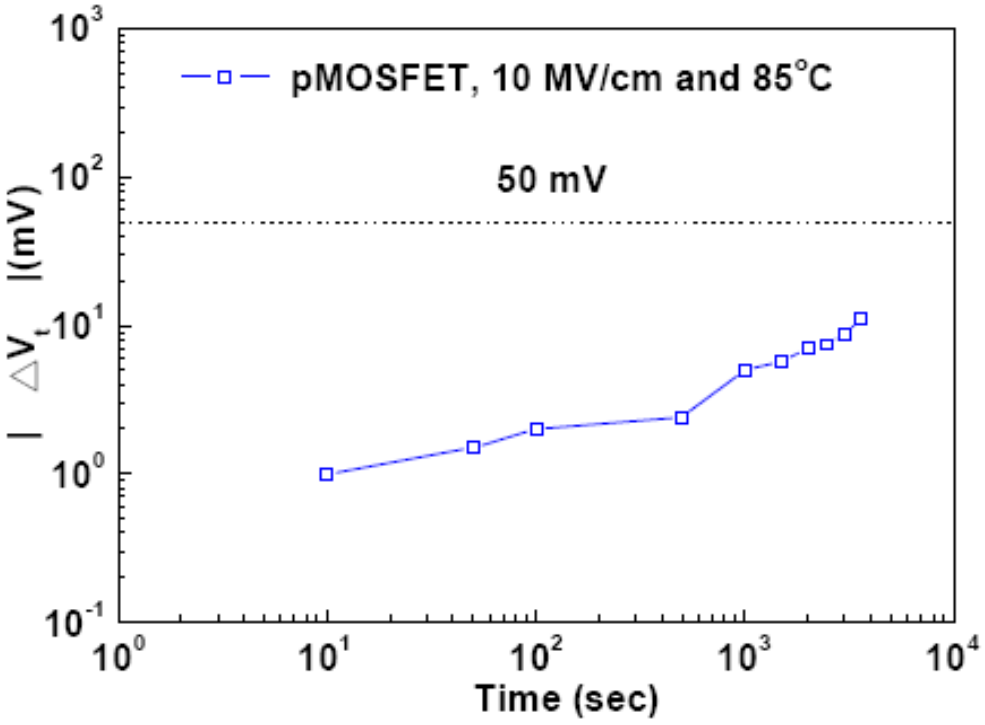

Fig. 3-15 The ΔVt shift of Ir_xSi/HfLaON p-MOSFETs stressed at 85℃ and 10 MV/cm for 1 hour.

High-κ	Crystallization	Metal Gate	$\phi_{m\text{-}eff}$ (eV)	V_t (V)	RTA Temp.	μ (cm^2/Vs)
HfLaON	>1000°C	TaN	4.24	0.18	1000°C	217
HfO_2 [1]	600°C	TaC	4.28	-	1000°C	250
HfAlON [4]	>1000°C	Yb_xSi	4.15	0.1	Gate last	180
HfSiON [6]	>1000°C	$NiSi_2$	4.4	0.47	Gate last	230
HfLaO [15]	900°C	TaN	3.9	-0.32	1000°C	240
HfLaON	>1000°C	Ir_xSi	5.08	-0.10	1000°C	84
HfO_xN [19]	-	$PtSi_x$	4.86	-0.39	Gate last	130
HfAlON [4]	>1000°C	Ir_xSi	4.9	-0.29	950°C	80
HfSiON [6]	>1000°C	Ni_3Si	4.8	-0.69	Gate last	65
HfLaO [15]	900°C	Pt	5.5	+0.6	1000°C	60

Table 3-1 The table summarizes the comparison among various metal-gate/ high-κ CMOS.

Chapter 4

Conclusion

We report novel 1000℃-stable HfLaON p-MOSFET with Ir_3Si gate. Low leakage current of 1.8×10^{-5} A/cm^2 at 1 V above flat band voltage, good effective work function of 5.08 eV and high mobility of 84 cm^2/Vs are simultaneously obtained at 1.6 nm equivalent-oxide thickness. This gate-first p-MOSFET process with self-aligned ion implant and 1000℃ RTA is fully compatible to current VLSI fabrication lines.

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