國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

射頻功率偵測器的應用

Applications of RF Power Detectors

研究生：謝易耕

指導教授：郭建男 教授

中 華 民 國 九十七 年 七月

射頻功率偵測器的應用

Applications of RF Power Detectors

研究生: 謝易耕　　Student: Yi-Keng Hsieh

指導教授: 郭建男　　Advisor: Chien-Nan Kuo

國立交通大學

電子工程學系 電子研究所碩士班

碩士論文

A Thesis

Submitted to Department of Electronics of Engineering & Institute of

Electronics College of Electrical Engineering and Computer Engineering

National Chiao Tung University

In Partial Fulfillment of the Requirements

For the Degree of

Master

In

Electronic Engineering

July 2008

Hsinchu, Taiwan, Republic of China

中華民國 九十七年 七月

射頻功率偵測器的應用

學生 : 謝易耕　　指導教授 : 郭建男　教授

國立交通大學

電子工程學系　電子研究所碩士班

摘要

本論文提出兩個射頻功率偵測器的應用電路。主要是利用現有的射頻電路架構搭配一些功能性的類比電路，而以功率比較的方式達成射頻偵測的目的。第一個電路應用在 WiMAX 傳送端上。為了能完成 I/Q 自動校正的閉迴路系統，一個具有較寬動態範圍的射頻功率偵測電路是必須的。此電路使用了台積電 0.18um，而模擬結果顯示在本地振盪器漏訊號，IQ 增益及相位誤差補償模式下都符合規格要求。

另一個應用則是 5GHz 低雜訊放大器的自我測試電路。偵測待側電路增益的方法是以可調整式衰減器及兩個射頻功率偵測器的輸出進行比較的方式達成。後模擬結果顯示，可以完成一個增益為 15.68dB 的低雜訊放大器的偵測。不幸地，因為天線效應的影響，量測沒辦法和模擬結果相互驗證。之後，提出另一個自我測試電路的架構，主要是以電阻分壓的方式來克服對溫度及製程變異的影響。

Applications of RF power detector

Student : Yi-Keng Hsieh Advisor : Chien-Nan Kuo

Department of Electronics Engineering & Institute of Electronics

National Chiao-Tung University

ABSTRACT

In this thesis, two applications of RF power detector are designed using power comparing methodology as a design principle. The first application is the power detection design in WiMAX transmitter. In order to form a closed loop I/Q auto-calibrated system, a wide dynamic range power and detection circuit is necessary. Simulations results show that the power detection circuitry designed in TSMC 0.18um technology meets the specifications in all compensation mode, such as LO feedthrough, gain imbalance, and phase imbalance.

Another application of RF power detector is the built-in self-test design for a 5GHz LNA. The circuit under test is test by a variable attenuator and comparing the DC output of the power detectors. The post-simulation results show that the circuit achieves gain test for a 15.68dB, 5GHz LNA. Unfortunately, function verifications cannot be made due violations of the antenna rule. Another BIST architecture using voltage division by a resistor string is also proposed to break-through the bottlenecks of sensitive to process and temperature variations.

誌謝

能夠完成畢業論文，順利取得碩士學位，要感謝的人真的很多。首先是，我的父母親，能夠提供我一個沒有經濟負擔的環境一路往上念，並且適時關心我，並鼓勵我繼而攻讀博士學位。再來，我要對我的指導教授至上誠摯的感謝。這兩年來，不僅提供了良好的研究環境與設備，並且讓我對射頻及類比電路的領域有深層的了解。適時的指點迷津，讓我學習到有邏輯的分析方法與嚴謹的研究態度。此外我要對昶綜與宗男兩位學長致上萬分的謝意，除了教導我許多軟體與硬體上的使用，也時常分享寶貴的研究與人生經驗，讓我一直有學習的好榜樣。

感謝實驗室的其他學長姐，俊興、燕霖、淑惠、明清、鴻源、鈞琳、培翔等的不吝指教與技術支援。感謝一起奮鬥一起研究的好同學，煥昇，以及建忠、子超、俊豪、信宇、俊毅、瑋琪、佑偉、宇航等學弟，你們使實驗室不再是一個無聊的地方。

最後感謝女朋友詠文從大學一直到研究所的陪伴，謝謝你在這兩年碩士生活中陪伴我走過許多人生的起起伏伏。在我研究上遇到瓶頸時，你的鼓勵與支持讓我走過種種一切的不如意;在我忙碌於研究時，你總是默默的陪伴在我身邊替我加油，讓我能無後顧之憂的向成功邁進。

謝易耕

九十七年 七月

CONTENTS

Abstract (Chinese)……I

Abstract (English)……II

Acknowledgments……..….III

Contents……IV

Table Captions……VII

Figure Captions……VIII

Chapter I Introduction……1

1.1 Motivation……...1

1.2 Thesis Organization……1

Chapter II Fundamentals of RF detection circuits……2

2.1 Introduction…….2

2.2 Meyer power detector…….3

2.3 Logarithmic amplifier…….9

Chapter III RF power detection circuit design in WiMAX transmitter……..16

3.1 Motivation……16

3.2 RF power detection circuit design……....20

3.2.1 Input buffer……...21

3.2.2 Pre-amplifier……22

3.2.3 Meyer power detector & PD buffer…….…….23

3.2.4 Comparator……...……26
3.3 Simulation results…….30
3.4 Chip layout & summary……31
Chapter IV Built-in self-test circuit designs for 5GHz LNA
4.1 Introduction……33
4.2 RF BIST design with a digital step attenuator……..34
4.2.1 The BIST architecture……....34
4.2.2 Low noise amplifier…….37
4.2.3 Switch A……...37
4.2.4 Power detector……38
4.2.5 Digital step attenuator…….....43
4.2.6 Design guidelines of the DSA…….…47
4.2.7 Post simulation results……..48
4.2.8 Chip implementations and measurement……..53
4.3 RF BIST design with R-72R ladder……..…61
4.3.1 Variations of the DSA…….…….61
4.3.2 R-72R voltage attenuator…….64
4.3.3 R-72R ladder and power detector combination……...…66
4.3.4 Current amp PD with high input impedance……....69
4.3.5 Comparator……70
4.4 Summary…….…74
Chapter V Conclusion and Future Work

5.1 Conclusion……76

5.2 Future Work……..76

References……77

TABLE CAPTIONS

Table 1 Attenuation levels……...…….36

Table 2 Performance summary of the CUT in operating mode……51

Table 3 Compare with recent RF BIST designs……...75

FIGURE CAPTIONS

Fig. 2-1 Meyer power detector…….. 3

Fig. 2-2 Transfer curve of the Meyer power detector……6

Fig. 2-3 Frequency response of the Meyer power detector ……...8

Fig. 2-4 Logarithmic transfer curve……..11

Fig. 2-5 PN-junction based log amp…….12

Fig. 2-6 Principle diagram of successive detection logarithmic amplifier……...14

Fig. 2-7 Behavior model simulation of a log amp……15

Fig .3-1 Direct up-conversion mixer with auto-calibration for I/Q imbalance and LO feedthrough……...18

Fig. 3-2 LO feedthrough of one side of the I/Q mixer's output vs. control bits…….…...19

Fig. 3-3 The RF output signal of I/Q mixer's during gain error test vs. control bits...20

Fig. 3-4 RF power detection architecture…….21

Fig. 3-5 Simulation of input matching…….22

Fig. 3-6 Simulation of the switching path……23

Fig. 3-7 Meyer PD transfer curve…….25

Fig. 3-8 PD buffer transfer curve…….25

Fig. 3-9 Simulation results of the circuits before comparator……..26

Fig. 3-10 Schematic of comparator……..27

Fig. 3-11 Timing of the comparator…….28

Fig. 3-12 Simulation results of the comparator……30

Fig. 3-13 Simulation results of gain error and LO feedthrough……...31

Fig. 3-14 Layout of the RF power detection circuit…….32

Fig. 4-1 Proposed BIST architecture……34

Fig. 4-2 Modes of the RF BIST……...35

Fig. 4-3 Circuit under test……37

Fig. 4-4 Switch A……38

Fig. 4-5 PD characteristic curve……...38

Fig. 4-6 Power detectors……...40

Fig. 4-7 Time response with different input levels……...43

Fig. 4-8 Digital step attenuator……44

Fig. 4-9 DSA check……..46

Fig. 4-10 Post simulation results of the CUT……...50

Fig. 4-11 Test mode……..52

Fig. 4-12 Die photo……..53

Fig. 4-13 Violations of antenna rule……54

Fig. 4-14 Measurement results……58

Fig. 4-15 P1dB measurements……59

Fig. 4-16 Noise figure……..59

Fig. 4-17 Power detector curve measurement……..60

Fig. 4-18 Observation of process variations for the DSA……61

Fig. 4-19 27°C Simulation……...62

Fig. 4-20 55°C Simulation……...63

Fig. 4-21 R-72R Ladder……...65

Fig. 4-22 Simulation result of the R-72R ladder……..66

Fig. 4-23 Combination ideas……67

Fig. 4-24 High impedance power detector……...70

Fig. 4-25 Input offset cancellation……...71

Fig. 4-26 Schematic of the comparator……72

Fig. 4-27 Modified BIST architecture……73

Chapter I

Introduction

1.1 Motivation

A RF power detection circuit for auto-compensating I/Q mismatch and LO-feedthrough of the direct up-conversion mixer is necessary to form a closed-loop design in my senior's project [1]. The first task was to design cascading stages of RF power detection circuits, including a pre-amplifier, a power detector, and a comparator, that can meet the specifications given. Some of the design backgrounds of RF power detection during this work is covered up. Furthermore, this motivates research topics on applications for the power detectors, such as built-in self test (BIST) designs for RF-circuits.

In this thesis, a RF BIST design using power comparing method instead of designing wide dynamic range and low error power detectors to test the gain of a low noise amplifier is described. Another work of modifying the original idea is also proposed to break-through the bottleneck of process variations.

1.2 Thesis organization

In Chapter II, some of the backgrounds of the RF detection techniques will be cover. In Section 2.1, basics of Meyer power detector along with its design equations are introduced. The successive detection theory of the logarithmic amplifier is written in Section 2.2. In Chapter III, the power detection circuit design in a WiMAX transmitter is introduced. In Chapter IV, BIST circuit designs for 5GHz LNA are described. Finally, some conclusion and future work is written in Chapter V

Chapter II

Fundamentals of RF detection circuits

2.1 Introduction

This chapter introduces some of the recent approaches of detecting RF signals. The surveyed publications can be categorized into two groups. One group is the circuits that detect RF signals directly and convert it into a DC value [2]-[12] which are able to work at frequencies GHz-frequencies, such as power detector, peak detector, amplitude detector, RMS detector, rectifier, etc.

The other one is the logarithmic amplifier (log amp) [13]-[20] that can convert a large dynamic range dB-linear input into small dynamic range linear output which usually works at MHz-frequencies. Logarithmic amplifiers are typically used in AGC-loops as RSSIs (received signal strength indicator) to detect the signal amplitude. Especially in communication systems, it is very important to know the incoming signal level accurately so that a reliable decision between a successful or a failed connection can be made. Also the required number of bits for the A/D-converter which is usually placed as the following circuit block can be more relaxed with an AGC amplifier. This implies that the dynamic range, accuracy, and process dependency are the major design challenges. Logarithmic amplifier can also be arranged as the succeeding stage of a power detector [10]-[12] (or the other detectors mentioned above) that compress the large dynamic range to a readable output during detection.

In Section 2.2, a popular Meyer power detector is analyzed by means of Taylor

series. In Section 2.3, an overview of the logarithmic amplifier is given.

2.2 Meyer power detector

A monolithic low power RF power detector using bipolar transistors (f_T=8GHz) was first invented by Meyer [2] in 1995. This detector can be used for embedded RFIC test because it has the advantages of simplicity, wide bandwidth, low power, small chip size, and temperature stability. The detector was also analyzed by Zhang using similar approach, such as Bessel function [3]. A modified design was also proposed to extend its dynamic range. The following will repeat their analysis by means of Taylor series and replace the bipolar transistors with MOSFET biased at sub-threshold region which the current is also expressed in exponential function.

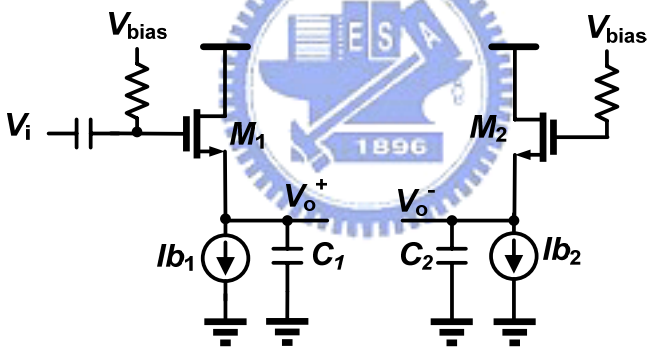


Fig. 2-1 Meyer power detector

Fig. 2-1 is the schematic of a Meyer power detector (Meyer PD). M_1 acts as the nonlinear rectifying element on signal voltage V_i. Transistor M_2 sets up a replica circuit so that DC voltage $V_O(=V_O^+ - V_O^-)$ is zero for zero AC signal input at V_i. Notice that M_1 and M_2 are identical and are biased at their sub-threshold region. C_1 and C_2 are large enough to filter out the unwanted high frequency components and generate a pure DC output as possible. V_O can be expressed as:

$$V_O = V_O^+ - V_O^- = (V_X - V_O^-) - (V_X - V_O^+) = V_{GS2} - V_{GS1} \tag{2.1}$$

The sub-threshold current of M_1 can be expressed as:

$$\begin{aligned} i_{D1} &= I_{D0}\frac{W}{L}\exp[\frac{v_{GS1} - V_{THN}}{nV_T}] \\ &= I_{D0}\frac{W}{L}\exp[\frac{(V_{GS1} + v_{gs}) - V_{THN}}{nV_T}] \\ &= I_{D0}\frac{W}{L}\exp[\frac{V_{GS1} - V_{THN}}{nV_T}] * \exp[\frac{v_{gs}}{nV_T}] \\ &= I_{D0}\frac{W}{L}\exp[\frac{V_{GS1} - V_{THN}}{nV_T}] * [1 + (\frac{v_{gs}}{nV_T}) + \frac{1}{2!}(\frac{v_{gs}}{nV_T})^2 + \frac{1}{3!}(\frac{v_{gs}}{nV_T})^3 + \frac{1}{4!}(\frac{v_{gs}}{nV_T})^4 + ...] \end{aligned} \tag{2.2}$$

Set $v_{gs} = V_{in}\cos\omega t$, where V_{in} is the amplitude of the input signal and ω is the input frequency

then, ${v_{gs}}^2 = {V_{in}}^2\cos^2\omega t = {V_{in}}^2\frac{1+\cos 2\omega t}{2}$, there will be a DC term such as $\frac{{V_{in}}^2}{2}$

Similarly, we can get: ${v_{gs}}^4 = [{V_{in}}^2\frac{1+\cos 2\omega t}{2}]^2$, and there will be a DC term such as $\frac{3{V_{in}}^4}{8}$

So the DC term of i_{D1} will be:

$$I_{D0}\frac{W}{L}\exp[\frac{V_{GS1} - V_{THN}}{nV_T}] * [1 + \frac{1}{2!}(\frac{1}{nV_T})^2\frac{{V_{in}}^2}{2} + \frac{1}{4!}(\frac{1}{nV_T})^4\frac{3{V_{in}}^4}{8} + ...] \tag{2.3}$$

Since identical current sources are used, the equation can be written as:

$$\begin{aligned} & I_{D1} = I_{D2} \\ \Rightarrow\ & I_{D0}\frac{W}{L}\exp[\frac{V_{GS1} - V_{THN}}{nV_T}] * [1 + \frac{1}{2!}(\frac{1}{nV_T})^2\frac{{V_{in}}^2}{2} + \frac{1}{4!}(\frac{1}{nV_T})^4\frac{3{V_{in}}^4}{8} + ...] = I_{D0}\frac{W}{L}\exp[\frac{V_{GS2} - V_{THN}}{nV_T}] \\ \Rightarrow\ & [1 + \frac{1}{2!}(\frac{1}{nV_T})^2\frac{{V_{in}}^2}{2} + \frac{1}{4!}(\frac{1}{nV_T})^4\frac{3{V_{in}}^4}{8} + ...] = \exp[\frac{V_{GS2} - V_{GS1}}{nV_T}] \end{aligned} \tag{2.4}$$

With (2.1) and (2.4) $V_o = nV_T * \ln[1 + \frac{1}{2!}(\frac{1}{nV_T})^2\frac{{V_{in}}^2}{2} + \frac{1}{4!}(\frac{1}{nV_T})^4\frac{3{V_{in}}^4}{8} + ...]$

(2.5)

When V_{in} is small, V_O can be approximated as:

$$V_o = nV_T * \ln[1 + \frac{1}{2!}(\frac{1}{nV_T})^2 \frac{{V_{in}}^2}{2}] \approx \frac{{V_{in}}^2}{4(nV_T)} \qquad (2.6)$$

(2.6) shows that when the input signal is small, the differential DC output will be proportional to the square of the input signal amplitude and this is referred as the square law region of the power detector. Besides, it is apparent that the output is approximately inversely proportional to absolute temperature. Temperature could be compensated by dividing by a quantity proportional to temperature. Meyer also derived the equation for large V_{in} and the DC output can be expressed as:

$$V_o = V_{in} - V_T \ln \sqrt{\frac{2\pi V_{in}}{nV_T}} \qquad (2.7)$$

This can be approximated as a linear relation between V_O and V_{in}.

We can conclude shortly that the power detector can work in the linear region for large signal detection and in square law region for small signal detection. Fig. 2-2 is a simulation of a Meyer PD using TSMC 0.18um technology to verify the mathematical derivation above. The transition power level of the linear and square law region is about -15dBm. The dynamic range is at least -35dB for the square law region and 25dB for the linear region. Notice that the output of Meyer PD is logarithmic linear.. A logarithmic amplifier can be added behind the PD to convert linear in dB input into linear output.

Instead of examining the Meyer PD by tedious mathematical equations, we can still use our "engineer's intuition" to explain the mechanism. Re-visit Fig. 2-1 and assume that there isn't any input signal. Hence, the V_{GS} of both transistors will ideally be the same since they are biased with identical current sources. While there is an input signal, *M1* then adjusts its V_{GS} to maintain the constant DC current. Since the gate voltage of *M1* is fixed, its source (V_O^+) will change proportionally to the strength

of the input.

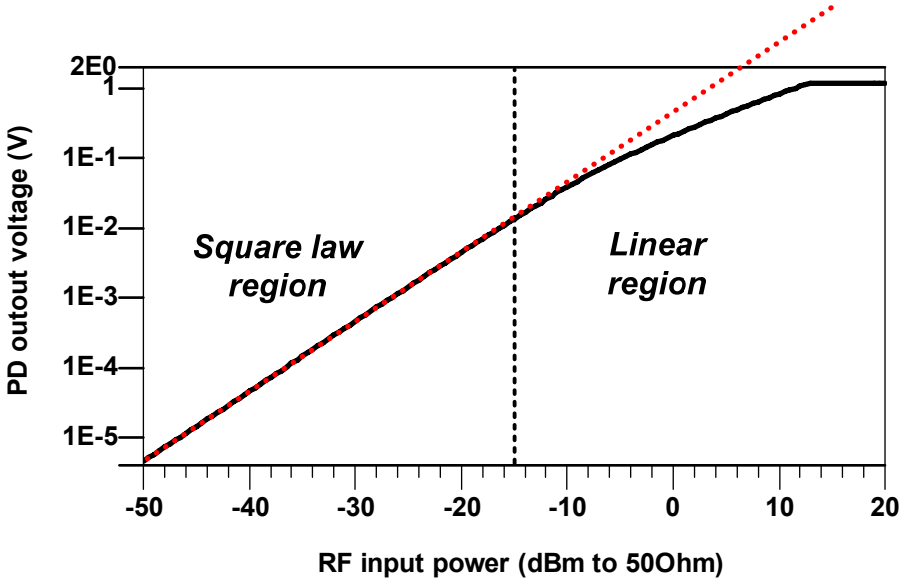


Fig. 2-2 Transfer curve of the Meyer power detector

In [3], an analysis of a periodic input signal of any shape instead of a pure sinusoidal is given. It shows that the possibilities of Meyer PD in multi-tone detections. The input periodic signal can be represented as the sum of *N* harmonics, where *N* is a positive integer.

$$V_i = \sum_{i=1}^{N} V_{in,i} \cos(\omega_i t + \theta_i) \tag{2.8}$$

where $V_{in,i}$, ω_i, θ_i are the amplitude, angular frequency, and phase of the *i*th harmonic.

Thus, the current of *M1* can be expressed as:

$$\begin{aligned} i_{D1} &= I_{D0} \frac{W}{L} \exp[\frac{v_{GS1} - V_{THN}}{nV_T}] \\ &= I_{D0} \frac{W}{L} \exp[\frac{V_{GS1} + v_{gs1} - V_{THN}}{nV_T}] \\ &= I_{D0} \frac{W}{L} e^{\frac{V_{GS1} - V_{THN}}{nV_T}} \prod_{i=1}^{N} e^{\frac{V_{in,i} \cos(\omega_i t + \theta_i)}{nV_T}} \end{aligned} \tag{2.9}$$

The equation above can be re-written in the form of Bessel functions [23].

$$i_{D1} = I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}e^{\frac{V_{in,i}\cos(\omega_i t+\theta_i)}{nV_T}}$$

$$= I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}[I_0(b_i)+2I_1(b_i)\cos(\omega_i t+\theta_i)+2I_2(b_i)\cos(\omega_i t+\theta_i)+....] \quad (2.10)$$

where $I_0(b_i)$ is modified Bessel function of n and $b_i = \frac{V_{in,i}}{nV_T}$.

It is seen in (2.10) that each harmonic (*i*th harmonic) produces a DC component $I_0(b_i)$ and other AC components. The total current depends on all of the harmonics. Since $\omega_i \neq \omega_j,\ \forall i \neq j$, cross-modulation among them does not produce any DC component. Thus, the DC current component of i_{D1} can be viewed as the result of DC components produced by the corresponding harmonics.

For small signal detection, where the b_i's are small,

$$I_0(b_i) \cong 1+\frac{{b_i}^2}{4} \quad (2.11)$$

Therefore, the DC current will be:

$$I_{D1} = I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}(I_0(b_i))$$

$$= I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}(1+\frac{{b_i}^2}{4})$$

$$= I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}(1+\frac{{V_{in,i}}^2}{4(nV_T)^2}) \quad (2.12)$$

Similarly, since identical DC current sources are used.

$$I_{D0}\frac{W}{L}e^{\frac{V_{GS1}-V_{THN}}{nV_T}}\prod_{i=1}^{N}(1+\frac{{V_{in,i}}^2}{4(nV_T)^2}) = I_{D0}\frac{W}{L}e^{\frac{V_{GS2}-V_{THN}}{nV_T}} \quad (2.13)$$

Combining (2.1) and (2.13),

$$V_o = V_{GS2} - V_{GS1} = nV_T \sum_{i=1}^{N} \ln(1 + \frac{V_{in,i}^{\ 2}}{4(nV_T)^2}) \cong \frac{1}{4nV_T} \sum_{i=1}^{N} V_{in,i}^{\ 2} \quad (2.14)$$

It shows that the output voltage is linearly proportional to the sum of the squares of all harmonics' amplitudes, which corresponds to the total power. However, no mathematical analysis for the linear region is given in [3] any further. Maybe analysis for multi-tone large signal detection will be another interesting research topic in the future.

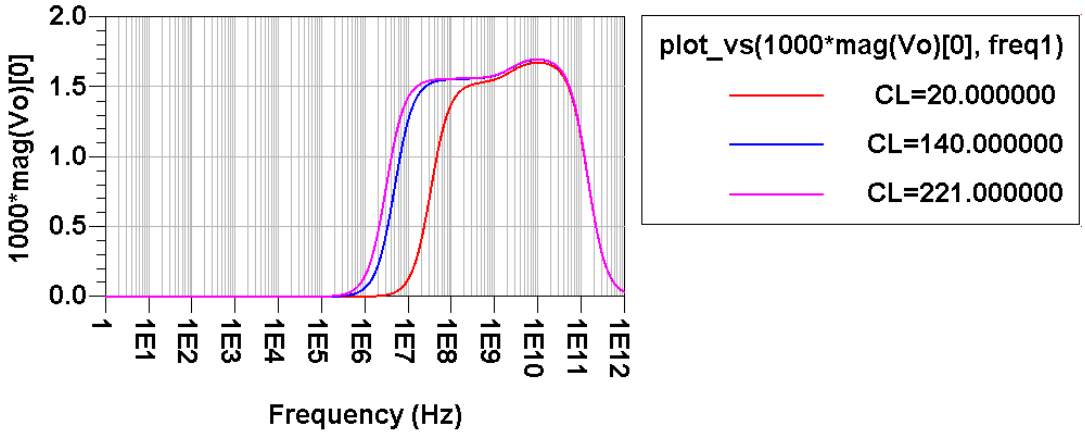


Fig. 2-3 Frequency response of the Meyer power detector

Fig. 2-3 shows that the Meyer PD can work in the GHz range. The low frequency response depends on the size of the loading capacitor.

2.3 Logarithmic amplifier

2.3.1 Ideal logarithmic transfer function

The general transfer function of a logarithmic amplifier can be given as [13]

$$V_{out} = K_1 \log V_{in} + K_1 \log K_2 \tag{2.8}$$

where K_1 and K_2 are constants associated with the logarithmic amplifier. Fig. 2-2 shows the equation above graphically with three sets of K_1 and K_2. The design parameter K_2 can be solved by setting $V_{out} = 0$

$$K_1 \log V_{in} = -K_1 \log K_2$$

$$\Rightarrow K_2 = \frac{1}{V_{in}} \tag{2.9}$$

In Fig. 2-3(a) K_2 can be visualized to determine the starting point of logarithmic action. The larger K_2, the smaller V_{in} for $V_{out} = 0$. Increasing K_1 changes the degree of output compression. However, Fig. 2-3(b) is the best illustration which has a logarithmic x-axis. As can be seen, the output is a straight line. We will go one step further and define the x-axis in terms of dBm, as depicted in Fig. 2-3(c).

The corresponding voltage magnitude of RF power referring to 50Ohm can be expressed as:

$$V_{in}\big|_{dBm} = 30 + 10 * \log \frac{(\frac{V_{in}}{\sqrt{2}})^2}{50}$$

$$\Rightarrow V_{in}\big|_{dBm} = 30 + 10 * \log \frac{V_{in}^{\ 2}}{100} \tag{2.10}$$

$$\Rightarrow V_{in} = 10 * 10^{\frac{V_{in}|_{dBm} - 30}{20}}$$

Substituting (2.10) into (2.8)

$$V_{out} = K_1 \log 10 * 10^{\frac{V_{in}|_{dBm} - 30}{20}} + K_1 \log K_2$$
$$\Rightarrow V_{out} = K_1 (1 + \frac{V_{in}|_{dBm} - 30}{20}) + K_1 \log K_2 \quad (2.11)$$

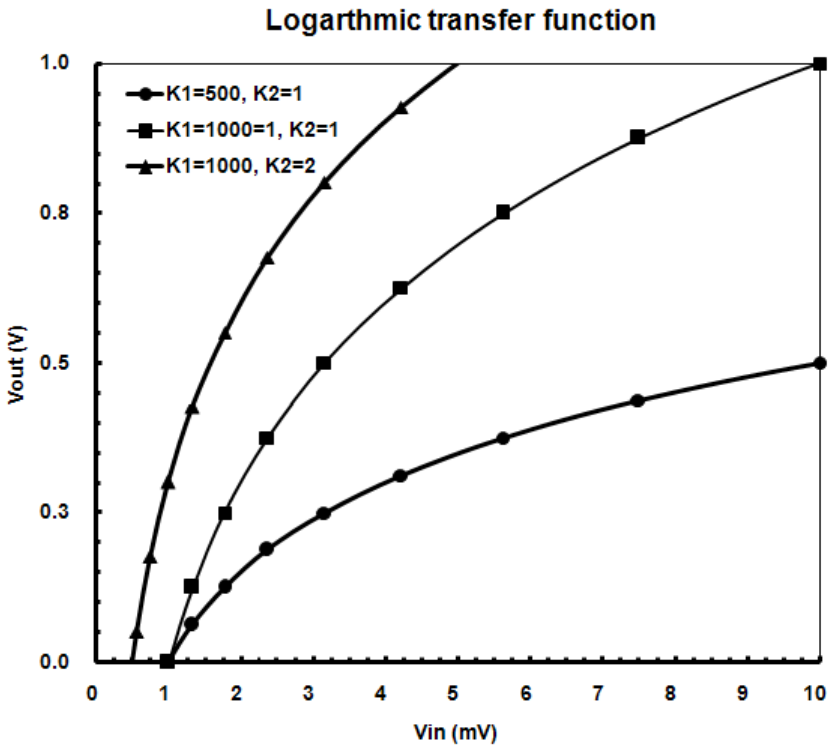
Thus, (2.11) is a straight line with logarithmic slope (LS) of

$$LS = \frac{K_1}{20}\left(\frac{mV}{dB}\right) \quad (2.12)$$

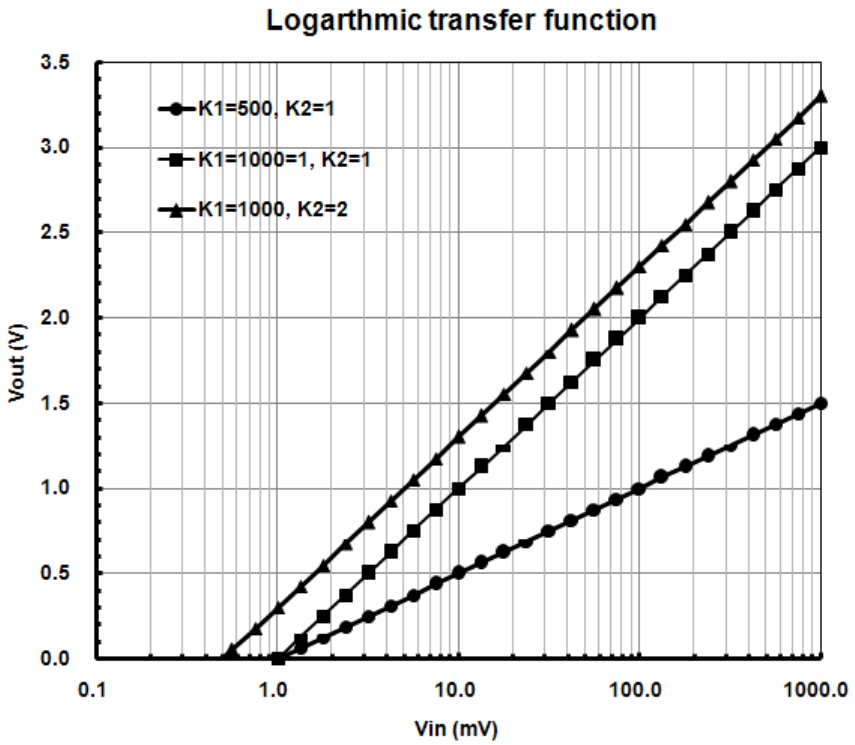
The start of logarithmic action $V_{in}|_{dBm}^{V_{out}=0}$, the input power level that makes output voltage equals to zero, may be found from (2.11) as:

$$V_{in}|_{dBm} = 20(-1 - \log K_2) + 30 \quad (2.13)$$

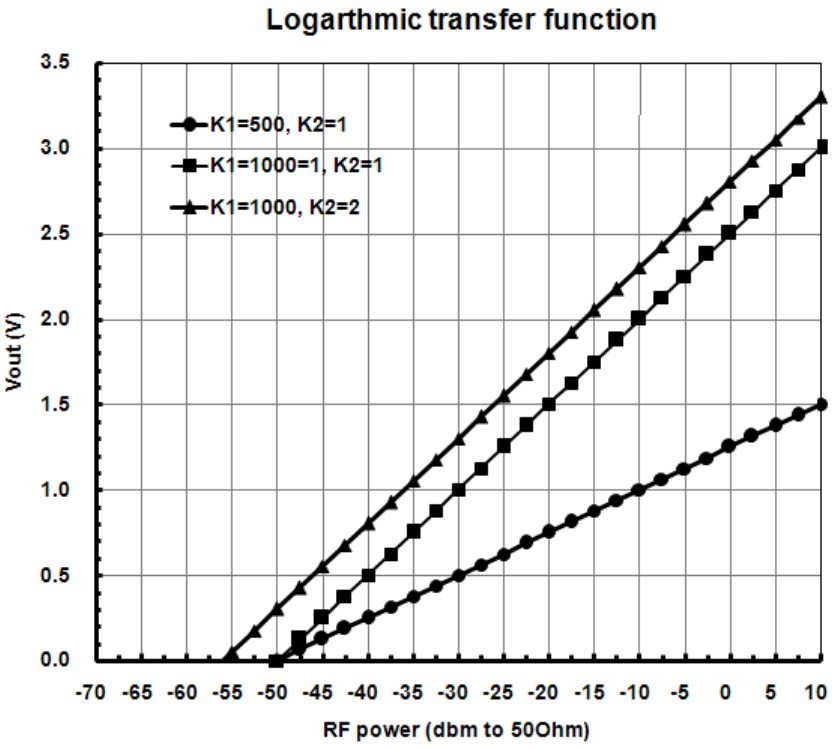
By (2.13), the zero crossing points in Fig. 2-3 can be calculated for *K2*=1,2 respectively. The designer usually controls the starting point and LS of a logarithmic transfer function to the desired values.



(a)



(b)



(c)

Fig. 2-4 Logarithmic transfer curve (a) V_{in} in linear scale (b) V_{in} in log scale (c) The corresponding RF input power of V_{in}

2.3.2 Transfer function implementations

An inverting OP amp with PN-junction feedback and successive detection are mainly the two approaches of implementing the logarithmic transfer function. Fig. 2 -5 gives an example of PN-junction based log amp.

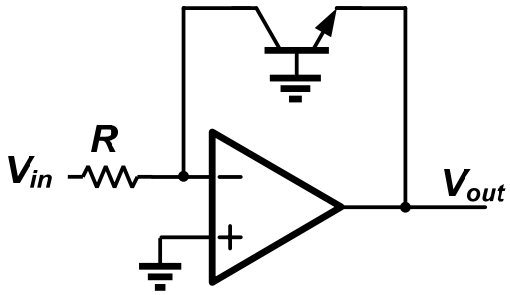


Fig. 2-5 PN-junction based log amp

Since the bipolar transistor forms a negative feedback around the OP amp, the current passing through *R* and the bipolar transistor can be expressed as follows:

$$I_{in} = \frac{V_{in}}{R} = I_s \exp[\frac{V_{be}}{V_T} - 1] \approx I_s * \exp[\frac{V_{be}}{V_T}] \tag{2.14}$$

So the output can be derived as:

$$V_{out} = -V_{be} = -V_T * \ln \frac{V_{in}}{I_s R} \tag{2.15}$$

However, this type of log amp has limited dynamic range at high frequencies due to the gain-bandwidth product limitation [16]. As such, the PN-junction has strong temperature dependency and affects the accuracy. Furthermore, offset voltages has to be compensated at very low signal levels.

An alternative structure is the successive detection based on the piecewise-linear approximation of the logarithmic transfer function. It has commonly been used because of better accuracy [13]-[20]. Fig. 2-6(a) is the principle diagram of the successive detection log amp and Fig. 2-6(c) shows circuit building clocks of a typical successive detection log amp.

Each stage represents a linear limiting amplifier that has the transfer curve shown in Fig. 2-6(b), where A_V is the gain and V_L is the maximum output of the limiting amplifier. When the input of each limiting stage exceeds $\frac{V_L}{A_V}$, the output will be saturated to V_L. So it is very straight forward to see that when V_{in} increases slowly, *stage n* will be saturated first, then *stage (n-1)*, and so on until all stages are limited.

The summed output V_{out} for Fig. 2-6(a) can be written as:

$$V_{out} = V_1 + V_2 + ... + V_n \tag{2.16}$$

Assume that $V_{in} = \frac{V_L}{A_V^4}$ and increases A_V times larger each step until all stages are limited (let n=4).

$V_{in} = \frac{V_L}{A_V^4}$, stage 4 is limited and $V_{out} = \frac{V_L}{A_V^3} + \frac{V_L}{A_V^2} + \frac{V_L}{A_V^1} + V_L$

$V_{in} = \frac{V_L}{A_V^3}$, stage 3 and 4 are limited and $V_{out} = \frac{V_L}{A_V^2} + \frac{V_L}{A_V^1} + 2V_L$

$V_{in} = \frac{V_L}{A_V^2}$, stage 2, 3 and 4 are limited and $V_{out} = \frac{V_L}{A_V^1} + 3V_L$

$V_{in} = \frac{V_L}{A_V^1}$, stage1, 2, 3 and 4 are limited and $V_{out} = 4V_L$

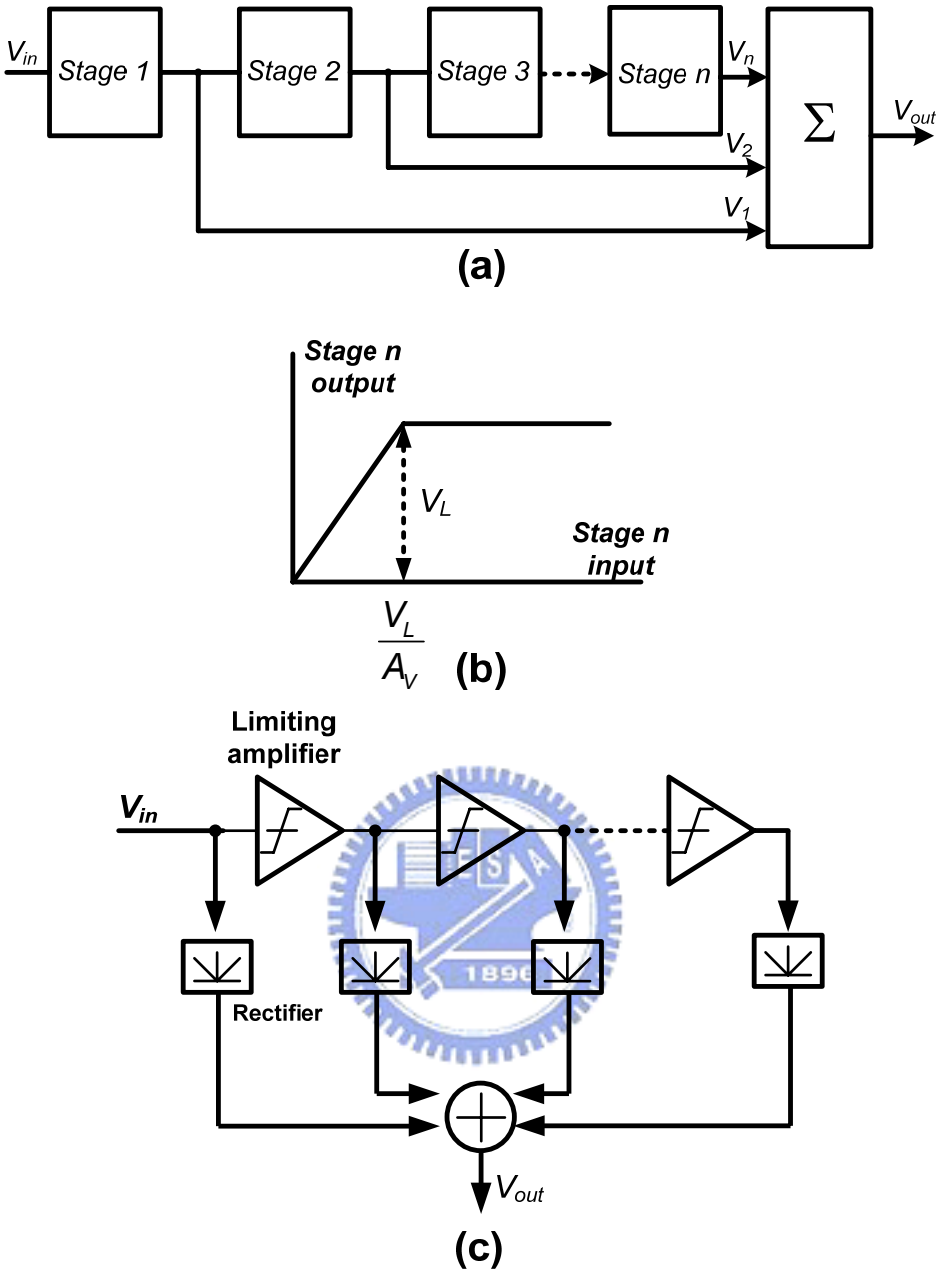


Fig. 2-6 (a) Principle diagram of successive detection logarithmic amplifier (b) Limiting amplifier transfer curve (c) Circuit block diagram

Here, we give a simple example of logarithmic amplifier that convert 70 dB dynamic range from -60 to10dBm (0.1mV~1000mV) input into a 0~1.8V output with four stages of limiting amplifier. Since four stages are used, then $4V_L \le 1.8$ and choose $V_L = 0.45$. The first transition point is at -50dBm, and means that $\frac{V_L}{A_v^4} = 1mV$ and $A_V = 4.605$. Fig. 2-7 is the simulation done by behavior model in

ADS environment.

The logarithmic function is useful but at the cost of hardware and design complexities. The following two chapters are some RF power detection designs that use comparing methods instead of trying to obtain the absolute power levels.

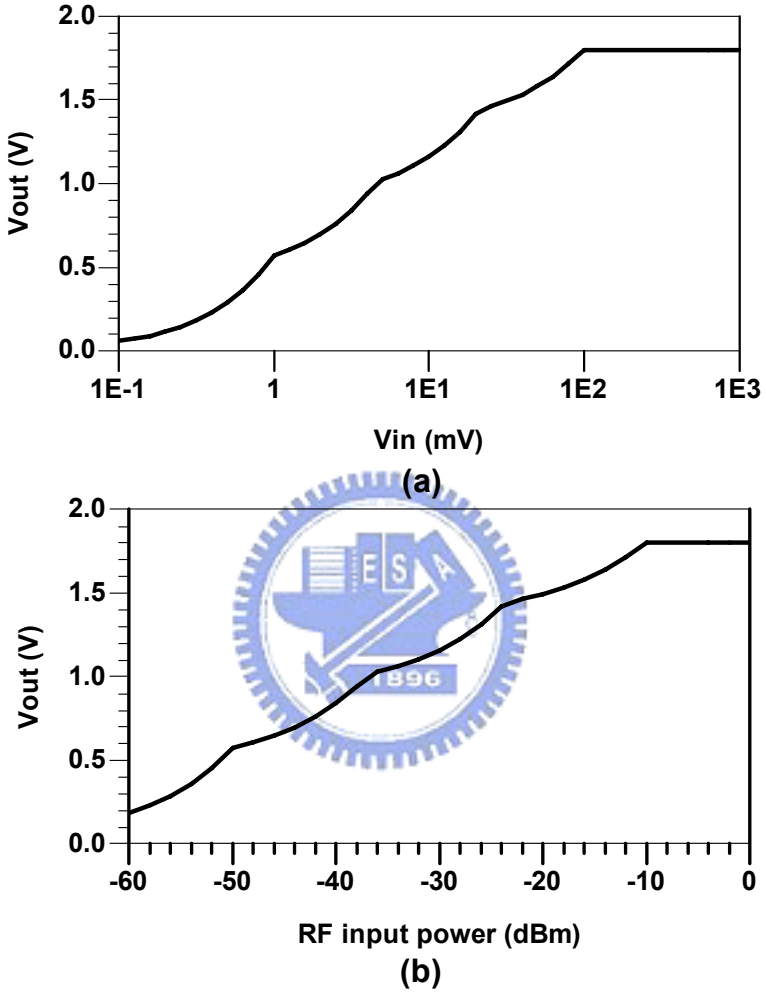


Fig. 2-7 Behavior model simulation of a log amp (a) *Vout* vs. *Vin* in log-scale (b) *Vout* vs. corresponding of *Vin* to 50Ohm

Chapter III

RF power detection circuit design in WiMAX transmitter

3.1 Motivation

The standard of IEEE 802.16 family, popularly known as WiMAX, provides wireless transmissions of high data rates over metropolitan areas. The transmitted signal format may include complicated modulation such as 64-QAM. To ensure correct data receiving, the measure of EVM (error vector magnitude) quantifies the error of transmitted signals and defines the performance of digital radio transmitters. It is therefore critical to minimize the EVM. Many non-ideal circuit effects contribute to EVM degradation in the RF end, including LO phase noise, carrier feed-through, I/Q imbalance, and nonlinearity. The normal figure of transmitter circuitry achieves the level from -20dB to -25dB. In the latest released WiMAX mobile standard, however, it defines a severe EVM level of -30dB which implies more advanced circuit designs is necessary.

Fig. 3-1 is the architecture of the proposed direct up-conversion mixer with auto-calibration for I/Q imbalance and LO feedthrough. The IF and RF frequency is designed at 10MHz and 2.6GHz respectively. The dotted box is the open loop design done by me senior [1]. It consists of two LO buffers to tune the gain/phase mismatch errors and IDACs on the transconductance stage of the Gilbert cell mixers to suppress the LO feedthrough. All of them are digitally controlled by the 3-wire shift register.

In order to accomplish an auto-calibrated closed loop system, a RF power

detection circuitry that consists of a pre-amplifier, a power detector, sample and hold circuit (S/H), and a comparator is necessary. This RF to digital interface first samples the RF power of a bit and holds the converted DC output of the PD. After that, we tune the next control bit, this signal is also converted to DC by the PD. The comparator distinguishes which one if larger and gives logic output to the digital circuits to tune the bit higher or lower.

In LO feedthrough compensation mode, baseband signals are not fed to the mixers so that LO feedthrough signals can be directly detected at the RF output of the mixers. Fig. 3-2(a) plots the simulation results of LO feedthrough of one side of the differential output. An external balun is used to combine the differential output of I/Q mixer since the power detection circuit is single-ended input. Fig. 3-2(b) is the calculation of equivalent output voltage of the balun to 50 Ohm.

In gain imbalance compensation mode, we use baseband test vectors (A,0) and (0,A). The gain imbalance can be suppressed which means the ratio of the output power is minimized by tuning the LO Q buffer. In phase calibration mode, we use baseband vectors (A,A) and (A,-A) and the phase mismatch is minimized by tuning the I buffer. According to my senior's simulation and calculations, the levels of RF output signals during gain and phase calibration are the same. However, the bit difference of gain error is smaller which means phase error can be detected so long as gain error is detected. Fig. 3-3(a) plots the simulation results of gain error and Fig. 3-3(b) is the equivalent output voltage of the balun to 50 Ohm.

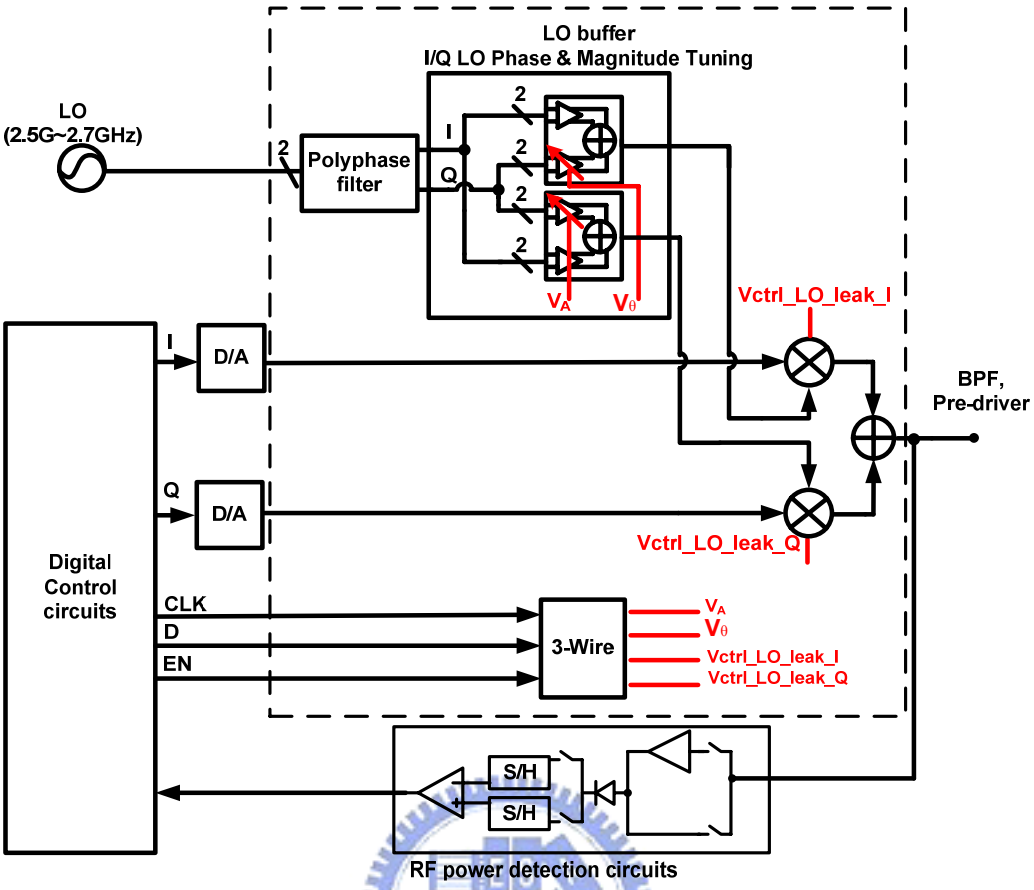
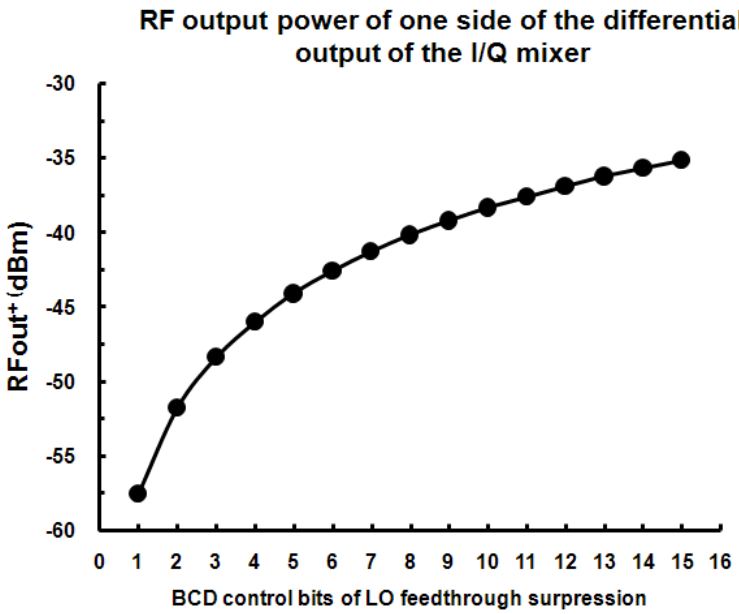
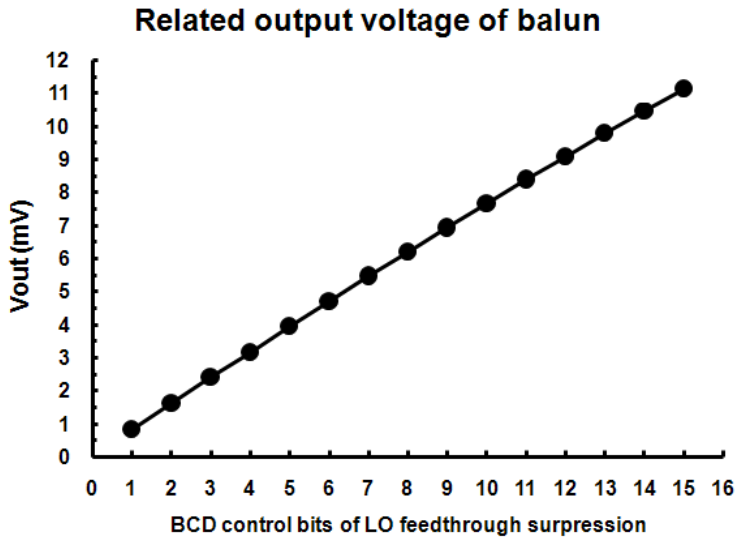


Fig .3-1 Direct up-conversion mixer with auto-calibration for I/Q imbalance and LO feedthrough

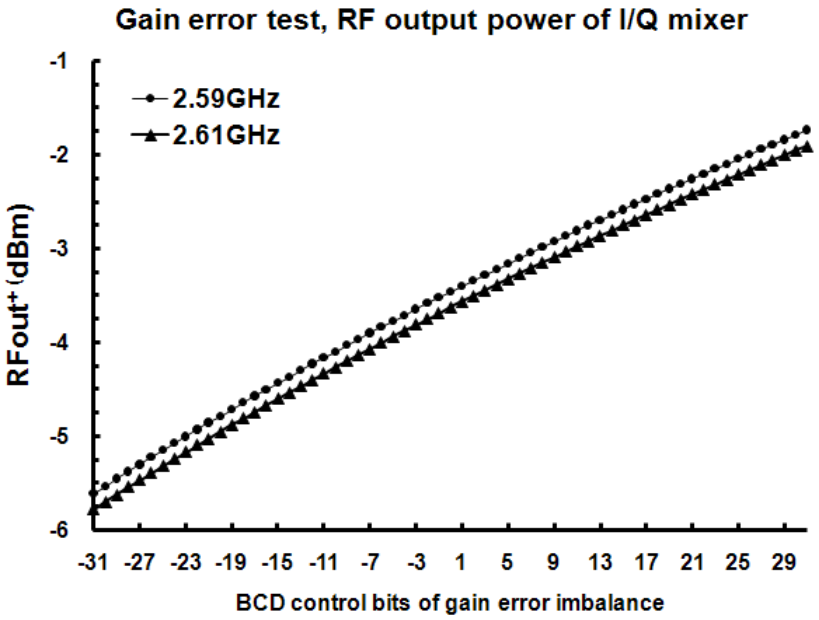


(a)

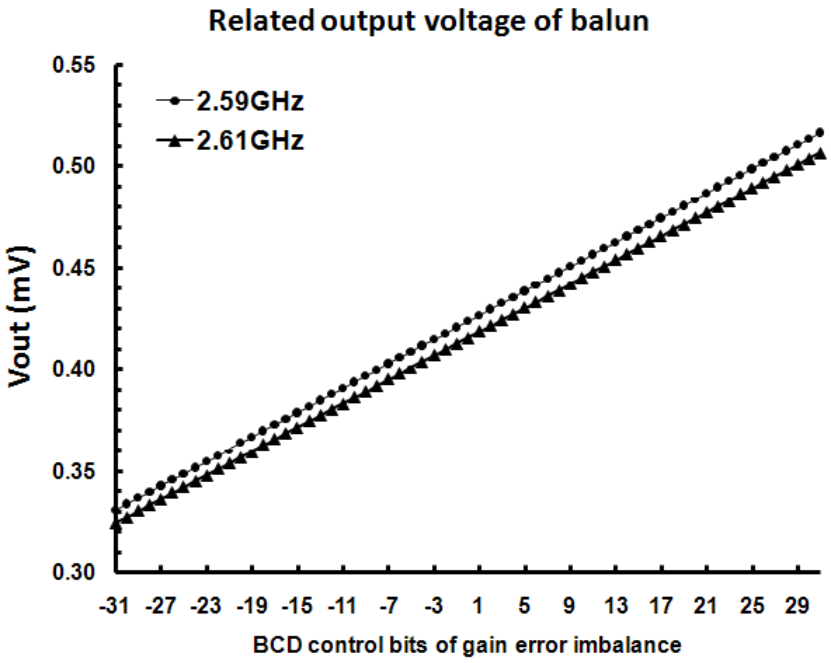


(b)

Fig. 3-2 (a) LO feedthrough of one side of the I/Q mixer's output vs. control bits (b) Related output voltage after balun vs. control bits



(a)



(b)

Fig. 3-3 (a) The RF output signal of I/Q mixer's during gain error test vs. control bits

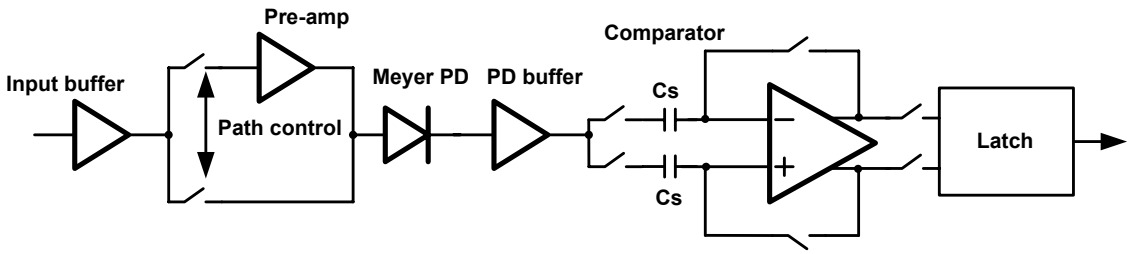
(b) Related output voltage after balun vs. control bits

3.2 RF power detection circuit design

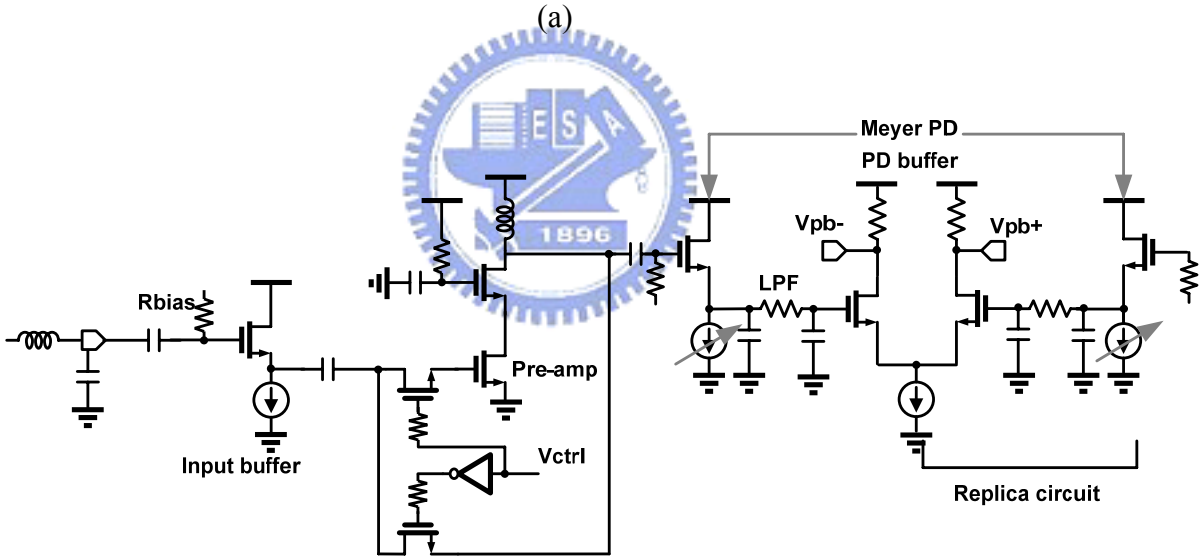
From the previous section, we can know that detection circuit must be capable to detect wide dynamic and small differences RF signals, such as LO feedthrough from 0.84mV to 11.14mV with minimum bit difference of 0.66mV and gain error signal from 321mV to 516mV with minimum bit difference of 2.9mV.

Fig. 3-4(a) and (b) are the architecture and schematic of the RF detection block. In order to have lower losses, a source follower (SF) is employed as an input buffer at the front-end of the detection path. Since only the linear region of a Meyer PD can produces a comparable input for the comparator, small LO signals need to be amplified first. Therefore, the detection path is divided into two: an amplification path for the LO leakage and a bypassing path or the gain/phase error. A simple control switch is used o choose which path is turned on. The Meyer PD then converts the

detected RF signals to a DC level. However, not only the DC output levels but also their differences are too low for the comparator to compare. An additional PD buffer is necessary to amplify the DC signals once again. Besides, it also supports a good isolation between the Meyer PD and the comparator. The following are some descriptions for each circuit building block.



(a)



(b)

Fig. 3-4 (a) RF power detection architecture (b) Schematic of the RF power detection circuits before the comparator

3.2.1 Input buffer

As depicted in Fig. 3-4(b), the source follower is designed to match 50 Ohm taking the parasitic effects of pad and bond wire into account. Hence, measurements

can be made with open loop design or alone. If the size of R_{bias} it too large, the source follower output impedance contains an inductive component. The dependence of this inductive component upon R_{bias} implies that if a source follower is driven by a large resistance, then it exhibits substantial inductive behavior [22]. Here, a small size of 50Ohm is used both for preventing this effect and matching to the input 50Ohm port. Fig. 3-5 is the simulation result of the input impedance of the RF detection circuit. It shows that a smaller than -20dB of input return loss is sufficient.

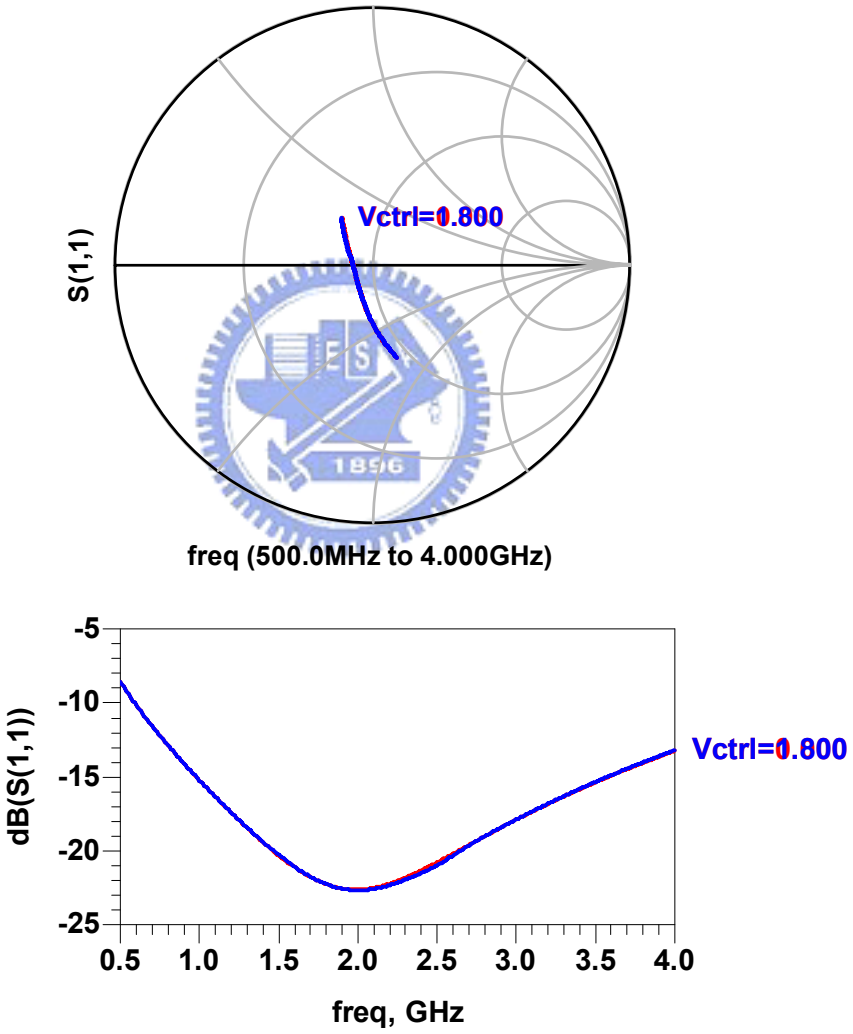


Fig. 3-5 Simulation of input matching

3.2.2 Pre-amplifier

The pre-amplifier uses a simple cascode topology with inductive shunt peaking

to amplify the LO feedthrough signals with 25dB at 2.59~2.61GHz. Fig. 3-6 is the simulation results of the switching path in amplification mode and bypass mode.

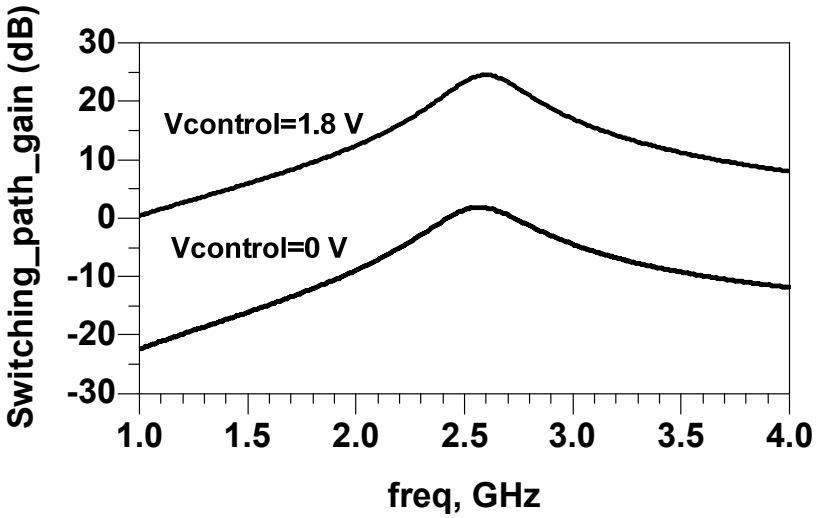


Fig. 3-6 Simulation of the switching path

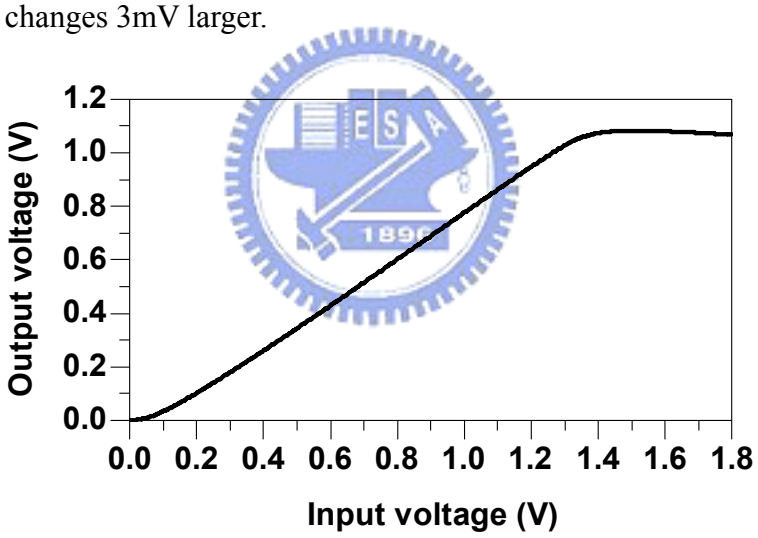
3.2.3 Meyer power detector & PD buffer

As discussed in the previous chapter, there are two regions in the transfer curve of the Meyer PD: square law and linear. If the square law region is used, the output voltage is too small to compare. So it is necessary to add a stage of log amp. In order to reduce the circuit complexities and to save power, we use the linear region instead.

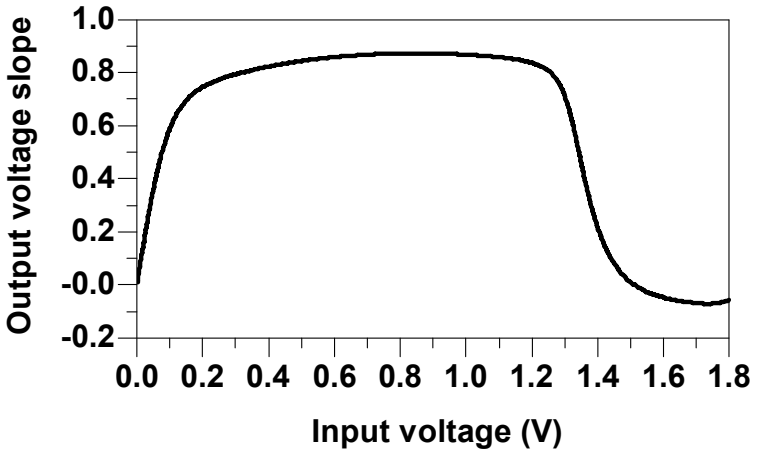
The schematic of the Meyer PD is the same as Fig. 2-2. In order to make the *M1* and M_2's sub-threshold current sources *Ib1* and *Ib2* work at their saturation region properly, the dimensions of M_1 and M_2 are chosen as large as *5um*50/0.18um.* As depicted in Fig. 3-7(a), the transfer curve of a Meyer PD is plotted a little bit different from Fig. 2-2, which x-axis and y-axis are changed to linear voltage, so as to make observations of linear region easier. Fig. 3-7(b) shows the slope of Fig. 3-7(a). As can be seen, the slope of the Meyer PD is below unity. It implies that the output difference of each bit is below the comparable difference. Notice that the comparator's threshold

voltage is assumed conservatively 1.3mV.

A PD buffer, which is a simple differential-pair, is added to solve this problem. As shown in Fig. 3-8(a) the differential pair is designed to have a wide linear input range. Fig. 3-8(b) plots the slope of Fig. 3-8(a) to check how much the bit difference can be amplified. In practical implementations, DC offsets is unpreventable both on the Meyer PD and PD buffer. As indicated in Fig. 3-4(b), the DC offset is compensated by tuning the current sources of the Meyer PD and observing the DC output voltage of the PD buffer. Fig. 3-9 is the combination simulation results of the circuits before the comparator. Fig. 3-9(a) is a 0.84mV, 2.59GHz input signal and changes 0.66mV larger after 2usec. Fig. 3-9(b) shows that the DC output difference of the PD buffer changes 3mV larger.

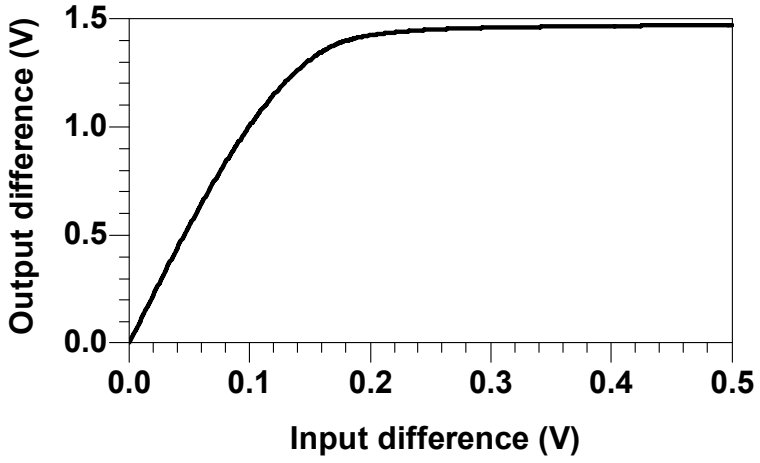


(a)

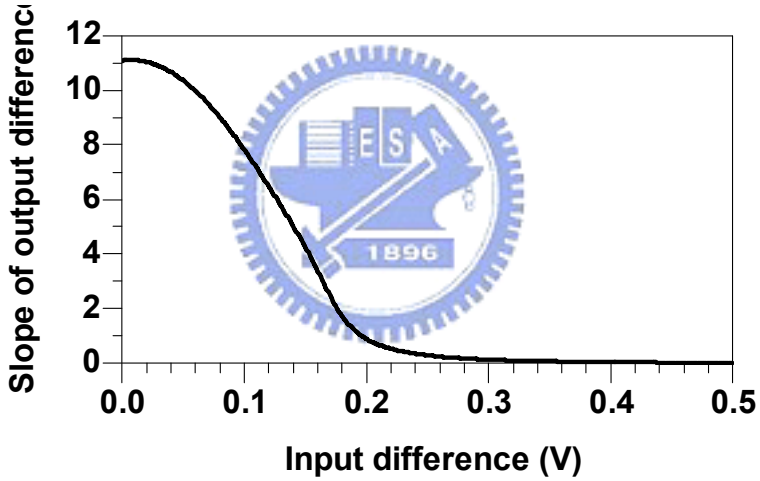


(b)

Fig. 3-7 (a) Meyer PD transfer curve (b) slope of the transfer curve

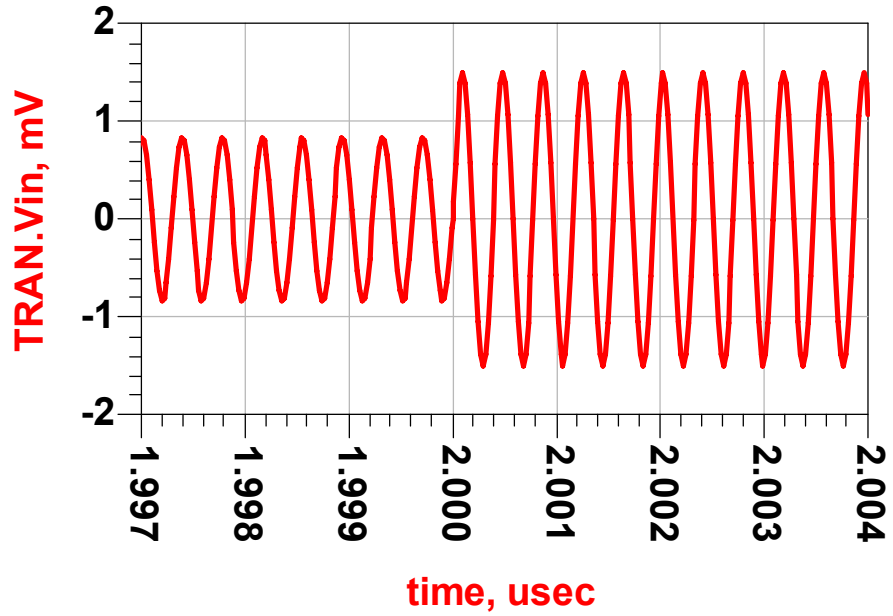


(a)

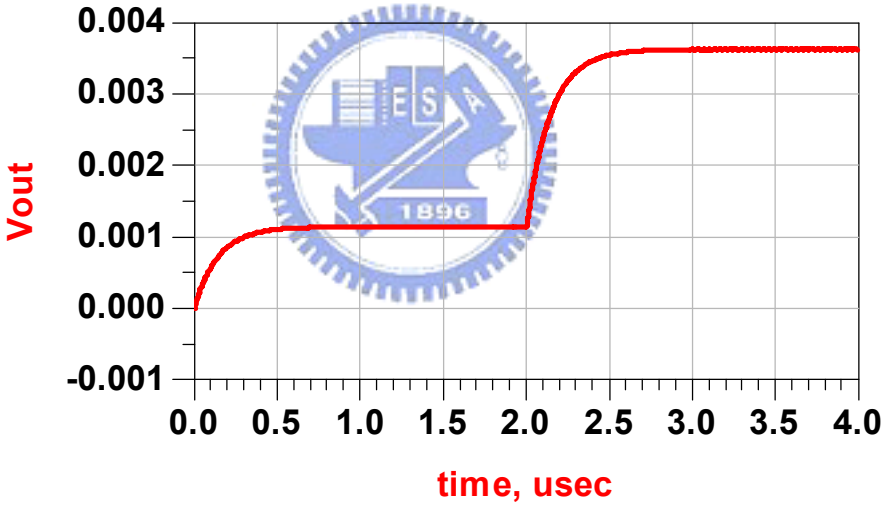


(b)

Fig. 3-8 (a) PD buffer transfer curve (b) slope of the transfer curve



(a)



(b)

Fig. 3-9 Simulation results of the circuits before comparator

3.2.4 Comparator

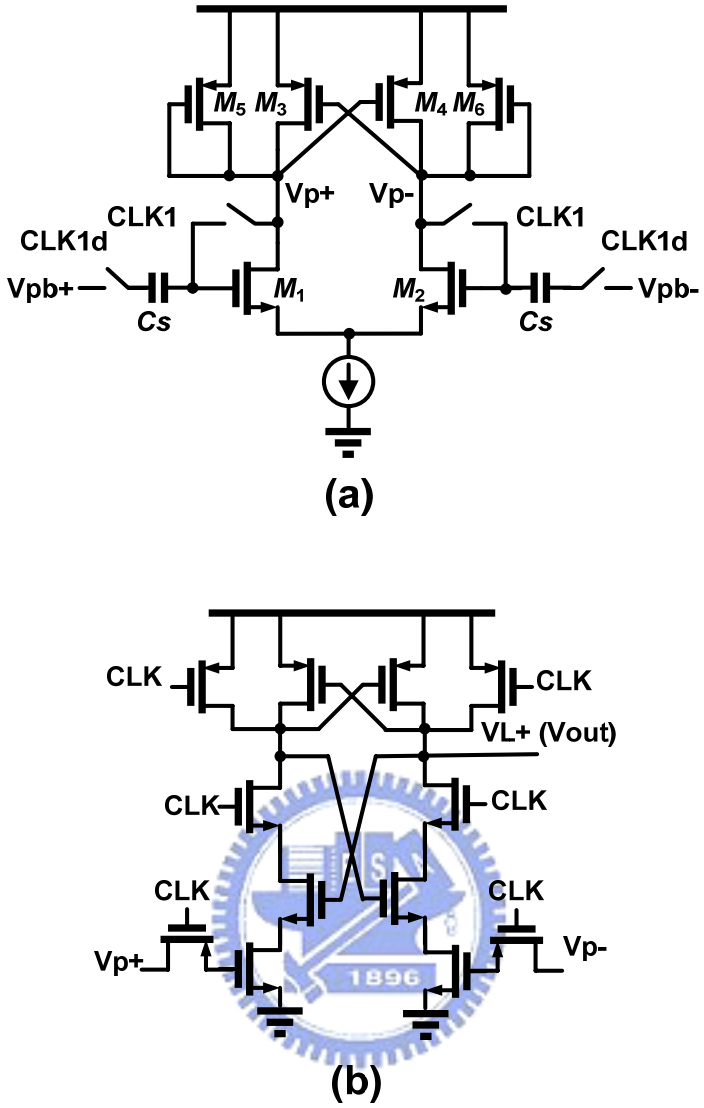


Fig. 3-10 Schematic of comparator (a) Pre-amplifier (b) Latch

Fig. 3-10 is the schematic of the comparator employed in the power detection circuitry. This topology merges S/H and comparator together. In order to prevent kickback noise, the comparator is separated into pre-amp and latch. The differential mode gain of the cross couple load of the pre-amp can be expressed as (3.1). The common mode gain can be expressed as (3.2).

$$A_{DM} = G_{m1,2} \frac{1}{G_{m5,6} - G_{m3,4}} \tag{3.1}$$

$$A_{CM} = \frac{G_{m1,2}}{1+2G_{m1,2}r_O} \cdot \frac{1}{G_{m3,4}+G_{m5,6}} \tag{3.2}$$

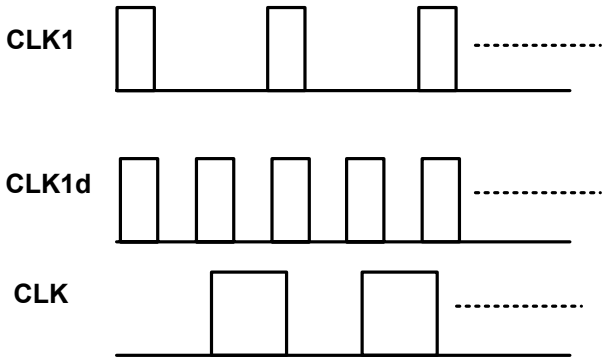


Fig. 3-11 Timing of the comparator

In order to compare the RF power of two control bits, the timing is set as Fig. 3-11.

1. CLK1=”1”, CLK1d=”1”, CLK=”0”:

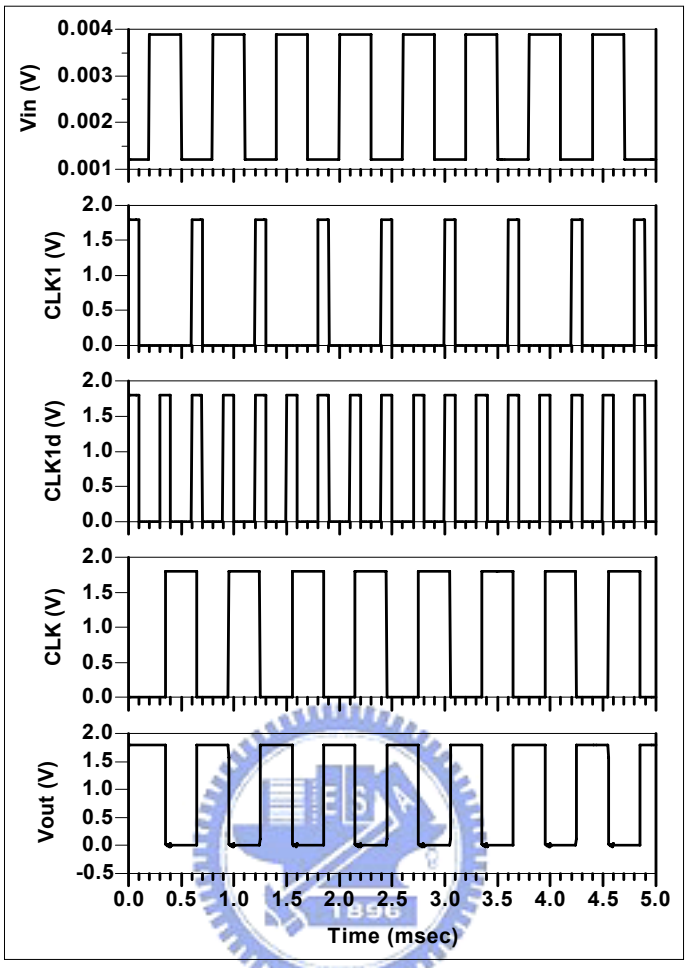
The PD converts the RF output power of the first bit to DC The pre-amplifier acts as a unit gain buffer. Both DC offset and the converted DC output of the first bit, V_{time1} is hold in the sampling capacitor, *Cs* while latch is in the reset mode and outputs “logic 1”.

2. CLK1=”0”, CLK1d=”1”, CLK=”0”:

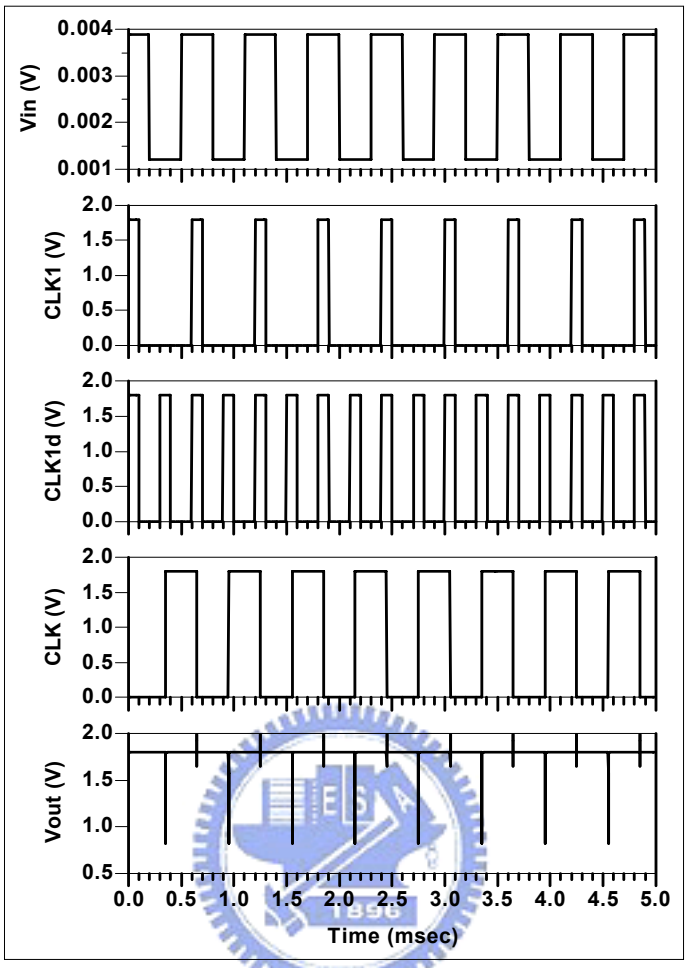
After switching to next compensation bit in the open loop circuits, the PD converts RF output power to a DC voltage, $V_{time2.}$ The pre-amplifier then compares V_{time1} and V_{time2}. DC offset is cancelled. The latch still remains in the reset mode.

3. CLK1=”1”, CLK1d=”1”, CLK=”1”:

The amplified difference of V_{time1} and V_{time2} is past to the latch. The latch pulls it to logic high or low. Fig. 3-12 is the simulation result of the comparator.


Vin (V)
0.004
0.003
0.002
0.001
CLK1 (V)
2.0
1.5
1.0
0.5
0.0
CLK1d (V)
2.0
1.5
1.0
0.5
0.0
CLK (V)
2.0
1.5
1.0
0.5
0.0
Vout (V)
2.0
1.5
1.0
0.5
0.0
-0.5
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0
Time (msec)

(a)



(b)

Fig. 3-12 Simulation results of the comparator

3.3 Simulation results

The simulation results of LO feedthrough compensating modes and gain error compensating mode is shown in Fig. 3-13.

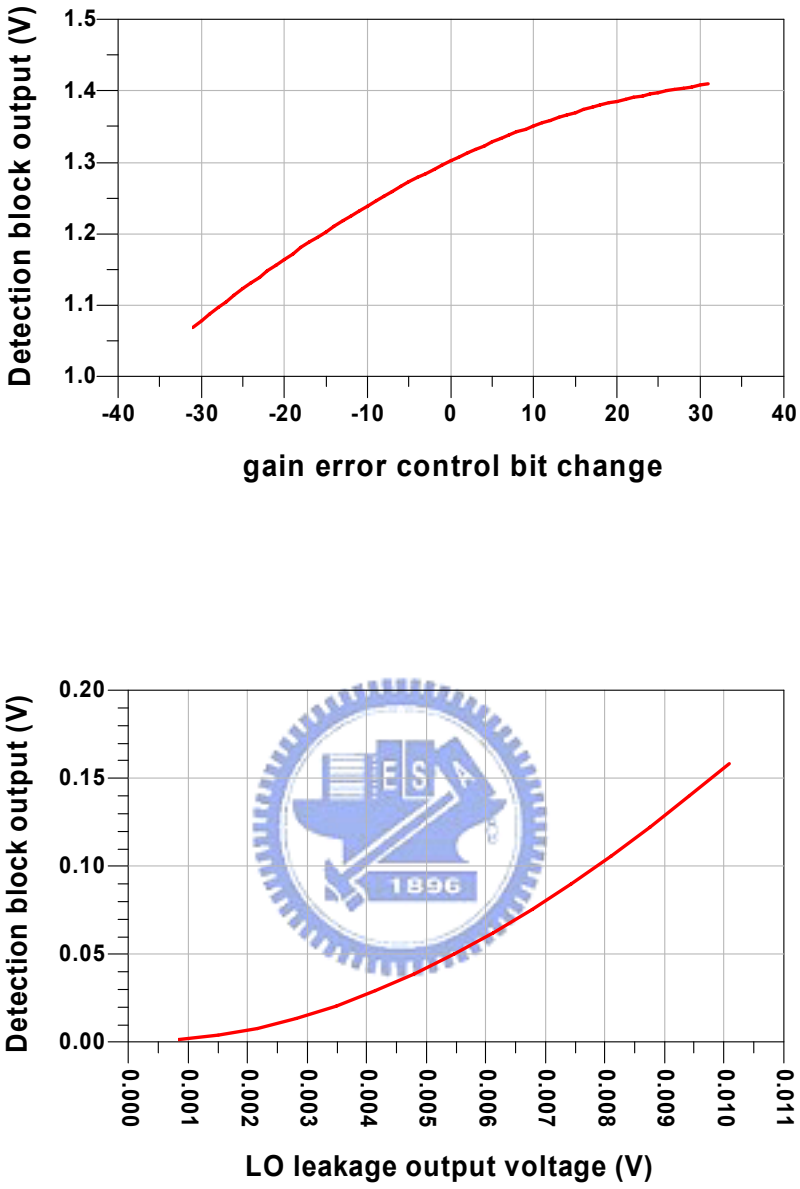


Fig. 3-13 Simulation results of (a) gain error (b) LO feedthrough

3.4 Chip layout & summary

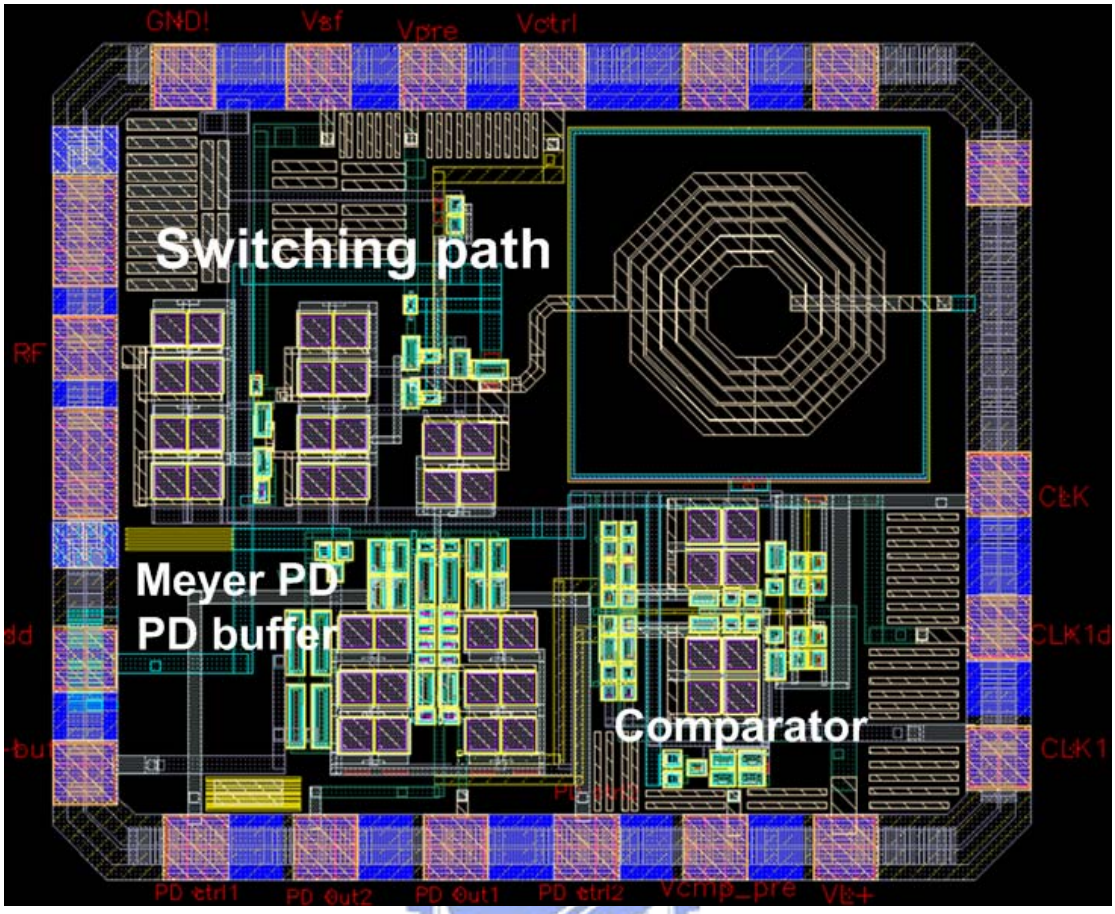


Fig. 3-14 Layout of the RF power detection circuit

Fig. 3-14 is the chip layout in TSMC 0.18m technology. The chip size is mainly limited by the number o pads. Therefore, using large area of RF P-cells for the comparator doesn't matters. The layout area is 1.055X0.9 mm^2.

Unfortunately, the 3-wire control of open loop chip is latched-up and no functional verifications for practical implementations can be made. Hence, the power detection design that is to meet the specifications of that chip has not been fabricated yet. In the future, identifications of the chip failure and re-consider some of the design issues will be made first. After that, we will integrate both designs and complete an auto-calibrated I/Q modulator.

Chapter IV

Built-in self-test circuit designs for 5GHz LNA

4.1 Introduction

With the mature progress in CMOS technology nowadays, integrating more and more functional analog and digital building blocks into a single chip solution is a trend. However, this increases not only the cost but also the complexities of test. Embedded built-in self-test (BIST) on chip seems to be a good solution. In contrast to digital and analog circuits that BIST has been widely utilized, RF BIST circuit designs are still in the early-age development.

The recent proposed BIST architectures can be categorized into loop back test for overall RF transceiver [8] and individual circuit block tests with the aid of embedded power detectors (or RMS detectors) [6]-[10]. The latter testing methods depend on the accuracy of power detector (PD) to measure the absolute input and output power level of the circuit under test (CUT). As such, a logarithmic amplifier (Log amp) is necessary to convert the output level from dB-linear into linear scale [10].

In this chapter we proposed a power comparing method to monitor the status of the CUT. This technique alleviates the loading of the PDs and shifts the accuracy difficulties to a digital step attenuator (DSA). Meanwhile, a low dynamic range PD is sufficient. By using a 3-bit digital control, the goal of monitoring our CUT, a 5GHz low noise amplifier (LNA) can be achieved. Moreover, an invention of the R-72R that deals with the process variations of the most critical block of the BIST circuitry, the DSA, is also introduced in this chapter.

Section 4.2 gives detailed descriptions of RF BIST design with a digital step attenuator. Both simulation results and experimental are also shown in this section. In Section 4.3, a new configuration of R-72R ladder gives a solution to the process variation issue in Section 4.2. Last, a conclusion and summary is given in Section 4.4.

4.2 RF BIST design with a digital step attenuator

4.2.1 The BIST architecture

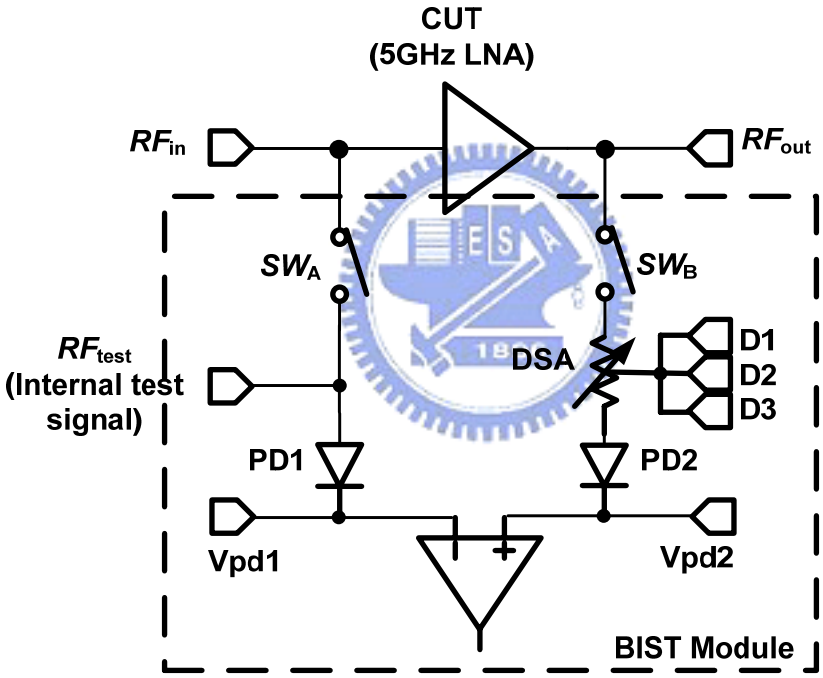


Fig. 4-1 Proposed BIST architecture

Fig. 4-1 is the proposed BIST architecture including a 15.XXdB 5GHz LNA as our CUT and the BIST module. Two PDs are employed to convert RF signals into DC levels. The switch at the left hand side (SW_A) contributes -2dB attenuation. The switch at the right hand side (SW_B) along with a 3 bit 8 level DSA contributes a tunable attenuation from -8dB to -15dB. The overall attenuation of the detection circuit is

therefore -10dB~-17dB. The comparator in the bottom compares the DC levels of *Vpd1* and *Vpd2*. In this work, the comparator has not been integrated in yet. Instead, a DC voltage meter will be used in the measurement to verify the idea.

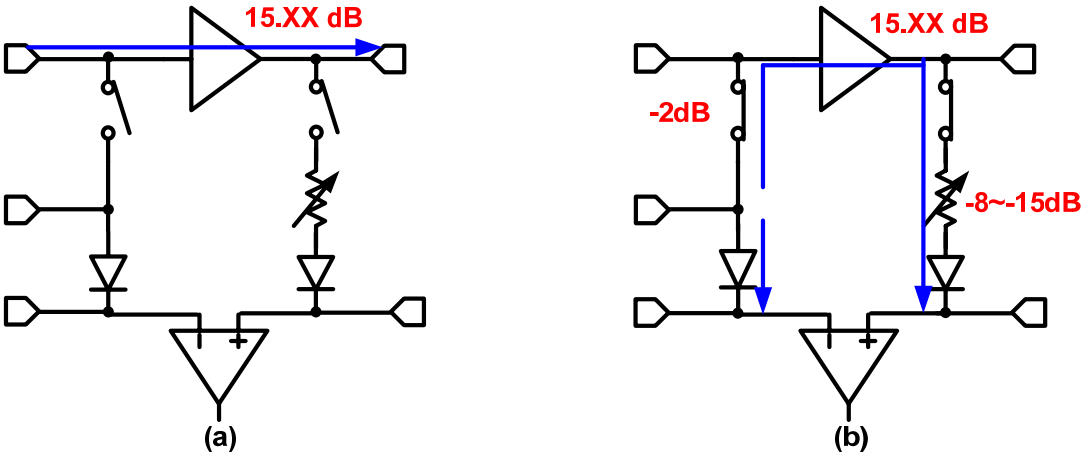


Fig. 4-2 (a) Operating mode (b) Test mode

As shown in Fig. 4-2, the BIST circuit can be switched between two modes:

(a) Operating mode:

As shown in Fig. 4-2(a), we turn off SW_A and SW_B in order to make the LNA operates normally. The RF signal delivers from RF_{in} to RF_{out}. We can use network analyzer and signal generator along with spectrum analyzer to do the LNA measurement as what we always do.

(b) Test mode:

As shown in Fig. 4-2(b), we turn on SW_A and SW_B to connect our CUT with the BIST module and move our input from RF_{in} to RF_{test}. The test RF signals will be generate from the local oscillator (LO) when this architecture is integrated into a transceiver in the future. For verifying the idea, signal generator will be used instead. The test signals will be swept around 5GHz since we cannot know exactly whether the CUT is still peaking at 5GHz or not due to the process variations and all kinds of

design uncertainties. The test power level cannot be too high a level due to the linearity of the CUT and cannot be set too low that will generate a too low DC level from the PD. Thus, I fixed it at an appropriate value of -25dBm.

As indicated in Fig. 4-2(b), there are two paths for the 5GHz test signal. It travels downwards to let PD1 convert it into a DC level *Vpd1*. It travels upwards through SW_A, CUT (LNA), SW_B, DSA, and finally PD2 convert it to another DC level *Vpd2*. We can tune the 3 control bits of the DSA with 1dB/step.

Initially, we start from the control bit *000* which is a lowest attenuation level and *Vpd2* will be greater than *Vpd1*. The comparator will give us a "*logic 1*" output. By tuning controls bits, the attenuation level increases 1dB higher per bit that eventually makes *Vpd2* larger than *Vpd1*. The comparator output will then switch from "*logic 1*" to "*logic 0*". At this certain bit, the gain of the CUT can be known by us. In this work, the CUT is designed with the gain of 15~16dB in the TT corner. From Table.1 below, we can know that when we switch from *101* to *110*, *Vpd (=Vpd2-Vpd1)* will switch from positive to negative ideally.

Table 1 Attenuation levels

	Control bit	Attenuation (dB)
0	000	-10
1	001	-11
2	010	-12
3	011	-13
4	100	-14
5	**101**	**-15**
6	**110**	**-16**
7	111	-17

In this version the comparator is not integrated in the BIST module yet.

Neglecting the threshold voltage of the comparator, we postulate that *Vpd=Vpd2-Vpd1>0*, gives "logic 1" and *Vpd=Vpd2-Vpd1≦0*, gives "logic 0" for simplicity. The following sections are the circuit building blocks in Fig. 4-1.

4.2.2 Low noise amplifier

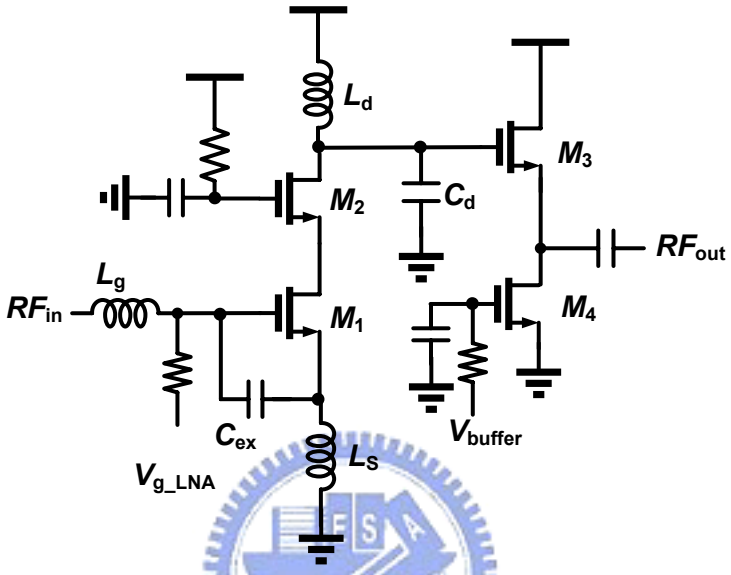


Fig. 4-3 Circuit under test: a 5GHz low noise amplifier

Fig. 4-3 is the CUT that uses a conventional cascode LNA topology [21]. *Ls*, *Lg*, and *Cex* give us the simultaneous input impedance and noise matching. The transistor *M2* is adopted for excellent reverse isolation and the output *LC*-tank composed of L_d and C_d make the *S21* peak at 5GHz. For measurement considerations, a source follower, consists of *M3 and M4*, is added to match the output port to 50 Ohm.

4.2.3 Switch A (SW_A)

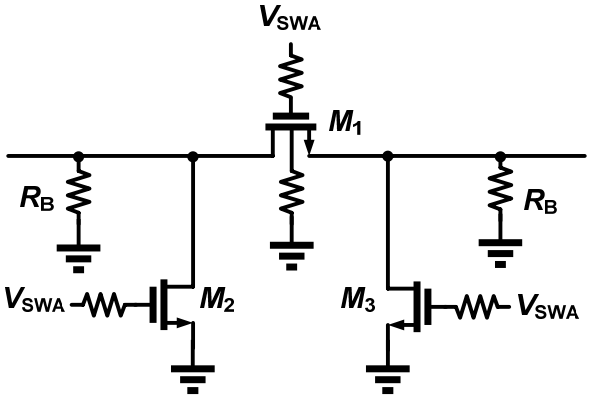


Fig. 4-4 Switch A

Depicted in Fig. 4-4, an π attenuator that has -2dB attenuation is adopted for SW_A for the sake of matching the CUT with the test port. The linearity issue of the attenuator can be ignored since the test signal is as low as -25dBm. Therefore, resistors of an π attenuator can all be replaced by MOSFETs as switches. A large HRI resistor of several Kilo-Ohms is connected from the bulk of *M1* to ground for the purpose of minimizing the parasitic effects. Furthermore, two large resistors R_B are connected to from source and drain to ground to prevent DC level uncertainties.

4.2.4 Power detector (PD)

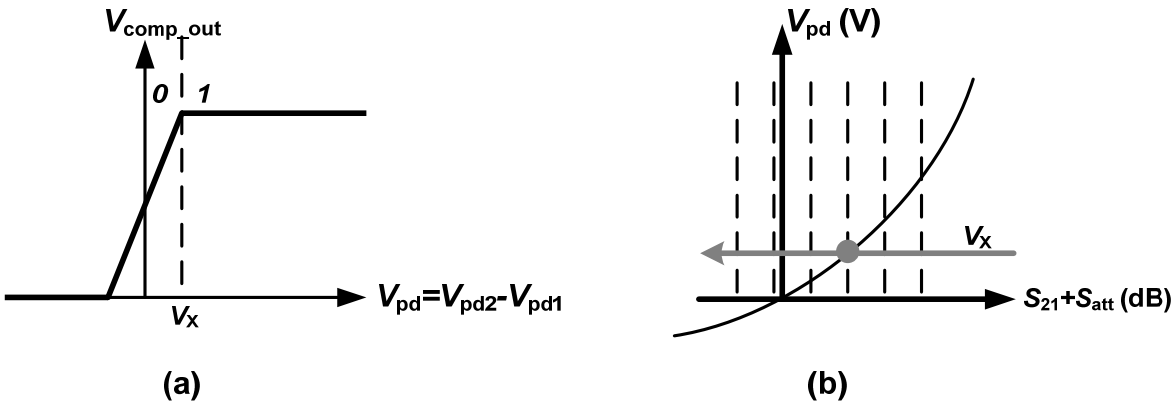


Fig. 4-5 (a) Threshold voltage of the comparator (b) PD characteristic curve

In this BIST architecture, the power detectors are not only to convert RF signals into DC voltages but also need generate a comparable voltage difference for the comparator. In Fig. 4-5(a), we can define the threshold voltage of the comparator as *Vx*. The comparator outputs a "*logic 0*" if the input is below it. For the following analysis, we simply model the transfer function of a power detector as:

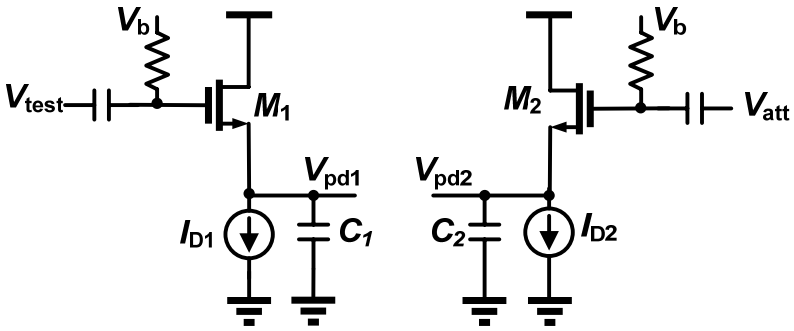
$$V_{pd} = KV_{in}^{2} \tag{4.1}$$

where K is a constant representing the PD characteristic.

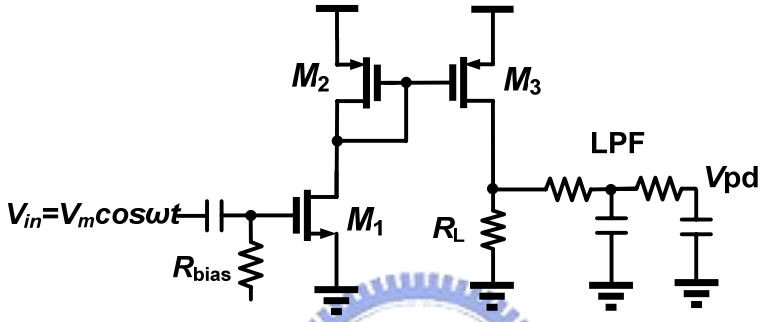
The input of the comparator which is the output difference of the PDs can be expressed as:

$$\begin{aligned} V_{pd} &= V_{pd2} - V_{pd1} \\ &= KA_{LNA}^{2} A_{att}^{2} V_{test}^{2} - KV_{test}^{2} \\ &= KV_{test}^{2}(A^2 - 1) \\ &= KV_{test}^{2}(10^{\frac{S_{21}+S_{att}}{10}} - 1) \end{aligned} \tag{4.2}$$

where A_{LNA} is the voltage gain of the LNA, A_{ATT} is the voltage attenuation of the attenuator, and V_{test} is the test voltage. We also assume perfect matching to 50Ohm between inter stages. The design parameters will then be simplified to K and V_{test} by (4.2). We can know that the larger the K the more relaxed for the comparator. Employing the Meyer PD in Section 2.2 is the first thought came to mind. However, the following analysis tells us that Meyer PD has its own limitations in this application.



(a)



(b)

Fig. 4-6 (a) Meyer power detector (b) Current amplifier power detector

A bit different from Fig. 2-1, the Meyer PD in Fig. 4-6(a) has input signals on both transistors, *M1* and *M2*.

Using the results of (2.3), the DC current of *M1* can be re-written as:

$$\begin{aligned} I_{D1} &= I_{D0}\frac{W}{L}\exp[\frac{V_{GS1}-V_{THN}}{nV_T}]*[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{test}^{\ 2}}{2}+\frac{1}{4!}(\frac{1}{nV_T})^4\frac{3V_{test}^{\ 4}}{8}+...] \\ &\approx I_{D0}\frac{W}{L}\exp[\frac{V_{GS1}-V_{THN}}{nV_T}]*[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{test}^{\ 2}}{2}] \end{aligned} \tag{4.3}$$

Similarly,

$$I_{D2} \approx I_{D0}\frac{W}{L}\exp[\frac{V_{GS2}-V_{THN}}{nV_T}]*[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{att}^{\ 2}}{2}] \tag{4.4}$$

Since identical current sources are used:

$$I_{D1} = I_{D2}$$

$$\Rightarrow I_{D0}\frac{W}{L}\exp[\frac{V_{GS1}-V_{THN}}{nV_T}]*[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{test}{}^2}{2}] = I_{D0}\frac{W}{L}\exp[\frac{V_{GS2}-V_{THN}}{nV_T}]*[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{att}{}^2}{2}]$$

$$\Rightarrow \exp[\frac{V_{GS1}-V_{GS2}}{nV_T}] = \frac{[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{att}{}^2}{2}]}{[1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{test}{}^2}{2}]}$$

$$\Rightarrow V_{GS1}-V_{GS2} = nV_T*[\ln(1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{att}{}^2}{2}) - \ln(1+\frac{1}{2!}(\frac{1}{nV_T})^2\frac{V_{test}{}^2}{2})]$$

(4.5)

By means of the Maclaurin Series below,

$$\ln(1+x) = x - \frac{x^2}{2} + \frac{x^3}{3} - \frac{x^4}{4} + \ldots + (-1)^n\frac{x^{n+1}}{n+1} + \ldots \quad (-1<x\le 1)$$

(4.6)

(4.5) can be approximated as:

$$V_{GS1}-V_{GS2} = \frac{1}{4nV_T}(V_{att}{}^2 - V_{test}{}^2)$$

(4.7)

So finally, with (4.7) V_{pd} can be expressed as:

$$V_{pd} = V_{pd2} - V_{pd1} = (V_b - V_{GS2}) - (V_b - V_{GS1}) = V_{GS1} - V_{GS2} = \frac{1}{4nV_T}(V_{att}{}^2 - V_{test}{}^2)$$

(4.8)

We can know from (4.7) that $K = \frac{1}{4nV_T}$ and this value is too low.

Depicted in Fig. 4-6(b), the topology of current amplifier PD [3] is adopted to overcome the design difficulties due to small *K* of Meyer PD. The concept of nonlinearities of a transistor is much similar to Meyer PD if we bias *M1* at its sub-threshold region. *M2* and *M3* compose a current mirror and amplify the sub-threshold current generated from *M1* by their ratio. R_L then converts this current into voltage. Last, two stages of low pass filter are added to filter out the high

frequencies and just to keep their DC levels.

We can express the descriptions above all in one equation:

$$V_{pd} = I_{D0}(W/L)_1 \frac{(W/L)_3}{(W/L)_2} R_L * \exp(\frac{V_{GS1}}{nV_T}) * (1 + \frac{V_m^2}{4n^2V_T^2}) \tag{4.9}$$

Therefore, the difference of the PDs' output can be derived as follow:

$$V_{pd1} = I_{D0}(W/L)_1 \frac{(W/L)_3}{(W/L)_2} R_L * \exp(\frac{V_{GS}}{nV_T}) * (1 + \frac{V_{RFtest}^2}{4n^2V_T^2})$$

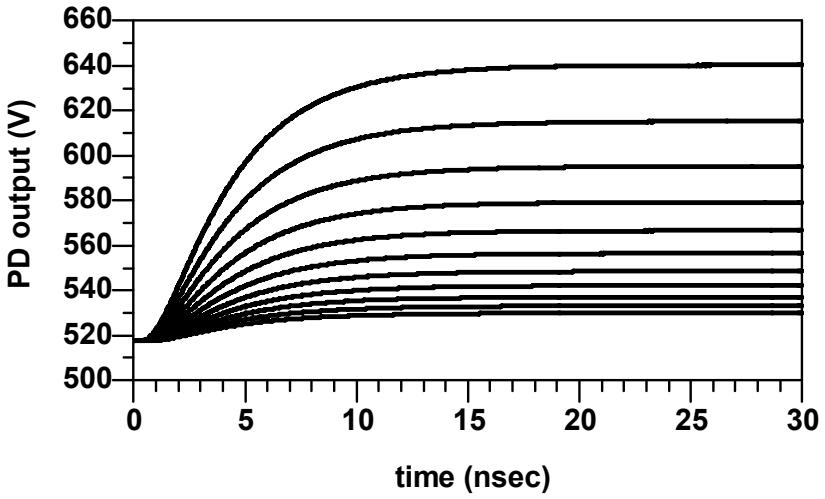
$$V_{pd2} = I_{D0}(W/L)_1 \frac{(W/L)_3}{(W/L)_2} R_L * \exp(\frac{V_{GS}}{nV_T}) * (1 + \frac{V_{DSAout}^2}{4n^2V_T^2})$$

$$V_{pd} = V_{pd2} - V_{pd1} = I_{D0}(W/L)_1 \frac{(W/L)_3}{(W/L)_2} R_L * \exp(\frac{V_{GS}}{nV_T}) \frac{1}{4n^2V_T^2} (V_{DSAout}^2 - V_{in}^2) \tag{4.10}$$

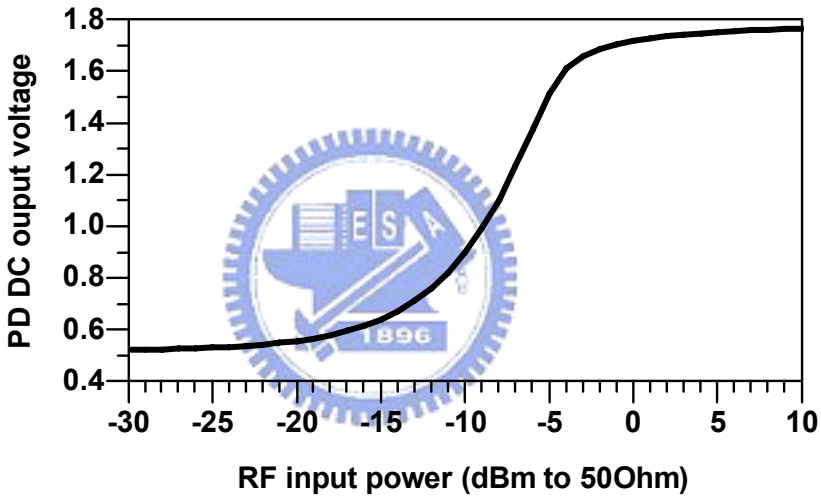
Obviously, the *K* for current amp PD can be designed suitable in this application.

Notice that the path in test mode is designed in power domain which is a 50Ohm-environment in order to make the detected voltage closed to the power gain (S_{21}). The bias resistor, R_{bias}, of *PD2* is set to a value near 50Ohm. Since SW_A is already has input impedance matched to 50Ohm, we only need a large R_{bias} for PD1 to minimize the loading effects.

Fig. 4-7 is the simulation results of a current amp PD designed in TSMC 0.18um technology. We can see from Fig. 4-7(a) that the output of the PD rises from its initial DC bias point (517.5mV) when there is a RF signal input. The output reaches its steady state around 25ns. Fig. 4-7(b) is result of the harmonic balance simulation. The input power is swept from -30dBm to 10dBm. The simulation results show that the output difference of -25dBm and -24dBm input is around 3mV which is sufficient for the comparator.



(a)



(b)

Fig. 4-7 (a) Time response with different input levels (b) DC output voltage vs. input power

4.2.5 Digital step attenuator (DSA)

Fig. 4-8 (a) shows the configuration of the DSA. By switching between the two attenuation levels of the attenuation cell a -8~-15dB with -1dB/step can be achieved. Fig. 4-8 (b) is the attenuation cell used. Here I called it a "complementary π attenuator". Matching closed to 50 Ohm while switching between

the two attenuation levels is a merit. Besides this, the signal at the output of the LNA is larger and causes linearity to be an issue. Resistive network, however, has high linearity that will be suitable here. Here, inverter is used to give us *D1* and *D1b*. For larger attenuation levels, we can turn on *D1* and turn off *D1b* to make the series resistance larger and shunt resistance smaller and vice versa for smaller attenuation levels.

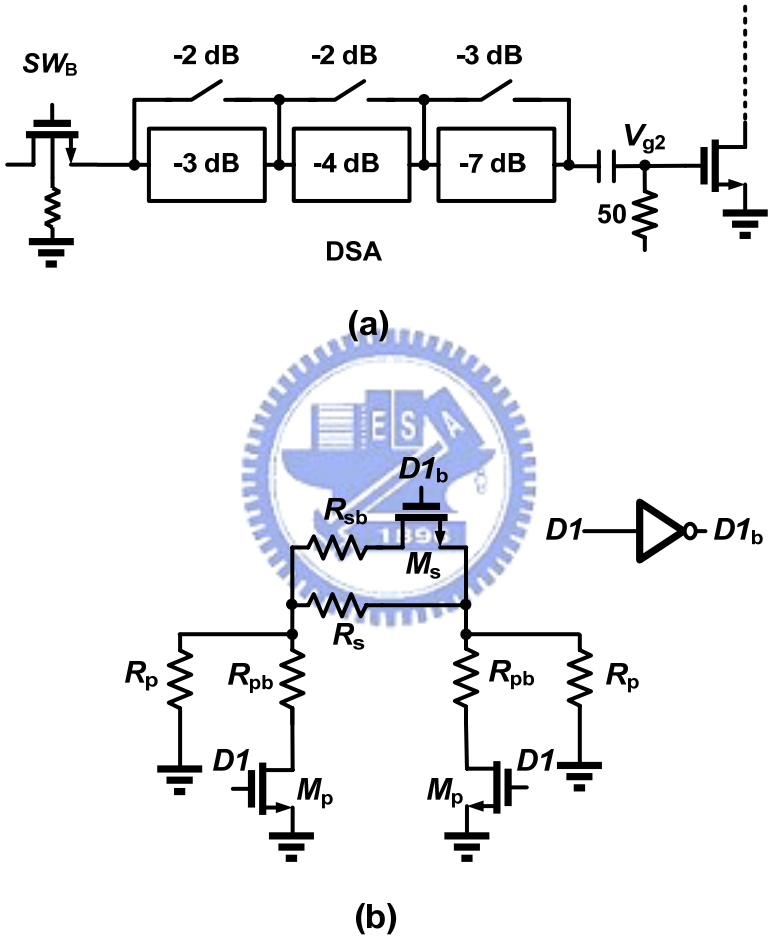


Fig. 4-8 (a) Digital step attenuator (b) attenuation cell

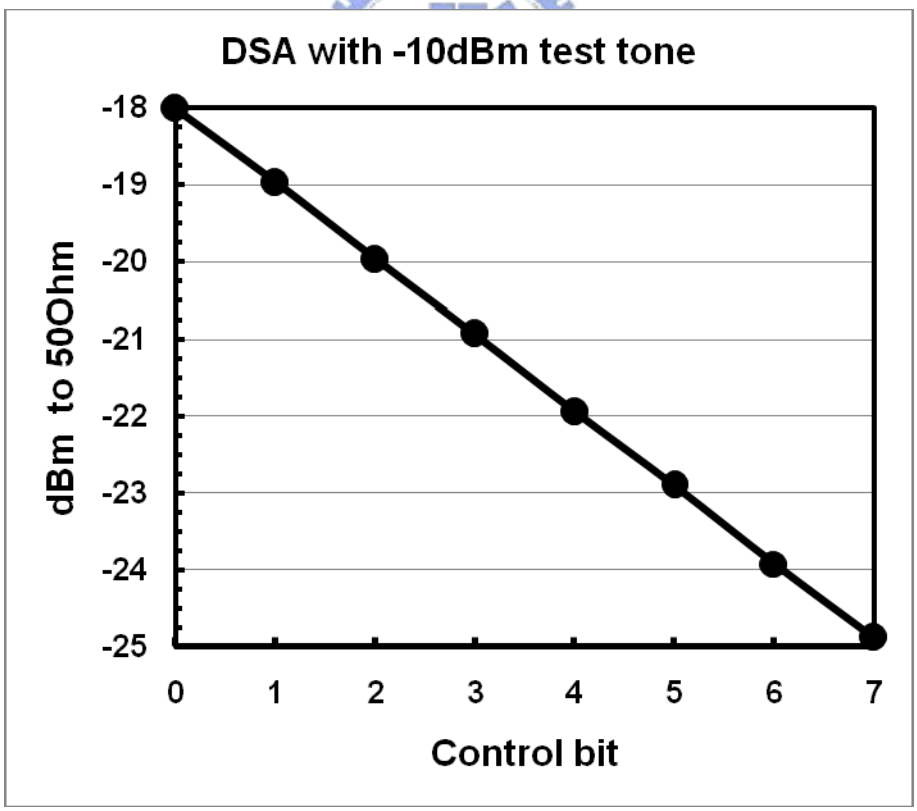
In order to make the power gain equal to the voltage gain, the DSA is designed to make the input impedances closed to 50Ohm (or *S11*<*-20dB*). Besides, a very linear 1dB-attenuation is necessary simultaneously at each step. Besides the lowest attenuation level -7dB of the DSA itself, an additional 1dB loss is contributed from

SW2 and the AC couple capacitor between the DSA output and the gate of PD's M1 to make the lowest attenuation of this path -8dB.

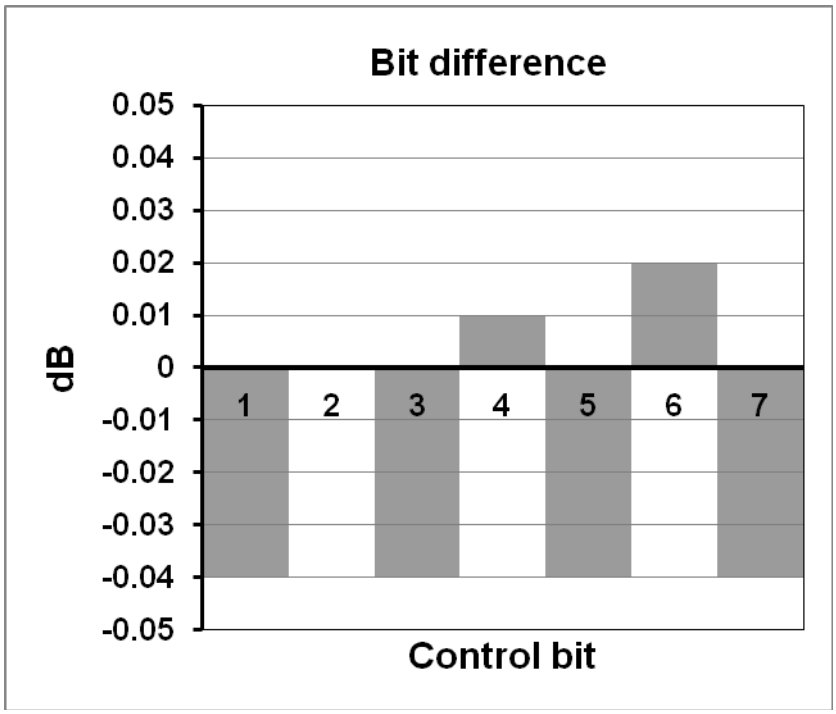
Fig. 4-9 are some simulation results of Fig. 4-8 (a) using a -10dBm which has 50Ohm source resistance 5GHz input test tone. Fig. 4-9(a) shows the power level at V_{g2} referring to 50Ohm. If we view the DSA as a DAC, the bit difference or DNL can be simply define as:

$$Bit\ difference(i) = \frac{output\ power(i) - output\ power(i-1)}{1\ dB}\ \text{(LSB)} \tag{4.11}$$

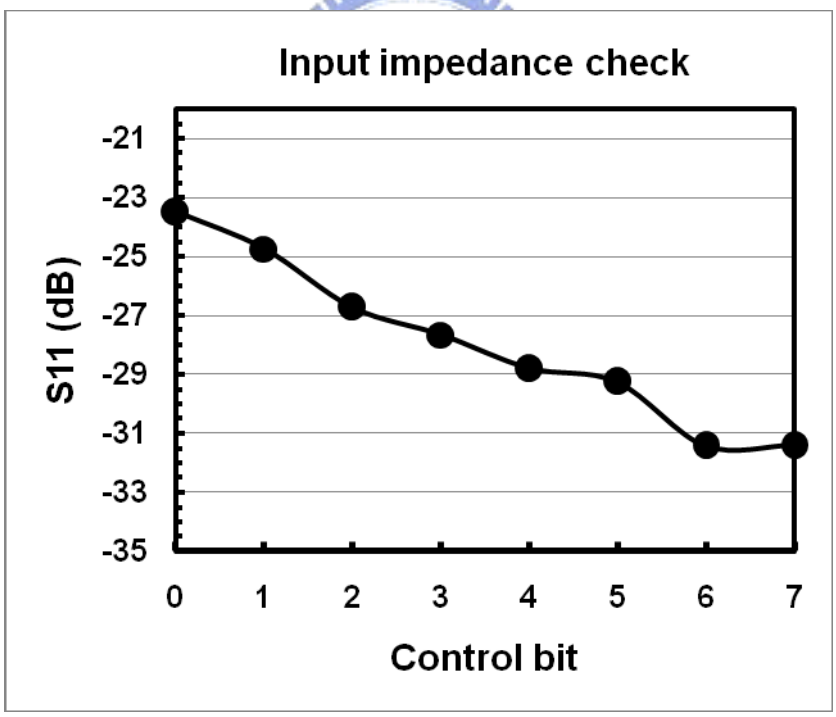
where LSB equals to 1dB. Fig. 4-9(b) is a plot of bit difference after calculations. Fig. 4-9(c) plots the variations of input impedance.



(a)



(b)



(c)

Fig. 4-9 (a) Output power of the DSA with -10dBm test tone (b) Bit difference (c) Input impedance check

4.2.6 Design guidelines of the DSA

One may wonder how the DSA is designed so perfectly as the Fig. 4-9. No doubt a beginner may spend hours and hours, days and days on trimming owing to the non-idealities of the component values, such as parasitic effects and turn on/off resistance of the MOS. Here, we came up to some design guidelines not great as a theory but just to let us never become an "ADS tuning monkey!" The following steps are the designer's "know how." Belief it or not, rapid and efficient design can be made by following them.

Step I: One can first calculate the ideal values of *Rs, Rsb, Rp,* and *Rpb* in Fig. 4-8(b). Construct an ideal attenuation cell with the calculated resistor values, an ideal switch, and an inverter. Double check the attenuation levels (or S_{21}) of the two modes and the input impedance Z_{in}. Make sure that one designs one attenuation cell at a time. Please don't haste to combine the attenuation cells altogether at the very beginning or you might in big trouble.

Step II: Change the ideal series switch to *Ms* and sweep the dimension of it. Take a glance at both S_{21} and Z_{in}. One can notice that larger dimensions of *Ms* result in a more ideal $S_{21.}$ However, this causes the real part of Z_{in} to shrink more than smaller dimensions. One may stupidly want to make the *Rsb* smaller, since it is series with an on resistance of *Ms.* However, the results are even worse. The smaller the *Rsb*, the more Z_{in} shrinks

Step III: Sweep the size of *Rp* instead. One may notice that by making the size few tens Ohms larger than the calculated value, the results will be closer to the ideal value. Besides, Z_{in} doesn't shrink anymore. We can conclude shortly that the series branch of an attenuation cell is the most sensitive part. Don't ever try to change it.

Step IV: Change the ideal parallel switch to *Mp*. Larger dimension size results in a smaller on resistance and a bigger off capacitance that makes *"000"* the smallest Z_{in} when combing the attenuation cells together. As *Rs, Rsb, and Rp* are fixed already from Steps I~III, *Rpb* is the only degree of freedom left. Chance of fixing the attenuation cell closer to ideal is to make *Mp* smaller and *Rpb* bigger.

Step V: Since the estimated values is given from steps above, change the resistors to practical ones, such as HRI, RP-poly, etc. A little bit of fine tuning the component size afterwards is necessary since there are still some parasitic effects of the practical resistors.

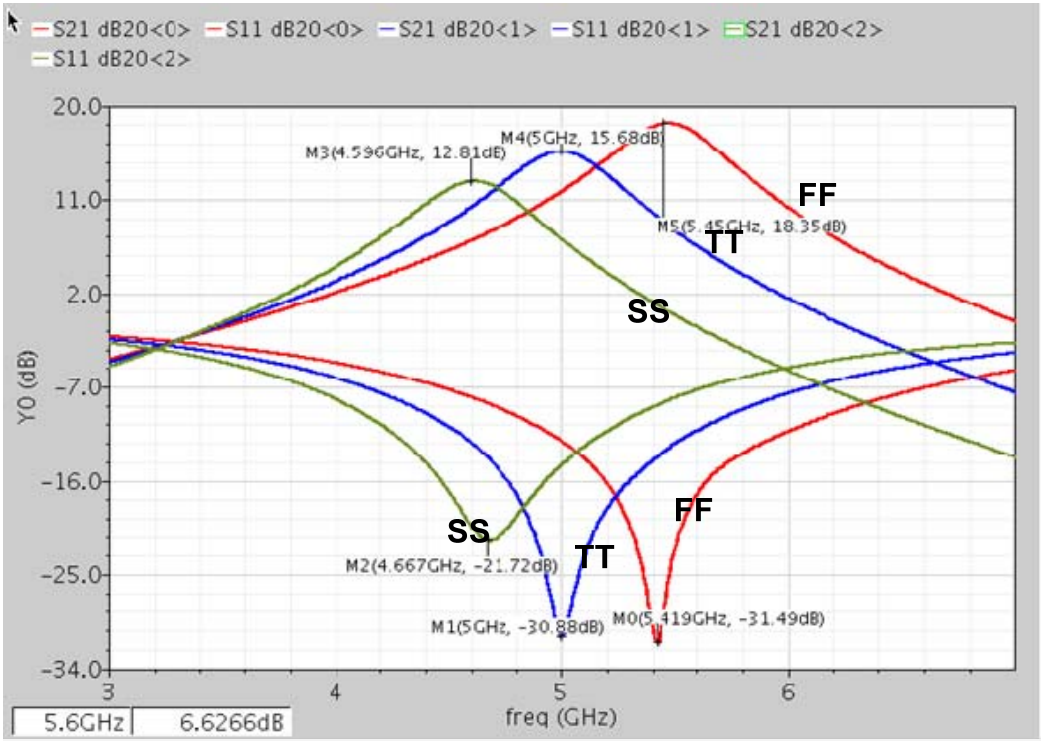
Step VI: Finally, do the same steps to design each attenuation cell and combine them together.

A point to mention is that attenuation cells are easier to design if the difference of the two desired attenuation levels is not so high since Z_{in} won't be switched so severely.

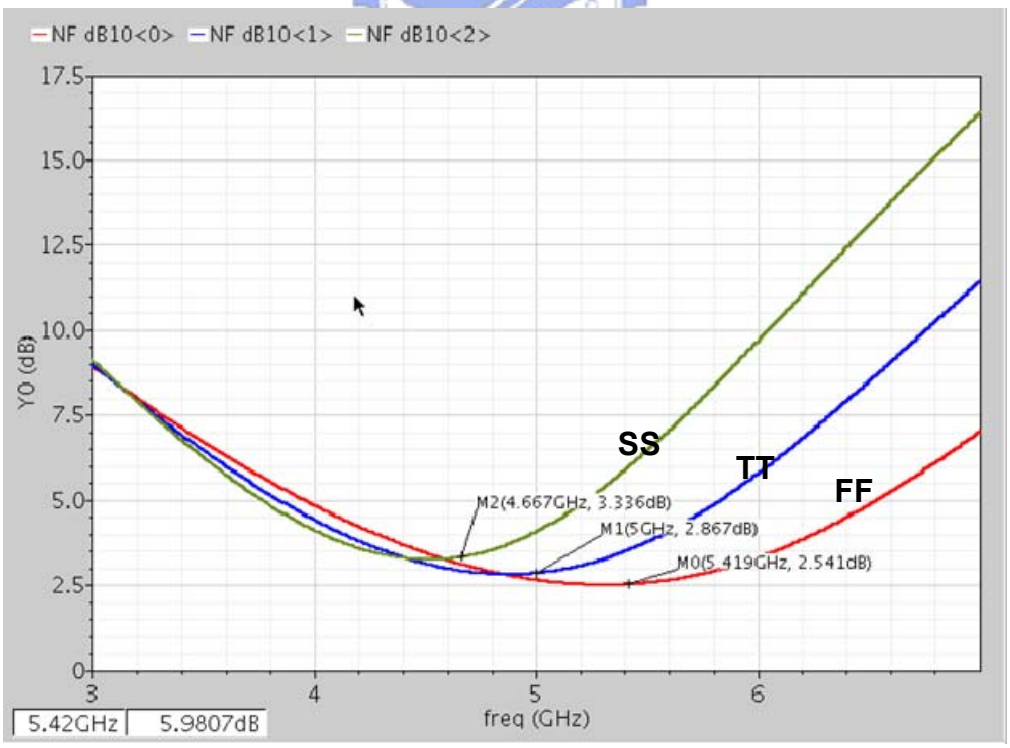
4.2.7 Post-simulation results

Fig. 4-10 is the results of the operating mode using Cadence Spectre RF and Ansoft Designer for post layout EM simulation. I organized these data in Table 2 that can give us the reference information for the test mode.

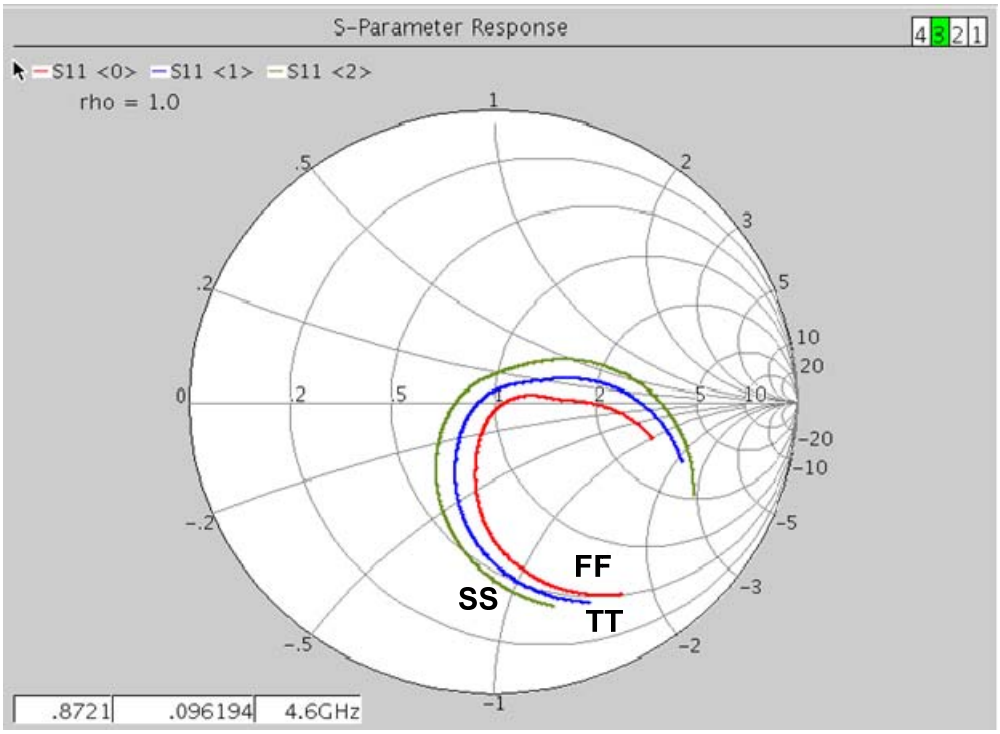
(a) Operating mode


S21 dB20<0>
S11 dB20<0>
S21 dB20<1>
S11 dB20<1>
S21 dB20<2>
S11 dB20<2>
M3(4.596GHz, 12.81dB)
M4(5GHz, 15.68dB)
M5(5.45GHz, 18.35dB)
FF
TT
SS
SS
FF
TT
M2(4.667GHz, -21.72dB)
M1(5GHz, -30.88dB)
M0(5.419GHz, -31.49dB)
YO (dB)
freq (GHz)
5.6GHz
6.6266dB

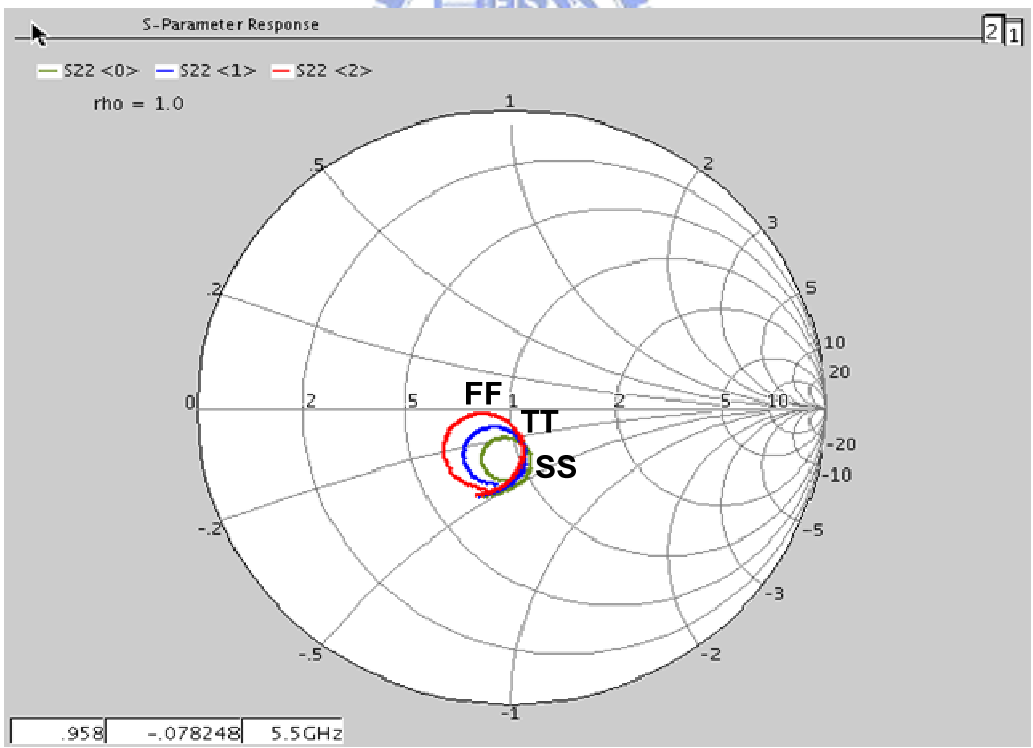
(a)


NF dB10<0>
NF dB10<1>
NF dB10<2>
SS
TT
FF
M2(4.667GHz, 3.336dB)
M1(5GHz, 2.867dB)
M0(5.419GHz, 2.541dB)
YO (dB)
freq (GHz)
5.42GHz
5.9807dB

(b)



(c)



(d)

Fig. 4-10 Post simulation results of the CUT (a) S11 &S21 (b) Noise figure (c) S11

Smith Chart (d) S22 Smith Chart

Table 2 Performance summary of the CUT in operating mode

Corner case	TT	SS	FF
S21 peak	**15.68 dB @5GHz**	**12.81 dB @4.60GHz**	**18.35 dB @5.45GHz**
S11 dip	-30.88 dB @5GHz	-21.72dB @4.67GHz	-31.49dB @5.419dB
S22 dip	-22.20 dB @5GHz	-19.45dB @4.58GHz	-26.81dB@5.51dB
Noise figure	2.867 dB @5GHz	3.33dB @4.67GHz	2.541dB @5.42dB

(b) Test mode

According to Table 1&2, the zero crossing point of V_{pd} $(V_{pd2}$-$V_{pd1})$ should occurs at 101 to 110 for TT corner case, 010 to 011 for SS ideally. Since the gain of the FF corner is out of range, we just consider the quantity is larger than 17dB. The simulation result is plotted in Fig. 4-11. Since the BIST module is designed in TT corner case, its function is correct. However, the zero crossing occurs at 011 to 100 or SS corner which is a bit next to the ideal. This is somewhat tricky. In order to obtain a correct BIST function, an invariable circuit is to test a variable circuit (CUT). However, we forgot that that the BIST circuitry also varies with process and temperature variations during design. This issue will be discussed further in Section 4.3.

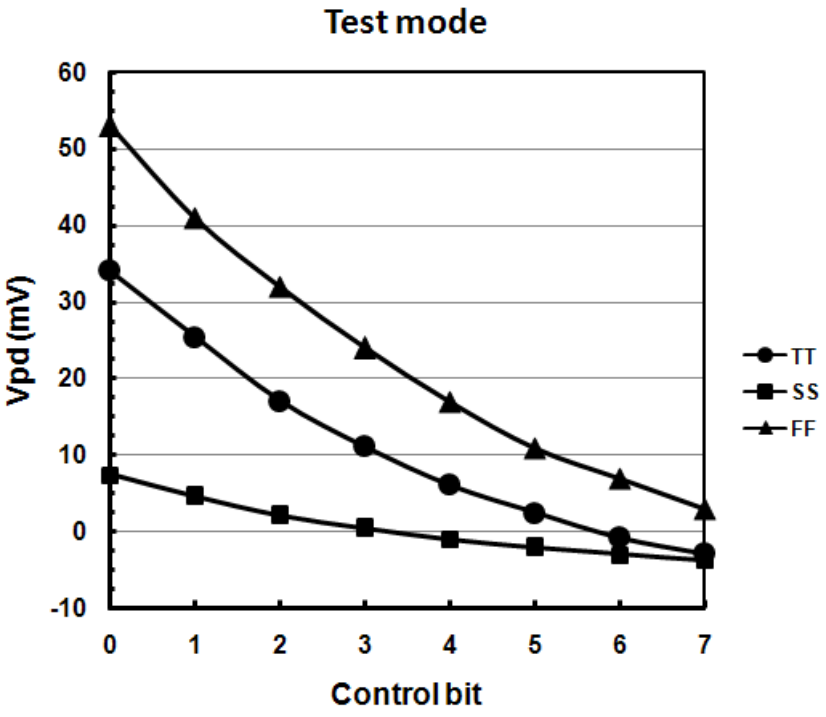


Fig. 4-11 Test mode: The output difference of the two power detectors vs. control bit

4.2.8 Chip implementations and measurement

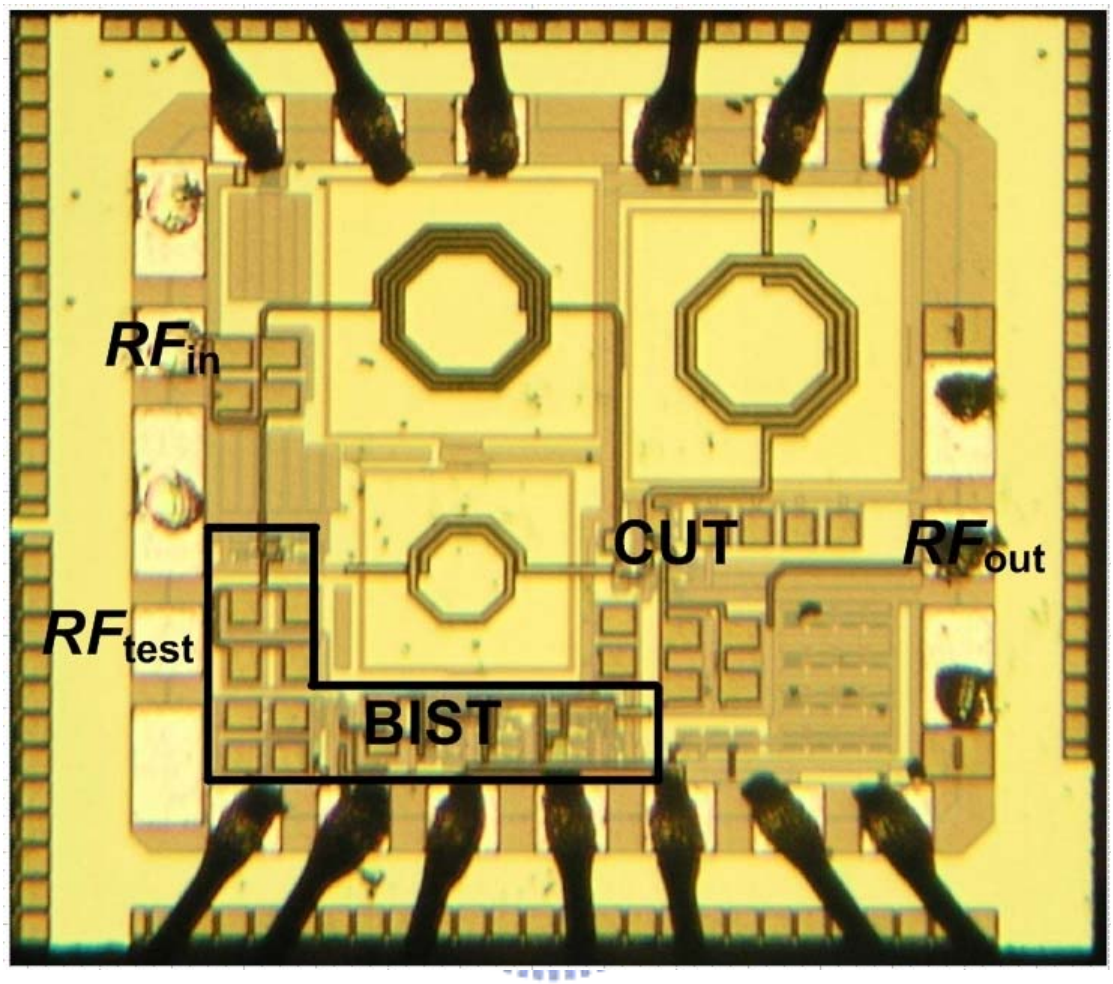


Fig. 4-12 Die photo

The RF BIST module integrated with a 5GHz LNA is implemented in TSMC 0.18um CMOS technology. Fig. X shows the die photo of the fabricated circuit with total active area (excluding the pads) of 0.698mm x 0.622mm. The BIST area is 10.79% of the active area. MIM capacitors used for AC coupling and low pass filter dominants the whole BIST area. Baseband MOS and resistors which don't have large area of deep N well guarding them are utilized to minimize the BIST area. Layout techniques such as dummy resistors are used to reduce the mismatches for the DSA.

Unfortunately, the digital controls of the DSA and the power detector back of it are both failed by antenna effects. Therefore, observations of DSA cannot be made.

Without noticing to check the antenna rules, large pieces of metal are connected to the gates of these circuits whose dimensions are designed particularly small, as depicted in Fig 4-13.

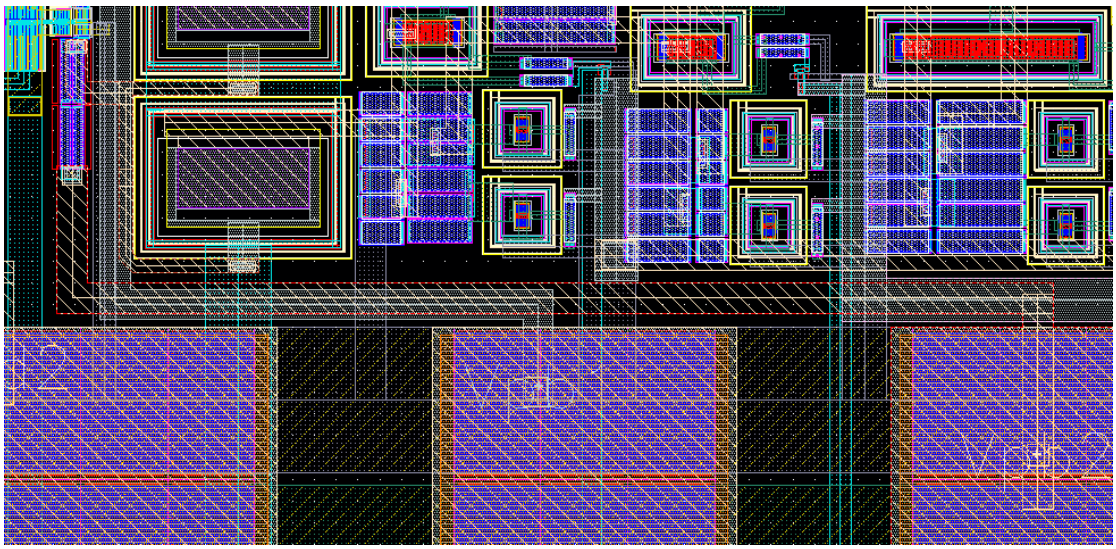


Fig. 4-13 Violations of antenna rule

The antenna effect, more formally plasma induced gate oxide damage, is an effect that can potentially cause yield and reliability problems during the manufacture of MOS integrated circuits. The word "*antenna*" is somewhat misleading. The problem is really the collection of charge, not the normal meaning of antenna, which is a device for converting electromagnetic fields to/from electrical currents. The antenna effect generates stress-induced leakage currents that can lead to either immediate or delayed failure of the overstressed dielectrics. A solution to fix violations of the antenna rule is to add *M1-Nactive*s on the biasing resistors for ESD protection.

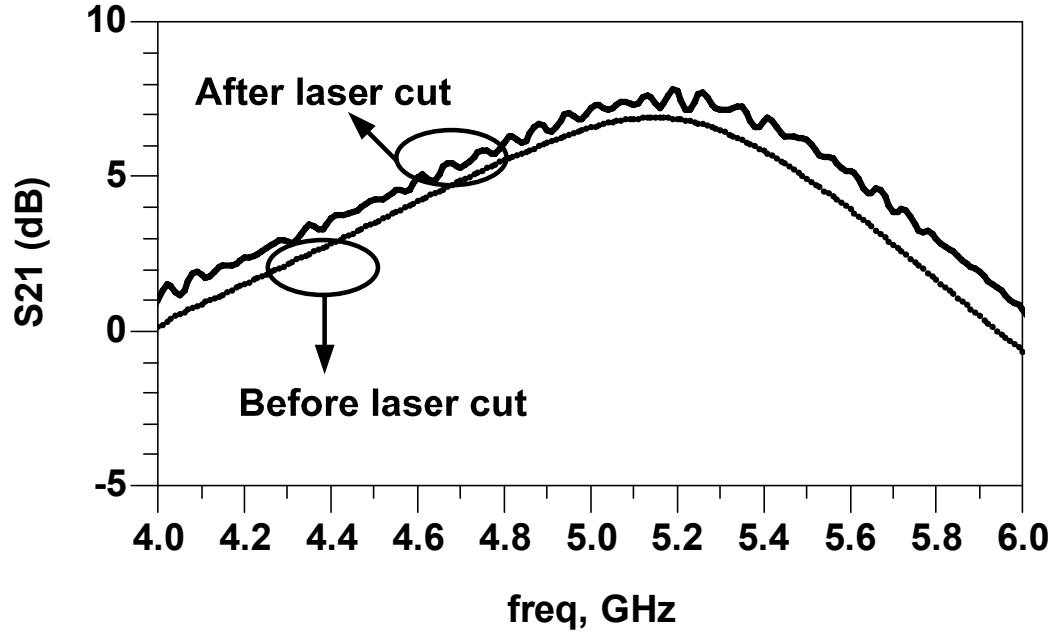
By the symptoms below, it is confirmed that the chip failure is caused by antenna effect.

(1) Current consumption from VDD is as large as 1.9mA while the other bias voltages of the circuit are off.

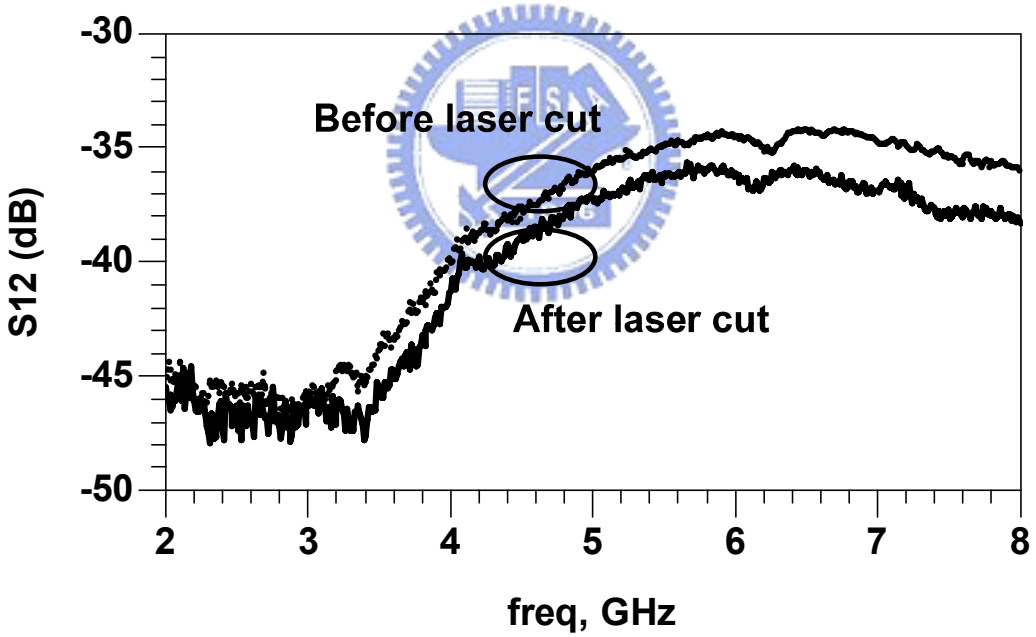
(2) Currents passing through the gates of the DSA digital controls are as large as 110mA.

(3) Currents passing through the gate bias of *PD2* are as large as 1.23mA

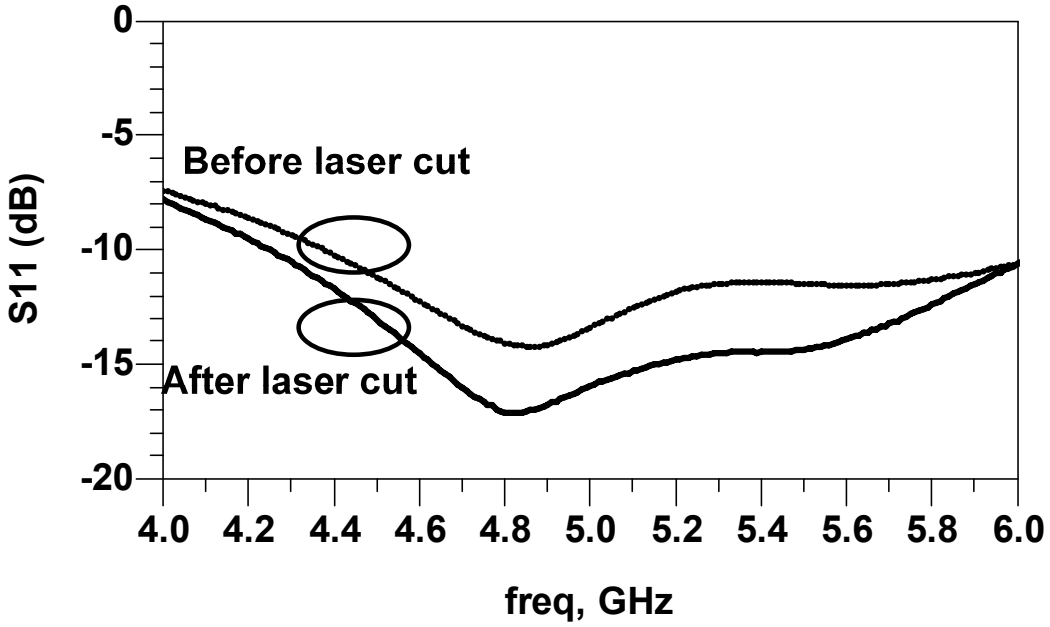
Another problem of the chip is that the maximum gain of the LNA is only around 7dB. We first speculate that the performance of the LNA during maybe affected by the BIST module. Therefore, laser-cut were made on the connections between the LNA and the BIST module. Fig. 4-14 shows the S parameter measurements of the LNA performance before and after after-laser-cutting. It can be see that the gain didn't enhance greatly. There are ripples on the curve of S_{21}. Fig. 4-15 shows the P1dB is around -12dBm. Measurement result of noise figure is sown in Fig, 4-16.Luckily, *PD1* can still be measured, as shown in Fig. 4-17.


10
5
0
-5
S21 (dB)
After laser cut
Before laser cut
4.0
4.2
4.4
4.6
4.8
5.0
5.2
5.4
5.6
5.8
6.0
freq, GHz

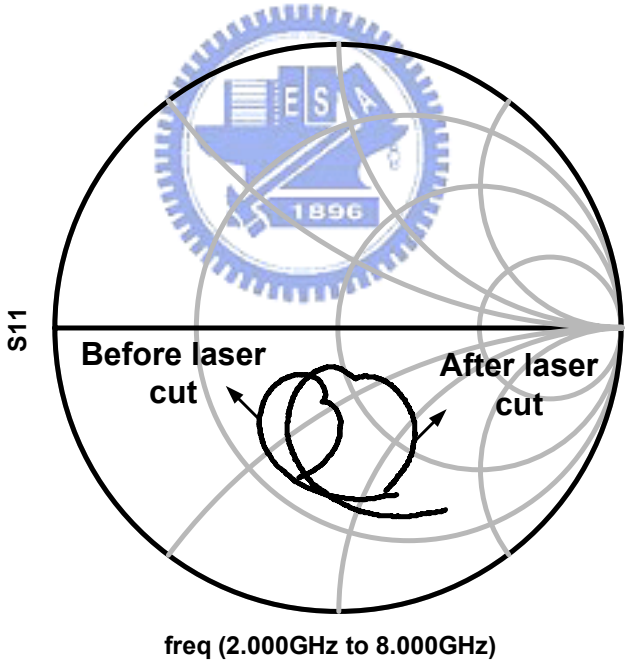
(a)


-30
-35
-40
-45
-50
S12 (dB)
Before laser cut
After laser cut
2
3
4
5
6
7
8
freq, GHz

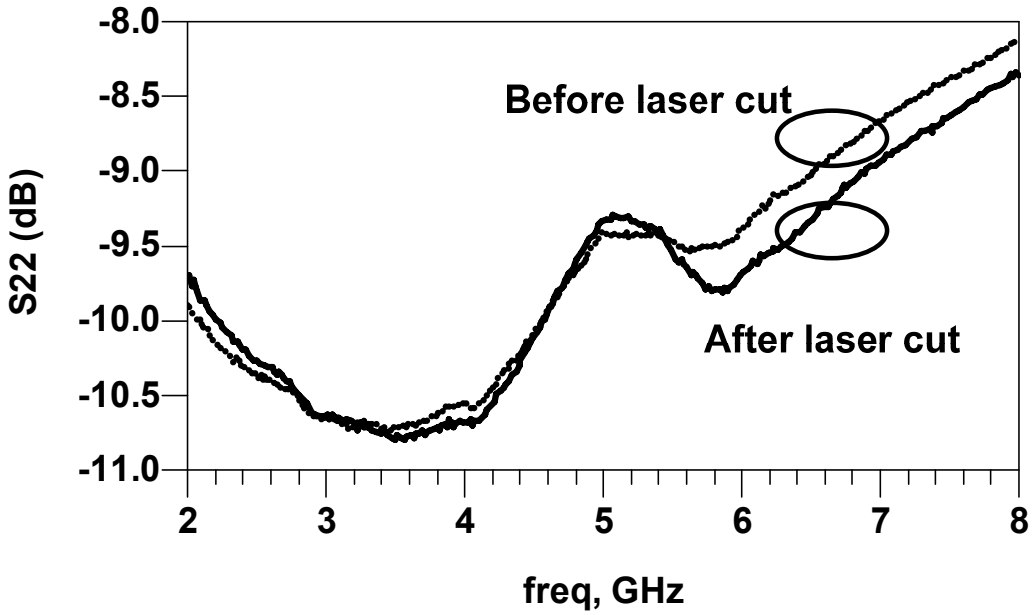
(b)


0
-5
-10
-15
-20
S11 (dB)
Before laser cut
After laser cut
4.0
4.2
4.4
4.6
4.8
5.0
5.2
5.4
5.6
5.8
6.0
freq, GHz

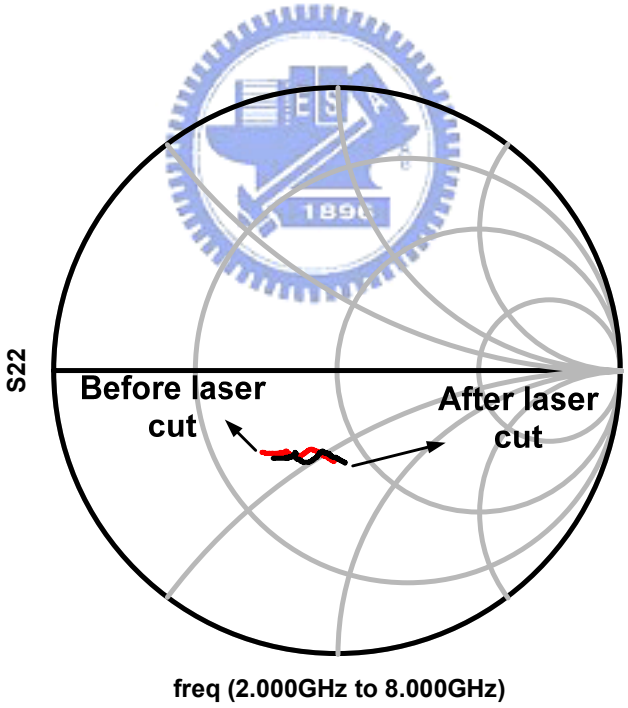
(c)


S11
Before laser cut
After laser cut
freq (2.000GHz to 8.000GHz)

(d)



(e)



(f)

Fig. 4-14 (a) S21 (b) S12 (c) S11 (d) S11 Smith Chart (e) S22 (f) S22 Smith Chart

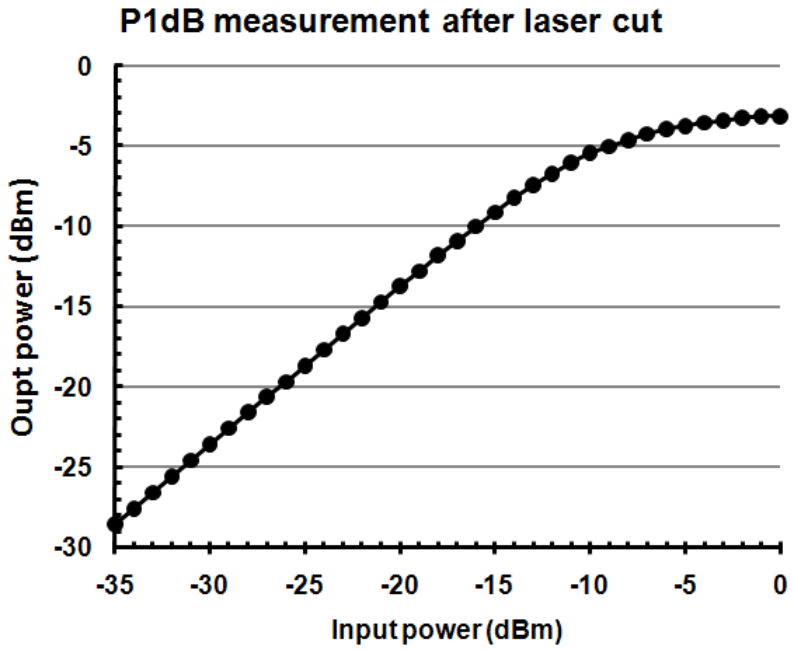


Fig. 4-15 P1dB measurements

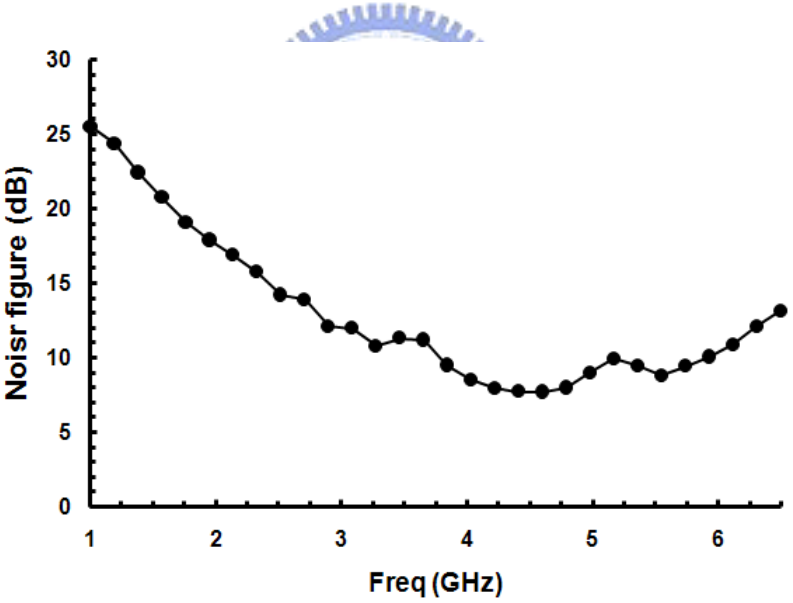


Fig. 4-16 Noise figure

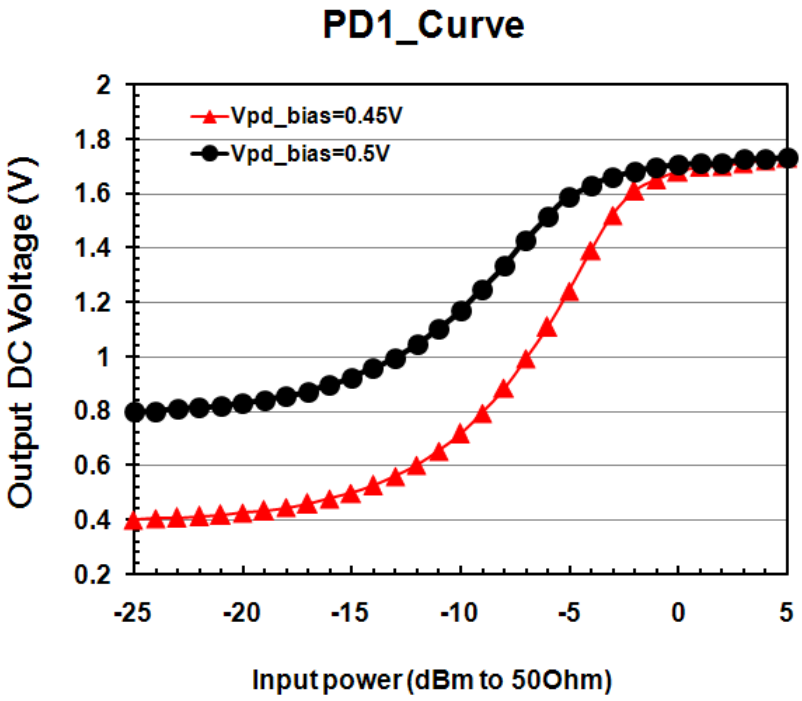


Fig. 4-17 Power detector curve measurement

4.3 RF BIST design with R-72R Ladder

4.3.1 Variations of the DSA

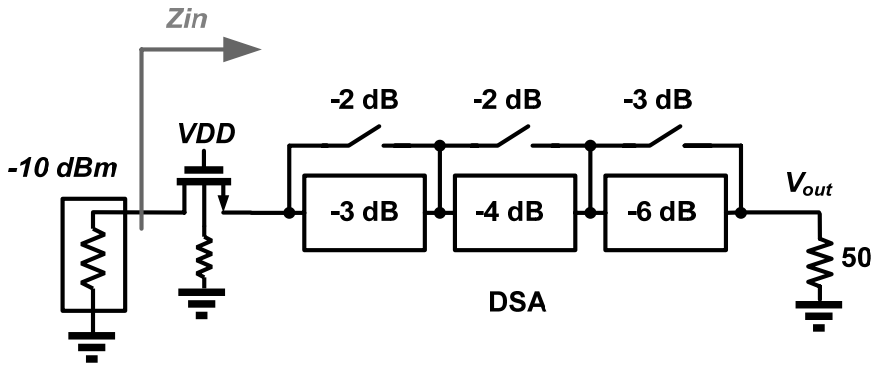
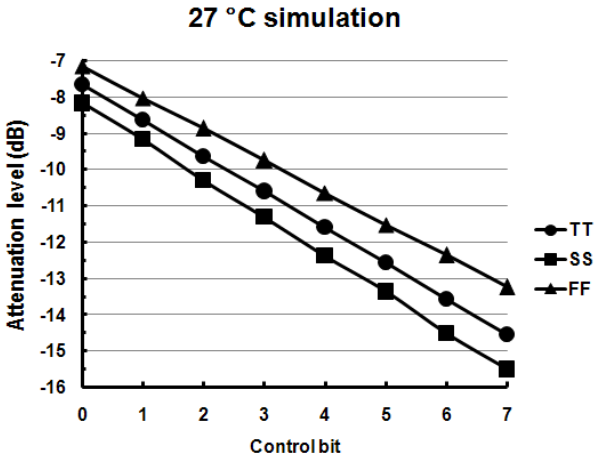


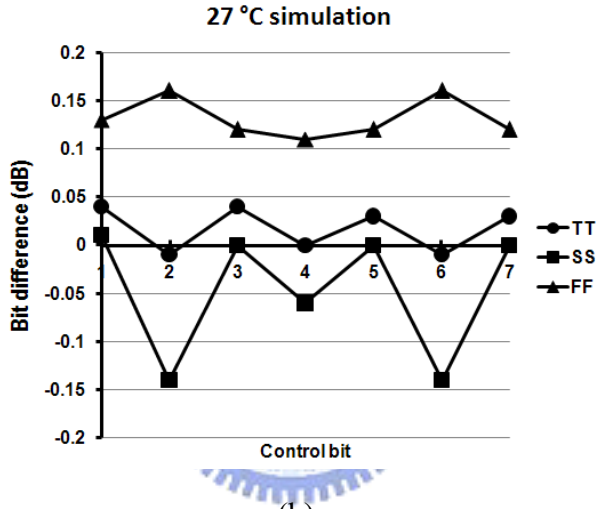
Fig. 4-18 Observation of process variations for the DSA

The proposed BIST architecture depends on the accuracy of the DSA. This means that this critical circuit building block must be tolerance to both process and temperature (PT) variations in order to ensure the BIST accuracy. Fig. 4-18 is the simulation setup to observe the variations of a DSA. The factors from PD2 and AC coupling capacitor are removed by replacing the load with an ideal 50 Ohm. Fig. 4-19 and Fig. 4-20 are the simulation results of different corner cases in two different temperatures by a 5GHz -10dBm test tone. Notice that I shift the whole attenuation levels of Fig. 4-19, 20 (a) 10dB higher to make the observations easier. Fig. 4-19, 20(b) is calculation of Fig. 4-19, 20 (a) by (4-11). Fig. 4-19, 20(c) is the real part of input impedance of the entire path.

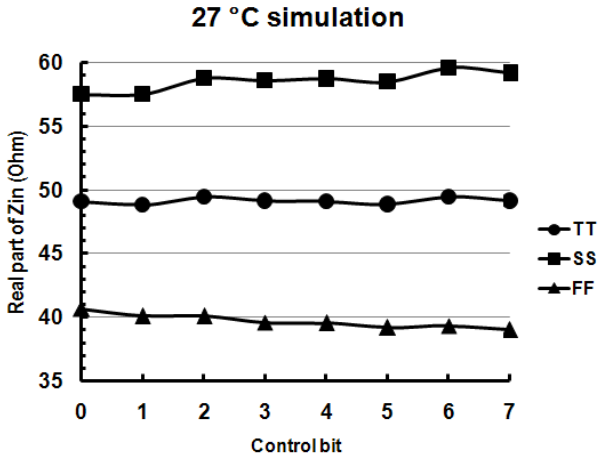
The TT corner case is nearly ideal that has bit difference smaller than 0.05dB and the real part of input impedance pretty close to 50Ohm at all control bits. However, the bit difference is as large as 0.15dB for both SS and FF corner cases. Moreover, the range of the input impedance varies at a range of 20Ohm is another serious problem. So as to say, DSA is not a reliable circuit building block for in this BIST architecture.



(a)

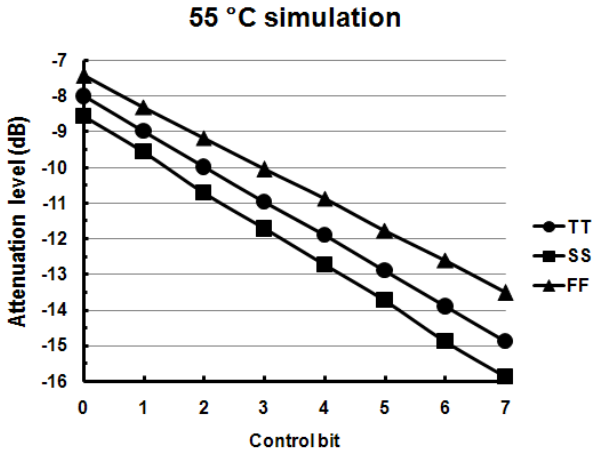


(b)

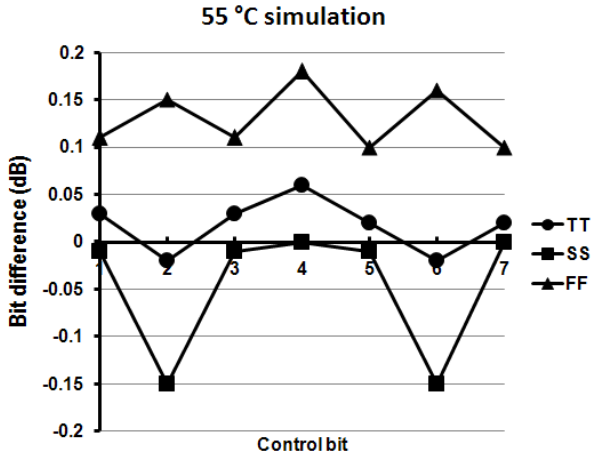


(c)

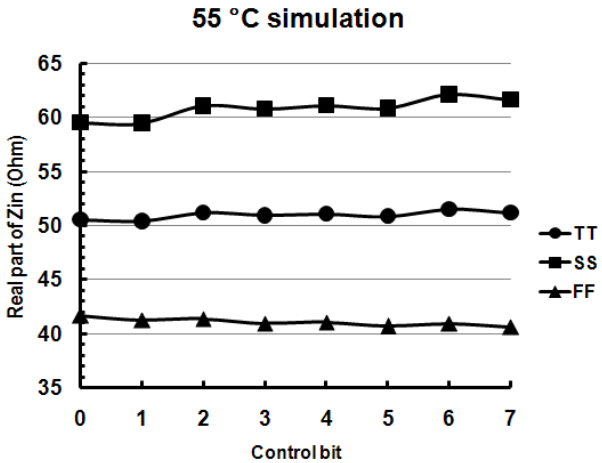
Fig. 4-19 27°C Simulation (a) Attenuation (b) Bit difference (c) Input impedance



(a)



(b)



(c)

Fig. 4-20 55°C Simulation (a) Attenuation (b) Bit difference (c) Input impedance

4.3.2 R-72R voltage attenuator

A new configuration of R-72R voltage attenuator is proposed to deal with the process variation problems of the DSA. The bottleneck of DSA design is that specific power attenuation levels can only be generated by certain resistor values of an π attenuator and causes both matching and attenuation level varies with the process and temperature variations dependently. Intuitively speaking, relative voltage division by means of resistor string can be independent of any process and temperature variations. Here, we utilize this characteristic to design a voltage attenuator with -1dB/step.

The following equations show the required relative resistor values to produce a -1dB attenuation, depicted in Fig. 4-21(a).

$$\frac{V_O}{V_i} = A_{ATT}$$
$$-1\ dB = 20 * \log A_{ATT}$$
$$A_{ATT} = 10^{\frac{-1}{20}} = 1.122^{-1} = \frac{2.244^{-1}}{2} \approx \frac{2.25^{-1}}{2} = \frac{2}{2.25} = \frac{8}{9} = \frac{1}{1+8} \quad (4.12)$$

Thus -1dB attenuation can be achieved by the voltage division of R and 8R coincidentally. Notice that the actual attenuation level of R and 8R is -1.023dB but we still approximate it as - 1dB.

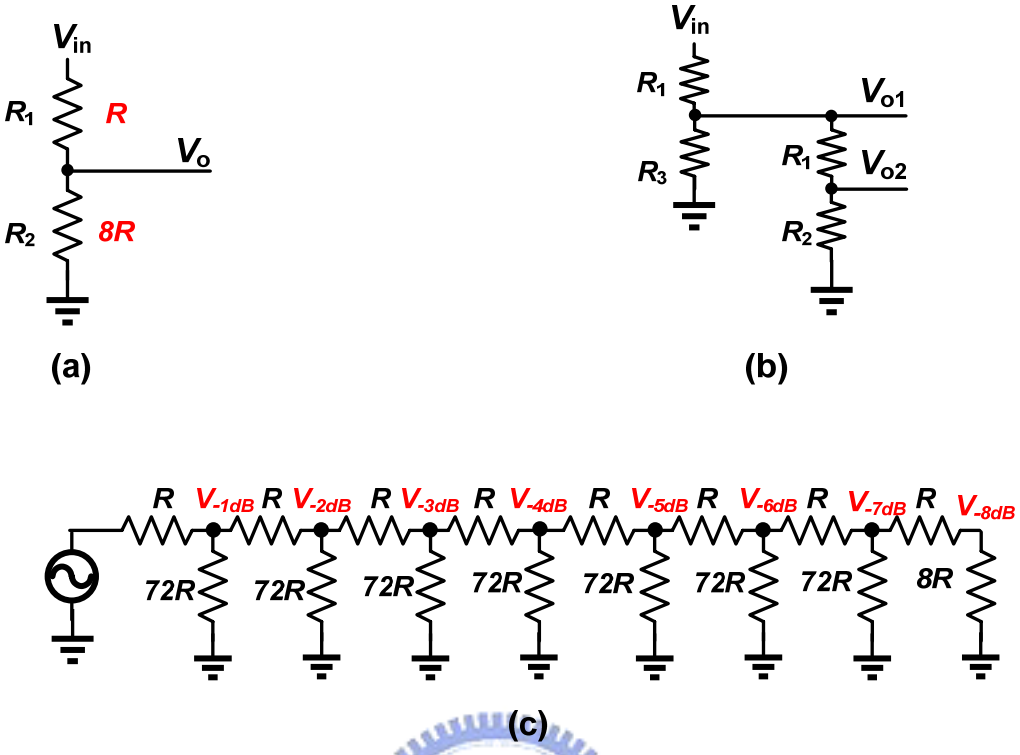


Fig. 4-21 (a) -1dB calculation (b) -1&-2dB calculation (c) R-72R ladder

We can extend the resistor string of Fig. 4-21(a) to (b) to make V_{O1} 1dB below V_{IN} and V_{O2} 2dB below V_{IN}. Equations can be listed as follows,

$$V_{o2} = \frac{8}{9}V_{o1} \Rightarrow \frac{R_1}{R_1 + R_2} = \frac{8}{9}$$

$$V_{o2} = \frac{8}{9}V_{o1} \Rightarrow \frac{R_1}{R_1 + [(R_1 + R_2) // R_3]} = \frac{8}{9}$$

$$\Rightarrow R_1 = R,\ R_2 = 8R,\ R_3 = 72R \qquad (4.13)$$

where R is an arbitrary value.

Fig. 4-22 shows a simulation result of the R-72R ladder in Fig. 4-21(c). Notice that *72R* is an enormous value if we use identical resistors for *R*. By replacing *8R* with *R*, *R* with 8 parallel *R*, and *72R* with 9 series *R*, the number of resistors used is reduced.

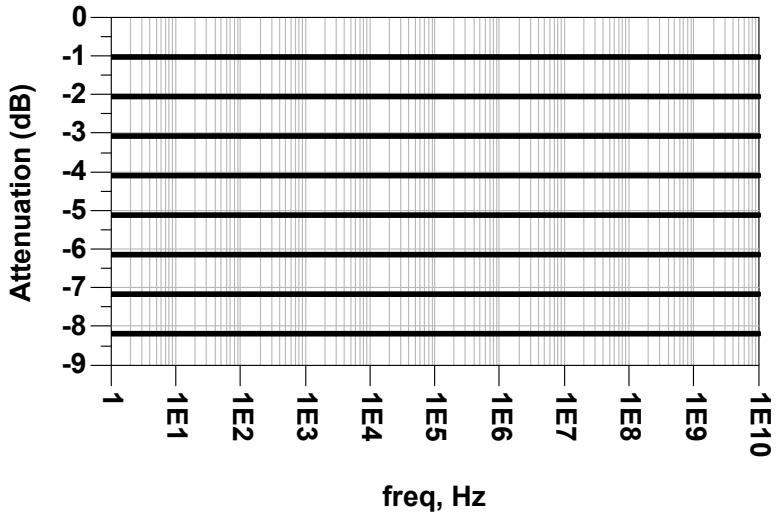


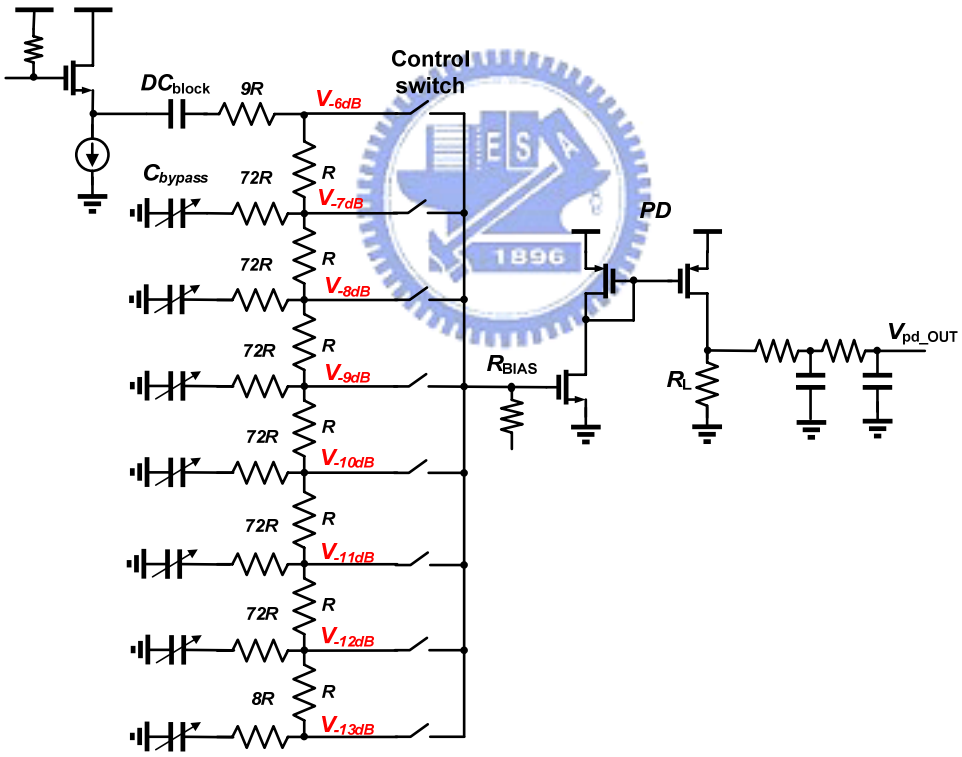
Fig. 4-22 Simulation result of the R-72R ladder

4.3.3 R-72R ladder and power detector combination

The BIST circuitry would definitely need a high input impedance (in contrast to 50Ohm) to minimize the loading effects to our CUT since we move the attenuation circuit from power domain to voltage domain. It also implies that the power detector acting as the following stage of the R-72R ladder needs an even higher input impedance in order not to break the excellent voltage division relation of the ladder. The schematics depicted in Fig. 4 are the history of several combination ideas.

A very straight forward approach is to add switches as path control between the ladder and the PD which is shown in Fig. 4-23(a). Varactors are used for bypass capacitors instead of MIM capacitors to minimize the area of BIST circuitry. Besides, an additional source follower is employed as a buffer between CUT and BIST module. A resistor of *9R* is added for high impedance loading at the buffer's output. Although the input impedance of the PD can be designed as high as possible, the voltage division relation is drastically effected by the loading of PD flipping around the

output nodes of the ladder. An alternative approach depicted in Fig. 4-23(b) adds dummy loadings whose values are the same with the PD. When one of the attenuation paths is selected, the others are switched to the dummy loadings to make the loading of the ladder fixed. However, the area of switch is increased two times and the exact input impedance of the PD is difficult to implement. The approach depicted in Fig, 4-23(c) is the best I can think of. In this configuration, identical PDs with extremely high input impedance are used. The simulation of input impedance of a PD wibb be shown in the next section. The PDs can all share the common part, R_{LOAD} and low pass filter, in order to minimize the area.



(a)

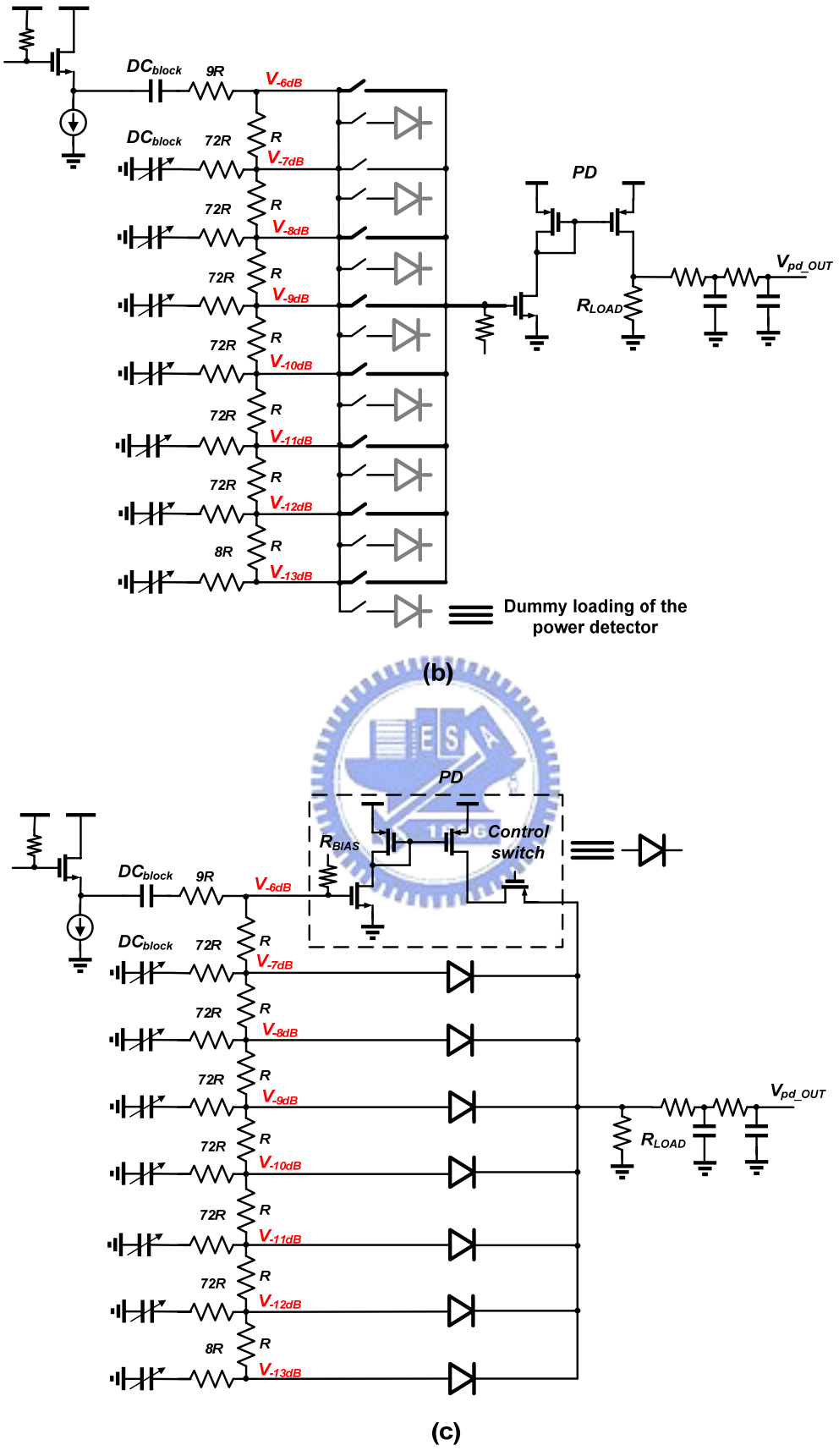
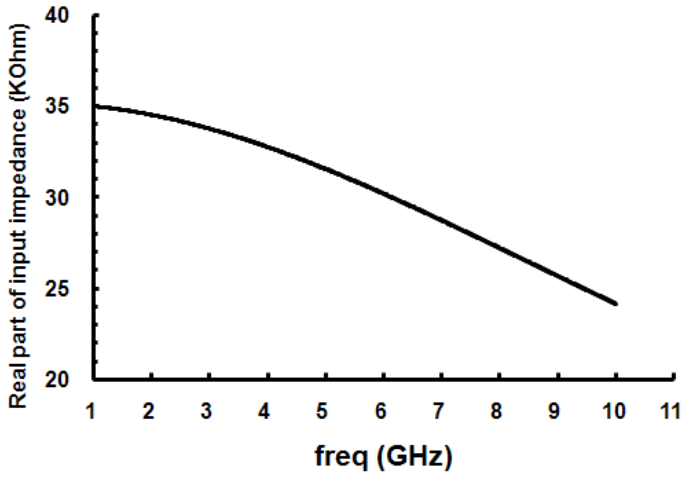


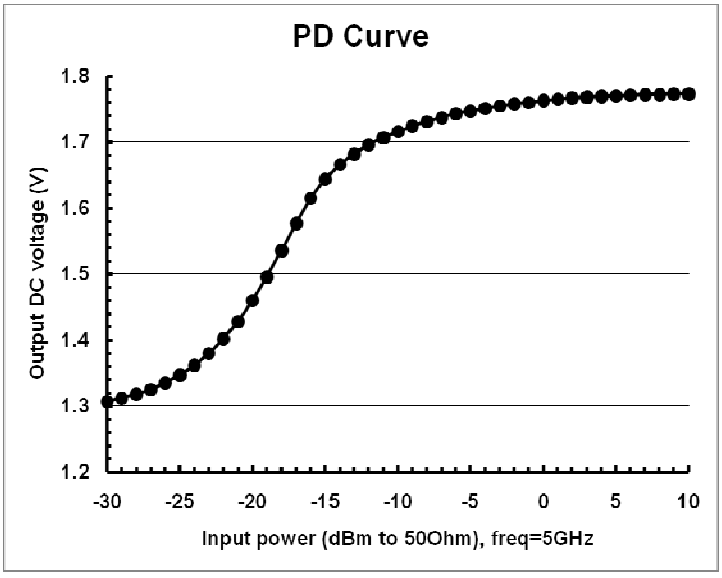
Fig. 4-23 Combination ideas

4.3.4 Current amp PD with high input impedance

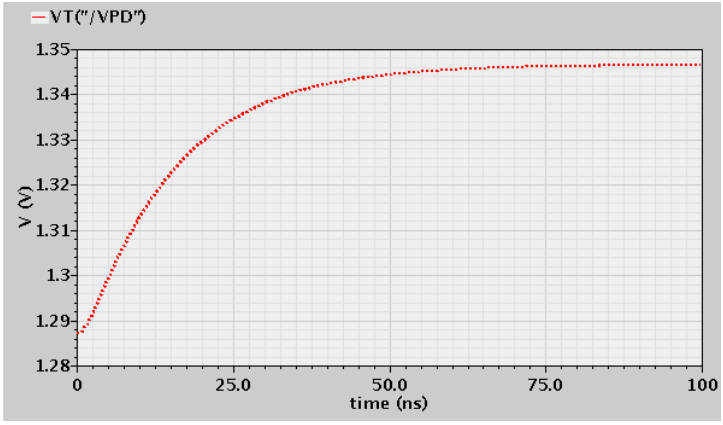
The current amp PD is re-designed to an extremely high impedance by using. The parasitic effects can be by selecting a small dimension MOS. Fig. 4-24(a) plots the real part. Fig. 4-24(b) is a check of the PD curve. A 15mV of DC output difference between -24 and -25dBm input power relaxes the design of comparator's threshold voltage. With input power 17.78mV (-25dBm to 50Ohm), Fig. 4-24(c) shows the response time of the PD to reach its steady state is around 100nsecs. Since small size of the MOS are used, current consumption is only 87.87uA for the turn on PD cell plus a total of 10.15 (7*1.45uA) for the turned off cells.



(a)



(b)



(c)

Fig. 4-24 High impedance power detector (a) real part of input impedance (b) PD transfer curve (c) Transient response

4.3.5 Comparator

In this version of RF BIST design, a comparator is integrated in for function completeness. Fig. 4-25 is a brief review of the conventional input offset cancellation mechanism. *Vos* is the input offset voltage and *V1*, *V2* are the two voltages to be compared. *CLK1a* advances *CLK1* a bit to let the circuit only affected by the charge injection of *SW1*. In *CLK1*, both *V1* and the offset voltage are stored into the sampling capacitor, C_s. The voltage stored can be expressed as:

$$Vc = V_1 - \frac{A}{1+A} Vos \tag{4.14}$$

where *A* is the gain of the comparator.

In *CLK2*, the output voltage *Vo* can be expressed as:

$$\begin{aligned} Vo &= A[V_+ - V_-] \\ &= A[Vos - (V_2 + \frac{A}{1+A} Vos - V_1)] \\ &\approx A[V_1 - V_2] + \frac{1}{1+A} Vos \end{aligned} \tag{4.15}$$

The equation above indicates a larger gain can compress the offset voltage.

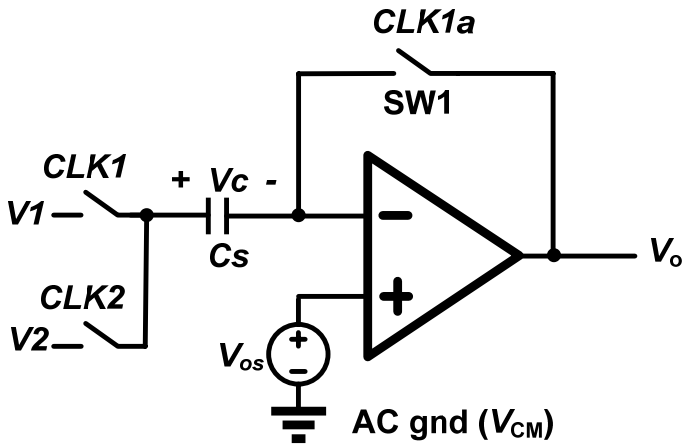


Fig. 4-25 Input offset cancellation

Since the PD needs 100nsec to reach its steady state, we arranged another 100nsec of margin for storing or comparing. Thus, the clock width will be 200nsec (period of 400nsec) for *CLK1a*, *CLK1*, and *CLK2*. This means that a high speed comparator is not required.

Depicted in Fig. 4-26, a conventional single-end output OP amp is employed for the comparator. The transistor *Mz* operates as a null resistor to eliminate the effect of RHP zero from feedforward through the compensating capacitor, *Cc*. In order to speed up the comparison time, we can disconnect the compensating capacitor during the comparison phase. In the storing phase, the OP amp acts like a unity gain buffer which has stability issues, we can then connect *Cc* back again. Two extra inverters are placed to make the compared output reaches an accurate logic level.

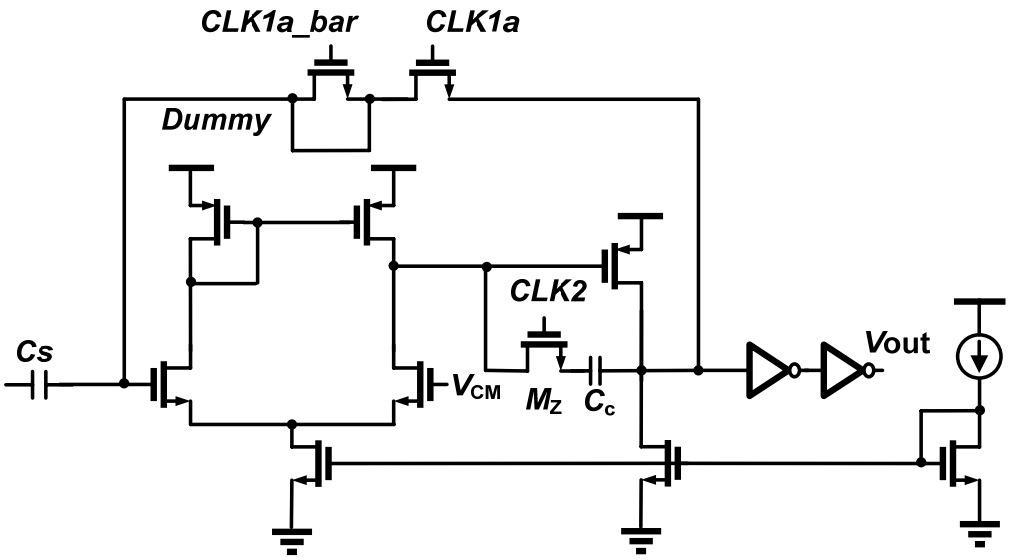


Fig. 4-26 Schematic of the comparator

4.3.6 Modified BIST architecture

Fig. 4-27(a) is a modified BIST architecture that replaces the DSA with R-72R ladder and also integrates a comparator into it. An identical buffer is added between the CUT and the RF output port so as to make measure comparable to the BIST module. *CLK1*, *CLK1a* and *CLK2* are arranged for merging the input offset cancellation techniques of a comparator and the BIST loop together. A 3 to 8 decoder is added to minimize the number of the control pads. The NAND gates are adopted for enable control of the whole path Fig. 4(b). Although clocks are usually undesirable to appear in RF frontends, they are used only in off-line tests.

The operating mode is indicated in Fig. 4(b) where the *CLK2* is turn off and the buffer in the BIST module is shut down in order to make our CUT operates normally. The test mode can be separated into two timings, *CLK1* and *CLK2*. In CLK1 phase as Fig. 4(c), the RF test signal is converted to a DC level by means of the PD1 and then stored in the sampling capacitor, *Cin*. Beside, input offset of the comparator is also stored in the sampling capacitor. A little bit of different from the former design is that

the PD1 must also match with the test port. In *CLK2* phase as Fig. 4(d), the test signal travels through the CUT, the R-72R ladder, and finally compares with the voltage stored. By few bits of iterations, the gain of the CUT can be readout from us.

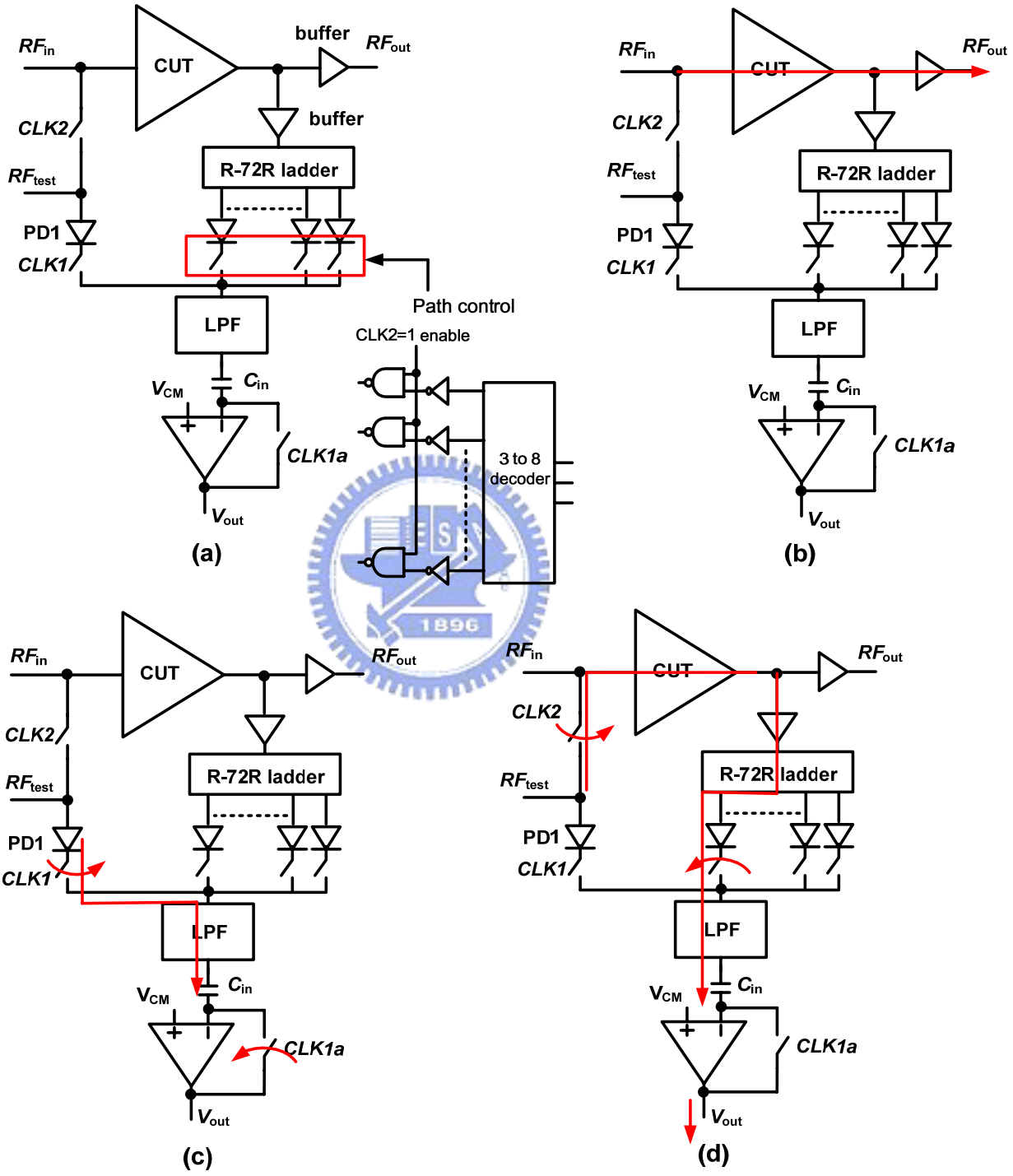


Fig. 4-27 (a) Modified BIST architecture (b) operating mode (c) & (d) test mode

4.4 Summary

The BIST design of a 5GHz that uses power comparing method is fabricated in TSMC 0.18um technology, consist of a 5GHz LNA as CUT, two power detectors, digital step attenuator. However, function verifications cannot be made due to antenna effect. Only partial measurements are made: S parameters, P1dB, and noise figure of LNA, power detector. Table 3 is the performance comparison table of recent RF BIST designs. The variations issues that cause error in the BIST function are explored. An alternative approach of R-72R ladder is proposed that is tolerance to PT variations.

Table 3 Compare with recent RF BIST designs

	VTS' 05[6] (post-simulation) & RFIC'07[7]	**VTS' 06 [9]**	**VTS' 07 [10]**	**This work (post-simulation)**
Technology	TSMC 0.35um	TSMC 0.18um	TSMC 0.18um	TSMC 0.18um
Operating frequency (GHz)	2.4	5.2	5	5
CUT/performance	LNA	VGA	LNA	LNA
CUT Operating mode	9.5	12.1/9.4 (dB)	16.7	15.68
BIST area (mm^2)	0.031	0.06	0.044	0.077
BIST Method	I/O power sensing	I/O power sensing	I/O power sensing	I/O power comparing
Testable items	Gain P1dB	Gain P1dB	Gain P1dB Current	Gain P1dB
BIST power consumption (mW)	10 (single RMS detector)	3.5	1.8	1.35
BIST error	N/A	+/- 1.5dB	0.7 dB	< 1dB
Dynamic range of the PD (dB)	20	>25	30 (-15~15dBm)	30 (-25~-5dBm)
BIST calibration	No	Yes	Yes	No

Chapter V

Conclusion and future work

5.1 Conclusion

In this thesis, two application circuits of RF power detector are designed. The main design principle is using power comparing instead of obtaining the absolute power levels. The first application is the power detection design in WiMAX transmitter. Although fabrication was not made, a design methodology is given. The architecture is suitable for wide dynamic range detection and small difference comparing.

Another application of RF power detector is the BIST design for a 5GHz LNA. The circuit under test is test by a variable attenuation and power comparing. Unfortunately, function verifications cannot be made due violations of the antenna rule.

5.2 Future work

For the auto-calibrated IQ modulator, the 3-wire needs to be re-designed o avoid latch up. The power detection design can be integrated in the open loop chip for function completeness.

The modified BIST architecture is proposed. Further design and chip implementations can be made. Layout of digital controls of attenuation path should avoid large pieces of metal connecting to their gates.

Reference

[1] Tsung-Nan Yu, “ Direct Up-Conversion Mixer with Matching Compensation Eliminating I/Q Imbalance and LO Feedthrough in WiMAX and WiFi Transmitter, “ Master Thesis, NCTU Hsin-Chu Taiwan, May 2008

[2] R.G. Meyer, “Low-Power Monolithic RF Peak Detector Analysis,” *IEEE J. Solid State Circuit*s, vol. 30 no. 1, pp.65-67, Jan. 1995

[3] Tao Zhang, William R. Eienstadt, Robert M. Fox, and Qizhang Yin ” Bipolar Microwave RMS Power Detectors,” *IEEE J. Solid State Circuits*, vol. 41 no. 9, pp.2188-2192, Sep. 2006

[4] Tao Zhang, William R. Eienstadt, Robert M. Fox, ”A Novel 5GHz RF Power Detectors,” *IEEE ISCAS*, 2004, pp. 897-900.

[5] Qizhang Yin, William R. Eienstadt, Robert M. Fox, and Tao Zhang, “ A Translinear RMS Dectector for Embedded Test Of RF ICs,” *IEEE Trans. Instrumentation and Measurement*, vol. 54, no. 5, pp. 1708-1714, Oct. 2005.

[6] Alberto Valdes-Garcia, *et al.,* “A CMOS RF RMS Detector for Built-in Testing of Wireless Transceivers,” *IEEE VLSI Test Symp.*, 2005.

[7] Alberto Valdes-Garcia, *et al.*, “Built-in Self Test of RF Transceiver SoCs: from Signal Chain to RF Synthesizers (Invited),” *IEEE RFIC Symp.*, 2007, pp. 335-338.

[8] Alberto Valde-Garcia and Jose Silva-Martinez, “On-Chip Testing Techniques for RF Wireless Transceivers,” *IEEE Design and Test of Computers*, vol. 23, pp. 268-277, July 2006.

[9] H-H. Hsieh and L.-H. Lu, “Integrated CMOS power sensors for BIST

applications," *IEEE VLSI Test Symp.*, 2006.

[10] Yen-Chih Huang, H-H. Hsieh and L.-H. Lu, "A low noise amplifier with integrated current and power sensors for RF BIST Applications," *IEEE VLSI Test Symp.*, 2007.

[11] Yijun Zhou and Michael Chia Yan Wah, "A Wide Band CMOS RF Power Detector," *IEEE ISCAS*, 2006, pp. 4228-4231.

[12] Kenneth A. Townsend, James W. Haslett, John Nielsen,"A CMOS Integrated Power Detector for UWB," *IEEE ISCAS*, 2007, pp. 3039-3042.

[13] Richard Smith Hughes, *Logarithmic Amplification with application to Radar and EW,* Artech House, 1986.

[14] Po-Chiun Huang, Yi Huei Chen, and Chorng-Kuang Wang, "A 2V 10.7MHz CMOS Limiting Amplifier/RSSI," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1474-1479, Oct. 2000.

[15] Katsuji Kimura, "A CMOS Logarithmic IF Amplifier with Unbalanced Source-Couple Pairs," J. Solid-State Circuits, vol. 28, no. 1, pp. 78-83, Jan. 1993.

[16] Kimmo Koli and Kari Halonen, "A 2.5 V temperature compensated CMOS logarithmic amplifier," *IEEE Custom Integrated Circuits Conf.*, May 1997, pp. 79-82.

[17] Chao Yang and Andrew Mason, "Process/Temperature Variation Tolerant Precision Signal Strength Indicator," *IEEE Trans. On Circuits Syst. I, Fundamental Theory and Applications*, vol. 55, no. 3, pp. 722-729, Apr. 2008.

[18] Tsuneo Tsukahara and Masayuki Ishikawa, "A 2GHz 60dB Dynamic-Range Si Logarithmic/Limiting Amplifier with Low-Phase Deviations," *IEEE ISSCC*, Feb. 1997.

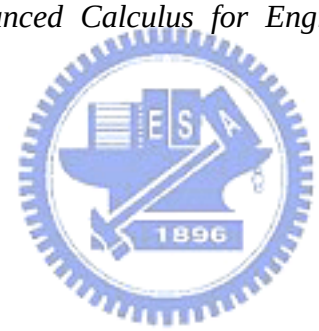
[19] S. Khorram, A. Rofougaran, and A. A. Abidi, “A CMOS Limiting Amplifier and Signal-Strength Indicator,” IEEE Symp. VLSI Circuits Digest of Technical Papers, June 1995, pp.95-96.

[20] Stacy Ho, “A 450MHz CMOS RF Power Detector,” *IEEE RFIC Symp.*, 2001, pp. 209-212.

[21] Jung-Suk Goo, Hee-Tae Ahn,, Donald J. Ladwig, Zhiping Yu, Thomas H. Lee, and Robert W. Dutton, ”A Noise Optimization Technique for Integrated Low-Noise Amplifiers,” IEEE J. Solid State Circuits, vol. 37 no.8, Aug. 2002

[22] Behzad Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

[23] F. B. Hildebrand, *Advanced Calculus for Engineers*. Englewood Cliffs, NJ: Prentice-Hall, 1949.



Vita

謝易耕 Yi-Keng Hsieh

出生日期: 1983/05/29

出生地:台北,台灣

教育程度:

2002/09~2006/06

國立交通大學電機與控制工程學系學士

2006/08~2008/08

國立交通大學電子研究所 碩士