國　立　交　通　大　學

電子工程學系　電子研究所碩士班

碩 士 論 文

10Gbps 自動增益控制電路

10Gbps Automatic Gain Control Circuit

研 究 生 ： 吳國維

指導教授 ： 陳巍仁　博士

中華民國九十七年十一月

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10Gbps 自動增益控制電路

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ABSTRACT (CHINESE)

近年來隨著半導體製程的不斷演進，以及大眾對於功率效能的需求，使得多核心運算成為實現高資料運算量的處理平台主流之一；而由於光纖傳輸具有低串音(Cross Talk)以及低電磁干擾(EMI)的特性，被視為適合應用於此類高密度高速率的資料傳輸媒介。因此，在互補式金屬氧化物半導體(CMOS)製程下實現小面積、低成本的光纖收發機電路，以期應用於高密度傳輸平台之系統單晶片設計，成為富有挑戰性以及實用性的研究主題。

為實現一個可使用脈衝振幅調變(Pulse Amplitude Modulation, PAM)的光纖接收端前級電路，增益變異的功能對輸入動態範圍有其存在的必要性；又為克服傳統全類比自動增益控制電路所面對之挑戰，如增益控制線性度不足、反應時間過長等，本論文提出一個無電感下資料傳輸速率達10Gbps，以數位方式控制增益的自動增益控制系統，並期待能應用於低電壓架構以及先進製程。

內含之可調增益放大器之部份，提出巢狀主動回授架構來增加傳輸頻寬，且使其轉移函式符合貝索濾波器(Bessel Filter)響應，以減少群體延遲(Group Delay)變異量;並以數位方式控制輸入級源級退化阻值以改變等效轉

導值，藉此改變放大器增益。再利用數位電路實現具有-二分搜尋/線性搜尋-雙模式的增益控制電路，達到快速鎖定、長時穩定的設計考量。

為了使輸出電壓擺幅能在需求範圍之內，電路中也包含了輸出擺幅峰值偵測器(Peak Detector)以及比較器，來鎖定擺幅極大值並且和參考電壓值進行比較。電壓偵測器中利用數位電路設置了開關機制來減少重置時間(Reset Time)以及趨穩時間(Settling Time)；比較器亦使其具有遲滯效應(Hysteresis Effect)，避免雜訊干擾以及增益調整解析度的有限造成電路不穩。

測試晶片使用標準 0.18μm CMOS 製程來製造。在 1.8V 的操作電壓之下，量測到的資料傳輸速率可達約 8Gbps，輸入動態範圍為 22dB，二分搜尋鎖定時間為 170ns；在 24 位元溫度計碼的控制之下，增益控制解析度可達 0.9dB/bit；晶片大小為 620x620μm^2 ，總功率消耗為 86.4mW。

10Gbps Automatic Gain Control Circuit

Student: Guo-Wei Wu **Advisor: Prof. Wei-Zen Chen**

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ABSTRACT (ENGLISH)

Recently, with the progress of the semi-conductor technology, and the demand of power efficiency, multi-cores computation becomes one of the mainstreams to realize a high speed processing platform. Due to the slight cross talk and low EMI properties, optical links are believed to be the suitable media for this high speed, high density data transmission. As a result, implementation of optical transceiver in CMOS technology with small form factor and low cost becomes a challenging and practical research topic for the SOC design of the high density communication platform.

To implement an optical receiver front-end which is suitable for PAM (Pulse Amplitude Modulation), a mechanism of gain variation is indispensable for an input dynamic concern. Furthermore, to overcome the problems of conventional analog AGC (Automatic Gain Control) circuit, such as the gain non-linearity or long response time, an inductor-less, 10Gbps, digitally gain-controlled AGC circuit is proposed in this thesis, and prospected to be applied in low voltage design and advanced process.

In order to enhance the bandwidth of the amplifier, nested active feedback architecture is proposed in the VGA (Variable Gain Amplifier) design, and its transfer function is corresponded with a Bessel type filter response, to alleviate group delay variation. For gain variation, the source degeneration resistance of input stage is controlled digitally and hence the equivalent transconductance. Moreover, the gain-controlled circuit with dual mode, binary search and linear search, is implemented by digital circuit for the design consideration of fast locking and being steady in the lone run.

To keep the output swing in the range of requirement, there are peak detector and comparator in this AGC, for utilities of peak amplitude acquisition and comparing to the reference voltage. In the peak detector, switches are adopted to reduce the reset time and settling time with digital control signal; and the comparator with Hysteresis effect can avoid the instability caused by noise and finite resolution of gain control.

The test chip is implemented in standard 0.18μm CMOS technology. Under 1.8V operating voltage, the measured data rate is about 8Gbps; input dynamic range is 22dB, with 170ns binary search settling time. With 24 bits thermometer code, gain-controlled resolution is 0.9dB/bit. Chip size is 620x620μm^2, and total power consumption is 86.4mW.

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感謝上帝，一切因著祂的恩典。

吳　國　維

于 交大

戊子 秋

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Chapter 1 Introduction

1.1 Motivation

With the growth of the semi-conductor technology, Giga-scale computing has been realized in these ten years, and brought simple and convenient signal processing and image processing for common people. Due to the demands of higher performance and lower cost never stopped, Tera-scale computing is already a topical subject for next generation.

No matter what component, algorithm or architecture is adopted, data processing ability of one chip still has its limits. When physics, algorithm and architecture face the bottleneck, or we can say, new semiconductor technique, instruction level parallelism and software level improvement can not satisfy the specifications of the system, hardware level parallelism properly becomes the solution, and gives the birth of multi-cores platform.

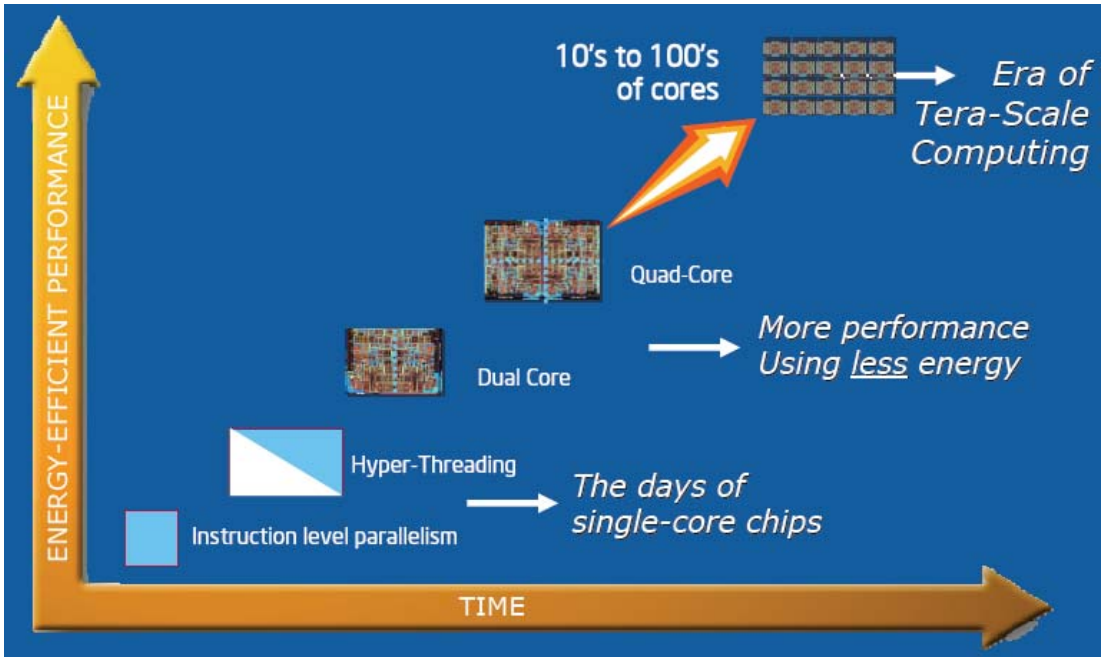


Fig. 1-1 Evolution of energy-efficient platform source: Intel

Fig. 1-1 illustrates a scenario of Intel. It shows that the multi-cores platform is one of the solutions for energy-efficient Tera-scale computation. In such a data-intensive system, channel bandwidth and density might be the key factor because of the heavy data traffic between the cores. However, high density electrical interconnects such as copper lines may suffer form severe cross talk and EMI (Electro-Magnetic Interference) as the semi-conductor process scaled down. By contrast, optical links has slight cross talk and low EMI property, may alleviate the difficulties that the electrical interconnects may face.

As a result, how to build up the optical transceiver with low cost and small form factor in semi-conductor process for SOC design becomes the critical problem. Recently, researches for optical transceiver never stopped, and even the fully integrated receiver in CMOS process has been announced [1], with data rate in multi Giga bits per second.

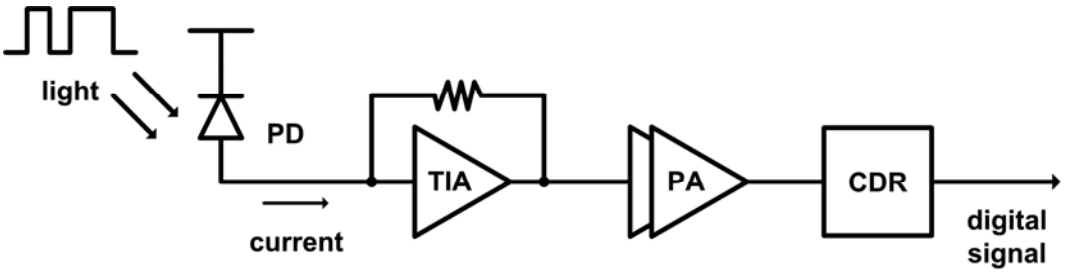


Fig. 1-2 Typical optical receiver architecture

A typical optical receiver is shown in Fig. 1-2. It is composed of PD (Photo Detector), TIA (Transimpedance Amplifier), PA (Post-Amplifier) and CDR (Clock and Data Recovery) circuit. The PD detects the light and turns it into current signal, and the succeeding TIA can change the current signal into voltage. After PA shapes the signal and delivers sufficient swing to the next stage, CDR circuit can determine the clock and data for digital processing.

Considering the channel efficiency and the bandwidth limitation of fully CMOS photo detector, PAM (Pulse Amplitude Modulation) is a one of the useful signal encoding technique to implement an optical transmission system whose data rate reaches tens Giga bits per second. Like Fig. 1-3, a 4-PAM signal could gives 2 bits information in one symbol, and increase the data rate by 2 times in a different form.

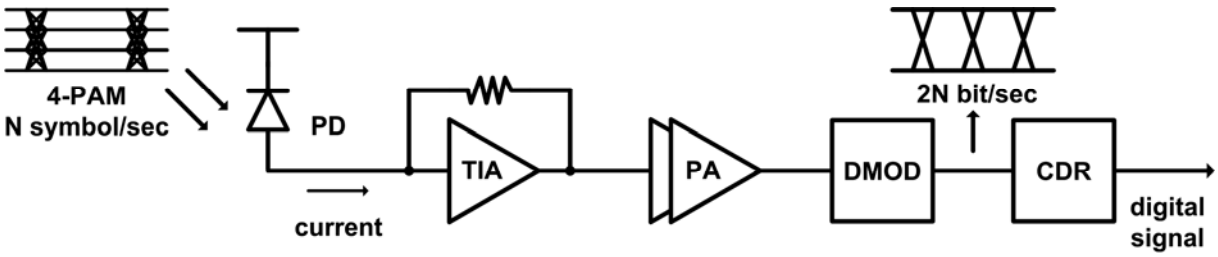


Fig. 1-3 Optical receiver architecture for PAM system

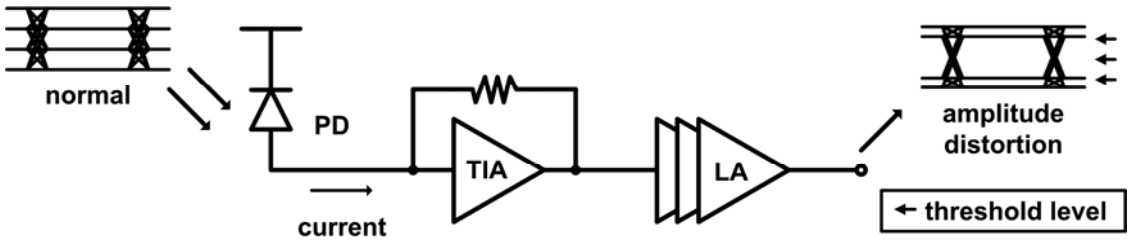


Fig. 1-4 Optical receiver composed of limiting amplifier

But, amplitude distortion and insufficient magnitude are the problems that can't be ignore in the PAM system, because it may accompany decision error for the demodulation circuits (DMOD block in Fig. 1-3).

As shown in Fig. 1-4, using an LA (Limiting Amplifier) as the post-amplifier could provide stable and large gain for the receiver, it can reduce the risk of insufficient swing because the output will be or nearly be saturated; but due to the large gain of the LA, normal input swing will certainly face the problem such as amplitude distortion, and increase the risk of demodulation error in a PAM system. So, here we can say, a LA with constant gain as the post amplifier is not so applicable for a PAM system because the threshold levels for a PAM system need to be precisely and fixed.

As a result, a linear amplifier is much suitable for succeeding demodulation in this kind of receiver front-end. Moreover, if there is uncertain channel insertion loss or varied input optical power, a gain-tuning mechanism such as VGA with enough dynamic range and its gain control circuit are indispensable, which can be signified in Fig. 1-5 in the next page.

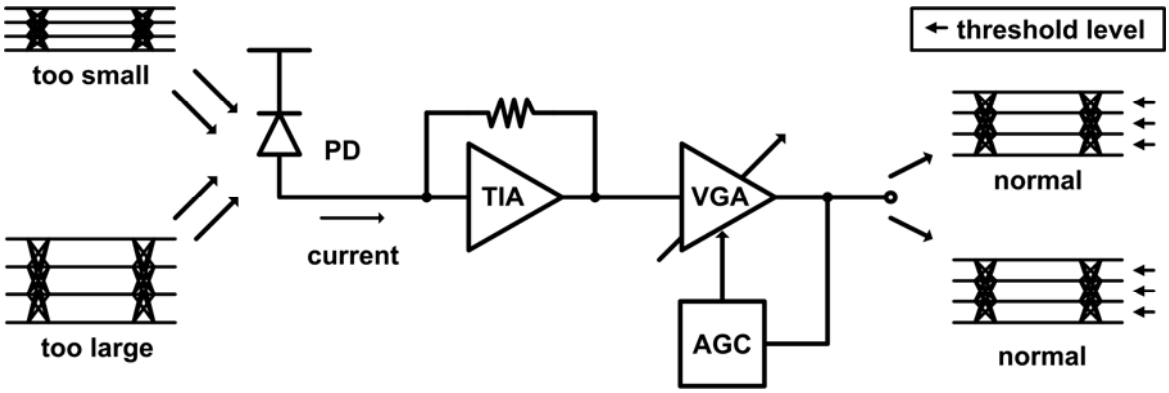


Fig. 1-5 Optical receiver composed of VGA and AGC

In the receiver front-end prototype, "how to control the gain" is the succeeding problem. For application in the optical receiver, it can be anticipated that gain control signal path could be turned into an automatic gain control loop, by the presence of peak amplitude detection, reference voltage and gain control. That is why there is not only a VGA in the receiver but also an AGC (Automatic Gain Control), like Fig. 1-6, and bringing the benefits of automation such as high speed and identical accuracy.

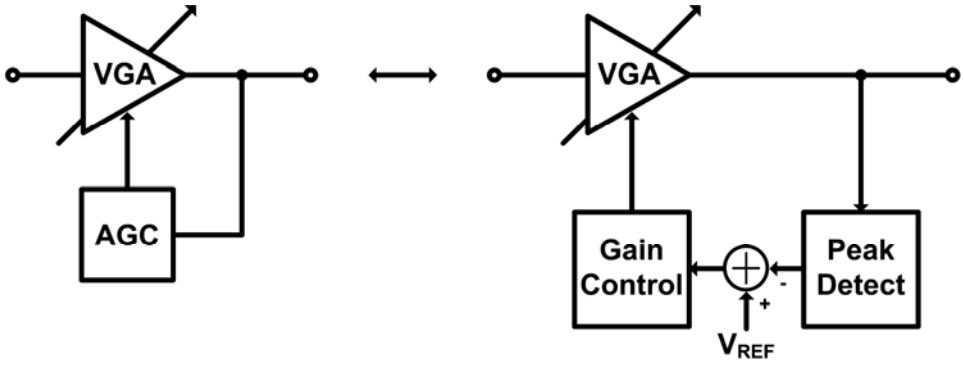


Fig. 1-6 Detailed blocks of AGC

AGC circuits roughly could be categorized into two kinds; one is continuous VGA with analog gain control loop, and the other is discrete gain step VGA with digital controller. For an AGC which is based on analog control

loop, it usually has some shortcomings, such as the trade-off between response time and gain stability, or inconsistent response time caused by gain non-linearity. A slow locking AGC needs a long preamble time before data transmission, and it degrades the channel efficiency in a different form.

On the contrary, a digitally controlled AGC, such as commonly-used 2-gain-mode TIA for bust mode transmission, usually has short response time; but it just has few gain modes, and brings the trade-off between dynamic rage and gain resolution, which is unfortunately a key point that a PAM system will focus on. So, now the problem is: Is there any solution for a fast locking, constant response time and high resolution AGC circuit with enough dynamic range?

In this research, the design and implementation of a digital controlled AGC circuit is proposed. The gain of VGA has 24 different gain modes between 20dB dynamic range; and the digital gain control circuit gets the appropriate thermometer code by binary/linear 2-mode searching engine, making the gain of VGA locked precisely and quickly, and also been stable in the long run. The detail specifications of this AGC are defined to satisfy a 4-PAM, 10Gbps optical receiver analog front-end, and a fully integrated optical transceiver with CMOS PD and laser diode in single chip is our prospect.

1.2 Overview of Thesis

In this thesis, design issues of the AGC will be divided into 5 chapters. And in chapter 1, the fountainhead and application of this AGC is given.

In chapter 2, some typical VGA techniques are introduced, and so are the pros and cons of these different categories. In order to take from the long to add to the short, the analysis of conventional AGC and architecture of proposed digital controlled AGC will be shown; and the specifications of this AGC could be figured out from the total optical receiver considerations.

Detail circuit design is in chapter 3. Schematics and design considerations of the AGC sub-circuits, such as VGA, peak detector, comparator, and digital gain controller circuit will be described respectively. Because quite a few critical issues are involved, analysis of VGA is emphasized in this chapter.

Experimental Results are shown in chapter 4, with the chip photo, test setting and measured results. Performances of this chip will be summarized in a table, and the benchmark will follow it.

Finally, a conclusion will be given in chapter 5.

Chapter 2 Architecture

2.1 AGC Architecture Overview

For the conventional analog controlled AGC loop, amplitude acquisition and adjustment usually occur during the preamble time of a data transition; but this duration should be optimized for an efficient use of the channel capability, or the degradation of channel efficiency will occur. However, if this duration is dependent on the input amplitude, the preamble time should be longer than the slowest one that can be achieved and seems no optimization for system performance. As a result, settling time of an AGC loop should be signal independent [2].

In this section, basic gain variation techniques and the conventional architecture of AGC will be introduced. The importance of linear-in-dB gain control in an analog controlled AGC loop for a constant settling time will be described in section 2.1.2. Since linear-in-dB gain variation has its own trade-off for fully CMOS design, the merits of the proposed AGC will be reflected.

2.1.1 Basic Gain Variation Prototypes

VGA plays an important roll in the AGC loop. Specifications like input referred noise, data rate and dynamic range are critically dependent on the performance of VGA. The critical issue of a VGA is how its gain is varied, and how the gain variation mechanism affects the properties mentioned above.

With common sense, an amplifier can be viewed as a combination of transconductance stage and transimpedance stage; this combination can not only be simple MOS with resistive load, but can also be complicated Gm cell with a feedback TIA. If the gain of the amplifier needs to be varied, either the effective Gm or the effective impedance will change. This concept can be represented by the prototype and an example in Fig. 2-1.

Fig. 2-1 shows a high gain amplifier and the resistive feedback network. If the high gain amplifier is presented as A(s), transfer function of the network can be simplified as the equation in the next page.

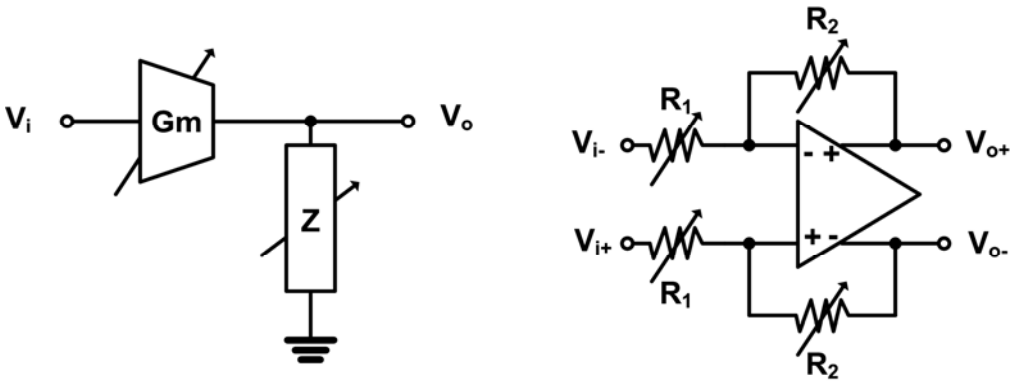


Fig. 2-1 Gain variation prototype and an example

$$V_o / V_i = -\frac{R_2}{R_1} \frac{1}{1 + \frac{1}{A(s)}(1 + \frac{R_2}{R_1})} \quad (1)$$

This gain can be varied by changing R_2 and/or R_1, which denote the effective Gm and impedance. In this circuit, large loop gain can provide high linearity for this circuit [3]; but if there is a dominated pole in the core amplifier, it's easy to see that the variation of the resistors will lead to variation of system bandwidth. Since there is a trade-off between gain and bandwidth, the dynamic range will critically depend on the bandwidth of the amplifier; as a result, power of the amplifier is hard to optimize when the best and worst cases are both covered, and so is phase linearity. To the author's knowledge, much of the VGA which are based on effective impedance variation faced the same problem. With common sense, if the transconductance stage is composed of active components, the system bandwidth will roughly be determined by the transimpedance stage. To avoid the defects mentioned above, a varied Gm stage with a constant transimpedance stage will be a better choice. In Fig. 2-2, two common effective Gm variation methods are introduced.

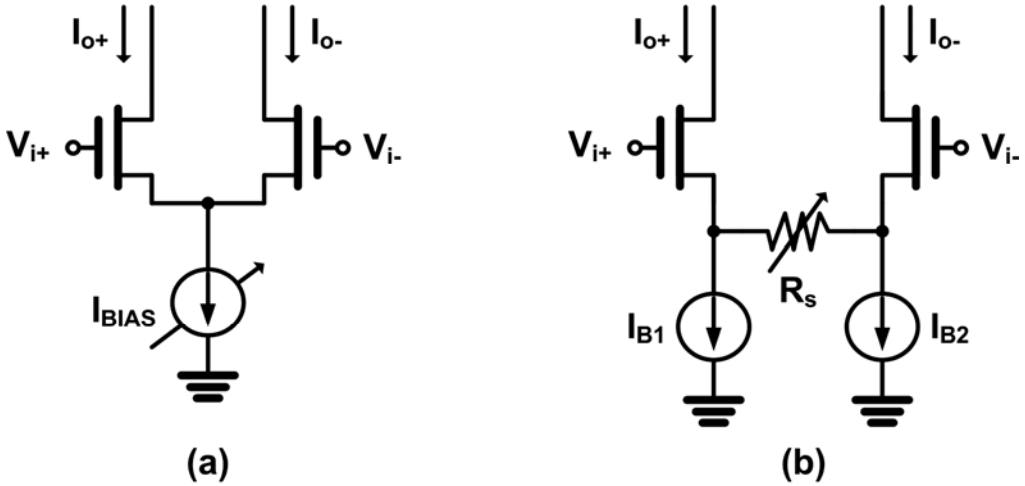


Fig. 2-2 Two Gm variation methods

In Fig. 2-2(a), transconductance of the source coupled pair varies if the bias current varies. As a result, the circuit gain can be varied by changing bias voltage V_c.

$$I_o / V_i = g_m \propto \sqrt{I_{bias}} \propto (V_c - V_{th}) \quad \textbf{(2)}$$

Different bias currents bringing different current summation might be a problem for DC value of the output nodes, but it can be solved easily by a Gilbert cell prototype, taking a source coupled pair as the biases and dual source coupled pair as the input stage. In this circuit, moreover, large bias current can provide high gain and low noise performance in high gain mode; but when the signal is large, the low bias current for low gain mode can degrade the linearity [3]. As another conception, there is a source coupled pair with degeneration resistor in Fig. 2-2(b), and transconductance of the source coupled pair varies as soon as the degeneration resistance R_s varies.

$$I_o / V_i = G_m \approx \frac{g_m}{1 + \frac{1}{2} R_s \cdot g_m} \approx \frac{2}{R_s} \quad \textbf{(3)}$$

When the input signal is small, high gain is obtained by small R_s and results in low noise performance. On the contrary, when the input signal is large, low gain is obtained by large R_s and brings high linearity. For this topology, it seems that there is a good tendency between signal, noise and distortion [3].

In the source degeneration prototype, the degeneration resistance and parasitic capacitance at source will generate a zero for the transfer function of this source coupled pair, and benefit the system bandwidth if design

appropriately; but it will be a problem that the varied degeneration resistance leads to zero location variation, and hence the phase response. Considering the noise and linearity performance, source coupled pair with degeneration resistor seems to be the better one, and the detailed discussion of its variation and transfer function will be described in Chap. 3.

2.1.2 Analysis of Analog AGC Model

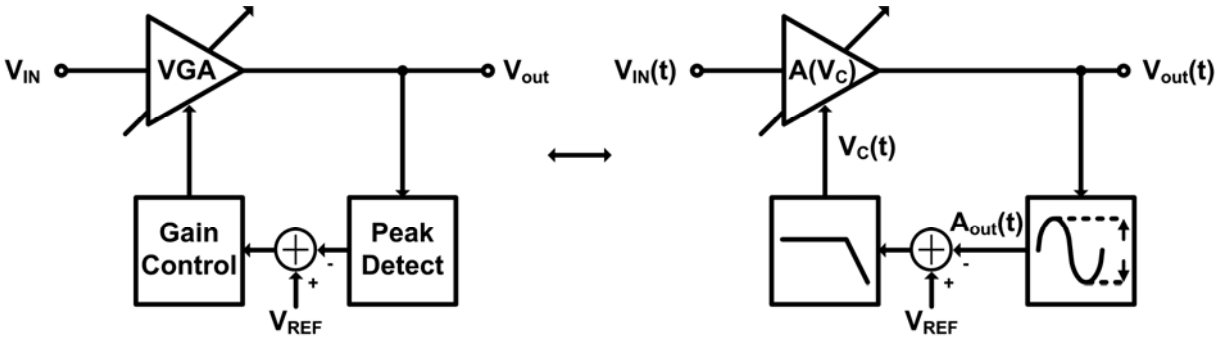


Fig. 2-3 Basic block diagram of an AGC loop

The basic block diagram of an analog AGC loop is shown in Fig. 2-3. A VGA provides tunable gain which depends on V_C for input signal, and the output peak amplitude A_{OUT} is acquired by the peak detector. After comparing peak amplitude to the reference voltage V_{REF}, the subtracting or comparing result can be adopted to determine the gain control signal V_C by the gain control circuit. Briefly said, if the peak amplitude is smaller than the reference voltage, gain control signal will bring the appropriate information to the VGA to get a higher gain, and vice versa.

For an analog-controlled VGA, conventionally the gain control circuit in Fig. 2-3 can be viewed as a loop filter and provides an analog voltage to control either bias current or resistance in the VGA, and hence the gain as mentioned in section 2.1.1. Taking a long term view, this loop filter always accumulates the difference result and provides a rather stable control voltage for the VGA to settle down, so an integrator like G_m-C filter is commonly used in this loop.

In following discussion, an AGC model based on Fig. 2-3 is presented to show how important it is to keep gain control signal and VGA gain linear-in-dB for a constant settling time and some other issues; and similar modeling method is used in [2].

In order to simplify the model for mathematical analysis without abandoning the core value of this loop, four presuppositions are given. First, signal and function of VGA will be transferred into logarithmic function for simpler equation representation; it means, an equation like

$$V_{OUT}(t) = A(V_C) \cdot V_{IN}(t) \tag{4}$$

can be presented as

$$\ln[V_{OUT}(t)] = \ln[A(V_C)] + \ln[V_{IN}(t)] \tag{5}$$

Second, assuming that this AGC loop only operates on and responds to signal amplitude; so the input and output signal of AGC are represented in terms of their amplitudes, $A_{IN}(t)$ and $A_{OUT}(t)$, to simplify the function of peak detector and the derivation. Third, for this analog loop, the gain control circuit is represented by an integrator whose time constant is τ_{int}. Last, a logarithmic amplifier will be included in the loop for this constant settling time derivation, as the dotted block shown in Fig. 2-4 in the next page. (If this logarithmic amplifier is omitted, the property of constant settling time can still exist under some small signal approximation. Please see Appendix A for details.)

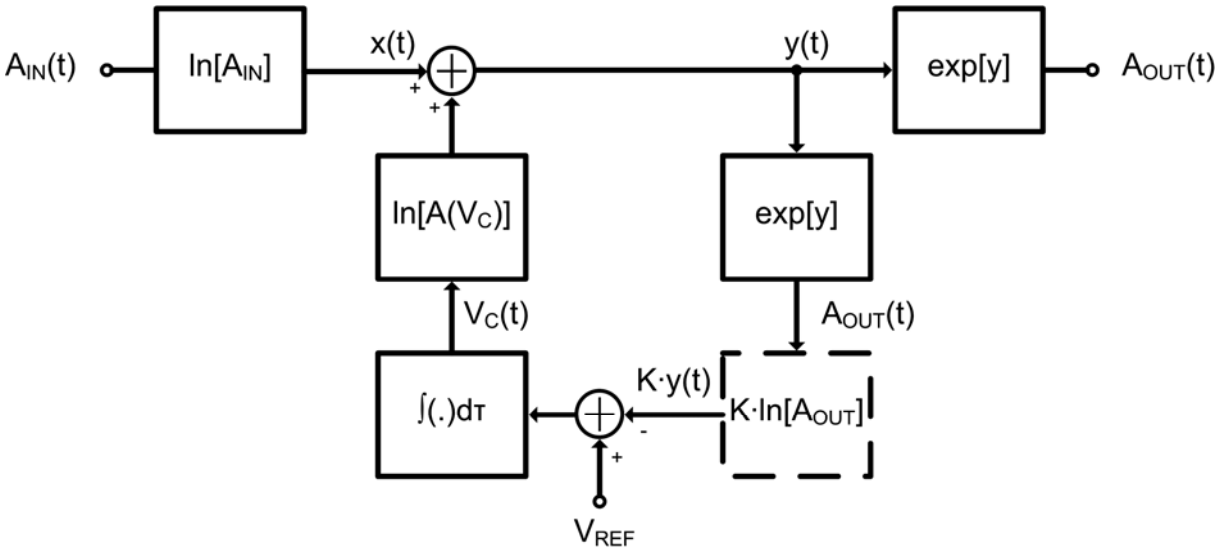


Fig. 2-4 Model for typical analog AGC loop

As shown in Fig. 2-4, x(t) and y(t) are A_{IN} and A_{OUT} in logarithm form,

$$y(t) = x(t) + \ln[A(V_C)] \tag{6}$$

and the gain control signal V_C is derived as

$$V_C(t) = \frac{1}{\tau_{\text{int}}} \int_0^t [V_{REF} - K \cdot y(\tau)] d\tau \tag{7}$$

where τ_{int} is the time constant of the integrator.

Taking the derivative of (6) and substituting the derivative of (7) into it (neglecting the constant of integration), the following equation can be derived:

$$\frac{dy}{dt} = \frac{dx}{dt} + \frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} \cdot \frac{1}{\tau_{\text{int}}} \cdot [V_{REF} - K \cdot y(t)] \tag{8}$$

If the coefficient of the second term of (8) is forced to be a constant C,

$$\frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} \cdot \frac{1}{\tau_{\text{int}}} = C \tag{9}$$

there will be a linear relationship between x(t) and y(t) under this assumption:

$$\frac{dy}{dt} + C \cdot K \cdot y(t) = \frac{dx}{dt} + C \cdot V_{REF} \tag{10}$$

and (10) could be transferred into frequency domain as

$$y = \frac{s}{s + C \cdot K} \cdot x + \frac{C}{s + C \cdot K} \cdot V_{REF} \tag{11}$$

Consequently, there is some information that could be acquired from (11). First, this equation shows a first order linear system. Because there is a high pass response from x to y, it can be understood as the high frequency component of output is determined by the input, like data transition. Second, the low frequency component of output is occupied by the second term of (11) due to the low pass response; another saying, the output amplitude is critically determined by the reference voltage; and that is what we want to see in an AGC.

Third, time constant of this system is

$$\tau = \frac{1}{C \cdot K} = \left[\frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} \cdot \frac{1}{\tau_{\text{int}}} \cdot K\right]^{-1} \tag{12}$$

where $A(V_C)$ is the function of VGA, τ_{int} is the time constant of integrator, and K is the gain of the logarithmic amplifier in Fig. 2-4. This time constant τ critically affects the settling time of this loop, data bandwidth, and noise performance.

To get a constant settling time with constant τ_{int} and K, the following constrain should be satisfied:

$$\frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} = C_2 \tag{13}$$

where C_2 is a constant. (13) can be represented as another form using the common integral knowledge:

$$A(V_C) = C_3 e^{C_2 V_C} \tag{14}$$

where C_3 is a constant for integration.

As a result, those derivations describe that a VGA whose gain is linear-in-dB to the control signal will leads to a constant settling time for the AGC loop, and this settling time is critically dependent on C_2 and τ_{int}. As a result, how to get a steeper slope in VGA transfer function for a quick settling, and the trade-off between amplitude stability and settling time caused by the loop filter, both are the problems that a conventional analog AGC loop faced.

2.1.3 Control Signal Techniques

Until now, VGA circuits based on multiple technologies such as bipolar, BiCMOS, and CMOS have been introduced worldwide, but due to the low cost consideration, CMOS is usually the preferred technology. However, it is difficult to realize the mentioned linear-in-dB relationship between gain and control signal, due to the square or linear characteristic function of CMOS transistor, in saturation or triode region respectively.

In order to keep the exponential function between control voltage and gain of the VGA in CMOS technology, pseudo-exponential functions [4] like

$$e^{2ax} \cong \frac{1+ax}{1-ax} \approx \frac{k+(1+ax)^2}{k+(1-ax)^2} \quad \textbf{(15)}$$

is a technique to realize this character. Using pseudo-exponential functions as the technique to control the bias current can provide a wide gain tuning range per stage, and this technique can not only be adopted in bias current control, but also in resistance variation [5]. But the square-law between I_D and V_{GS} may not stand for sure as the CMOS process scales down and short channel effects occur, this technique faces some problem in the lone run.

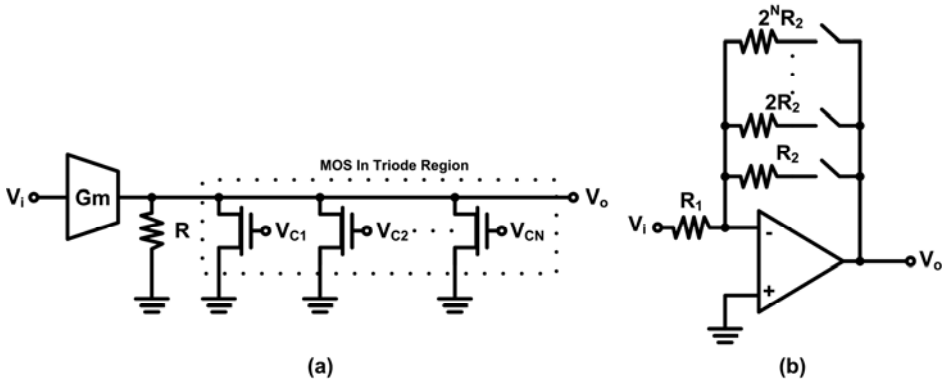


Fig. 2-5 VGA using successive approximation

For a VGA whose gain variation is based on output resistance variation, successive approximation [6] is the most commonly-used method to realize quasi-exponential function. But successive approximation, like Fig 2-5(a), needs a large number of transistors in parallel at the output node to get a large linear range, and the parasitic capacitance and bandwidth variation will be the severe problem for a high speed VGA. Fig 2-5(b) shows a similar concept in digital type, and faces the similar problem.

Recently, exponential voltage generator which is using parasitic bipolar transistor in CMOS technology has been announced [7]; the exponential I-V characteristic of the bipolar transistor is helpful and convenient to introduce a linear-in-dB VGA; however, this characteristic is strongly dependent on the temperature and needs temperature compensation circuit [8] for a robust design.

Similarly, transistor operating in a sub-threshold region is another similar method to provide exponential relationship, but it's also face noise and variation immunity problems. As the analog AGC face the problems, such as control signal difficulties and trade off between settling time and amplitude stability, digital controlled AGC seems to be a way to ease the problems, and gets the benefits as the processes scaled down.

2.2 Design Considerations and Specifications

2.2.1 Proposed AGC Architecture

For fast and constant setting time without noisy gain control signal, analog AGC loop which provides linear-in-dB character will face some problems as mentioned in section 2.1.2 and 2.1.3; on the contrary, a digital gain control circuit can easily avoid these difficulties and will not be critically dependent on the process' scale. Moreover, there are some algorithm can be applied in the digital gain controller to enhance the locking speed, such as binary search. So, the proposed digital-controlled AGC architecture is shown in Fig. 2-6:

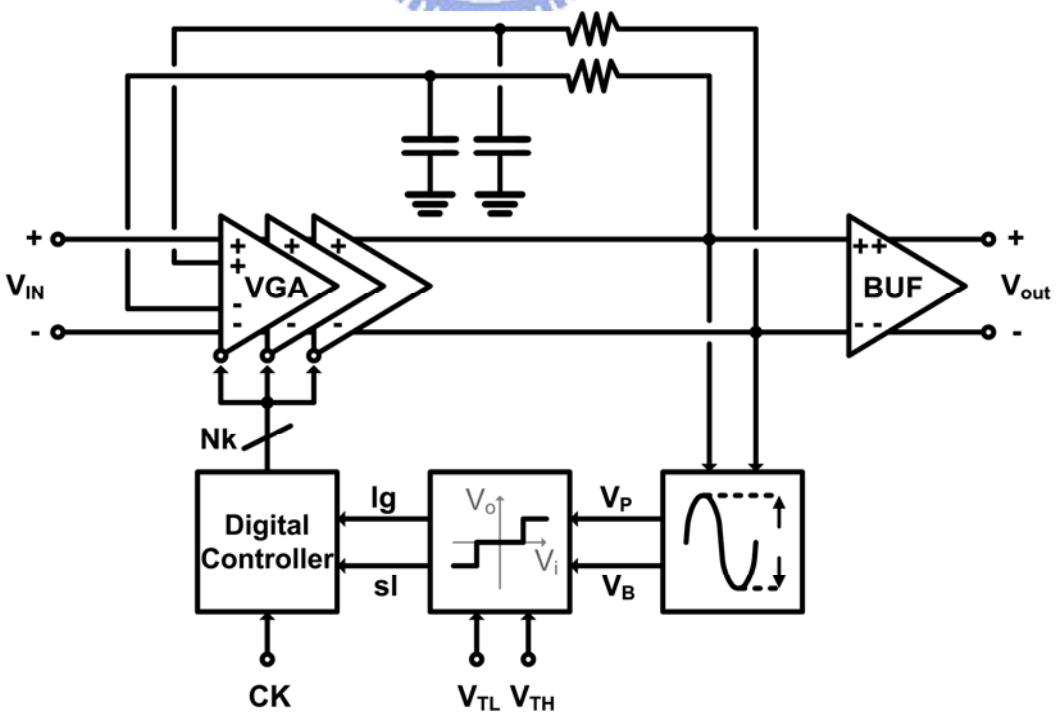


Fig. 2-6 Proposed digital-controlled AGC architecture

In Fig. 2-6, digital-controlled VGA are N-stage cascaded to provide enough dynamic range, and each stage is controlled by k bits digital signal. DC offset problem is killed by the feedback loop containing a low pass filter. Peak and bottom value of output amplitude, V_P and V_B, are acquired by the peak detector; and after comparing the output swing to the threshold voltages V_{TH} and V_{TL}, the information that the digital controller needs can be given by the results, lg (large) and sl (small).

Due to a bi-state comparator can just only recognize either large or small, and will be hard to bring a steady state for the digital controller; a tri-state comparator is adopted here, to compare the output swing to the threshold voltages. If the output swing is between V_{TH} and V_{TL}, the comparing result will stop at the third state, and the controller will not receive any information for gain variation.

After using a digital controller as the loop filter, the settling time of this AGC is determined by the time spending on amplitude acquisition and gain-control code searching. In order to look for the proper gain-control code quickly, a binary search engine is included in the controller; however, input swing may vary after the binary searching period, so a linear searching engine is added into the controller as a digital loop filter, for the stability concern in the long run view.

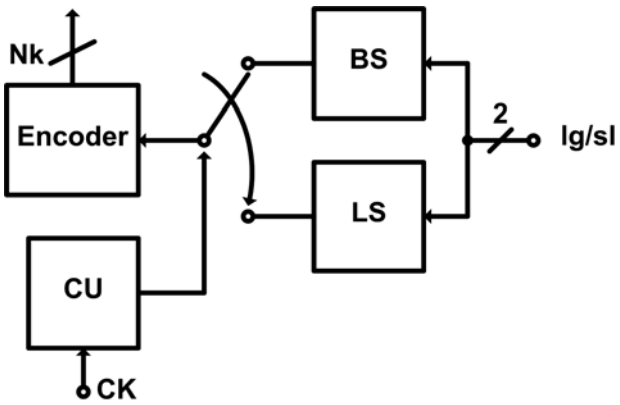


Fig. 2-7 Block diagram of proposed digital controller

Like Fig. 2-7, using a CU (Control Unit) as clock generator and changing the searching mode from BS (Binary Search) to LS (Linear search), both the fast response and long time stability concerns can be kept. After the two search engine, Nk bits gain control code applied in this VGA can be determined in the encoder according to the searching results of the two engines.

2.2.2 Specifications of AGC

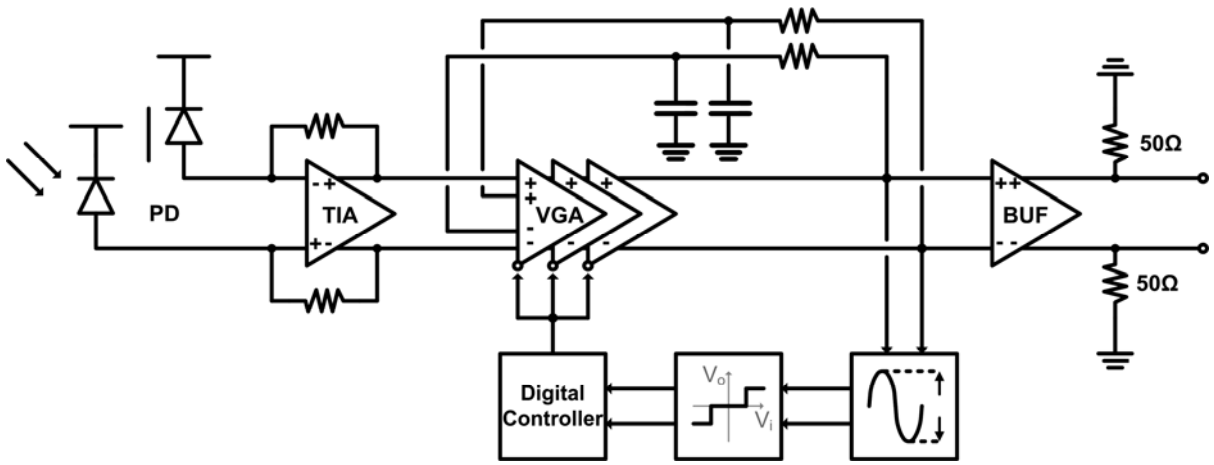


Fig. 2-8 Prospective optical receiver front-end

Fig. 2-8 illustrates the prospective single chip optical receiver analog front-end for a PAM system. It is composed of on-chip CMOS photo detector, a transimpedance amplifier, and the proposed automatic gain control circuit.

Concerning the bandwidth limitation of CMOS PD that is reported to date, a transmission using 4-PAM encoded data to reach 10 Gbps rate (symbol rate of it is 5 GS/s) is the reasonable choice. As a result, the target bandwidth of this VGA is 5 GHz for less ISI (Inter-Symbol Interference); and in order to compromise the trade-off between ISI and noise performance, bandwidth of TIA should be near the symbol rate in this PAM system.

Input referred noise of this receiver is the summation of input referred noise of TIA and that of VGA divided by TIA gain; with a high gain and low noise

TIA, the noise contribution of the VGA will not be the critical problem. For a PD whose sensitivity is about 11.5dBm at 10^{-12} bit error rate, the sensitivity of the VGA can be derived and is about 20mV.

In general, the maximum input optical power generate by a VCSEL is 0dBm, and assuming the insertion loss is for the channel is less than -10dBm; under these two assumption, it will reveal that the input power will be in the range of 100~1000μW. And if the receiver operates with a CMOS photo detector whose responsivity is 0.1A/W, the specification of this system can be planned and summarized in the following table:

Parameter	PD	TIA	VGA	BUF
Gain	0.1A/W	70dBΩ	4~24dB	>-6dB
Bandwidth	---	~5GHz	5GHz	>5GHz
Sensitivity@ BER=10^{-12}	<-11.5dBm	<8 μA_{pp}	<20mV_{pp}	---
Target Input	-10~0dBm	10~100 μA_{pp}	32~320mV_{pp}	500mV_{pp}

Table 2-1 Specifications of perspective optical receiver

Briefly said, dynamic range of this VGA should be about 20dB, and providing a voltage gain from 4dB to 24dB, to deliver 500mV_{pp} output swing to drive the succeeding stage. A buffer with 50Ω loading is added into the system for testing and measurement, and its design issue is focused on the bandwidth and phase response, rather than its gain and power.

Another specification of the AGC should be specified is the setting time; but without any public standard, the target settling time of this proposed AGC should be analysis before it has defined.

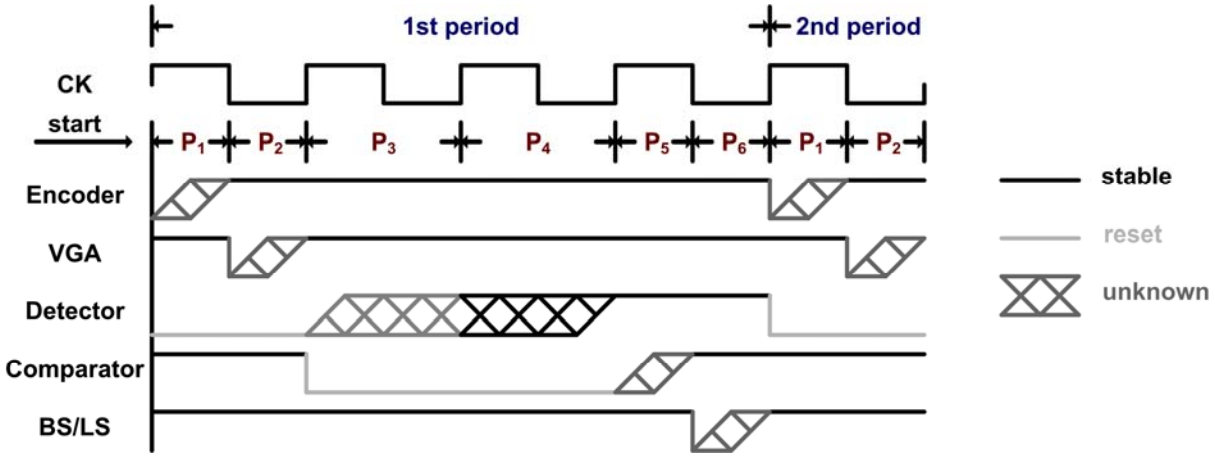


Fig. 2-9 Timing sequence

Fig. 2-9 illustrates the timing sequence of the proposed AGC loop. One time gain mode searching will be accomplished in one period, and how many periods it will take for binary search and linear search will depend on the design of search engine. In each period, there will be 6 major processes should be done, denoted as P_1 to P_6 in Fig. 2-9. They are (1) encoding, (2) VGA gain settling, (3) fast amplitude acquisition, (4) acquired amplitude settling, (5) comparing output swing to reference voltage and (6) gain mode searching.

In P_1, reset signal or result of search engine will give the information to encoder and determine what the gain control bits will be. The falling edge of the first clock in each period will be taken for encoder output synchronization.

In P_2, the negative edge of the first clock is planned for VGA settling. After the gain control bits change, VGA will take a response time to settle down its output swing, and this task will be finished during P_2.

For acceleration, amplitude acquisition in the detector can be divided into two sub-processes; the first one is “reload” (P_3), it means that amplitude acquisition in the peak detector will not have any low pass filtering effect in this time but just charging the capacitors; this sub-process focuses on the speed, rather than the stability. The second process is “LPF” (P_4), which indicates low pass filtering. Because the acquired output swing should be steady for succeeding comparison, there should be a low pass filter after the peak amplitude detection, making the acquired amplitude comes into a stable value. The function of this low pass filter is wished to be turned on after detector reload, and it takes some time to filter the noise; so it needs 2 clock for the detector which are denoted as P_3 and P_4 in Fig. 2-9, and spends half of the time in each period.

The last clock time in one period is planned for comparator and search engine. After the amplitude detection is over, steady output swing can be compared to the reference voltage; because the succeeding controller is a digital one, there should be a latch in this comparator for synchronization. Due to the clock falling edge can be planned for latching, searching engine can take the negative half clock period for responding time. Generally, the critical processes which cost most of the time in one period are P_3 and P_4; it will take a lot of time for charging and being stable. Concerning the trade-off between charge speed

and accuracy of amplitude acquisition, the target clock rate is 100MHz for a comparable settling time without peak detector design difficulty. Total settling time will be about 100~200ns if the binary search comes into an end after 3~5 searching period, and this becomes the design target.

Chapter 3 Design and Implementation

3.1 Variable Gain Amplifier

In this section, design considerations and analysis of the VGA will be introduced. The proposed nested active feedback architecture, digitally tunable resistor for digital-controlled gain variation, and low pass filter for offset cancellation will be described respectively

3.1.1 Proposed VGA Architecture

From the viewpoint of high frequency and high linearity operation which is required in a PAM receiver, the VGA prototype which is based on source degeneration variation is superior among the types of VGA that are presented; due to the effective transconductance is more linear for large input, and zero generated by the degeneration impedance may benefit the frequency response, providing a wide bandwidth for this transconductance amplifier.

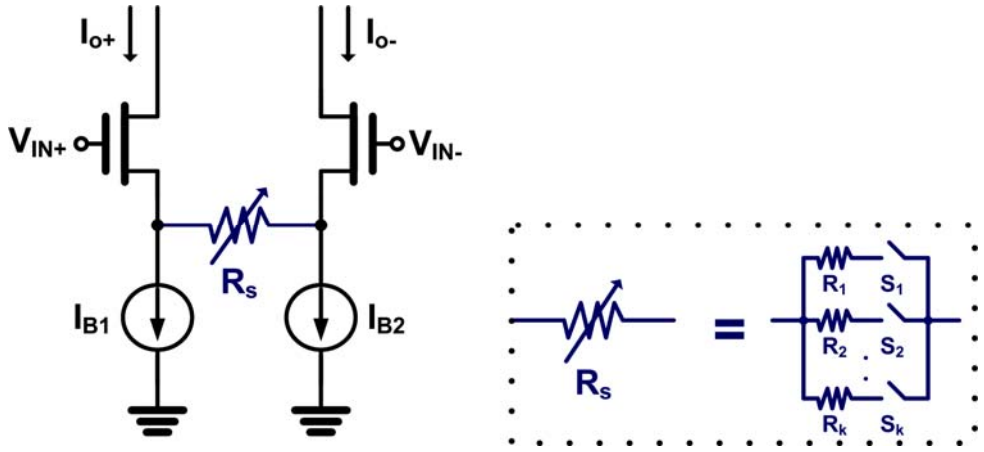


Fig. 3-1 Digital-controlled VGA based on source degeneration prototype

Under this consideration, the digital-controlled VGA based on source degeneration prototype is adopted in this design, like Fig 3-1; but it seems to face two critical problems. First, it is a question how to construct a digital-controlled resistor as the degeneration resistance and provide enough dynamic range with high resolution; the second one is how to enhance phase linearity in the defined bandwidth and so as to solve the severe zero frequency variation that may occur.

Design consideration for the first problem will be declared next to the following section, and that for the second problem will be described as following. For a design which achieves multi-Giga Hz bandwidth, the succeeding impedance stage of this transconductance amplifier should provide both wide bandwidth and moderate gain. But, there will be an obvious difficulty to achieve this goal in 0.18μm process if there is just a passive resistor on it; so an active element such as feedback TIA is a solution for this design. Moreover, for a broadband amplifier to avoid a lower loop gain caused by the paralleled

passive resistive feedback to the resistive load of the amplifier, active feedback is recognized as a better choice to ease this difficulty.

Consequently, active feedback is a useful technique to enhance the gain-bandwidth product [9]. As a result, the prototype of the proposed VGA becomes in Fig 3-2. Generally, the bandwidth of this prototype will be limit by the feedback TIA; in order to provide a wild bandwidth for entire response, -3dB bandwidth of the core amplifier in the TIA ("A" in Fig 3-2) should be more than that. However, it seems that any conventional differential pair without inductive peaking or feedback mechanism is hard to achieve a multi-Giga Hz bandwidth; so the active feedback technique is applied in the core amplifier once again for inductor-less concern, and bring the birth of nested active feedback.

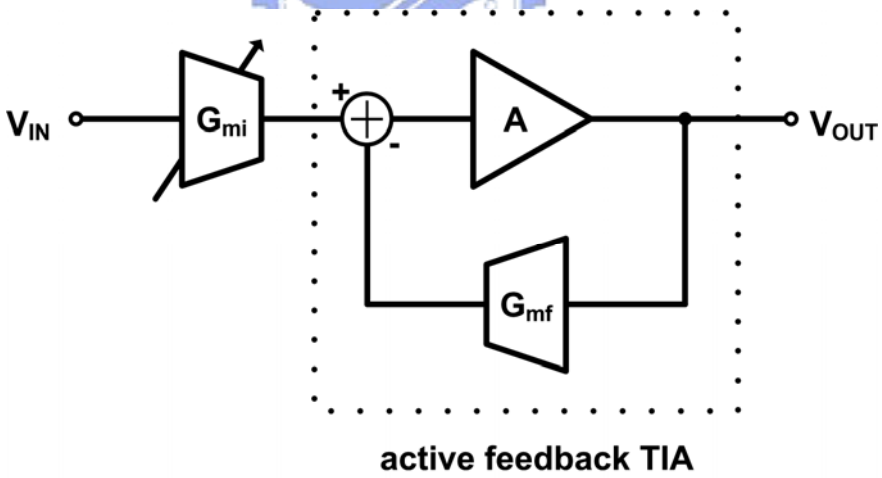


Fig. 3-2 Equivalent block of proposed VGA prototype

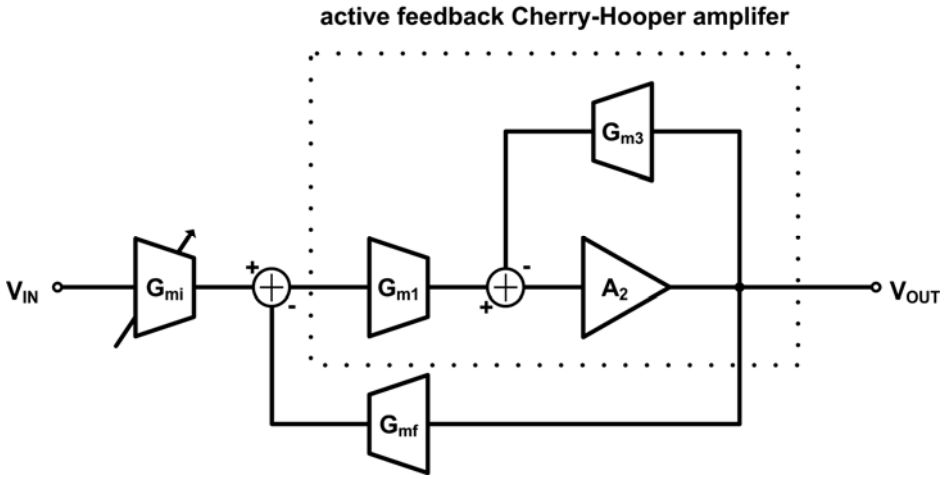


Fig. 3-3 Proposed nested active feedback

Above figure shows the proposed nested active feedback; gain of this VGA is varied as the degeneration resistance of input transconductance stage varies, and a TIA which is based on a core Cherry-Hooper amplifier and active feedback is adopted in this design, to provide a wide bandwidth with moderate gain and dominate the phase response in this structure. For frequency domain compensation and bandwidth issue, active feedback component G_{mf} in this structure is accomplished by the source degeneration pair, which is similar as the input transconductance stage.

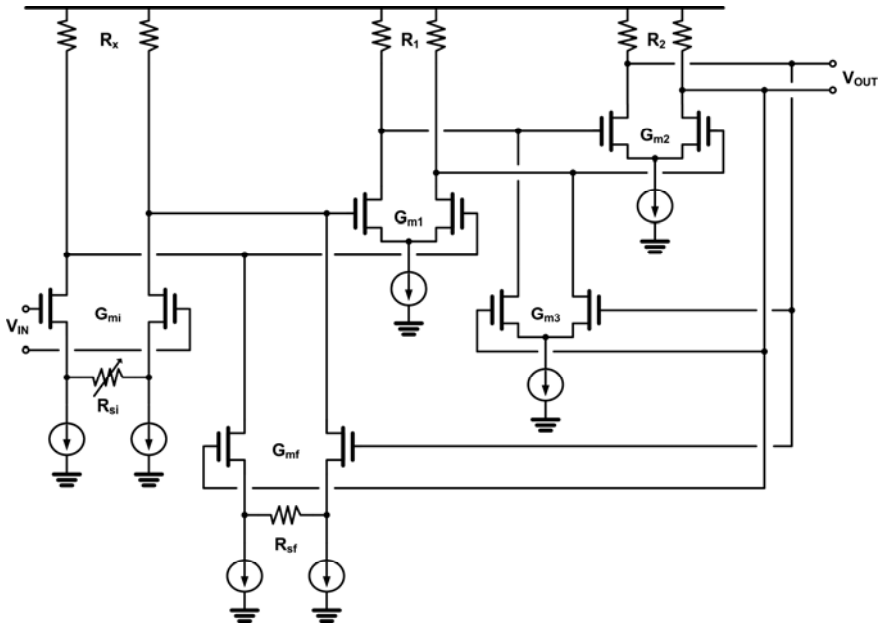


Fig. 3-4 Detailed schematic of Nested active feedback

3.1.2 Analysis of Nested Active Feedback

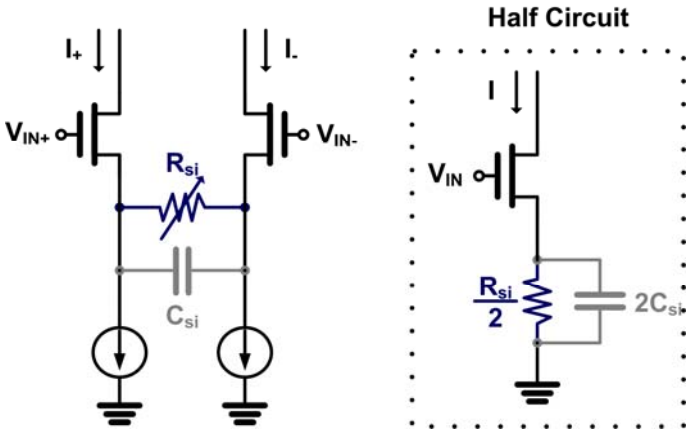


Fig. 3-5 Half circuit of source-coupled pair with degeneration resistance

Before analyzing the total transfer function of the nested active feedback structure, transfer function of source-coupled pair with degeneration resistance and the Cherry-Hooper amplifier should be given first. Fig. 3-5 shows the half circuit of source-coupled pair with degeneration resistance. Due to the source degeneration impedance makes a feedback loop for the effective transconductance, the transfer function for V_{IN} to I is:

$$\frac{I}{V_{IN}} = G_m(s) \approx \frac{g_m}{1 + g_m(\frac{R_{si}}{2} // \frac{1}{s \cdot 2C_{si}})} \quad \textbf{(16)}$$

(16) can be reorder into:

$$G_m(s) \approx \frac{g_m}{1 + g_m(\frac{R_{si}}{2} // \frac{1}{s \cdot 2C_{si}})} = \frac{g_m(1 + sC_{si}R_{si})}{(1 + \frac{g_m R_{si}}{2}) + sC_{si}R_{si}} \quad \textbf{(17)}$$

$$G_m(s) \approx \frac{g_m}{1+\frac{g_m R_{si}}{2}} \cdot \frac{1+ s/\omega_z}{1+ s/\omega_p} \approx \frac{2}{R_{si}} \cdot \frac{1+ s/\omega_z}{1+ s/\omega_p} \text{ if } R_{si} >> \frac{1}{g_m} \quad \textbf{(18)}$$

$$\text{where } \omega_z = \frac{1}{R_{si}C_{si}} \text{ and } \omega_p = \frac{1+\frac{g_m R_{si}}{2}}{R_{si}C_{si}} >> \omega_z$$

(18) shows that the transfer function of source-coupled pair with degeneration resistance can be simplified into a one-pole-one-zero system, the zero is determined by the RC time constant of the degeneration impedance, and the distance from zero to pole is related to the transconductance and degeneration resistance.

After the source degeneration pair, transfer function of Cherry-Hooper amplifier is going to be shown, and this analysis is similar as [9].

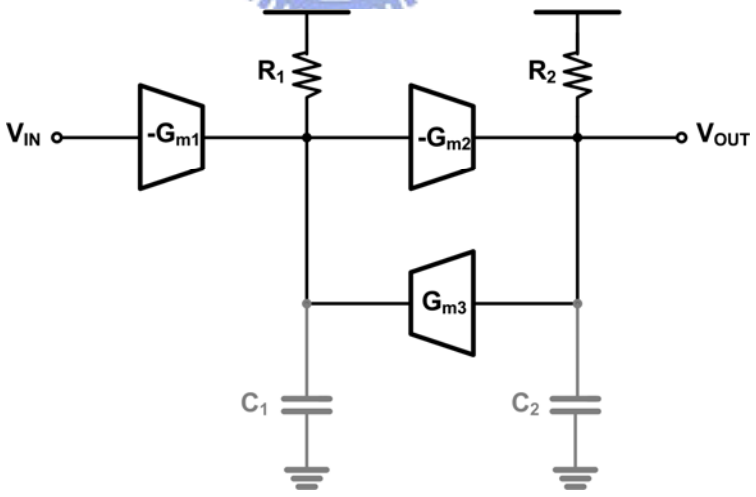


Fig. 3-6 Architecture of Cherry-Hooper amplifier with active feedback

Fig. 3-6 shows the model of common active feedback, and its transfer function can be easily figured out by KCL and KVL:

$$\frac{V_{out}}{V_{in}} = A(s) = \frac{G_{m1}G_{m2}R_1R_2}{(R_1R_2C_1C_2)s^2 + (R_1C_1 + R_2C_2)s + (1 + G_{m3}G_{m2}R_1R_2)} \quad \textbf{(19)}$$

(19) indicates that this transfer function is a two-pole system, so it can be represented as:

$$A(s) = A_{v0}\frac{\omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}}$$
$$where\ A_{v0} = \frac{G_{m1}G_{m2}R_1R_2}{1 + G_{m3}G_{m2}R_1R_2} \approx \frac{G_{m1}}{G_{m3}} \quad \textbf{(20)}$$
$$\zeta = \frac{1}{2}\frac{R_1C_1 + R_2C_2}{\sqrt{R_1R_2C_1C_2(1 + G_{m3}G_{m2}R_1R_2)}}$$
$$\omega_n = \sqrt{\frac{1 + G_{m3}G_{m2}R_1R_2}{R_1R_2C_1C_2}}$$

and this equation represents that the -3dB frequency of this amplifier will be related to the natural frequency ω_n.

After (18) and (20) this two presuppositions, the total transfer function of VGA can be derived.

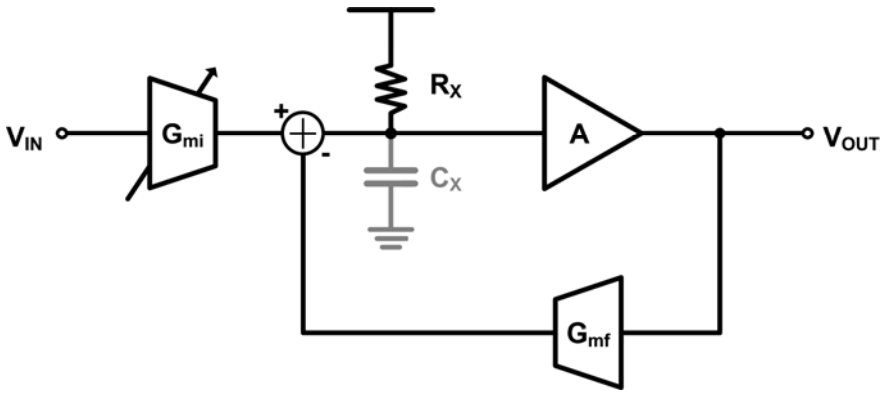


Fig. 3-7 Nested active feedback diagram

Assuming the loading of the input transconductance and active feedback stage are R_x and C_x, as shown in Fig. 3-7, the total transfer function of this nested active feedback structure is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_x(s)\cdot A(s)\cdot G_{mi}(s)}{1+Z_x(s)\cdot A(s)\cdot G_{mf}(s)}$$
$$where\ Z_x(s) = (R_x \,//\, \frac{1}{sC_x}) = \frac{R_x}{1+sR_xC_x} = \frac{R_x}{1+\frac{s}{\omega_{px}}} \quad \textbf{(21)}$$

Substitute (18) and (20) into (21), following equation can be derived:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_{sf}}{R_{si}}\cdot \frac{(1+\frac{s}{\omega_{zi}})(1+\frac{s}{\omega_{pf}})}{(1+\frac{s}{\omega_{zf}})(1+\frac{s}{\omega_{pi}})+\frac{1}{A'}\cdot(1+\frac{s}{\omega_{px}})(1+\frac{s}{\omega_{pi}})(1+\frac{s}{\omega_{pf}})(1+\frac{2\zeta}{\omega_n}s+\frac{s^2}{\omega_n{}^2})} \quad \textbf{(22)}$$
$$where\ A' = A_{v0}\cdot G_{mf}(0)\cdot Z_x(0)$$

in this equation, the suffix "i" or "f" means this component belongs to G_{mi} or G_{mf} , respectively; and ω_{px} is the inverse of time constant generated by R_x and C_x, A' denotes the loop gain of the active feedback TIA with input loading. This equation represents a fifth order system, and in order to optimize its phase response, some assumptions should be taken before further analysis.

To optimize this transfer function, it's not a good choice to find the exact equation of its phase response, because it's very complicated to do response differentiation and succeeding Taylor series approximation, needless to say how difficult to solve the simultaneous equations. In order to simplify the succeeding analysis, let

$$g_m \cdot R_s >> 1$$
$$\omega_{pi}\ , \omega_{pf} >> \omega_{Normalize} \quad \textbf{(23)}$$

$\omega_{Normalize}$ denotes the system bandwidth. Due to the pole of the source coupled pair with degeneration resistor is far from the zero if g_mR_s is much larger than one, this assumption in (23) is reachable. As a result, (22) can be simplified into:

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{R_{sf}}{R_{si}} \cdot \frac{(1+\frac{s}{\omega_{zi}})}{(1+\frac{s}{\omega_{zf}})+\frac{1}{A'}\cdot(1+\frac{s}{\omega_{px}})(1+\frac{2\zeta}{\omega_n}s+\frac{s^2}{\omega_n{}^2})} \quad \textbf{(24)}$$

(24) reveals some information. First, the zero of the feedback transconductance cell will become one of the major poles; it's easy to know that ω_{zf} is hard to ignore for a moderate gain and leads to that R_{sf} dominates the system gain. Second, DC gain of this system depends on the ratio of R_{sf} and R_{si} and A' (loop gain of feedback TIA with input loading); a big A' will lead to a higher gain, but will certainly get a smaller ω_{zf} , ω_{px} or ω_n due to the trade-off between gain and bandwidth, and benefits no bandwidth performance.

To optimize the phase response, considering that Bessel type filter is the generally acknowledged filter which has the most linear phase; as a result, the denominator coefficients of the nested active feedback transfer function are going to correspond to a third order Bessel filter, whose general type is:

$$T(s) = \frac{C}{1+1\cdot s+\frac{2}{5}\cdot s^2+\frac{1}{15}\cdot s^3} \quad \textbf{(25)}$$

As we expanding (24) as (26):

$$\frac{V_{OUT}}{V_{IN}} \approx \frac{R_{sf}}{R_{si}} \cdot \frac{(1+\frac{s}{\omega_{zi}})}{a+b\cdot s^1+c\cdot s^2+d\cdot s^3}$$

$$\text{a} = (1+\frac{1}{A'})$$

$$\text{b} = (\frac{1}{\omega_{zf}}+\frac{1}{A'\cdot\omega_{px}}+\frac{2\zeta}{A'\cdot\omega_n}) \quad \textbf{(26)}$$

$$\text{c} = (\frac{2\zeta}{A'\cdot\omega_{px}\cdot\omega_n}+\frac{1}{A'\cdot\omega_n{}^2})$$

$$\text{d} = \frac{1}{A'\cdot\omega_{px}\cdot\omega_n{}^2}$$

and comparing (25) and (26), it shows that if the design parameters satisfying the following simultaneous equations, the phase response will be the most linear one.

$$\begin{cases} \dfrac{1}{(1+\frac{1}{A'})\cdot\omega_{zf}}+\dfrac{1}{(1+A')\cdot\omega_{px}}+\dfrac{2\zeta}{(1+A')\cdot\omega_n}=1 \\ \dfrac{2\zeta}{(1+A')\cdot\omega_{px}\cdot\omega_n}+\dfrac{1}{(1+A')\cdot\omega_n{}^2}=\dfrac{2}{5} \\ \dfrac{1}{(1+A')\cdot\omega_{px}\cdot\omega_n{}^2}=\dfrac{1}{15} \end{cases} \quad \textbf{(27)}$$

Due to the number of variables is more than that of equations, assuming that the damping factor is 0.7 to get a flat gain response for the Cherry-Hooper amplifier, and A' is equal to 1 to get a balance contribution between gain and bandwidth. Under these assumptions, the design parameters can be derived and summarized in the following table.

Parameter	A'	ξ	ω_{zf}	ω_{px}	ω_n
Value	1	0.7	1.39	4.11	1.35

Table 3-1 Ideal nested active feedback parameters

Notice that the ω parameters are normalized to the system bandwidth, 5GHz. Another design parameter that should be specified is ω_{zi}. Varied R_{si} will lead to a varied ω_{zi}, this situation is hard to avoid; but if the frequency variation of ω_{zi} is far from the system pole, the in-band variation will be reduced. As a result, assuming that the frequency of ω_{zi} is farther than that of $\omega_{Normalize}$, the varied zero frequency will not affect the phase linearity severely, and this assumption becomes a guide line to design the digital tunable resistor.

The parameters of the transfer function become the rule of thumb for this design; and the normalized frequency, $\omega_{Normalize}$, should be more than 5 GHz to meet the specification if there is more than one stage cascaded. "The bandwidth of core amplifier is wider than the system", this summarization closely meets our initial guessing; but in real case, the pole frequency is hard to be 4 times the normalized frequency. To compromise this difficulty, enhancing the bandwidth of the core amplifier (a larger ω_n) can make up this insufficiency, and taking the zero into account; it comes with an acceptable phase performance.

Parameter	A'	ξ	ω_{zf}	ω_{px}	ω_n	ω_{zi}
Value	1	0.7	1.39	1	3.5	1.3

Table 3-2 Designed nested active feedback parameters

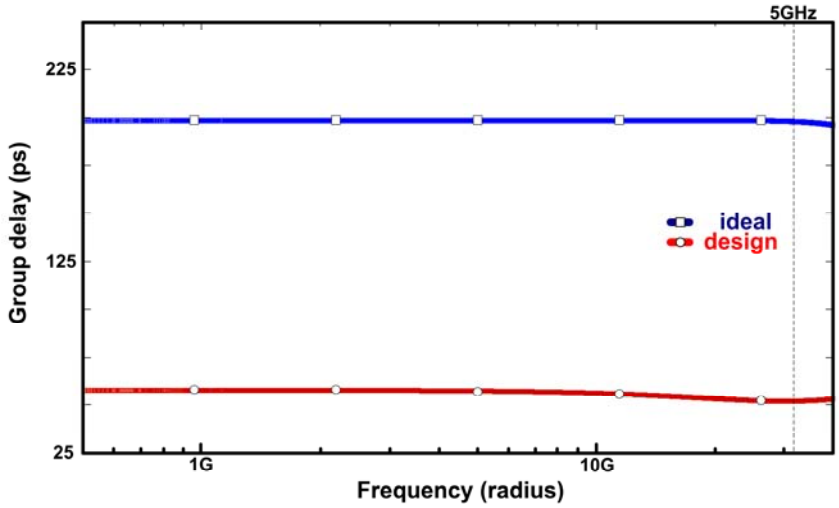


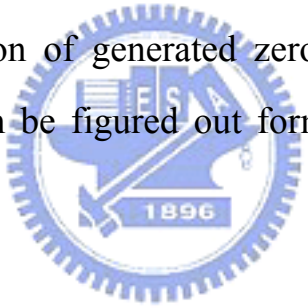
Fig. 3-8 Group delay response of nested active feedback

Above figure shows the group delay response with ideal parameters and the designed case; the group delay in real design case can be without too much variation, about 10 percent within 5GHz when ω_{zi} is designed as Table 3-2. The variation of ω_{zi} will leads to a noticeable group delay variation, and this phenomenon is hard to cancel as the source degeneration prototype is adopted; however, it could provide ω_{zi} about 4dB variation range for the group delay variation less than 100ps. in a similar MATLAB simulation.

3.1.3 Digitally Tunable Resistor

After the analysis of the nested active feedback prototype, realization and design issue of the digitally tunable resistor is going to be described.

A typical digital-controlled resistor is composed of switches and resistors in series or parallel; however, a common CMOS switch is hard to be ideal because of the trade-off between turn-on resistance and its parasitic capacitance. A large turn-on resistance will increase the risk of variation for the common resistors or degrade the resolution of gain variation (because turn-on resistance can be viewed as an offset); on the other hand, a large parasitic capacitance will critically affect the location of generated zero and hence the bandwidth and phase response, which can be figured out form (18) and (22) in the previous section.



Briefly said, there is a trade-off between dynamic range, resolution and parasitic capacitance for a resistor accompanying CMOS switch in series; on the contrary, using CMOS switches and their turn-on resistance as the digital-controlled resistor seem to be a better choice. The resistor turned on or not will determined by its overdrive voltage; if the gate-to-source voltage is larger than the threshold voltage, this resistor will be turned on and provide a turn-on resistance. The turn-on resistance will determined by the process parameter, gate-to-source voltage, and width divided by length of this transistor.

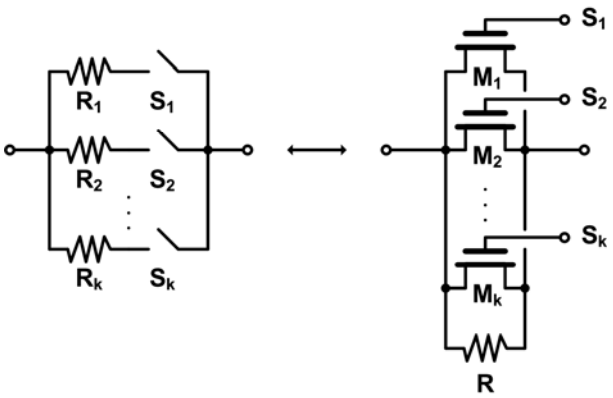


Fig. 3-9 Digital-controlled resistor

Fig. 3-9 shows the schematic of the digital-controlled resistor in this design. The transistors are combined in parallel, and gate voltage of them is equal to either operating voltage V_{DD} or ground. When the gate voltage of transistor M_i is V_{DD}, this transistor is turned on, and the effective resistance will critically depends on its width divided by length.

After putting the transistors with different width in parallel, total effective resistance is

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{\sum_{i=1}^{n} W_i}{L}[(V_{DD} - V_s - V_t)]} \approx R \cdot \frac{W}{\sum_{i=1}^{n} W_i} \quad \textbf{(28)}$$

and the index “n” represents the number of turned on transistor, V_s is the DC voltage of the resistor input/output node, R and W are just constants.

A common resistor R_N is combined with the transistors to get a better linearity performance, but it can be viewed as a transistor which is always turned on. As a result, (28) shows that the effective resistance R_{on} will critically depend

on the width of turn-on transistors, and the numbers of turned on transistor. Substituting (28) into (18) and (22) as "R_{si}", the relationship between VGA gain and this resistor will be:

$$gain = \frac{V_{OUT}}{V_{IN}} \propto G_{mi} \propto \frac{1}{R_{si}} \propto \sum_{i=1}^{n} W_i \tag{29}$$

In order to keep the gain variation linear-in-dB, the widths of the transistors are distributed in a geometric ratio and will be turned on in order, because

$$\begin{aligned} &\text{if } W_{j+1} = C \cdot W_j \Rightarrow \sum_{i=1}^{n} W_i = W_i \cdot \frac{(C^n - 1)}{C - 1} \\ &\log(\frac{V_{OUT}}{V_{IN}}) \propto \log(\sum_{i=1}^{n} W_i) \approx n \cdot \log(C) + \log(W_i) - \log(C - 1) \end{aligned} \tag{30}$$

(30) shows that gain will be dB-linear to "n", the number of turned on transistor. With this consideration, if the gain control signal is the thermometer code and control the gate voltage of these transistors, gain of the VGA will be dB-linear to the numbers of "1" in the thermometer code; or briefly said, gain is dB-linear to control signal, and that's expected in a VGA design.

Another design issue for this digitally tunable resistor is its parasitic capacitances. Based on typical CMOS knowledge, the parasitic capacitance of one node in this resistor will be

$$\begin{aligned} &C_{on} \approx \sum_{i=1}^{n} C_{GS} + C_{SB} + C_P \\ &\text{where } \sum_{i=1}^{n} C_{GS} = C_{overlap} + \frac{1}{2} \sum_{i=1}^{n} W_i \cdot LC_{ox} \end{aligned} \tag{31}$$

In (31), C_p represents the parasitic capacitance which is not belongs to the transistors in Fig. 3-9 but some other transistors that may connect to this node; C_{SB} represents that of source (or drain) to body. The summation symbol in front of C_{GS} indicates that it will depend on the total turn-on width, because the oxide capacitance will not exist if the gate voltage is not equal to V_{DD} but ground; if the transistor is turned off, the capacitance that will exist is only the overlap capacitance, which is caused by side-diffusion in the MOS.

From (28) and (31), the RC time constant of this node can be derived as

$$R_{on}C_{on} = RC + RC' \frac{W}{\sum_{i=1}^{n} W_i} \quad \text{(32)}$$

where $C' = C_{SB} + C_P + C_{overlap}$

$$C = W \cdot \frac{1}{2} \cdot LC_{ox}$$

(32) shows that the RC time constant will not increase as fast as the resistance increases. This indicates that the zero generated by this degeneration impedance will not vary as severely as the gain varies. It can be viewed as a self-compensation mechanism for zero location variation, and the ratio of this self-compensation is 10%~15% in this design, due to C_P is always the dominated term.

Concerning the trade-off between resolution and tuning range with acceptable parasitic capacitance, total number of parallel transistor in this digitally tunable resistor is 8 for one stage VGA; and 3 stages VGA are cascaded for enough dynamic range, which is about 20dB mentioned in section 2.2.2.

Under this consideration, each stage of the VGA provides about 6.6dB dynamic range, and each control bit will determine 0.8 dB gain variation; that is, if there is one more bit turned on, the updated gain will be 1.1 times the primitive one, and this information could be used to determine the ratio of the transistors.

3.1.4 Offset Cancellation

Due to process variation, temperature variation or components mismatch, DC offset may occur in the cascaded VGA and leads to unequal output DC voltage; this phenomenon will be more obvious in high gain mode if the input referred offset voltage is the same. In order to cancel the DC offset, a low pass filter is added from output to input stage; the detailed schematic is shown in Fig. 3-10.

A negative feedback path of DC voltage is generated by the RC low pass filter and a simple source coupled pair; if there is a DC offset and cause the DC value of V_{out+} is not equal to V_{out-}, the negative feedback path will adjust the DC value of node "A" and "B" in Fig. 3-10, and canceling the offset at the first stage.

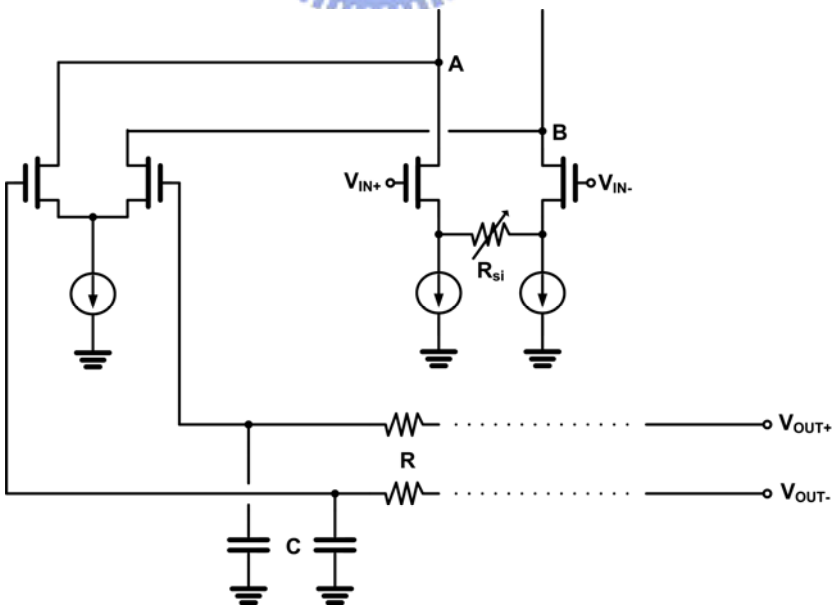


Fig. 3-10 Schematic of offset cancellation

Another way to express this mechanism, a feedback low pass response can be viewed as a high pass response for the VGA forward signal path, and the low -3dB pole of this high pass response is determined by the RC time constant. Because it is a high pass response for the forward signal, the gain of low frequency component, or briefly said, the DC gain will be restrained by the filter, and the DC offset caused by front stages will not be amplified from stage to stage, but attenuated, and leads to the offset cancellation.

Value of RC will determine how wide the pass band will be; large RC will provide a wide pass band but occupy the chip area. Concerning the specification, a RC filter which is composed of 150kΩ resistance and 30pF capacitance will provide enough pass bandwidth for the PRBS whose data rate is 10 Gbps, due to the low -3dB pole is less than 50 kHz.

3.1.5 Output Buffer

In order to drive the succeeding stage or the bounding pad for measurement, there is a buffer following the cascaded VGA. The input capacitance of this buffer can not be too large, or the parasitic capacitance will affect the response of the VGA. However, for the output impedance matching concern, the resistive loading in this prototype is 50Ω; taking the output swing specification into account, it's hard to use a conventional differential pair to achieve a small input capacitance buffer with appropriate gain.

As a result, the so-called ft-doubler is adopted in this design as the output buffer, and the schematic and equivalent diagram is shown in Fig. 3-11. Low pass filters are connected to the buffer input (VGA output), giving the DC value of buffer input to the dual source coupled pair. Compared to the conventional differential pair, a ft-doubler can reduce the input capacitance with comparable gain because the DC voltage is virtual ground for high frequency analysis, and the equivalent capacitance of two C_{gs} in series is half of it, as shown in Fig. 3-11.

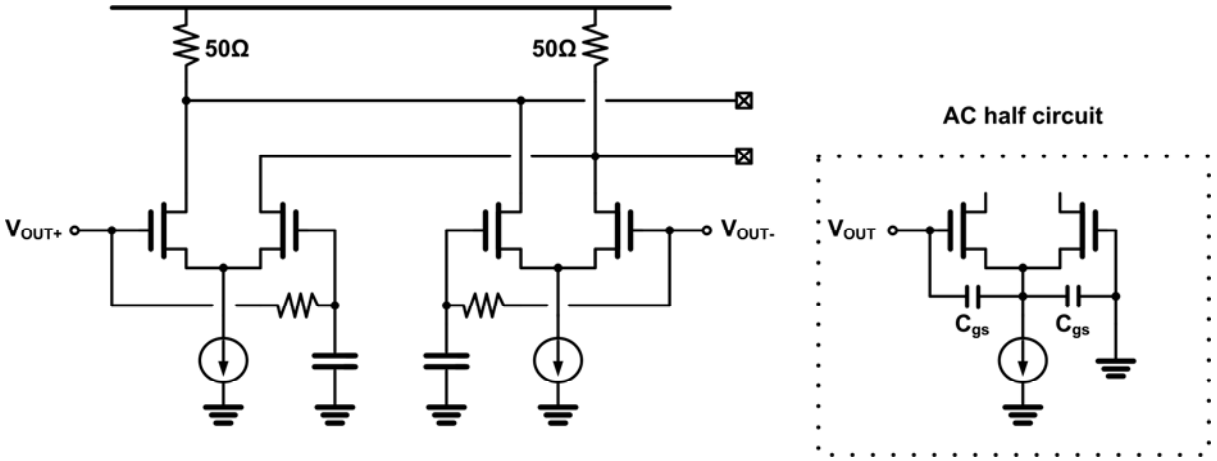


Fig. 3-11 Schematic and AC equivalent circuit of output buffer

A drawback of this circuit is the larger output capacitance, but due to the 50Ω resistive loading, the generated pole will not dominate the system response.

3.1.6 Simulation Results

From section 2.2.1 to section 3.1.5, the blocks, specifications, schematics and analysis of the amplifiers (including VGA and the buffer) are introduced. Depending on the design parameter in Table 3-2, the performance of the VGA with buffer can be shown in the following Fig. 3-12.

This is the post layout simulation result, with TSMC 0.18μm CMOS process. From this figure, it can be shown that the -3dB frequency is about 4GHz, and the group delay variation is less than 5ps within 4GHz. The 24 bits thermometer code will bring -2dB~17dB dynamic range (0.8dB/bit), and about 20ps group delay variation.

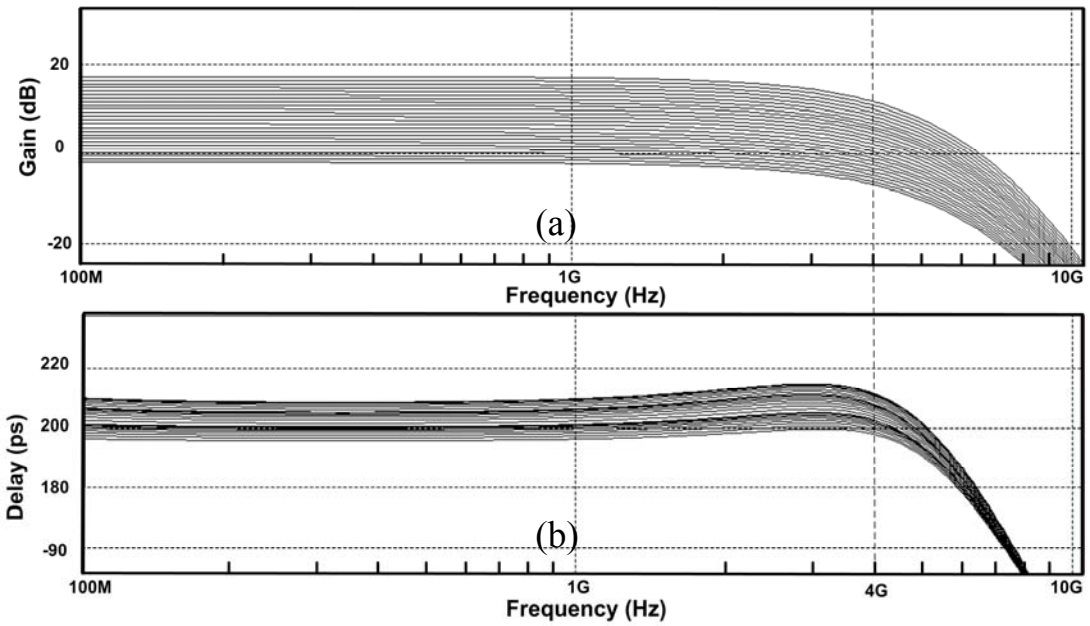


Fig. 3-12 Response of VGA with buffer (a) gain (b) group delay

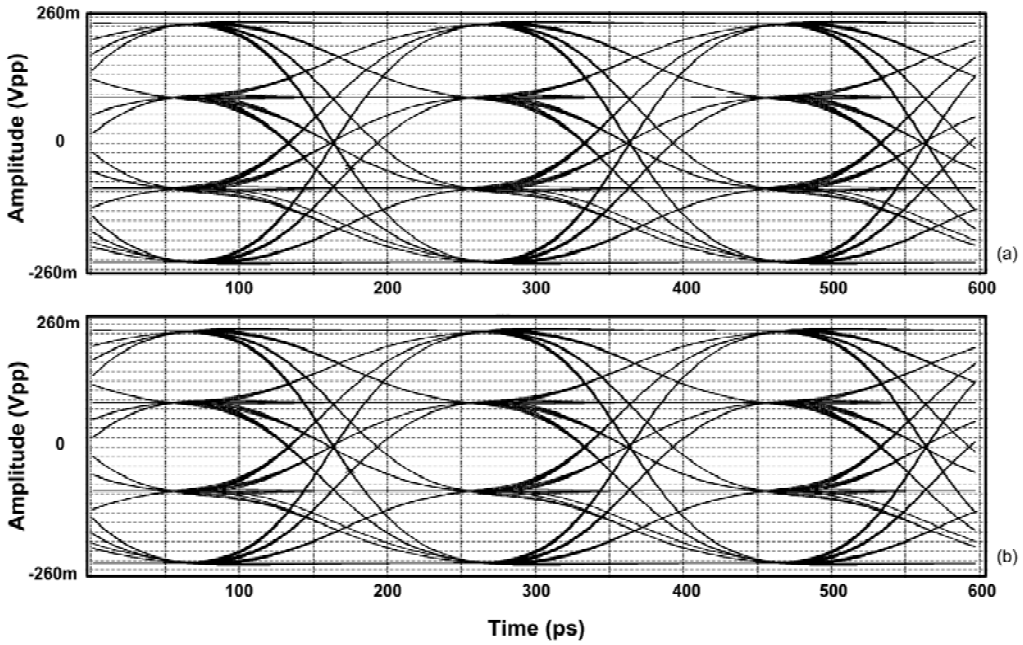


Fig. 3-13 4-PAM eye diagrams (a) high gain (b) low gain

3.2 Peak Detector

Utility of a peak detector is amplitude acquisition; the peak amplitude of the VGA output swing will be acquired in it and compared to a reference at the succeeding comparator. Because what is emphasized in this design is not the exact DC value of the VGA output voltage but the amplitude of swing, a peak hold circuit and a bottom hold circuit are adopted in this work to get peak and bottom value of the output; and the total amplitude will be represented by the difference of peak and bottom.

Diode is a useful component to get the peak value of a swing, because it can just be forward-conducting; if there is a diode connected with a capacitor, the peak value of voltage can be kept in the capacitor without a significant loss. A larger size diode commonly has a better charge ability due to its small equivalent resistance; however, larger leakage current may occur when the size is large. Considering the driving capability of the VGA, a large size diode may lead to large output capacitance and degrade the bandwidth,. As a result, a transconductance stage is adopted to drive the diode and capacitor, and the model of peak hold circuit in this design is shown in the following figure.

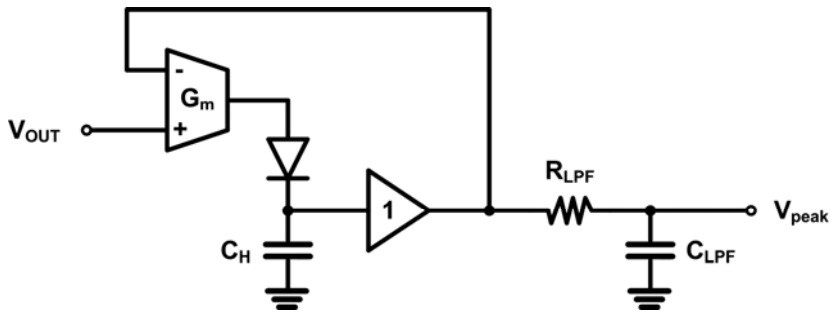


Fig. 3-14 Model of peak hold circuit

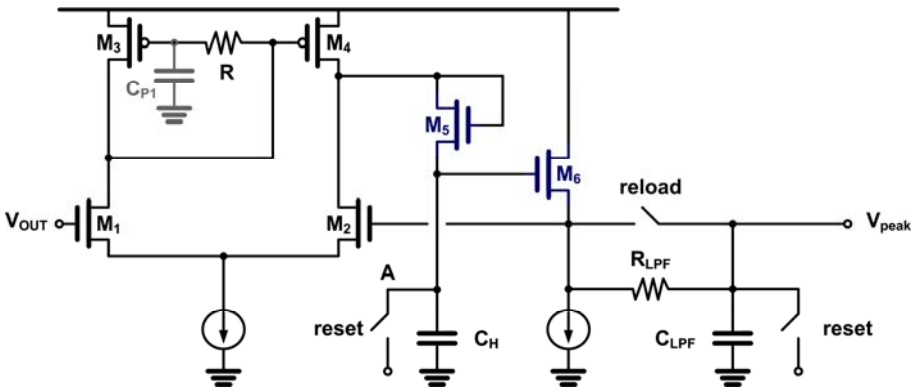


Fig. 3-15 Schematic of peak hold circuit

Peak value of VGA output swing will be kept on C_H in Fig. 3-14. Due to negative feedback path, the transconductance stage will charge C_H through the diode again if there is a more large swing. A buffer is added behind the connection of diode and capacitor to drive the succeeding low pass filter. A simple RC low pass filter is required here to reduce the voltage glitch caused by the leakage and non-ideality of the diode.

Schematic of this peak detector is shown above in Fig. 3-15; the resistor R between M_3 and M_4 will generate a zero to the G_m and enhance the bandwidth of this transconductance stage. M_5 is drain-gate connected as a diode and M_6 is the source follower, both of them are implemented by low threshold device due to DC voltage concern.

Due to the generated zero, the effective G_m can be presented as:

$$G_m \approx \frac{1}{2} g_{m2} + \frac{1}{2} g_{m1} \cdot (Z // r_{o3}) \cdot g_{m4}$$
$$where\ Z \approx \frac{1}{g_{m3}} (1 + s \cdot RC_{p1}) \quad \textbf{(33)}$$

and total transfer function can be derived as:

$$\frac{V_{peak}}{V_{OUT}} = \frac{1}{1+s\cdot\frac{C_H}{G_m}}\cdot\frac{1}{1+s\cdot C_{LPF}R_{LPF}} \quad \textbf{(34)}$$

Another detail that should be specified is the timing control and settling time of this circuit, the acquired peak value should be reset when another gain mode searching is started because the coming value may be smaller than this one. Before discussing that control, the schematic of the bottom hold circuit should be given first, as in Fig. 3-16.

Contrasted to node A and V_{peak} in Fig. 3-15 is the node B and V_{bottom} in Fig. 3-16. In order to speed up the processes of reset, the charging capacitor C_H and C_{LPF} will not reset to Vdd or ground but to the contrasted point, and get an average voltage when reset, and this signal is generated by control unit.

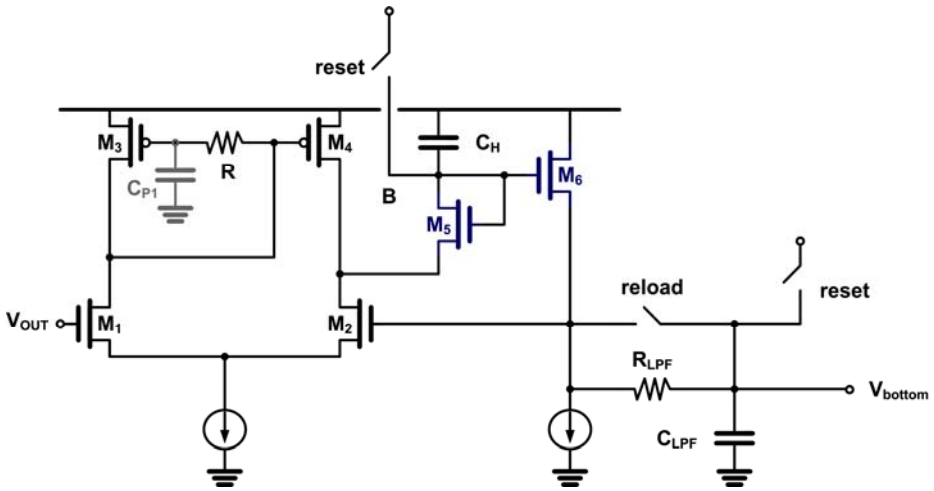


Fig. 3-16 Schematic of bottom hold circuit

The utility of “reload” duration has been explained in section 2.2.2; noise performance and settling time is a trade-off for the effective low pass filter here; in order to speed up the settling time with a comparable noise performance, the resistor R_{LPF} will be short by a switch during reload time, and just charging the capacitor C_{LPF} without concerning the noise. After the reload duration, the switch will open, and the low pass filter can suppress the noise and glitch generated by the diode non-ideality, giving a clean DC voltage to the succeeding comparator. Due to the reload mechanism, it seems that the critical settling time will not depend on the RC low pass filter, so the buffer driving capability and the -3dB frequency of the low pass filter is easy to design to fit the specification. For a 100 MHz clock rate, it will take 10ns for reload and 10ns for LPF duration in this design; using first order RC charging concept, if the time constant generated by C_{LPF} and the buffer output resistance is less than 2ns, C_{LPF} will be charged to more than 99% buffer output voltage in this 10ns reload duration, and it will ease the design difficulty of this RC low pass filter.

By (34), it’s obviously to know that the settling time performance will critically depend on the time constant generated by the transconductance stage G_m and its charged capacitor C_H. A small C_H will lead to a great glitch due to the leakage of the diode, but it will spend less settling time; and there is a trade-off between bandwidth and gain in the transconductance stage. To charge C_H to 90% VGA output swing in 10ns reload time, this time constant is set to be 4ns with about 5 GHz G_m bandwidth . Under this determination, glitch on C_H is still severe in reload duration, but the noise performance will be improved after the low pass filter, and can be ignored if the succeeding comparator has noise immunity.

In this design, the bandwidth of the Gm amplifier (open loop gain) is about 2GHz, so the data rate of preamble signal should be less than that of the normal data, which is 5GHz; or the settling time of the peak detector should be further long. The bandwidth of the closed loop (including Gm cell, diode, charged capacitor, and buffer) is set to be 250MHz for 90% accuracy in 10ns, and the simulation results is shown below.

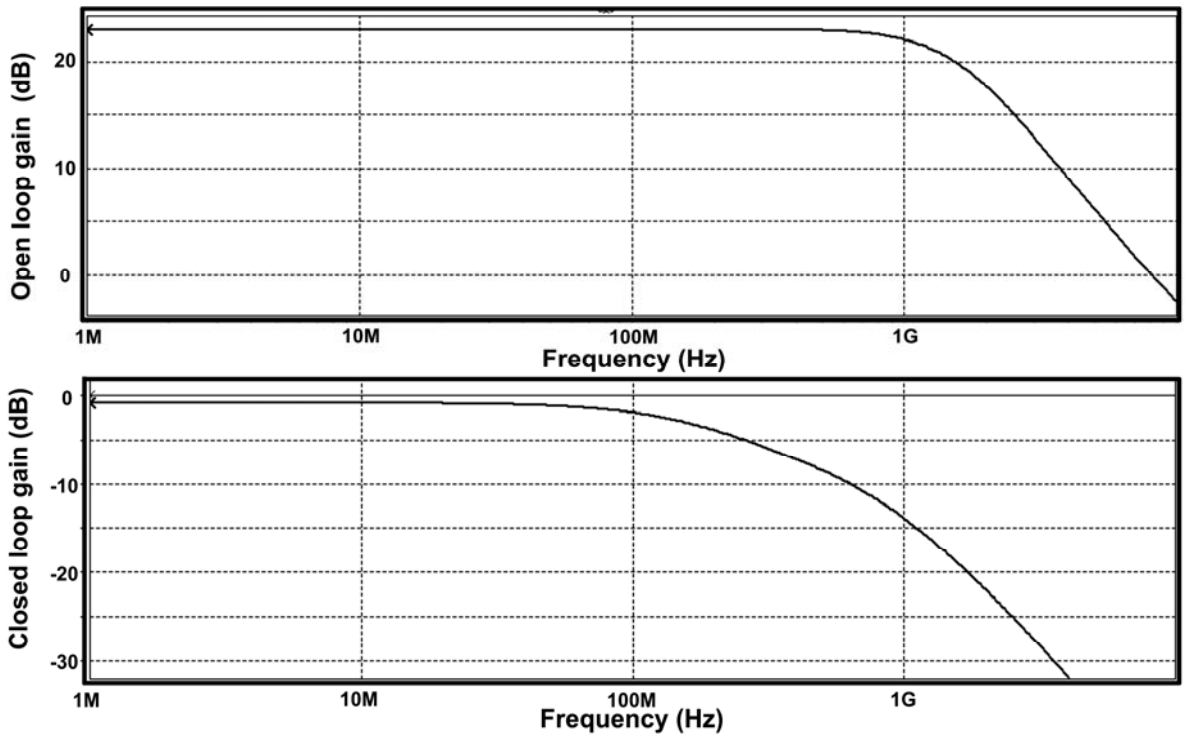


Fig. 3-17 Peak detector Simulation Results

3.3 Tri-state Comparator

To compare the VGA output amplitude to the reference voltage, and giving sufficient information to the digital controller for gain variation, a tri-state comparator is adopted in this design. If the comparator is bi-state, the result of the comparator will be either large or small, and this situation may cause the gain of VGA flipping between two close gain modes when the output amplitude approximates to the reference voltage.

A tri-state comparator needs two threshold voltages, V_{TH} and V_{TL}, to indicate that if the gain mode should be adjusted or not. As the output amplitude is larger than V_{TH}, gain of the VGA should be reduced, and an output amplitude less than V_{TL} will bring a higher gain mode. If the output amplitude is located between VTH and VTL, it means that the voltage is close to the reference, and the gain mode should be held.

With a simple thought, this tri-state comparator can be implemented by two sub-comparators; one compares the output swing to V_{TH}, and the other compares to V_{TL}. If the two results of them are both large or small, sending “lg” or “sl” information to the digital controller respectively; and nothing will be sent if the results are different. Prototype of the single comparator is composed of a Hysteresis amplifier and a succeeding latch; the Hysteresis amplifier is a dual source coupled pair with positive feedback loading. The positive feedback loading will lead to the Hysteresis effect and enhance the noise immunity for this comparator input stage.

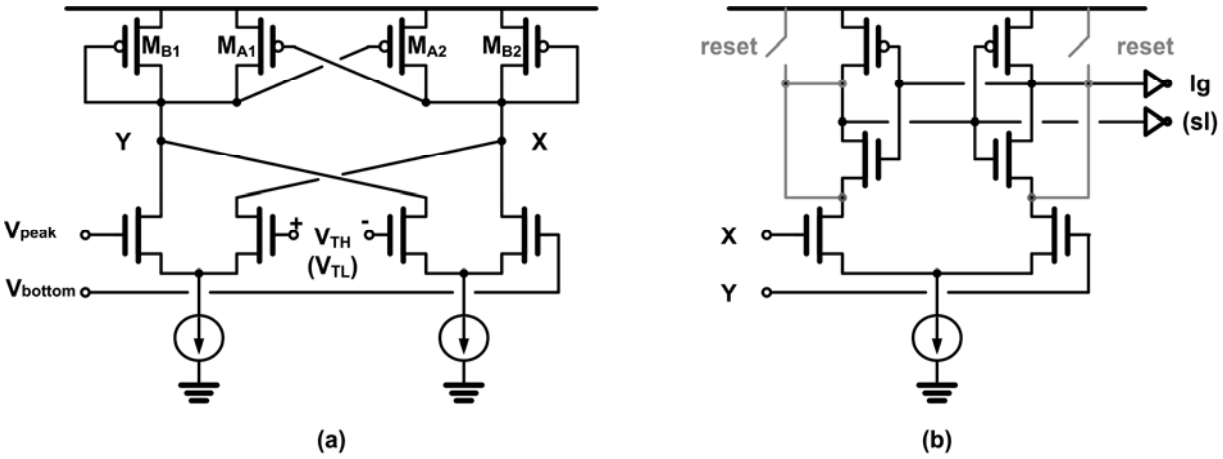


Fig. 3-18 Schematic of (a) Hysteresis amplifier and (b) latch

Schematic of the Hysteresis amplifier and the latch is shown above. As mentioned, input stage of the Hysteresis amplifier is a DSCP (Dual Source Coupled Pair). By the DSCP, the dual difference result can be gotten:

$$\begin{aligned} I_X - I_Y &= g_m \cdot [(V_{TH+} - V_{TH-}) - (V_{peak} - V_{bottom})] \\ &= g_m \cdot [V_{TH} - A_{out}] \end{aligned} \quad \textbf{(35)}$$

The loading of the DSCP is composed of 4 transistors, which are represented as $M_{A1,2}$ and $M_{B1,2}$ in Fig. 3-18(a). If the size of M_A is larger than M_B, this loading will be positive feedback and make the voltage difference between node X and node Y will be pulled apart, and make it larger than they will be with resistive load.

Node X and node Y are hard to change their positive/negative state due to this positive feedback effect, and this brings the Hysteresis effect. To explain this effect, assuming A_{OUT} (= V_{peak} - V_{bottom}) is larger than V_{TH} (= V_{TH+} - V_{TH-}) at first, making $V_X > V_Y$ and V_X is large enough to cut off M_{A1} and M_{B2}.

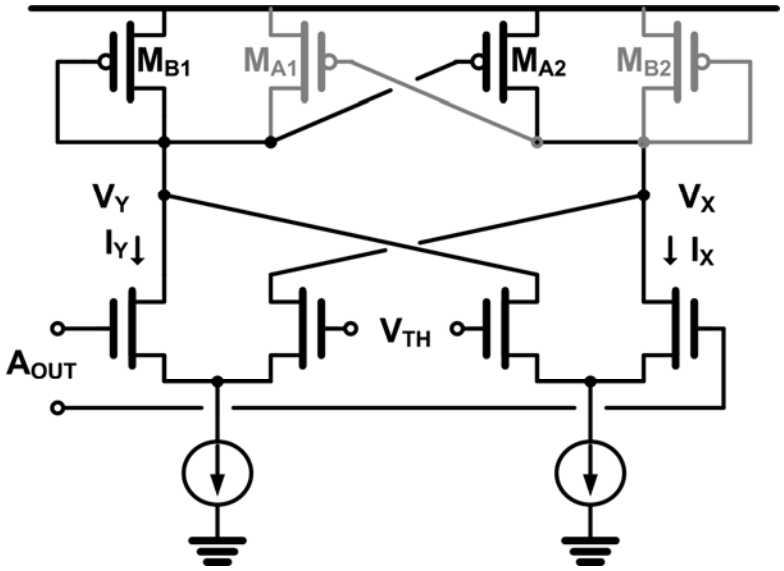


Fig. 3-19 Hysteresis effect explanation

As shown in Fig. 3-19, because size of M_{A2} is larger than that of M_{B1}, and their gate voltage are both equal to V_Y, I_X will be larger than I_Y and makes the voltage difference more severe. State of node X and node Y will not be changed when A_{OUT} is just a little smaller than V_{TH}, due to I_X is still larger than I_Y at this time; only when the difference of A_{OUT} and V_{TH} is sufficient to make up this current difference, the state will be changed.

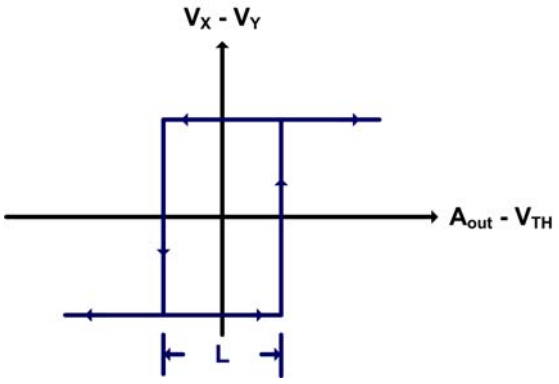


Fig. 3-20 Hysteresis transfer curve

Relationship between ($V_X - V_Y$) and ($A_{out} - V_{TH}$) can be presented as the above figure. It is called Hysteresis effect due to the gap "L", and interval of the gap depends on the current difference between I_X and I_Y, and the effective transconductance of the DSCP. Input stage of this comparator will has a better noise immunity because of this gap; any noise whose peak value is smaller than half of L won't change the state and lead to a wrong answer. Latch in this comparator design is another amplifier with positive feedback loading and reset switch. Seeing Fig. 3-18(b), loading of the amplifier is like a cross-coupled inverter; when the reset signal which is generated by control unit comes into an end, output voltage will be pulled apart rapidly according to the relative voltage level of node X and node Y. With the digital inverter as the buffer, results of the comparator will be a digital signal and can be adopted in the succeeding digital controller.

After integrating the two comparators which compares A_{out} to V_{TH} and V_{TL} respectively, the totally relationship between VGA output amplitude, V_{TH}, V_{TL} and the results – lg or sl, can be presented as the following figure:

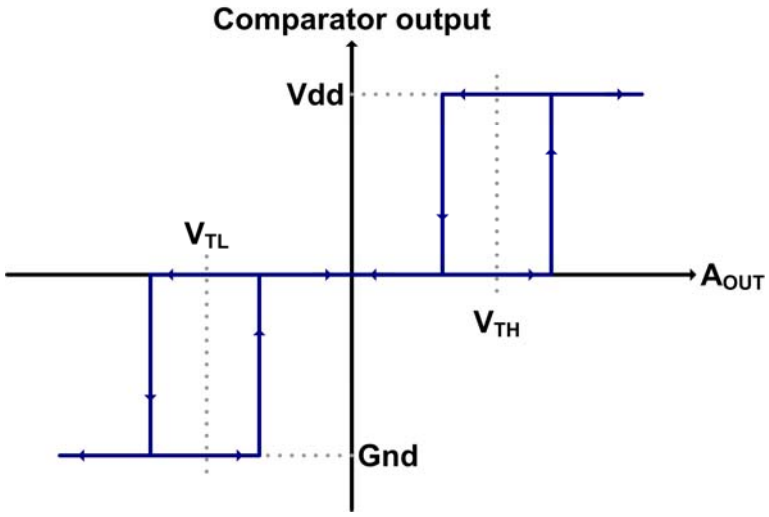


Fig. 3-21 Tri-state comparator transfer curve

V_{TH} and V_{TL} are tunable outside the chip in this design, and providing a more flexible comparator offset immunity. As mentioned in section 2.2 and 3.1.3, the target output swing of the VGA is about $500mV_{pp}$, and there will be about 0.8dB gain variation between every gain mode. Considering the resolution issue, 0.8dB is about 1.1 in decimal; so the interval between V_{TH} and V_{TL} should be about 50mV, and make the VGA output falling upon $475mV_{pp}$ ~ $525mV_{pp}$ for one bit resolution.

3.4 Digital Gain Controller

In this section, algorithm, timing chart and detailed circuit of the searching engine in the digital gain controller will be described. The searching engines generate the control signals for gain variation according to the comparator, and a following encoder will turn these control signals into thermometer code, because of the requirement of the digitally tunable resistor mentioned in section 3.1.3.

The timing control unit is the core of the digital gain controller. It generates all the clocks for searching engines and retiming latch, changes the searching mode form binary search to linear search, and also provides the reset signal for the peak/bottom detector and comparator.

3.4.1 Binary Search Engine

The purpose of the binary searching is accelerating the searching speed for the required thermometer code. Compared to the time complexity of linear search, that of binary search is reduced in a logarithmic scale; that is, if there is 2^n bits searching process, linear search will take 2^n unit interval for the worst case search, but binary search will just take n unit interval.

Concerning the hardware complexity and settling time of the AGC loop, a 4-time binary search is chosen in this design due to there is 24 bits thermometer code controlling the gain of VGA; the most appropriate 16 bits thermometer code will be determined after this 4-time binary search; the 8 remaining control

bits is designed to be controlled by the linear search engine, and will reset to the half. To construct a binary search engine, it should be started from the algorithm, and the binary search algorithm can be represented by a binary tree:

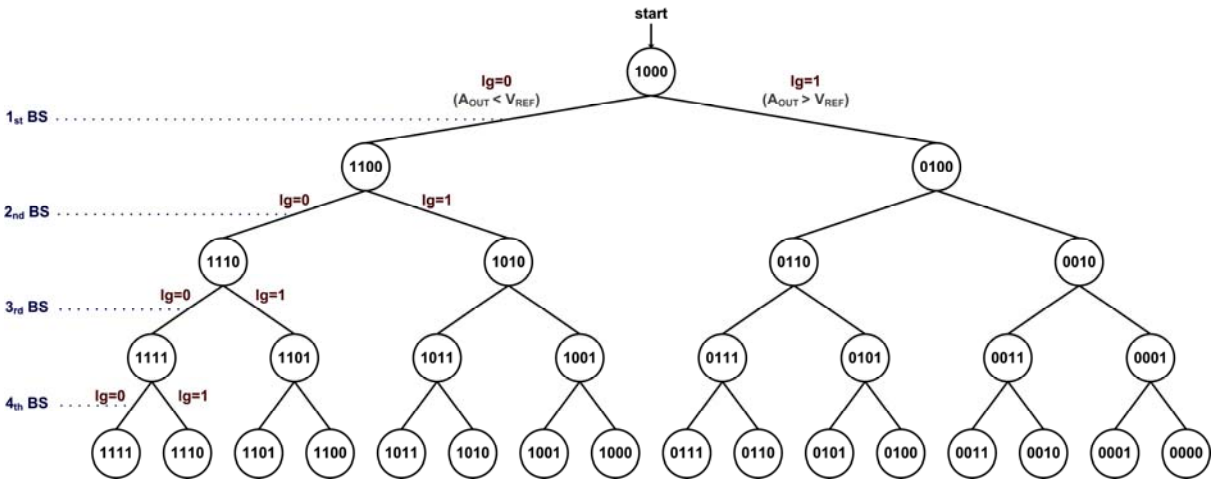


Fig. 3-22 4-time binary search tree

The 16 bits thermometer code is represented by 4 bits binary code in this binary search tree. If the MSB of the 4 bits binary code is called 1_{st} bit, and the LSB is called 4_{th} bit, this algorithm can be simplified as three steps:

(1) Start at the half of 4 bits binary code, 1000.

(2) At the beginning of i_{th} binary search, set the i_{th} bit of the binary code to 1.

(3) Reset i_{th} bit of the binary code to 0 during i_{th} binary search, if the output swing is larger than the reference voltage.

The binary search engine can be realized according to this algorithm as following figure, and provide 16 different gain modes in the gain range 1.5dB to 13.5dB. A timing sequence sample of a binary searching result 1101 is shown in the next figure, and it represents the signal flow of this binary search engine.

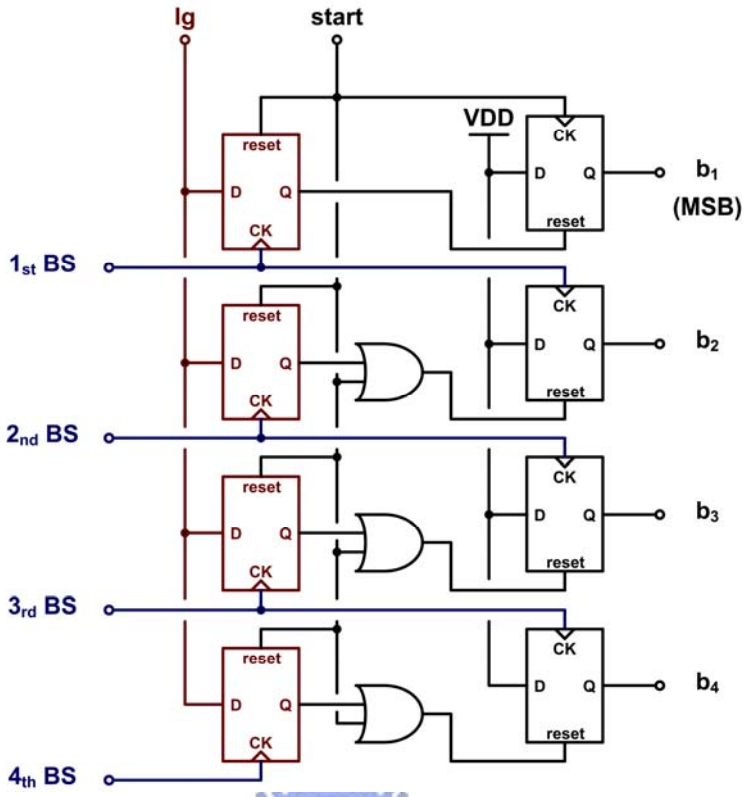


Fig. 3-23 4-time binary search circuit

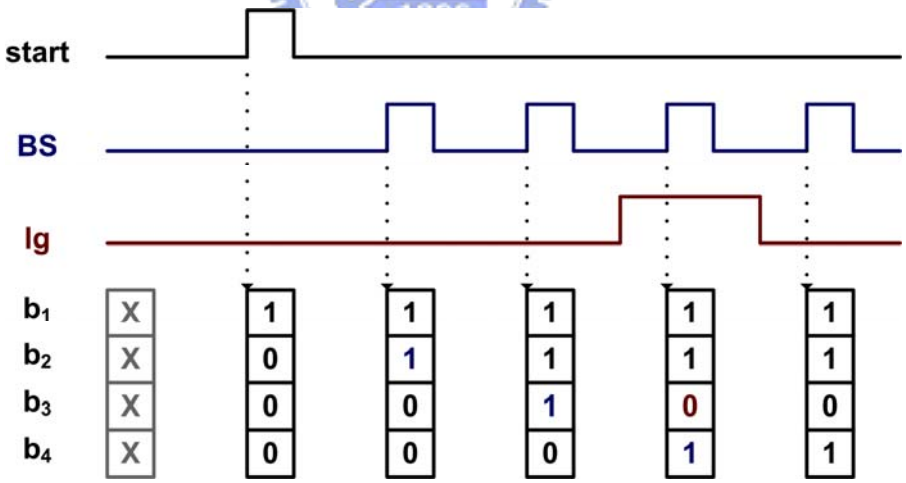


Fig. 3-24 Timing chart of searching result for an example 1101

3.4.2 Linear Search Engine

The purpose of the linear searching is providing long time stability for the AGC loop. A binary search engine can find the appropriate thermometer code quickly, but it is a one-time search flow and can hardly change the gain control bit again after the process comes into an end; because the VGA input swing may vary after the binary search process, a linear search engine will start after the end of binary search

The linear search engine in this design is based on shift register prototype, and the 1 or 0 in the register will shift according to the result of the tri-state comparator; if the shift register overflows or underflows, linear search engine will deliver a message to reduce or enhance the gain respectively.

A linear search engine can be viewed as a digital low pass filter in this AGC loop. It stands for the loop filter, accumulates the information if $A_{OUT} > V_{REF}$ or not, and change the gain of VGA moderately. As mentioned above, this linear search engine will adjust 8 bits thermometer code for gain variation; by the usage of the succeeding encoder, the 8 bits control signal will be determined, as the critical mission of this linear search engine is to accumulate the information of comparator output.

In order to determine the time constant of this digital low pass filter, loop bandwidth of the AGC should be taken into account. In general, a wide loop bandwidth will speed up the settling time, but the loop will has a weak point at

noise and spur issue, which will leads to the amplitude variation. In this 4 PAM system, there will be different amplitude for different symbol, so the loop bandwidth should be narrower than a binary transition system. Concerning the target clock rate and the time spent on one time searching, an 8 bits shift register is adopted in this design.

Algorithm of this linear search is shown as the follow figure, if the result of the comparator is lg, “1” in the register will be shifted, as “0” is shifted if the result of the comparator is sl; when the result is neither lg nor sl, the shift register will keep the current state. If the overflow or underflow occurs, the shift register will reset to 11110000, and send a message of reducing or enhancing the gain to the succeeding encoder.

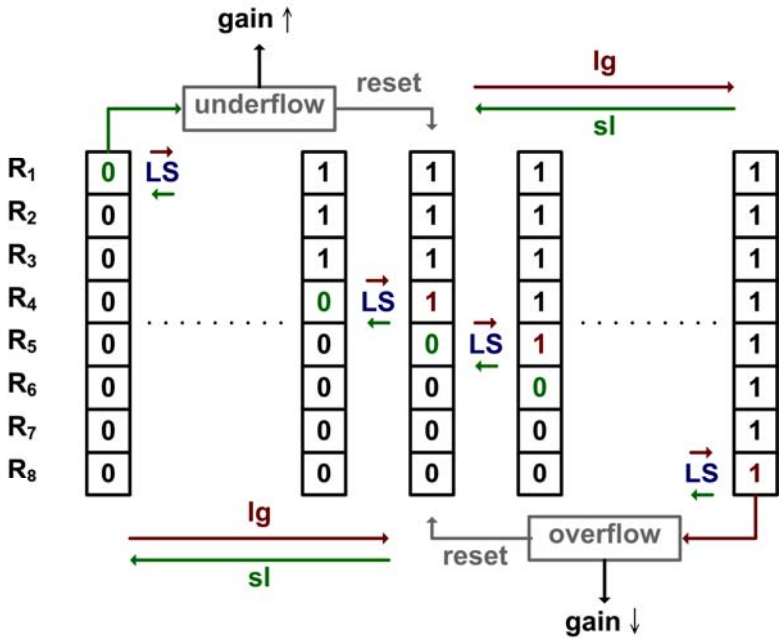


Fig. 3-25 Linear search algorithm

To realize this circuit according to this algorithm, a two-way shift register is indispensable. This circuit can be implemented by a selector and a common serial register; selector can help to determine the signal path, whether “1” or “0” should be shift. Detailed circuit schematic is shown in the following figure.

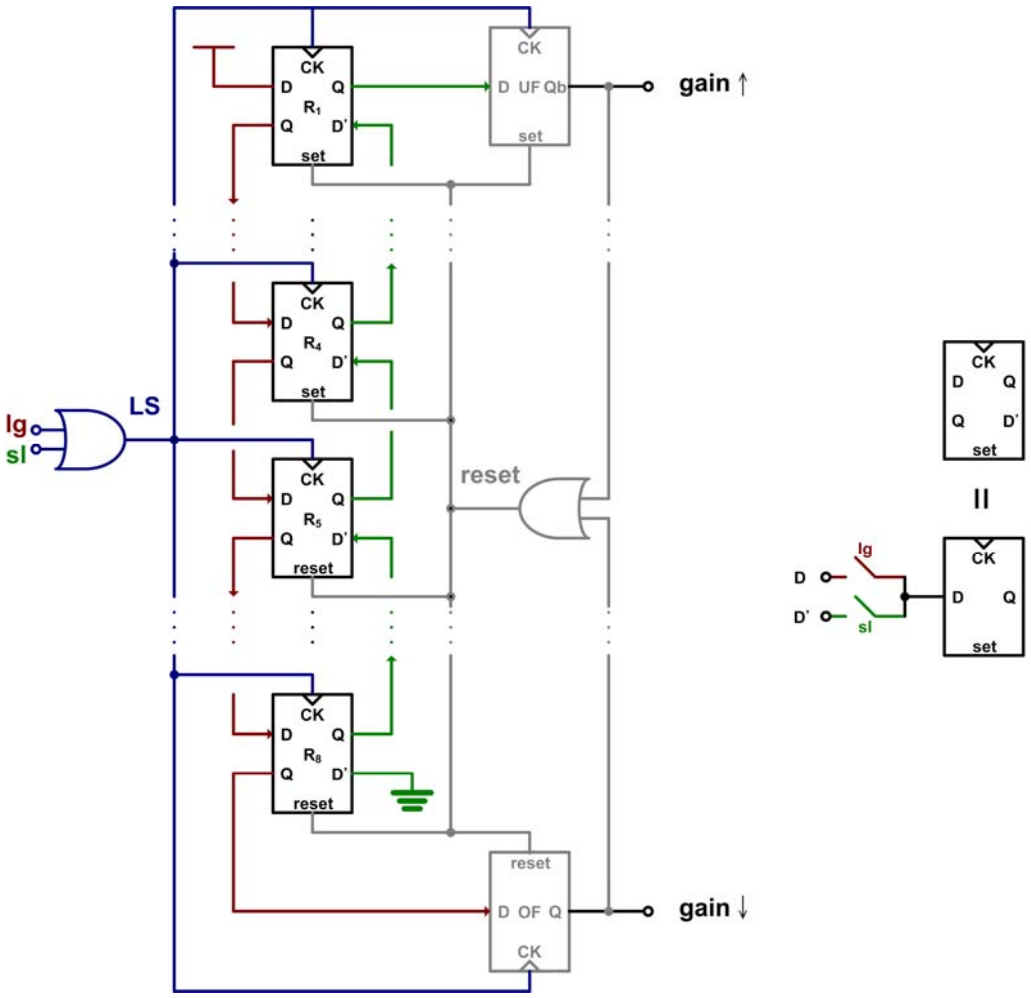


Fig. 3-26 Linear search engine

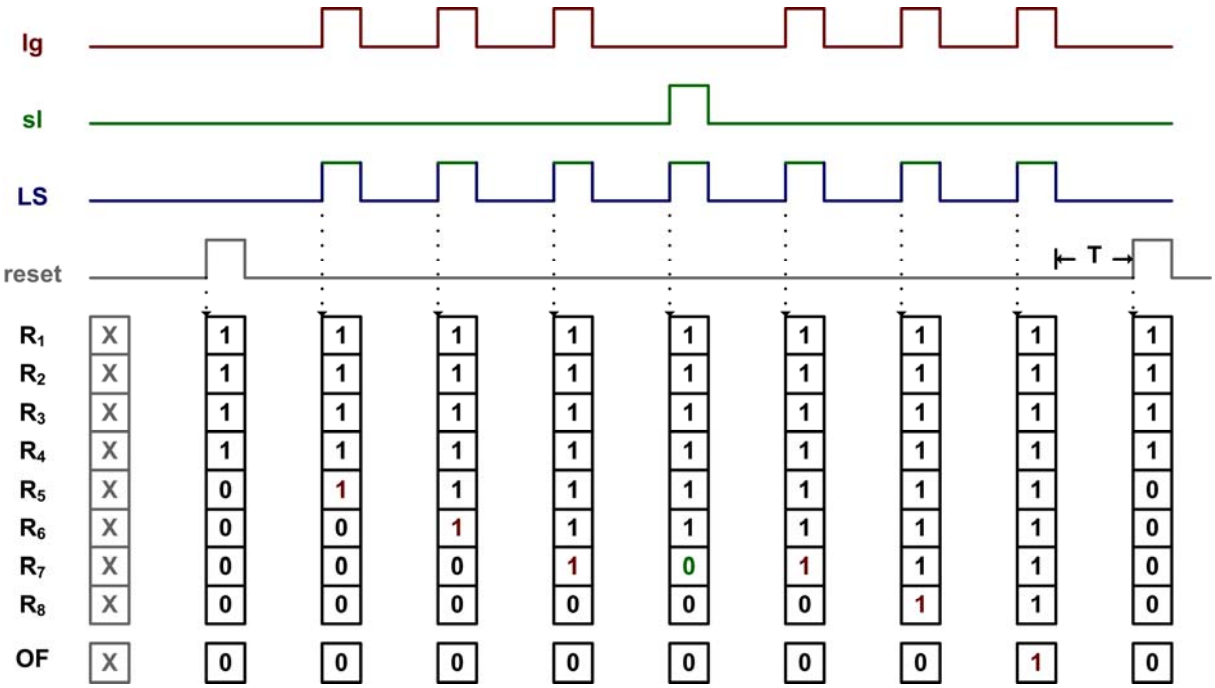


Fig. 3-27 Timing chart of an LS example

An overflow sample of a linear searching is shown in the above figure, and it represents the signal flow of this binary search engine (OF = overflow). Notice that there is some control signals not shown in the schematic; when the overflow or underflow occurs, there will be a buffer time ("T" in the timing chart above) for the overflow/underflow and gain enhancing/reducing signal to remain, and keeping the system stable.

The digital loop filter is declared, now the loop bandwidth of this AGC can be derived. In linear search mode, gain will be enhanced or reduced after 5 times net sl or lg; for a 100MHz clock rate and the one time comparison needs 4 clock, the time constant of this digital low pass filter is 200ns. Using (12) and concerning that every gain control bit determine 0.8dB for the VGA, the -3dB frequency of this loop, or loop bandwidth in briefly said, is about 5.5MHz.

3.4.3 Encoder

Due to the binary search engine only provides the binary code as the searching result, there should be a binary-to-thermometer encoder to turn the searching result into the thermometer code, for controlling the gain of VGA; on the other hand, the linear search engine only gives the information of enhancing or reducing the gain, a succeeding linear encoder will be adopted to control the remaining 8 bit thermometer code.

Binary	Thermometer	Binary	Thermometer
0000	0000000000000001	1000	0000000111111111
0001	0000000000000011	1001	0000001111111111
0010	0000000000000111	1010	0000011111111111
0011	0000000000001111	1011	0000111111111111
0100	0000000000011111	1100	0001111111111111
0101	0000000000111111	1101	0011111111111111
0110	0000000001111111	1110	0111111111111111
0111	0000000011111111	1111	1111111111111111

Table 3-3 Truth table of binary to thermometer encoder

The binary-to-thermometer encoder is realized by the combinational logic, the truth table is shown above. Let the symbols of the binary code are b_1 (MSB) to b_4 (LSB), and those of the thermometer code are T_{01} (MSB) to T_{16} (LSB), the Boolean function of the thermometer code can be derived and the detail circuit can be implement by basic inverter, NAND gate, and NOR gate. After the combinational logic, outputs will be synchronized by the D-FFs for stability concern.

T_{01}	$b_1 \cdot b_2 \cdot b_3 \cdot b_4$	T_{09}	$b_1+(b_2 \cdot b_3 \cdot b_4)$
T_{02}	$b_1 \cdot b_2 \cdot b_3$	T_{10}	$b_1+(b_2 \cdot b_3)$
T_{03}	$b_1 \cdot b_2 \cdot (b_3+b_4)$	T_{11}	$b_1+(b_2 \cdot (b_3+b_4))$
T_{04}	$b_1 \cdot b_2$	T_{12}	b_1+b_2
T_{05}	$b_1 \cdot (b_2+(b_3 \cdot b_4))$	T_{13}	$b_1+b_2+(b_3 \cdot b_4)$
T_{06}	$b_1 \cdot (b_2+b_3)$	T_{14}	$b_1+b_2+b_3$
T_{07}	$b_1 \cdot (b_2+b_3+b_4)$	T_{15}	$b_1+b_2+b_3+b_4$
T_{08}	b_1	T_{16}	always High

Table 3-4 Boolean function of binary to thermometer encoder

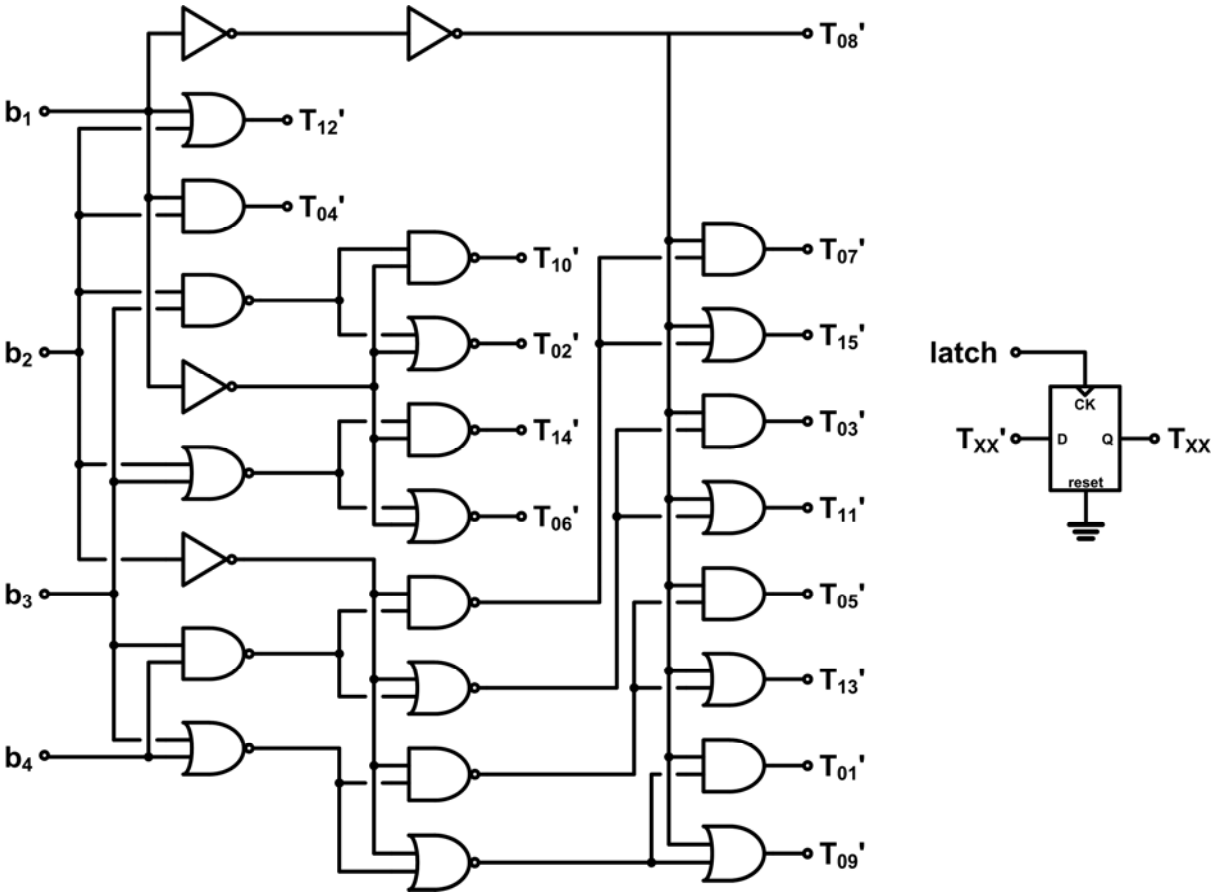


Fig. 3-28 Binary-to-thermometer encoder

Another two-way shift register was chosen to realize the linear encoder, because control bits of the VGA are thermometer code. To control the 8 bits thermometer code, this shift register will reset to 00001111 and provide maximum ±3.3 dB gain variation after binary search. If this linear encoder is overflow or underflow, that is, if the input swing varies 3.3dB (about 50%) after binary search, the AGC loop should be totally reset and settled again.

Let the symbol of the 8 bits thermometer code is T_{17} (MSB) to T_{24} (LSB), the following figure represents the linear encoder; as a detail, half of the D-FF will set to 1 when the reset signal come, and the others will reset to 0.

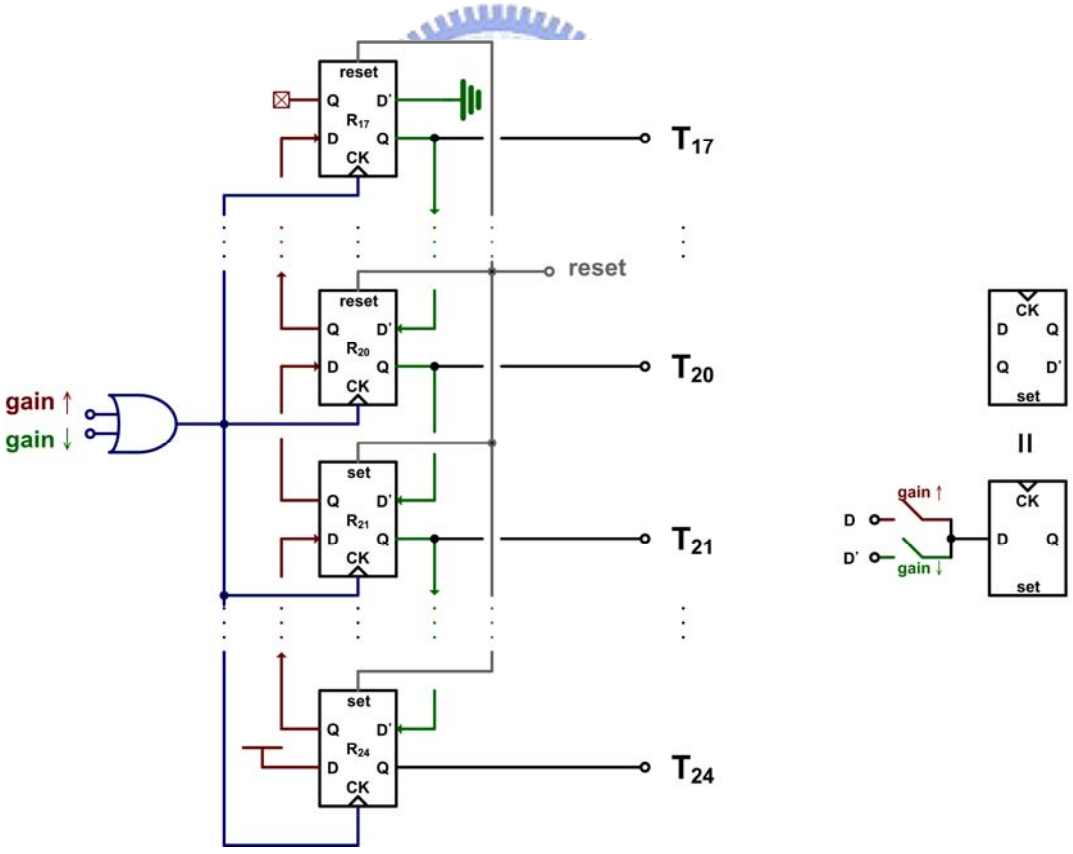


Fig. 3-29 Linear encoder

3.4.4 Control Unit

The control unit in the digital gain controller has two major utilities. First, turning the searching mode from binary to linear when binary search comes into an end; second, generating the reset signal for detector and comparator, and synchronizing the digital signals like gain control bits and the results of tri-state comparator.

Briefly said, this control unit puts all the blocks of the AGC loop in order, let them do the right thing at the right time; and it can be viewed as a clock generator, due to the searching is periodic. Detailed periodic timing sequence of the loop is shown in Fig. 2-9, and it is shown in the following figure again for convenience.

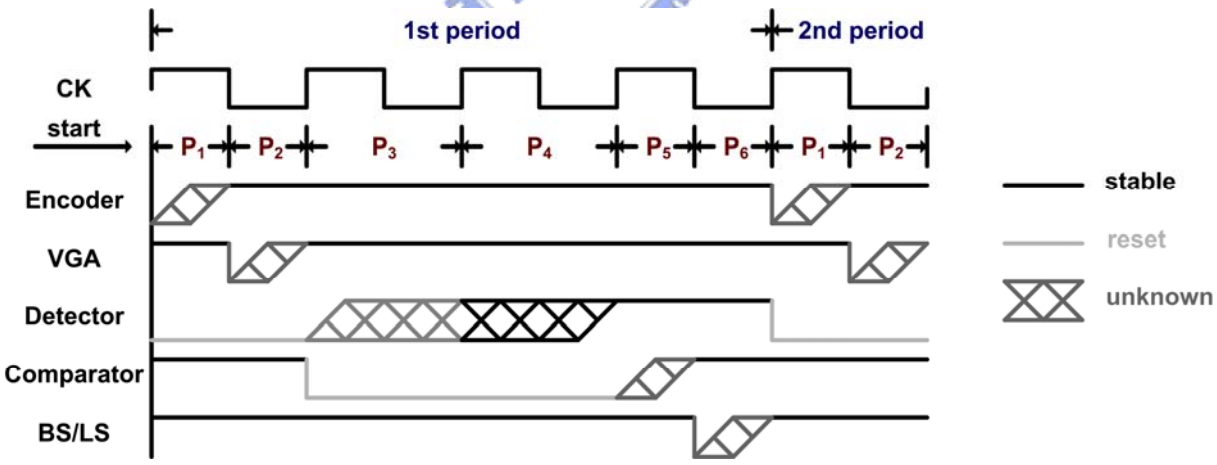


Fig. 3-30 Timing sequence

Based on the illustration of binary search engine and linear search engine, it can be known that binary search will stop after 4 periods, and linear search will be started and work periodically. As a result, this control unit can realize the periodic control signal by register rotation, and another counter is adopted to stop binary search and start linear search. The following Fig. 3-31 can be used to illustrate this concept.

After reset signal, the 4-bit shift register will move in circle, and generate the periodic clocks. This rotation will trigger another counter for binary search; if the counter overflows, binary search is over, and it starts linear search mode. The rotated shift register also controls the reset signal of detector and comparator. Detector will reload (capacitor charging) during P_3, and falling edge of 1_{st} and 4_{th} clock will do encoder synchronization and latching comparator result, respectively.

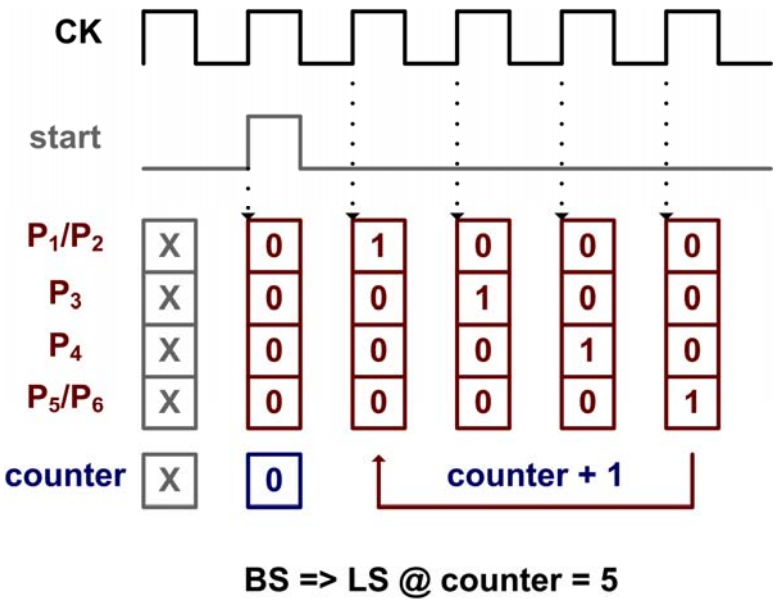


Fig. 3-31 Diagram of control unit

This control unit can be realized by D-FFs and basic logic cells, the simplified schematic can be shown as following figure:

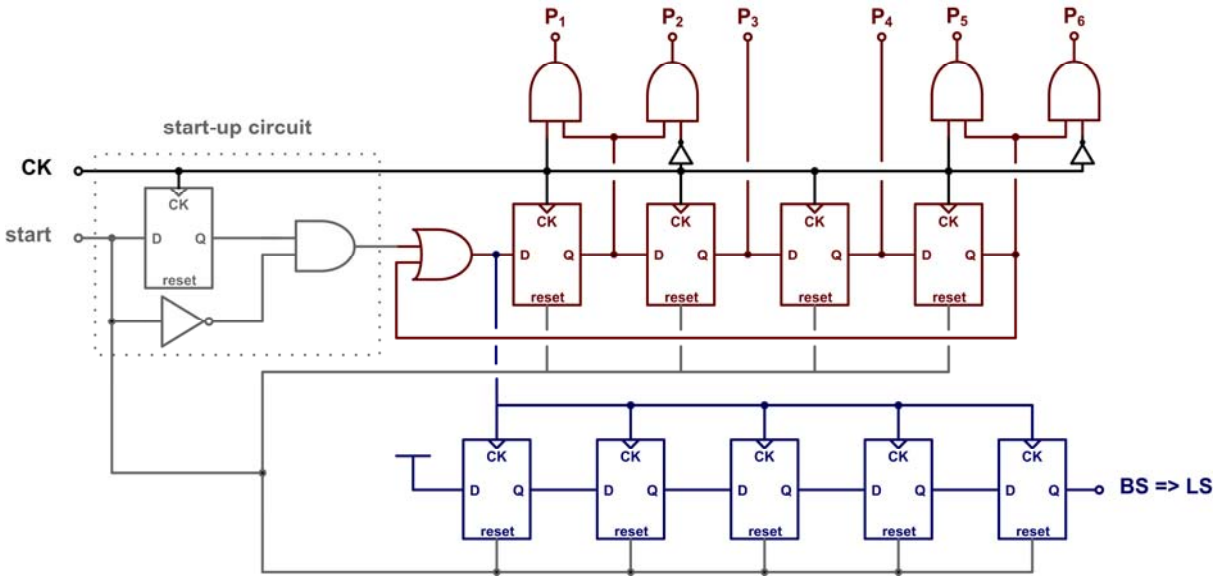


Fig. 3-32 Simplified schematic of control unit

3.4.5 Settling Time Simulation Results

Above sections in Chap 3 represents the detailed circuits of the proposed AGC, and performance of the VGA is shown in section 3.1.6. Now the following figure shows the settling time, another important specification of this AGC loop.

This figure shows that the input and output amplitude of the AGC. When the clock rate of the digital circuits is 100MHz, binary search will terminate in 170ns after the reset signal, and adjust the gain first to make the output amplitude near the reference voltage; after 400ns, input amplitude will be a smaller one, and here comes the linear search circuit, it will compensate the insufficient gain one time within 210ns.

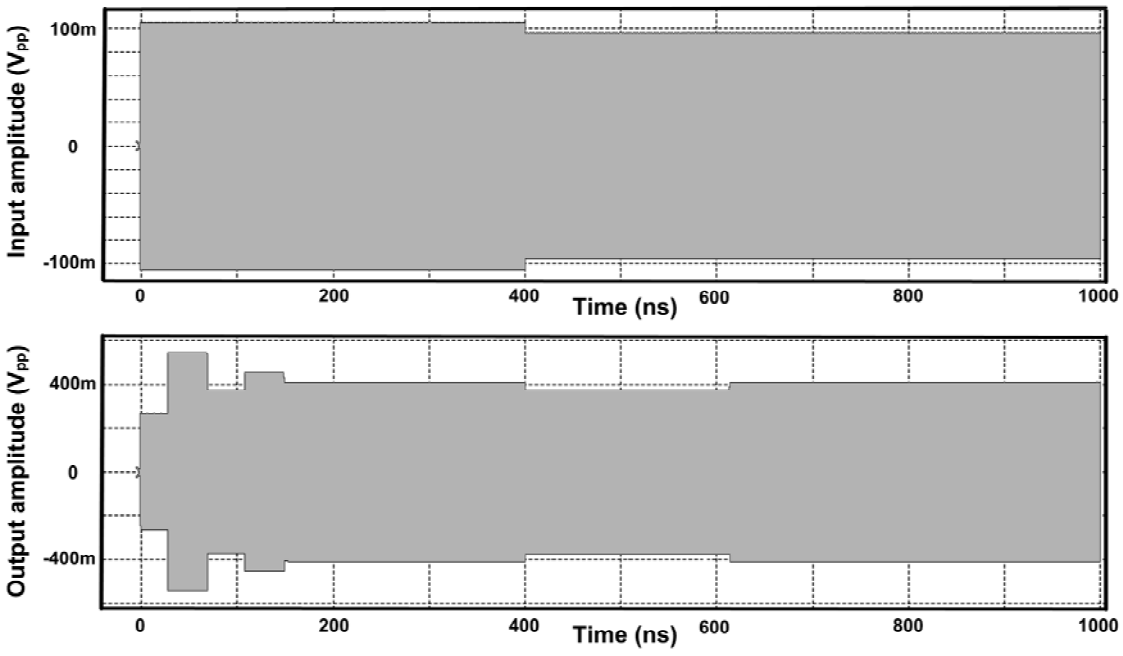


Fig. 3-33 Settling time of AGC

Chapter 4 Experimental Results

4.1 Layout and Chip Photo

The proposed automatic gain control circuit is fabricated in TSMC 0.18μm 1P6M CMOS process. The following figures show the layout, pin assignment and chip photo.

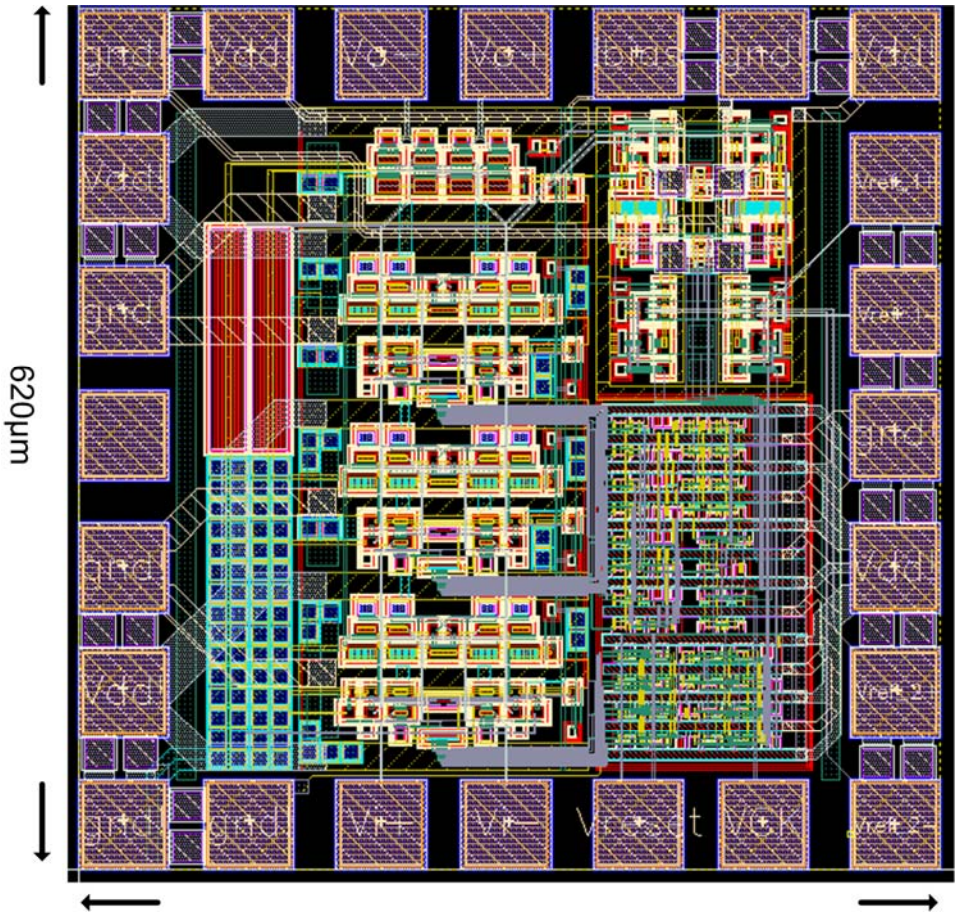
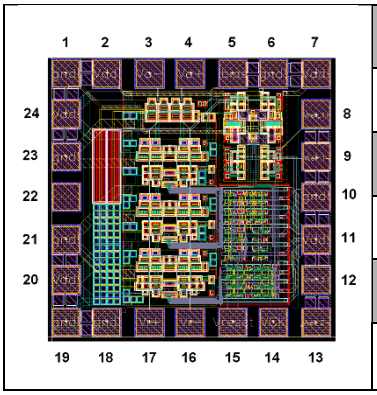


Fig. 4-1 AGC chip layout view



1	2	3	4	5	6	7	8
Gnd	Vdd	V_{OUT-}	V_{OUT+}	Bias	Gnd	Vdd	V_{TH+}
9	10	11	12	13	14	15	16
V_{TH-}	Gnd	Vdd	V_{TL+}	V_{TL-}	CK	reset	V_{IN+}
17	18	19	20	21	22	23	24
V_{IN-}	Gnd	Gnd	Vdd	Gnd	N/A	Gnd	Vdd

Table 4-1 Pin assignment

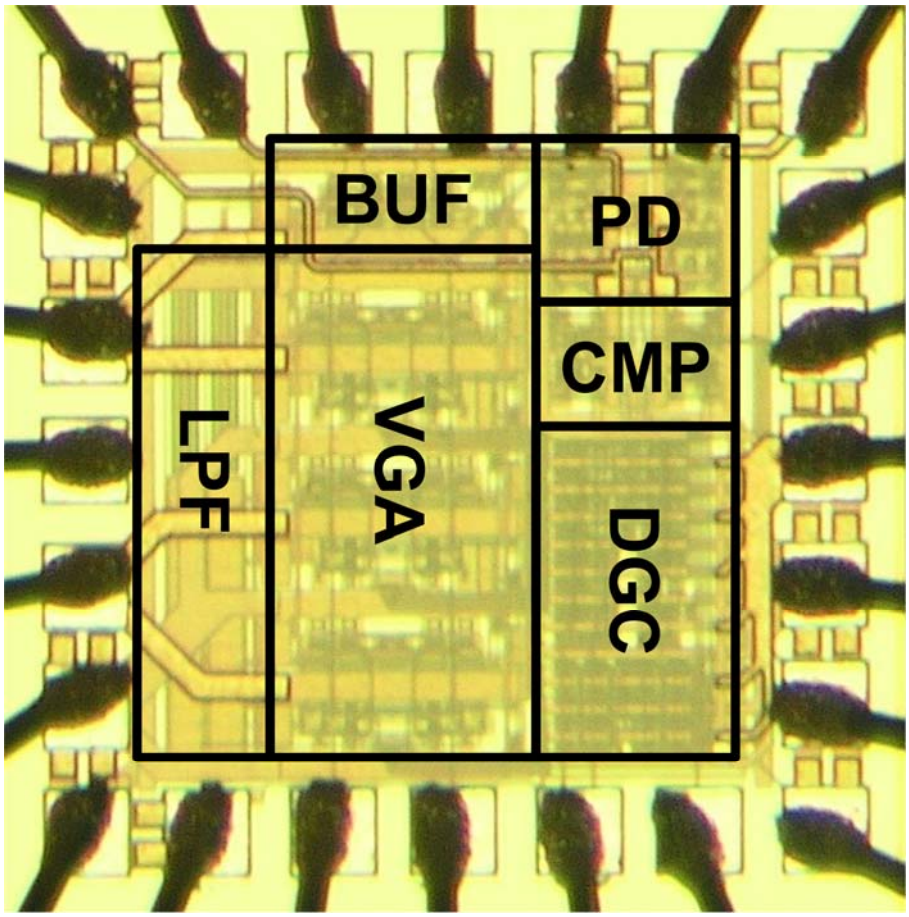


Fig. 4-2 Die photo

In above figure, LPF=low pass filter for DC offset cancellation; BUF=buffer; PD=peak detector; CMP=tri-state comparator; DGC= digital gain controller. Total chip area is 620 x 620 μm^2, including the pads. Its floor plan can be divided into four parts – VGA with buffer, peak detector, tri-state comparator, and the digital gain controller.

Differential outputs and inputs are delivered through pad 3, 4 and 16, 17; clock and reset signal are sent into the digital circuit by pad 14 and 15; other pads are DC paths.

4.2 Test Setup

The AGC chip is mounted on the PCB (Printed Circuit Board) for measurement; the parasitic and inductive characteristic of the bounded wire and PCB should be concerned in the whole circuit simulation. The following figure shows the AC board for the closed loop AGC, and the environment setup is arranged for settling time and eye diagram measurement. VGA inputs, the binary or 4-PAM signals, are generated by an AWG (Arbitrary Waveform Generator), and the results will be shown on the oscilloscope. Reset signal can be generated by a simple pulse generator, and the 100MHz clock is generated by HP 8311A whose data rate can be 3GHz.

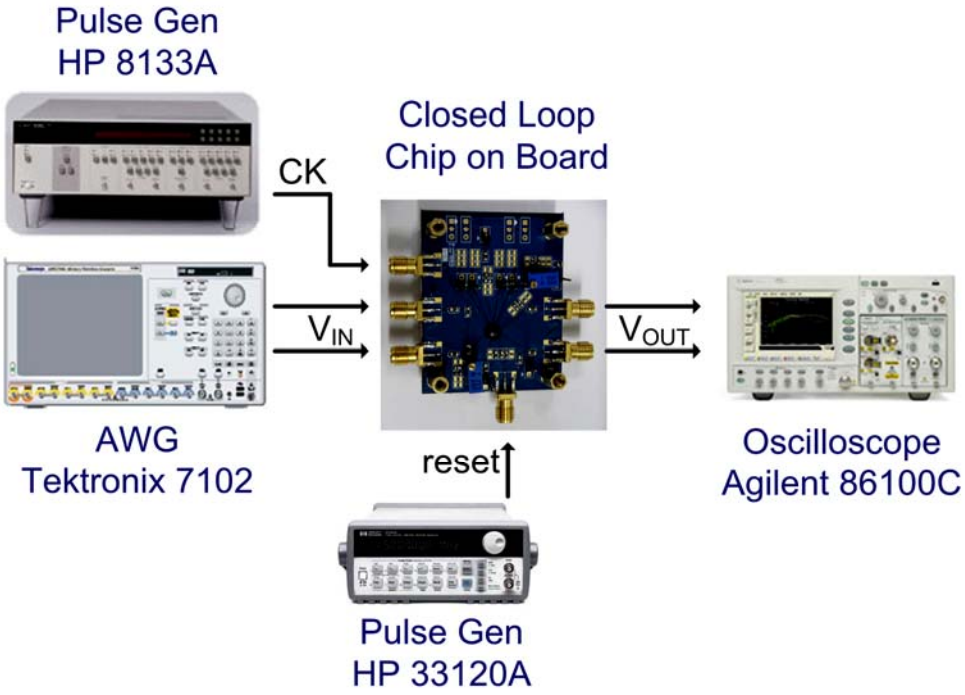


Fig. 4-3 Environment setup for closed loop measurement

Due to the automatic gain control, gain mode of the VGA is determined by circuit itself, and it's hard to be changed precisely and permanently when the circuit is still closed loop. As a result, an open loop prototype is utilized for another setup, to measure the frequency response and phase response, as the following figure. A simple clock generator is utilized to latch the gain control thermometer code in this open loop VGA. Because the network analyzer has only two ports, response of the VGA can not be measured differentially; As a result, the gain response of this single-in-single-out VGA will be 6dB smaller than what we prospect, which should be differential-in-differential-out.

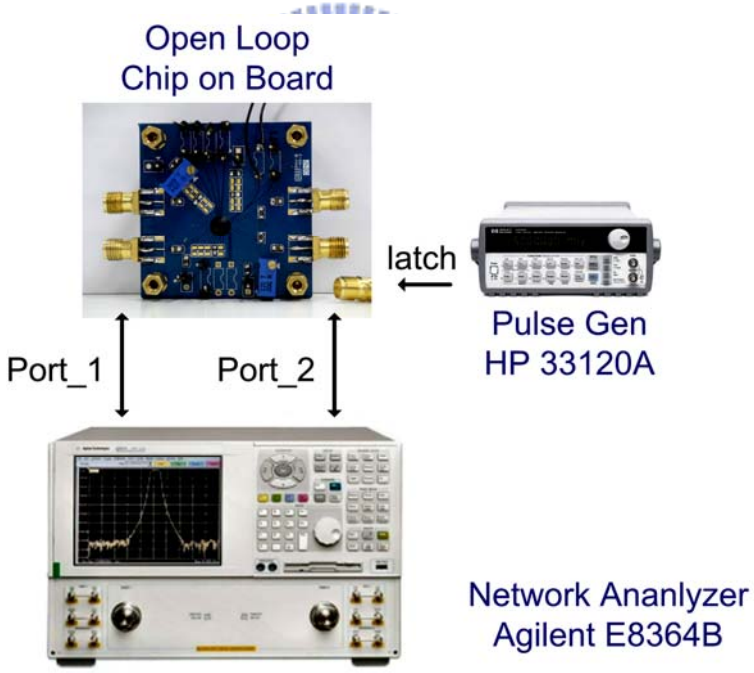


Fig. 4-4 Environment setup for open loop measurement

4.3 Measured Results

4.3.1 Response

The following figures show the measured S21 (frequency response) of the open loop VGA; due to pad numbers consideration, only the 16 different gain modes which is controlled by the binary search can be measured in this open loop prototype. The primitive printed file of highest and lowest gain mode that can be measured will be shown; and total 16 different S21 will be integrated in one diagram by graphic tool.

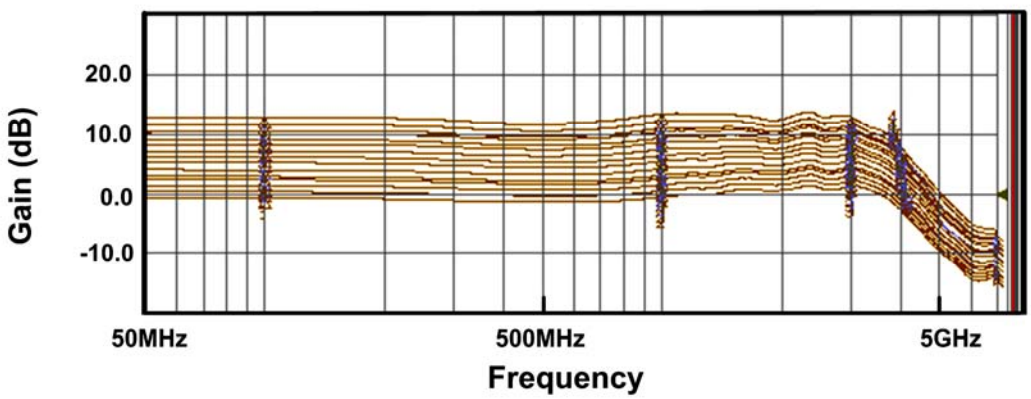
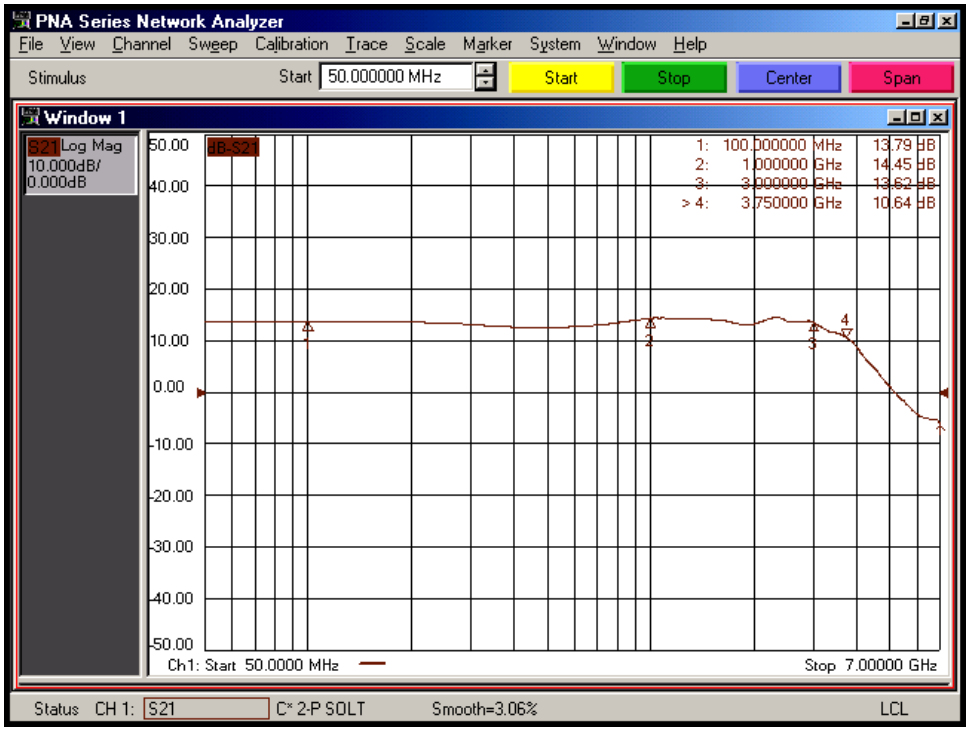
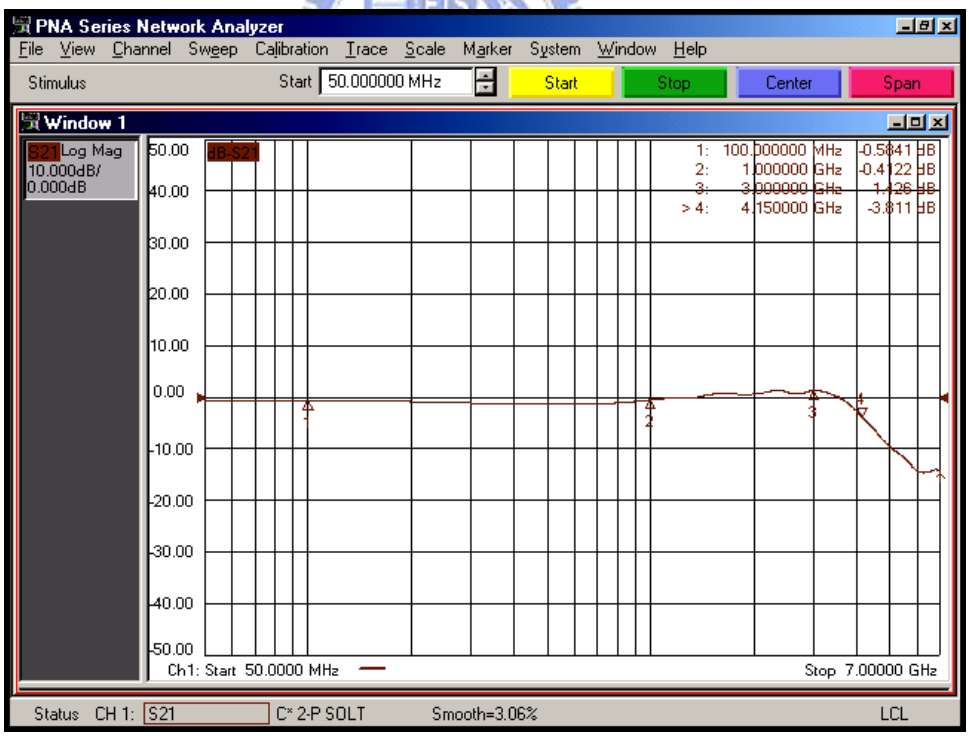


Fig. 4-5 Measured 16 different S21



(a)



(b)

Fig. 4-6 Measured S21 (a) high gain (b) low gain

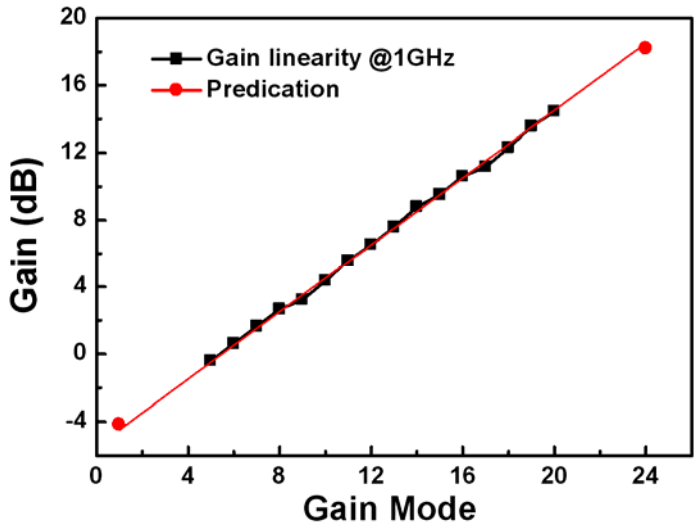
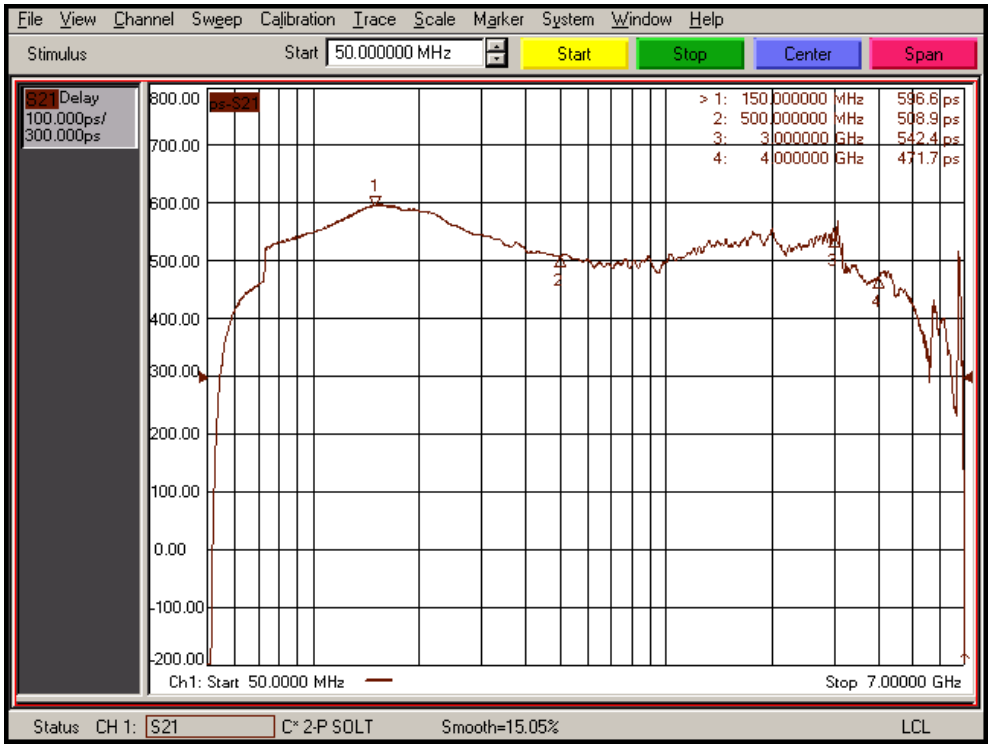


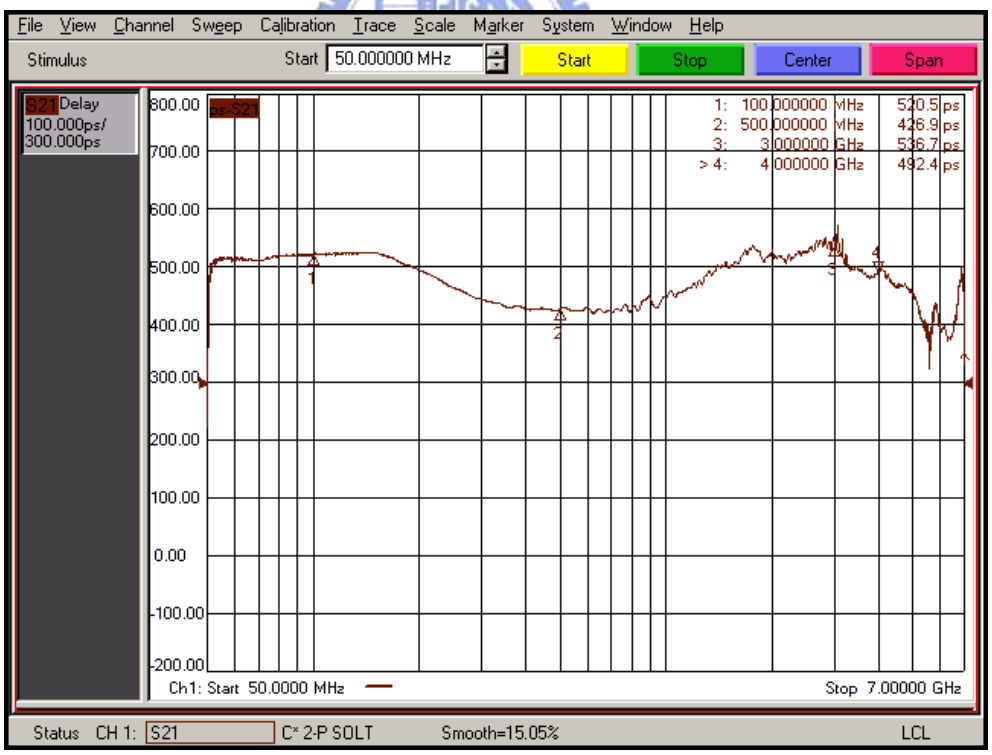
Fig. 4-7 Single-in-single-out gain linearity @ 1GHz

The above figure shows the gain linearity at 1GHz, and by approximation, the total VGA tunable range can be predicted. Knowing that the gain which is controlled by the linear search is set to the mid-gain and by the 16 measured different gain, the highest gain and lowest gain can be predicted to be 18.2dB and -4.1dB respectively, total tunable range will be 22dB. Because the network analyzer has just 2 ports and there is no available power divider whose frequency range is 50MHz to 5GHz, only gain of single-in-single-out can be measured, the exact differential-in-differential-out gain would be added 6dB, revealing that the differential gain range will be 1.9dB to 24.2dB, and 0.9dB/bit gain resolution.

The following figures show the measured group delay. Different gain mode will have an obviously different result at mid frequency; briefly said, group delay at mid frequency will increase but that at high frequency will remain the same. Roughly, the group delay variation will be about 100ps within 100MHz to 4GHz at each gain mode.



(a)



(b)

Fig. 4-8 Measured group delay (a) high gain (b) low gain

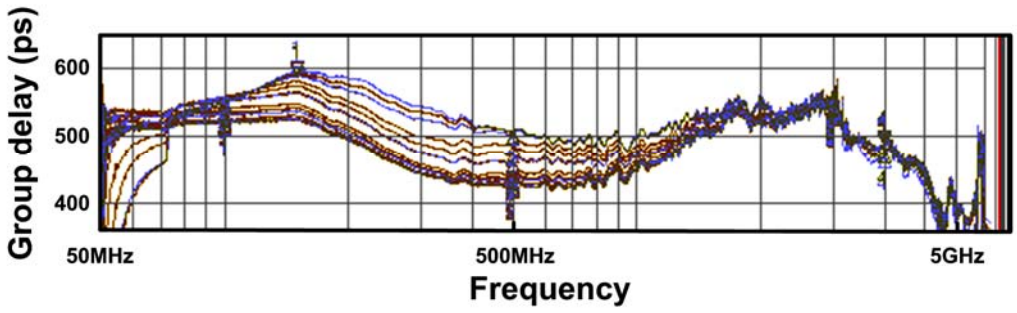


Fig. 4-9 Measured 16 different group delay

4.3.2 Eye Diagram

Fig. 4-10 to Fig. 4-17 show the measured 4-PAM eye diagram with different input and different gain, and both high gain mode and low gain mode output swing is near 500mV_{pp}.

4-PAM input data is generated by the AWG, due to the finite DAC resolution and sample rate of it, the input data is not an ideal one, and affects the output eye performance directly; when the data rate is 8Gbps, the output eye will has a visible opening. The input amplitude variation can be accomplished by the different attenuators; but with attenuators, the input will be noisy which can be discovered in the figure of high gain input eye. Due to there is no available 4-PAM modulator and demodulator, bit error rate is not measured here, and will be part of the future work. As a contrast, there are 2^{24}-1 PRBS measured results with a clear eye opening in Fig. 4-18 to Fig. 4-21, and the bit error rate could be less than 10^{-12}.

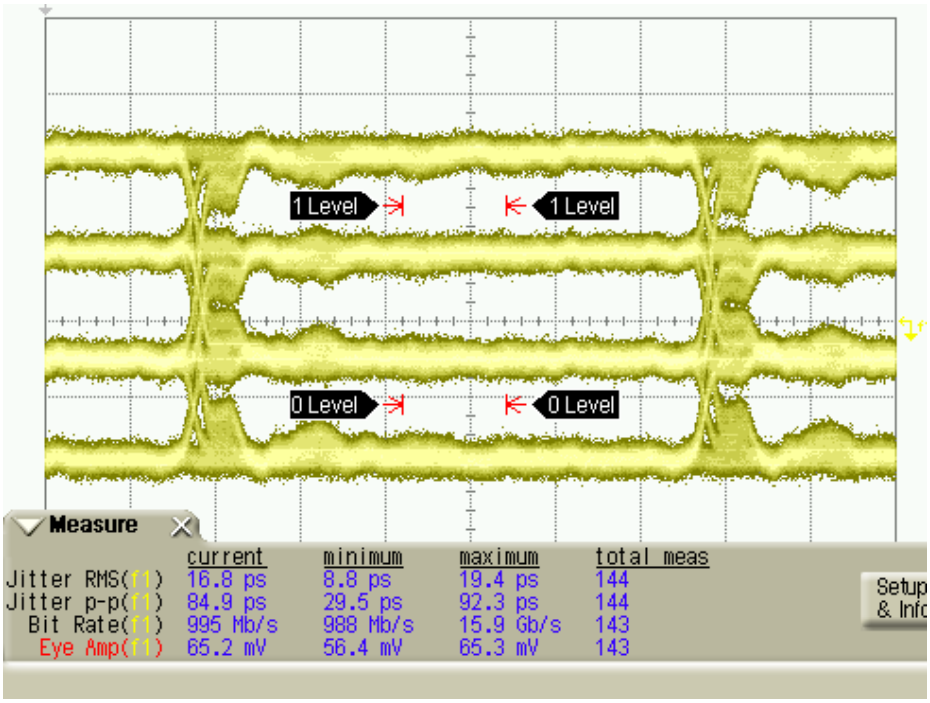


Fig. 4-10 2Gbps 4-PAM input eye @ gain = 15dB

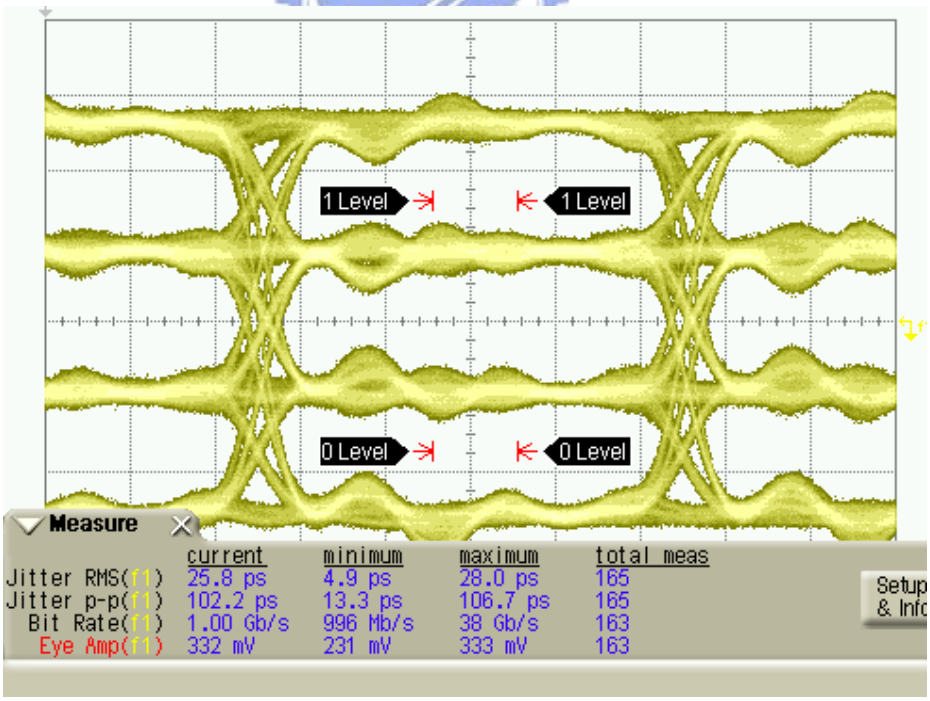


Fig. 4-11 2Gbps 4-PAM eye diagram @ gain = 15dB

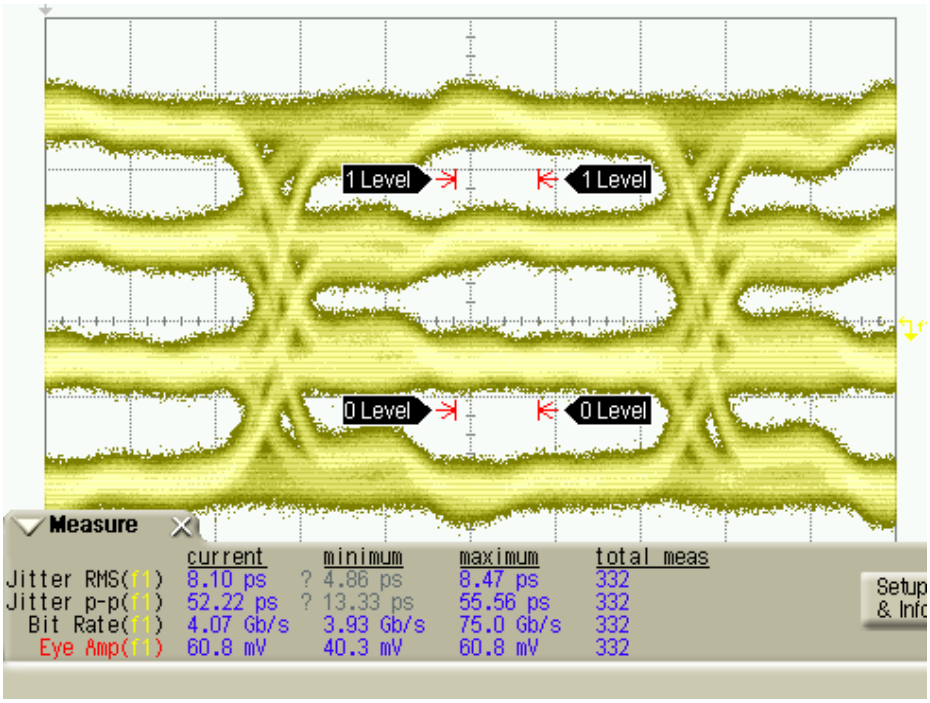


Fig. 4-12 8Gbps 4-PAM input eye @ gain = 15dB

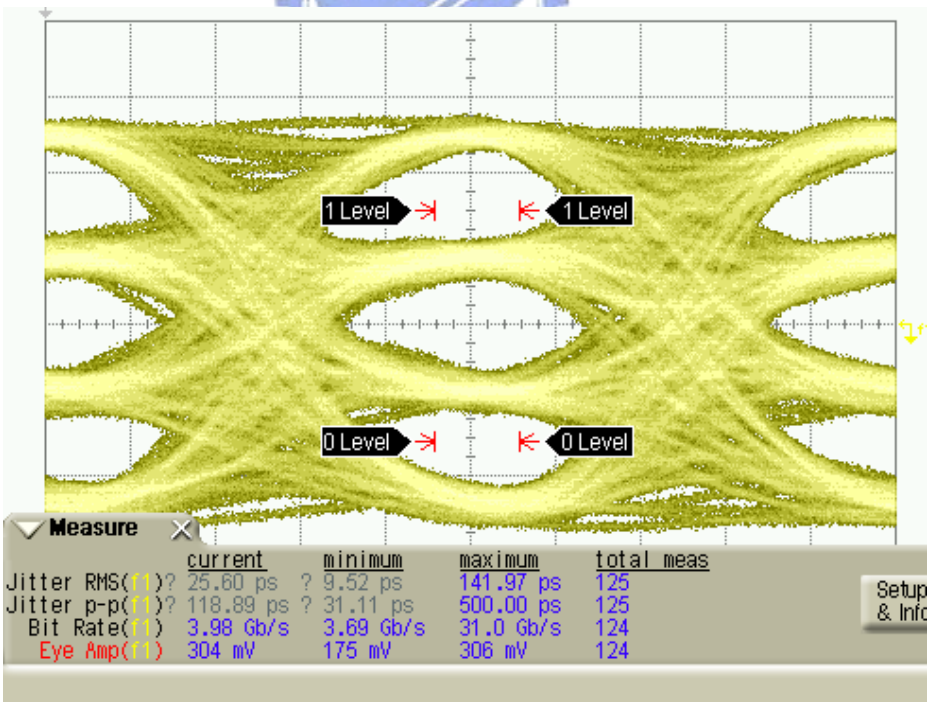


Fig. 4-13 8Gbps 4-PAM eye diagram @ gain = 15dB

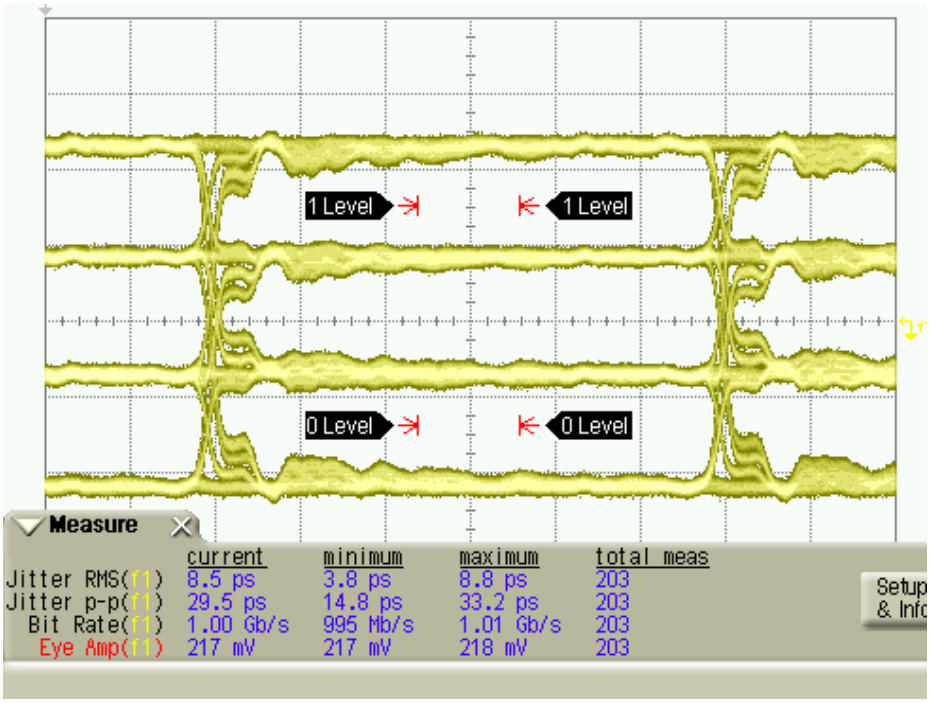


Fig. 4-14 2Gbps 4-PAM input eye @ gain = 5dB

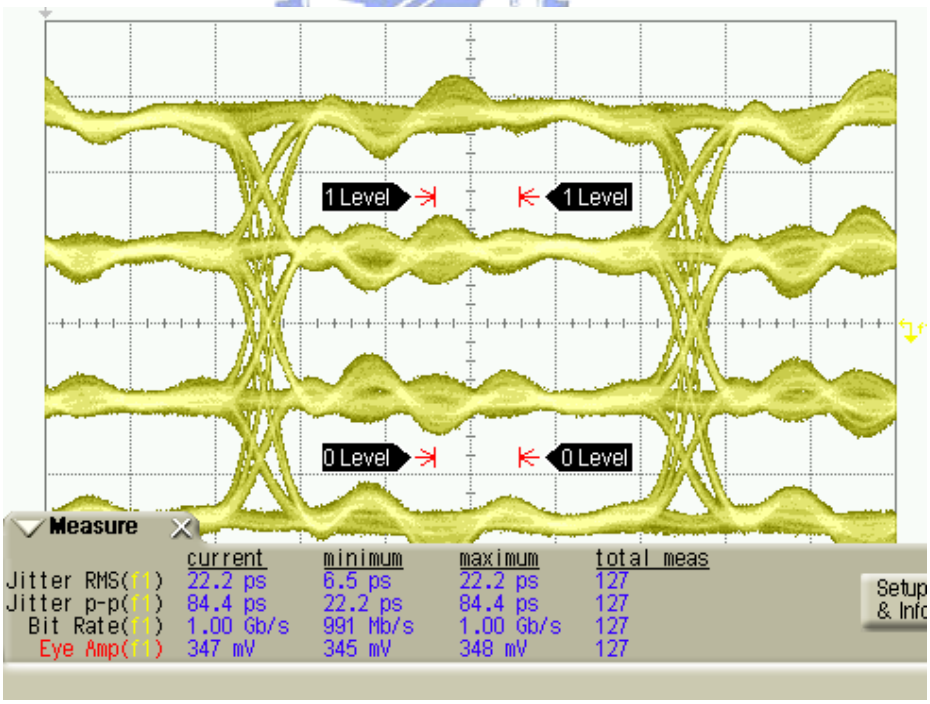


Fig. 4-15 2Gbps 4-PAM eye diagram @ gain = 5dB

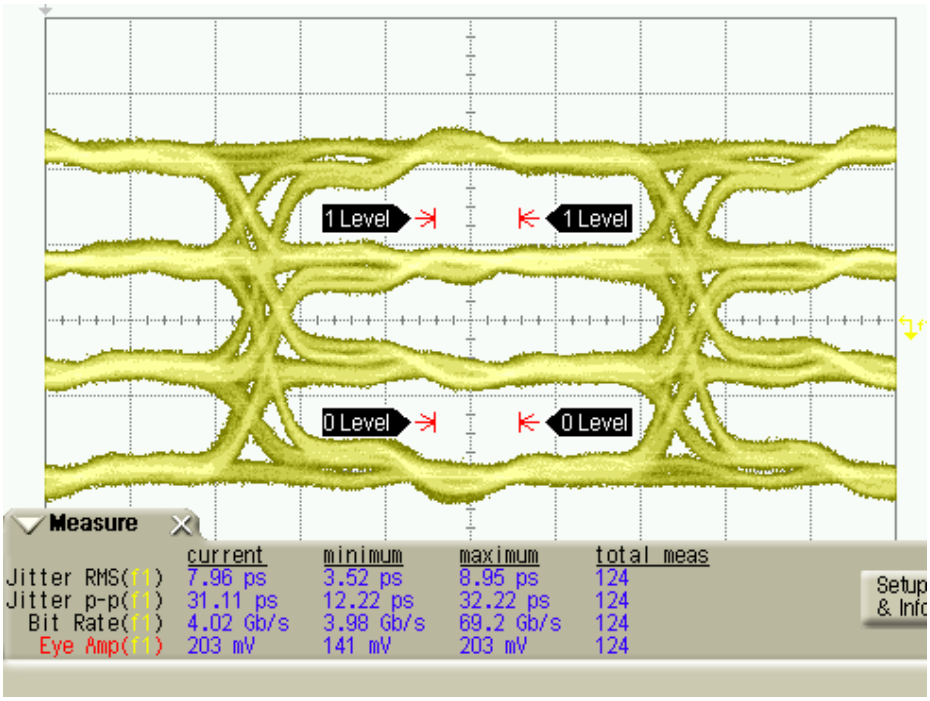


Fig. 4-16 8Gbps 4-PAM input eye @ gain = 5dB

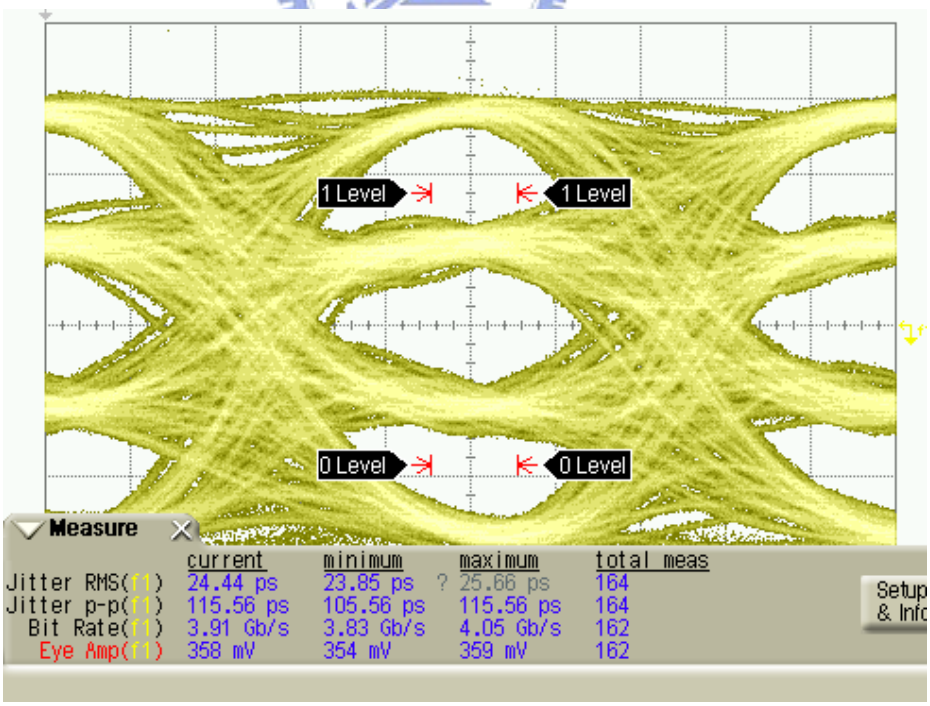


Fig. 4-17 8Gbps 4-PAM eye diagram @ gain = 5dB

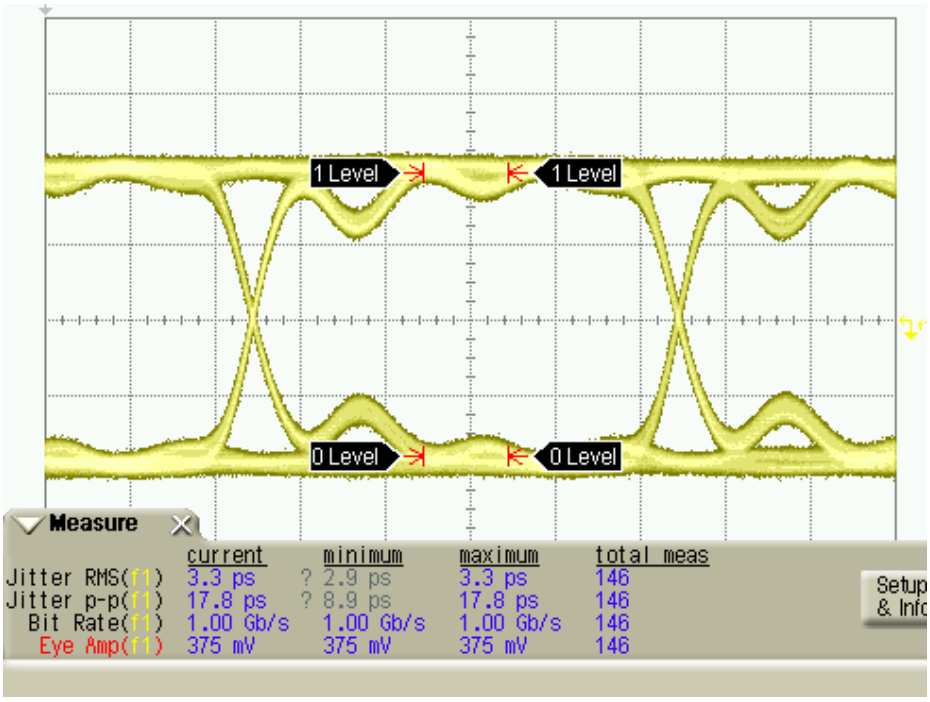


Fig. 4-18 1Gbps PRBS eye @ gain = 15dB

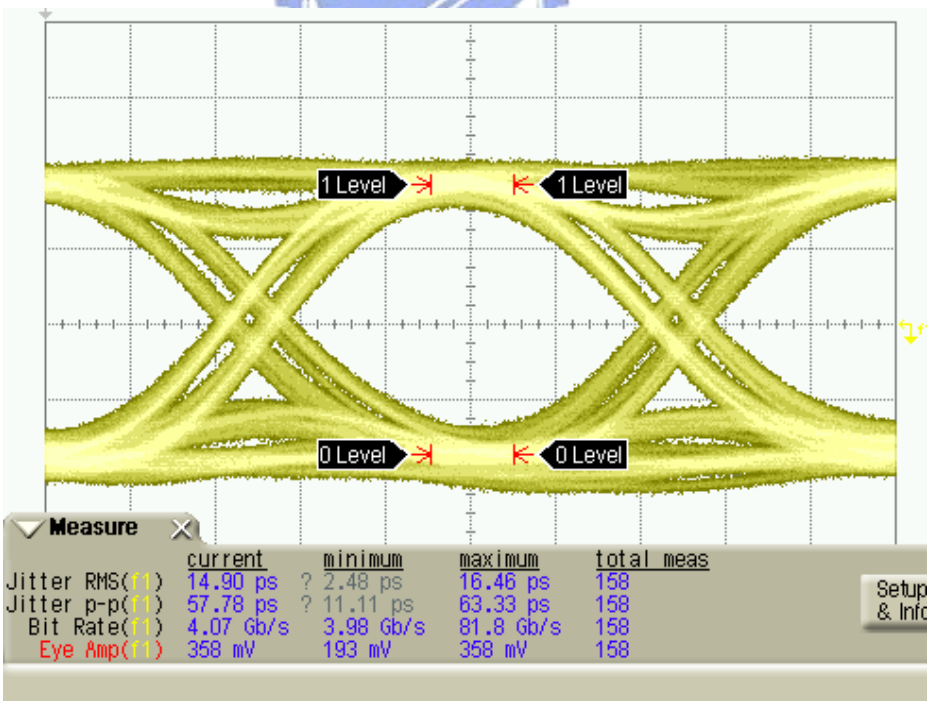


Fig. 4-19 4Gbps PRBS eye @ gain = 15dB

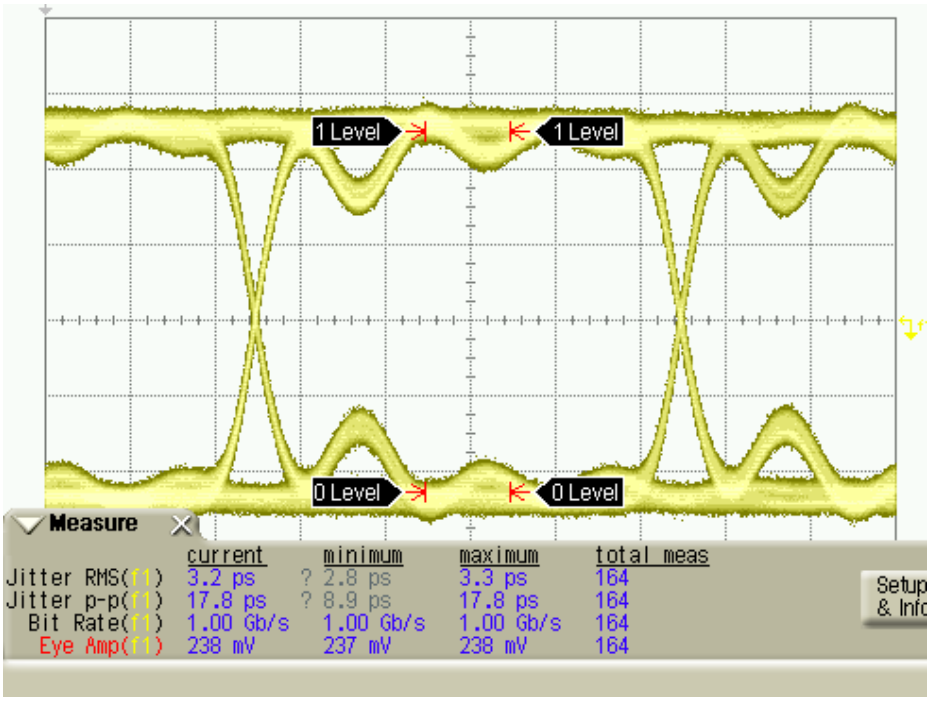


Fig. 4-20 1Gbps PRBS eye @ gain = 5dB

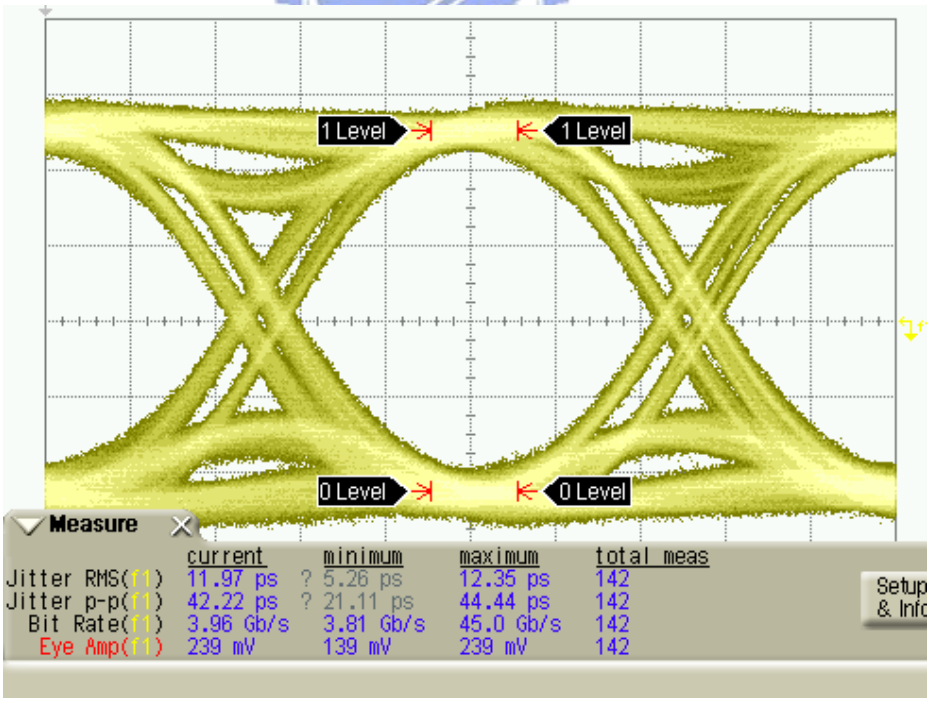


Fig. 4-21 4Gbps PRBS eye @ gain = 5dB

4.3.3 Settling Time

The following figures show the measured input and output amplitude. With different input, the binary search engine will settle down at different gain mode. Notice that the input signal is single-in, the exact input amplitude should be twice. A reset signal will be sent when the input signal is varied; after the reset signal, the binary search will start and comes in to an end after 170ns. An enlarged picture during 700ns and 120ns will be shown in the next figure, and giving a clearly view of the settling process

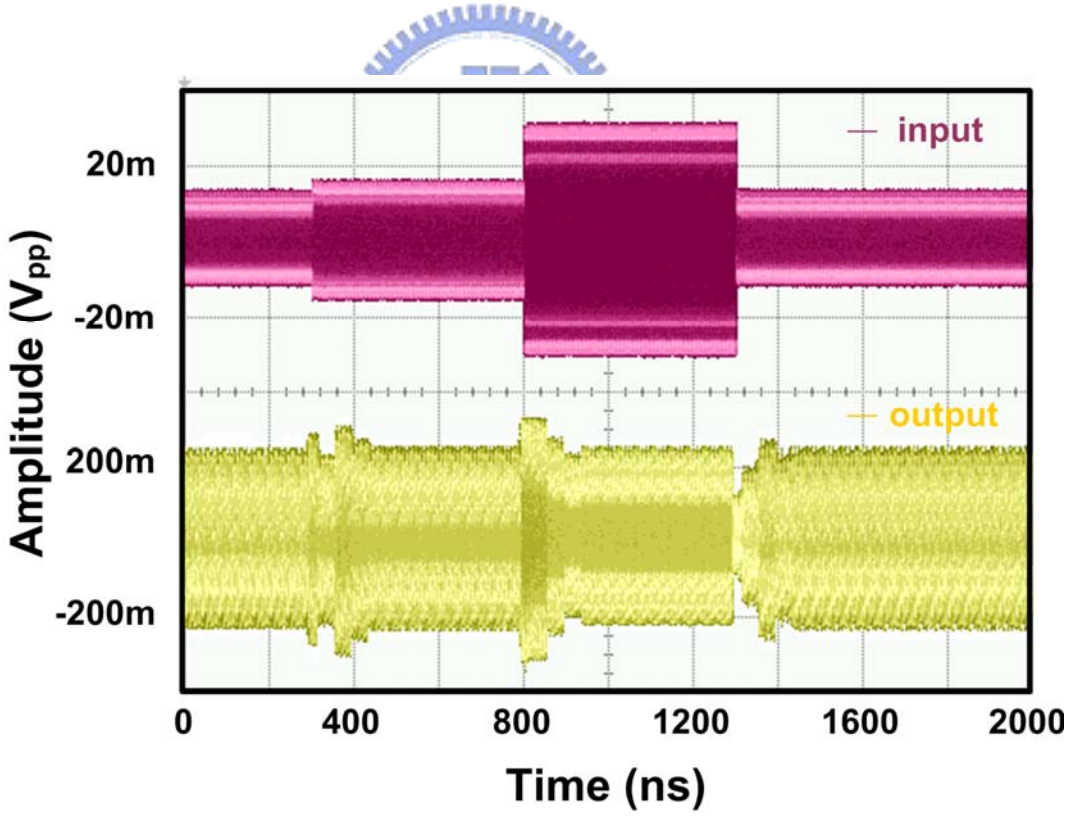


Fig. 4-22 Input and output amplitude variation

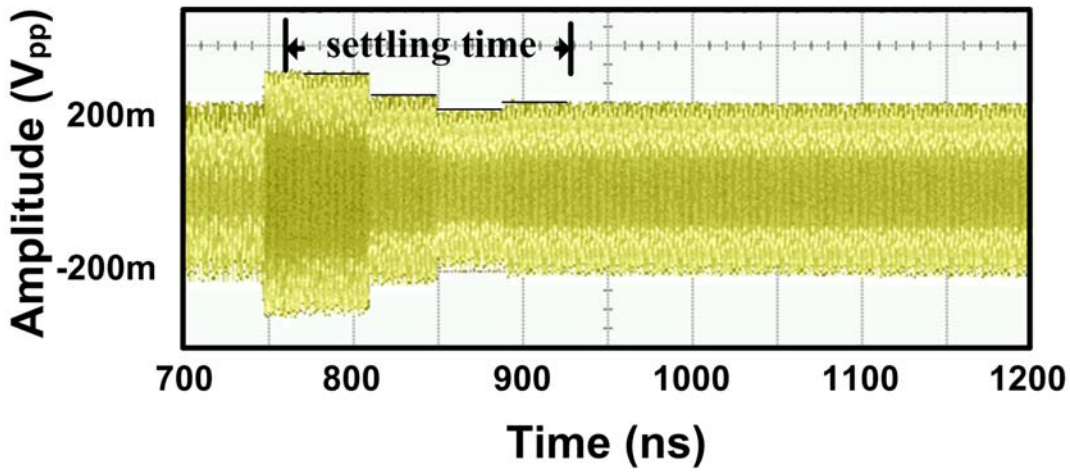


Fig. 4-23 Enlarged time diagram @ binary gain mode 0011

There is no linear search result because it seems that the linear search circuit does not work; but with 100MHz clock rate, the preliminary search (binary search) is working as we wish, and the settling time is less than 200ns.

4.4 Benchmark

Item	2006 ISSCC [7]	2007 ISSCC [10]	2008 ISSCC [11]	2008 TCAS [5]	This work
Technology	0.18μm CMOS	90nm CMOS	0.25μm SiGe	0.18μm CMOS	0.18μm CMOS
Supply voltage	1.8V	1.2V	2.7V	1.8V	1.8V
Data type	Binary	Binary	Burst mode	Binary	4-PAM
Gain mode	continuous	continuous	2	continuous	24
Dynamic range	35dB BER<10^{-12}	19dB BER<10^{-9}	12.2dB BER<10^{-10}	28.5dB BER<10^{-12}	22dB
max gain	25dB	N/A	N/A	18.5dB	24dB*
Data rate	10Gbps	40Gbps	9.8Gbps	1.25 Gbps	8Gbps
Settling time	N/A	N/A	<6ns	1.6μs	BS 170ns** LS 210ns***
Inductor	Yes	Yes	No	No	No
Chip area	1.5 x 0.88 mm^2	0.56 mm^2 TIA+AGC	N/A	0.82 x 0.56 mm^2	0.62 x 0.62 mm^2
Power	54mW	75mW	400mW	43.2mW	86.4mW

* Buffer included; ** Clock rate @ 100MHz; *** Simulation result

Table 4-2 Performance benchmark

The above table is the benchmark and concludes the performance of this work. Comparing to the AGC which is composed of inductors like [7] and [10], this work has no inductors and saves the chip area in standard 0.18μm CMOS technology. The power dissipation will be much smaller than [11], which has no

inductor but implemented in SiGe process. Using digital circuit to replace the loop filter, settling time is a remarkable achievement.

Chapter 5 Conclusion

5.1 Conclusion

An inductor-less, high data rate, fast response, digitally controlled AGC is proposed for PAM receiver in this thesis. Its characteristics are summarized as following:

1. Nested active feedback prototype is adopted in the VGA design, for wide band operation.
2. The transfer function of the VGA is reflected to a Bessel type filter, to alleviate group delay variation,
3. There is a 20dB input dynamic range for this AGC; with 24 gain control bits, gain resolution can be smaller than 1dB/bit.
4. Dual gain searching mode for both rapid settling time and long term stability.
5. System settling time is less than 200ns and will not depend on the gain mode or number of changed bits.
6. Without inductors, chip size is only 0.62 x 0.62 mm^2.

5.2 Future Work

After this work, the total optical receiver system integration can be the succeeding target. Integrated with a high performance CMOS photo detector, wide band TIA, succeeding PAM demodulator and CDR circuit, even with an equalizer or applied in a multi channel system, can be the challenging purpose.

In this AGC design, encoder of the binary search and linear search can be further combined; that is, the two-way shifting mechanism of linear search can be applied in the synchronizing DFF of the binary search encoder. After this combination, total 24 gain control bits can be acquired rapidly by 5-times binary search, and using the two-way shift register with MUX as the DFF for binary search synchronization, the settling time and stability of this AGC can be improved.

Bit error rate and sensitivity of this AGC is not measured because there is no available PAM modulator and demodulator; these circuits could be implemented in the future for measurement concern; on the other hand, the parasitic effects of the input pads, bonding wire, and PCB are not considered carefully, and it may leads to a worse measured S21 response.

In open loop measurement, the linear search encoder works normally, it means that the two-way shift register is not failed; however, the linear search does not work when the settling time is measured, the detailed reason should be checked.

Appendix A Analysis of AGC Loop

In section 2.1.2, a typical AGC model with a logarithmic amplifier is analyzed, and the relationship between V_{IN}, V_{OUT} and V_{REF} is shown. However, if the logarithmic amplifier does not exist in the real circuit, will the conclusions be consistent?

Fig. A-1 shows this model: an AGC loop without the logarithmic amplifier; another key assumption in the following derivation will be that the output amplitude of the AGC loop is operating near its fully converged state, that is, $A_{OUT}(t) \fallingdotseq V_{REF}$.

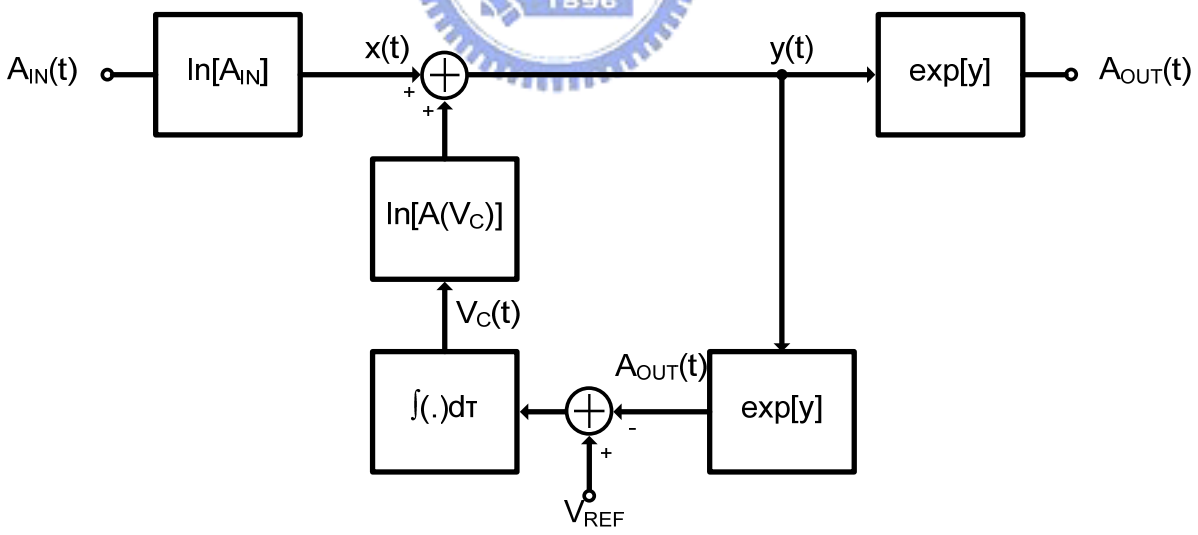


Fig. A-1 Model for analog AGC loop without log amp

As shown in Fig. A-1, x(t) and y(t) are A_{IN} and A_{OUT} in logarithm form,

$$y(t) = x(t) + \ln[A(V_C)] \tag{A-1}$$

and the gain control signal V_C is derived as

$$V_C(t) = \int_0^t \tau_{\text{int}} \cdot [V_{REF} - A_{OUT}(\tau)] d\tau = \frac{1}{\tau_{\text{int}}} \int_0^t [V_{REF} - e^{y(\tau)}] d\tau \tag{A-2}$$

where τ_{int} is the time constant of the integrator.

Taking the derivative of (A-1) and substituting the derivative of (A-2) into it, the following equation can be derived:

$$\frac{dy}{dt} = \frac{dx}{dt} + \frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} \cdot \frac{1}{\tau_{\text{int}}} \cdot [V_{REF} - e^{y(t)}] \tag{A-3}$$

If the coefficient of the second term of (A-3) is forced to be a constant C,

$$\frac{1}{A(V_C)} \cdot \frac{dA(V_C)}{dV_C} \cdot \frac{1}{\tau_{\text{int}}} = C \tag{A-4}$$

and taking the Taylor series of e^y at y=z (where $e^z = V_{REF}$),

$$e^y \approx e^z + \frac{e^z (y-z)}{1!} + \frac{e^z (y-z)^2}{2!} + \Lambda\ \Lambda \tag{A-5}$$

Due to the last assumption, $A_{OUT}(t) \fallingdotseq V_{REF}$, (A-5) can be simplified into the first order equation:

$$e^{y} \approx e^{z} + e^{z}(y-z) = V_{REF}(1+y-z) \quad \textbf{(A-6)}$$

Substituting (A-4) and (A-6) into (A-3), there will be a linear relationship between x(t) and y(t):

$$\frac{dy}{dt} + C \cdot V_{REF} \cdot y(t) = \frac{dx}{dt} + C \cdot V_{REF} \cdot \ln[V_{REF}] \quad \textbf{(A-7)}$$

(A-7) could be transferred into frequency domain as

$$y = \frac{s}{s + C \cdot V_{REF}} \cdot x + \frac{C \cdot V_{REF}}{s + C \cdot V_{REF}} \cdot \ln[V_{REF}] \quad \textbf{(A-8)}$$

When the reference voltage is a constant, VGA gain needs to be linear-in-dB to the control signal to get a constant settling time for the AGC loop. Except that the loop bandwidth will not depend on the gain of the log amp but the reference voltage, most of the conclusions in section 2.1.2 remain the same.

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