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應用於太陽能之有效率的電源管理系統

An Efficient Power Management System for

Solar Energy Harvesting Applications

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摘　　要

在本篇論文中，我們將目標放在設計並實現一個應用於太陽能之有效率的電源管理系統。這將包含電壓調節器、參考電壓產生器以及電荷幫浦的設計。

此次的研究發展出以下的結果：

1. 擁有高電流效益以及對負載有快速反應能力的新電壓調節器被提出。
2. 一個新的連接方法被提出，用於改善產生高電壓之電荷幫浦的能量效益。此電荷幫浦電路可以用標準的 CMOS 製程來實現並且無須使用特別的光罩來避免 CMOS 崩潰。
3. 一個應用於太陽能之有效率的電源管理系統被提出。此電源管理系統與一個可重複充電的電池工作，並且有效率的利用電池的能量。
4. 此電源管理系統接收太陽能電池的能量，並提供 500mV、-500mV 以及 1V 給運算電路以及記憶體電路。

An Efficient Power Management System for Solar Energy Harvesting Applications

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ABSTRACT

The goal of the thesis is to design and implement an efficient power management system for solar energy harvesting applications. This includes the design of voltage regulator, reference voltage generator and charge pump.

The result of this study has developed following results:

1. New voltage regulator with high current efficiency and fast load regulation is proposed.
2. A novel connect scheme is proposed for improving power efficiency of charge pump which generates ultra high voltage. The proposed charge pump circuit can be implemented in standard CMOS process without using special mask to prevent the breakdown of CMOS.
3. An efficient power management system for solar energy harvesting applications is proposed. The power management system works with a rechargeable battery and efficiently uses the energy of battery.
4. The power management system accepts energy from photovoltaic cell and outputs 500mV, -500mV and 1V for computation circuitry and memory circuitry.

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Chapter 1
Introduction

1.1 Motivation of the Thesis

In the recent years, the market of portable devices likes notebook, cell phone, PDA and smart phone is grow up rapidly and more new portable products will be developed in the near future. In the developing of portable devices, more and more functions are integrated into a product. At the same time, people concern that whether the product can use for a long time without charging the battery in charge socket. Recently, the price of oil keeps going up. This will impact the electric bill and cost of expense. To increase the utility time and lower the cost of expense, the low power techniques are urgent need. In alternative way, people look for the new alternative energy actively. Environmental energy like solar power, heat power and wind power is used for generating electric power.

Due to energy crisis and eco-awareness, the research of energy harvesting application is getting popular. Previously, the system of tracking maximum output power of photovoltaic cell was implemented [1]. An ultra-low voltage power management for energy harvesting applications was developed and worked with a FIR filter [2]. With low output voltage of solar cell, a micro power management system was proposed [3]. The micro power management system decided the working frequency of charge pump by the room lighting environment and outputted the maximum power to loading circuitry. An energy harvesting application with micro battery was also implemented [4]. This power management circuit accepted energy from RF power and thermo generator power and outputted the power to micro battery as energy storage. A battery management system for solar energy applications was developed [5]. The battery management system was used to increase the service life of the battery.

1.2 Research Goals and Contributions

The goal of this research is to design and implement an efficient power management system for solar energy harvesting applications. This includes the design

of voltage regulator, reference voltage generator and charge pump.

The contributions of this thesis are list as follow:

1. New voltage regulator with high current efficiency and fast load regulation.
2. A novel connect scheme for improving power efficiency of charge pump which generates ultra high voltage.
3. An efficient power management for solar energy harvesting applications. The power management system works with a rechargeable battery and efficiently uses the energy of battery.

1.3 Thesis Organization

The rest of the thesis is organized as follows: an overview of solar energy harvesting applications technique is introduced in the Chapter 2. The characteristics of photovoltaic (PV) cell and a maximum peak power tracking technique are introduced. The detail circuit of previous power management system for solar energy harvesting applications is also introduced.

The techniques of improving the stability and transient response of voltage regulator are introduced in the Chapter 3. The new voltage regulators with high current efficiency and fast load regulation are proposed in the Chapter 3.

The voltage doubler and Dickson charge pump are introduced in the Chapter 4. The techniques of improving the pumping efficiency of charge pump are also introduced. For improving the power efficiency of charge pump which generates ultra high voltage, a novel connect scheme is proposed in the Chapter 4.

An integrated power management system for solar energy harvesting applications is proposed in the Chapter 5. The power management system contains the new voltage regulator in Chapter 3 and the new charge pump in Chapter 4. The power management system has two power sources. Thus, a control unit is proposed to decide who will supplies energy to the power management system. The control unit also helps the power management system efficiently using the energy from battery.

Chapter 2
An Overview of Solar Energy Harvesting Applications

In this chapter, it introduces the overview of solar energy harvesting applications. The photovoltaic (PV) cell would be described in Section 2.1. A maximum peak power tracking would be introduced in Section 2.2. Section 2.3 and Section 2.4 introduce two power management systems for solar energy harvesting applications. Finally, Section 2.5 introduces the battery management system for solar energy harvesting applications.

2.1 Photovoltaic (PV) Cell

The photovoltaic cell is used to convert the light energy into electrical energy. The photovoltaic cell is a nonlinear device and can be represented as a current source model, as shown in Fig. 2.1. The traditional I-V characteristic of a photovoltaic cell, when neglecting the internal shunt resistance, is given by the following equation [6]:

$$I_o = I_g - I_{sat}\left\{\exp\left[\frac{q}{AKT}\left(V_o + I_o R_s\right)\right] - 1\right\} \quad (2.1)$$

Where I_o and V_o are the output current and output voltage of the photovoltaic cell, respectively, I_g is the generated current under a given insolation, I_{sat} is the reverse saturation current, q is the charge of an electron, K is the Boltzmann's constant, A is the ideality factor for a p-n junction, T is the temperature (K), and R_s is the intrinsic series resistance of the solar array.

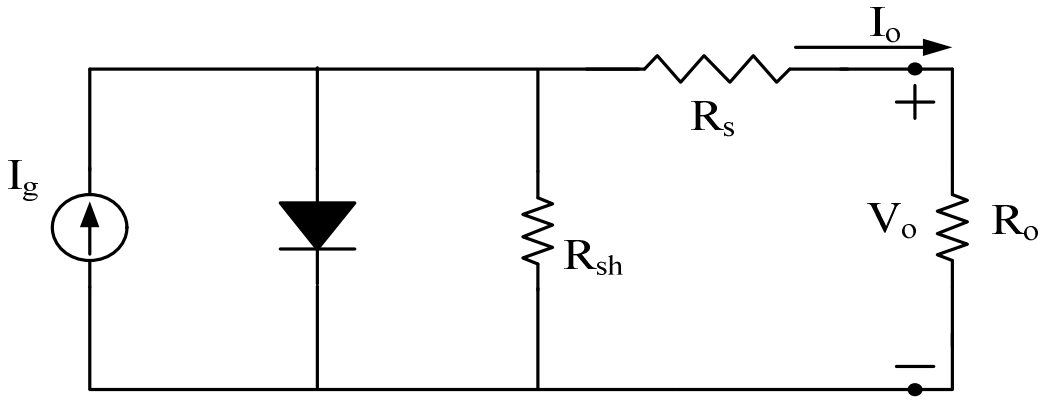


Fig. 2.1 Equivalent circuit of a photovoltaic cell.

The saturation current of the photovoltaic cell varies with temperature according to the following equation [6]:

$$I_{sat} = I_{or}\left[\frac{T}{T_r}\right]^3 \exp\left[\frac{qE_{GO}}{KT}\left(\frac{1}{T_r}-\frac{1}{T}\right)\right] \tag{2.2}$$

$$I_g = \left[I_{sc} + K_I\left(T_c - 25\right)\right]\frac{\lambda}{100} \tag{2.3}$$

Where I_{or} is the saturation current at T_r, T is the temperature of the photovoltaic cell (K), T_r is the reference temperature, E_{GO} is the band-gap energy of the semiconductor used in the solar array, K_I is the short-circuit current temperature coefficient and λ is the insolation in mW/cm^2. In literature, instead of the I-V characteristic given by (2.1) the following I-V characteristic is used to compute the output voltage of the PV cell:

$$V_o = -I_o R_s + \frac{AKT}{q}\ln\left[\frac{I_q - I_o + I_{sat}}{I_{sat}}\right] \tag{2.4}$$

From above equations, the electric power generated by a photovoltaic cell fluctuates depending on the solar radiation value and temperature, as shown in Fig. 2.2.

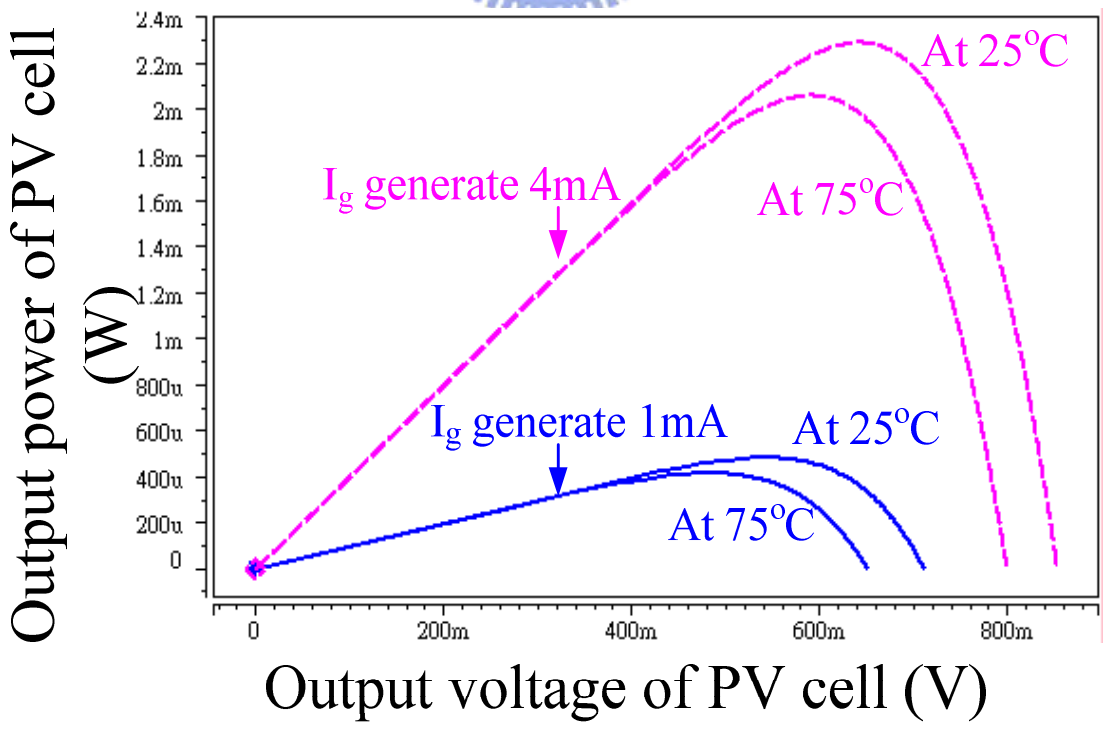


Fig. 2.2 P-V curve of photovoltaic cell under different temperature.

2.2 Maximum Power Point Tracking and Control Algorithm

2.2.1 MPPT Process

The electrical characteristic of the PV under a given insolation is illustrated in Fig. 2.3. For different loadings, the PV cell will operate at different point, either in current source region or in voltage source region, where the output current or voltage almost keeps a constant. In other words, the internal impedance of the solar array is low on the right side of the curve and high on the left side. The maximum output power point of PV cell exists at the crossing point of the two regions. According to the maximum power transfer theory, the power delivered to the load is maximum when the source internal impedance matches the load impedance. Thus, the impedance seen from the converter side (which can be adjusted by controlling the duty cycle) needs to match the internal impedance of the solar array if the system is required to operate close to the maximum power point of the photovoltaic cell.

Most traditional dc/dc converters have a negative impedance characteristic inherently, due to the fact that their current increases when voltage decreases. This behavior is due to the constant input power and the adjustable output voltage of the power supply. If the system operates on the high-impedance (low-voltage) side of the PV cell characteristic curve, the output voltage of PV cell will collapse. Therefore, the PV cell is required to operate on the right side of the curve to perform the tracking process. Otherwise, the converter will operate with the maximum duty cycle, and the output voltage of PV cell will only change with the insolation. Thus, the system cannot achieve maximum power tracking and might even mistake the present operating point for the maximum power point.

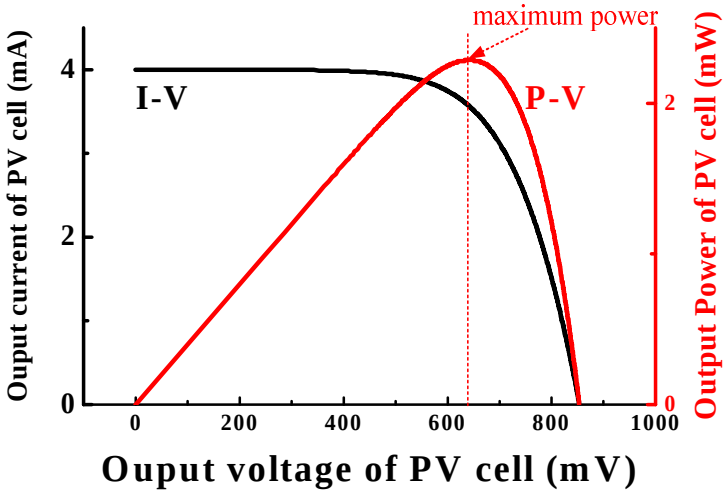


Fig. 2.3 The characteristic curves of PV cell.

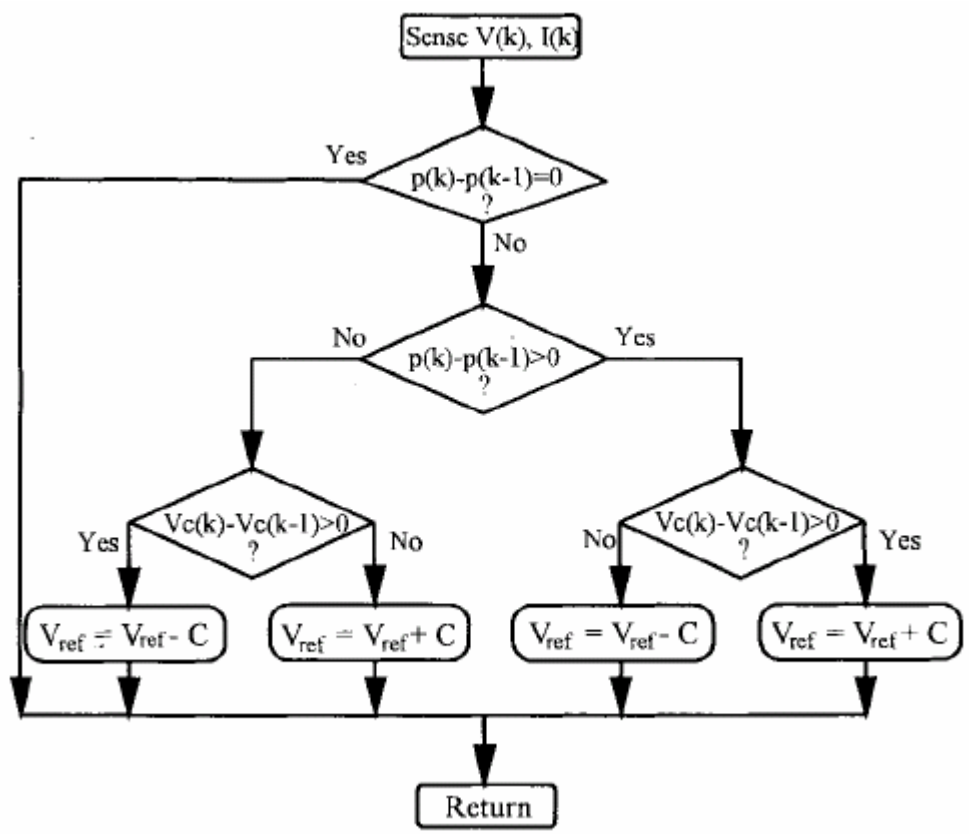


Fig. 2.4 The flowchart of MPPT control.

The control flowchart of the maximum power tracking system is shown in Fig. 2.4[1]. If a given perturbation leads to an increase in output power of PV cell, the next perturbation is made in the same direction. In this way, the maximum power tracker continuously seeks the maximum power point.

2.2.2 Control Algorithms for MPPT

Two control algorithms often used to achieve the maximum power point tracking are the perturbation and observation method and the incremental conductance method. Although the incremental conductance method offers good performance under rapidly changing atmospheric conditions, four sensors are required to perform the measurements for computations and decision making [7]. If the sensors or the system require more conversion time, a large amount of power loss will result. On the contrary, if the sampling and execution speed of the perturbation and observation method is increased, then the system loss will be reduced. Moreover, this method only needs two sensors, which results in the reduction of hardware requirement and cost.

Two different control variables are often chosen to achieve the maximum power control [8].

1) Voltage Feedback Control: This method assumes that any variations in the insolation and temperature of the PV cell are insignificant and that the constant

reference voltage is and adequate approximation of the true maximum power point. The output voltage of PV cell is used as the control variable for the system. The system keeps the array operating near its maximum power points by regulating the output voltage of PV cell and matches to a fixed reference value.

The control method is simple, but it has the drawback of neglecting the effect of the insolation and temperature of the PV cell. This method cannot be widely applied in the battery energy storage systems. Therefore, the control method is only suitable for use under the constant insolation condition, such as a satellite system, because it cannot track the maximum power points of the PV cell when variations in the insolation and temperature occur.

2) Power Feedback Control: The actual output power of PV cell, instead of its estimate from measurements of other quantities, is used as the control variable. Maximum power control can be achieved by forcing the derivative (*dP/dV*) equal to zero under the power feedback control. A general approach to the power feedback control is to measure and maximize the power at the load terminal. However, it maximizes the power to the load, not the power from the PV cell. A converter with MPPT offers high efficiency over a wide range of operating points. The full power may not be delivered to the load completely, due to the power loss for a converter without MPPT. Therefore, the design of a high-performance converter with MPPT is a very important issue.

2.3 Ultra Low Voltage Power Management and Computation Methodology for Energy Harvesting Applications

An ultra low voltage power management system for energy harvesting applications is illustrated in Fig. 2.5[2].

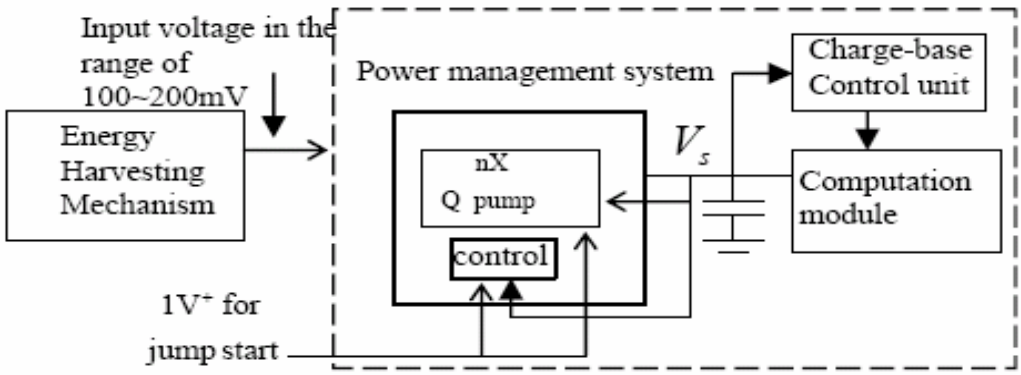


Fig. 2.5 Ultra low voltage power management system for energy harvesting applications.

The ultra low voltage power management system consists of four blocks, the energy harvesting mechanism, the power management system, the computation module and the charge-based control unit. A generic energy harvesting mechanism scavenges the energy from the environment, converts the energy into an electrical energy source and gives out an unregulated source voltage. Solar energy system is one example.

In this application, the output voltage of the energy harvesting mechanism is in the range of 100mV. The unregulated voltage is then input to the power management system. The power management system consists of a high conversion ratio integrated charge pump which steps up the voltage to >1V, and this unregulated voltage (Vs) then drives the controller such that the charge pump is self-powered once it is jump-started. The jump-start circuit can be a small primary battery that only needs to supply energy during start-up, and will be cut off from the system when self-powered operation is in place. To reduce the cost, the unregulated voltage (Vs) will be used directly by the computation unit. Therefore the computation unit has to cater for the fluctuation of the supply voltage. Because of the unstable source of the input energy, the energy may not be enough to sustain continuous operation of the computation. The charge-based control unit will make sure the energy available is enough for an atomic operation of the computation. Also it will trigger the calculation when enough energy is available.

2.3.1 Power Circuit

The power circuit of this power management system is shown in Fig. 2.6[2]. The power circuit mainly has two parts, a four stage 16x exponential charge pump circuit, and a clock generator. Since the voltage source V_{in} is around 80mv~200mv, the circuit needs a start up circuit, which only functions at the beginning of the circuit running. Once the circuit is started, the generated high voltage source V_{out} will provide the energy to the clock generator and cut the switch between the start-up voltage and the circuit. The circuit will then form an energy loop and be self powered, and at the same time provide energy to the outside circuit.

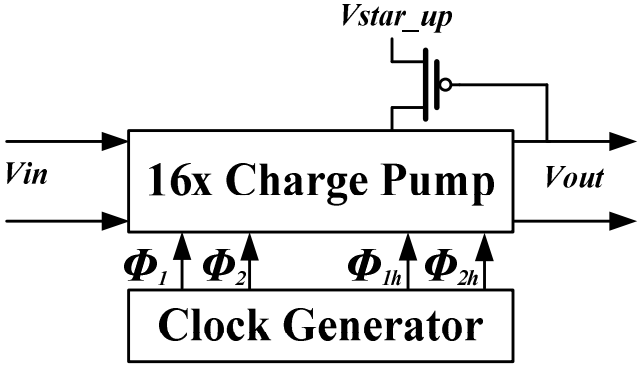


Fig. 2.6 Block diagram of the power circuit.

In the charge pump, two sets of clock driving signals are used: (φ1, φ2) and (φ1h,φ2h). The generators of these signals are shown in Fig. 2.7[2]. To save energy, in the generator for (φ1, φ2), all the inverters, except the last one of the buffer stage, has a swing between Vdd and Vin. For (φ1h,φ2h), the conventional level shifter is eliminated and a CMOS inverter is used to generate a driving signal swing between 2Vout and 4Vin. By doing so, the clock swing is reduced and the energy can flow back to some nodes in the charge pump circuit, which leads to more energy saving.

2.3.2 Computation Module

The power supply becomes unstable without the regulator. Variation in supply voltage affects the delay of the circuit and may cause timing problem for the computation. Therefore it is better if the computation unit can track the change of the supply voltage and automatically adjust the performance of the digital circuit to cater for the change. A self-time asynchronous pipeline design [9] is used to implement the computation module. In this case the operation of a pipeline stage is not dependent on a global clock but only on the completion of the previous stages. It is more robust over various operating conditions for its locally-generated timing signals and it is more suitable for the design to track with an unstable supply voltage. To simplify the asynchronous hand-shaking protocol and to cater for the static CMOS library, bundle delay method is used to implement the asynchronous pipeline. The bundle delay is designed to be a little bit larger than the computation delay with a safety margin for the process variation. When the supply voltage fluctuates, the bundle delay will automatically track the change and synchronize the computation in the pipeline. This can work over a large fluctuation in the supply voltage.

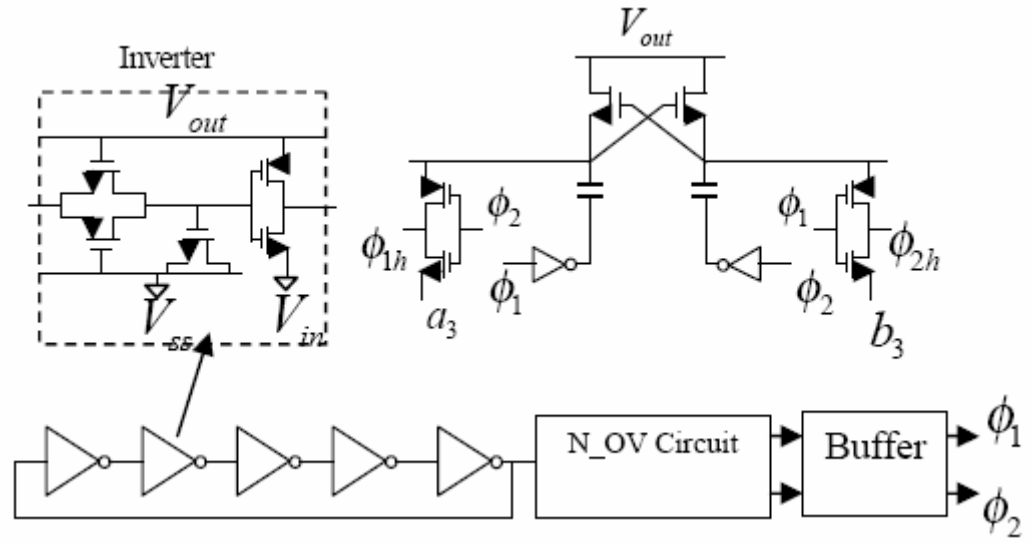


Fig. 2.7 Clock generator.

2.3.3 Charge-Based Control Unit

Due to the unpredictable nature of the energy source, sometimes the energy available at a particular time interval may not be enough for a certain computation and if system carries out the computation, the computation may not be able to finish and even worse the voltage may drop to a level that some of the stored data will be lost. To cater for this situation, a charge-based computation methodology is used. The charge required at different voltage levels for a certain atomic computation is estimated and stored in the device. The atomic computation refers to a computation that will results in data stored in the memory, or data output to external world and does not need to be used again. The atomic computation will only be triggered when the harvested energy can provide the charge for it with some margin. In addition, a supply-side paradigm of computation is used. For some very low energy applications, such as environmental data collection using wireless sensor device, the computation does not have a hard deadline requirement. Based on the energy available, the system can decide whether an operation should be triggered and executed. Moreover, the computation can be prioritized, both in task level or bit level (an example of bit level priority is multiple bit resolution). Depending on the energy available and the priority, different computations will be executed based on the decision of the charge-based control unit.

2.4 A Micro Power Management System with Maximum Output Power Control for Solar Energy Harvesting Applications

The micro power management system with maximum output power control for solar energy harvesting applications is shown in Fig. 2.8[3].

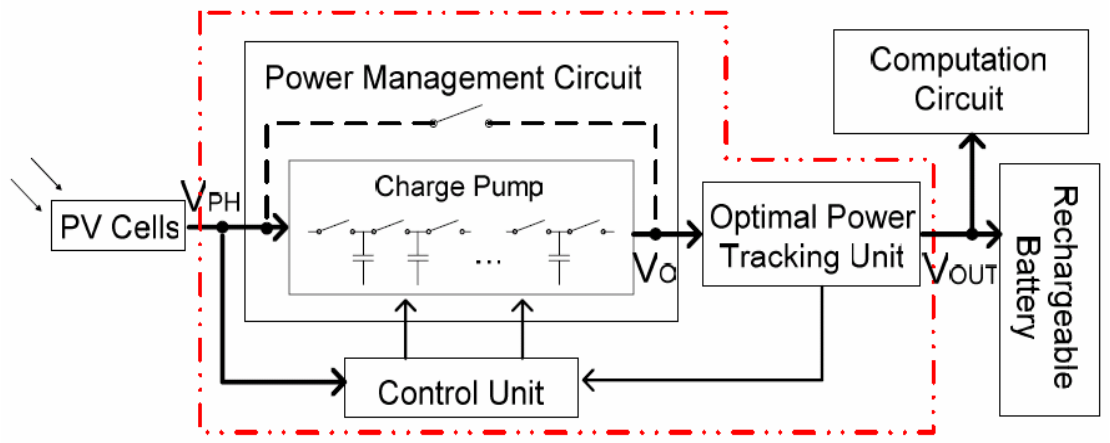


Fig. 2.8 Block diagram of micro power management system with maximum output power control for solar energy harvesting applications.

To cater for different light intensities, the micro power management system tracks the voltage of the PV cells and the battery to determine whether the charge pump is used or bypassed. Under low light intensity, the PV voltage is low and the charge pump steps up the voltage either for charging the rechargeable battery or powering the computation circuit. At the same time, the optimal power tracking unit monitors the charge pump output power and determines the adjustment of the system operating parameter. Based on the adjustment decision, the control unit tunes the operating frequency of the charge pump in order to maximize the system power output. Rechargeable battery is used to support the system continuous operation even when the light source is out.

2.4.1 Optimal Power Tracking Unit

In order to supply maximum power to charge the battery or to directly drive the computation circuit, the optimal power tracking unit is used to monitor the amount of power flowing out of the charge pump. The detail circuit is shown in Fig. 2.9[3].

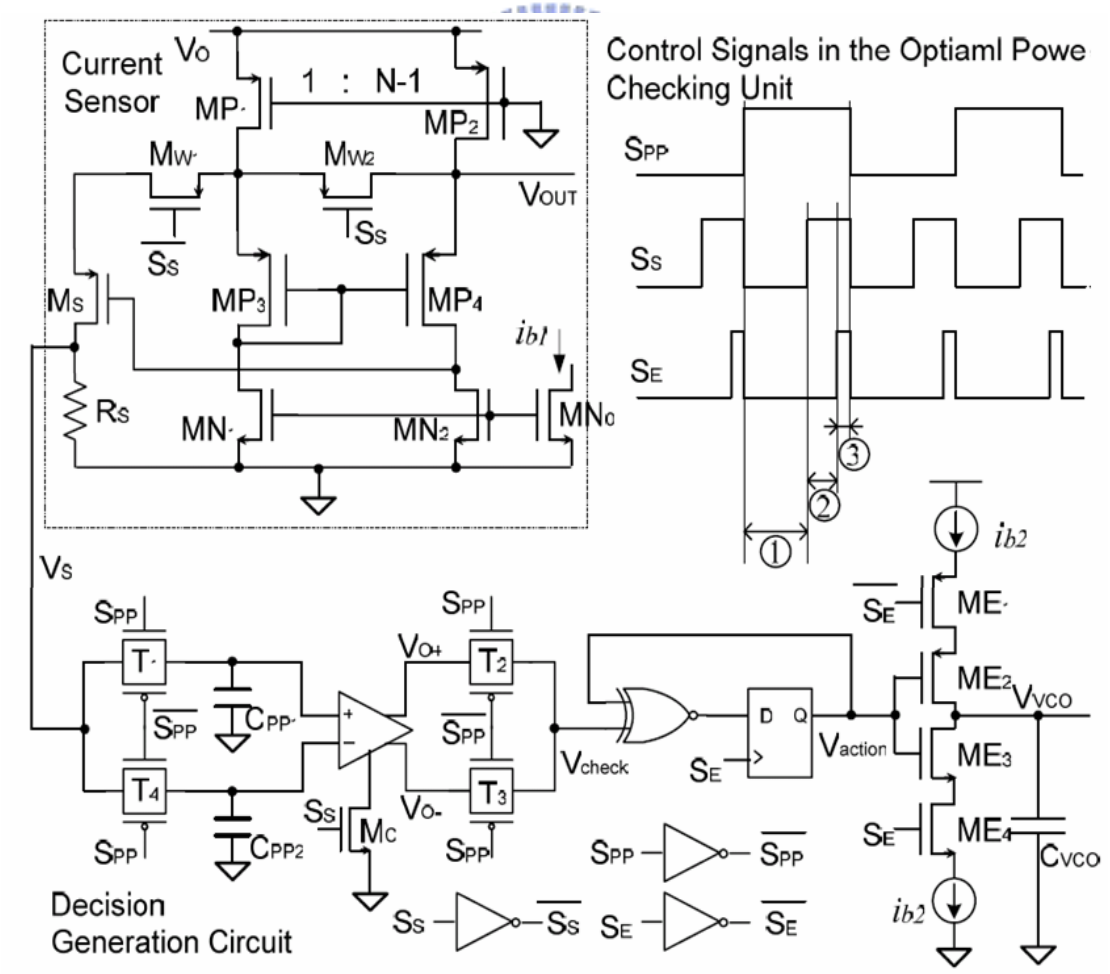


Fig. 2.9 Circuit of the optimal power tracking unit. **(①normal working phase, ②sensing phase, ③evaluation phase)**

The optimal power tracking unit monitors the charge pump output power and generates the adjustment decision for the switching frequency of the charge pump so that the system is working around the optimal output power point. The optimal power tracking unit contains two parts. Since the system output voltage is regulated by the battery and the voltage of the battery changes very slowly, thus, maximizing the system output power is equivalent to maximizing the system output current. The circuit uses current sensor to measure the charge pump output current. Based on the measured current value, the tracking unit checks whether the system is at the optimal point and generates the corresponding decision signal to tune the system parameters. Basically a generic hill climbing algorithm is used in the circuit for the optimal point tracking. The charge pump switching frequency affects the system output current. Hence the tracking unit generates the corresponding voltage value to vary the switching frequency through a VCO in the control unit. The tracking unit consists of a current sensor. With the biasing current through MN_1 and MN_2, the source voltages of MP_3 and MP_4 are clamped the same. When the current sensor power supply V_O is connected to the charge pump output, due to the size ratio of MP_1 and MP_2, about 1/N of the total output current flows to the resistor R_S though the transistor M_S. Hence the output current level from the charge pump is reflected by the voltage drop across RS (V_S), which is then sent to the decision generation circuit. The rest of the output current would flow to the battery or the computation circuit through MP_2 at node V_{OUT}. Since the output current from the charge pump is in pulse shape, a smoothing capacitor is connected to the node V_O to obtain a smooth current profile for the accurate measurement of the average value of the output current through the current sensor. The sensed current which is represented by the value of V_S, is sent to the decision generation circuit to implement the generic hill climbing algorithm. By comparing the current sensed current value with the previous one, the circuit can determine the direction of the change in output current and make the decision on whether to increase or decrease the switching frequency. This action continues and the output current will oscillate around the maximum current point finally. In the decision generation circuit, the current sensed V_S value and the previous value are stored in the sample capacitors, C_{PP1} and C_{PP2}, alternatively. If $_{CPP2}$ holds the previous value, the transmission gates T_3 and T_4 are off while T_1 and T_2 are on. The current sensed V_S will be stored in C_{PP1}, and V_{check} will output the comparison results from V_{O+} of the comparator. V_{check} is equal to logic '1' if the current sample value is larger than the previous one. In the next sample period, T_1 and T_2 will be turned off while T_3 and T_4 are on, and C_{PP1} holds the old sample while C_{PP2} stores the current V_S value. V_{check} will output the comparing results from V_{O-} for this sample period. This value is XNORed with the previous adjustment decision which is stored in a

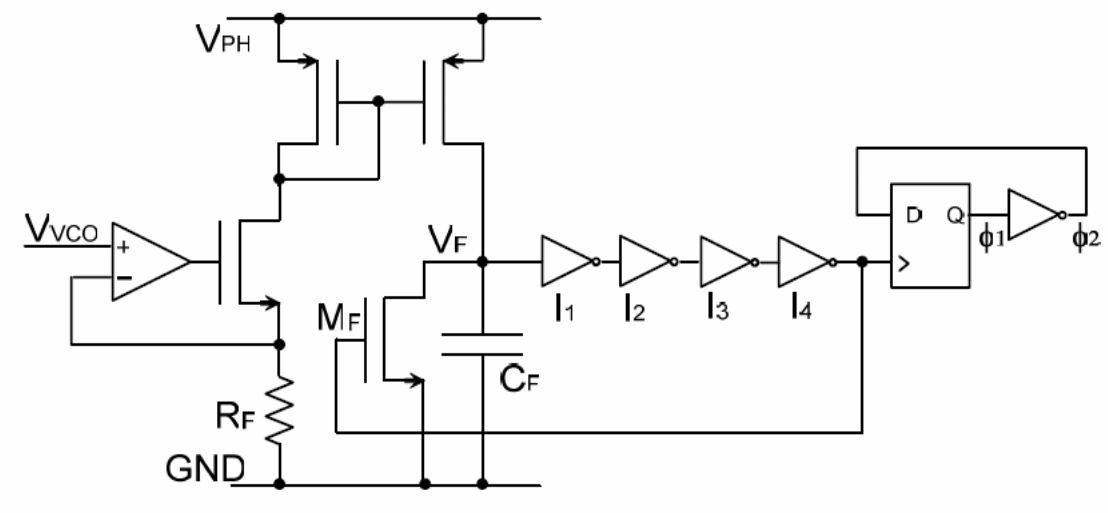


Fig. 2.10 Control unit for the charge pump.

D-flipflop and the new decision value V_{action} will be updated at the rising edge of the control pulse S_E. The logic value of the decision signal V_{action} indicates whether the charge pump switching frequency should be increased or decreased. Depending on the V_{action} logic value, the capacitor C_{VCO} is either charged by the current i_{b2} through transistor ME_1, or discharged by the current i_{b2} through transistor ME_4, during the control pulse interval of S_E. In this way, the voltage of V_{VCO} is either increased or decreased and it is then sent to the control unit to adjust the switching frequency through the VCO.

In order to reduce the power overhead, the optimal power tracking unit operation is divided into three phases during each sample period, which is shown in Fig. 2.9. Here, the sample period means the time interval between 2 consecutive frequency adjustments. During each period, the transmission gate control signal S_{PP} is either high or low, which determines whether the previous sampled VS or the current one is stored in C_{PP1} or C_{PP2}, and whether V_{O+} or V_{O-} of the comparator will output the checking results. After each frequency adjustment, the tracking unit is disabled so that all the charge pump output current can flow to V_{OUT}. This denotes as the normal working phase. At the end of the normal working phase, sensor control signal S_S will activate the optimal power tracking unit where the charge pump output current is sensed and the current changing is checked at node Vcheck. This denotes as the sensing phase. After some delay, the tracking unit enters the evaluation phase in which a pulse S_E is generated. Decision signal is updated in the D-flipflop and the capacitor C_{VCO} is charged or discharged during the S_E pulse interval according to the generated decision. After that, the power checking unit is disabled and the operation goes back to normal working phase again.

2.4.2 Control Unit

The control unit is used to adjust the system operating parameters based on the decision from the optimal power tracking unit in order to maximize the output power from the charge pump. The charge pump switching frequency has a profound impact on the system output power. A VCO is implemented in the control unit to generate a variable frequency clock. The circuit structure is shown in Fig. 2.10[3]. V_{VCO} is the output decision signal from the optimal power tracking unit which determines the switching frequency to be outputted through the inverter chain I_1~I_4. An edge-triggered D-flipflop re-adjusts the clock duty cycle and then sends the clock signal to the charge pump. To achieve good power transfer efficiency, the power consumption of the control unit should be minimized. Hence, the currents of the amplifier branches and the VCO branches have to be carefully controlled. Moreover, since V_F varies around the threshold of the inverter I_1, the short circuit current of I_1 is significant. In order to reduce the current loss, the I_1 is implemented in small size. True Single Phase Clocked (TSPC) register is implemented for the D-flipflop in order to reduce the number of transistors and also its power consumption.

2.5 A Battery Management System for Energy Harvesting Applications

A battery management system for energy harvesting applications is shown in Fig. 2.11[4].

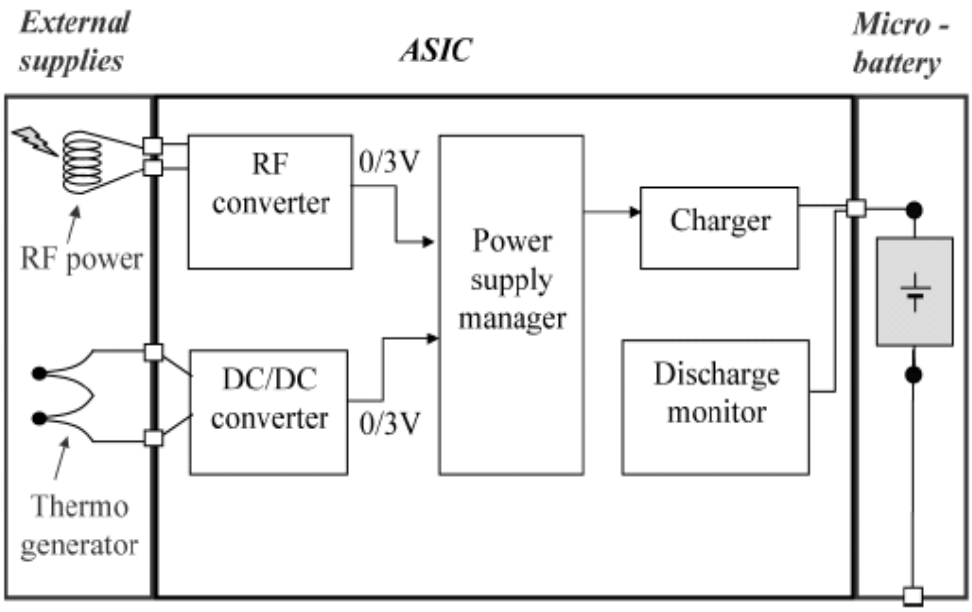


Fig. 2.11 The battery management system for energy harvesting applications.

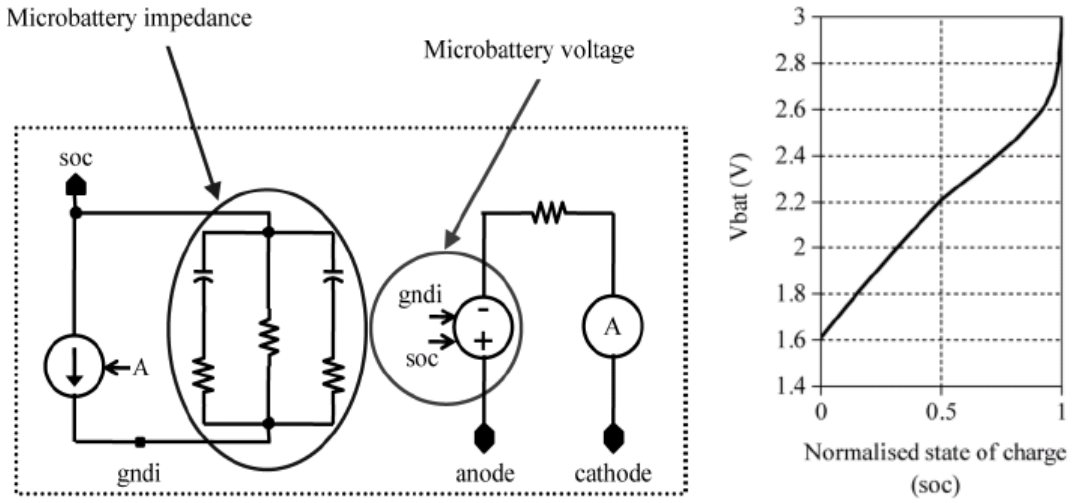
The microsystem architecture is comprised of two power sources, RF and thermoelectric, a microbattery used as storage unit and power supply manager to transform and manage the harvested energy and interface the microbattery. Both sources are managed by the ICs: the microbattery being charged either using thermal energy harvested by the thermogenerator associated with the DC/DC converter or using external RF power converted by the RF converter. The state of charge of the storage device is monitored periodically.

2.5.1 Thin-Film Solid-State Battery Electrical Model

The circuit model of microbattery is shown in Fig. 2.12(a) [4]. The voltage-dependent generator generating the microbattery voltage is based on a table. The model has two outputs reproducing the battery state of charge and the voltage across the battery. The microbattery voltage versus its state of charge is shown in Fig. 2.12(b) [4].

2.5.2 Microbattery State of Charge Monitor

In order to ensure permanent monitoring, the microbattery state-of-charge monitor is supplied by the microbattery itself. The state-of-charge monitor must also be resistant to supply voltage variations to be compatible with the microbattery. The state-of-charge monitor is shown in Fig. 2.13[4]. The monitor compares voltage of battery to a reference voltage and sets the digital soc flag to “low” level when the micro-battery is discharged.



(a) (b)

Fig. 2.12 (a) Microbattery electrical model. (b) Voltage versus normalized state of charge.

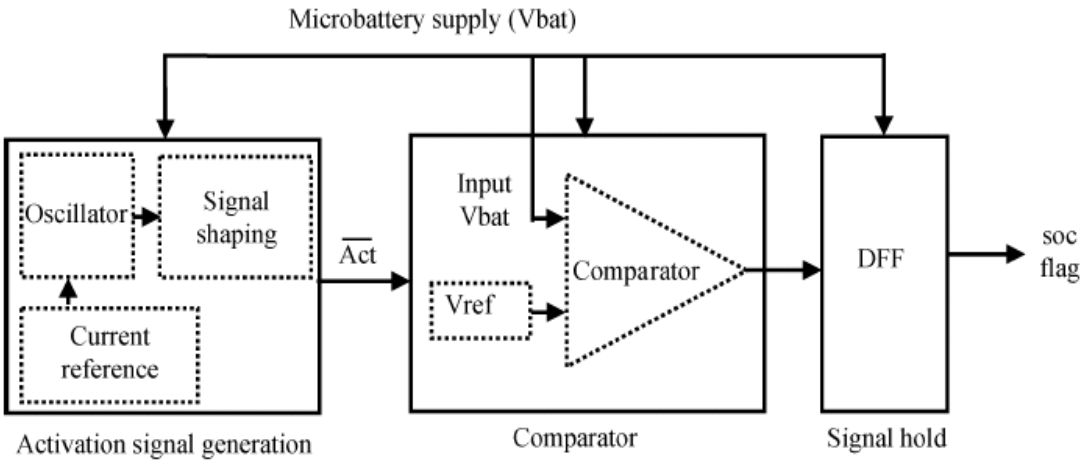


Fig. 2.13 Sate of charge monitor architecture.

To achieve ultra low power consumption, the comparator is periodically activated, only for one second every hour and a half. This sampling rate is sufficient since the microbattery lasts for about one year for the envisaged low duty-cycle applications. The comparator can be seen in Fig. 2.13[4], as well as the circuit which generates the comparator activation signal (composed of a current reference, an oscillator, and a signal shaping block including a Schmitt trigger, a frequency 2^{12} divider and sequencing logic), and a last circuit which just holds the comparator output value when the comparator is disabled.

2.5.3 Power Supply Manager and Battery Charger

The microbattery can be charged by the thermogenerator's DC/DC output or by the RF converter. Therefore, the power supply manager, comprising a specific unit along with an asynchronous finite state machine, manages priority between the two sources when they are simultaneously present and activates self-powered microbattery protection in the case of external power source interruption. The microbattery charge control circuit architecture is shown in Fig. 2.14[4]. The power supply manager generates an internal power supply Vdd from the two external sources. This Vdd supply is used by the microbattery charge controller to provide a constant current for a 20 mn microbattery charge. The power supply manager also creates an internal power supply Vmax defined instantaneously by the maximum voltage between Vdd and Vbat, the battery voltage. Consequently, this power supply Vmax is permanent while using as little power as possible from the battery: it is used to activate microbattery protection against untimely discharge in case of external power source interruption.

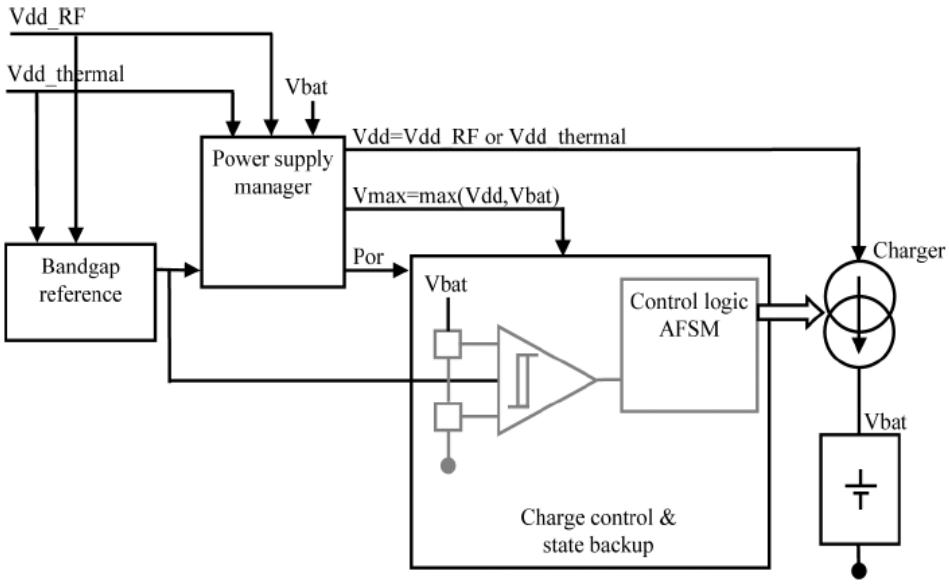


Fig. 2.14 The architecture of microbattery charge control circuit.

2.5.4 A Battery Management System to Increase the Service Life of Battery

From above introduction, we know that more and more power management systems for energy harvesting system are cooperated with a rechargeable battery to ensure that the system can work without the power source from natural energy. The problem is that the natural power source is not an ideal source for charging batteries. Without control mechanism, the batteries are regularly deep discharged and it is not possible to ensure an optimum charge/ discharge cycle. The poor charge/ discharge cycle may result in sulfation, stratification, or gassing resulting in an end of battery life. A battery management system is used to prevent the battery from repeatedly overcharged or undercharged. The battery management system is shown in Fig. 2.15[5].

The battery charging method is a very important factor in prolonging the life of the battery in an energy harvesting system. A charge control mechanism is shown in Fig. 2.16[5]. The charge controller has different set points. The set points prevent the battery from being overcharged or over-discharged.

1) VR: The voltage regulation set point limit the maximum voltage that the battery can reach (disconnects the battery from the array).
2) ARV: The array reconnect voltage set point gives the voltage at which the battery and array are reconnected.
3) LVD: The low voltage disconnect set point gives the point at which the battery will be disconnected from the load to prevent over-discharged.
4) LRV: The load reconnect voltage set point gives the voltage at which the load can be reconnected to the battery

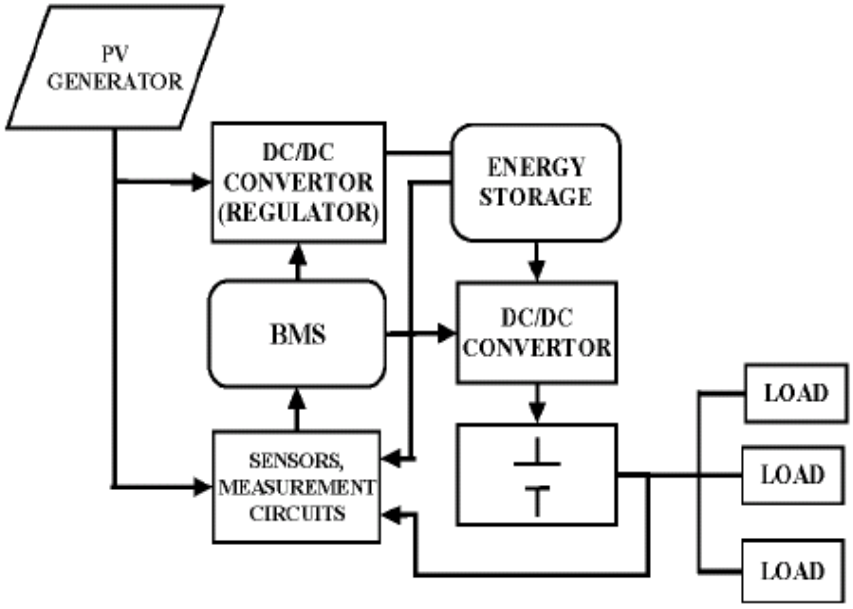


Fig. 2.15 Battery management system with charge controller.

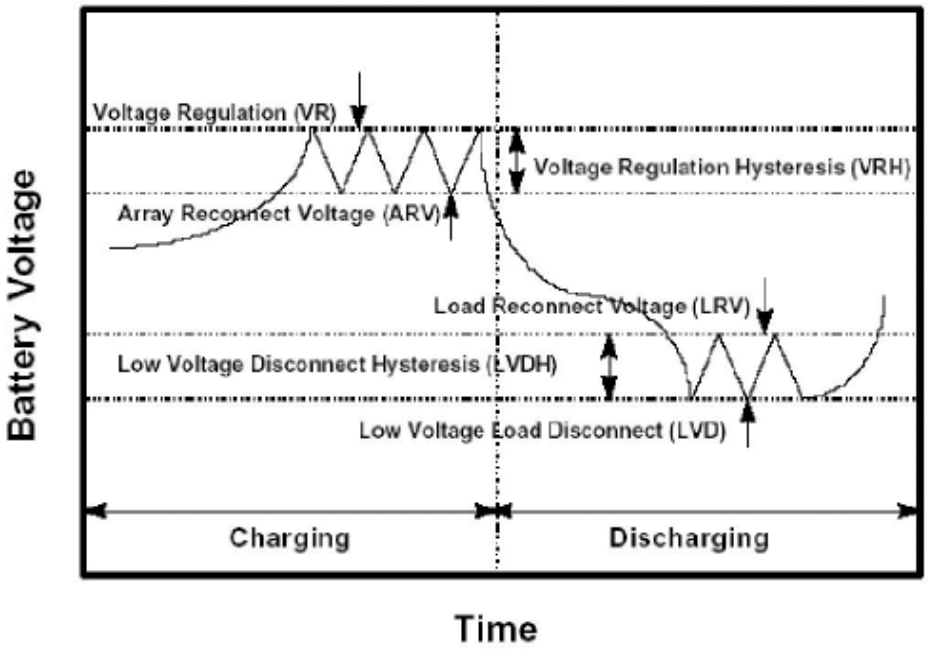


Fig. 2.16 Charge controller set points.

2.6 Summary

In this chapter, the characteristic of PV cell is introduced and its circuit mode is implemented. A maximum power point tracking technique was used for PV cell. The MPPT controller sensed the output voltage and current of PV cell and adjusted the reference voltage of dc/dc converter to keep the PV cell operating in maximum power point.

For ultra-low voltage energy harvesting application, a power management system with small battery to jump start was implemented. The power management system also contained a low power clock generator for a four stage 16x exponential charge pump circuit. Whit the unpredictable power source, the power management used a charge-base control unit to prevent the computation error.

A charge pump is usually used in solar energy harvesting applications. For efficiently using the energy, a micro power management system with maximum output power control was implemented. The system contained an optimal power tracking unit to monitor the output power of charge pump and generated the adjustment decision for the switching frequency of the charge pump so that the system was working around the optimal output power point. Finally, a micro battery model is introduced. Two battery management systems were designed to co-operate with the battery.

Chapter 3
Voltage Regulators

A voltage regulator is composed of an op amp, reference voltage generator and an output MOSFET. The ideal voltage regulator is low dropout voltage, low quiescent current, good loading capability and small output transient undershoots and overshoots.

To archive high output current and low dropout voltage, the output MOSFET must be very large. But the larger MOSFET will increase the intrinsic capacitor of its gate node. This will cause stability problem. To archive high-precision output voltage regulator, a high loop gain is required. But the stability is sacrificed when loop gain is too high. Good transient response is related to slew rate at the gate drive of the power transistor and the loop-gain bandwidth. This can be improved by a high slew-rate buffer and advanced frequency compensation technique.

In this Chapter, the techniques of improving stability of voltage regulator are introduced in Section 3.1. The techniques of improving transient response of voltage regulator are introduced in Section 3.2. A linear regulator using digital buffer is introduced in Section 3.3. The reference voltage circuit is described in Section 3.4. Finally, we proposed two voltage regulators with high current efficiency and fast load regulation in Section 3.5. All results are simulated in UMC 90nm CMOS technology model.

3.1 Stability Scheme of Voltage Regulator

3.1.1 The Dynamic-Biased Shunt Feedback Buffer

A typical structure of a low-dropout regulator is shown in Fig. 3.1[10], which consists of an error amplifier comparing a scaled-down output signal to a bandgap voltage V_{bg}, a PMOS pass transistor M_p, and an intermediate buffer stage driving M_p. There are three poles in the LDO structure located at the output of the error amplifier (N1), the output of the buffer (N2), and the output of the LDO (V_{out}). In particular, these poles are given by

$$\begin{aligned} p_1 \mid N_1 &= 1/(r_{o1}C_1) \\ p_2 \mid N_2 &= 1/(r_{ob}C_p) \\ p_o \mid N_{out} &= 1/(R_{oeq}C_L) \end{aligned} \tag{3.1}$$

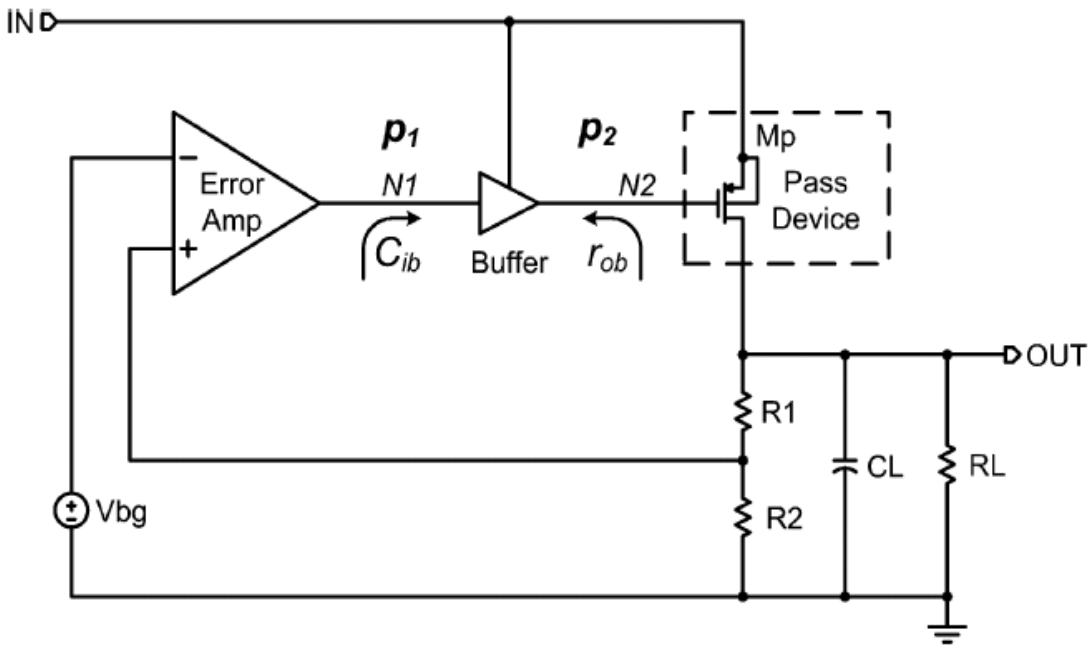


Fig. 3.1 Typical structure of a low-dropout regulator with an intermediate buffer stage.

The r_{o1} is the output resistance of the error amplifier, C_1 is the equivalent capacitance at N_1 which is dominated by the input capacitance of the buffer C_{ib}, r_{ob}, is the output resistance of the buffer, C_p is the input capacitance of M_p, and R_{oeq} is the equivalent resistance seen at the output of the LDO. Ideally, both C_{ib} and r_{ob} should be very small in order to achieve single-pole loop response by locating both p_1 and p_2 at frequencies much higher than the unity-gain frequency of the regulation loop.

In order to construct the required intermediate buffer stage, a simple PMOS source-follower is first considered to implement the buffer and its structure is shown in Fig. 3.2[10]. The PMOS source-follower can provide near complete shutdown of the pass device under light-load conditions. Since the output resistance r_{ob} of the source-follower is given by $1/g_{m21}$, it is necessary to increase g_{m21} in order to decrease the value of r_{ob} and allow p_2 to be located at frequencies much higher than the unity-gain frequency of the LDO regulation loop. Transconductance g_{m21} can only be increased either through using a larger W/L ratio of transistor M_{21}, or through increasing the DC biasing current I_{21} through M_{21}, or both. Increasing I_{21} would, however, increase the total quiescent current of the LDO, thereby degrading the current efficiency of the LDO. Using a larger W/L ratio of M_{21} would increase the input capacitance C_{ib} of the buffer, which in turn pushes p_1 to a lower frequency and the stability can be poorly affected. A simple PMOS source-follower is, therefore, not a suitable implementation of the intermediate buffer stage in the LDO.

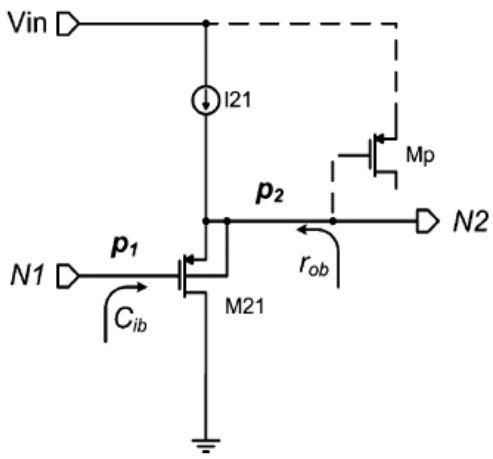


Fig. 3.2 Source-follower implementation of the intermediate buffer stage.

In order to minimize W/L ratio of M_{21} and the quiescent current required to reach a given r_{ob}, the source-follower with negative feedback shown in Fig. 3.3(a)[10] is used. In particular, the npn transistor Q_{20} is the feedback device connected in parallel to the output of the source-follower M_{21} in order to reduce r_{ob} through shunt feedback. From a qualitative standpoint, when the input voltage at N_1 is constant and the output voltage increases, the magnitude of the drain current of M_{21} also increases, which in turn increases the base current of Q_{20}. As a result, the collector current of Q_{20} increases, reducing the output resistance r_{ob} by increasing the total current that flows into the output node. The output resistance looking into the follower is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta)} \tag{3.2}$$

Equation 3.2 shows that the output resistance of the follower is reduced by the current gain β of the shunt feedback device Q_{20}. For example, when an npn transistor with $\beta = 10$ is used, the value of r_{ob} would be decreased by about 10 times and the frequency of p_2 at the gate of the pass device is then pushed to a decade higher. As a result, the quiescent current needed through M_{21} is greatly reduced to realize g_{m21} for a given r_{ob}. Similarly, the transistor size of source-follower M_{21} required is also reduced. The input capacitance of the buffer C_{ib} is then decreased, which allows p_1 given in (3.1) to be located at a higher frequency without dissipating additional quiescent current. It should be noted that the shunt feedback device Q_{20} can also be implemented by a NMOS transistor in single-well technologies to achieve a similar reduction in the output resistance.

Since the unity-gain frequency of the LDO regulation loop increases with the load current, the output resistance of the buffer should decrease when the load current increases in order to maintain p_2 far beyond the unity-gain frequency under the entire load current range. The buffer with dynamically-biased feedback

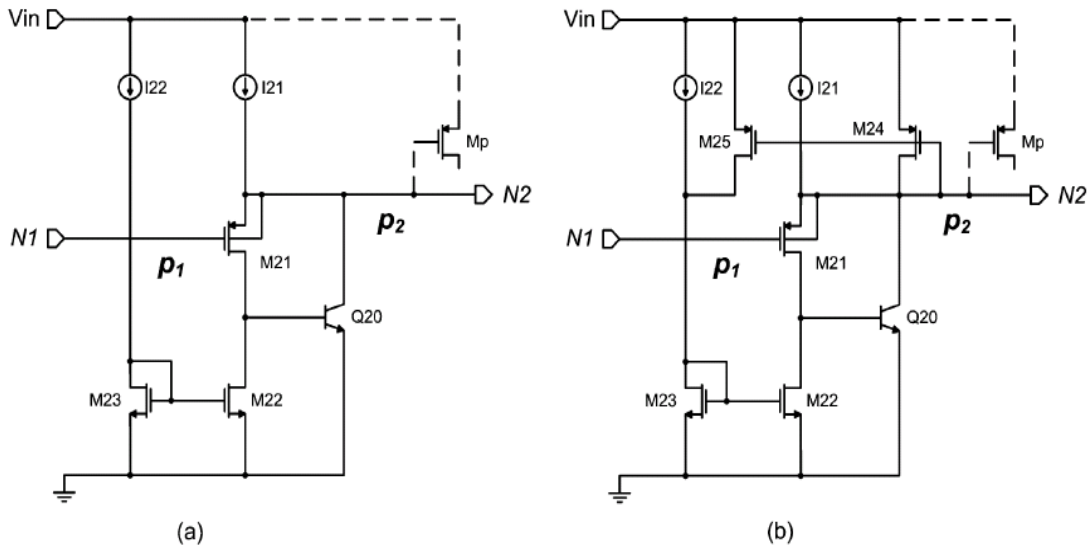


Fig. 3.3 (a) Source-follower with shunt feedback. (b) The buffer with dynamically-biased shunt feedback for output resistance reduction under different load currents.

is shown in Fig. 3.3(b)[10]. Two PMOS transistors M_{24} and M_{25} and the npn transistor Q_{20} realize dynamically-biased shunt feedback to decrease r_{ob} under different load current conditions. The output resistance of the buffer is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta) + g_{m24}} \tag{3.3}$$

The g_{m24} is the transconductance of the diode-connected transistor M_{24}. As shown in Fig. 3.3(b), when the load current flowing through the pass device M_p increases, both voltages at N_1 and N_2 decrease. The gate-source voltage of M_{24} is increased and hence more current flows through M_{24}. This current then mirrors through M_{25} such that the current through the follower device M_{21} dynamically increases with the load current. This boosts the value of g_{m21}, thereby further reducing the output resistance of the buffer according to (3.3). In addition, the increase in g_{m24} with the load current can reduce the value of r_{ob}. This effect is significant under heavy load current conditions. Moreover, when the load current increases, part of the dynamically-increased current through M_{21} flows into the base of Q_{20} and increases its collector current. The current gain β of the vertical parasitic npn transistor slightly increases with the collector current, which also helps on reducing the value of r_{ob} when the load current increases.

The dynamically-biased shunt feedback technique reduces both the input and output impedance of the buffer by decreasing the values of C_{ib} and r_{obs}. In particular, the reduction in the value of r_{ob} increases with the load current. As a result, p_2 is located at sufficiently high frequencies under different load currents, while the LDO

only dissipates low quiescent current at no-load condition. The benefit of having a smaller C_1 by using a smaller size of source-follower device in the buffer also improves the stability of the LDO.

3.1.2 Zero-Pole Cancellation

A classical CMOS LDO is shown in Fig. 3.4[11]. This LDO is composed of an error amplifier, a voltage buffer, a power PMOS transistor operating in saturation region, a feedback-resistor network and a voltage reference.

The three poles of this LDO are generated at the output of LDO, the voltage buffer and the error amplifier, as mentioned in Section 3.1.1. The stability of classical LDO based on dominant-pole compensation with pole-zero cancellation as shown in Fig. 3.5[11]. The second pole p_2 is cancelled by the zero z_1 created by the ESR of the output capacitor. With a large output capacitance, the LDO stability is achieved by locating p_3 beyond the unity-gain frequency of the loop gain to provide sufficient phase margin. However, when loop gain is too high, p_3 locates before the unity-gain frequency, and an even larger output capacitance is required to retain LDO stability.

Moreover, the power PMOS transistor in the classical LDO must operate in saturation region due to the stability problem at different input voltages. The change in voltage gain due to different drain–source voltage is not substantial when the transistor operates in saturation region [12]–[13]. However, if the transistor operates in linear region at dropout, the transistor will operate in saturation region instead as the input voltage increases. As mentioned previously, when the loop gain increases, the classical LDO based on dominant-pole compensation may be unstable. Therefore, the power PMOS transistor needs to operate in saturation region throughout the entire range of input voltage, so a large transistor size is required to provide a small saturation voltage at the maximum output current.

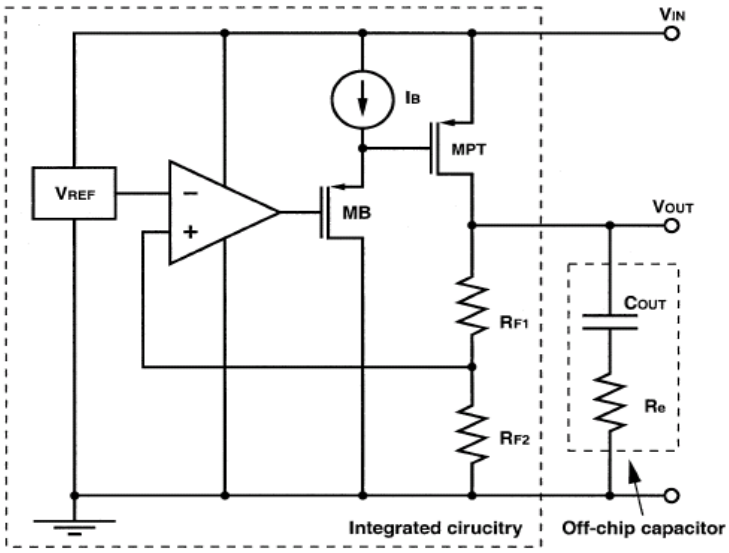


Fig. 3.4 Structure of classical LDO.

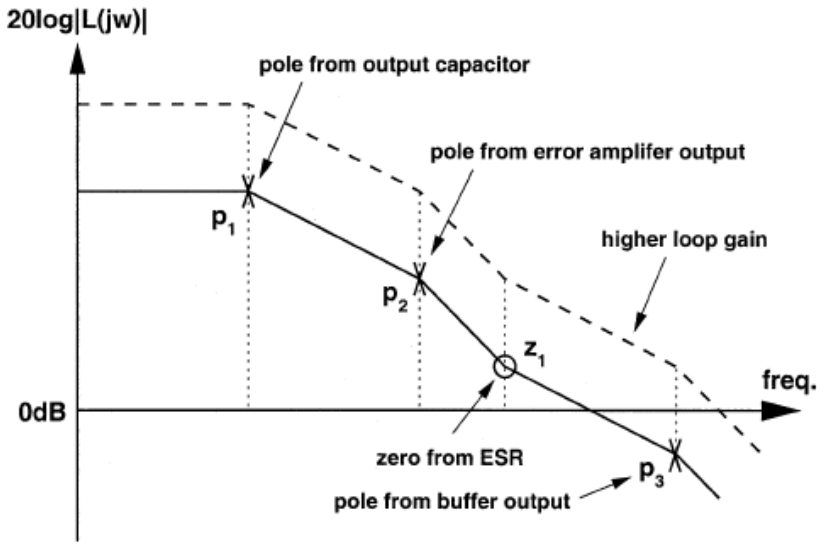


Fig. 3.5 Loop gain of classical LDO.

3.1.3 Damping Factor Control Compensation

From the previous discussion, the classical LDO suffers from a stability problem. This problem is due to the low-frequency poles, and hence, large off-chip capacitance and ESR are needed for closed-loop stability. In fact, this problem can be solved by pole splitting. However, classical two-stage-amplifier topology is not optimum since the power transistor cannot function as a high-gain stage in dropout condition. The pole-splitting effect is thus not effective and the output precision is also degraded. Instead, an LDO can be viewed as a three-stage amplifier with the power transistor as the last stage. When using this approach, the positions of the nondominant poles depend on the transconductance of the power transistor and the output capacitance. The larger transconductance and smaller output capacitance results in higher frequencies of the nondominant poles. Therefore, the worst case stability occurs at zero load-current condition as the transconductance is minimum (about 5–10 mA/V) when only a current equaled to $V_{OUT}/(R_{F1}+R_{F2}) \approx 1-5uA$ drains from the power transistor. Advanced frequency compensation techniques are required to generate a more effective pole-splitting effect incorporated with pole-zero cancellation. The pushed nondominant poles can be cancelled more effectively by extra zeros at higher frequencies. The required passive components to generate the zeros can be much smaller, and the coupling noise is, hence, reduced significantly. A stable and fast-response LDO with DFC frequency compensation is shown in Fig. 3.6[11].

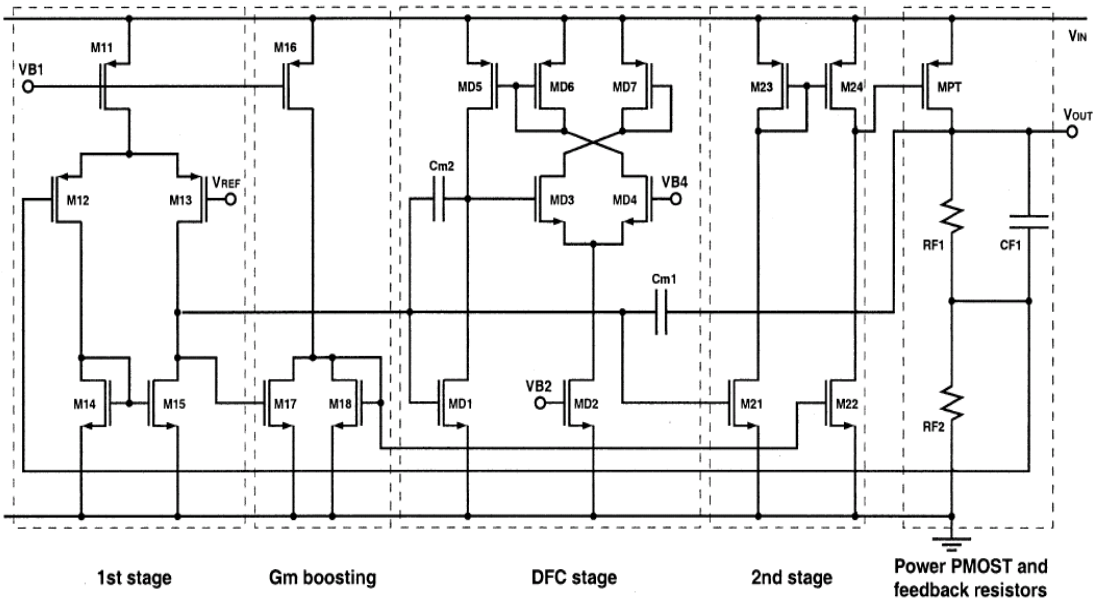


Fig. 3.6 The schematic of LDO with DFC frequency compensation.

The DFC stage is composed of a negative gain stage with a compensation capacitor C_{m2}, and the DFC stage is connected at the output of first stage. Another compensation capacitor Cm1 is required to achieve pole-splitting effect. The feedback-resistive network creates a medium frequency zero for improving the LDO stability and its schematic is shown in Fig. 3.7[11]. The transfer function of feedback-resistive network is given by

$$\frac{v_x(s)}{v_s(s)} = \left(\frac{R_{F2}}{R_{F1} + R_{F2}} \right) \left[\frac{1 + sC_{F1}R_{F1}}{1 + sC_{F1}\left(R_{F1} // R_{F2}\right)} \right] \tag{3.4}$$

From the above analysis, it is shown that one pole (p_f) and one zero (z_f) are created, and p_f and z_f are, respectively, given by

$$p_f = \frac{1}{C_{F1}\left(R_{F1} // R_{F2}\right)}$$
$$z_f = \frac{1}{C_{F1}R_{F1}} \tag{3.5}$$

The zero frequency is lower than the pole frequency and can be used to cancel the effect of non-dominant pole created in the regulator. In order to have $z_f << p_f$, R_{F2} should be much smaller than R_{F1}.

Due to the effective pole-splitting effect by DFC compensation, the non-dominant pole frequencies are high, and so the required C_{F1} is small and is about 5pF. In addition, the transient response will not be slowed by C_{F1} because it is small and is connected at the regulator output.

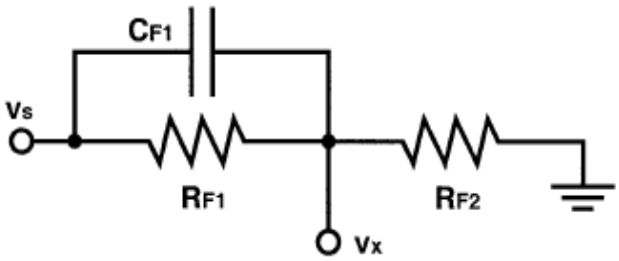


Fig. 3.7 Feedback-resistive network with first-order high-pass characteristic.

To enhance the DFC scheme to provide a wider loop-gain bandwidth, the gm boosting circuitry is used. The gm boosting circuitry is shown in Fig. 3.8[11]. The function of M17 and M18 is to create a signal $-v_1$ from the input signal v_1, and these two signals v_1 and $-v_1$ are applied to M21 and M22, respectively. With *k*-times current mirror, the effective transconductance is increased by 2*k* times.

Following discussion is the stability of LDO with and without off-chip capacitor.

1) Stability with off-chip capacitor:

The stability of the proposed LDO is considered for two cases: $I_{OUT}=0$ and $I_{OUT}\neq 0$. When $I_{OUT}=0$, the transconductance g_{mp} and the output resistance r_{op} of the power PMOS is at the minimum and maximum, respectively. This is the worst case stability of the proposed compensation scheme. In this case, the DFC scheme provides a transfer function given by

$$L_{o(cap)}(s)|_{I_{OUT}=0}=\frac{L_o\left(1+\frac{s}{z_e}\right)\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left[1+s\left(C_{OUT}R_e+\frac{C_gC_{OUT}g_{m4}}{C_{m1}g_{m2}g_{mp}}\right)+s^2\frac{C_gC_{OUT}}{g_{m2}g_{mp}}\right]\left(1+\frac{s}{p_f}\right)} \quad (3.6)$$

Where C_g is the gate capacitance of the power PMOS and g_{m4} is the transconductance of the DFC stage.

$$L_o=((R_{F2})/(R_{F1}+R_{F2}))g_{m1}R_{o1}g_{m2}R_{o2}g_{mp}r_{op}$$

$$p_1=1/C_{m1}R_{o1}g_{m2}R_{o2}g_{mp}r_{op}$$

$$z_e=1/C_{OUT}R_e$$

L_o, p_1 and z_e are the low-frequency loop gain of the DFC scheme, the dominant pole and ESR zero respectively, and g_{m1}, g_{m2}, R_{o1}, R_{o2} and R_e are the transconductance of the error amplifier, the transconductance of the second gain stage, the output resistance of the error amplifier, the output resistance of the second gain stage, and the

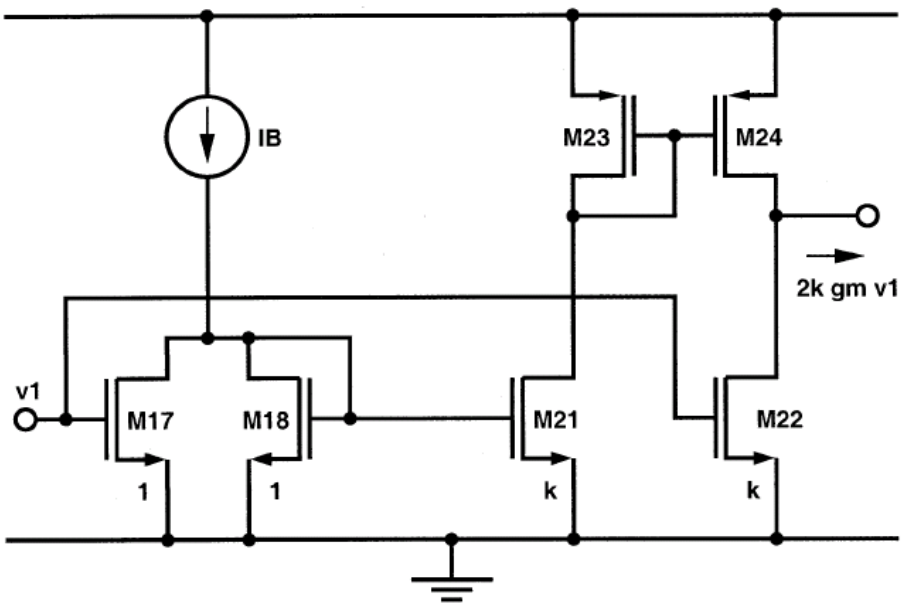


Fig. 3.8 Transconductance-boosting circuitry.

ESR of the output capacitance, respectively.

When $I_{OUT}=0$, the current drain from the power transistor is $V_{OUT}/(R_{F1}+R_{F2})$, which is less than 1–5 uA for low-power LDO designs. Therefore, g_{mp} is very small, and this causes the effect of $C_{OUT}R_e$ in the s term at the denominator of (3.6) to be negligible. As a result, (3.6) is approximated to

$$L_{o(cap)}(s)|_{I_{OUT}=0} \approx \frac{L_o\left(1+\frac{s}{z_e}\right)\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+s\frac{C_g C_{OUT} g_{m4}}{C_{m1} g_{m2} g_{mp}}+s^2\frac{C_g C_{OUT}}{g_{m2} g_{mp}}\right)\left(1+\frac{s}{p_f}\right)} \tag{3.7}$$

Comparing the second-order function in (3.7) with a standard second-order function given by

$$F(s)=1+s\left(\frac{2\varsigma}{p_c}\right)+\left(\frac{s}{p_c}\right)^2$$

where ς is the damping factor and p_c is the pole frequency of the complex poles. The value of p_c is given by

$$p_c = \sqrt{\frac{g_{m2} g_{mp}}{C_g C_{OUT}}} \tag{3.8}$$

The damping factor is given by

$$\varsigma = \frac{1}{2}\sqrt{\frac{C_g C_{OUT}}{g_{m2} g_{mp}}}\cdot\left(\frac{g_{m4}}{C_{m1}}\right)$$

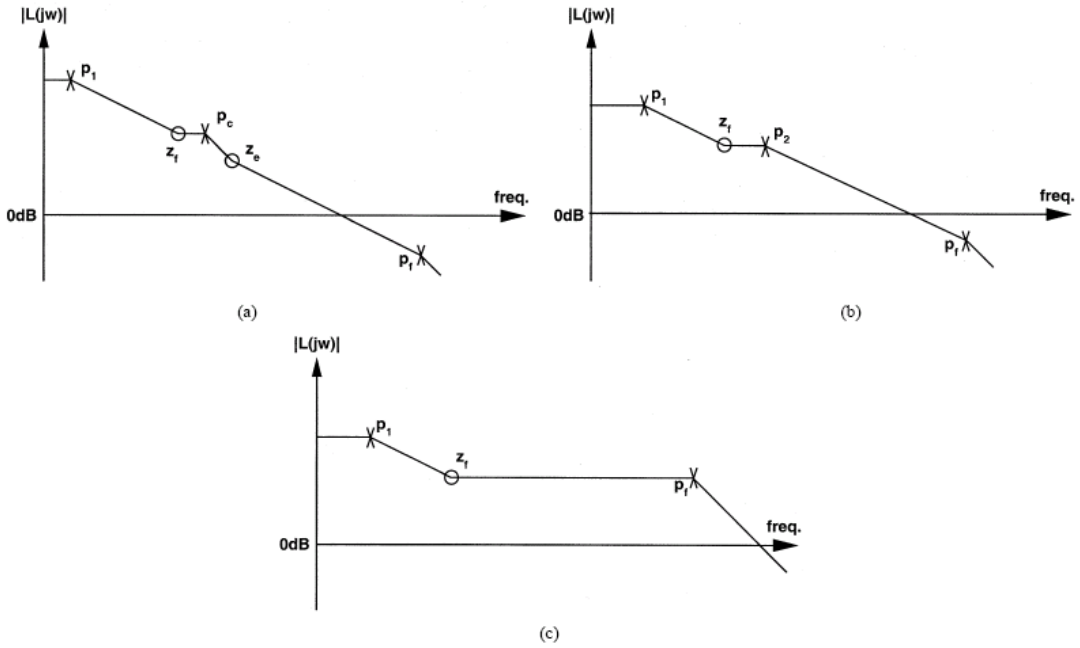


Fig. 3.9 Loop gain of the LDO with DFC scheme. (a) $C_{OUT} \neq 0$ and $I_{OUT} = 0$. (b) $C_{OUT} \neq 0$ and $I_{OUT} \neq 0$. (c) $C_{OUT} = 0$ and $I_{OUT} \neq 0$.

The damping factor is critical to the LDO stability. If the damping factor is too small, a frequency peak occurs and pole-zero cancellation by separated zeros is not effective. If the damping factor is too large, the complex poles become two separated real poles and the loop-gain bandwidth will be degraded. Therefore, the damping factor is set to $1/\sqrt{2}$ as a compromise under the conditions that

$$C_{m1} = g_{m1}\sqrt{\frac{8C_g C_{OUT}}{g_{m2} g_{mp}}}$$

$$g_{m4} = 4g_{m1}$$

It is noted that C_{m2}=C_{m1} is set for proper operation of the DFC scheme.

As shown in Fig. 3.9(a), the effect of the complex poles can be cancelled by z_e and z_f. Since the complex poles are split to a high frequency by the DFC scheme, z_e and z_f are at high frequencies. This implies that a low ESR, which is the key to a better load transient response and PSRR, is required. Moreover, p_f is designed to be higher than the unity-gain frequency of the loop gain for a good phase margin.

When there is a little increase of load current, as shown in (3.8), the complex poles will shift to a little higher frequency due to the increase of g_{mp}. The LDO is still stable since the pole-zero cancellation is still effective for pole-zero separation of less than a half of a decade.

When the load current increases significantly, g_{mp} also increases significantly and

the second-order function at the denominator of (3.6) is altered. The transfer function in the case of $I_{OUT} \neq 0$ is given by

$$L_{o(cap)}(s)|_{I_{OUT}\neq 0} = \frac{L_o\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+s\frac{C_g}{g_{m2}g_{mp}R_e}\right)\left(1+\frac{s}{p_f}\right)}$$

In this case, the ESR zero has no effect since an ESR pole is created simultaneously. The LDO is reduced to a one-zero three-pole system, where the new pole $p_2 = (g_{m2}g_{mp}R_e)/(C_g)$ is created. As shown in Fig. 3.9(b), z_f can be used to cancel p_2 to make the system stable.

2) Stability without off-chip capacitor:

When the proposed LDO is used in system-on-chip designs without an off-chip capacitor, the LDO is also stable. There is a minimum load current such that the LDO is still stable. The output capacitance comes from the power line, and the required minimum load current is larger for a larger load capacitance. Under such circumstance without the off-chip capacitor, ESR does not exist. Moreover, the second and third poles are pushed to frequencies that are higher than the unity-gain frequency of loop gain due to a large g_{mp}. The transfer function is given by

$$L_{o(capfree)}(s) \approx \frac{L_o\left(1+\frac{s}{z_f}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_f}\right)}$$

As shown in Fig. 3.9(c), pole-zero cancellation is automatically achieved by z_f and p_f, and thus, the theoretical phase margin is 90^o. However, parasitic poles and zeros will degrade the phase margin.

3.2 Transient Response Scheme of Voltage Regulator

3.2.1 Replica Feedback Circuit

The replica feedback circuit is shown in Fig. 3.10[14]. This regulator is composed of Bandgap reference, voltage comparator, charge pump, replica feedback circuit and output NMOS. The NMOS has inherently low output impedance for all frequencies. It also ensures a good PSRR because the NMOS behave like a cascade

device for the internal supply. The charge pump decreases the dropout voltage of regulator. The large capacitor C1 is necessary to reduce the capacitive coupling from the output to the gate voltage V_G at higher frequencies through the gate-source capacitance of output transistor M1.

Instead of sensing the output voltage directly, a replica branch is used for feedback which guarantees stability independent of the load. This is an advantage since the exact load is not known. The influence of process variations and temperature at dc settings is cancelled due to the matched structure of the replica. The replica ensures that the output is controlled toward the correct nominal dc setting, and implies that the loop is not influenced by load current variations. The influence of replica feedback circuit is illustrated in Fig. 3.11[14].

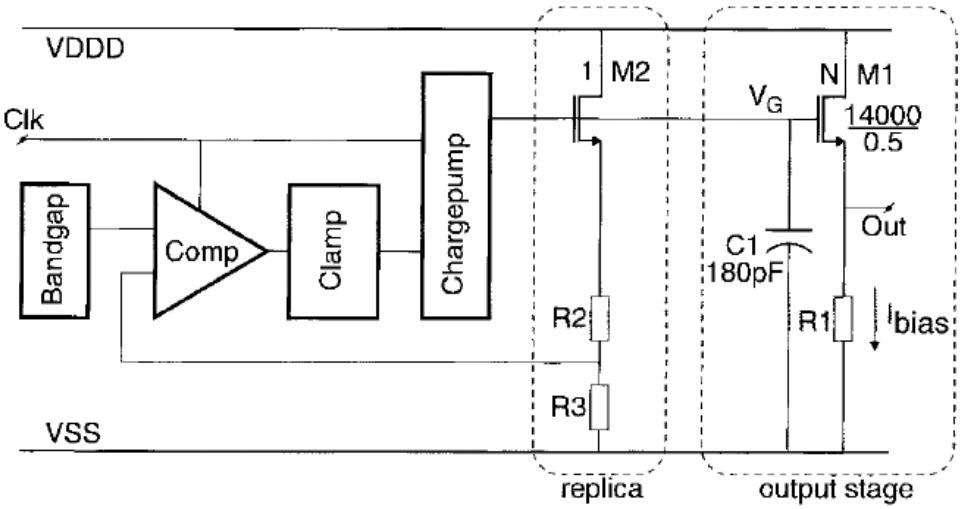


Fig. 3.10 The voltage regulator with replica feedback circuit.

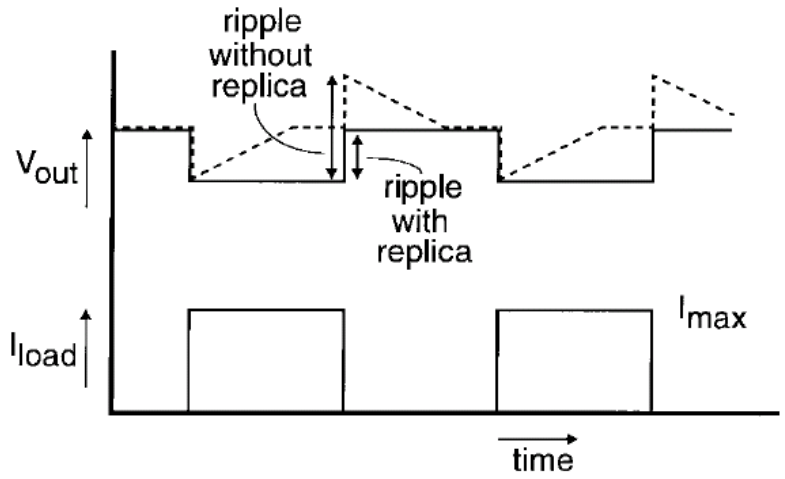


Fig. 3.11 Influence of replica feedback. With replica, the ripple in Vout is reduced by a factor 2.

3.2.2 Voltage Positioning

Optimum droop response is achieved for a constant, resistive output impedance of the regulator across the full frequency range of the load current, including dc. This concept, also called voltage positioning, is illustrated in Fig. 3.12[15].
Voltage positioning is easily implemented in replica-biased designs by adjusting the gain of the load regulation loop so that the dc and ac droops are equal. The regulator is shown in Fig. 3.13[15].

This regulator is composed of op amp A_0, pre-driver N-stage NS, replica circuit PS_{0R}, output stage PS_0~PS_{19}, resistor ESR and capacitor C_{DIE}. The P-stage circuit is illustrated in Fig. 3.14[15] and N-stage is a dual circuit of P-stage. By cascading the N-stage and P-stage, the line regulation at high frequency will be improved because the supply noise coupled by the N-stage cancels out with the noise coupled by the P-stage.

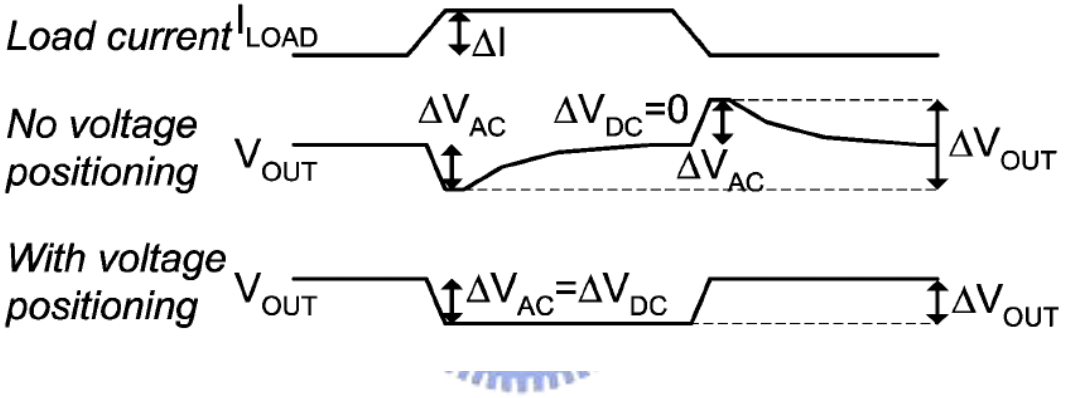


Fig. 3.12 Optimum transient response with voltage positioning.

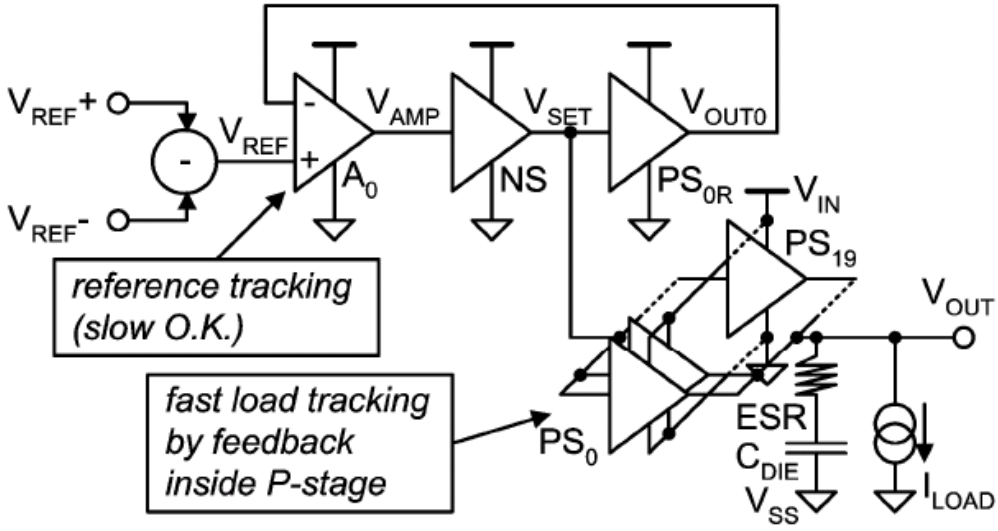
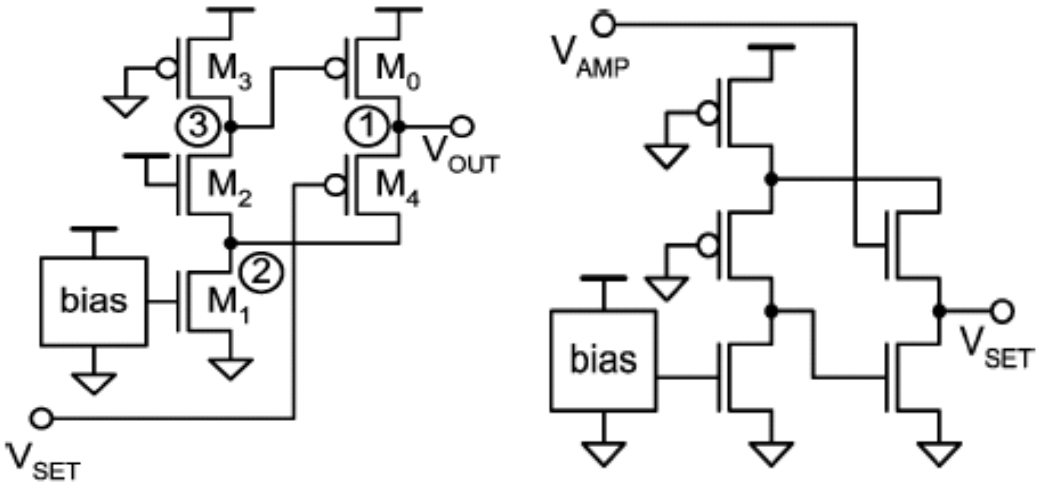


Fig. 3.13 The regulator with voltage positioning and ultra-fast load regulation.



(a) (b)

Fig. 3.14 (a) The schematics of P-stage and (b) N-stage.

The poles and zeros of this regulator is given by

$$S_{P0} = \frac{g_{D3}\left(g_{D4}+g_{D2}+g_{M2}\right)+g_{D2}g_{D4}}{C_{GS0}\left(g_{D4}+g_{D2}+g_{M2}\right)} \qquad S_{P1} = \frac{1}{ESR*C_{DIE}}$$

$$S_{Z0,1} = \frac{R+ESR}{2L}\left(1\pm 2\sqrt{1-\frac{L}{\left(R+ESR\right)C_{DIE}}}\right)$$

$$R = \frac{g_{D3}\left(g_{D4}+g_{D2}+g_{M2}\right)+g_{D2}g_{D4}}{g_{M0}g_{M4}\left(g_{D2}+g_{M2}\right)} \qquad L = \frac{C_{GS0}\left(g_{D4}+g_{D2}+g_{M2}\right)}{g_{M0}g_{M4}\left(g_{D2}+g_{M2}\right)}$$

Ideal response with voltage positioning is achieved when the zeros S_{Z0} and S_{Z1} cancel out the poles S_{P0} and S_{P1}, which happens for ESR=R, and $C_{DIE}=L/R^2= S_{P0}/R$.

3.3 Voltage Regulator with Digital Buffer

The conventional linear regulator shown in Fig. 3.15[16] has several limitations. First, same feedback loop is used for tracking of V_{REF} as well as for responding to varying load demand. This problem can be alleviated by using replica biasing with a fast local feedback loop for load regulation. Second, the response time depends on the slew rate of the analog buffer that drives the large output device. The slew rate of a class A buffer is directly proportional to the quiescent current which limited the speed of the fast regulator with single stage load regulation. A class AB buffer is more power-efficient but tends to degrade the phase margin of the feedback loop, which leads to more aggressive compensation and lower bandwidth.

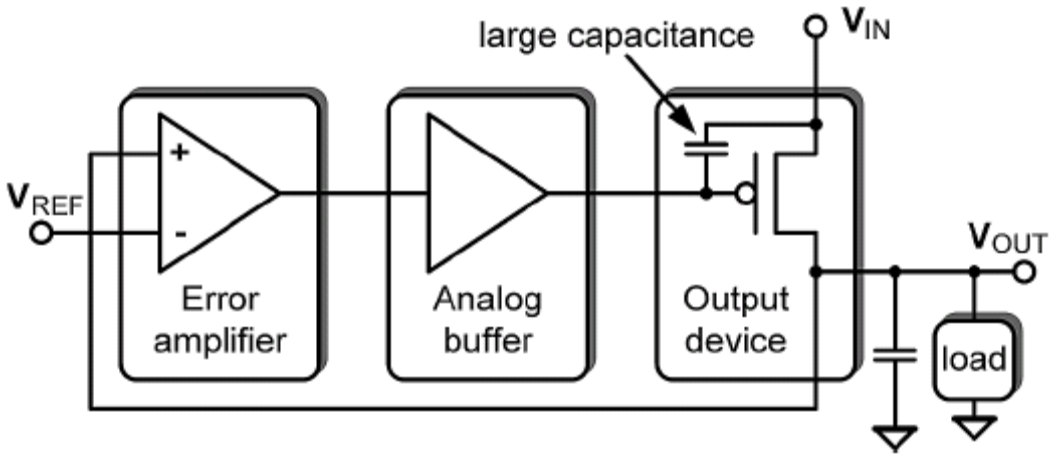


Fig. 3.15 Conventional linear regulator topology.

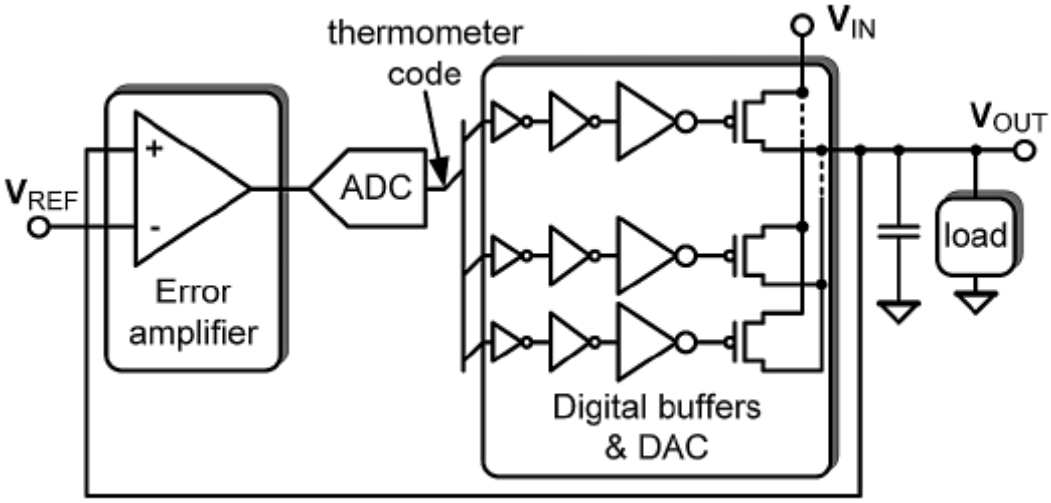


Fig. 3.16 Linear regulator with digital buffer.

The inverters are nearly perfect class AB circuits. They draw very little current when idle and provide large output current when switching. As shown in Fig. 3.16[16], the inverters are used as digital buffer. The signal from the error amplifier is first translated by an A/D converter into a thermometer-coded digital output. Digital buffers add drive strength so that the A/D converter can quickly turn on and off the parallel legs of the output device. In the steady state, very little current is consumed in driving of the output devices, which eliminates speed-power tradeoff that plagues traditional class A analog buffers. The schematic of regulator is shown in Fig. 3.17[16].

The reference voltage V_{REF} is produced between I_0 and I_5. Circuits in the 1 x V_{MAX} domain (AMP_1, ADC_1, DAC_1) are supplied between ground and V_{OUT} and circuits in the 2 x V_{MAX} domain (AMP_2, ADC_2, DAC_2) are supplied between V_{OUT} and V_{IN}. Inverters $I_0 – I_2$, $I_5 – I_7$, and the comparators in ADC_1 and ADC_2 are matched to have equal trip point. Inverters I_3 and I_4 have wider NMOS devices to lower the trip point. Inverters I_8 and I_9 have wider PMOS devices to raise the trip point. Skewing of the

trip points is indicated by an offset added to the inputs of I_3 and I_8. Gain of AMP1 and AMP2 are relative to size of I_1 to I_2, I_3 to I_4, I_6 to I_7 and I_8 to I_9. A feedback signal from VOUT couples to AMP1 and AMP2 via the supply rail. The amplifier will create different voltages across the resistive networks of ADC_1 and ADC_2.When $V_{OUT}=V_{REF}$, the resistors of ADC_1 and ADC_2 are biased below and above the comparator trip points, thereby producing 16-bit thermometer codes of all ones and all zeros, respectively. The NMOS devices of DAC_1 and PMOS devices of DAC_2 are off and the output current is zero.

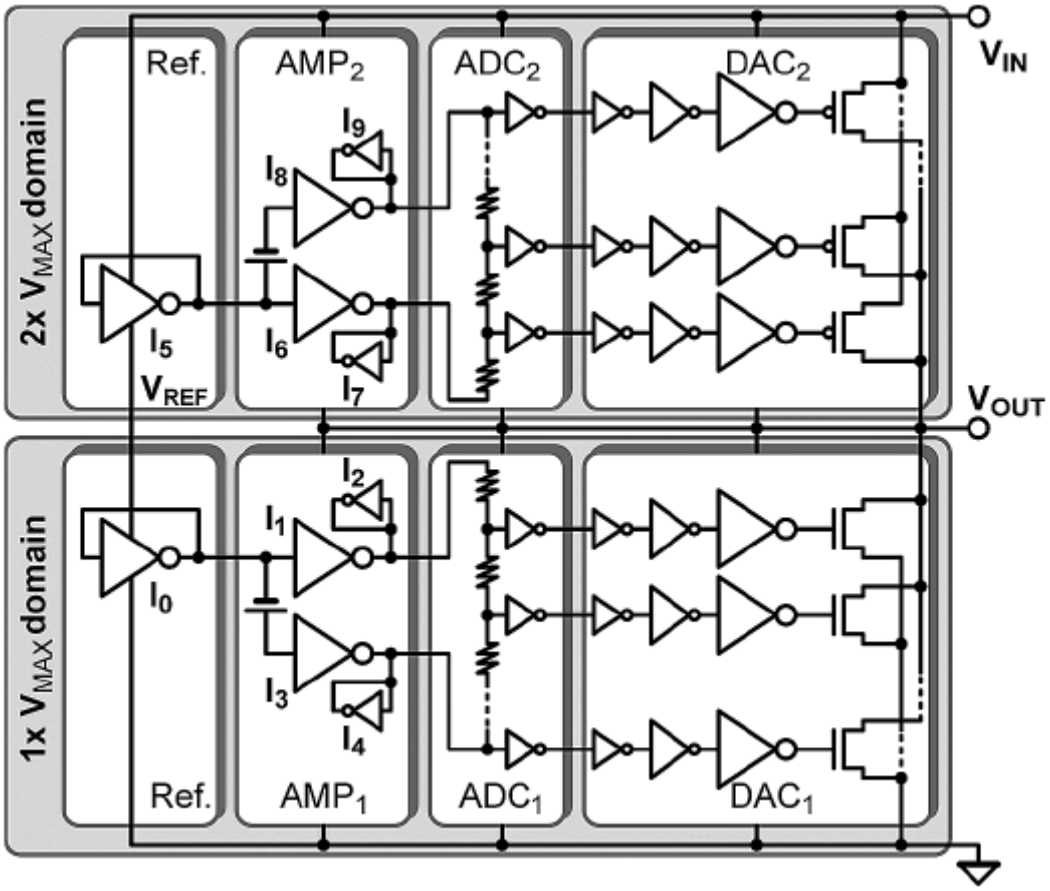


Fig. 3.17 Schematic of linear regulator with digital buffer.

3.4 Reference Voltage Circuit

The voltage regulator needs a reference voltage to bias the output voltage. The reference voltage circuit is reference from senior and is shown in Fig. 3.18[17]. The reference voltage circuit is composed of a startup circuit and a reference voltage generator. The startup circuit is composed of M1, M2 and M3. M1, M2 and M3 are operated at saturation region. The reference voltage generator is composed of M4, M5, M6, M7 and M8. M5, M7, M8 are operated at saturation region. M4 and M6 are operated at linear region. The design concept is shown in Fig. 3.19[17]. The M5 and

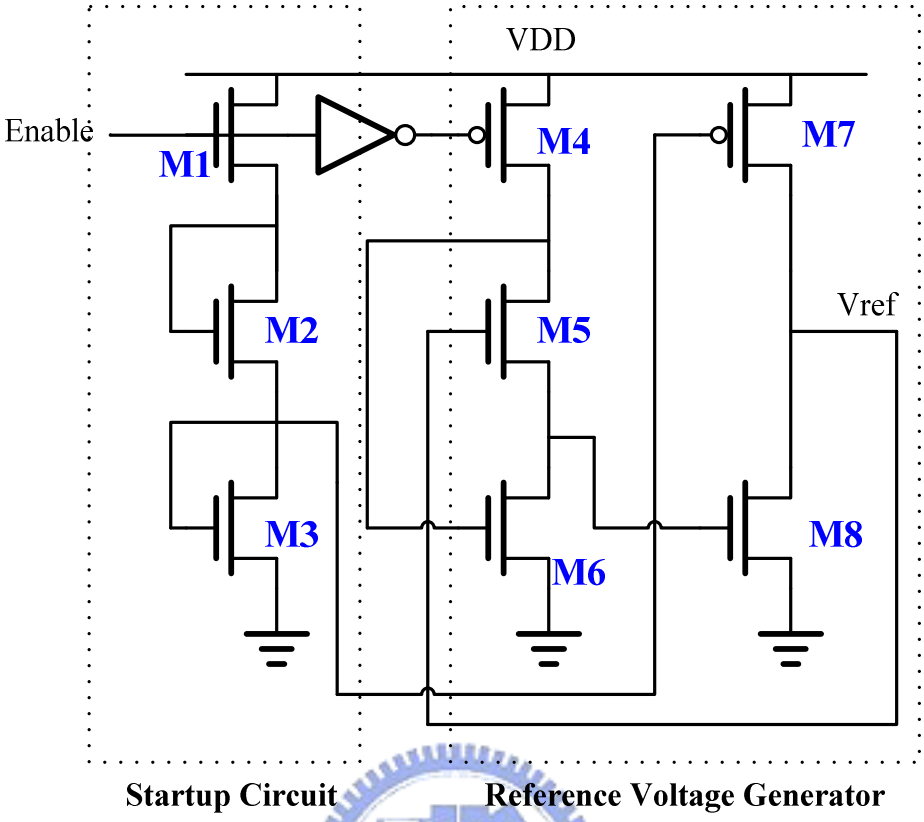


Fig. 3.18 Reference voltage circuit [17].

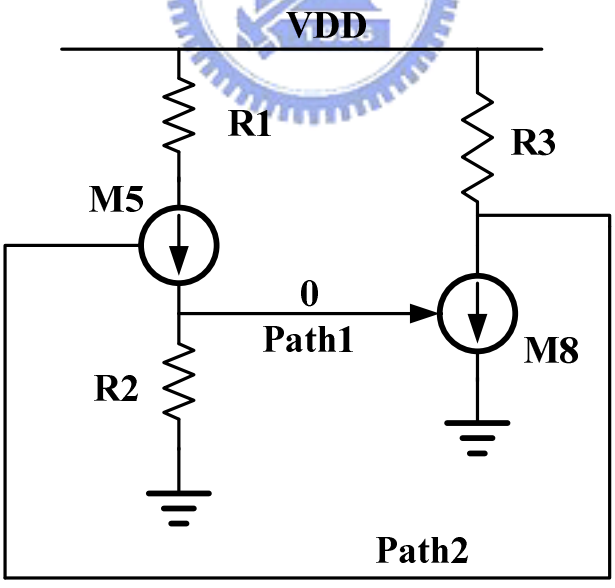


Fig. 3.19 The design of reference voltage circuit [17].

M8 are operated at saturation region, so it is to be a current source which is shown in Fig. 3.19. M4, M6 and M7 are operated at linear region, so it is to be a resistor. In this reference voltage generator, there are two important paths, path1 (P1) and path2 (P2). P1 is a supply-independent skill to reduce the dependency between M2 current and

supply voltage. P2 is a negative feedback compensation to increase the V_{ref} stability. M5 and M8 are operated in saturation region to be a voltage control current source, so M5 and M8 will pull each other. On the other hand, it should be point out that in this reference voltage generator, the M5 and M8 must be operated at saturation region, so it is to be a current source. The M4, M6 and M7 must be operated at linear region, so it is to be a resistor.

The work in [17] is implemented in 130nm CMOS technology. We have transport it into UMC 90nm CMOS technology. In order to improve the stability of reference voltage under different temperature, we change the devices of M1 and M7. As shown in Fig. 3.20, M7 is NMOS, and its gate is biased by gate of M2. For biasing M7, the M1 is changed to PMOS.

Temperature variation analysis:

The temperature variation affect the threshold voltage of M1~M8 in Fig. 3.18 [17] and Fig. 3.20. The difference in these two circuits is the influence of M2, M3 and M7. In Fig. 3.18, as the temperature going up, the voltage of M3's gate is decreased and M7's threshold voltage is decreased. Thus, the temperature affects the M3 and M7 to increase the current of M7. In Fig. 3.21, as the temperature going up, the voltage of M3's gate is decreased and M7's threshold voltage is decreased. Because the M7 is NMOS, so the temperature affects the M3 to decrease the current of M7. Therefore, the circuit in Fig. 3.20 will more stable in different temperature. The simulation results are shown in Fig. 3.21. The results are simulated in UMC 90nm CMOS technology.

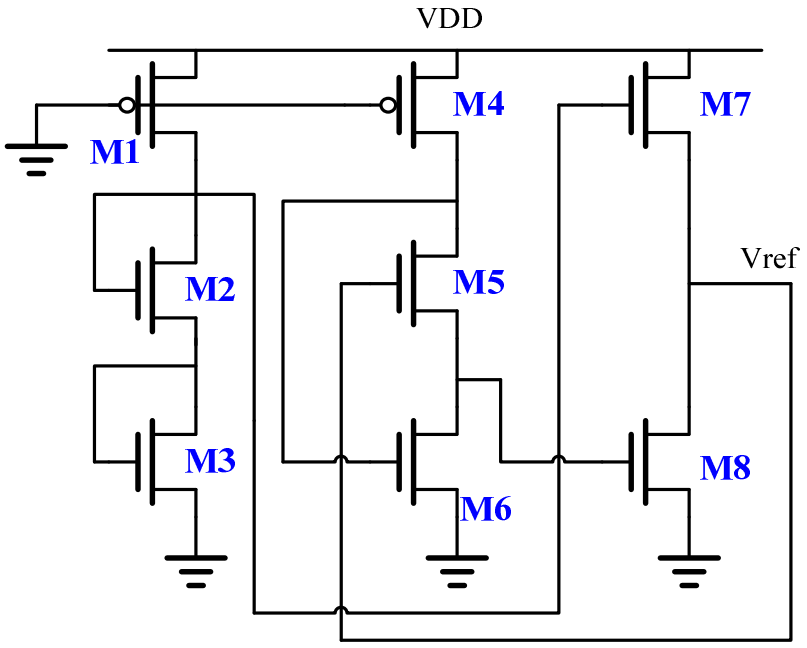
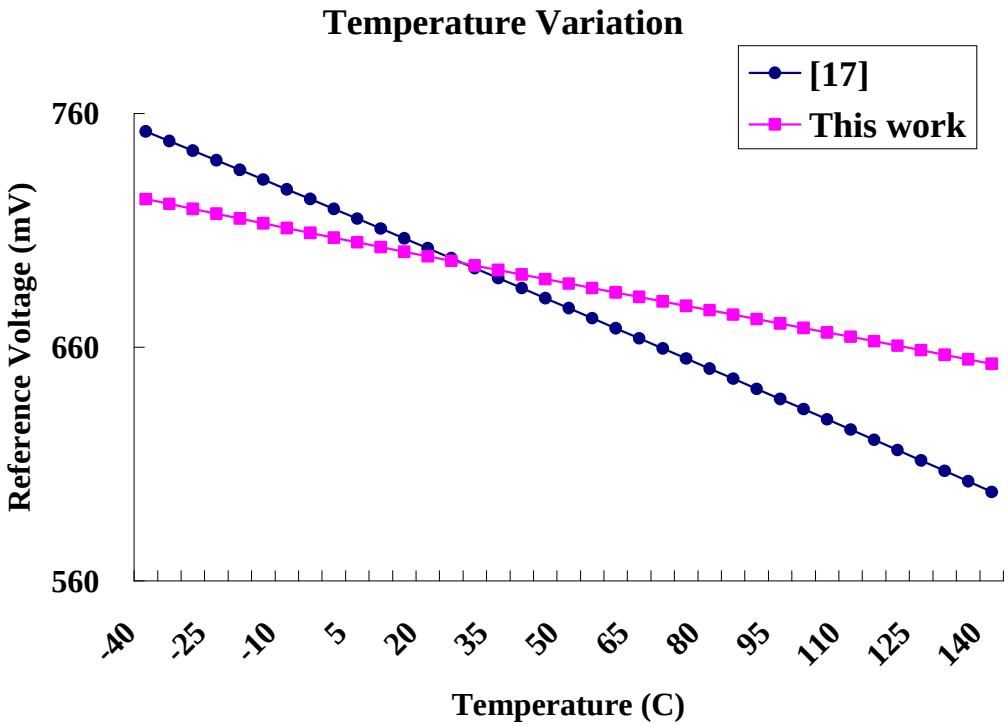
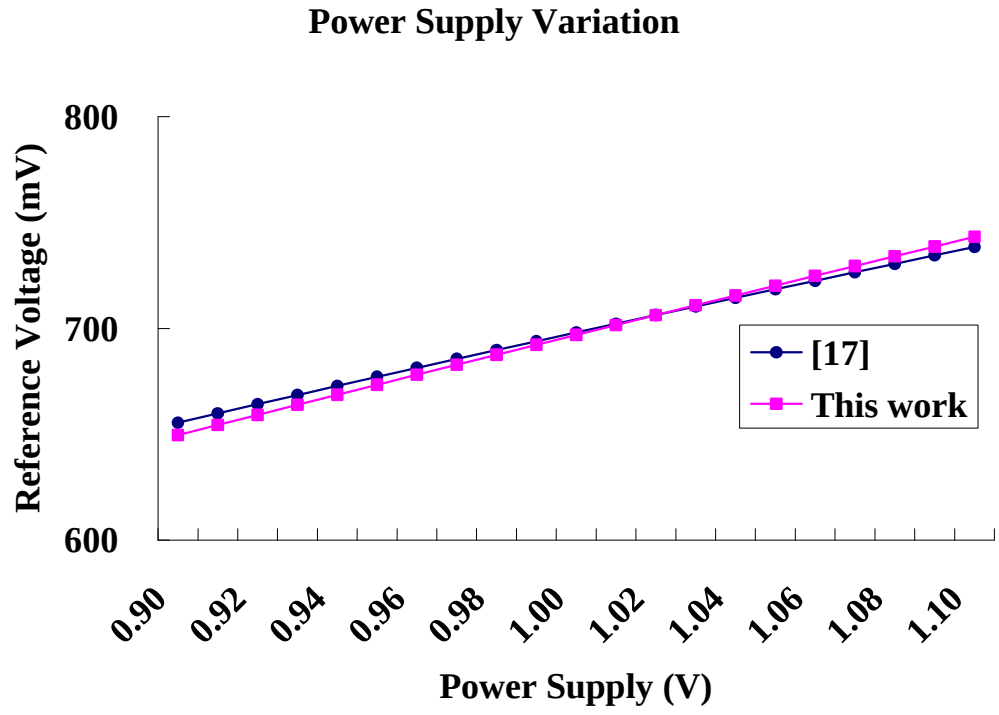


Fig. 3.20 Reference voltage circuit in this work.



(a)



(b)

Fig. 3.21 Reference voltage circuit generates 700mV. (a) Temperature variation. (b) Power supply variation.

Table 3.1 Comparison 700mV generator of [17] and this work.

	[17]	This work
Technology (nm)	90	90
Supply voltage (Vsupply)	1V	1V
Reference voltage (Vref)	700mV	700mV
Supply variation (0.9V~1.1V)	655mV~738mV	650mV~743mV
ΔVref / ΔVsupply (V/V)	0.42	0.47
Temperature variation (-40^{o}C~140^{o}C)	752mV~598mV	723mV~653mV
ΔVref / ΔTemperature (V/^{o}C)	0.86	0.39
Power consumption	74.5uW	65.5uW

3.5 Proposed Voltage Regulator

3.5.1 A Voltage Regulator using Dynamic-Biased OP Amp

In order to decrease the bias current of op amp and stabilize the transient response of regulator simultaneous, we proposed a dynamic-biased control scheme for biasing op amp. The schematic of proposed voltage regulator is shown in Fig. 3.18.

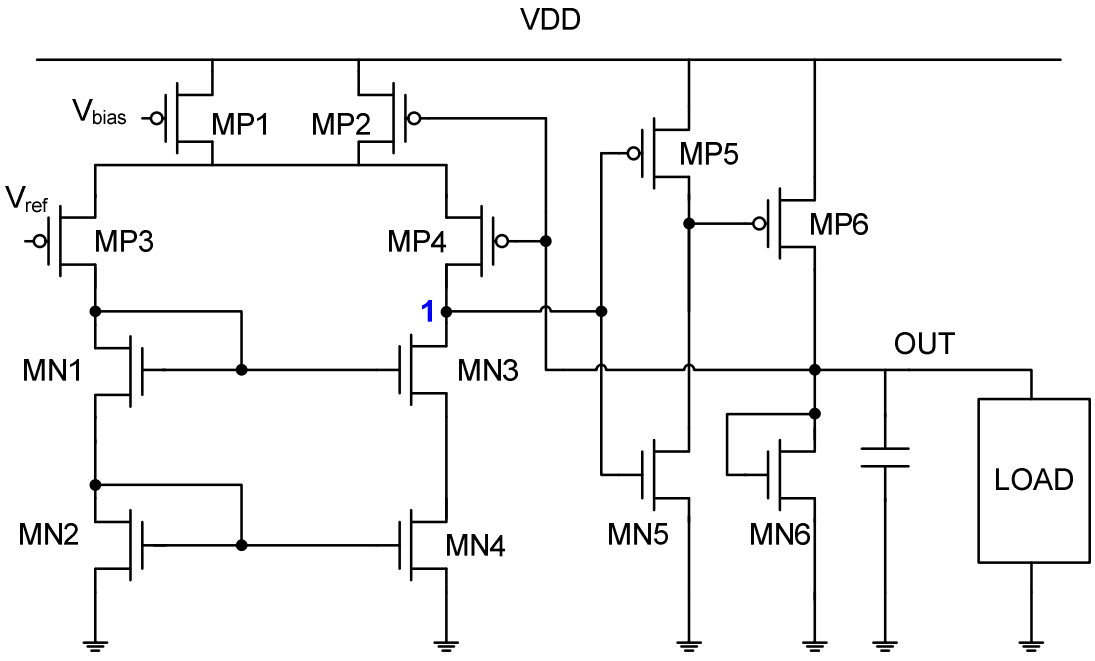


Fig. 3.22 Voltage regulator with dynamic-biased op amp.

The voltage regulator is composed of op amp, a voltage buffer, a POWERT PMOS transistor and dynamic-biased circuit. The op amp is composed of MP1, MP3, MP4, MN1, MN2, MN3, and MN4. The voltage buffer is composed of MP5 and MN5. The voltage buffer is an inverter, thus its output swings between VDD and 0. The dynamic-biased circuit is MP2. The gate of MP2 is controlled by node OUT. When there is no load current, the voltage of node OUT is Vref and the MP2 supplies a little current to op amp. As the load current increase suddenly, the voltage of node OUT will drop down. Thus, the MP2 will supply extra current to op amp. With the extra current from MP2, the slew rate of op amp is increased and the voltage of node 1 will be raised up rapidly. Therefore, the buffer will turn on the POWER PMOS MP6 to supply current to loading.

The simulation results of voltage regulator using dynamic-biased OP amp are shown in Fig. 3.23. When load current is 0mA, the voltage regulator outputs 730mV and the quiescent current is 1mA. When load current is 100mA, the output voltage of voltage regulator will drop down and is stable in 620mV. The current efficiency is 99%.

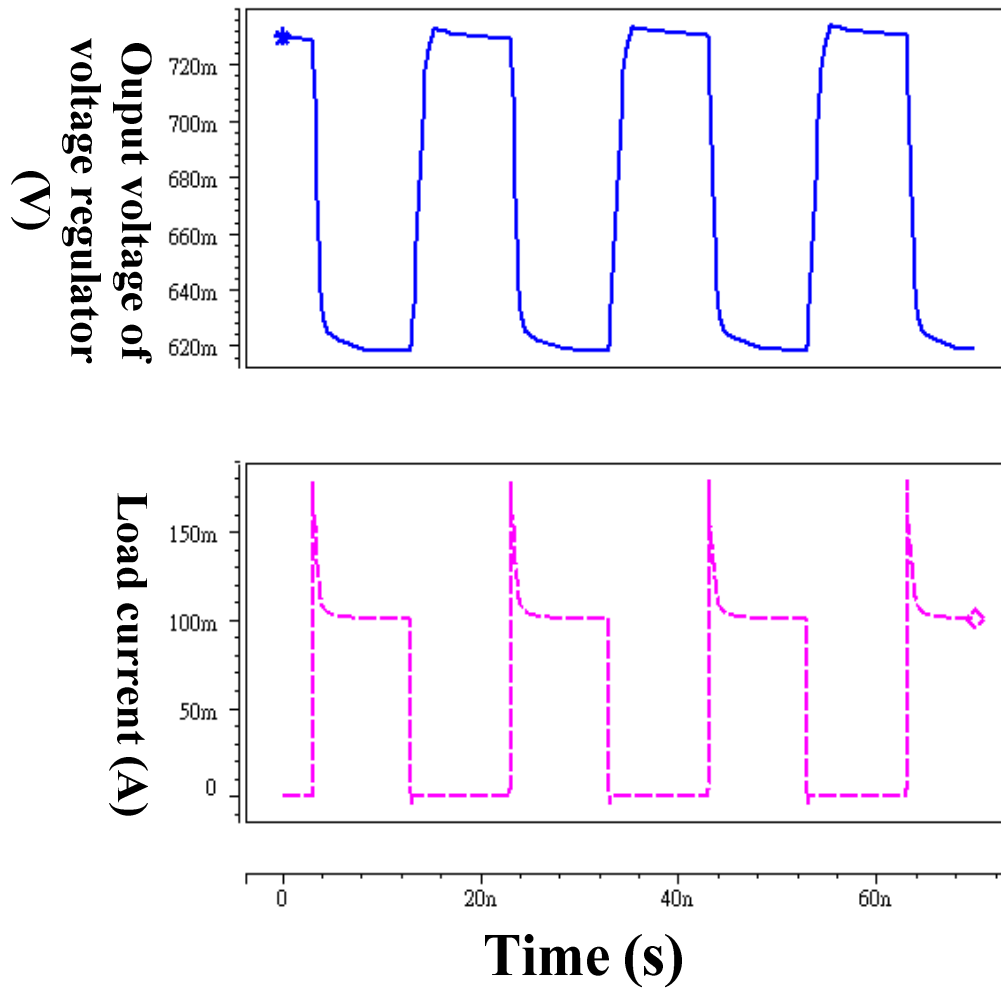
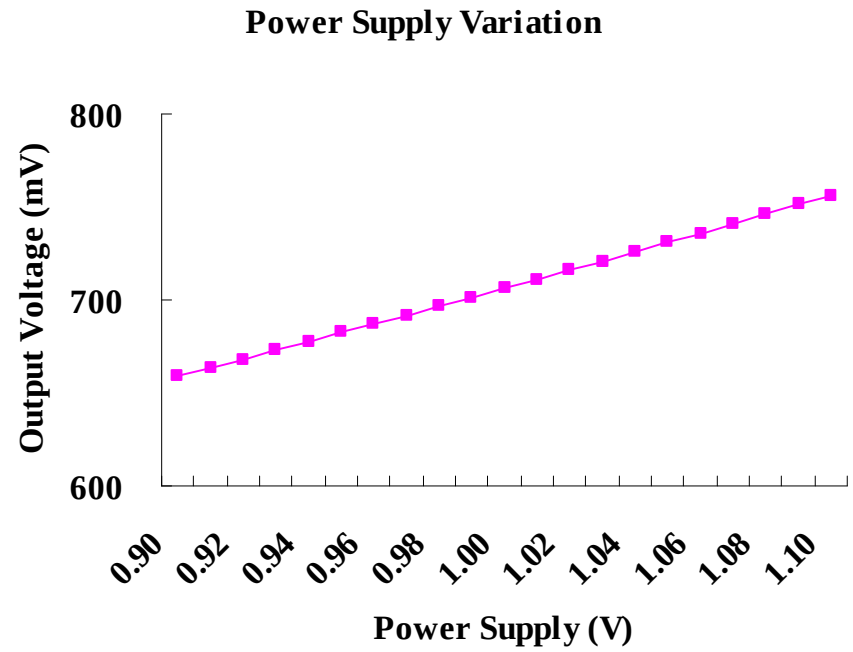
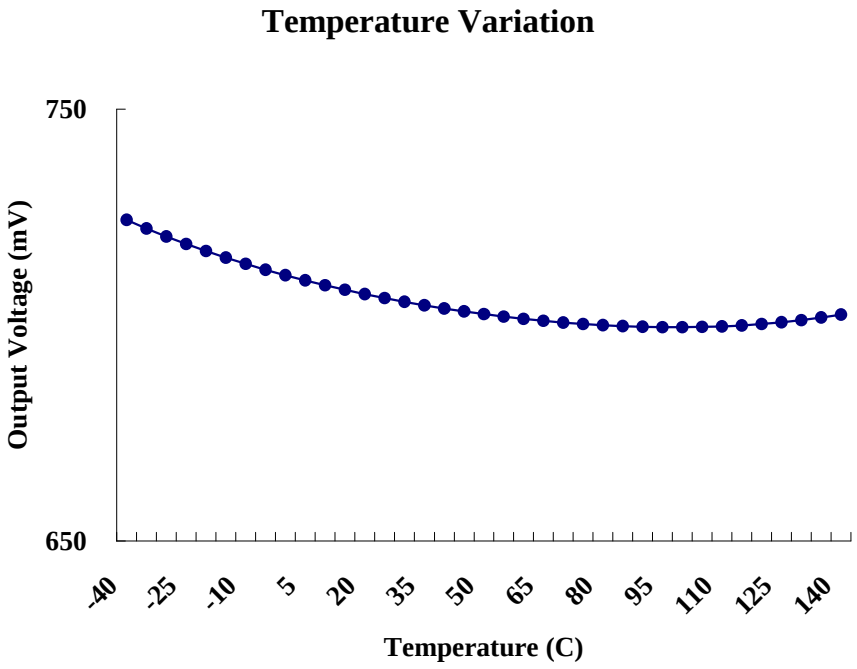


Fig. 3.23 Output voltage of voltage regulator under different Load current.

The simulation of output voltage under different supply voltage and temperature are shown in Fig. 3.24. When the supply voltage varies from 1.1V to 0.9V, the output voltage is varied from 659mV to 756mV. When the temperature varies from $-40^{\circ}C$ to$140^{\circ}C$, the output voltage swings between 699mV and 724mV.



(a)



(b)

Fig. 3.24 Output voltage with (a) supply voltage variation (b) temperature variation.

3.5.2 A Voltage Regulator using Schmitt Trigger

The operation of voltage regulator is when output voltage is smaller than Vref, the POWER PMOS transistor of voltage regulator will be turned on to supply current to loading. As the output voltage is larger than Vref, the POWER PMOS transistor of voltage regulator will be turned off. Therefore, the Schmitt trigger can apply to voltage regulator.

The voltage regulator using Schmitt trigger is shown in Fig. 3.25. The regulator is composed of bias part and compensation part. The bias part is composed of MN1, MN2, MP1 and MP2. The compensation part is composed of two Schmitt trigger. When load current is zero, the bias part supplies a dc voltage to output node. As output voltage is drop down, the Schmitt trigger 2 will turn on the MOUT. Because the Schmitt trigger has characteristic of low quiescent current and high response speed, so the quiescent of the voltage regulator is very small.

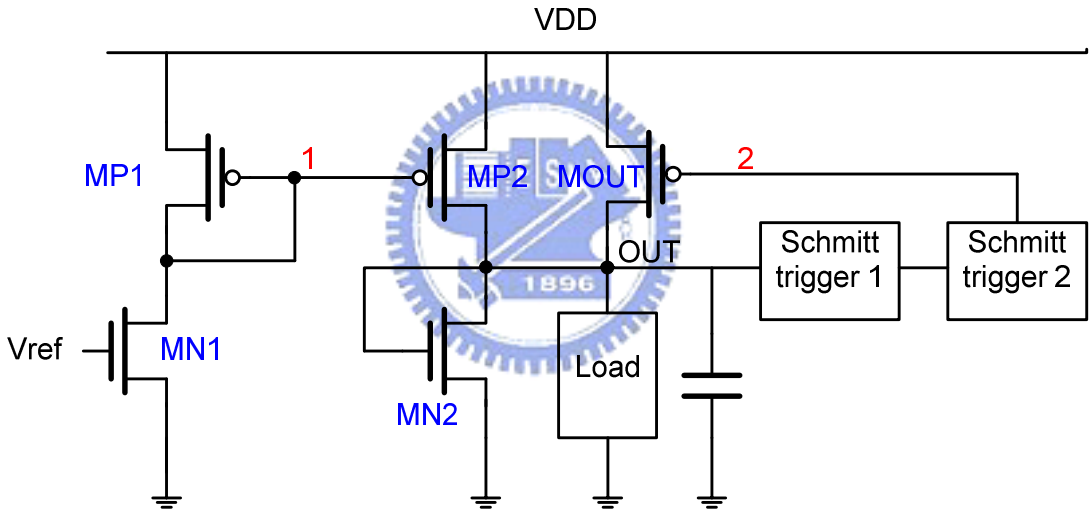


Fig. 3.25 Voltage regulator using Schmitt trigger.

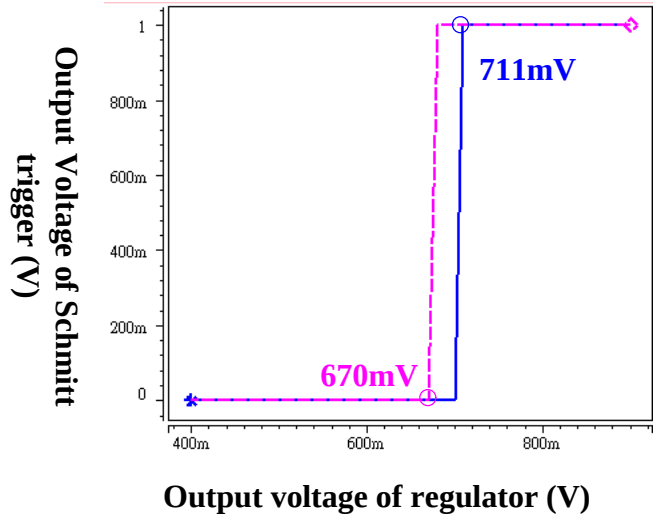


Fig. 3.26 Transfer function of the cascading Schmitt trigger.

The simulation results of voltage regulator using Schmitt trigger are shown in Fig. 3.26 and Fig. 3.27. The transfer function of cascading Schmitt trigger is shown in Fig. 3.26. As the output voltage of regulator is smaller than 670mV, the Schmitt trigger will turn on the POWER PMOS transistor of voltage regulator to supply current to loading. As the output voltage of regulator is larger than 711mV, the Schmitt trigger will turn off the POWER PMOS transistor.

When load current is 0mA, the voltage regulator outputs 720mV and the quiescent current is 0.65mA. When load current is 100mA, the output voltage of voltage regulator will drop down and is stable in 600mV.

The simulation of output voltage under different supply voltage and temperature are shown in Fig. 3.28. When the supply voltage varies from 1.1V to 0.9V, the output voltage is varied from 646mV to 732mV. When the temperature varies from $-40^{o}\mathrm{C}$ to $140^{o}\mathrm{C}$, the output voltage swings between 680mV and 711mV. The current efficiency is 99.4%.

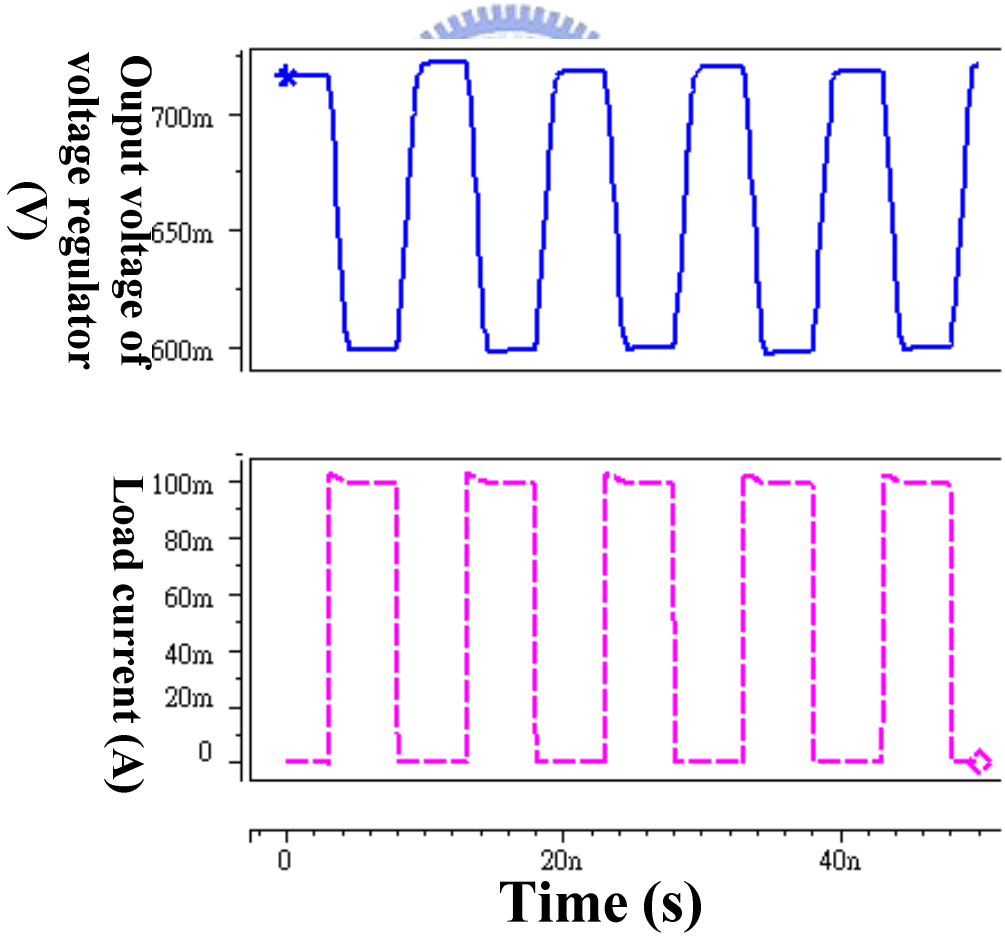
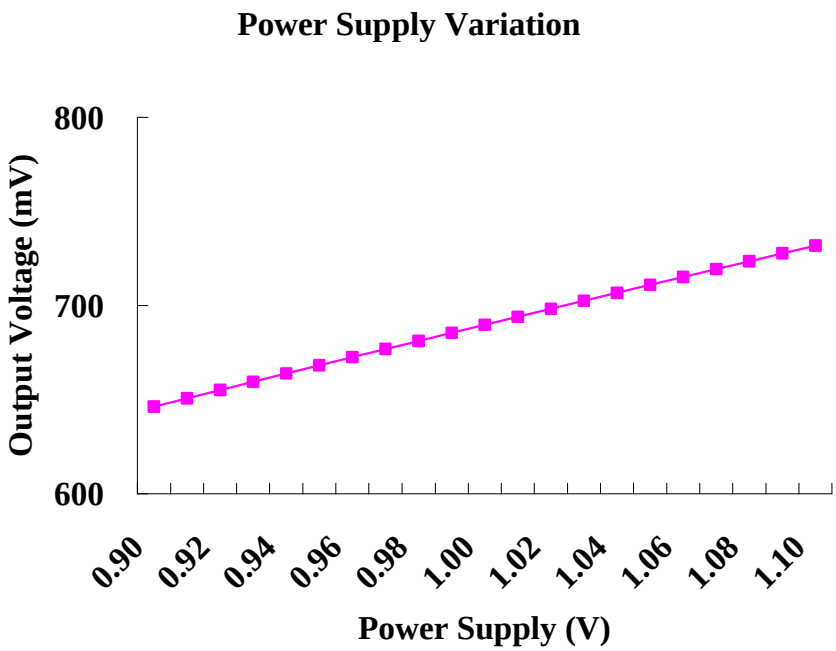
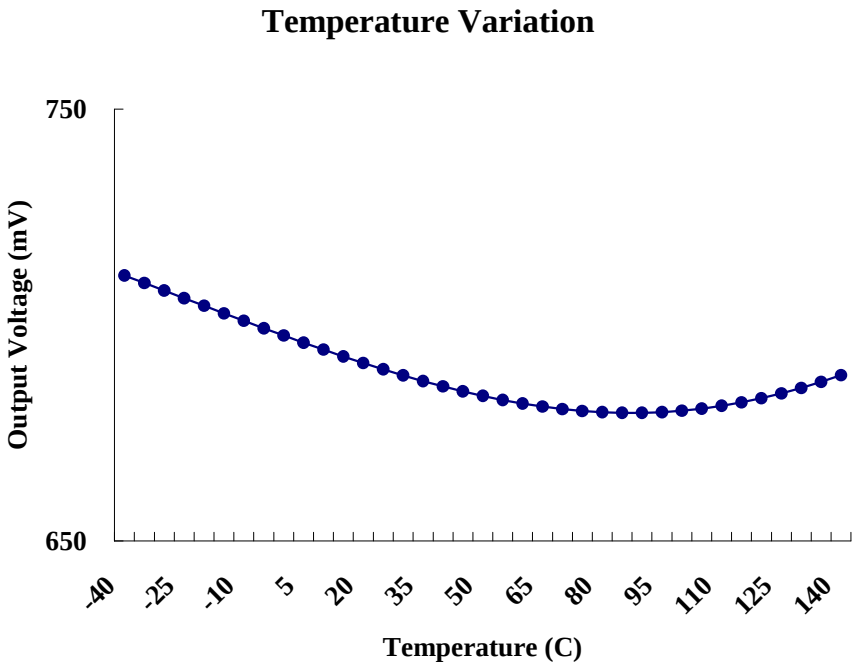


Fig. 3.27 Output voltage of voltage regulator under different Load current.



(a)



(b)

Fig. 3.28 Output voltage with (a) supply voltage variation (b) temperature variation.

3.5.3 Comparison

The comparison of these two voltage regulator with previous work ([15] and [16]) is shown in table 3.2.

Table 3.2 Comparison of [15], [16] and proposed voltage regulator.

	[15]	[16]	Voltage regulator I	Voltage regulator II
Technology (nm)	90	90	90	90
Input Voltage	1.2V	2.4V	1V	1V
Output Voltage	0.9V	1.2V	0.7V	0.7V
Output droop ΔV_{OUT}	90mV	120mV	110mV	120mV
Rise time of Step Load current	100ps	50ps	100ps	100ps
MAX Load Current	100mA	1A	100mA	100mA
I_Q (quiescent current)	6mA	25.7mA	1mA	0.65mA
Current Efficiency	94.3%	97.5%	99%	99.4%
Decoupling Cap.	0.6nF	2.4nF	0.4nF	1.1nF
Response time	540ps	288ps	440ps	1320ps
FOM	32ps	7.4ps	4.4ps	8.58ps

*** Voltage regulator I: the voltage regulator using dynamic-biasing op amp.**

*** Voltage regulator II: the voltage regulator using Schmitt trigger.**

$$Current\ efficiency = \frac{I_{MAX}}{I_{MAX} + I_Q}$$

$$T_R = \frac{C * \Delta V_{OUT}}{I_{MAX}} \qquad FOM = T_R \frac{I_Q}{I_{MAX}} = \frac{C * \Delta V_{OUT}}{I_{MAX}} * \frac{I_Q}{I_{MAX}}$$

C : Decoupling capacitor

ΔVOUT : Output droop

I_{MAX} : Maximum load current

IQ : Quiescent current

3.6 Summary

In this chapter, the stability scheme, transient response scheme of voltage regulator is introduced. The voltage regulator using digital buffer is also introduced. A reference voltage circuit is introduced. We improve the temperature coefficient of the reference voltage circuit and apply it to our voltage regulator.

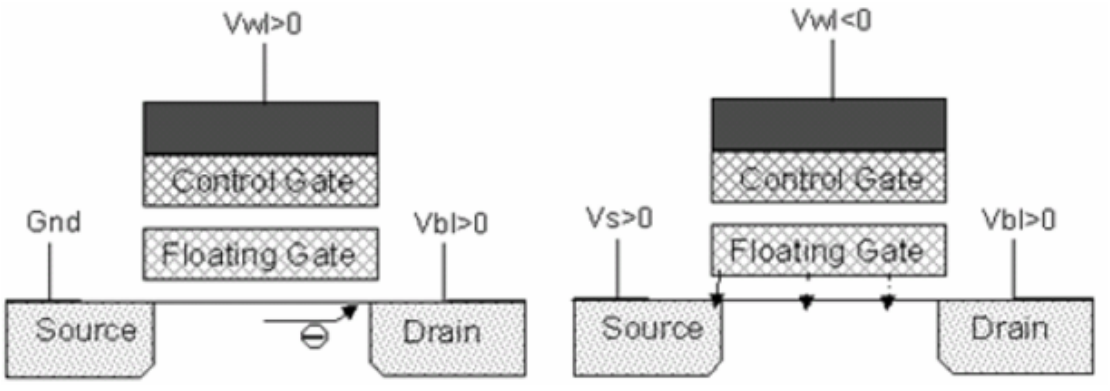
We proposed two voltage regulators that are voltage regulator using dynamic-biased scheme op amp and voltage regulator using Schmitt trigger. The voltage regulator using dynamic-biased scheme op amp has only 1mA quiescent current when no load current. Its current efficiency is 99% and the FOM is 4.4ps. The voltage regulator using Schmitt trigger has only 0.65mA quiescent current when no load current. Its current efficiency is 99.4% and the FOM is 8.58ps.

Chapter 4
Charge Pumps

To programming the information of nonvolatile memory like flash memory, the voltage adding to the gate must higher than power supply voltage as shown in Fig. 4.1(a) [18]. And negative voltage will add to gate when erasing the information of flash memory as shown in Fig. 4.1(b). Charge pump is used to generating such high voltage and negative voltage. Also, the high voltage can be used to improve the performance of the circuit.

There are many types of charge pump such as voltage doubler, voltage multiplier and Dickson charge pump. The Dickson charge pump is usually used to generate ultra high voltage like ten times of power supply voltage. The Dickson charge pump also can generate negative voltage.

In this Chapter, the voltage doubler is introduced and analysis in section 4.1. Ultra high voltage can be generated by Dickson charge pump. The techniques of improving the pumping efficiency of Dickson charge pump will be introduced in Section 4.2. The negative voltage generator is also introduced in Section 4.3. In Section 4.4, we proposed a simple architecture of Dickson charge pump of generating ultra high voltage. And a novel connect scheme of charge pump is proposed for generating ultra high voltage with using CMOS as pumping capacitor. All results are simulated in UMC 90nm CMOS technology model.



(a) (b)

Fig. 4.1 (a) Programming: channel hot electron (CHE) injection in the floating gate at the drain side. (b) Erasing: Fowler-Nordheim (FN) electron tunneling current through the tunnel oxide from the floating gate to the silicon surface.

4.1 Voltage Doubler

The voltage doubler can generate twice the magnitude of supply voltage. A voltage doubler is illustrated in Fig. 4.2[22].

During clock phase Φ, switches S_1 and S_3 are closed and the capacitor is charged to the supply voltage, V_{DD}. Next switch S_2 is closed and the bottom plate of the capacitor assumes a potential V_{DD}, while the capacitor maintains its charge of $V_{DD}C$ from the previous phase. This means that during $\overline{\Phi}$

$$(V_{out} - V_{DD}) \cdot C = V_{DD} \cdot C$$

or

$$V_{out} = 2 \cdot V_{DD}$$

Thus, in the absence of a dc load, an output voltage has been generated that is twice the supply voltage.

4.1.1 Voltage Multiplier

Voltage multiplication greater than twice the supply voltage can be achieved by cascading more than one capacitor in series. This voltage multiplier technique is proposed by Cockroft and Walton. The Cockroft-Walton multiplying circuit is shown in Fig. 23. Three capacitors, C_A, C_B and C_C, each of capacity C, are connected in series and capacitor C_A is connected to the supply voltage V_{DD}. During phase Φ capacitor C_1 is connected to C_A and charge to voltage V_{DD}. When the switches change position during the next cycle, $\overline{\Phi}$, capacitor C_1 will share its charge with capacitor C_B and both will be charged to $V_{DD}/2$ if they have equal capacity. In the next cycle,

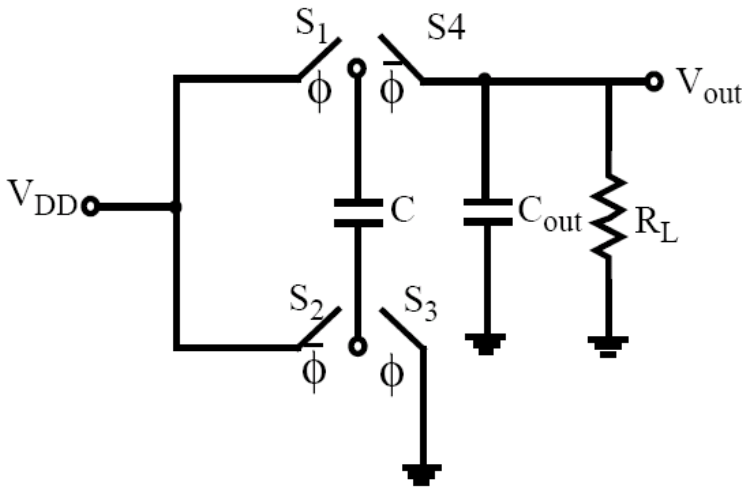


Fig. 4.2 Voltage doubler.

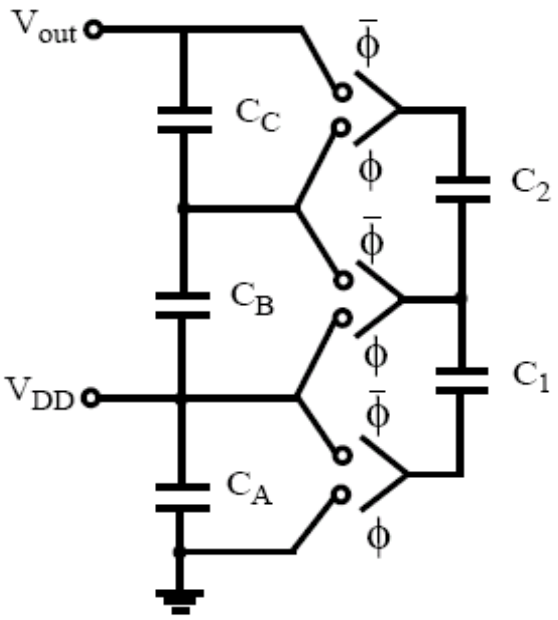


Fig. 4.3 Cockcroft-Walton voltage multiplier

C_2 and C_B will be connected and share a potential of $V_{DD}/4$ while C_1 is once again charged to V_{DD}. It is thus obvious that if this process continues for a few cycles, charge will be transferred to all the capacitors until a potential of $3V_{DD}$ is developed across the output V_{out}.

4.1.2 Analysis of Voltage Doubler

A state-of-the art charge pump for flash-EEPROM high-voltage generation is shown in Fig. 4.4[23]. It is a boosted charge pump with a four-phase clocking scheme. This circuit shows a very good power efficiency at low output currents (65% at 40 uA), but the efficiency is very low at high current loads (20% at 200 uA). The reason is that in boosted charge pumps, the transistors must withstand a voltage drop of twice the supply voltage; special (high-voltage) transistors are used to avoid breakdown. The main drawback is that these transistors have higher voltage threshold and parasitic capacitances in comparison to standard ones, therefore, their behavior when used as switches is not very good. This causes the efficiency drop at high current loads and limits the switching frequency, which is usually around 10–20 MHz. The use of standard transistors is highly desirable to reduce voltage threshold and parasitic capacitances and to increase current drive capability. Reduced voltage thresholds will permit a better behavior of transistors when used as switches, which will increase efficiency and voltage gain; reduced parasitic capacitances will permit switching frequency to increase, which will reduce capacitor area.

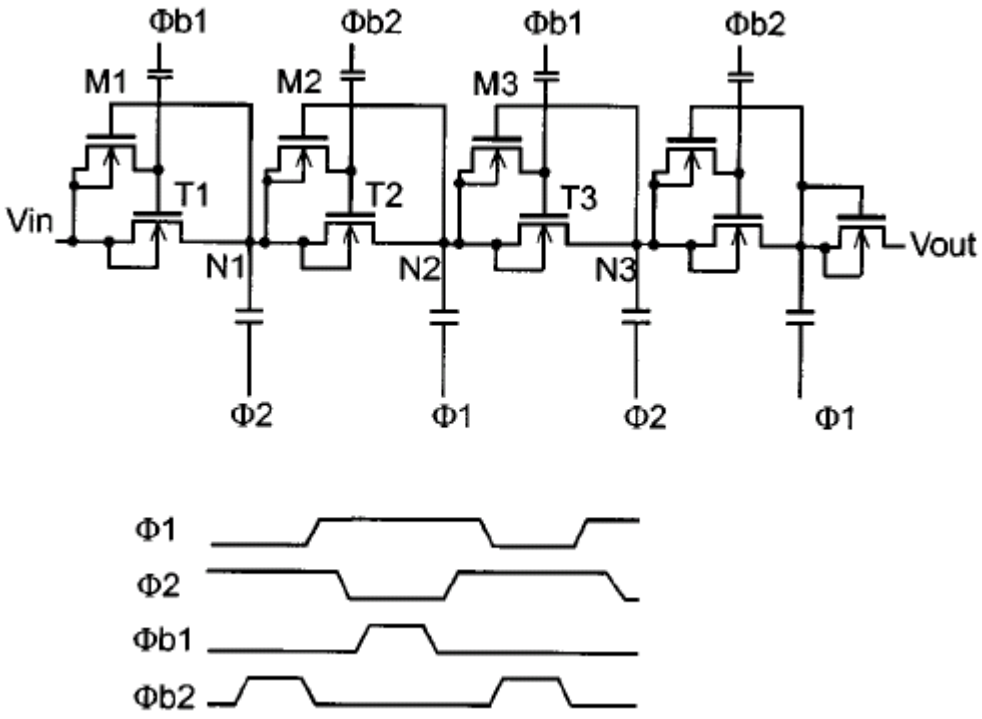


Fig. 4.4 Four stage boosted charge pump for positive high voltage generation with n-MOS transfer gates and conventional four-phase clocking scheme: Φ1 and Φ2 for charging the pump capacitors, Φb1 and Φb2 for boosting the gates during charge transfer.

On the other hand, standard transistors cannot stand voltages higher than the supply; this dictates the use of a different architecture. A simple two-phase voltage doubler is presented in Fig. 4.5[24], achieving a 70% power efficiency at 2-mA current load with 100-pF capacitors and 10-MHz switching frequency. Unfortunately, these voltage doublers cannot be cascaded because of breakdown in nMOS transistors. This problem can be solved with a triple-well process, which allows changing the nMOS bulk voltage, as shown in Figs. 4.6(a)[25]. In this way, the voltage drop across each transistor is never higher than V_{dd}. Then the pump is a cascade of voltage doubler stages with nMOS transistors in triple well; each stage can be realized with standard transistors and is driven by a simple two-phase clocking scheme; the final stage is the same as the others, i.e., no specific output stage is needed. This solution has been proposed in [26] for a step up with no current load and a low (2-MHz) switching frequency. Here, we to use it also with a current load and increasing the switching frequency to 100 MHz to reduce the capacitors; 2.5-pF capacitors are used.

In Fig. 4.6(a), suppose that I_{out}=0. After the initial transient, a stationary situation is reached. During the first half cycle, $CK=V_{dd}$, $CK_{neg}=0$, M_0 and M_3 are

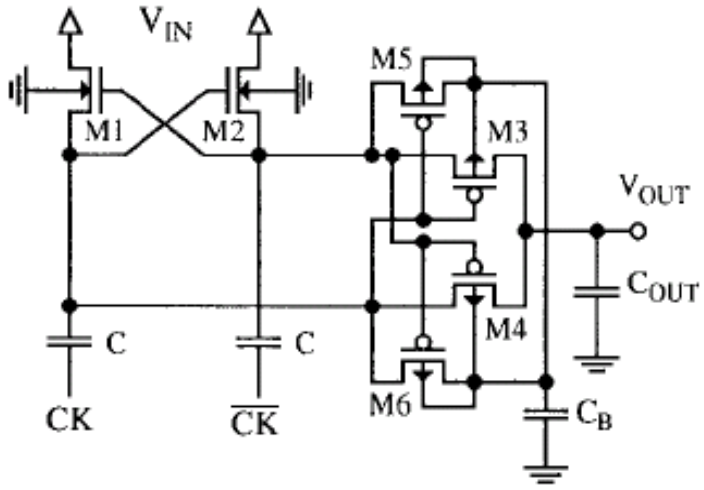


Fig. 4.5 Voltage doubler[24].

on, M_1 and M_2 are off; C_1 is discharged to V_{low} through M_0, while C_0 is charged to V_{high}, which is $V_{low}+V_{dd}$, through M_3. During the second half cycle, CK=0, $CK_{neg}=V_{dd}$, M_0 and M_3 are off, M_1 and M_2 are on; C_0 is discharged to V_{low} through M_1, while is C_1 charged to V_{high}, which is $V_{low}+V_{dd}$, through M_2. A voltage gain is therefore obtained between V_{low} and V_{high}. When $I_{OUT} \neq 0$, the voltage gain is reduced because of the stage output resistance and its value can be approximated by the following expression:

$$\Delta V = V_{dd} \cdot C / (C + C_{par1}) - R_{out} \cdot I_{out}$$

$$R_{out} = f(f_C, R_{switch})$$

$C = C_0 = C_1$, C_{par1} is the parasitic capacitance on the internal nodes of the stage, R_{out} is the stage output resistance and R_{switch} is the on-resistance of the transistor switches. R_{out} has a nonlinear dependence on f_C and R_{switch}, symbolized by the function f. C_{par2} is the bottom plate parasitic capacitance of capacitors C0, C1 shown in Fig. 4.6(a).

Cascading n stages as shown in Fig. 4.6(b), gives:

$$V_{out} = V_{dd} + n \cdot \Delta V$$

The main current contribution to the load is given by the stage drivers. Drivers and switches must be carefully dimensioned so that at every clock cycle the power transfer is efficient. The proposed values have been chosen for maximum power efficiency at f = 100MHz. The following expression is used to evaluate power efficiency, Where $\underline{V_{out}}$ and $\underline{I(V_{dd})}$ are the mean values of V_{out} and $I(V_{dd})$.

$$Eff = 100\% \cdot P_{out} / P_{in} = 100\% \cdot \underline{V_{out}} \cdot I_{out} / V_{dd} \cdot \underline{I(V_{dd})}$$

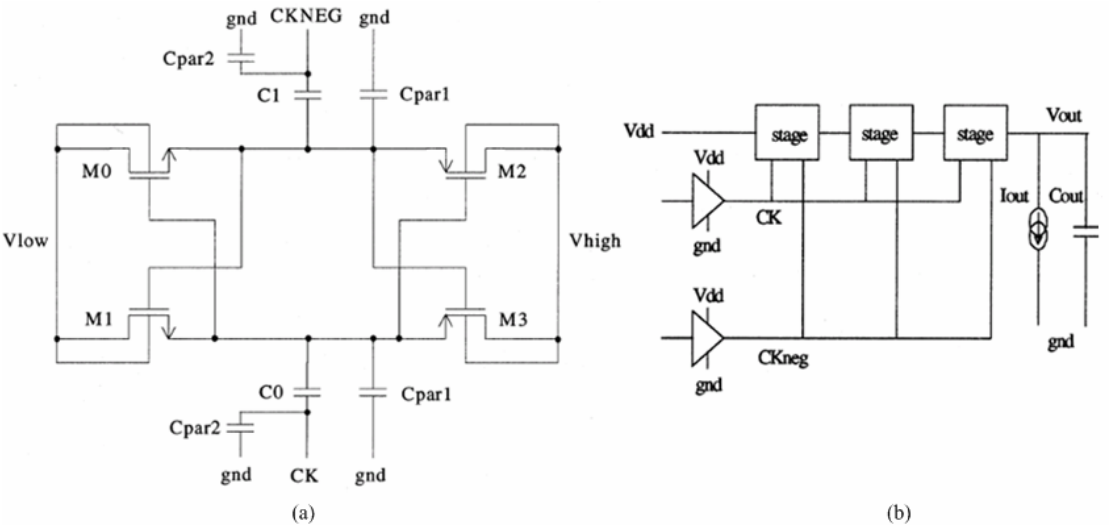


Fig. 4.6 (a) Stage schematic of the two-phase charge pump[25]. (b) Complete schematic of the tree-stage two-phase charge pump.

4.2 Dickson Charge Pump

The four-stage diode charge pump circuit using the pn-junction diodes as the charge transfer devices is shown in Fig. 4.7(a) [27]. It is difficult to implement the fully independent diodes in the common silicon substrate. In other words, the charge pump circuit with diodes shown in cannot be easily integrated into the standard CMOS process. Therefore, most charge pump circuits are based on the circuit proposed by Dickson. Fig. 4.7(b) [27] shows the four-stage Dickson charge pump circuit, where the diode-connected MOSFETs are used to transfer the charges from the present stage to the next stage. Thus, it can be easily integrated into standard CMOS processes. However, the voltage difference between the drain terminal and source terminal of the diode-connected MOSFET is the threshold voltage when the diode-connected MOSFET is turned on. Therefore, the output voltage of the four-stage Dickson charge pump circuit has been derived as

$$V_{out} = \sum_{i=1}^{5} (VDD - V_{t(Mi)})$$

where $V_{t(Mi)}$ denotes the threshold voltage of the diode-connected MOSFET M*i*. Traditionally, the bulk terminals of the diode-connected MOSFETs in the Dickson charge pump circuit are connected to ground. The threshold voltage ($V_{t(Mi)}$) of the diode-connected MOSFET becomes larger due to the body effect. The threshold voltage will increase when the source of NMOS is pumped up. Thus, the pumping efficiency will degrade as the pumping stage is increase. To solve this problem,

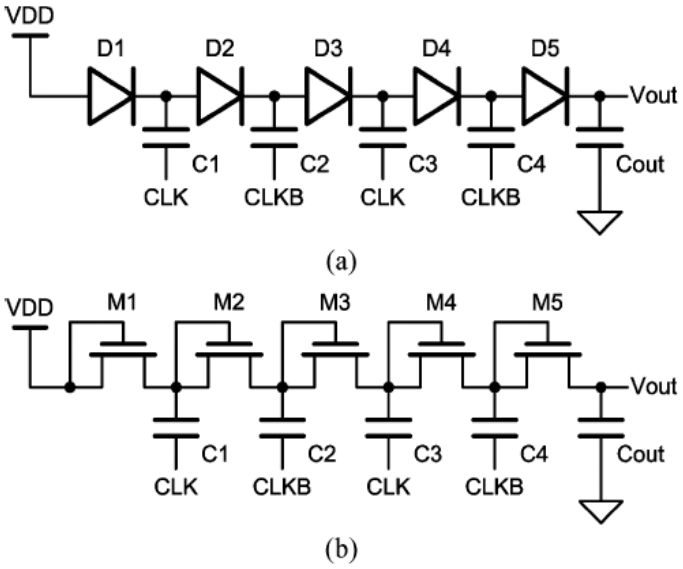


Fig. 4.7 (a) Four-stage diode charge pump circuit. (b) Dickson charge pump circuit.

solutions such as CTS (charge transfer switch), dynamic body bias scheme and four-phase clock scheme are proposed.

4.2.1 Charge Transfer Switch

To improve pumping efficiency, the CTS use NMOS as switch to transfer charge. This will ideally increase the pumping efficiency of every stage by one V_T. The structure is shown in Fig. 4.8[28].

1) Charge Pump Using Static CTS's:

The Φ_1 and Φ_2 are CLK and CLKB. When voltage is pumped up, the source voltage of next stage will turn on the switch and help previous stage to transfer charge directly. But there is a reverse charge sharing problem. Because of the switches always turn on, the charge of stage will flow back to previous stage by switch. Thus, the dynamic CTS scheme is proposed in Fig. 4.9[28].

2) Charge Pump Using Dynamic CTS's:

When CLK is low, node 1 will be VDD and node 2 will be 3vdd, then MN1 is turned off and MP1 is turned on. Thus, the MS1 will turn on to transfer charges from the power supply to node1.When CLK is high, node 1 and node 2 will be 2vdd, then MN1 is turned on and MP1 is turned off. Thus, the MS1 will turn off to prevent the charges back to the power supply. The problem is that the maximum gate to source voltage will be 3VDD, this will cause the MOS breakdown. Thus, a design with consideration of gate oxide reliability is proposed.

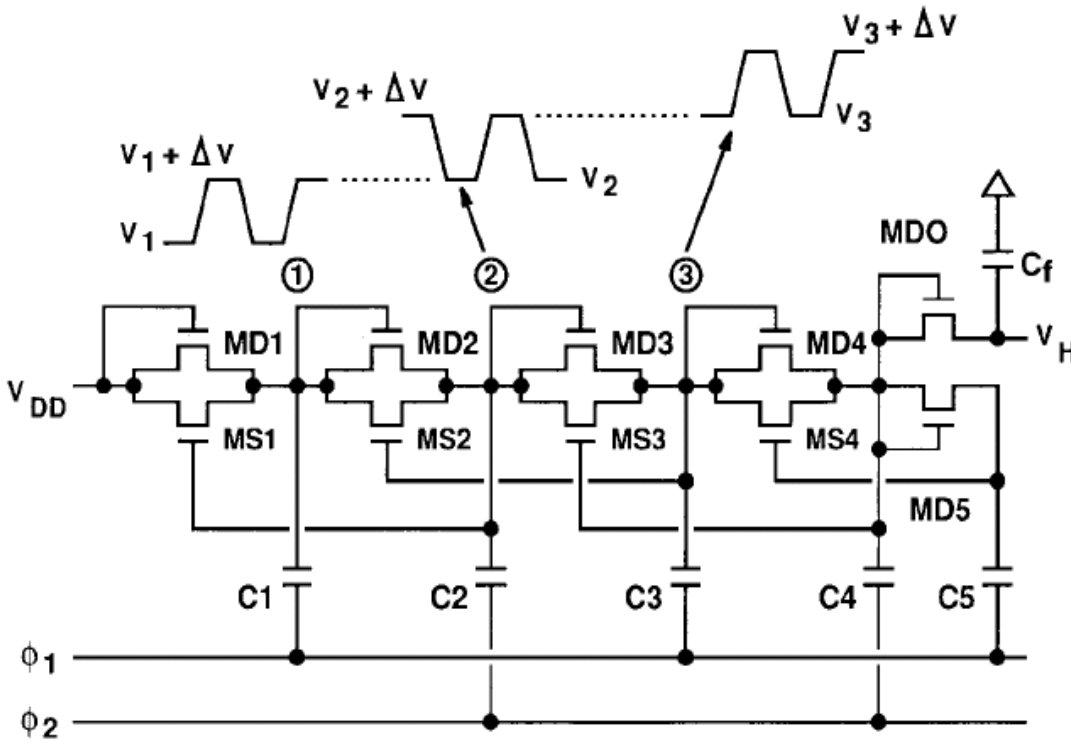


Fig. 4.8 A four-stage charge pump using static CTS's.

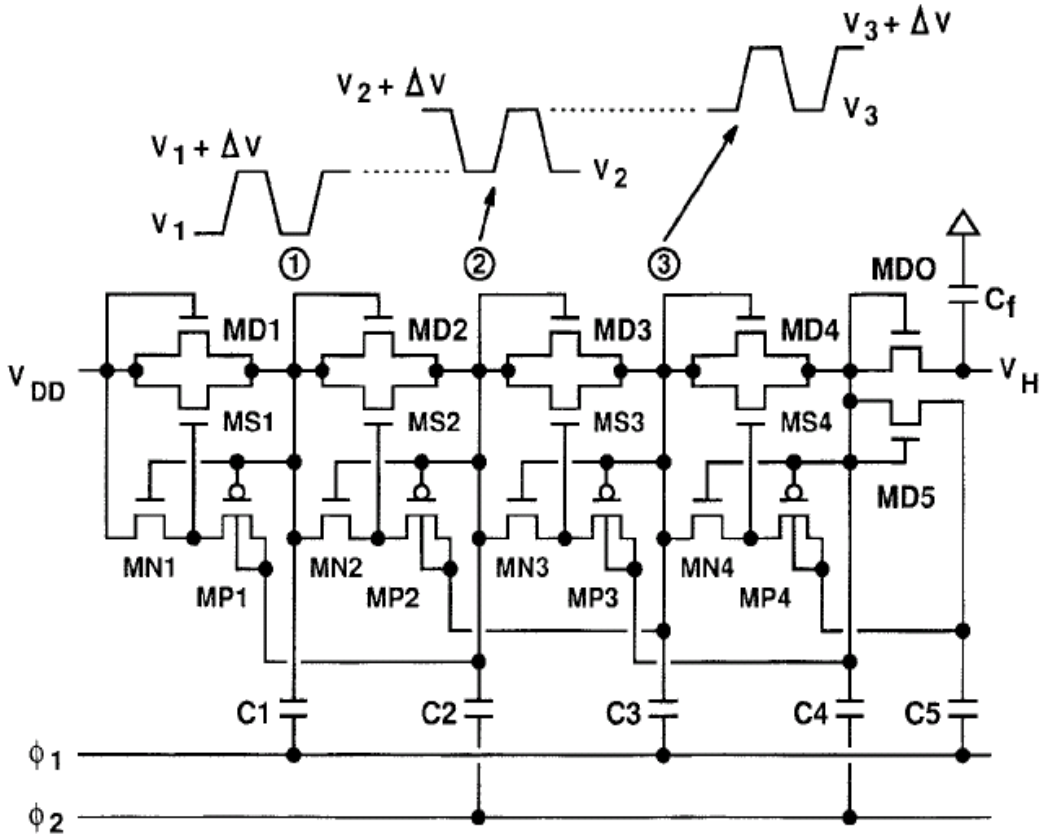


Fig. 4.9 A four-stage charge pump using dynamic CTS's.

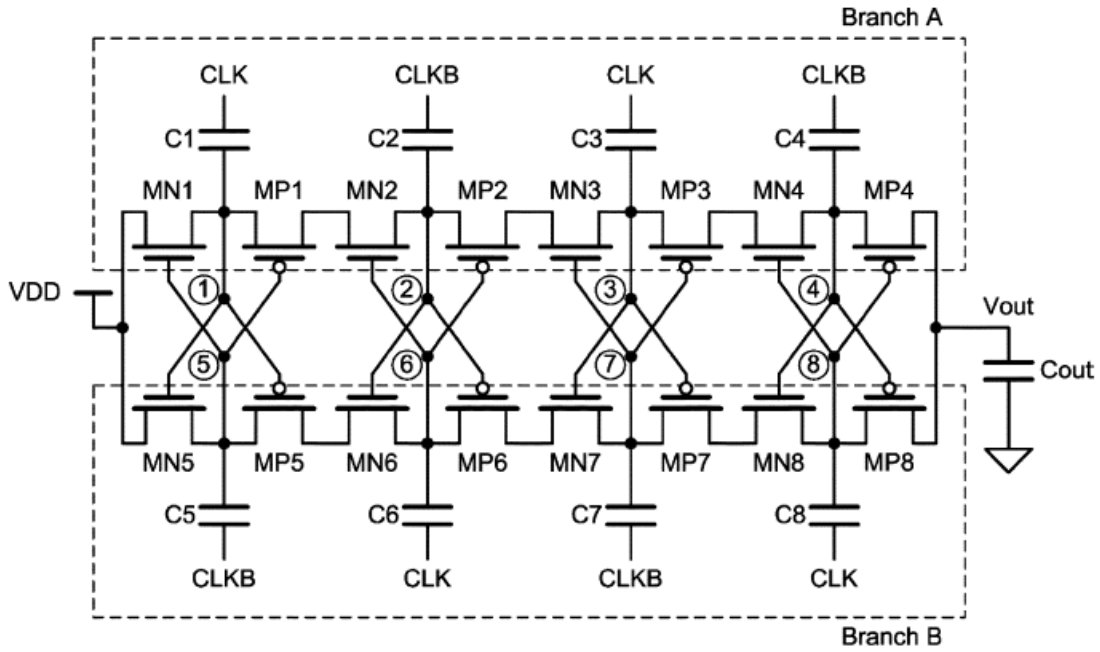


Fig. 4.10 Charge pump circuit with consideration of gate oxide reliability.

4.2.2 Charge Pump With Consideration of Gate Oxide Reliability

To avoid gate oxide breakdown problem, a new charge pump is proposed [27]. The charge pump is shown in Fig. 4.10[27]. To avoid the body effect, the bulks of the devices in the proposed charge pump circuit are recommended to be connected to their sources respectively. As shown in Fig. 4.10, there are two charge transfer branches, branch A and branch B, in the charge pump circuit. Branch A is comprised of transistors MN1, MN2, MN3, MN4, MP1, MP2, MP3, and MP4 with the capacitors C1, C2, C3, and C4. Branch B is comprised of transistors MN5, MN6, MN7, MN8, MP5, MP6, MP7, and MP8 with the capacitors C5, C6, C7, and C8. The control signals of branches A and B are intertwined. Besides, clock signals of branches A and B are out-of-phase. When the clock signals of the first and the third pumping stages in the branch A are CLK, those in the branch B are CLKB. Similarly, when the clock signals of the second and the forth pumping stages in the branch A are CLKB, those in the branch B are CLK. Thus, branches A and B can see as two independent charge pump circuits but their output nodes are connected together. Because the clock signals of the branch A and those of the branch B are out-of-phase, the voltage waveforms of nodes 1–4 and those of nodes 5–8 are also out-of-phase. Hence, branches A and B can pump the output voltage to high, alternately. The detailed operations of the new proposed charge pump circuit are described below.

In the first half cycle, the CLK is low, V51 will be VDD, then MN1 will turn on to transfer charges from power supply to node 1, but the MN5 will turned off to cut off

the path from node 5 to the power supply. Thus, the node 1 will be charged to VDD-V_{tn}. When CLK is high in first cycle, the node 1 will be 2VDD-V_{tn} and the node 5 will be charged to VDD. Thus, the V51 will be – (VDD-V_{tn}) (In this time, V62 will be VDD), then MP1 and MN2 will turn on to transfer charges from node 1 to node 2. In the second half cycle, the node 1 will be discharged to VDD and node 2 will be 2VDD. When CLK is high in second cycle, the node 1 will be 2VDD and node 2 will be VDD. Thus, the output voltage of this charge pump will be 5VDD.

4.2.3 Dynamic Bias Scheme

To solve body effect problem, the technique of dynamically biasing body node is proposed. The architecture is shown in Fig. 4.11[29]. Its detail operations are described below.

In first half cycle, the CLK=low and the M1, M2 are turned on, the M3 is turned off. Thus, the body of M1 is connected to terminal V_{DD}. When CLK=high in first cycle, the M1 and M2 are turned off and the M3 is turned on. Thus, the body of M1 is connected to node 1. In the following stage, when the charge-transfer MOSFET is ON, the body of the charge-transfer MOSFET is connected to its source side; otherwise, connected to its drain side. When the voltage is pumped up, the body node will be pumped up too. Thus, the pumping efficiency will not decrease with increasing pumping stage.

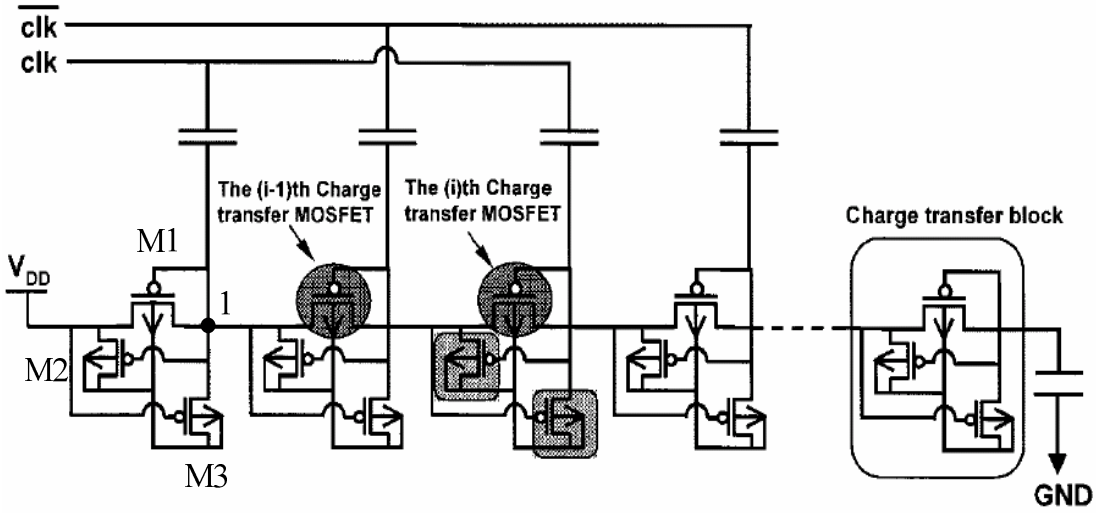
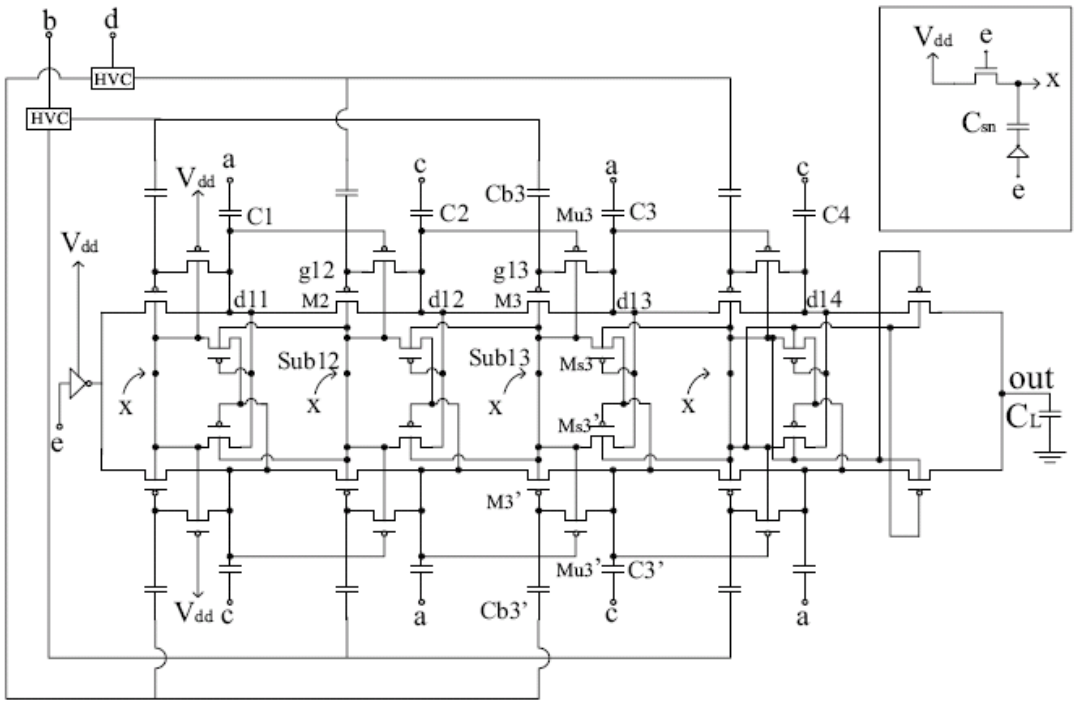


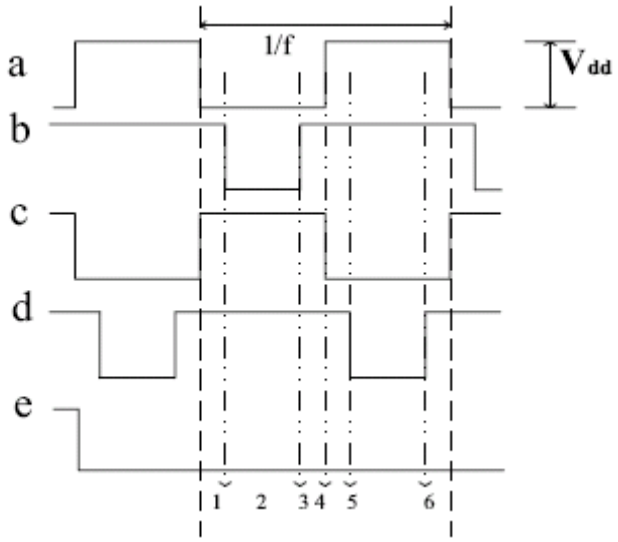
Fig. 4.11 Charge pump circuit with dynamically biasing body node.

4.2.4 Four-Phase Clock Scheme

A charge pump employs special dual branch substrate connection technique to eliminate the body effect and avoid p-n junction forward conduction is shown in Fig. 4.12(a)[30]. The 4-phase clocks from [a] to [d] given in Fig. 4.12(b).



(a)



(b)

Fig. 4.12 (a) Charge pump circuit with four face clock. (b) The four-phase clocks for the charge pump divided into 6 time slots.

Before the charge pump starts to work, an initial setup to prevent from p-n junction forward conduction is attained by precharging the wells of all transistors. The pre-charge procedures are as follows:

1) The node x is charged by an NMOS transistor with the source connected to x and the drain connected to the supply voltage. The substrate capacitor (Cs*n*) holds the voltage level around Vdd-Vtn, where Vth is the threshold voltage of NMOS transistors.
2) The NMOS transistors are turned off using the signal [e]. In the mean time, another node of the substrate capacitor (Cs*n*) is raised from the original ground level to Vdd using inverters. Hence, the wells will hold at least the value of 2Vdd-Vtn.

After that the four phase clocks are applied to the pump, the detailed operations for the upper branch in the third stage with respect to the 6 time slots illustrated in Fig. 4.12(b) are follows:

1) The First time slot: Clock [a] (Low) and clock [c] (High) turn on the substrate transistor (Ms3) which charges the well of the main pass transistors (M3 and M3') to the high potential level. Clock [b] (High) and clock [d] (High) turn off the main pass transistors of the upper and lower branches.
2) The second time slot: Clock [b] (Low) turns on the main pass transistor (M3), so the upper branch performs charge-sharing operation.
3) The third time slot: Clock [b] is high and clock [a] is low. Vgs of the main pass transistor (M3) is higher than Vtp (negative value) to make sure the main pass transistor (M3) to be off before clock [a] goes to high.

4.3 Negative Voltage Generator

The Dickson charge pump also can be used to generate negative voltage as shown in Fig. 4.13. The operation is described below:

In the first half cycle, CLK = high, the node 1 will be discharged to 0. When CLK = low in first cycle, the node 1 will be –VDD and the M1 is turned off state.

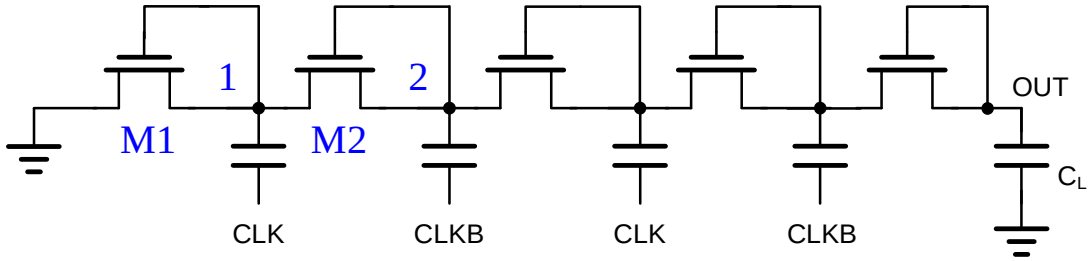


Fig. 4.13 Dickson charge pump generates negative voltage.

In this time, the M2 is turned on and the node 2 will be discharged to 0. When CLK = high in second cycle, the node 2 will be –VDD and node 1 will be 0. When CLK = low in second cycle, the node 2 and node 1 will be -0.5VDD. In the end of third cycle, the node 2 will be -0.75VDD. In the end of next cycle, the node 2 will be -0.875VDD. Thus, the node 2 will vary between –VDD and -2VDD. Then the OUT will be discharged to -4VDD.

4.4 Proposed Charge pump

4.4.1 A Solution of Improving Body Effect of Dickson Charge Pump

We proposed a solution to improve the body effect of Dickson charge pump. The circuit is shown in Fig. 4.14. In the first half cycle, when CLK = 0, the node 1 is charged to VDD-$V_{tn1}(t)$, the $V_{tn1}(t)$ is threshold voltage of MN1:

$$V_{tn1}(t) = V_{t0} + \gamma \left[\sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f} \right]$$
$$= V_{t0} + \gamma \left[\sqrt{(-VDD) + 2\phi_f} - \sqrt{2\phi_f} \right]$$

Thus, the $V_{tn1}(t)$ is smaller than the threshold voltage of NMOS's body connecting to ground. When CLK = VDD in first cycle, the node 1 is 2VDD-$V_{tn1}(t)$. In this time, the threshold voltage of MN1 is $V_{tn1}(t+1)$:

$$V_{tn1}(t+1) = V_{t0} + \gamma \left[\sqrt{V_{sb} + 2\phi_f} - \sqrt{2\phi_f} \right]$$
$$= V_{t0} + \gamma \left[\sqrt{(VDD - V_{tn1}(t)) + 2\phi_f} - \sqrt{2\phi_f} \right]$$

Therefore, the leakage flow from node 1 to VDD is decreased. As the voltage pump up in following stages, the threshold voltage of NMOS in every stage is the same as $V_{tn1}(t)$. So, the problem of body effect is improved.

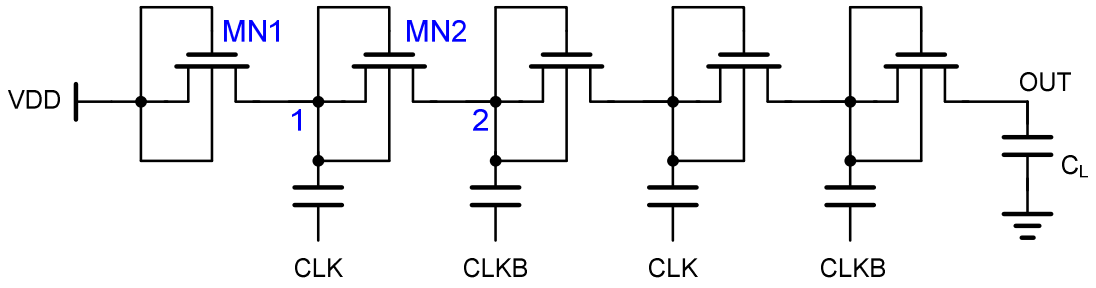


Fig. 4.14 Proposed charge pump.

The comparison of proposed charge pump with previous works is shown in Fig. 4.15 and Fig. 4.16. Charge pumps in this comparison are four stage. The simulation results show that the proposed charge pump has better loading capability and highest power efficiency.

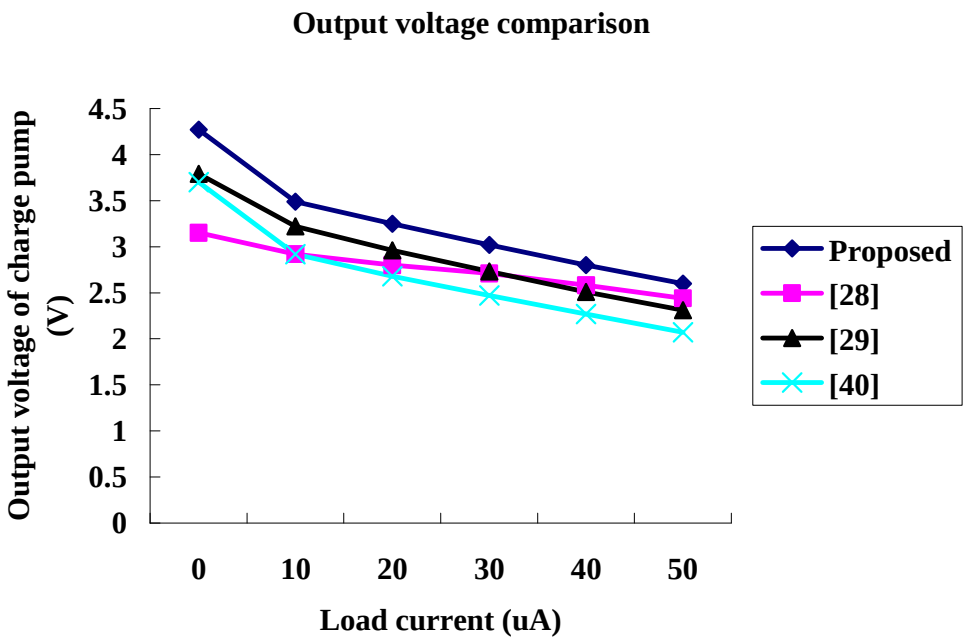


Fig. 4.15 Output voltage of charge pumps in different load current.

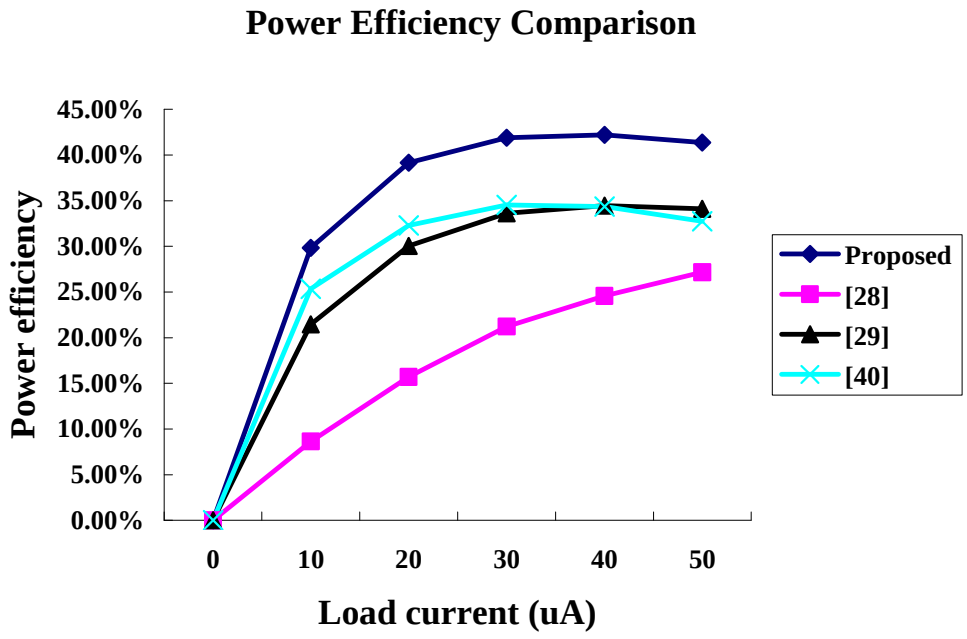


Fig. 4.16 Power efficiency of charge pumps in different load current.

4.4.2 A Novel Connect Scheme of Charge Pump

For flash memory applications, ten times power supply voltage is used. To generate ultra high voltage, the architecture in Fig. 4.17 is used. We can cascade more stage to generate higher voltage. Base on this architecture, we proposed a novel connect scheme for ultra high voltage generating. The proposed architecture is shown in Fig. 4.18.

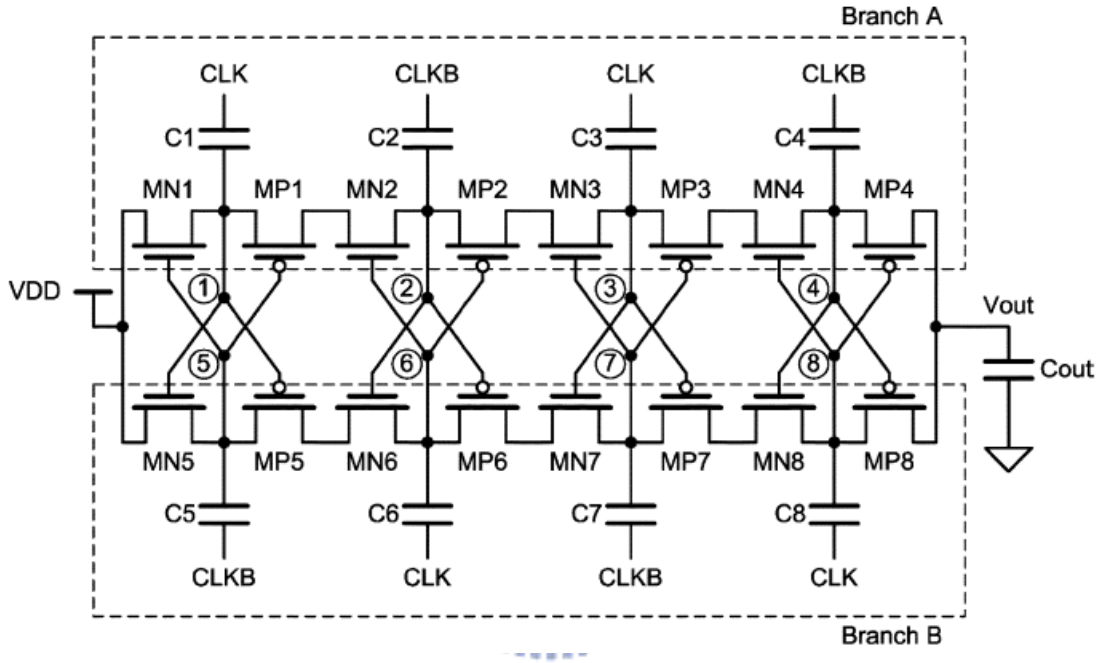


Fig. 4.17 Charge pump generating ultra high voltage.

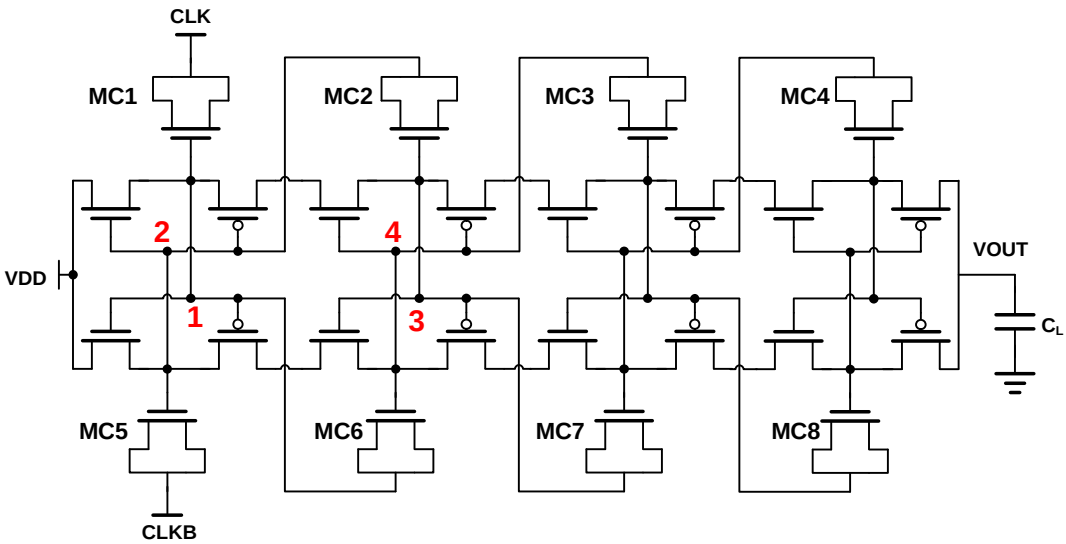


Fig 4.18 Proposed novel connect scheme for generating ultra high voltage.

In Fig. 4.17, we know that node 1 swings between VDD and 2VDD. The node 6 will swing between 2VDD and 3VDD due to the CLK signal swings between 0 and VDD. Base on this concept, we can connect the CLK node of C6 to node 1 due to node 1 swings between VDD and 2VDD. And we can connect the CLKB node of C2 to node 5 due to node 5 swings between 2VDD and VDD. So, the overall architecture is the same as Fig. 4.18. Furthermore, in the proposed architecture, we can use CMOS to replace capacitor. In Fig. 4.17, the maximum cross voltage of C2, C3 and C4 are 2VDD, 3VDD and 4VDD, respectively. And the maximum cross voltage of C6, C7 and C8 are 2VDD, 3VDD and 4VDD, respectively. If we want to use CMOS to replace the capacitor in Fig. 4.17, the special mask is needed to prevent the break down of CMOS. In Fig. 4.18, the maximum cross voltage of MC1 ~ MC8 are VDD Thus, the architecture in Fig. 4.18 can be implemented in standard CMOS process without using special mask to prevent the break down of CMOS.

The comparison of [27] and proposed charge pump is shown in Fig. 4.19 and Fig. 4.20. Note that the size of 1pF capacitor is 33u*33u. The CMOS (MC1~MC8) size using in Fig 4.18 is 30u*30u. [27] 1pF means the capacitor of Fig. 4.17 is 1pF. The simulation results show that the loading capability and power efficiency of proposed charge pump is nearly the [27] 1.5pF and is better than [27] 1pF. The area of proposed charge pump is smallest.

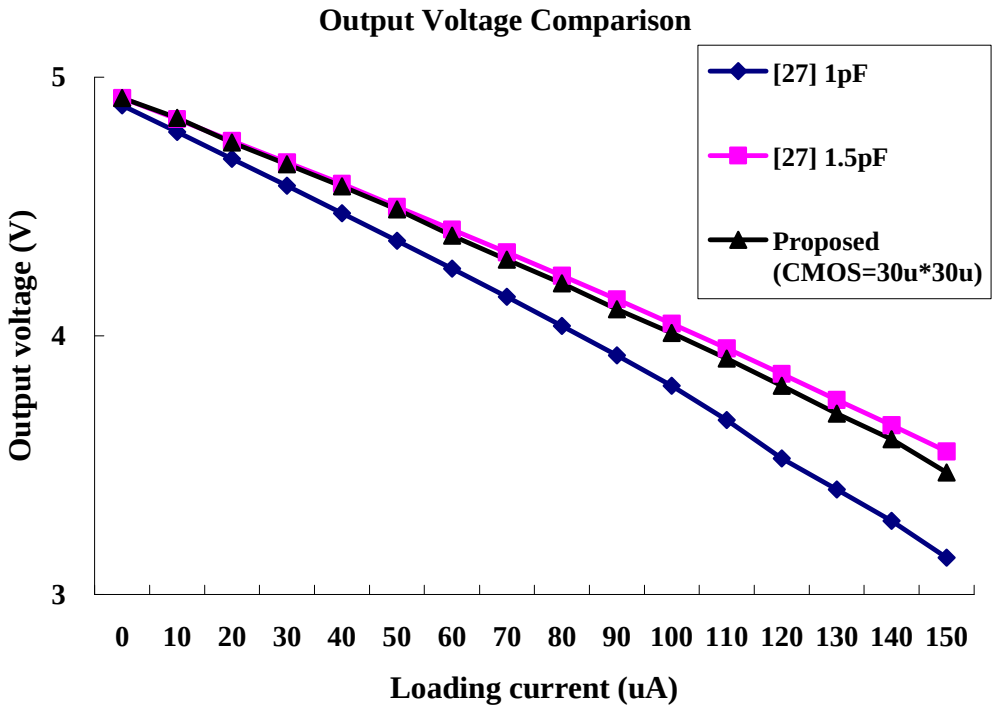


Fig. 4.19 Output voltage of charge pumps in different load current.

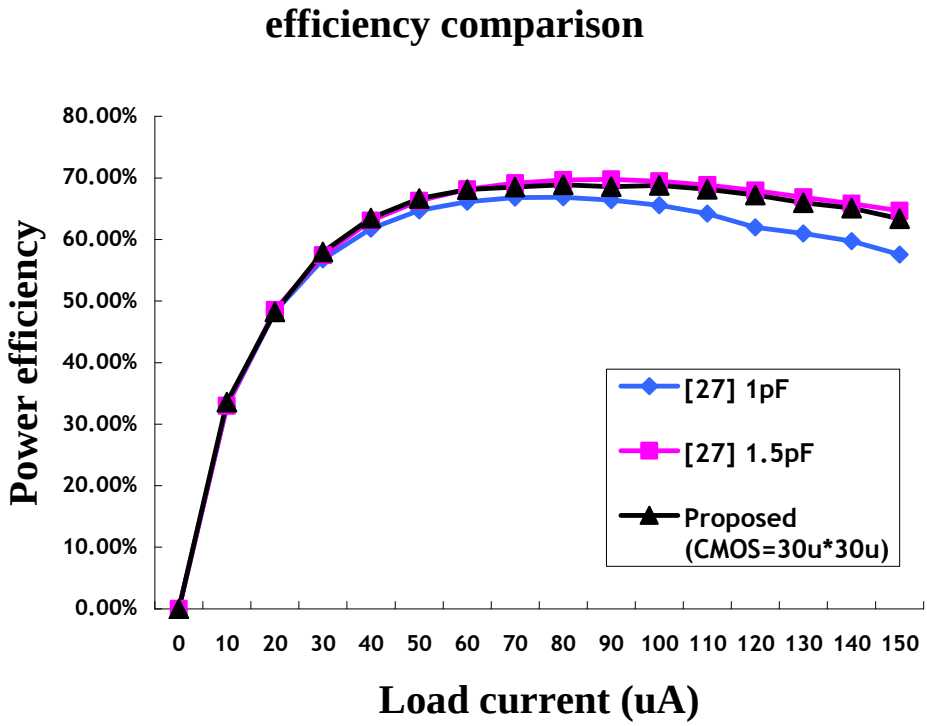


Fig. 4.20 Power efficiency of charge pumps in different load current.

4.5 Summary

In this chapter, the voltage doubler and Dickson charge pump are discussed. The techniques of improving Dickson charge pump's pumping efficiency are introduced. For flash memory applications, ultra high voltage and negative voltage are needed for programming and erasing the information in flash memory. To generate ultra high voltage, the gate oxide reliability is considered. The charge pump design with gate oxide reliability considering is introduced. The negative voltage generator is also introduced.

Finally, we proposed a solution of improving Dickson charge pump's pumping efficiency and a novel connect scheme for generating ultra high voltage. The proposed solution of Dickson charge pump's body effect problem has the better loading capability than [28], [29] and [40]. And it has the highest power efficiency in these four charge pump. The proposed novel connect scheme improved the loading capability and power efficiency of the charge pump. The charge pump with novel connect scheme can be implemented in standard CMOS process without using special mask to prevent the break down of CMOS.

Chapter 5

An Integrated Power Management for Solar Energy Harvesting

An integrated power management system for solar energy harvesting applications is proposed. The PV cell outputs voltage of 0mW~2.3mW and its output voltage is 0mV~840mV. The power management system will output 500mV, 1V and -500mV for computation circuitry and memory circuitry. A power efficiency optimization unit is designed for charge pump. In light loading case, the power efficiency optimization unit outputs low frequency clock to charge pump. This will reduce the power consumption. In heavy loading case, the frequency of clock is increased for keeping the output voltage level of charge pump.

The power management also contains a rechargeable battery. In daytime, the energy of power management system is supplied by photovoltaic (PV) cell and the battery is charged. In the night, the battery will be discharged and supplies energy to the power management system. With proposed control unit, the power consumption decreased 80% compared to system without control unit. The maximum total power efficiency is 69%.

In section 5.1, we will discuss the floorplan of the power management system for solar energy harvesting application. The overview of power management system is shown in Section 5.2. The detail circuitry and the characteristic of PV cell are shown in Section 5.3. The results are simulated in UMC 90nm CMOS technology and are shown in Section 5.4. Finally, we will conclude the power management for solar energy harvesting applications.

5.1 The Floorplan of Power Management System for Solar Energy Harvesting Applications

In this application, we design a power management system that accepts energy from PV cell and outputs 500mV, 1V and - 500mV. The system also contains rechargeable battery. So, there are PV cell, battery, voltage regulator and charge pump in this system. There are several kinds of floorplan in this system.

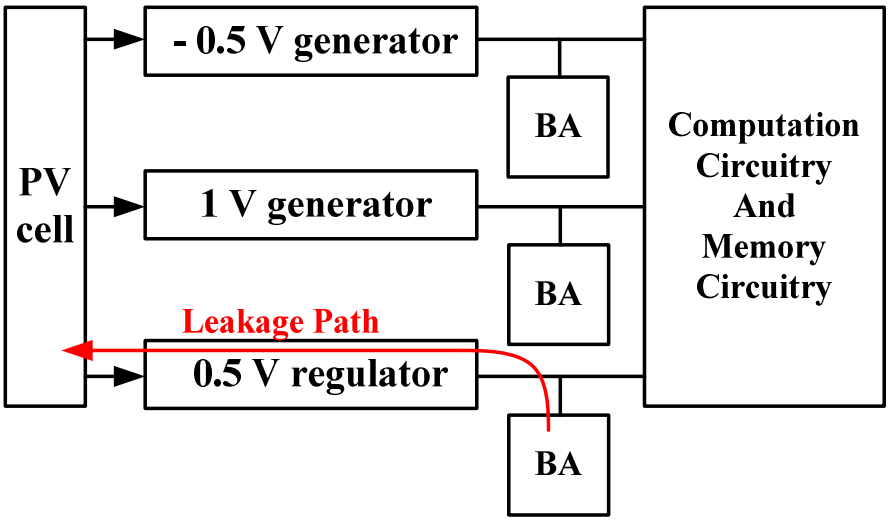


Fig. 5.1 First kind floorplan of power management system.

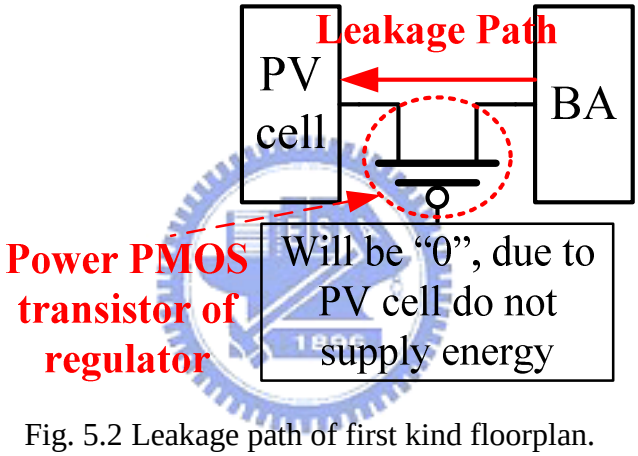


Fig. 5.2 Leakage path of first kind floorplan.

1) First kind floorplan :

The first kind floorplan is shown in Fig. 5.1. The PV cell supplies -0.5V generator, 1V generator and 0.5V regulator. The batteries are placed in the output node of every voltage generator.

Drawbacks :

1. This floorplan needs tree batteries, maybe it will need three output pins.
2. The battery in the output of 0.5V regulator has a serious leakage path. When PV cell do not supply energy, there are current flow from battery to PV cell, as shown in Fig. 5.2. As we want the regulator has low drop out, the size POWER PMOS must be very large. Thus, the leakage will increase. It is complicated to design a control mechanism for decreasing leakage, because the POWER PMOS must be controlled by the signal from op amp to keep the output voltage of regulator the same as Vref.

3. The PV cell variation will affect significantly. The 1V generator and - 0.5V generator are charge pump. If the PV cell varies ΔV, the charge pump will vary 2*ΔV.

2) Second kind floorplan :

The second kind floorplan is shown in Fig. 5.3. The PV cell supplies -0.5V generator, 1V generator. The 0.5V regulator is supplied by 1V generator. The batteries are placed in the output node of -0.5V generator and 1V generator.

Drawbacks :

1. This floorplan needs two batteries, maybe it will need two output pins.
2. Due to the 1V generator is charge pump. The size of capacitor in 1V generator will be large, because it supplies power to 0.5 regulator. If the size of capacitor in 1V generator is not large enough, the loading capability of 1V generator will be poor. Thus, it can not supply a precise 1V. As the size of capacitor increase, the power consumption of charge pump also increase due to the clock charge and discharge the capacitor at every moment.
3. The PV cell variation will affect significantly. The 1V generator and - 0.5V generator are charge pump. If the PV cell varies ΔV, the charge pump will vary 2*ΔV. The output of 0.5V regulator will vary in a lager range.

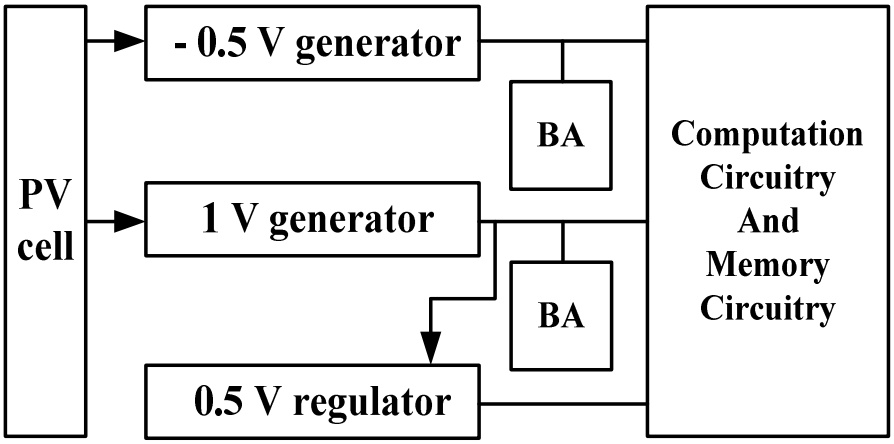


Fig. 5.3 Second kind floorplan of power management system.

3) Third kind floorplan :

The third kind floorplan is shown in Fig. 5.4. The PV cell supplies 0.5V regulator. The 1V generator and - 0.5V generator is supplied by 0.5V regulator. The batteries are placed in the output node of 0.5V regulator. This floor plan needs only one battery and it solve the output variation of 1V generator and – 0.5V generator, because the regulator will regulate the output voltage of PV cell. But it has the same leakage path as shown in Fig. 5.2.

4) Fourth kind floorplan :

The fourth kind floorplan is shown in Fig. 5.5. The PV cell supplies 0.5V regulator. The 1V generator and - 0.5V generator is supplied by 0.5V regulator. The batteries are placed in the output node of PV cell. This floor plan needs only one battery. The variation problem of 1V and - 0.5V generator is solved. Although it has a directly leakage path from battery to PV cell, we can add a control mechanism to decrease the leakage.

Base on above discussion, we decide using the fourth floorplan and add a control unit to decrease the leakage current from battery to PV cell when PV cell don't supply energy.

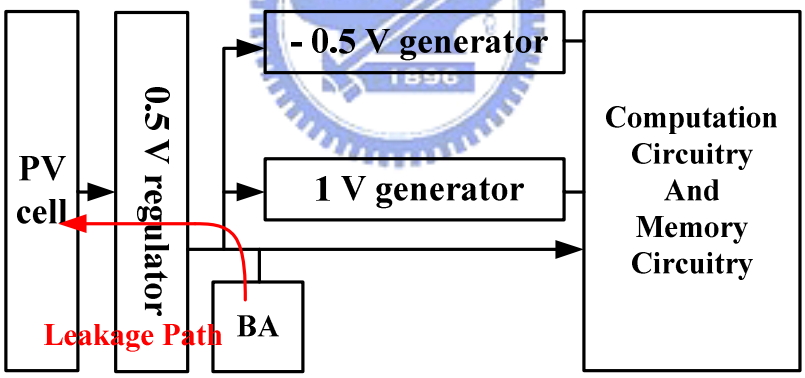


Fig. 5.4 Third kind floorplan of power management system.

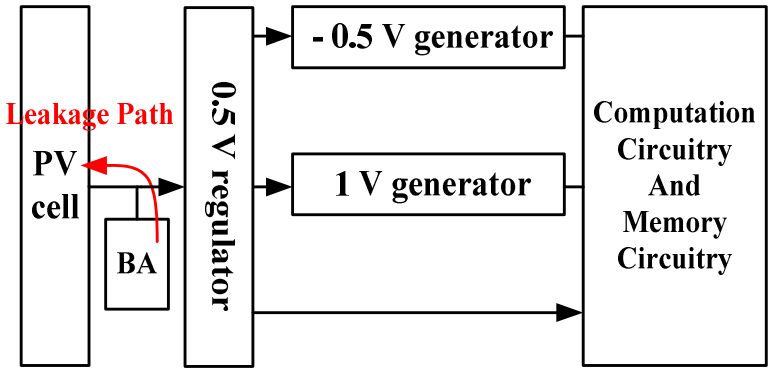


Fig. 5.5 Fourth kind floorplan of power management system.

5.2 The Overview of Power Management System for Solar Energy Harvesting Applications

The proposed power management system for solar energy harvesting applications is shown in Fig. 5.6. The power management system contains a PV cell, control unit, voltage regulator, clock generator, voltage generator, battery charger and rechargeable battery.

The control unit decides who will supply energy to voltage regulator. The voltage regulator outputs 500mV to clock generator, three charge pump and power efficiency optimization unit. The voltage generator and battery charger is composed of charge pump. The voltage regulator, 1V generator and - 0.5V generator will supply three voltage level to computation circuitry and memory circuitry. The power efficiency optimization unit supplies a variable frequency clock to 1V generator. The PV cell and battery are also implemented in circuit model and simulated with power management system.

5.3 PV Characteristic and Detail Circuitry

5.3.1 Photovoltaic (PV) Cell

The I-V curve and P-V curve of PV cell is shown in Fig. 5.7. The black line is I-V curve of output load current and output voltage of PV cell. The output voltage of PV cell is between 840mV and 0mV. The red line shows the P-V curve of output power and output voltage of PV cell. The maximum output power of PV cell is 2.3mW.

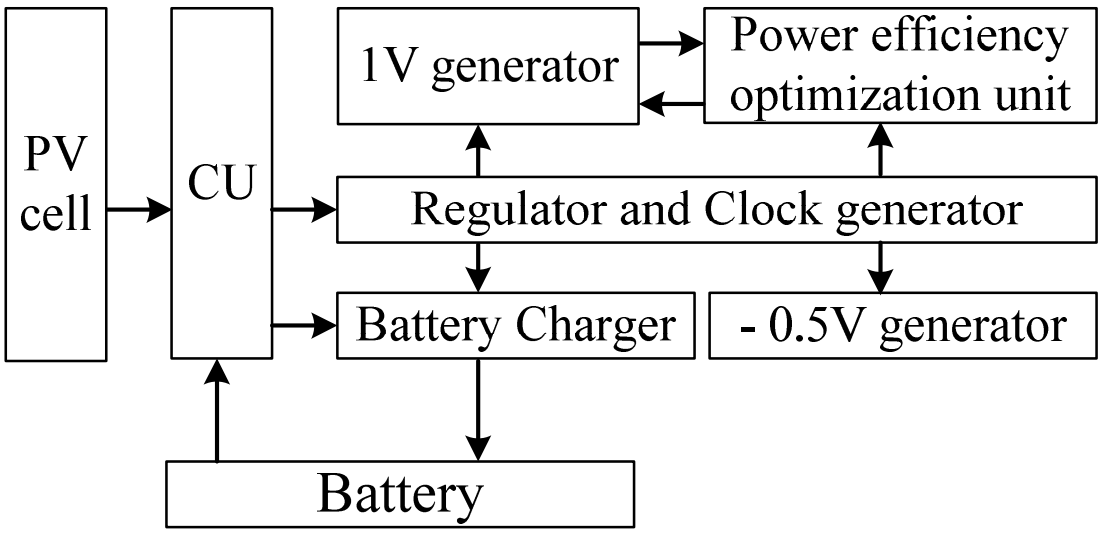


Fig. 5.6 Block diagram of proposed power management.

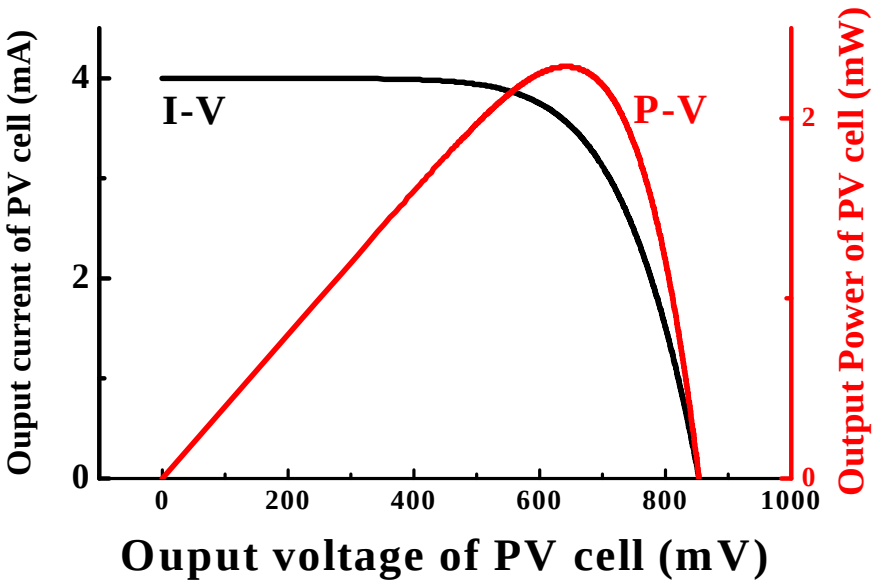


Fig. 5.7 P-V and I-V curve of PV cell. The x-axis is output voltage of PV cell. The left y-axis is load current. The right y-axis is output power.

5.3.2 Control Unit (CU)

Because there are two supply voltage sources of power management, we design a control unit to increase energy utility efficiency of overall system. The schematics of control unit are shown in Fig. 5.8.

When the PV cell supplies energy to voltage regulator, the direction of current flow is from node 1 to node 2. Thus the voltage of node 1 is higher then node 2. The op amp will outputs “1” to inverter and the MP1 will be turned on. In this case, the battery charger is active.

When the battery supplies energy to voltage regulator, the direction of current flow is from node 2 to node 1. Thus the voltage of node 2 is higher then node 1. The op amp will outputs “0” to inverter and the MP1 will be turned off. The MP2 will be turned on and the battery supplies power to voltage regulator. In this case, the control unit will disable the battery charger. With decreasing the current flow back to PV cell and disabling the battery charger, the energy of battery is used efficiently.

Note that the op amp and inverter shown in Fig. 5.4 are supplied by battery. In the beginning, the battery has no energy, so its output voltage is “0”. Thus the inverter will output “0” to turn on the MP1.

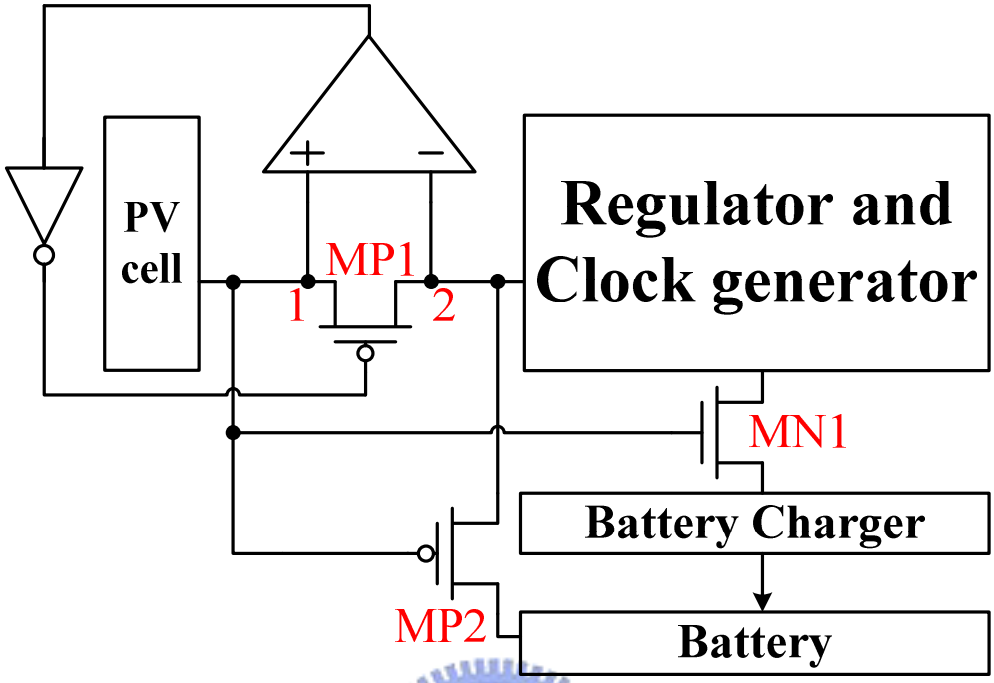


Fig. 5.8 The schematic of control unit (CU).

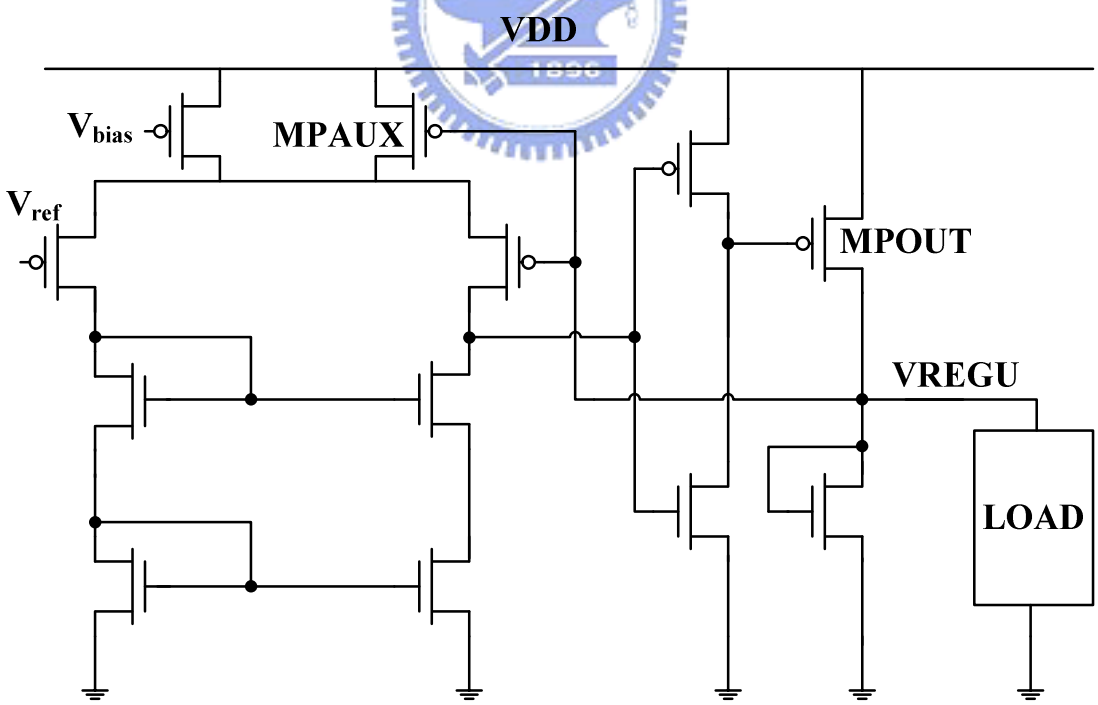


Fig. 5.9 Circuit of voltage regulator.

5.3.3 Voltage Regulator

The voltage regulator is composed of a differential amplifier, an inverter as a buffer and a power PMOS. The schematics of voltage regulator are shown in Fig. 5.9. With the MPAUX PMOS, as voltage of VREGU node dropping down, the MPAUX will supply more current to differential amplifier. Thus, the MPOUT will turn on rapidly and supply more current to VREGU node. When there is no load current, the MPAUX PMOS will slightly turn on and decrease the consumption power of differential amplifier.

5.3.4 Reference Voltage

The reference voltage circuit is shown in Fig. 5.10. The architecture is like Fig. 3.20. We remove the M2 from Fig. 3.20 for the power management system.

5.3.5 Voltage Generator

The power management system outputs tree different voltage level that is 0.5V, 1V and -0.5V. The 0.5V is generated by voltage regulator. The 1V and -0.5V are generated by charge pump.

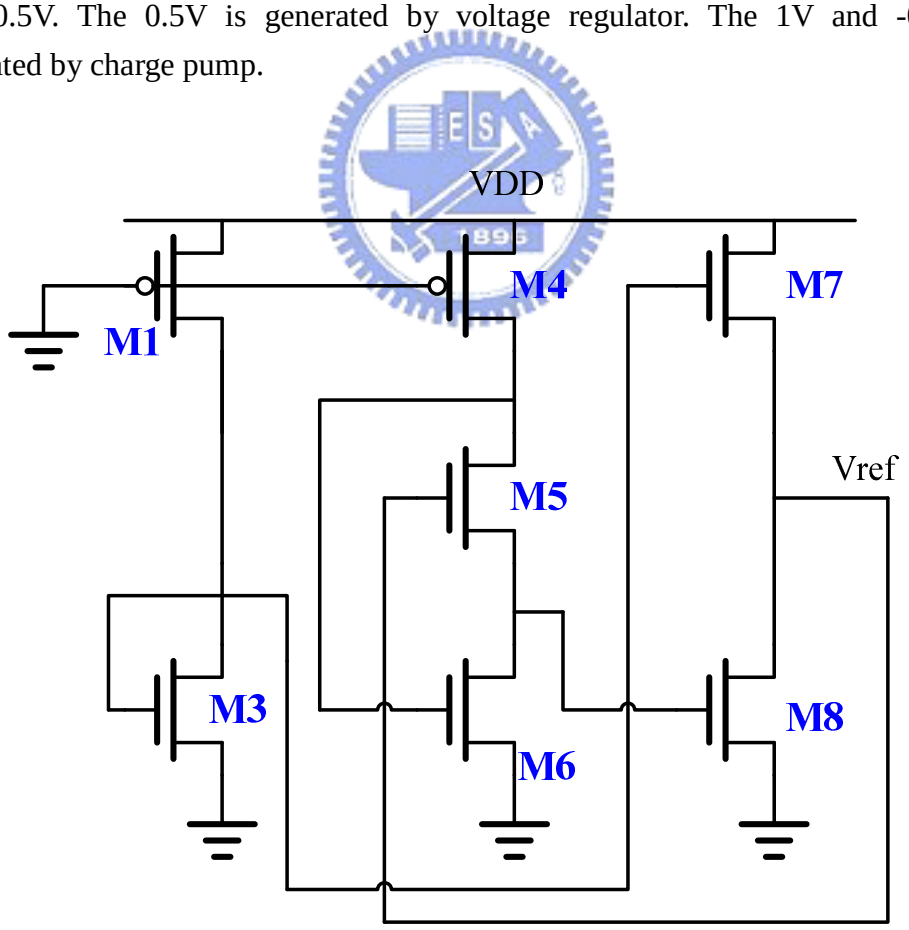
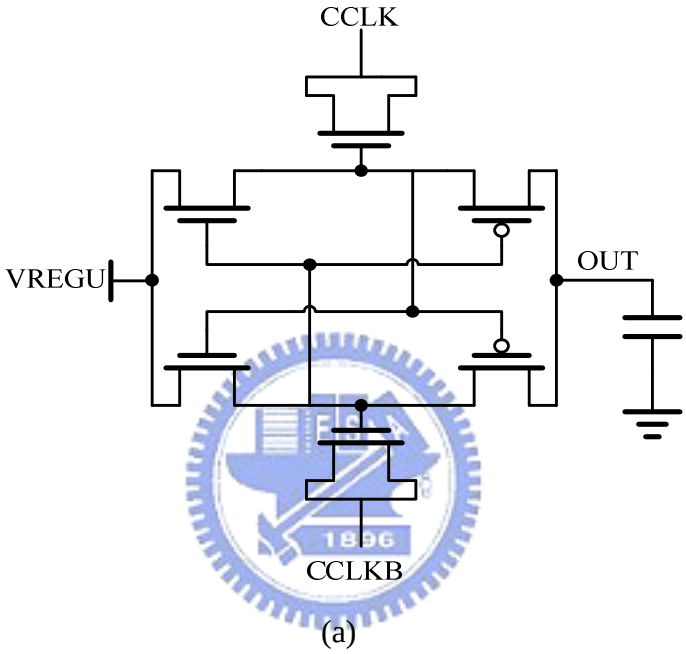
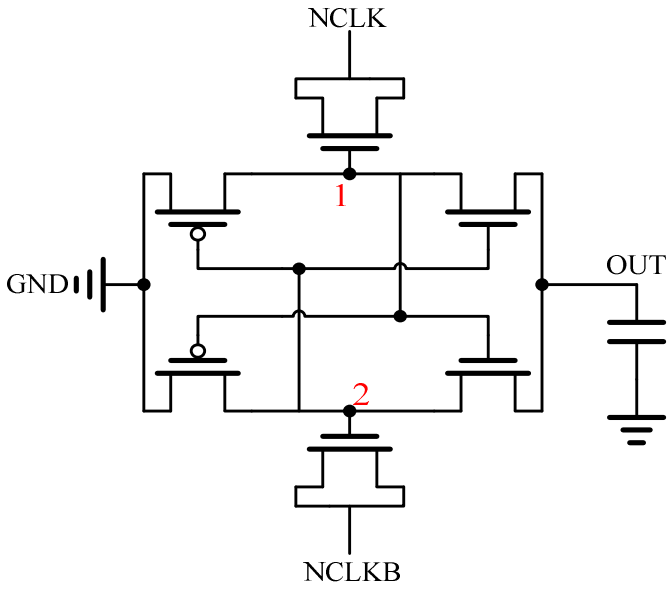


Fig. 5.10 Reference voltage circuit for power management system.

The circuit of 1V generator and -0.5V generator is shown in Fig. 5.11. The CCLK, CCLKB, NCLK and NCLKB are supplied by voltage regulator. The 1V generator is a voltage doubler. It accepts the supply voltage of 0.5V from voltage regulator and output 1V to loading circuit. The negative voltage generator accepts GND as input voltage. When NCLK = 0.5V, the voltage of node 2 is 0V and the voltage of node 1 will be “0”. When NCLK = 0V, the voltage of node 1 will be -0.5V and voltage of node 2 will be discharged to 0V. Then, the output voltage will be -0.5V. When NCLK = 0.5V, the voltage of node 2 will be -0.5V and node 1 is 0V. Thus, the OUT node will be -0.5V.



(a)



(b)

Fig. 5.11 (a) Circuit of voltage doubler. (b) Circuit of negative voltage generator.

5.3.6 Battery Charger

There are three charge pumps in the power management system. These charge pumps are powered by voltage regulator. The schematic of battery charger is shown in Fig. 5.12.

In this work, the clock generator is supplied by voltage regulator. The initial state is that node 1 = 0V and node 2 = 0V.When CLK=0.5V, the node 1 is 0.5V and node 2 is "0.5V-V_{Tn}". When CLKB=0.5V, the node 2 is "1V- V_{Tn}" and the node 1 is 0.5V. As the node CLK is charge to 0.5V again, the node 1 is 1V. In first stage, the node 1 and node 2 will vibrate between 0.5V and 1V. The NMOS capacitors of second stage are connected to node 1 and node 2. Thus the node 3 and node 4 will vibrate between 1V and 1.5V. The node VOUT will be 2.5V.

5.3.7 Clock Generator

The clock system consists of two parts. The constant clock generator which simply generates constant clock is used to supply the battery charger and -0.5V generator. The variable clock generator which changes the clock frequency dynamically is designed to supply 1V generator. It is controlled by the power efficiency optimization unit.

The proposed variable clock generator is shown in Fig. 5.13. It contains basic ring oscillator and insert two transmission gates between the inverters. The frequency of variable clock is controlled by the voltage bias of Vp and Vn. When Vp goes down and Vn goes high, the delay time of transmission gate is short, and the frequency of the clock rise, vice versa. Vp and Vn is biased by the net bias circuit. The variable clock generator achieves wide frequency range and low power. It can provide frequency range from 33MHz to 300MHz. the power consumption is 29uW when operated at 300MHz including the net bias circuit.

5.3.8 Power Efficiency Optimization Unit

The power efficiency optimization unit controls the clock frequency of variable clock generator and optimizes the power efficiency of 1V generator according to the loading condition. The power efficiency unit used voltage detector to detect the loading condition of the 1V generator output. The proposed voltage detector is shown in Fig. 5.14. When the output voltage of 1V generator decrease, vd will increase and it will be compare to the vref. The detecting flag will be sent according to the result of comparison.

If the load current increase and output voltage of 1V generator is below 900mV, the voltage detector will sent the flag signal and the 5-bits counter will count up to speed up the clock frequency of variable clock generator. The high frequency will give more pumping strength to pump the output voltage. If the load current decrease and output voltage of 1V generator is above 900mV, the flag will disable and the clock frequency of variable clock generator will decrease until reach the minimum clock frequency.

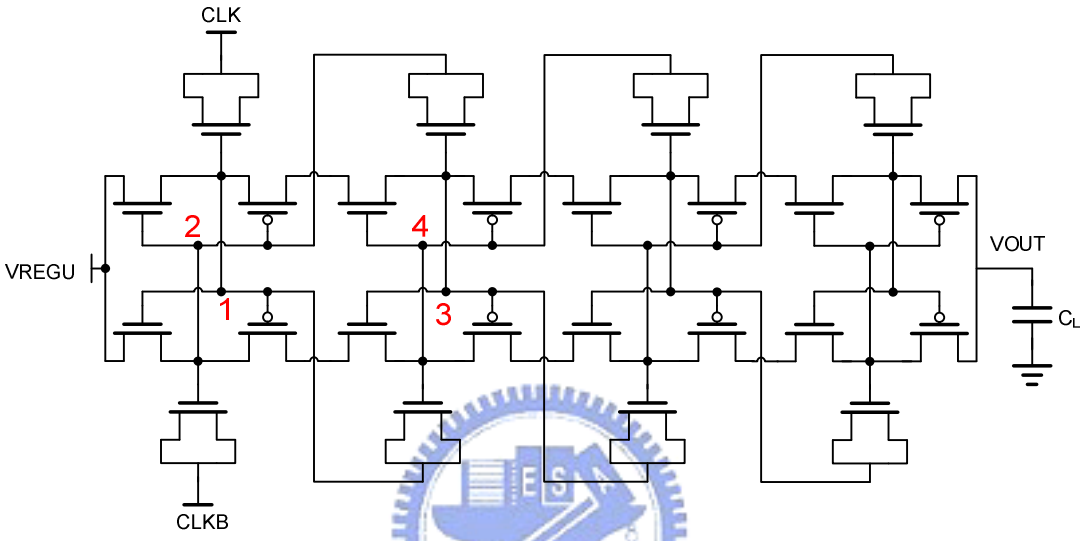


Fig. 5.12 Circuit of battery charger.

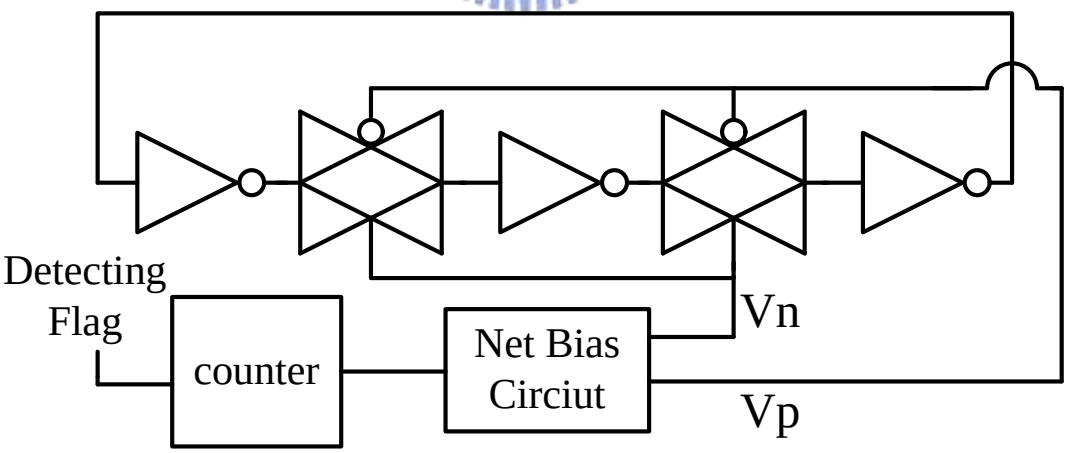


Fig. 5.13 Circuit of variable clock generator.

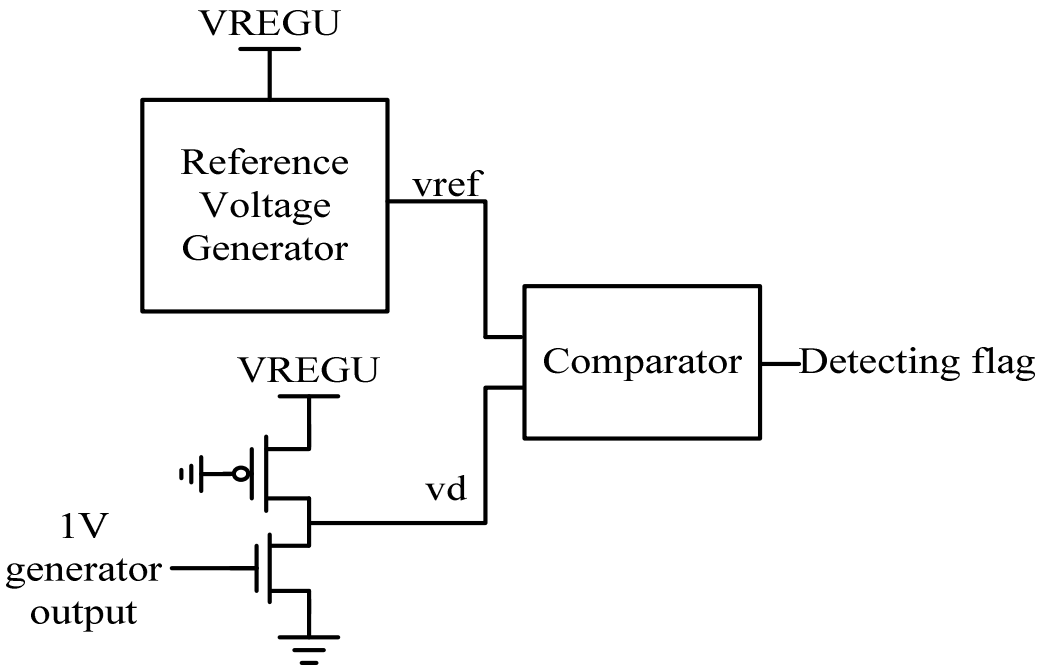


Fig. 5.14 Architecture of voltage detector.

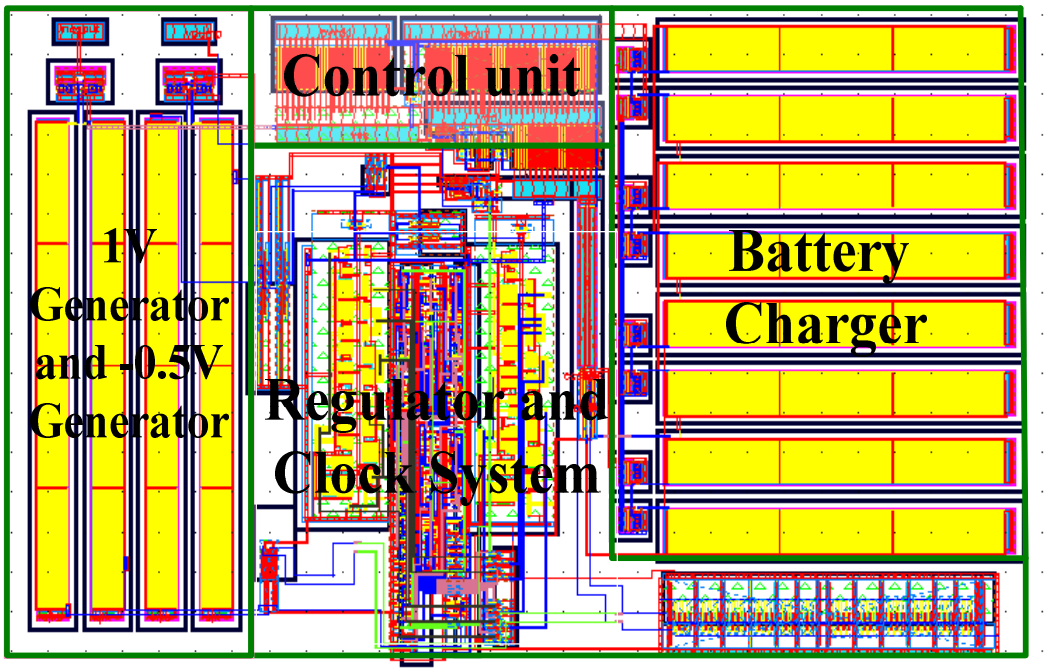


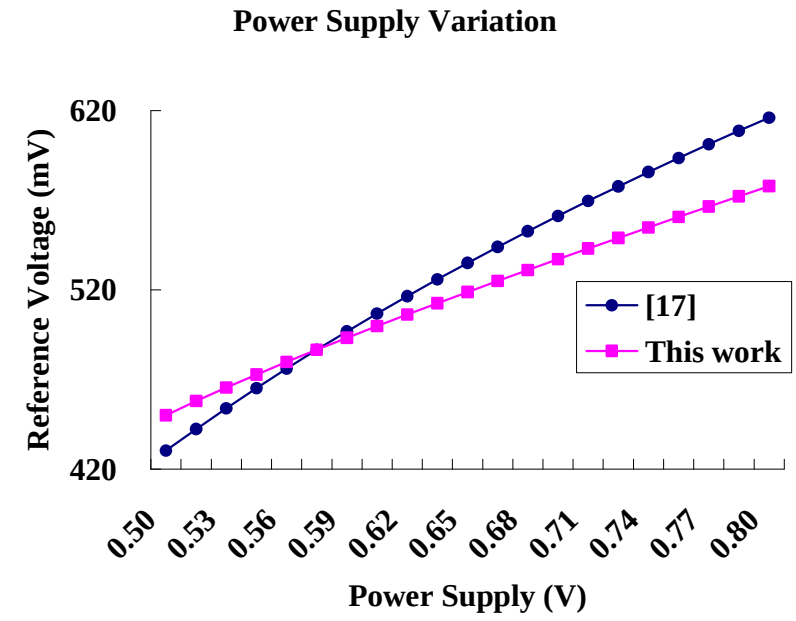
Fig. 5.15 Layout view of power management system for solar energy harvesting applications.

5.4 Simulation Results

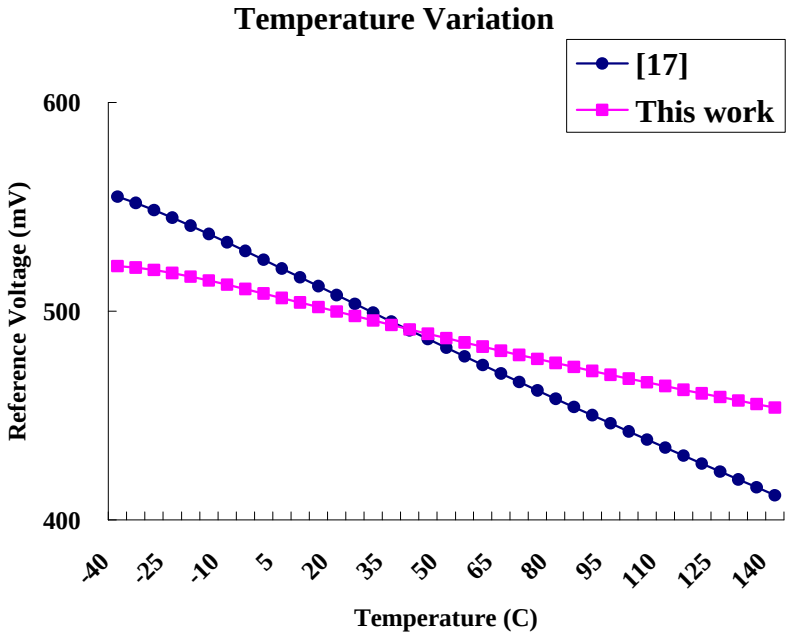
To verify the power management system, the design is implemented in UMC 90nm CMOS technology model. Layout view of the power management system is shown in Fig. 5.15.

5.4.1 Reference Voltage

The comparison of reference voltage compare with [17] is shown in Fig. 5.16. Table 5.1 shows the numerical comparison of these two circuit.



(a)



(b)

Fig. 5.16 Comparison of this work and [17].

Table 5.1 Comparison 500mV generator of [17] and this work.

	[17]	This work
Technology (nm)	**90**	**90**
Output voltage	**500mV**	**500mV**
Supply variation (0.5V~0.8V)	**430mV~616mV**	**450mV~578mV**
ΔVref / ΔVsupply (V/V)	**0.62**	**0.42**
Temperature variation (-40^{o}C~140^{o}C)	**555mV~412mV**	**522mV~454mV**
ΔVref / ΔTemperature (V/^{o}C)	**0.79**	**0.38**
Power consumption	**15uW**	**19.2uW**

5.4.2 PV Variation

In this simulation, the supply current of PV cell is varying from 4mA to 0mA. The result is shown in Fig. 5.17. The PV cell outputs zero current in 10us. The first row is output voltage of PV cell. It varies from 840mV to 177mV. The PV cell drains a little current from battery. The second row is output voltage of voltage regulator. It varies from 592mV to 482mV. The third row is 1V generator. It varies from 1.11V to 0.9V. The fourth row is -0.5V generator. It varies from -547mV to -440mV.

5.4.3 Power Efficiency Optimization

The power efficiency of proposed optimization unit compare to the constant clock supply is shown in Fig. 5.18. It shows the dynamic detection of the power efficiency optimization unit gives better power efficiency performance over the constant clock supply with different load current condition.

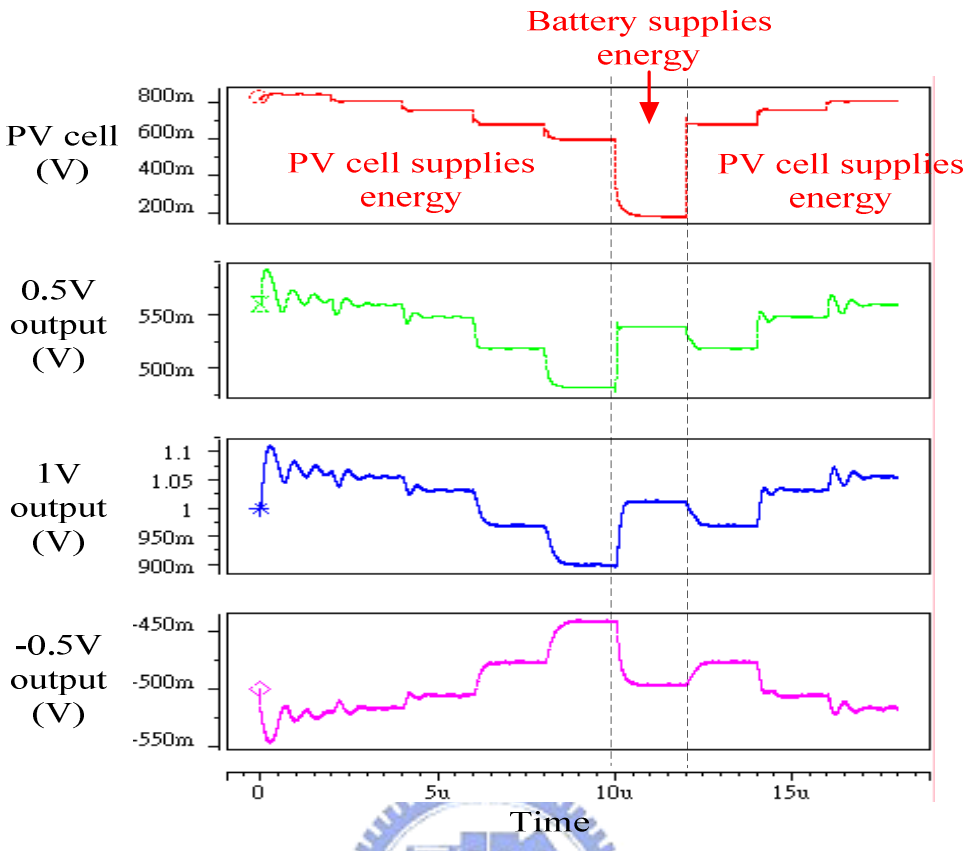


Fig. 5.17 The three different output voltage with variation of current from PV cell.

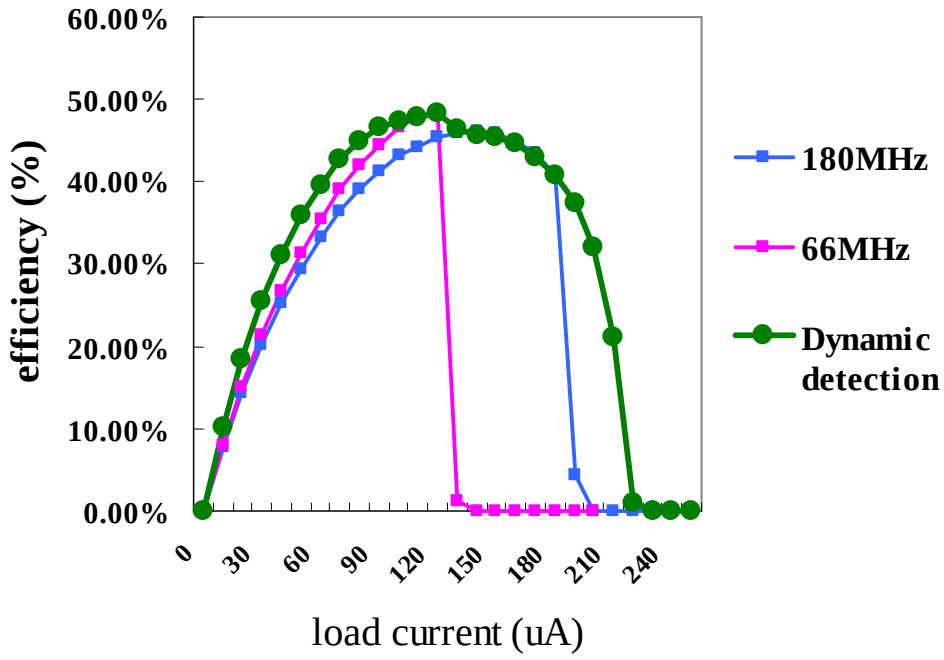


Fig. 5.18 The power efficiency of 1V generator with different load current.

5.4.4 Comparison of System with CU and without CU

The difference of power management system without CU and with CU is shown in Fig. 5.19. In this simulation, the PV cell is set to output zero current and the power management system is supplied by battery.

If the power management system without control unit that is the PV cell is connected to voltage regulator, the output current of battery is 961uA in 30ns. With the control unit, the output current of battery is reduced to 200uA in 30ns.

The simulation result shows that with CU, the power consumption of battery will be reduced 80% compare to power management system without CU. This will increase the using time of battery. The specifications of power management system is summarized in TABLE I.

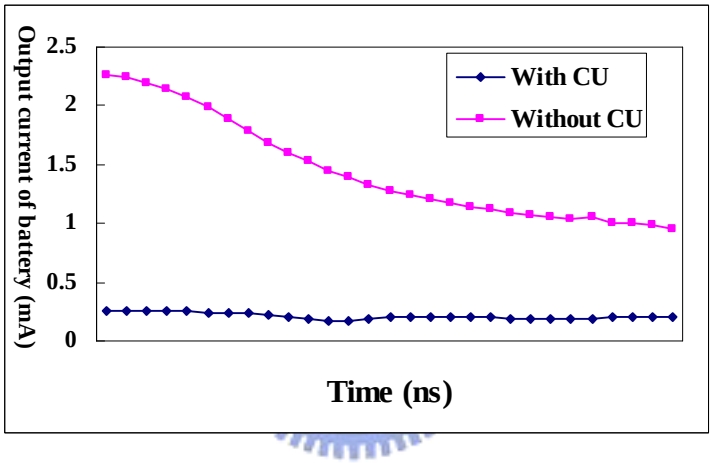


Fig. 5.19 Comparison of power management system with CU and without CU.

Table 5.2 Power management system for solar energy harvesting.

Technology	UMC 90nm CMOS Technology
Output current of PV cell	4mA~0mA
Output voltage of PV cell	840mV~177mV
Output power of PV cell	2.3mW~0mW
0.5V output	592mV~482mV
1V output	1.11V~0.9V
-0.5V output	-547mV~-440mV
Maximum total power efficiency	69%

$$Total\ power\ efficiency = \frac{\left(P_{0.5V\_out} + P_{1V\_out} + |P_{-0.5V\_out}|\right)}{P_{solar\_in}}$$

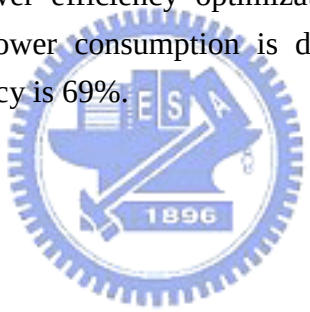
5.5 Summary

An integrated power management system is proposed. The power management system works with PV cell and rechargeable battery. The output current of PV cell varies from 4mA to 0mA and its output voltage varies from 840mV~177mV.

The power management system outputs voltage of 0.5V, 1V and -0.5V to loading circuitry. The 0.5V output is vary from 592mV~482mV. The 1V output is vary from 1.11V~0.9V. The -0.5V output is vary from -547mV~ -440mV.

With power efficiency optimization unit, clock switching frequency of 1V generator is slow in light loading case, thus the power consumption is less than constant high frequency (180MHz) clock. In heavy loading case, the clock switching frequency of 1V generator is fast, thus the loading capability is better than constant low frequency (66MHz) clock. The power efficiency optimization unit is co-design with Chih-Hao Kan.

With control unit and power efficiency optimization unit, the battery supplies energy efficiently and the power consumption is down to one fifth (20%). The maximum total power efficiency is 69%.



Chapter 6
Conclusions and Future Work

In this thesis, we proposed a voltage regulator with 99% current efficiency in Chapter 3. A novel connect scheme of charge pump for generating ultra high voltage is proposed in Chapter 4. In Chapter 5, we proposed an integrated power management for solar energy harvesting applications. The research results of Chapter 3 and Chapter 4 are applied to this power management system. The power management system accepts the power from PV cell and outputs 500mV, -500mV and 1V for computation circuitry and memory circuitry. The power management system also contains a rechargeable battery. Thus, the system can work in day and night. We proposed a power efficiency optimization unit to increase the power efficiency of 1V generator. A control unit is also proposed to prevent the leakage current flow back to PV cell when the PV cell do not supply energy.

Base on the MPPT concept, we can apply the MPPT mechanism to our system, as shown in Fig. 6.1. When PV cell supplies energy, the MPPT will monitor the output voltage of regulator and decide the amount of supply current to battery charger. Thus, the output power of PV cell and output voltage of voltage regulator can be controlled in our desired range.

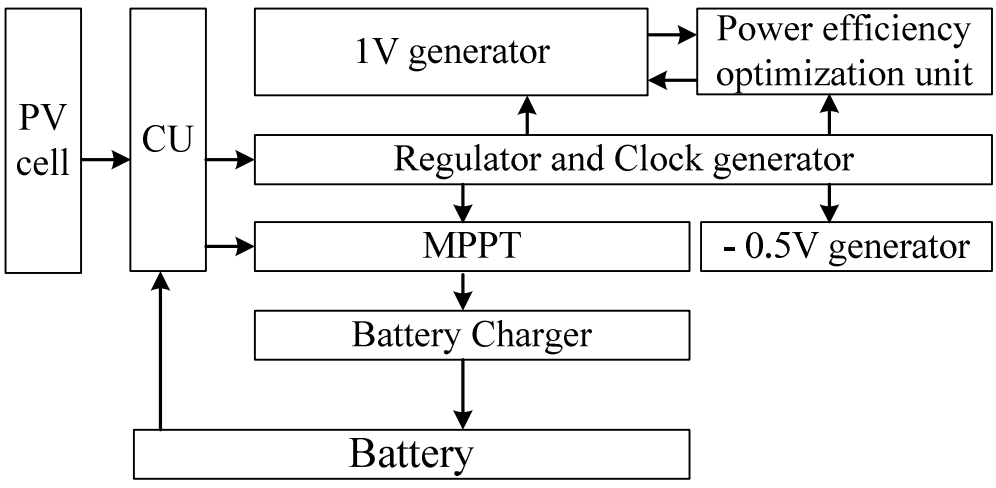


Fig. 6.1 Efficient power management system with MPPT mechanism.

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