一個 4PAM 可操作於 Gbps 具有主動式阻抗匹配的雷射二極體驅動電路

A 4PAM CMOS Laser Driver with Active-back Termination

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一個 4PAM 可操作於 Gbps 具有主動式阻抗匹配的雷射驅動電路

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ABSTRACT (CHINESE)

傳統的雷射驅動電路是採用被動性負載做為阻抗匹配，但是會消耗額外功率在被動性負載上，在這篇論文中，提出利用主動性元件作為負載，來取代被動性負載的雷射驅動電路，除了有作為阻抗匹配的功能之外，相較於傳統採用被動性負載的雷射驅動電路，它能減少傳統的雷射驅動電路功率消耗。雷射二極體其發光的功率大小，是由電流大小來決定，可將雷射二極體輸出光功率代表數位訊號一和數位訊號零，為了能於有限頻寬內傳送更多的資料，於此利用脈衝振幅調變(Pulse Amplitude Modulation, PAM)的方式，將欲傳送的資料先進行調變，將流過雷射二極體的電流振幅劃分成四種不同大小的振幅，其中每種振幅大小分別代表兩個位元的資料，如此可達到總資料傳送量為頻寬的兩倍。編碼上在此使用葛雷碼(Gray Code)，每一等份的振幅變化只改變一個位元，如此一來可降低位元錯誤率(Bit Error Rate, BER)。

在論文中我們所實現的雷射二極體驅動電路以 tsmc018 的製程來完成設計，在 1.8V 的操作電壓下，量測到的資料傳輸速率為 4Gbps；功率消耗約為 200mW；晶片大小為 1600x800μm^2。

A 4PAM Multi-Gbps Laser Diode Driver with Active Back-termination

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ABSTRACT (ENGLISH)

Conventional laser diode drivers adopt passive back-termination as impedance matching; however it consumes additional power on passive load. In this thesis we propose a new active back-termination as termination, besides it consumes less power dissipation compared to conventional laser diode driver. The output optical power of laser diode is determined by the current flows through it. We use the output as representations of digital signals “0” and “1”. In order to deliver more data in limited bandwidth, the pulse amplitude modulation is used. We define four different amplitude optical levels; each signal level represents two bits data information by modulating before transmits. In this way the total data rate is doubled under the same bandwidth. The Gray code is adopted to reduce the bit error rate (BER)

The laser diode driver is fabricated in TSMC 0.18μm process. Under 1.8V, the delivered data rate is about 4Gbps, power consumption is about mW, the die area is 1600x800μm^2.

Acknowledgment

感謝我的指導教授陳巍仁博士，給了我機會加入 307 實驗室這個大家庭，讓我認識了許多好朋友，並帶領我進入類比積體電路的領域。回顧碩士生涯，陳巍仁老師在研究上不時的提點我不足的地方，糾正我錯誤的觀念，給予我寶貴的意見，教導我做研究應該有的態度，並提供許多資源才讓我得以完成這小小的拙作。感謝吳介琮教授、劉深淵教授李泰成教授撥冗答應口試給予指導，不吝意見讓我對自己的不足更為了解。

在研究過程中受到許多 307 學長姊的幫助:金牌台祐大大在電路模擬給許多幫助，一直期盼能回來的建文學長開導我走出低潮，每天早晨看星星的阿傑學長陪我量測到天明，很常一起去吃熱炒，講話詼諧有趣的文哥、小哈棒學長、大家來比黑的正哥，都時常開導我勉勵我好好做研究。總是一人獨自努力的 188 學長，無緣的 Taka 桑，神鵰俠侶松諭大大與巧伶學姐與經長縱慾的 AD 神，都惠我良多，特別感謝 chip 僑仔豪哥，在我研究領域中電路設計與 layout 上，甚至還陪我量測，這些都傳授給我很多專業知識。請我喝過珍奶的神童、非常 nice 的李魚、唱歌好聽的舜哥、風光大葬的忠哥、地產大亨晏維還有常被我吐槽的 Canadian 維德，你們幽默詼諧的言語，讓整個實驗室在嚴肅的研究氣氛仍保有歡樂。

同期一起進來的好伙伴：燁仁，最有禮貌的老木哥，準備出國中的蒙神，常常一起去重訓的喜憨範、魔鬼筋肉鴨，最愛介紹美食的騷邦，520 戰神施小開，雲遊四海征服喜馬拉雅山的逼阿歧，意志力紙紮的陸小小，與你們相處一起打屁出遊，我何其有幸能遇到你們，在人生中記錄這美好難忘的一頁。偉大的 leader 小帆、負隊長昕爺、王牌尾刀宅、丟不準歪一邊的罵己萬謎，謝謝你們在我苦悶時陪我排憂解悶，帶給我歡樂。當助教超嚴格的國維，猛將區文跟我一起熬夜趕下線寫作業，教我 PCB 與量測，渡過沒日沒夜難熬的日子，著實讓我受益良多。講話最有份量，指點我很多人生道理的黑羊，從你身上學到很多東西。鬼才塔哥

跟台中逢甲夜市通丂丂，一起談天說地展望未來趨勢，要是少了你們的陪伴了話，我想我應該撐不下去吧，謝謝大 A 帶我去吃許多美食，在我心情不好時聽我訴苦，口試前還陪我量測到半夜，還把我納入 club 中的一員，真是揪感心乁。

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最後我要感謝我的最愛的家人：爸爸、媽媽、哥哥以及兩個妹妹，我知道我待在家的時間不長，陪在你們身邊的時間很少，但你們總是不遺餘力的提供我所需的一切，容忍我這個不成材兒子的自私無知與沒用，虧欠你們的實在太多，無法讓你們以我為榮。我的受盡委屈的女友姿君總是在身旁默默的守候我，給予我支持與鼓勵，也非常體貼我，很抱歉陪你的時間太少了。謝謝你們因為你們我才能無後顧之憂完成學業。

己丑年秋　吳宗恩

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Introduction

It is evident from the explosive evolution of data traffic and multimedia services over the past several years that sending massive amounts of data around the globe is becoming the next communication paradigm. Millions of end users have become obsessed with sending rich content between one another from wherever they are. Starting with simple text-based e-mails and Web pages, the offered content and services have evolved to encompass high-resolution pictures, high-definition video, voice, music, gaming, e-commerce, and peer-to-peer file sharing. In order to support the applications listed above, optical transport has evolved as the enabling technology for high-bandwidth communications across the board, from interconnects in data centers and massive fiber-to-the-home (FTTH) build-outs over transparent metropolitan and regional optical networks all the way to nationwide long-haul optical backbones and submarine systems spanning the globe. Besides, optical fibers permit transmission over longer distances and at higher bandwidth than other forms of communications. Fibers are used instead of metal wires because signals travel along them with less loss, and they are also immune to electromagnetic inference. Therefore, optical signal seems to be better than electrical signal, while speaks of large data and long distance transmission.

1.1 Motivation

Conventional high speed optical integrated circuits (10-40Gb/s) are implemented in GaAs MESFET, HEMT, InP HBT, SiGe or BiCMOS technologies. However, over the past decades, CMOS technology becomes mature and it is feasible for system integration, including both high frequency analog and high density digital circuits on a single chip. This motivates our research of cost effective optical transceiver in this technology.

Usually there are two commonly used lasers (distributed feedback (DFB) and Fabry-Perot (FP)) adopted in optical network. Those lasers which operate at wavelength 1310nm and 1550nm are more costly and more power consuming. Recent advances in manufacturing have introduced the vertical cavity surface emitting laser (VCSEL) as a low power and low cost alternative for optical applications. The VCSEL operate at wavelength 850nm which is feasible to replace DFB and FP laser in some optical applications. A key element in further cost reduction for these optical applications is the integration of a low-power VCSEL driver circuit with the physical layer IC.

1.1.1Optical links

A backbone network is a part of computer network infrastructure that interconnects various pieces of network, providing a path for the exchange of information between different local area network (LAN). A backbone can tie together diverse networks in the same building, in different buildings in a campus environment,

or over wide areas. Normally, the backbone's capacity is greater than the networks connected to it. A large corporation that has many locations may have a backbone network that ties all of the locations together, for example, if a server cluster needs to be accessed by different departments of a company that are located at different geographical locations. The pieces of the network connections that bring these departments together are often mentioned as network backbone. Figure 1-1 shows a short-haul backbone links, which is usually used in enterprise backbone and the transmission length is less than or equal 20km.

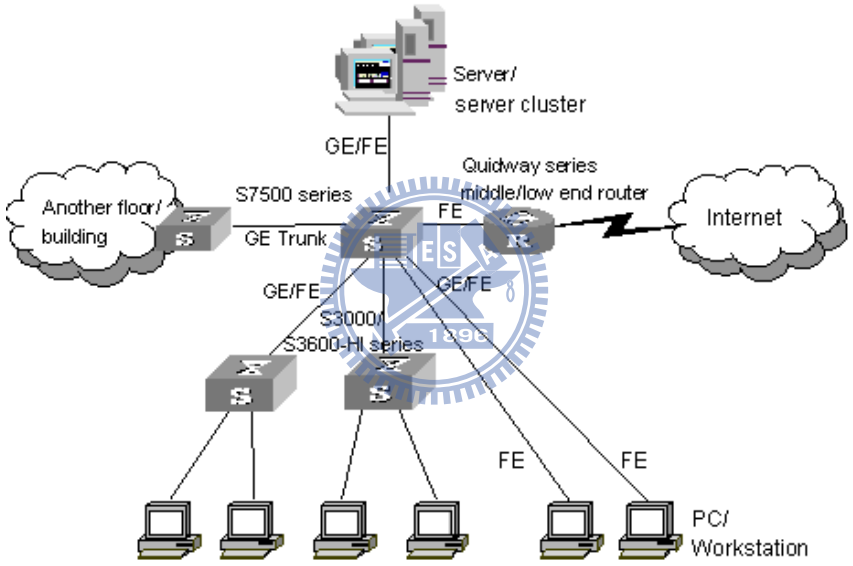


Figure 1-1 Short-haul network

Figure 1-2 shows a genuine optical links, [1], multiplexer transforms parallel digital data into serial bits. Those serial signals drive laser to illuminate through laser driver. For keeping laser's extinction ratio constant, photo diode is used to monitor laser's optical power. Besides, there is another power control loop to adjust laser driver. Thus the output power of laser is kept away from temperature variation and the aging issue of laser itself. At the receiver end, photo diode senses the light and generates current. The transimpedance amplifier (TIA) transforms the current signal

into voltage signal and limiting amplifier (LA) keeps enlarging voltage signal. Also there is a control circuit-auto gain control (AGC) to keep voltage signal amplitude constant.

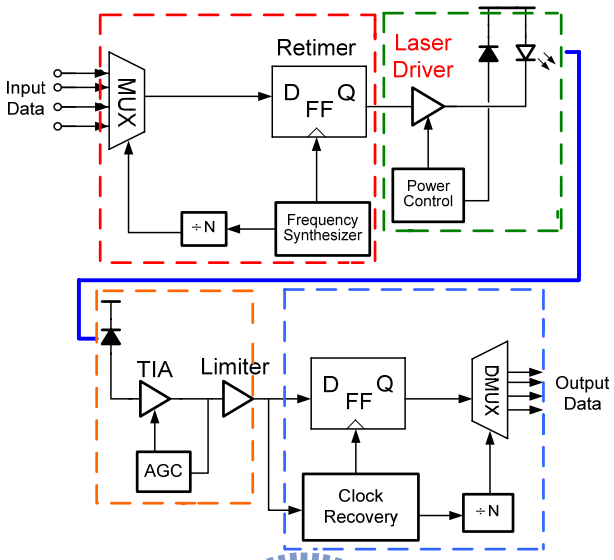


Figure 1-2 Optical transceiver links

1.1.2Integrated CMOS Photonics

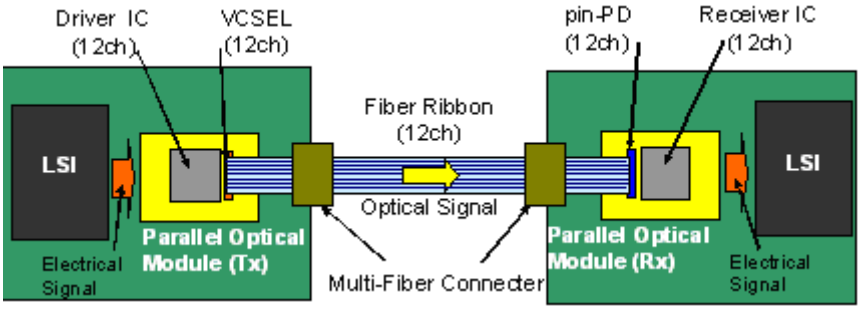


Figure 1-3 Optical interconnection of chip to chip

Recent developments in the microprocessor industry have indicated the end or the uni-processor design and the emergence of multi-processor architectures. Chip

designers have reached the limit of instructive-level parallelism that can be exploited with better pipeline design, as well as the improvements from clock scaling due to packaging and technology constraints.

Typically modern day on-chip interconnection networks are implemented as electronic packet switched topologies. In some multi-core architectures, the network accounts for over 50% of the total power consumption of the chip. This proportion will be exacerbated as workload demand on these on-chip networks can be traced off the limited peripheral area, which results in a large mismatch in on- and off-chip bandwidth. In order to alleviate these issues of power and bandwidth, one proposed solution is the use of photonic interconnection network.

In Figure 1-3 shows an optical interconnection between two chips. With the photonics to the chip-level can potentially bring increased bandwidth, reduce latency, and improved power efficiency. The main advantage of on-chip photonics lies in the decoupling of distance with power consumption. For chip-scale distance, signals can be modulated once and carried completely to their destination regardless of how far away it is. Conversely, electronics requires buffering every few millimeters, which consumes more power as data travels further. In addition to this key advantage for on-chip communications, photonics brings the added advantage that this concept also applies for chip IO, while maintaining the same bandwidth delivered on-chip. Speed of light in silicon end-to-end propagation can also yield significant improvements in latency. Because optics is not constrained to the common electrical restrictions that prevent high signaling rates across interfaces, it effectively solves the bandwidth mismatch.

Besides the limitation of bandwidth in electronic interconnection, the high density electronic interconnection may suffer from severe cross talk and electro-magnetic interference (EMI). Optical signals, of course, are not affected by

EMI, or other forms of electronic noise. Thus, the use of optical links for communication between multi-chip modules has great value in removing some interconnection bottleneck for data flow in systems.

1.2 Organization

This thesis consists of five chapters. The first chapter describes the motivation of this work and thesis organization. In the second chapter, since our objective is to design a laser diode driver, we illustrate some terms often mentioned when design a laser driver, besides, we also point out the drawback of conventional laser diode drive and review some proposed active back-termination.

In the third chapter, we make a brief of pulse amplitude modulation (PAM) which is adopted in the thesis, and the proposed 4-PAM laser driver architecture. And the circuit details that realize the proposed architecture are also presented in order, in the third chapter. In the fourth chapter, experimental results including chip photo, testing environment and measured eye-diagrams are shown. Finally, the last chapter, we make a conclusion of our work and discuss the future work.

Chpater2

VCSEL Characteristic and Laser Driver

2.1 VCSEL Characteristics

2.1.1 VCSEL Structure

The VCSEL is a type of semiconductor laser diode and emits the light per-pendicular from the wafer top surface rather than at the edges of the chip (parallel to the wafer surface), as the Fabry-Perot (FP) or distributed-feedback (DFB) lasers do. The VCSEL consists of a gain medium located in a very short vertical cavity with Bragg mirrors at the bottom and the top as shown in Figure 2-1 the Bragg mirrors are formed by many layers of alternating high and low refractive-index material. Each layer has a thickness of a quarter of the laser wavelength in the material, yielding intensity reflectivities above 99%.Because of the short cavity length, high reflectivity mirrors are required in VCSEL to balance the short axial length of the gain region.

In common VCSEL the upper and lower mirrors are doped as p-type and n-type materials, forming a diode junction. In more complex structures, the p-type and n-type regions may be buried between the mirrors, requiring a more complex semiconductor process to make electrical contact to the active region, but eliminating electrical

power loss in the DBR structure.

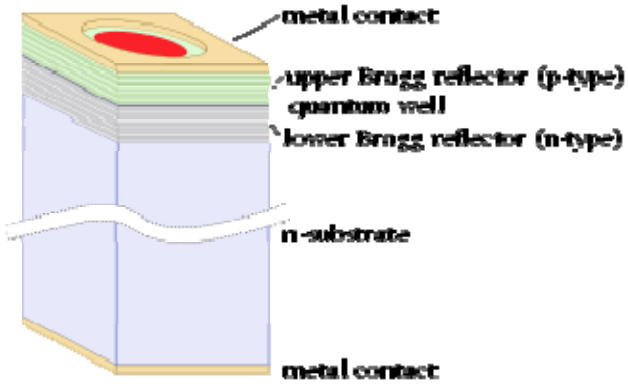


Figure 2-1 Cross section of VCSEL

There are several advantages to producing VCSEL when compared with the production process of edge-emitting lasers. Edge-emitters cannot be tested until the end of the production process. If the edge-emitter does not work, whether due to bad contacts or poor material growth quality, the production time and the processing materials have been wasted. VCSEL however, can be tested at several stages throughout the process to check for material quality and processing issues. For instance, if the vias have not been completely cleared of dielectric material during etching, an interim testing process will flag that the top metal layer is not making contact to the initial metal layer. Additionally, because VCSEL emits the beam perpendicular to the active region of the laser as opposed to parallel as with an edge emitter, tens of thousands of VCSELs can be processed simultaneously on a three inch Gallium Arsenide (GaAs) wafer. Furthermore, even though the VCSEL production process is more labor and material intensive, the yield can be controlled to

a more predictable outcome. Therefore, we can conclude the following advantages of VCSEL.

(1) The structure can be integrated in two-dimensional array configuration.

(2) Circular and low divergence output beams eliminate the need for corrective optics.

(3) Low threshold currents enable high-density arrays.

(4) Low-cost potential because the devices are completed and tested at the wafer level.

(5) Lower temperature-sensitivity compared to edge-emitting laser diodes.

(6) High transmission speed with low power consumption.

2.1.2 I/V Characteristics of VCSEL

From an electrical point of view, the semiconductor laser is a forward-biased diode. The relationship between the laser current, I_L, and the forward-biased drop, V_L, is described by the so-called I/V curve. Figure 2-2 shows an I/V curve of a laser. For such a laser, the small signal resistance is one over the I/V curve slope, whereas the forward-voltage drop is about 1V. Both of characteristics depend on the current, temperature, age, and band-gap of the semiconductor materials used.

A simple large-signal AC model for the VCSEL is shown in Figure 2-3 It consists of a resistance, forward-voltage and parasitic capacitor. The capacitor models the junction and diffusion capacitance of the forward-biased p-n junction and typical is fairly large, especially when compared with the capacitance of a corresponding photodiode. Compared with edge-emitter lasers, the VCSELs tend to have a large resistance and a smaller junction capacitance. To model a packaged laser, additional

elements, such as the bond-wire inductance, must be added to the equivalent circuit in Figure 2-3.

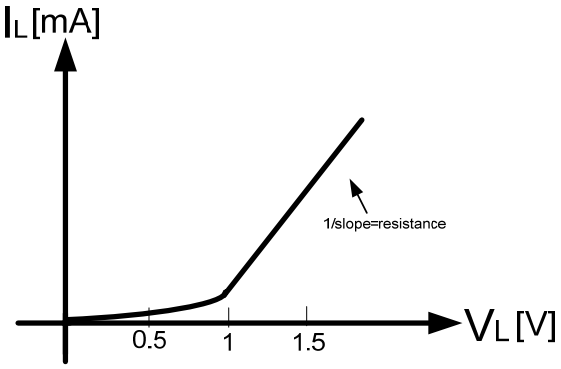


Figure 2-2 I/V curve of VCSEL

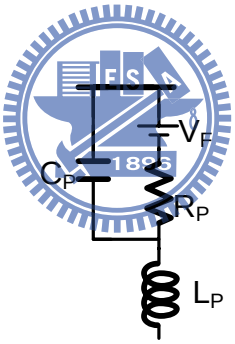


Figure 2-3 Small signal model of VCSEL

2.1.3 P/I Characteristic of VCSEL

The static relationship between the laser current, I_L, and the light output, P_{out}, is described by the so-called P/I curve. Figure 2-4 illustrates such a P/I curve. In the following, we define some terms shown in the P/I curve of the laser.

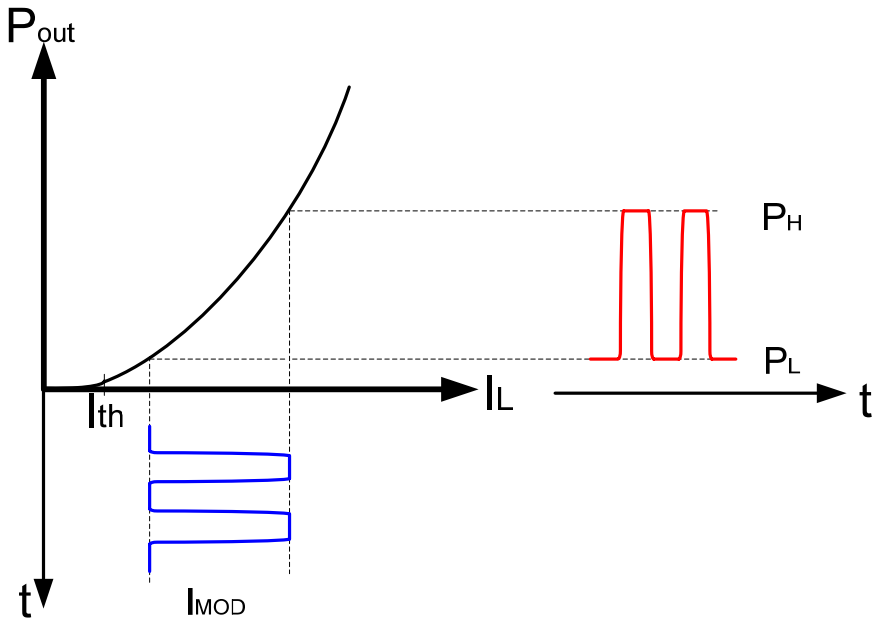


Figure 2-4 P/I curve of VCSEL

(1) Threshold current.

Threshold current is the minimum current that laser outputs only a small amount of incoherent light. In the regime, the net optical gain isn't large enough to sustain lasing, thus only spontaneous emission is produced.

(2) Biasing current.

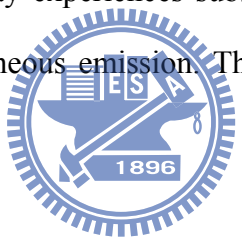
Since laser essentially is a diode, it must encounter the turn on delay issue while it turns on. The way to relax the problem is by providing a dc current such that laser is already turned on. The dc current is the so-called biasing current which is usually large than threshold current. By adding biasing current, it also reduces the turn on delay jitter, the amplitude of the relaxation oscillations and the optical chirp.

(3) Modulation current

The output optical power of lasers is determined by the current flows through itself. Therefore, we can define the data type by providing an ac current. The ac current is the so-called modulation current. Usually the high and low output laser power represent data “high” and “low” respectively.

(4) Turn on delay

When a laser diode is turned on, the photon generation begins as spontaneous emission until the carrier exceeds a threshold level. Thus, stimulated emission occurs after some delay. If the laser current begins from below the threshold current, then the turn on delay experiences substantial random variations due to the random nature of spontaneous emission. Thus, the optical data suffers from jitter.



(5) Relaxation Oscillation

When the laser current changes from a small value (below the threshold current) to a large value, the laser output power does not vary in the form of a simple step. Depicted in Figure 2-5, the output time-domain waveform suffers from “ringing”, requiring some time to settle. This effect is so-called relaxation oscillation.

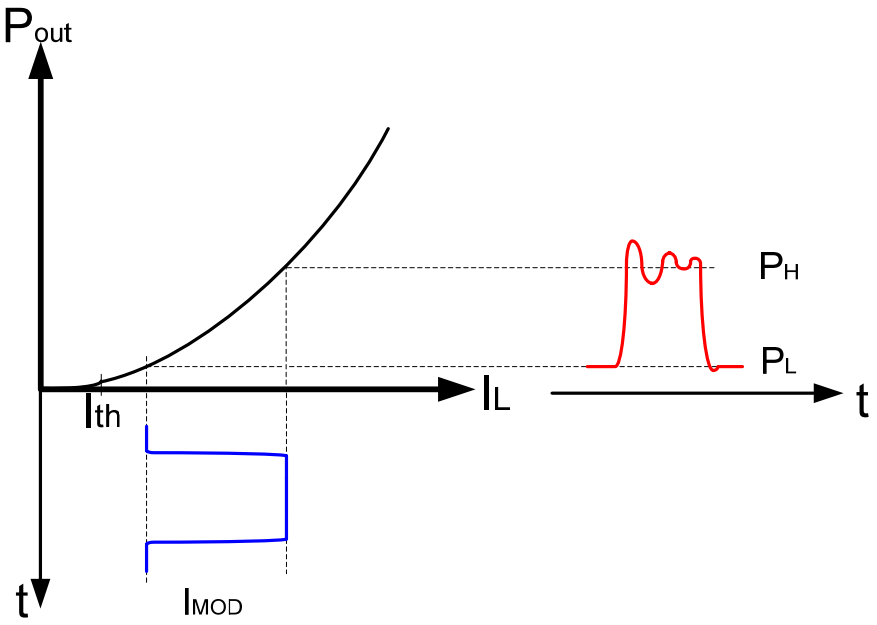


Figure 2-5 Optical relaxation of VCSEL

2.1.4 Temperature Effect to Laser

The optical power of VCSEL is determined by the current. From Figure 2-4, we see the relationship between power and current, however the ambient temperature around the VCSEL affects the P/I curve seriously. As shown in Figure 2-6, as the temperature increases the power efficiency gets worse. It is obviously that the same current flows through VCSEL, the less optical power emits. Unfortunately, the unwanted drawback is inherent and inevitable in the applications of VCSEL. Such that the extinction ratio and the signal fidelity degrades when the VCSEL experiences a temperature change. To solve this issue, many studies focus on using a photo diode and an automatic power control circuits to adjust the VCSEL power. In this thesis we do not focus on discussing the solutions.

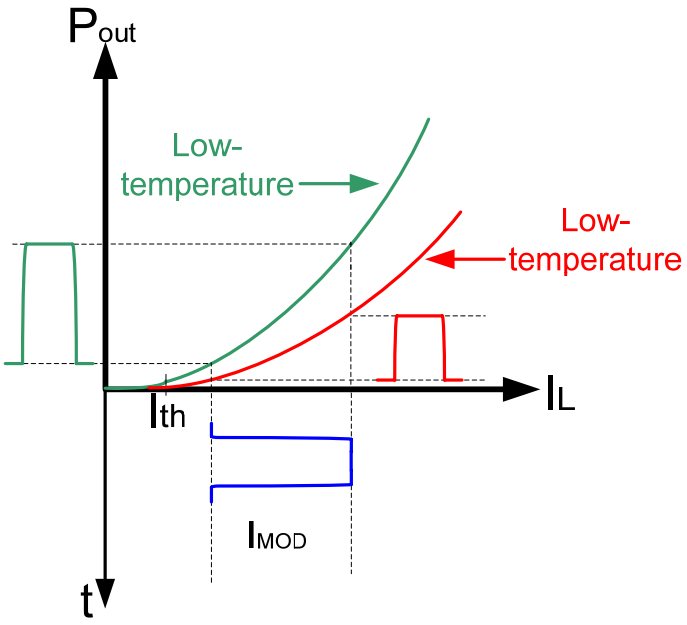


Figure 2-6 P/I curve of VCSEL with different temperature

2.2 Laser Driver

The race for higher and low power consumption in cheaper communication ICs does not appear to ever abate. This is particularly true for the circuits at the interface of optical communication systems, where it is desirable to exploit the full data rate allowed by optical fibers as much as possible while still ensuring manageable power dissipation.

A laser-diode driver requires output transmission-line back termination that absorbs signal reflection from the imperfectly terminated load, especially when a low-cost laser diode is used to build a high-speed optical transmitter. Otherwise, it may lead to degraded waveform fidelity and reduced eye-mask margin. Conventional laser-diode driver implement the passive back-termination with on-chip resistors due to its simplicity. However the passive termination resistor inevitably becomes an additional load for the output driver, which results in significant decrease of the modulation current range. To overcome the reduced modulation current range, various design topologies of active back-termination have been proposed and successfully demonstrated for laser diode drivers fabricated in GaAs or SiGe bipolar process in the past few years. The following two sections will discuss the drawback of the conventional laser-diode driver and review the proposed active back-termination configuration so far.

2.2.1 Back-Termination

When using a transmission line to connect the driver to the load, undesirable reflections may occur at its ends. To avoid reflections from the load end of the

transmission line back into the driver, the laser must be matched to the characteristic impedance of the transmission line. The following part of this section we will discuss different kinds of impedance matching configuration.

Open Drain

Figure 2-7 shows the current switch of output stage and the laser load is driven through a transmission line. If the load impedance matches the characteristic impedance of the transmission line exactly this arrangement works very well. However, if there is a mismatch, a reflected wave is generated at the load propagating back into the driver. This may occur, for example, in the case of an electro-absorption modulator (EAM) load, where laser load is bias dependent and cannot match the line impedance under all conditions. Furthermore, at high frequencies the EAM load is capacitive, resulting in a mismatch to the real line impedance. Now, when the reflected wave arrives back at the driver, it sees a high impedance (an open) and consequently is reflected again (nearly untenanted) forward into the load. Theses undesirable double reflections may degrade the driver's extinction ratio and jitter performance. A driver stage that is unable to absorb reflections coming back form the load is known as an open drain stage. In general, such a stage can be used only if a good matching at the load end is guaranteed.

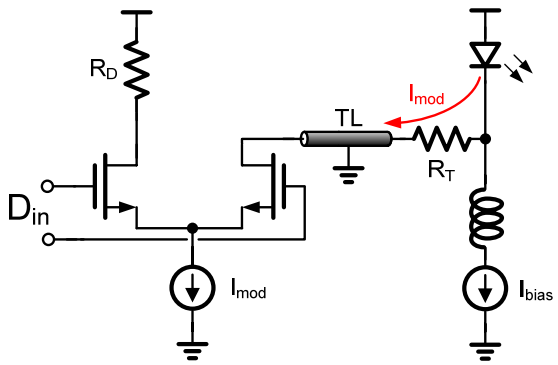


Figure 2-7 Output stage without back-termination

Passive back-termination

The problem of double reflections can be resolved by incorporating a back-termination into the drivers. A simple way to realize this is shown in Figure 2-8, where the conventional laser driver output stage with resistive load, matching the characteristic impedance of the transmission line has been added to the output stage. Now, any wave that may come back because of a load mismatch is absorbed by this resistor, thus preventing a second reflection into the load. However, the price to pay for this feature is a doubling of the modulation current. In Figure 2-8, assume we want to illuminate the laser by providing current I_{mod} and the resistance of the resistive load, R_M, is equivalent to the driven load, thus the current source of the output stage needs 2 I_{mod}.

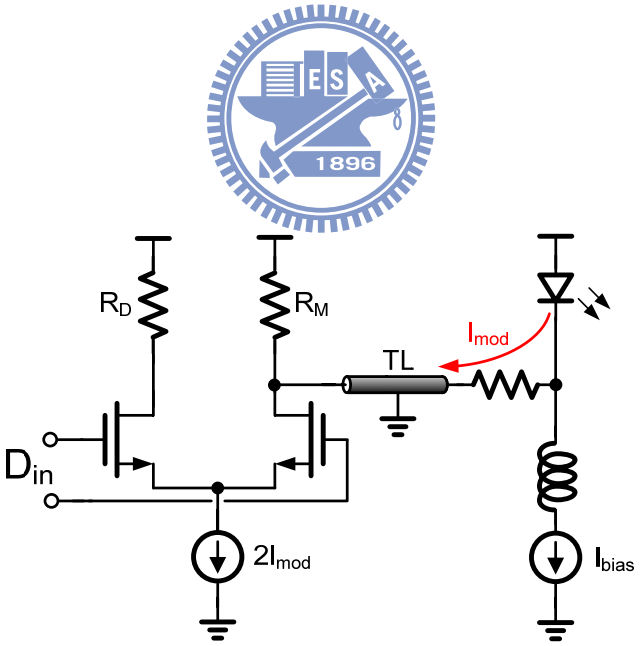


Figure 2-8 Output stage with passive back-termination

Active back-termination

A method to protect against double reflections without wasting too much power is given by the so-called active back-termination. Figure 2-9 shows a same schematic, but the active device replaces the resistive load instead. In this case, the current source of the output stage is less than passive back-termination one, with the use of active device. It is obviously that the output stage with active device consumes less power than conventional one. Besides, the resistive load termination leads to other drawbacks: less laser modulation current range and voltage compliance. The next section we review some published active load circuits.

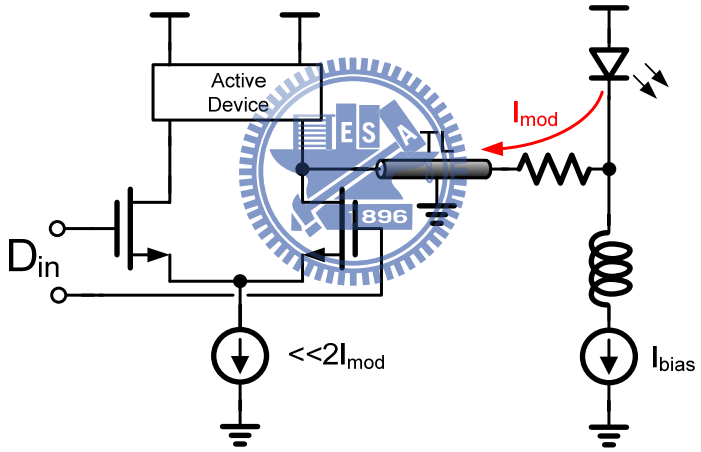


Figure 2-9 Output stage with active back-termination

2.2.2 Reviews of Active Load Laser Driver

In this section will review three proposed active back-termination, including methods of unit-gain buffer, active feedback and feedback using opamp.

Unit-Gain Buffer

Figure 2-10 shows the operating principle of the active output buffer. A

transmission line TL is terminated with an impedance R_L, represent the load, and is driven by a current source I_o, controlled by the data input signal. A replica V_o' of the intended output voltage $I_o \times Z_o$ is generated by means of a dummy current source $I_o' = I_o/k$, coupled to I_o, and a dummy load resistor $R_L' = k \times Z_o$. Unity-gain matching amplifier MA with output impedance $R_M = Z_o$ buffers V_o'. Reflection due to a mismatch between R_M and the load appear across R_M and are thus absorbed. Since the voltage between input and output of MA is essentially zero, no signal power is dissipated in the output of MA. The power reduction as compared to brute force termination results from the fact that MA only needs to accommodate reflections, which are a fraction of the size of the signal impressed upon the load.

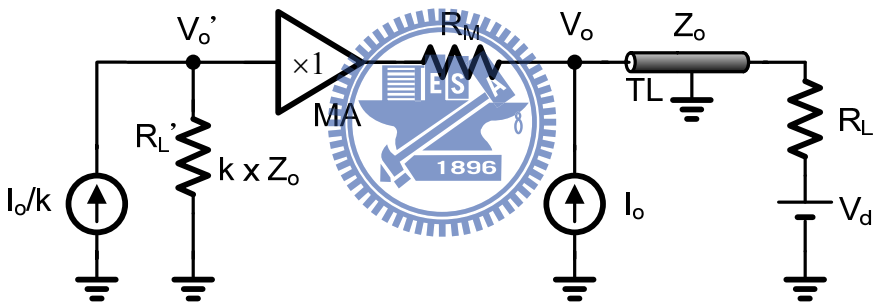


Figure 2-10 output buffer principle of [3]

Figure 2-11 shows the implementation of the output buffer. The load, in this case a laser diode, is driven by one side of differential pair M1/M2, which is biased with current I_{mod}. Differential pair M3/M4 forms the dummy current source that drives dummy load resistor R_L. Source follower M6, biased with current I_{b2}, performs the function of unity-gain matching amplifier. Since its gate and source voltage track, M6 does not carry any signal current and does not contribute to driving the load. Its sole function is to absorb reflections returning from the load. M6 is dimensioned so that the sum of its transconductance and output conductance equals 1/25 S. However, it consumes quite large current to achieve 1/25S.

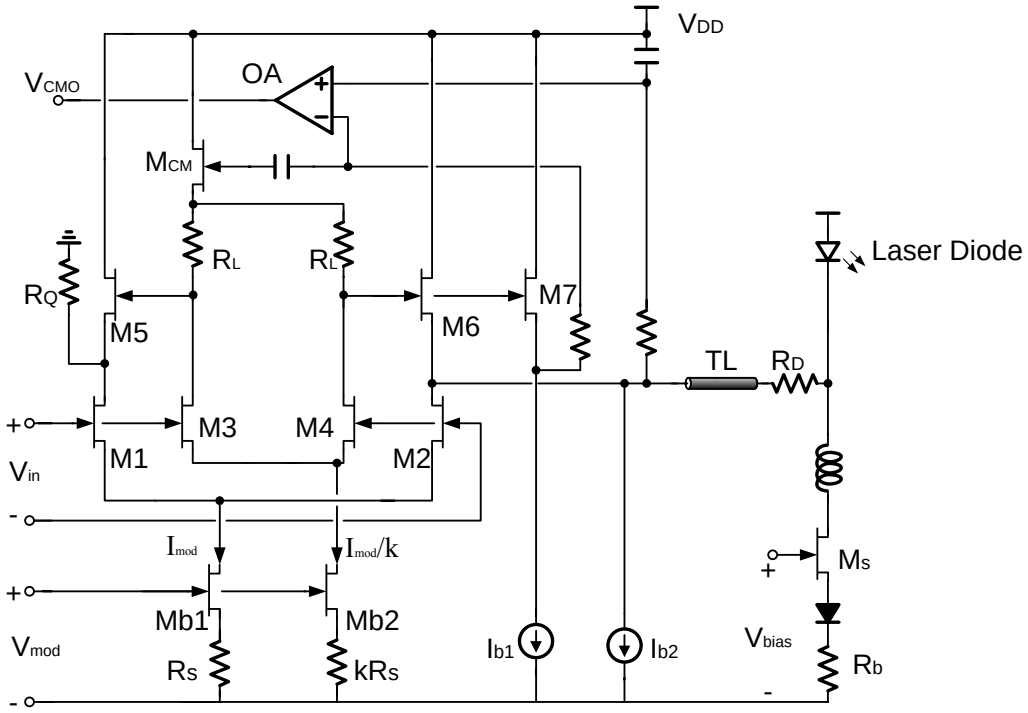


Figure 2-11 Output stage of [3]

Active Feedback

As shown in Figure 2-12, the laser diode driver output stage uses feedback around a linear amplifier, in contrast to the more commonly used differential pair current switch. This design implements a pseudo-differential feedback amplifier as a linear current gain block following an ECL-style limiting front-end data path. The amplifier is a transconductance (*Gm*) stage consisting of a degenerated differential pair (Q1, Q2) buffered by a pair of emitter followers (Q3, Q4). The output modulation current is adjusted by setting the value of the tail current I_1. After being switched by the differential pair, this current is gained up by the linear gain of the output stage to generate the modulation current at the driver output.

The equivalent impedance for match is observed by the Figure 2-13 and we can derive the loop gain, therefore the expression for the output impedance, $Ro = (Rf + Rs)/(1 + Gm.\ Rs)$, is obtain. The equivalent impedance is insensitive to imperfections in the load impedance.

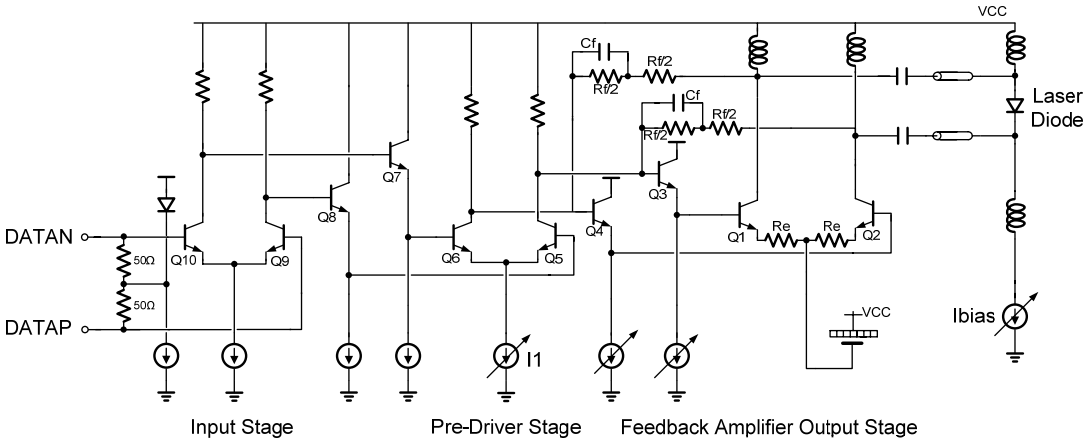


Figure 2-12 Laser driver with active feedback for back-termination [5]

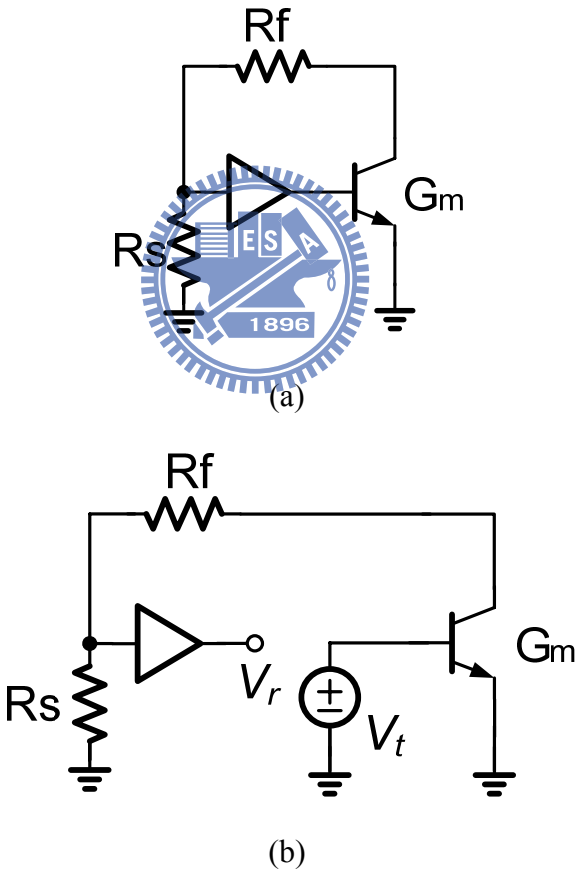


Figure 2-13 Feedback loop analysis of output impedance (a) Simplified model

(b) loop gain analysis [5]

$$loop\ gain = -\beta A = -\frac{V_r}{V_t} = -G_m\left(R_s + R_f\right) \times \frac{R_s}{R_s + R_f} = -G_m R_s$$

$$\therefore\ feedback\ resistor = \left(R_s + R_f\right) \Big/ \left(1 + G_m R_s\right) \tag{1}$$

To maintain the feedback action in the output stage it is biased at a current higher than the modulation current. This prevents either of the output devices switching off at maximum modulation current swing. The followers Q3 and Q4 are biased to prevent them from switching off during edge transitions, thereby opening the feedback loop.

Feedback using opamp

In Figure 2-14 it is possible to allow high output impedances in the driver, and still enforces 50Ω load impedance matching, by resorting to feedback. Each single-ended can be used to provide the correct termination for the other load impedance. Therefore, the impedance at one output is mirrored to the other output, and vice versa. The only drawback of the configuration is that it only applies to AC coupled lasers. The simplified schematic of the active load laser diode driver is shown in Fig, where PMOS transistors replace the output resistances. Feedback is introduced by the two resistances R_f and the opamp A driving the PMOS gates. If the gain of the feedback loop is large, then it is safe to assume that VCM is equal to the bias voltage VBIAS, i.e, V_{CM} is fixed. To show that each load resistor basically sees an impedance equal to the other load resistor, the circuit in Fig. is used. In this circuit, the right-side load is substituted by a small signal current source I_i, generating the small signal voltage V_i.

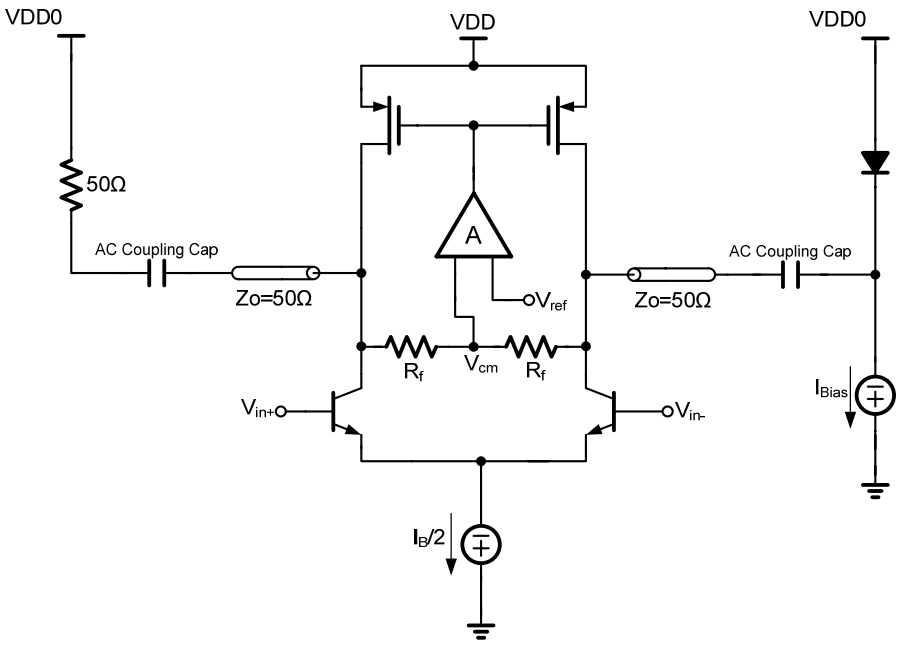


Figure 2-14 Laser driver circuit of [6]

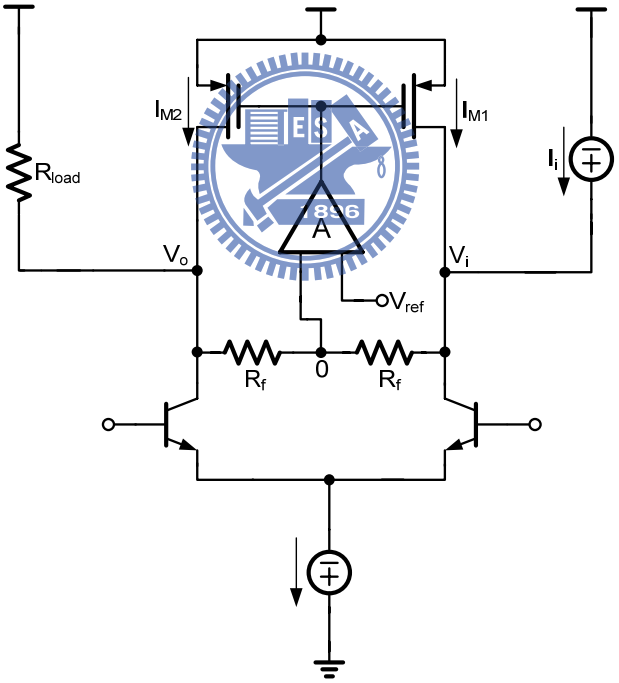


Figure 2-15 Small signal analysis of [6]

Since V_{CM} is fixed, then the same node has a zero small signal voltage, which immediately results in V_o=-V_i. Using Kirchoff's current law (KCL) at the output node, I_{M2} can be written as $I_{M2}=V_i/R_f-V_o/R_{load}=V_i/R_f + V_i/R_{load}$. Since $I_{M1}=I_{M2}$, KCL at the

input node finally yields $I_i=2V_i/R_f + V_i/R_{load}$. Therefore the input impedance R_i becomes

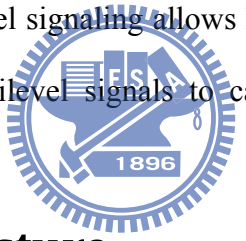
$$R_i = \frac{V_i}{I_i} = R_{load} \,||\, \frac{R_f}{2} \quad (2)$$

Which can be simplified to $R_i \fallingdotseq R_{load}$ if $R_f >> R_{load}$. Thus, as previously stated, the load resistance at the left-hand output can be used to terminate the load resistance at the right-hand output. Although this design exploits the active back-termination in simplicity way, the process used needs more masks than CMOS process and is more expensive.

Chapter 3

Design and Implementation

Since high data rates are necessary in optical communication systems, multilevel signaling has been developed to improve the spectral efficiency. The spectral efficiency is expressed in terms of bits per second per hertz and, also, is decided by signal bandwidth. Thus, multilevel signaling allows higher data rate transmission at a lower bandwidth by using multilevel signals to carry many data bits in a single symbol.



3.1 4-PAM Architecture

A higher data rate is possible by sending more complex symbols representing multiple bits during each bit-time. Although many modulation schemes can be used, multi-level pulse amplitude modulation (M-PAM) was chosen in our design for its simplicity and higher bits/Hz compared to conventional 2-PAM (binary). Multi-level PAM becomes attractive since it has smaller signal bandwidth and larger symbol period than binary signaling for the same data rate. By increasing the symbol period, the system has more tolerance to timing errors. In this section, the reasons for the choice of the modulation scheme used in this work are described in more detail.

3.1.1 4-level Pulse Amplitude Modulation

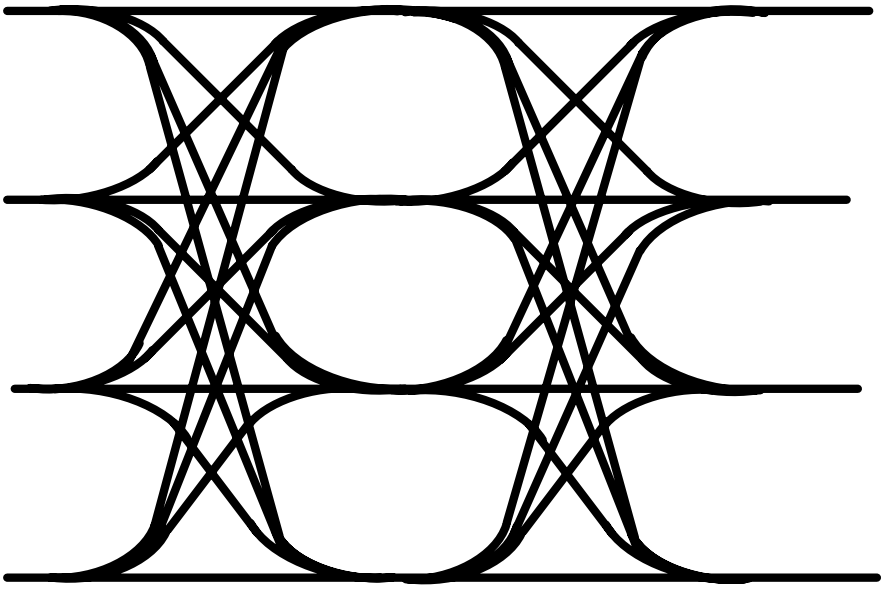


Figure 3-1 A 4-PAM eye diagram with finite transition times

By transmitting multiple bits in each symbol time, the required bandwidth of the channel for a given bit rate decreases and system channel efficiency increases. The simplest multi-level transmission scheme is *M*-level pulse amplitude modulation (*M*-PAM), where each pulse conveys $log_2(M)$ bits of information. For a given data rate, *M*-PAM modulation reduces the effective symbol-rate by a factor of $log_2(M)$ compared to a conventional binary (2-PAM) system. This symbol rate reduction reduces not only the in the channel, but also the maximum required on-chip clock frequency. However, the more complex transitions to multiple levels, the more complex circuitry to generate the multi-level signal.

This work uses 4-level PAM (As shown in Figure 3-1) for transmission, which decreases the symbol rate by a factor of two compared to 2-PAM. An *M*-PAM scheme with larger *M* was avoided due to limited signal resolution of the receiver, especially

at high speeds, and maximum transmitter output swing, both of which constrain the PAM level spacings. For a fixed transmitter swing budget, level spacings decrease with *M*:

$$LevelSpacing = \frac{XmitterSwing}{M-1} \quad (3)$$

The smaller the level spacings, the more vulnerable the signal will be to noise from a variety of sources. Since VCSEL operates at low current, it is not appropriate to divide many signal levels.

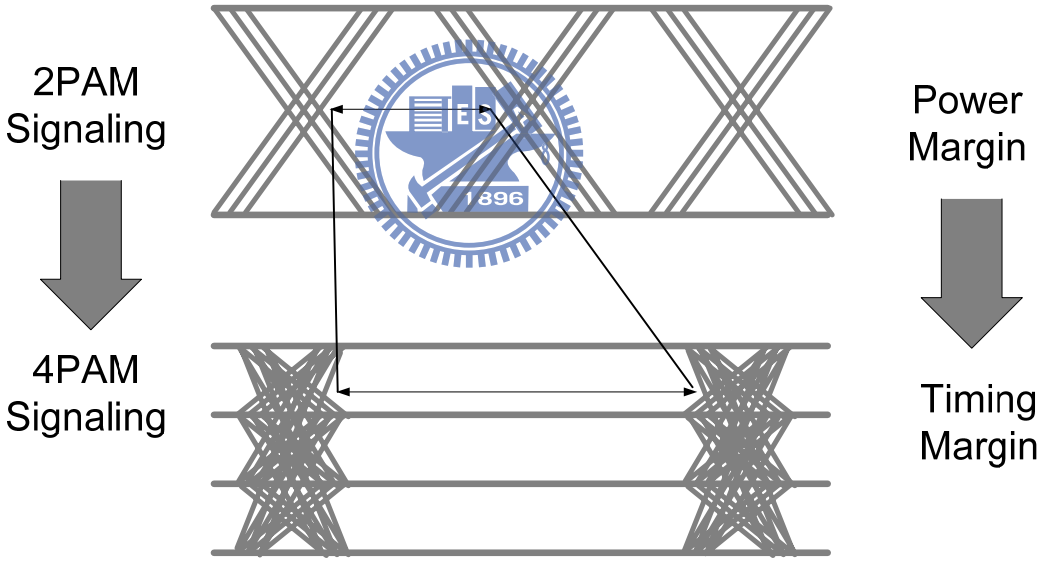


Figure 3-2 Comparison of 2-PAM and 4-PAM

As shown in Figure 3-2, the complex 4-PAM transitions result in an increase in eye-width which is much wide compared to 2-PAM signaling. Although the nominal eye height is reduced by a factor of three (as there are three eyes), the eye height is effectively decreased by less than 50%. Therefore, a 4-PAM scheme typically has a larger eye width, but smaller eye height, compared to 2-PAM at the same data rate. To

sum up, *M*-PAM scheme increases the timing margin of each bit interval, but it also needs to make a compromise with signal to noise ratio (SNR) under limited signal swing.

3.1.2 Proposed 4-PAM Laser Driver Architecture

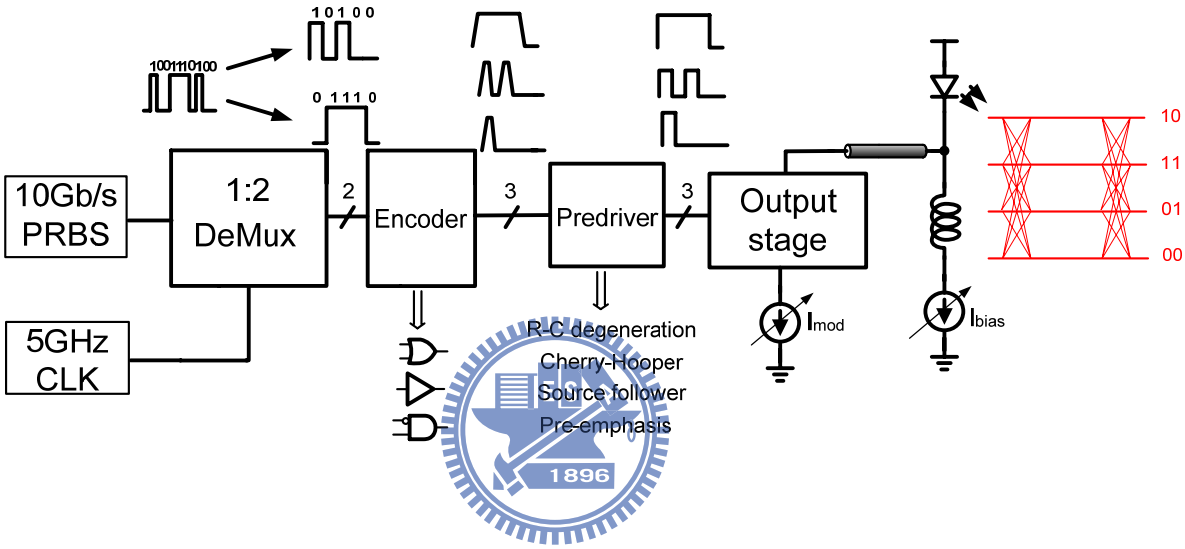


Figure 3-3 Architecture of proposed 4-PAM laser diode driver

Figure 3-3 shows the proposed 4-PAM laser diode driver architecture which consists of 1 to2 de-multiplexer, 2 to 3 encoder, pre-driver and output stage. Assume a serial 10 Gb/s pseudo random bit sequence (PRBS) is separated by the positive and negative edge of 5GHz clock. Next, the two parallel data paths are encoded and result in three logic signals. It is quite difficult for the output signals of encoder to drive current switches directly, so we place pre-driver between encoder and output stage. The pre-driver provides low output impedance which is beneficial for high speed operation. Finally, the output stage controlled by the logics generates three different level current signals to the laser diode. In the next few sections, we will discuss the

circuit design in more detail.

3.1.3 VCSEL Specification

Table 3-1 shows some specifications of the target VCSEL. However, before designing a VCSEL driver, there are some important characteristics needed to be defined by measuring the target VCSEL. The measured V/I and P/I characteristics of the VCSEL are shown in Figure 3-4 and 3-5.

VCSEL Charactristics

Parameter	Min	Typical	Max	Unit
Wavelength	830	850	860	nm
Threshold current	-	1.2	2.75	mA
Slope efficiency	0.05	0.08	0.12	mW
Forward voltage	1.6	1.8	2.1	V
Rise time/ Fall time	-	-	90	ps

Table 3-1 Specification of VCSEL

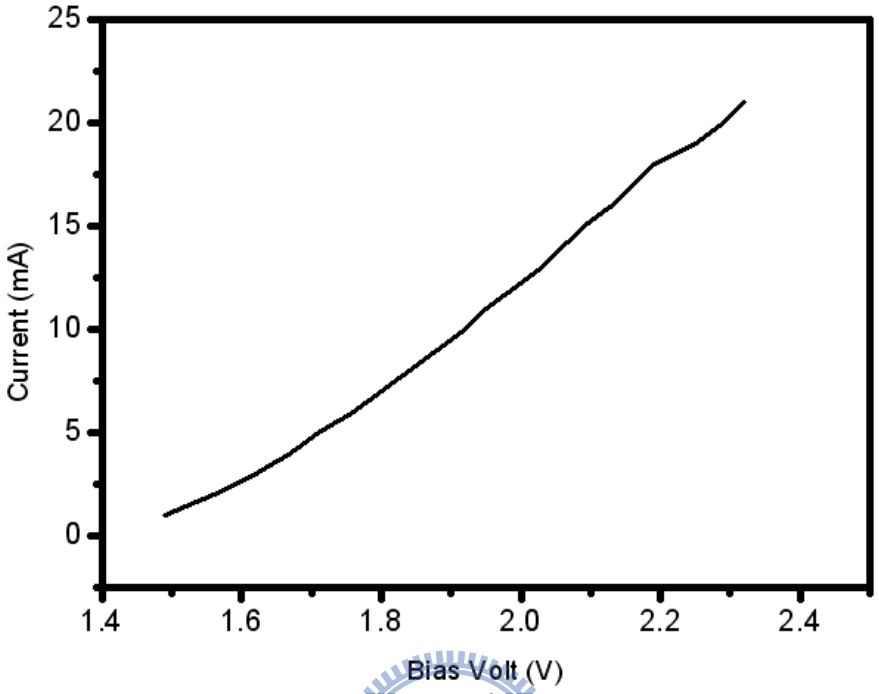


Figure 3-4 V/I curve of VCSEL

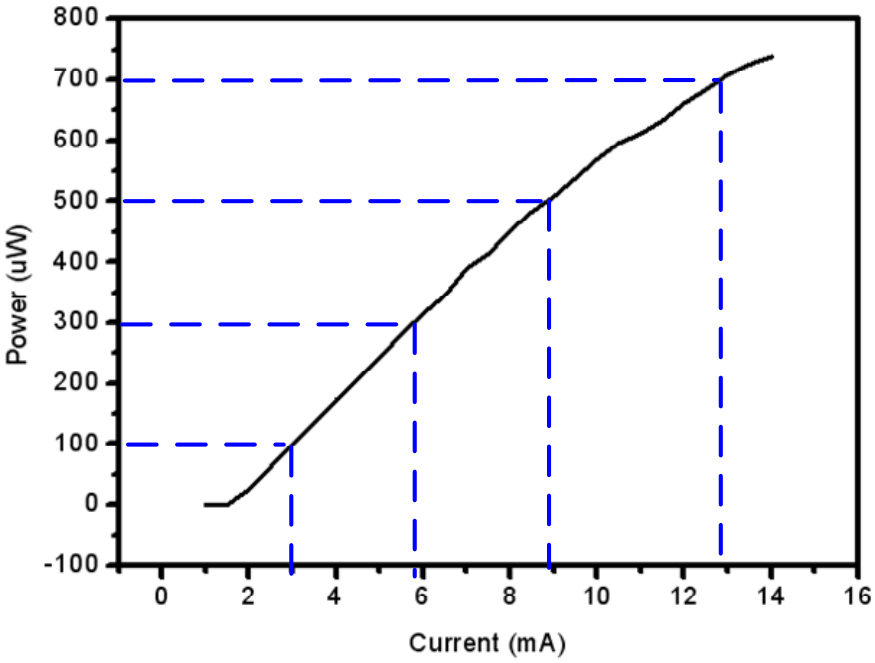


Figure 3-5 P/I curve of VCSEL

3.2 DeMux

In high speed laser and modulator drivers, the input data signal often is retimed or resynchronized with a clean clock signal before being fed to the pre-driver. The benefits of the data retiming are the elimination of pulse-width distortion and jitter from the input data signal.

Retiming flip-flops usually are implemented with current mode logic (CML), which is based on nested and cascaded current steering circuits. The advantages of CML are its high speed, its low sensitivity to common-mode and power supply noise, and its substantially constant supply current, which minimizes power and ground bounce.

As shown in Figure 3-6, in our design we separate the serial data sequence into two parallel streams by a 1 to 2 DeMux with the use of the positive and negative edge of the trigger clock. Figure 3-7 shows the 1 to 2 DeMux's timing chart. To obtain maximum timing margin, the clock signals should be aligned at the center of the data pulse.

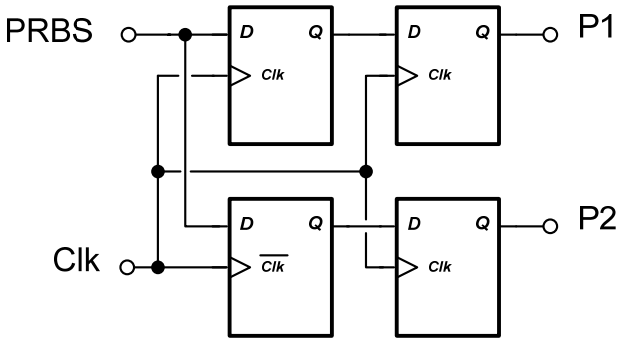


Figure 3-6 2 to 1 DeMux

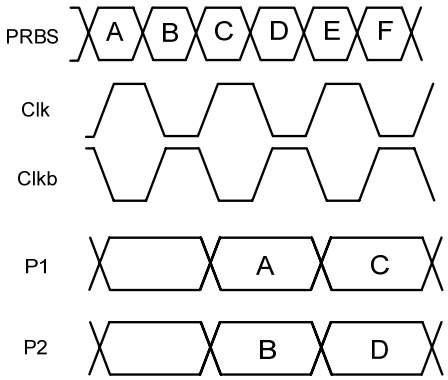


Figure 3-7 Timing chart of 2 to 1 DeMux

Figure 3-8 shows the detail circuit schematic of a single flip-flop. This flip-flop consists of a cascade of two identical D latches. The operation of flip-flop can be explained as follows: if M5 is turned on and M6 is turned off by the clock signal, the D latch acts as an amplifier, passing the input logic state to the output by means of M1, M2. Conversely, if M6 is turned on and M5 is turned off, the D latch acts as a regenerator storing the previous logic state by means of positive feedback through M3, M4. In the latter case, the output state is independent of the input state. The second D latch is clocked from the inverted clock such that when the first latch is in amplification mode, the second one is in regeneration mode and vice versa.

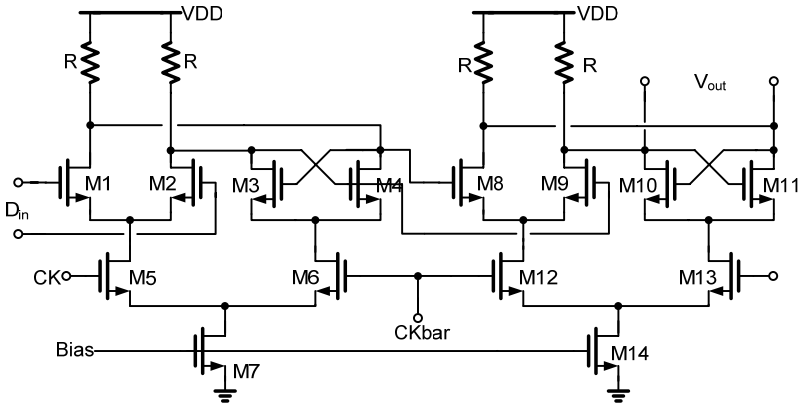


Figure 3-8 D flip-flop

3.3 Encoder

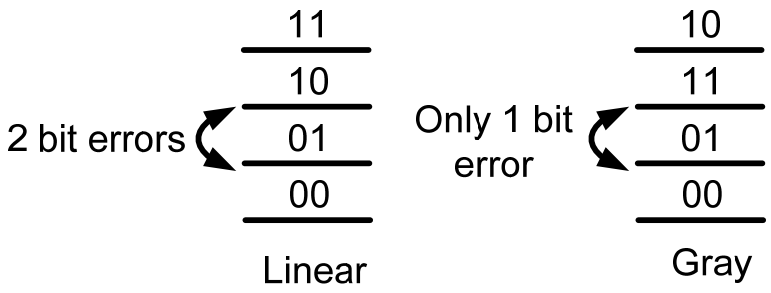


Figure 3-9 Linear versus Gray code mapping of levels

In this work, our goal is to generate 4-PAM signaling, namely, there are four signal levels need to be defined. The lowest level is decided by the laser bias current, hence, three additional current switches are needed to account for the other three signal levels. Since each symbol represents 2-bit data information, we have to encode bit sequences. As shown in Figure 3-9, there is a drawback in the traditional linear coding. When the signal level changes from "01" to "10", there is a two-bit transition. If coding miss occurs and then the bit error rate might be worse than Gray coding, because there are two bits changed. However, the Gray coding guarantees that every nearest bit error results in only one bit error. Thus the expected bit error rate is reduced to that of the linear coding.

For speed and voltage swing considerations, the current mode logic circuit is adopted for the encoder design. For example, $F = \overline{A + B}$ could be implemented in Fig. 3-10, however, the stack configuration might suffer glitch when some transition occurs and voltage headroom issue if the supply voltage is low. The circuit shows in Fig. 3-11, only adopts parallel configuration and it also relaxes the problems

mentioned above. Since there are two data signal paths and three current switches. Therefore, we can decide the corresponding logics for each current switch by the truth table show in Figure 3-12. Those current switches are shown in Figure 3-13.

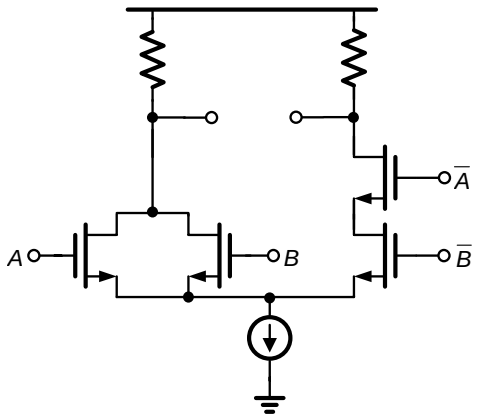


Fig. 3-10 Stack configuration of CML

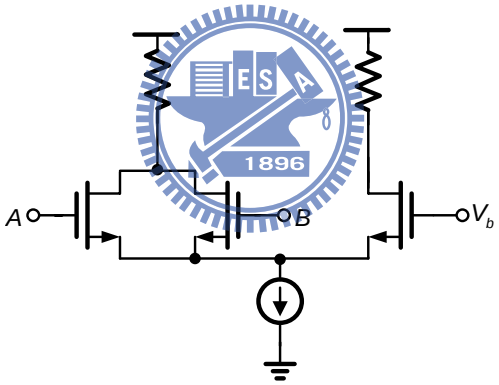
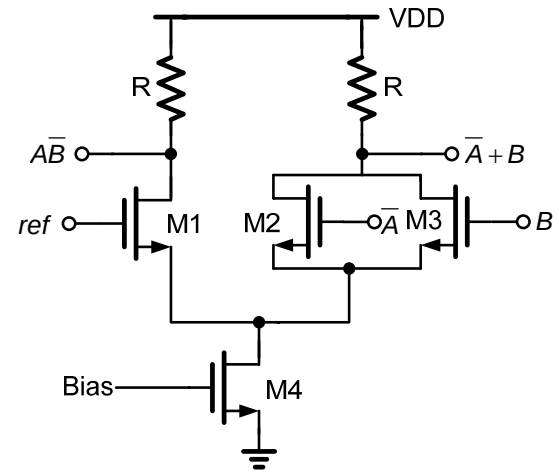


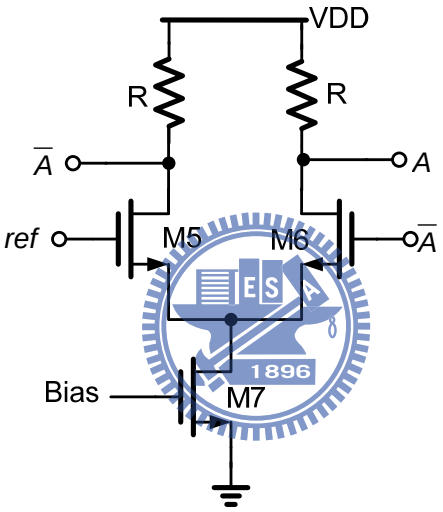
Fig. 3-11 Flat configuration of CML

A	B	D_3	D_2	D_1
0	0	0	0	0
0	1	0	0	1
1	1	0	1	1
1	0	1	1	1

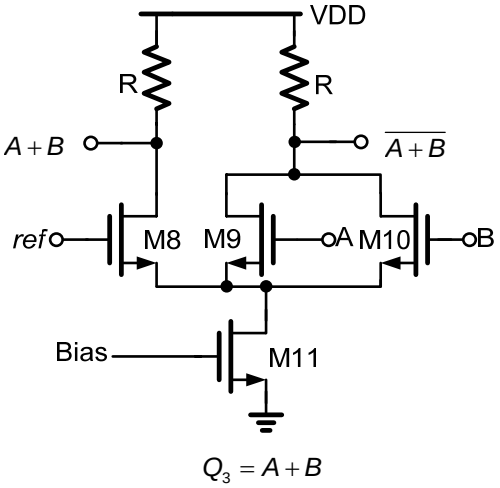
Figure 3-12 Truth table of encoder



$Q_1 = A\overline{B}$



$Q_2 = A$



$Q_3 = A+B$

Fig. 3-13 Circuit implementation of Gray coding encoder

3.4 Pre-driver

Since the transistors in the driver's output stage have to switch large current therefore must be made quite large. As a result, their input capacitance also becomes quite large. An on chip circuit block, such as a retiming flip-flop, may not be able to drive this large capacitance at the required speed. Another issue is the input voltage swing necessary to switch the output stage. Note that for am FET output stage, large devices are required to achieve a small switching voltage, but these devices also have a large input capacitance. Vice versa, a low input capacitance implies small devices, resulting in a high switching voltage. To resolve this dilemma, a so-called pre-driver generally is used to drive the output stage. The pre-driver must be able to drive a large capacitive load while keeping its input capacitance low. It also must provide sufficient voltage gain to ensure full, or near full, switching of the output stage.

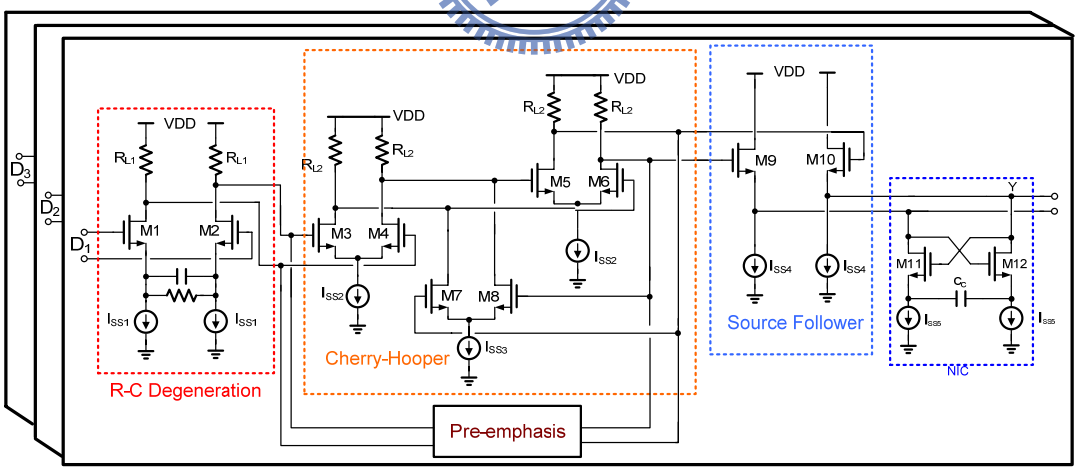


Figure 3-14 Pre-driver

Figure 3-14 shows the pre-driver which is composed of three sections. The first one is a differential pair with R-C degeneration which is designed for canceling the pole at the input of Cherry-Hooper amplifier, because there is another path, pre-emphasis connected with Cherry-Hooper input. Therefore R-C degeneration

would relax the parasitic effect. The next stage is Cherry-Hooper stage, which combines series and shunt feedback, thus its output impedance is quite small. For this reason, it can be used to provide gain in high speed pre-drivers. The final stage of the pre-driver is a source follower for level shifting and a negative capacitance circuit connected to the output of the pre-driver to compensate for some of the positive capacitance presented by the output stage. In the next few pages, we will discuss the circuit technique in more details.

3.4.1 Capacitive Degeneration

In order to create a broadband response, it is possible to degenerate the transistors in a differential pair such that their effective transconductance increase at high frequencies, thereby compensating for the gain roll-off resulting from the pole at the output node. Shown in Figure 3-15, the configuration employs both capacitive and resistive degeneration.

$$G_m = \frac{g_m(R_S C_S s + 1)}{1 + R_S C_S s + g_m R_S / 2} \quad (4)$$

The transconductance contains a zero at $1/R_S C_S$ and a pole at $(1 + g_m R_S/2)/(R_S C_S)$. If the zero cancels the pole at the drain, i.e., if $R_S C_S = R_D C_L$, then the overall amplifier's bandwidth is extended to $(1 + g_m R_S/2)/(R_S C_S) = (1 + g_m R_S/2)/(R_D C_L)$. In other words, as illustrated in Figure 3-16, the speed is increased by a factor of $1 + g_m R_S/2$. This is a trade-off between bandwidth and gain, since there is a reduction in gain by a factor of $1 + g_m R_S/2$.

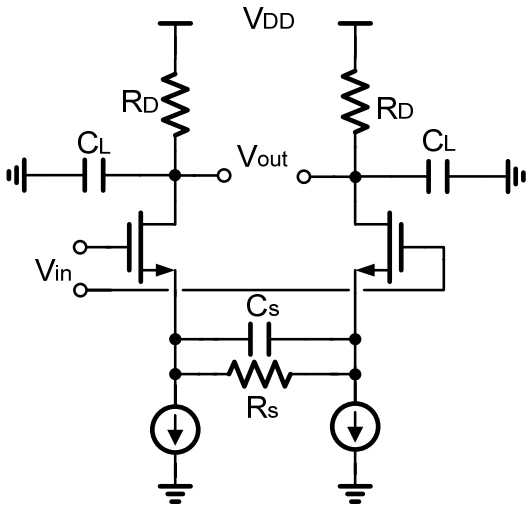


Figure 3-15 (a) Differential pair with capacitive degeneration

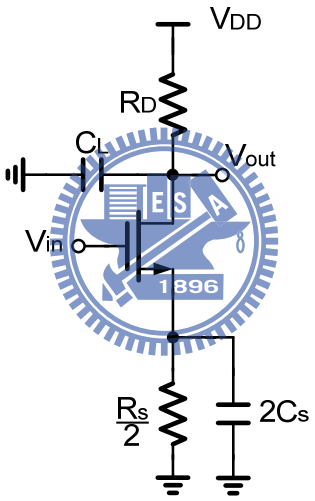


Figure 3-15 (b) half-circuit equivalent

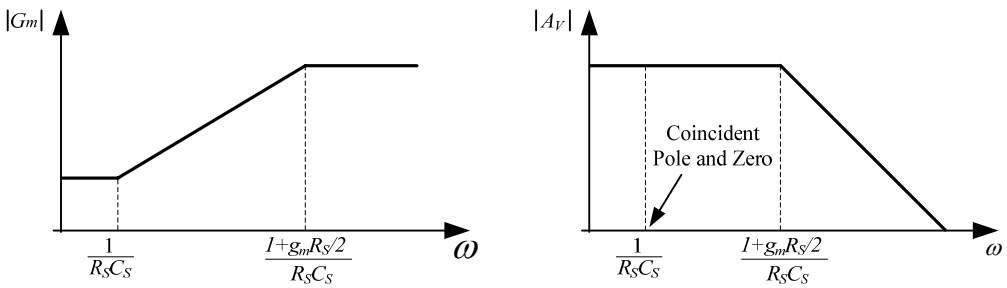


Figure 3-16 Variation of (a) Gm and (b) voltage gain with frequency

3.4.2 Negative Capacitance

A negative impedance converter (NIC) consisting of M3 and M4 in Figure 3-17 transforms Cc to a negative capacitance between nodes X and Y. if the gate-drain capacitance of M3 and M4 is neglected, the impedance seen looking into the drains is expressed as:

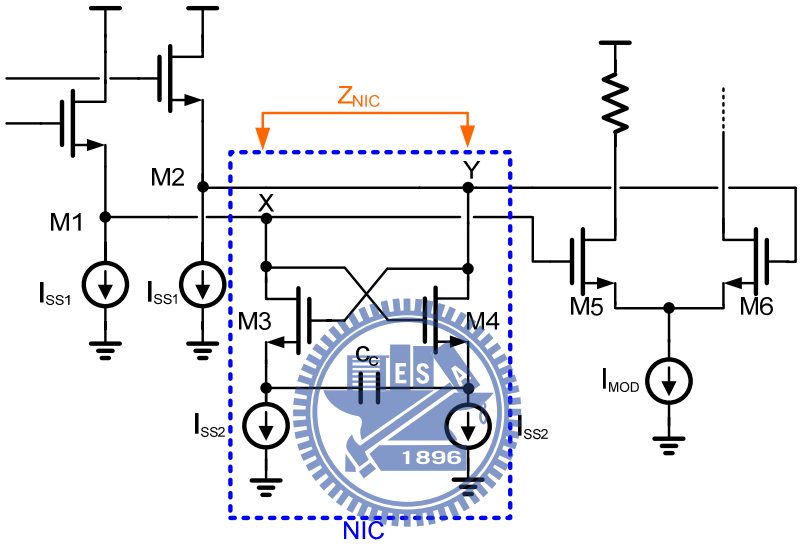


Figure 3-17 Negative impedance converter

$$Z_{NIC} = -\frac{1}{sC_c}\frac{g_m + s(C_{gs} + 2C_c)}{g_m - sC_{gs}} \quad (5)$$

Thus, for frequencies well below the f_T of the transistors, Z_{NIC} is equivalent to a negative capacitance $-C_C$ in series with a negative resistance $-\left(C_{gs}/C_C + 2\right)/g_m$

3.4.3 Pre-emphasis

FIR filter

Transmitter pre-emphasis uses a symbol-spaced finite impulse response (FIR) filter integrated (as shown in Figure 3-18) into the pre-driver, specified by the following equation:

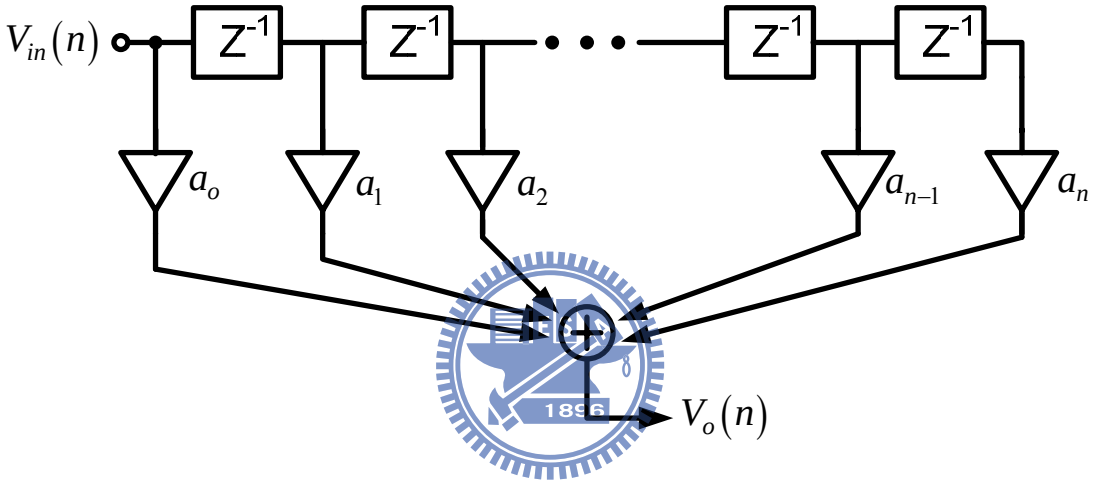
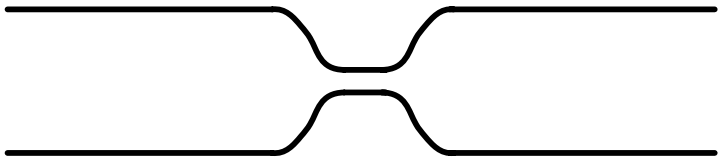


Figure 3-18 FIR filter

$$V_o(n) = a_o V_{in}(n) + \sum_{i=1}^{n} a_i V_{in}(n-i) \quad (6)$$

The inputs to this filter are the present and past transmitted symbols. The coefficients of the filter depend on the channel characteristics. The length of the filter N, (i.e. number of filter taps), depends on the number of symbols in the past that affect the present symbol. Therefore, the output of the filter is the present symbol value plus the weighted values of the past N symbols. Effectively, the FIR filter output, which is the sum of the present symbol and weighted values of N former symbols, will no longer have the distinct signal levels of the unfiltered signal stream, and the output driver in the fact.



(a)

(b)

Figure 3-19 Signal waveform (a) without pre-emphasis (b) with pre-emphasis

In the simplest case, the FIR filter effectively suppresses the power of low-frequency components by reducing the amplitude of continuous strings of same-value data on the line. At the same time, it keeps the power of high-frequency components constant by increasing the signal amplitude during transition. Figure 3-19 shows an example of the effect of a single tap transmit filter (a2,3….=0) on an isolated pulse in the field of zeros at both ends of the cable. The undistorted waveform on the top shows zero eye opening. With pre-distortion, as shown on the bottom, a clean eye opening is visible.

The main disadvantage of this approach is that the transmitter uses part of the signal amplitude budget to generate the pre-emphasis symbols following the main symbol. Therefore, the actual transmitted signal amplitude is:

$$Signal\ amplitude = Total\ amplitude \bullet \left(|a_0| - |a_1| - |a_2| - \cdots\cdots \right) \quad (7)$$

which effectively reduces the received signal amplitude, and therefore decreases the signal to noise ratio. One of the important advantages of transmit pre-emphasis filter is the ease of implementing long FIR filters at very high speed using this scheme. The reason is that all the previously transmitted symbols are already available to the

transmitter. It is only necessary to add or subtract the weighted values of these known symbols from the present symbol value.

Pre-emphasis design

Since the current switches of laser output stage contribute large parasitic capacitance at pre-driver output. The signal transient time would be limited. To compensate this unwanted effect, we propose a pre-emphasis circuit to equalize the pre-driver output signal. The pre-emphasis circuit enhances signal transient by the combination of the delayed and original signals. Since our architecture is parallel, complex pre-emphasis technique is not appropriate for our design. The pre-emphasis circuit in our design is shown in Figure 3-20. For simplicity we delay signal for half symbol period by latch. We want to improve the transient when signals occur transition, namely from high to low or from low to high. Consequently we introduce exclusive or logic circuit to detect whether the signal transition occurs or not. Those detected results control the pre-emphasis current switches. When those switches turn on, the current sums up at the pre-driver outputs. Also, it contributes a half symbol period peak in the output waveform and high-frequency components got enhanced.

Figure 3-21 shows the waveforms of the succeeding stage after the encoder. In order to synchronize the control signals of the current switches, we retime the output signals of encoder. As we can tell from the output waveform of Cherry-Hooper, the high frequency part is indeed enhanced.

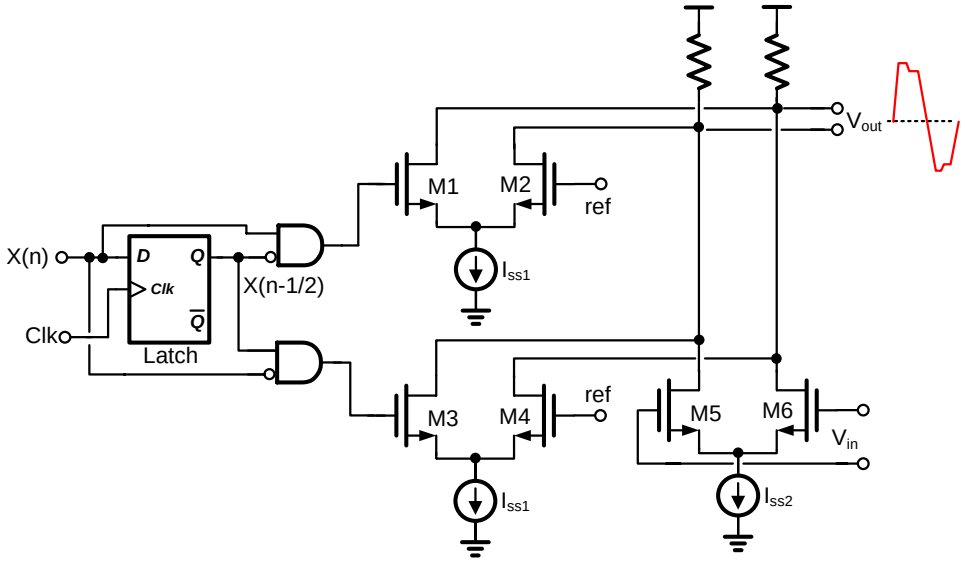


Figure 3-20 Implementation of pre-emphasis circuit

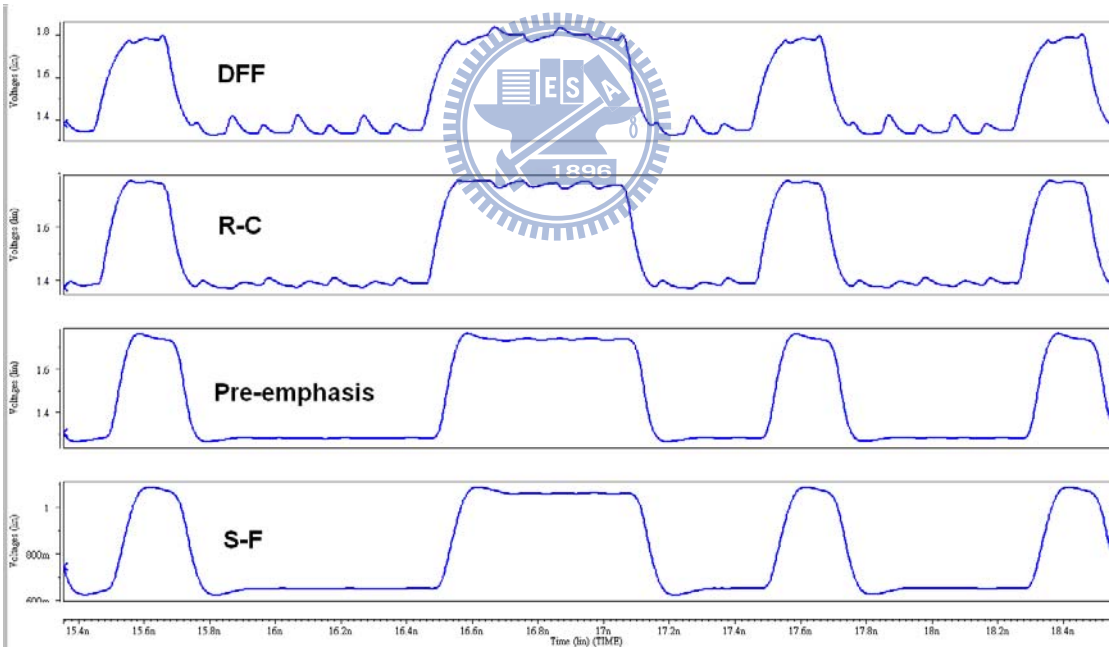


Figure 3-21 Waveforms of the each stage after encoder

3.5 Output Stage

Figure 3-22 shows the VCSEL output stage circuit, transmission line, and the VCSEL equivalent model with forward voltage, parasitic capacitance, resistor, and package inductance, included. The I-V curve (Figure 3-4) of our target VCSEL indicates the parasitic resistance of the VCSEL itself is 43ohms. Thus, for 50ohms impedance matching consideration, we add R_T, 7ohms. R_M is a dummy load resistor. Since the lowest output optical power of VCSEL is defined by the biasing current of VCSEL, in order to generate the three additional levels, the VCSEL output stage needs three current switches (M7~M12). Transistor M3~M6, R1, and R2 forms a Gilber cell like configuration which control the active back-termination.

We illustrate the active back-termination with Figure 3-23. When output stage delivers data, voltage drop occurs at the output of current switches. The equivalent voltage drop is equal to $N \bullet I_{\mathrm{mod}} \bullet (R_P + R_T)$. At the same time, there is also an equal voltage drop, $N \bullet I_{cont} \bullet R_1$, generated by the Gilbert cell at the gate of M1. Note that since M1's gate and source voltages have same voltage variation while output stage delivering signals. Namely, its Vgs keeps constant, M1 doest not carry any signal current and does not contribute to driving the VCSEL, therefore the modulation current is totally provided to the VCSEL. In our design, I_{cont} is scaled-down version of I_{mod}, by factor k, therefore R1 is the magnified version of $(R_P + R_T)$ by the same ratio.

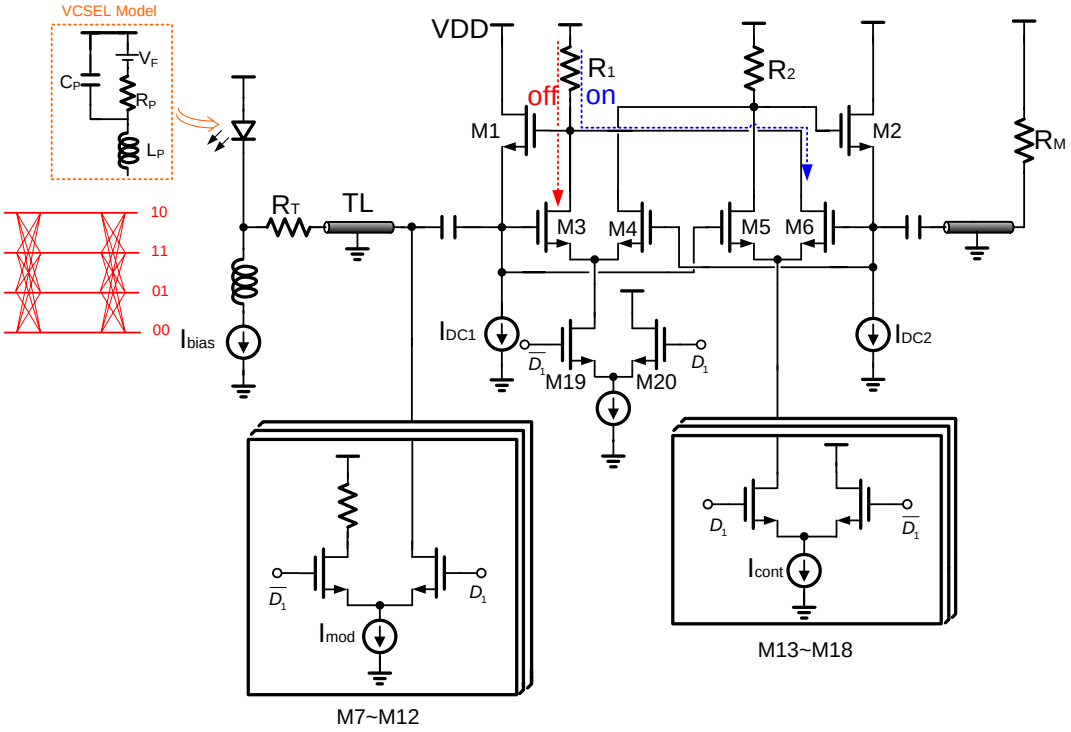


Figure 3-22 Implementation of output stage

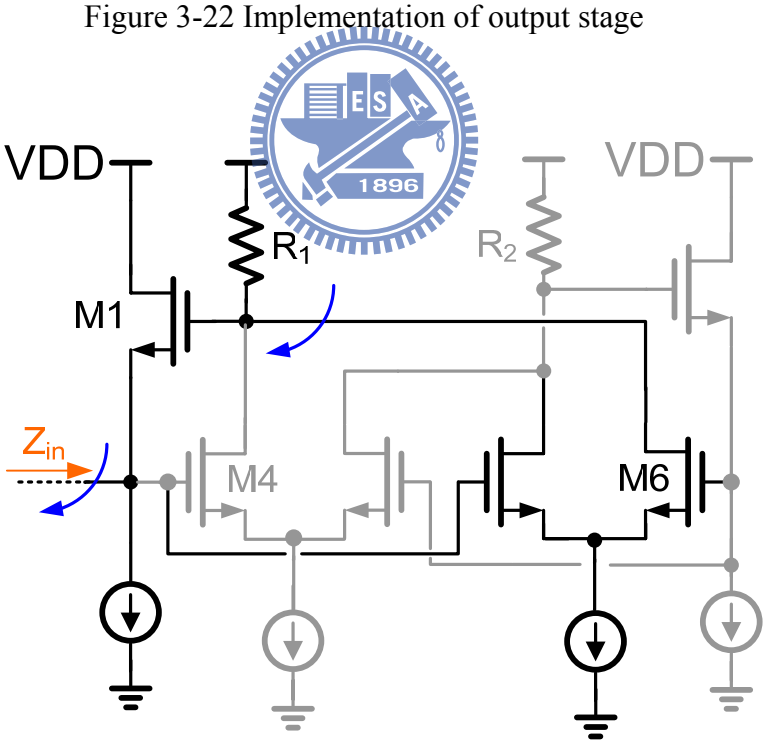


Figure 3-23 Active back-termination when modulation current is delivered

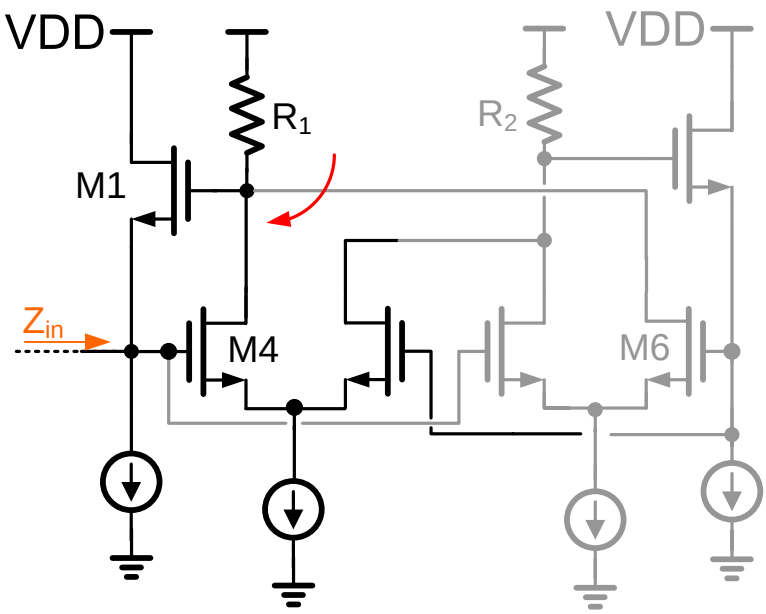


Figure 3-24 Active back-termination when no modulation current is delivered

Active Back-termination

In our design, when output stage delivers no signal, the voltage of laser cathode rises and the current switch controlled by LSB causes a voltage drop at the M1's gate. From the point view of transmission line, a positive and a negative AC signal is at the transmission line end respectively. Therefore the transmission line itself could be regarded as AC ground, which means transmission line reduces any reflections returning the load.

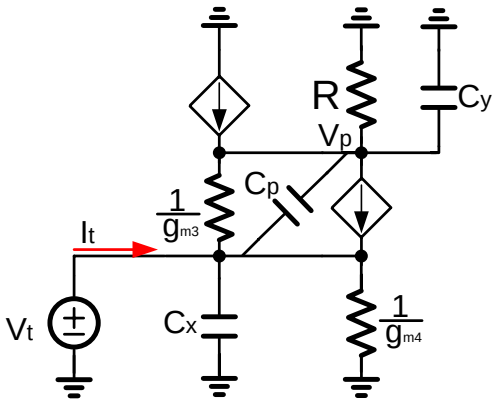


Figure 3-25 Equivalent circuit of termination

$$Z_{in}=\frac{V_t}{I_t}=\frac{1+sRC_y}{(sC_x+g_{m3})(1+sRC_y)-(sC_p+g_{m3})(sC_p-g_{m4})R}$$

$$s\longrightarrow 0 \quad Z_{in}=\frac{1}{g_{m3}+g_{m3}g_{m4}R} \qquad s\longrightarrow\infty \quad Z_{in}=\frac{1}{sC_x}=0 \tag{8}$$

The regulated cascode circuit we mentioned serves as an active back-termination. From the equivalent small signal model (shown in Figure 3-25), we can derive the equivalent impedance at M1's with source and parasitic effect considered. The equivalent impedance is derived in eq.(8). In eq.(8), the impedance is divided by a loop gain and it is capacitive when frequency increases.

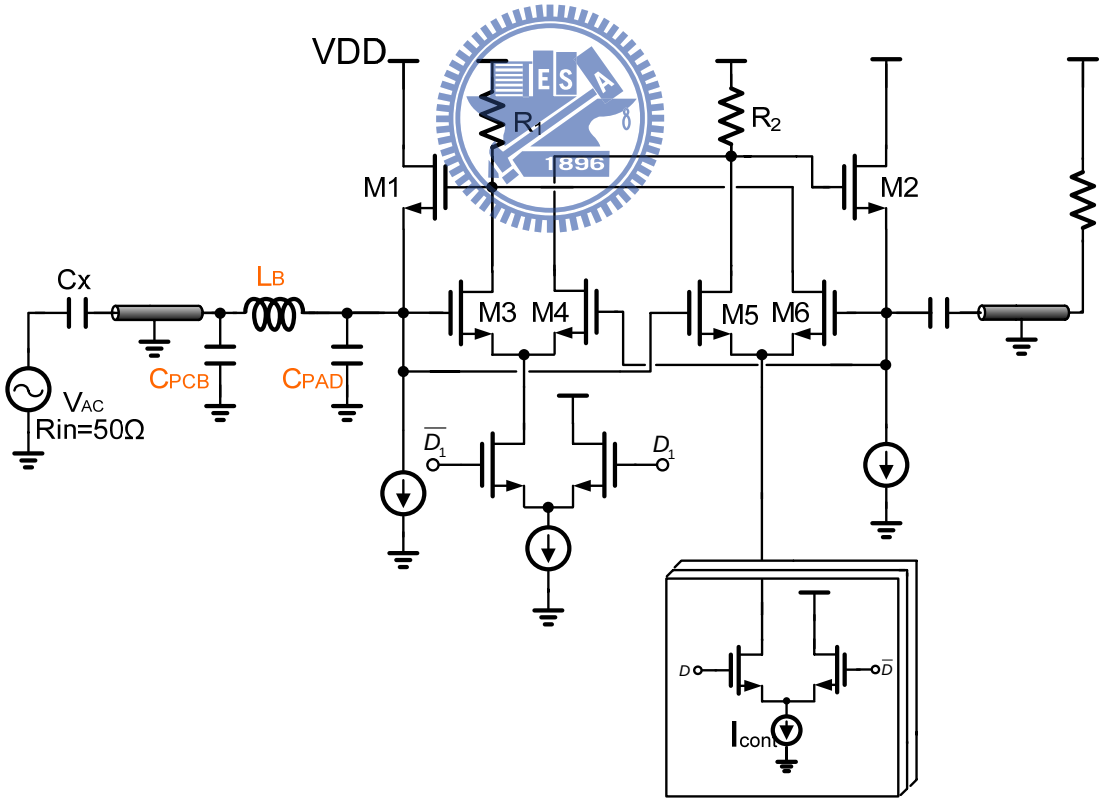


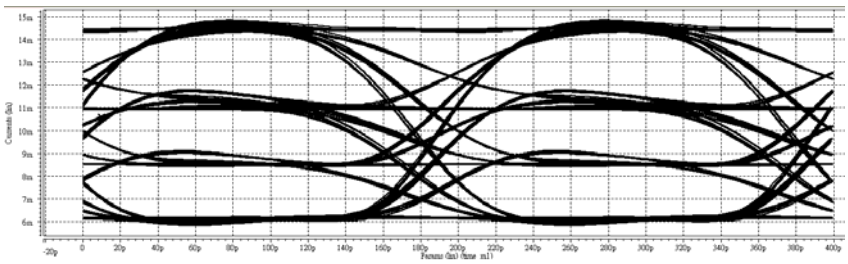
Figure 3-26 Simulation scenario of return loss

S-parameter

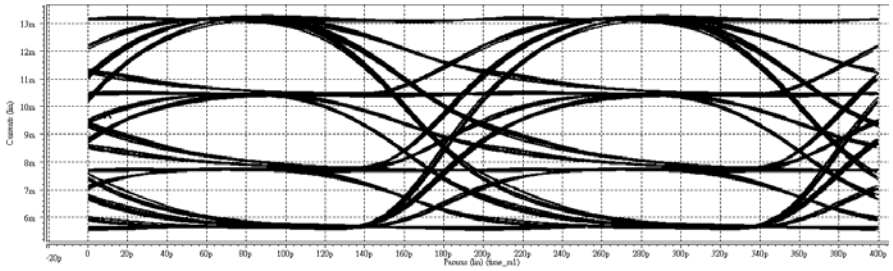
Figure 3-26 shows the simulation scenario of return loss, in order to estimate the return loss, we consider the parasitic effects contributed by pads, bond wire, and printed circuit board (PCB) pins. The capacitor Cx and the small signal source Vac with 50ohms resistance are the equivalent model of instrument. In the simulation, Vac provides a small signal and we measure the amount of reflection, such that we can realize much reflection is absorbed by our active back-termination.

Simulation results

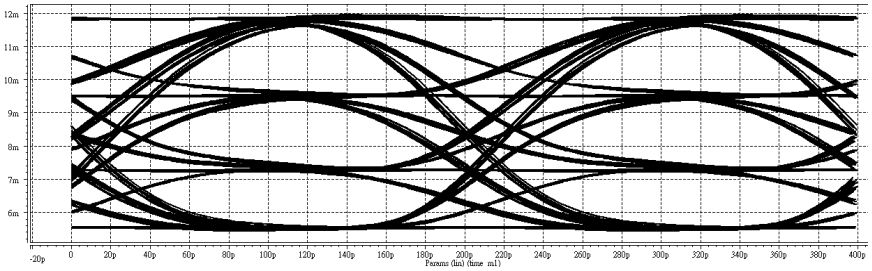
Figure 3-27 and 3-28 show the post-simulation of electrical eye-diagrams of 4-PAM VCSEL driver under different corners and the S-parameter, respectively.



(a) FF

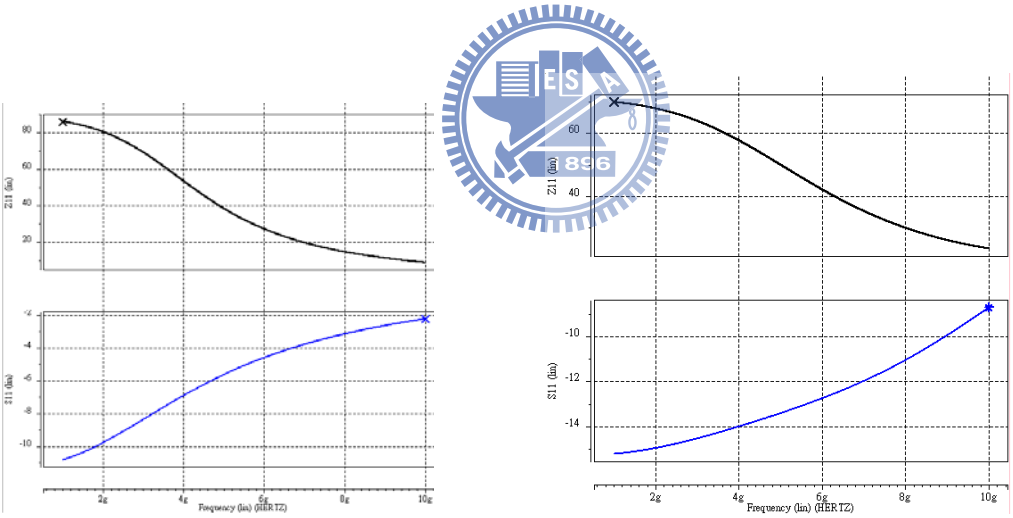


(b) TT



(c) SS

Figure 3-27 4PAM 10Gbps at 50℃ with different corners



(a) Data transmitting (b) No data transmitting

Figure 3-28 S-parameter (a) S22<-6dB at 5GHz (b) S22=-13dB at 5GHz

Chapter 4

Experiment Results

4.1 Chip Photo

Figure 4-1 shows proposed 4-PAM laser diode driver is fabricated in TSMC 0.18μm 1P6M CMOS process. The total chip area is 1600μm×780μm^2, including pads.

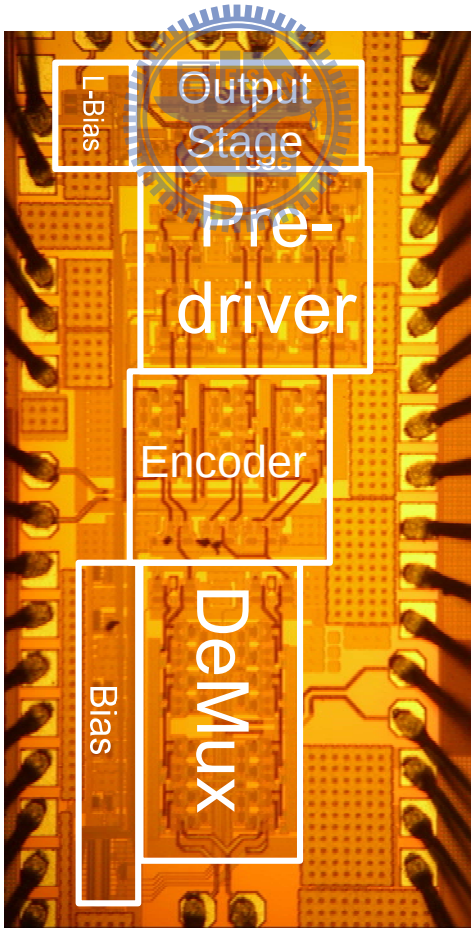


Figure 4-1 Chip photo of 4-PAM laser diode driver

4.2 Electrical Measurement

Figure 4-2 shows the environment setup for electrical measurement, the AWG (arbitrary waveform generator) provides the input serial PRBS, clock for de-multiplexing and clock for the retiming of encoder output signal. The output of the chip is biased by a voltage, V_{CC}, and senses the output modulation current by AC coupling, as shown in Figure 4-3.

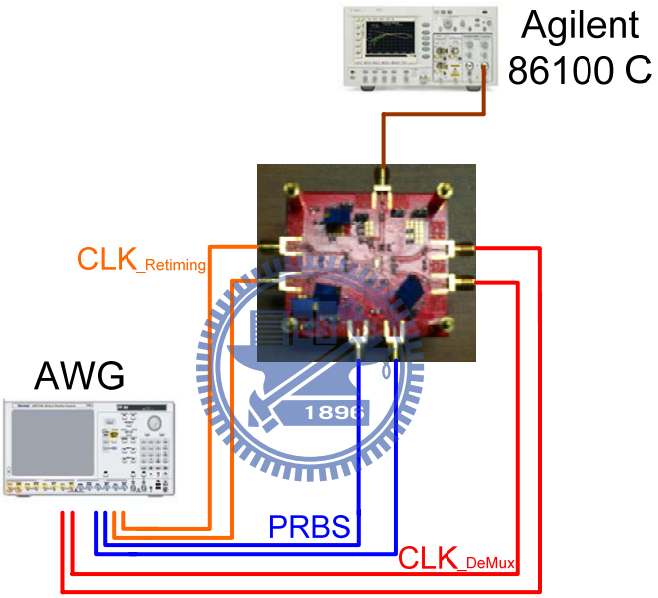


Figure 4-2 Electrical measurement setup

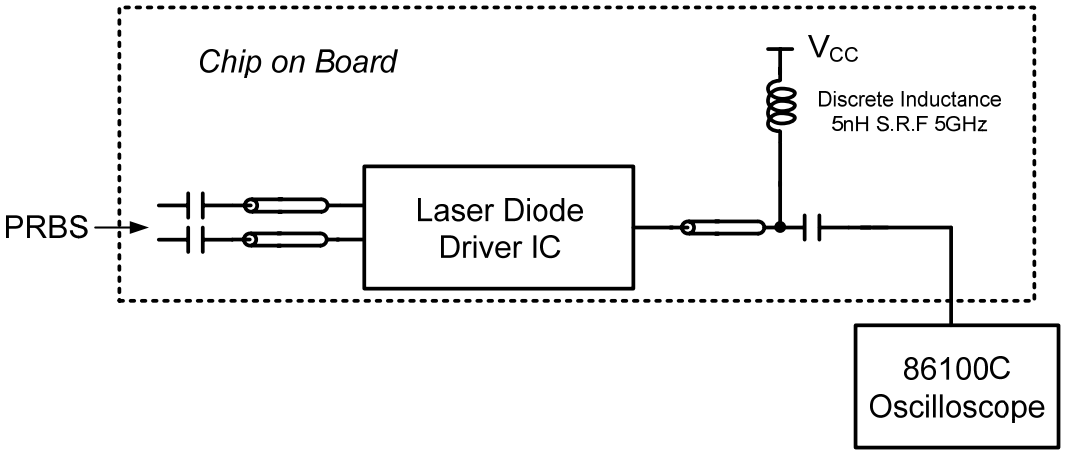


Figure 4-3 The output network of electrical measurement PCB

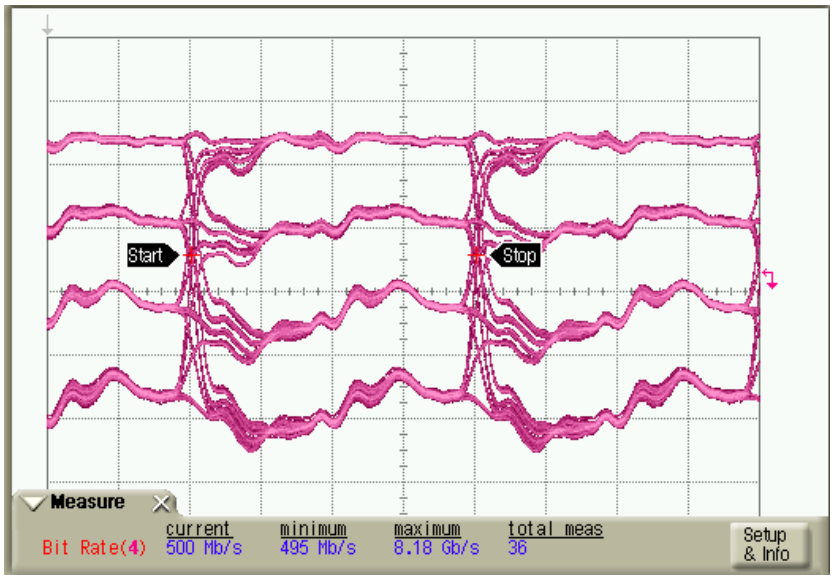


Figure 4-4 Eye-diagram of 4PAM 1Gbps

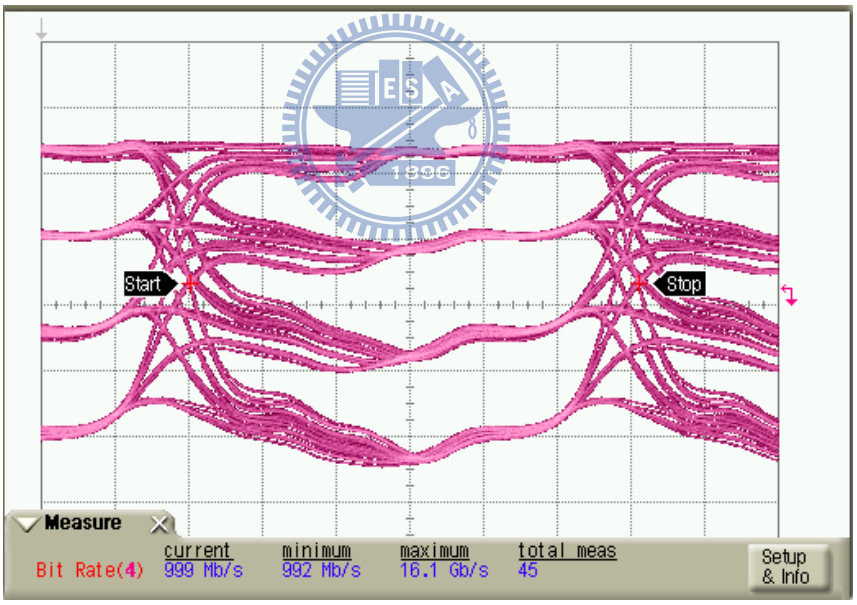


Figure 4-5 Eye-diagram of 4PAM 2Gbps

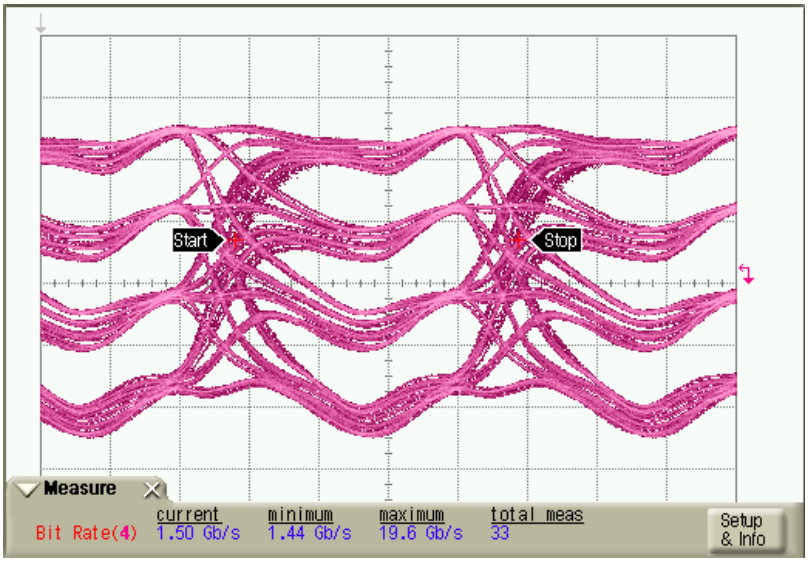


Figure 4-6 Eye-diagram of 4PAM 3Gbps

4.3 Optical Measurement

Figure 4-8 shows the top view of the PCB for optical power measurement, we can adjust the modulation current by tuning the three variable resistors on the PCB, in case of the VCSEL output optical power is not linear. However, the experimental results reveal the optical power is linear to modulation current. Thus we do not tune those variable resistors. Figure 4-9 shows the environment setup for optical measurement, the AWG provides the input serial PRBS, clock for de-multiplexing and clock for the retiming of encoder output signal. Finally, we use FC connector as a medium to transport the optical signals from VCSEL to the oscilloscope. The following Figures show the measured results with different input date rate.

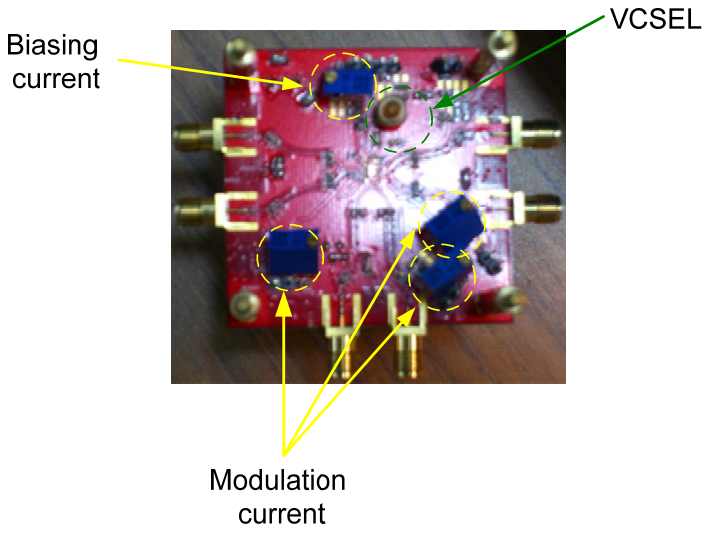


Figure 4-8 Top view of PCB

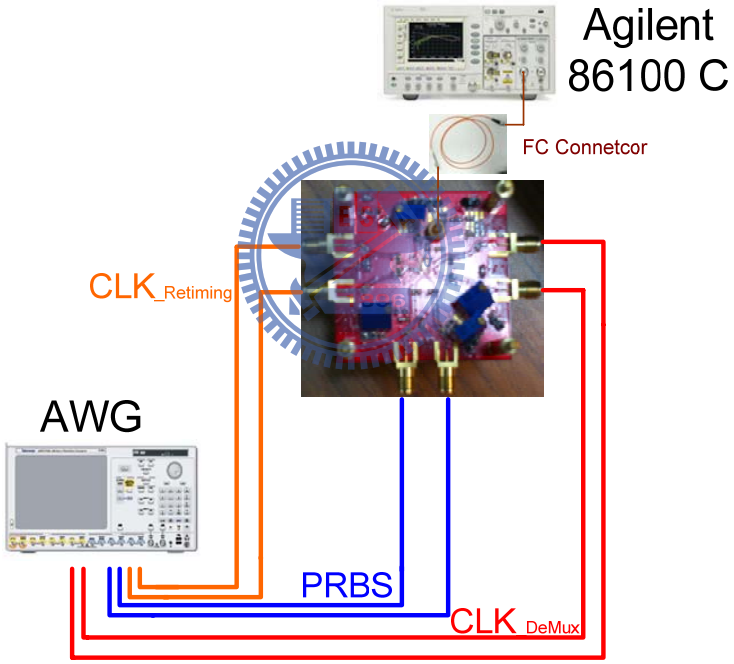


Figure 4-9 Optical measurement setup

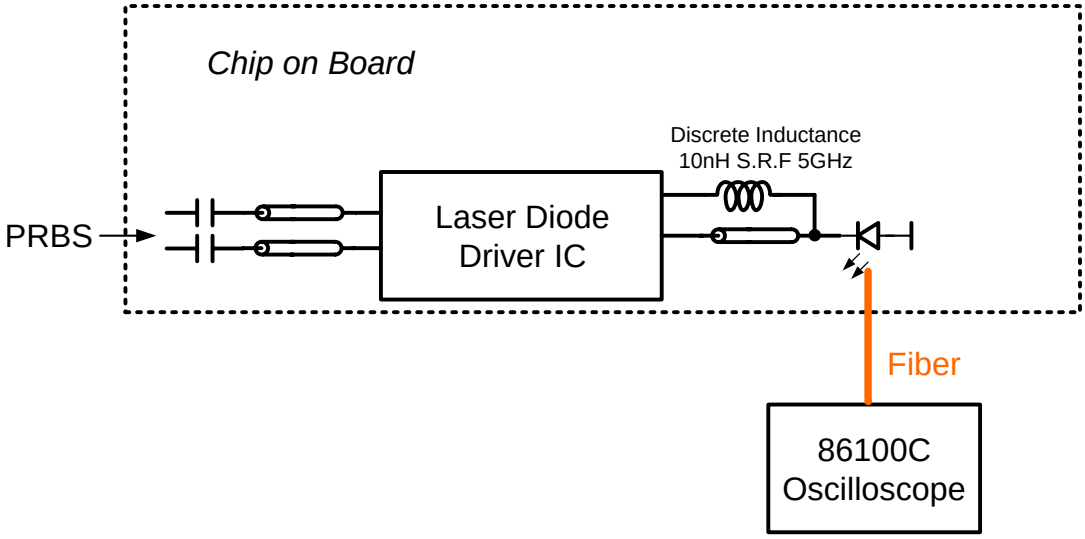


Figure 4-10 The output network of optical measurement PCB

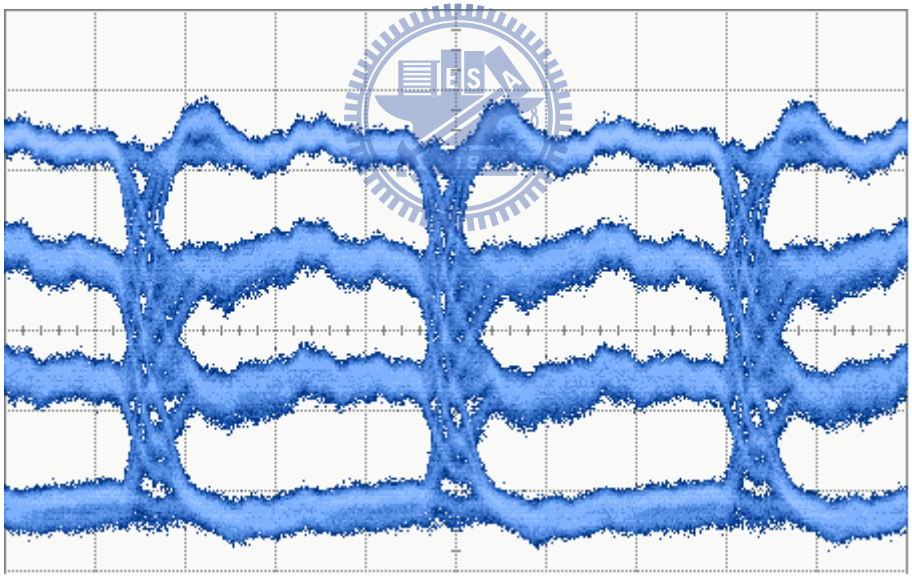


Figure 4-11 Optical eye-diagram of 1Gbps

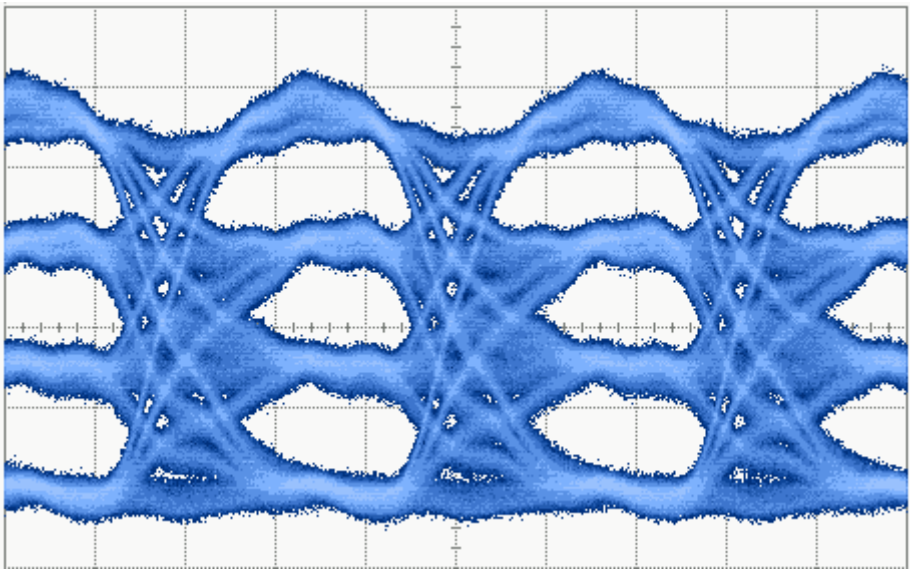


Figure 4-12 Optical eye-diagram of 2Gbps

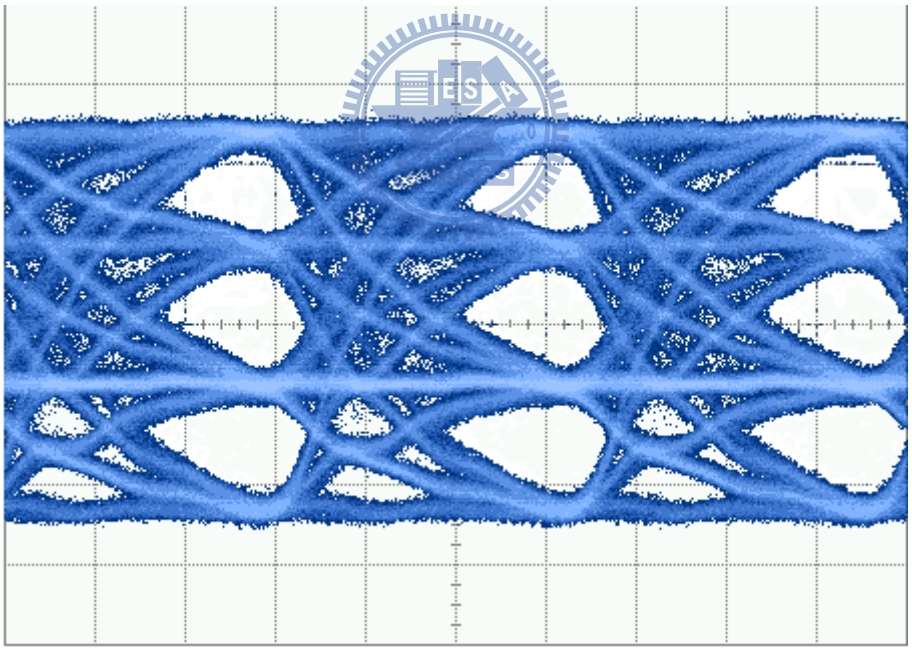


Figure 4-13 Optical eye-diagram of 3Gbps

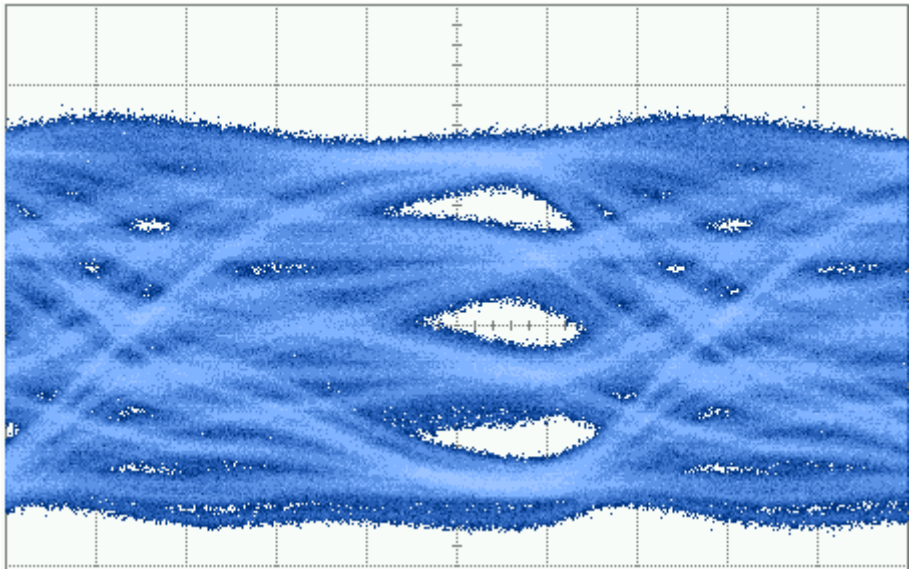


Figure 4-14 Optical eye-diagram of 4Gbps

4.4 Summary of Experimental Results

Power distribution

The total power consumption is about 200mW and the percentage of each circuit block is shown in Figure 4-15. Since there are three pre-drivers paths with pre-emphasis, they consume about 50% of total power consumption. The active back-termination consumes 9.72mW in the condition of 10mA modulation current. Therefore we can figure out that the power reduction of output stage compared with passive load laser diode driver output stage is about 23% by the following equation (1.8x10-9.72)/(20x1.8).

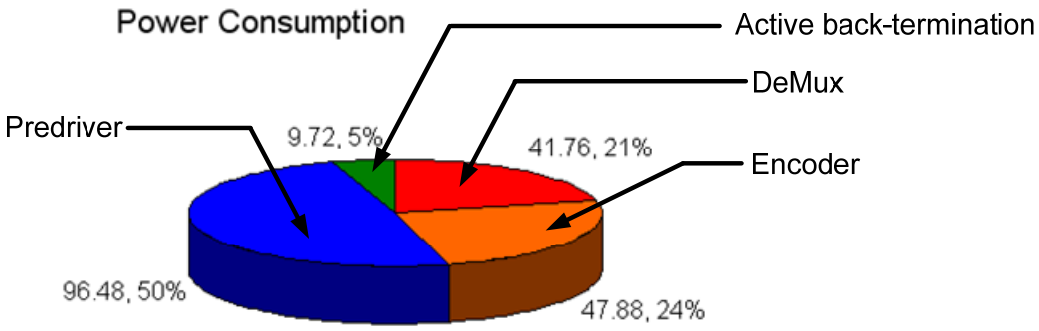


Figure 4-15 Power distribution

Benchmark

Source	JSSC(2000) [8]	ASSCC(2005) [9]	This work
Technology	300nm	180nm	180nm
Supply	3V	1.8V	1.8V
Data Type	4PAM	2/4PAM	4PAM
Data Rate	8Gbps	5/10Gbps	10Gbps** 4Gbps***
Modulation Current	8mA	12mA	10mA
Chip Area	N/A	1.1x1.2mm^2	1.6x0.8mm^2
Power	350mW*	183.2mW*	200mW

*Without Pre-driver **Simulation ***Measurement

Table 4-1 Benchmark

Chpater5

Conclusion

5.1 Conclusion

In this thesis, we propose a 4-PAM VCSEL driver which operates at multi-Gbps. Its features are summarized in the following statement:

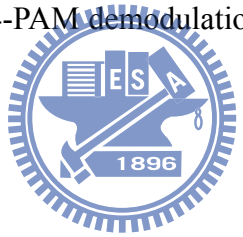
1. Pulse amplitude modulation is adopted; hence the bandwidth is used efficiency.
2. Pre-emphasis technique compensates the high frequency degradation of the bandwidth of transmitter.
3. A novel active back-termination based on regulated cascode configuration is proposed for impedance matching.
4. Power consumption of output stage is reduced by about 20% in this work.

5.2 Future Work

After this work, we can combine it with a high speed serializer to achieve decades-Gbps data transmission with the same process. However, there is an important issue we neglect in this work, the optical power is affected by temperature

and aging while the VCSELs are in real applications. In the 2-PAM VCSEL drivers, there are only two different signal amplitudes, high and low, if we want to adjust the optical power with the adverse influences; we just need to detect the low and high magnitude. With enough information of the transmitting optical power, we can ameliorate optical power by adjusting modulation current or biasing current, namely, the unwanted effects might be solved with two additional control loops. However, in this work, we adopt 4-PAM signaling which means that four signal levels needed to be adjusted. It is obviously that compare 2-PAM and 4-PAM systems, the latter needs more complicated control loops and more detection mechanisms to overcome temperature and aging issues.

In this thesis, we do not measure the BER, since we do design a 4-PAM optical receiver which is provided with 4-PAM demodulation function. Therefore, we are not capable of BER test.



References

[1] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw-Hill, 2003

[2] E. Säckinger, *Braodband Circuits for Optical Communication*, John Wiley & Sons, Mar. 2005.

[3] H. Ransijn, G. Salvador, D. D. Daugherty, and K. D Gaynor, "A 10-Gb/s Laser /Modulator Driver IC with a Dual-Mode Actively Matched Output Buffer," *IEEE J. Solid-State Circuits*, vol. 36, no. 9, pp. 1314-1320, Sept. 2001.

[4] S. Galal and B. Razavi, "10 Gb/s limiting amplifier and laser/modulator driver in 0.18μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138-2146, Dec. 2003.

[5] S. Morely, "A 3V 10.7Gb/s Differential Laser Diode Driver with Active Back-Termination Output Stage," *ISSCC Dig. Tech. Papers*, pp. 220-221 Feb. 2005.

[6] E. Ayranci, K. Christensen, and P. Andreani, "45% Power Saving in a 0.25μm BiCMOS 10 Gb/s 50Ω-Termination Packaged Active-Load Laser Driver," *ISSCC Dig. Tech. Papers*, pp. 552-553, Feb. 2007.

[7] D.-U. Li, C.-M. Tsai "A 10 Gb/s Burst-Mode/Continuous-Mode Laser Driver with Current-Mode Extinction-Ratio Compensation Circuit," *ISSCC Dig. Tech. Papers*, pp. 912-914, Feb. 2006.

[8] R. Farjad-Rad, C.-K Ken Yang, M. Horowitz, and T. Lee. "A 0.4μum CMOS 10 Gb/s 4-PAM Pre-Emphasis Serial Link Transmitter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 580-585, May 1999.

[9] C.-H. Lin and S.-J, Jou “A 4/2 PAM Pre-emphasis Transmitter with Combined,” *ASSCC*, pp. 189-192, Nov. 2005.