國 立 交 通 大 學

電子工程學系 電子研究所碩士班

碩 士 論 文

應用倍頻取樣相位偵測器
之鎖相迴路設計

Phase-Locked Loop Design with Double
Sampling Phase Detector

研 究 生：黃國爵　　Guo-Jue Huang

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

共同指導：溫文燊　博士　　Dr. Wen-Shen Wuen

中 華 民 國 九 十 七 年 六 月

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摘要

本論文提出應用倍頻取樣相位偵測器之鎖相迴路設計。倍頻取樣相位偵測器藉由加倍鎖相迴路之迴路頻寬降低鎖定時間，亦使參考頻雜訊移往高頻來降低參考頻雜訊。在系統分析方面，建立了一鎖相迴路使用倍頻取樣相位偵測器之線性模型。在驗證降低鎖定時間與參考頻雜訊的抑制方面，建立了 Verilog-AMS 鎖相迴路使用倍頻取樣相位偵測器與一般相位偵測器之暫態模型。在電路設計方面，設計一鎖相迴路可操作在倍頻取樣相位偵測器或一般相位偵測器模式，輸出頻率切換在 2.88 兆赫茲與 2.304 兆赫茲。在模擬結果中，鎖相迴路之鎖定時間可以降低50% 在30ppm 的輸出頻率精準度，參考頻雜訊降低16dB且被移往倍頻。

Phase-Locked Loop Design with Double Sampling Phase Detector

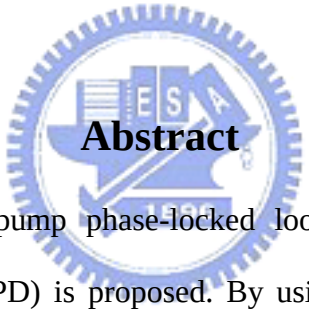
Student：Guo-Jue Huang Advisor : Dr. Kuei-Ann Wen

Co-advisor : Dr. Wen-Shen Wuen

Department of Electronics Engineering

Institute of Electronics

National Chiao-Tung University



Abstract

In this thesis, a charge-pump phase-locked loop (PLL) design with double sampling phase detector (DSPD) is proposed. By using the double sampling phase detector, the PLL loop bandwidth is doubled to obtain the fast settling time and meanwhile shift the reference spur to higher frequency to suppress the reference spur. For system analysis, a third-order charge-pump PLL with DSPD linear model is developed. Verilog-AMS charge-pump PLL timing models with DSPD and conventional phase detector (PD) are developed to verify the fast settling time and reference spur suppression. A 2.304 GHz/ 2.88GHz charge-pump PLL with two operation modes, DSPD mode and conventional PD mode, is designed. From the simulation results, the settling time is reduced 50% in 30ppm frequency accuracy and the reference spur is suppressed 16dB.

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黃國爵

2008 年 6 月

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Chapter 1 Introduction

1.1 Motivation

In modern wireless communication systems, a frequency synthesizer in RF transceivers generate local oscillator (LO) signals for transmitter up conversion and receiver down conversion as shown in Figure 1.1. As multimode transceivers are integrated, the frequency synthesizer needs fast settling LO signals to provide seamless connectivity between different systems for mobile users. For example the requirement of the LO signal hopping time between WiMax and WiFi is limited in 10usec [1]. Frequency synthesizers are widely implemented by phase-locked loop technique and the settling time of the PLL-based frequency synthesizer is sensitive to the PLL loop bandwidth. PLLs with wide loop bandwidth can achieve fast settling time but the flowing large reference spur appearing at the upper and lower sideband will mix the interference (Interferer) signal to degrade the SNR of the desired signal, as shown in Figure 1.2. Hence for the PLL-based frequency synthesizer design, the requirement for fast settling and low reference spur is still a design issue. In this thesis, a double sampling technique is proposed to double the loop bandwidth to achieve fast settling and furthermore suppress the reference spur.

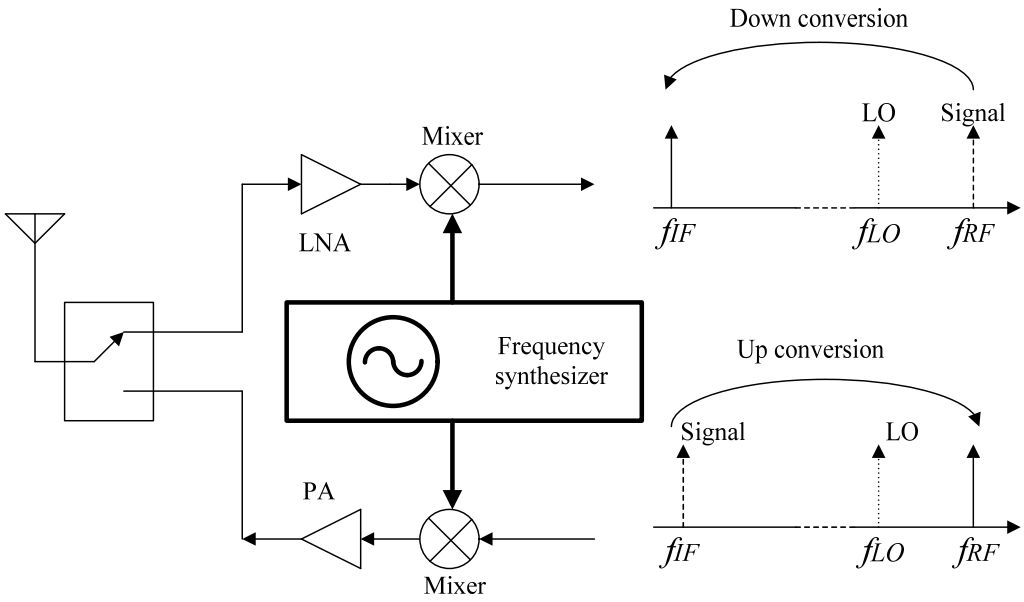


Figure 1.1 The typical transceiver architecture.

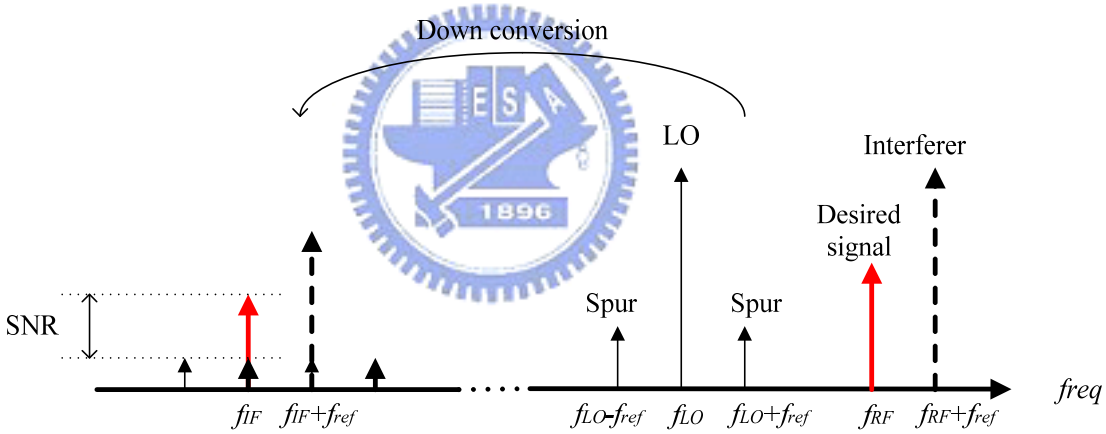


Figure 1.2 Effect of reference spurs of LO signal

1.2 Phase-Locked Loop

A block diagram of a phase-locked loop system is shown in Figure 1.3. The elements of the system are a phase detector (PD), a loop filter, a voltage control oscillator (VCO) and a feedback divider. For conventional charge-pump phase-locked loop, the phase detector is implemented by a phase frequency detector (PFD) and a charge pump (I_{CP}) as shown in Figure 1.4. The PFD samples the phase difference of

the f_{ref} and f_{out_N}, and produces sampling (Up/Down) signal pulse with pulse width proportional to the phase difference to control the charge pump switch. According to the sampling pulses the charge pump injects the average current in the loop filter every reference cycle. Hence, the phase difference of the conventional PD is sampled at the rate of the reference frequency.

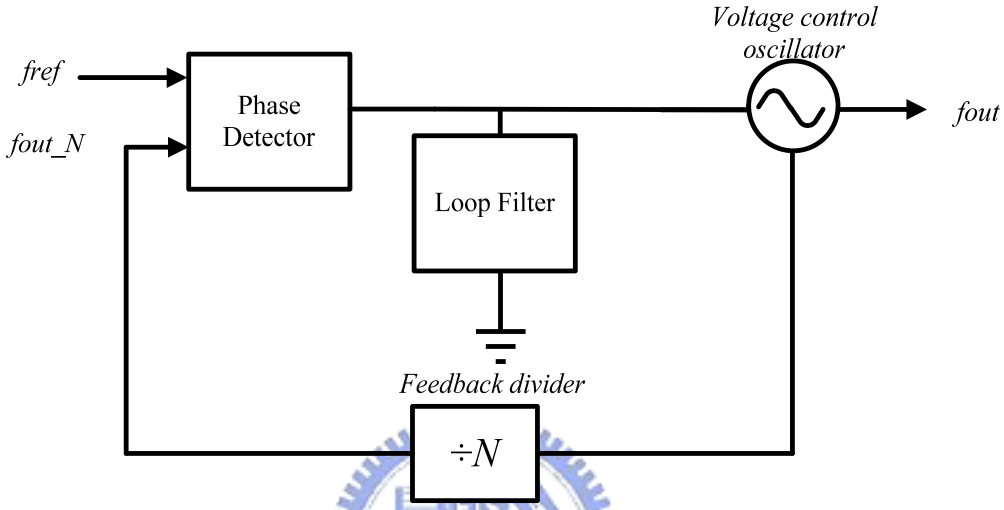


Figure 1.3 Phase-locked loop.

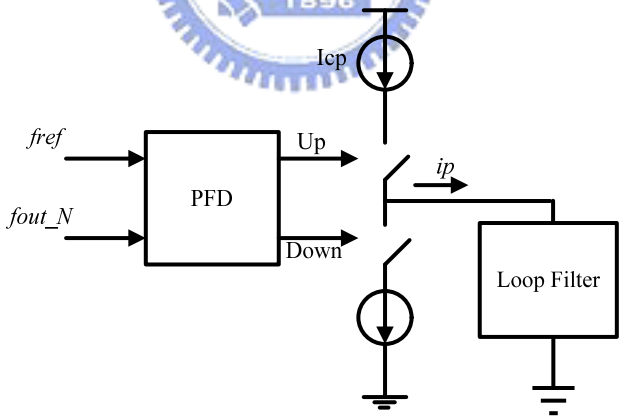


Figure 1.4 Phase detector of the charge-pump phase-locked loop

A common solution for PLL design to achieve both fast settling and low reference spur is the variable loop bandwidth technique. In this technique, the PLL works with the wide loop bandwidth in tracking state and with the narrower loop bandwidth in locked state. Figure 1.5 shows the dual-mode PLL [2] to achieve the variable loop

bandwidth. In PLL tracking state, the switches (S1, S2) are shorted and more charges are injected in to the loop filter to reduce the settling time while the switches (S1, S2) are opened when in locked state. However the PLL switching between two different states needs a switch (S3) to change the loop filter and the parasitic capacitance in the switches (S1 ,S2 ,S3) create unwanted current injected in to the loop filter during the discontinuity switching between different loop bandwidths and may cause the PLL to lose lock.

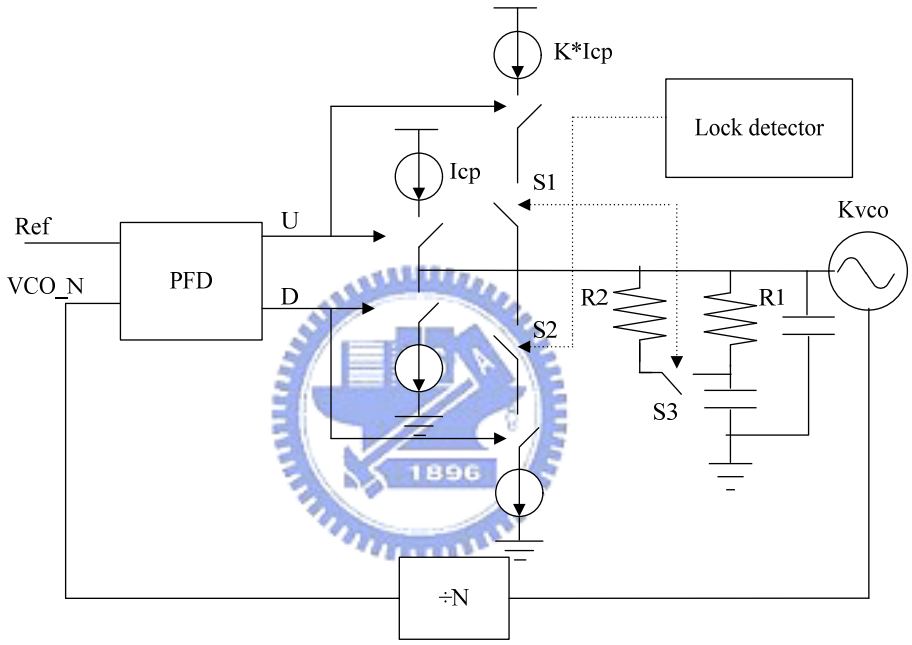


Figure 1.5 The dual-mode PLL.

1.3 Linear Phase-Locked Loop model

A typical charge-pump phase-locked loop can be modeled as a linear system, as shown in Figure 1.6. The K_{PD} is the phase detector gain and in the charge-pump PLL. The VCO is modeled as an integrator with a gain of K_{VCO} (rad/s). The loop filter is modeled with a transfer function $Z_{LF}(s)$. The feedback divider is modeled as a constant N.

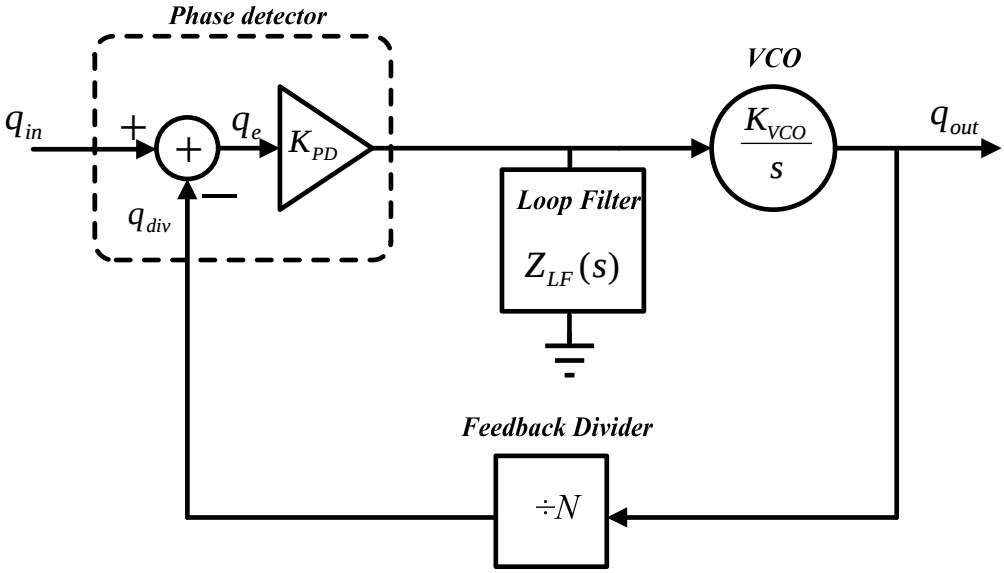


Figure 1.6 Linear model of the charge-pump phase-locked loop

1.3.1 Stability Analysis

In a third order charge-pump PLL with conventional PD, the loop filter is formed by one resistor and two capacitors as shown in Fig1.7. The loop filter creates one zero and one pole. The conventional PD gain is $K_{CON\_PD}=I_{CP}/2\pi$, and I_{CP} is the charge-pump current

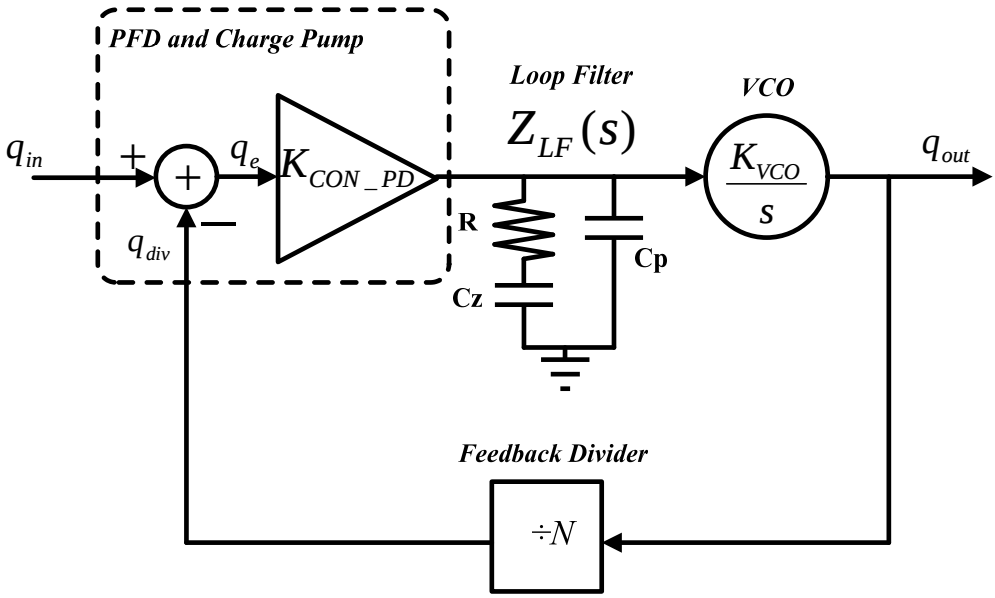


Figure 1.7 Linear model of the third order charge-pump phase-locked loop

For analysis of the stability, the system phase margin is introduced. In the third order charge-pump PLL, the transfer function of the open-loop transfer function is

$$\frac{q_{div}}{q_e} = G(s)H(s) = \frac{K_{CON\_PD}K_{VCO}}{s^2 C_p N t_z}\left(\frac{1+st_z}{1+st_p}\right) \tag{1.1}$$

where $G(s)=K_{CON\_PD}K_{VCO}Z_{LF}(s)/s$ is the forward-loop transfer function, $H(s)=1/N$ is the reverse-loop transfer function and $t_z = RC_z$ and $t_p = R(C_z \| C_p)$ define the pole and zero. The frequency response of the gain of the open loop transfer function is

$$\frac{q_{div}}{q_e}|_{s=jw} = \frac{-K_{CON\_PD}K_{VCO}}{w^2 C_p N t_z}\left(\frac{1+jwt_z}{1+jwt_p}\right) \tag{1.2}$$

From equation (1.2), the unity gain of the open-loop transfer function can be derived as follow

$$\left|\frac{q_{div}}{q_e}\right|_{s=jw_u} = 1 \rightarrow w_u = w_{BW\_CON} = \frac{K_{CON\_PD}K_{VCO}R}{N}\frac{b-1}{b} \tag{1.3}$$

where $b=t_z/t_p$. The unity gain is defined as the loop bandwidth (w_{BW_CON}) of the PLL. The frequency response of the phase of the open-loop transfer function is

$$f(w) = -180^{\circ} + \tan^{-1}(wt_z) + \tan^{-1}(wt_p) \tag{1.4}$$

From equation (1.4), the frequency corresponding to the maximum phase response can be defined from

$$\frac{df(w)}{dw} = 0 \tag{1.5}$$

then the relation between pole, zero and frequency corresponding to the maximum phase response can be expressed as

$$w = 1/\sqrt{t_z t_p} \tag{1.6}$$

The phase margin (*PM*) is defined as

$$PM = 180^{\circ} + f\left(w = w_{BW\_CON}\right) = \tan^{-1}(w_{BW\_CON} t_z) + \tan^{-1}(w_{BW\_CON} t_p) \qquad (1.7)$$

From equation (1.6) and (1.7), to design the third order charge-pump PLL system with the maximum *PM*, the relation between the pole, zero and loop bandwidth must satisfy the equation (1.8).

$$w_{BW\_CON} = 1/\sqrt{t_z t_p} \qquad (1.8)$$

The maximum *PM* can be expressed as a function of the ratio between pole and zero, can be shown as

$$PM_{\max} = \tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right) \qquad (1.9)$$

And the bode plot of the open loop transfer function is shown as Figure 1.8

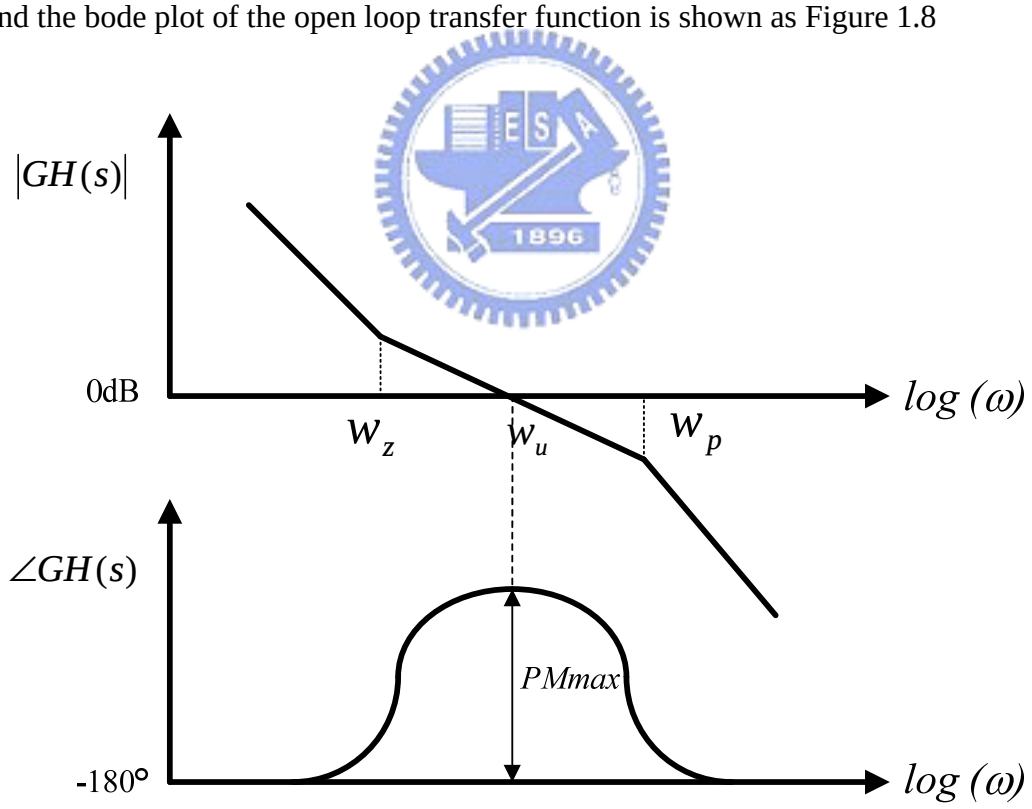


Fig1.8 Bode plot of the third order charge pump PLL transfer function.

1.3.2 Settling Time

For the transient behavior of the third order charge-pump PLL, assuming the ratio between pole and zero is large, the third order charge-pump PLL will act like the behaviors of the second order charge-pump PLL. The settling time can be approximated as [3]

$$T_{settling} \approx \frac{-\ln\left(\frac{tol}{f_2 - f_1}\sqrt{1-V^2}\right)}{Vw_n}. \tag{1.10}$$

The initial frequency is f_1 and the final frequency is f_2. The final frequency accuracy is *tol* and the natural frequency and damping ratio are given by

$$w_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC_z}} \quad V = \frac{1}{2}t_z\sqrt{\frac{K_{PD}K_{VCO}}{NC_z}} \tag{1.11}$$

Equation (1.10) can be expressed as

$$T_{settling} \approx \frac{-2\ln\left(\frac{tol}{f_2 - f_1}\sqrt{1-V^2}\right)}{w_{BW\_CON}} \quad w_{BW\_CON} = \frac{K_{PD}K_{VCO}R}{N} \tag{1.12}$$

According to the equation (1.12), increasing the loop bandwidth can shorten the PLL settling time.

1.3.3 Reference Spur

The periodic ripples on the control voltage of the VCO will modulate the VCO to generate the reference spur tone at the offset frequency f_{ref} from the carrier frequency. To estimate this effect, assume the VCO control voltage appears as a periodic function with a DC offset and expressed as

$$V(t) = V_t + A_m \cos(w_{ref} t) \tag{1.13}$$

The VCO output can be modeled as

$$V_{out}(t) = V_o \sin(w_{free} t + \int K_{vco} V(t) dt) \tag{1.14}$$

The magnitude of the reference spurs tone can be derived as follows

$$\begin{aligned} V_{out} &= V_o \sin(w_{free} t + K_{VCO} \int V_t dt + K_{VCO} \int A_m \cos(w_{ref} t) dt) \\ &= V_o \sin(w_{out} t + \mathbf{V}f \sin(w_{ref} t)) \\ &= V_o \left[\sin(w_{out} t) \cos(\mathbf{V}f \sin(w_{ref} t)) + \cos(w_{out} t) \sin(\mathbf{V}f \sin(w_{ref} t)) \right] \end{aligned} \tag{1.15}$$

where $w_{out} = w_{free} + K_{VCO} V_t$ and $\mathbf{V}f = \dfrac{K_{VCO} A_m}{w_{ref}}$

Assume $\mathbf{V}f$ is small, i.e., $\mathbf{V}f = p/2$, in equation (1.15)

$$\cos(\mathbf{V}f \sin(w_{ref} t)) = 1 \tag{1.16}$$

and

$$\sin(\mathbf{V}f \sin(w_{fref} t)) \approx \mathbf{V}f \sin(w_{ref} t) \tag{1.17}$$

Equation (1.15) can be expressed as

$$\begin{aligned} V_{out} &= V_o \left[\sin(w_{out} t) + \cos(w_{out} t) \mathbf{V}f \sin(w_{ref} t) \right] \\ &= V_o \left[\sin(w_{out} t) - \frac{\mathbf{V}f}{2} \sin(w_{out} - w_{ref}) + \frac{\mathbf{V}f}{2} \sin(w_{out} + w_{ref}) \right] \end{aligned} \tag{1.18}$$

From equation (1.18), the reference spur can be observed at the $w_{out} \pm w_{ref}$. The amplitude ratio between the reference spur and the carrier can be shown as

$$\frac{A_{reference\ spur}}{A_{carrier}} = \frac{\Delta f}{2} = \frac{1}{2}\frac{K_{VCO}A_m}{w_{ref}} \tag{1.19}$$

Equation (1.19) suggests that lower the VCO gain (K_{vco}) or the amplitude (A_m) by reducing charge-pump current can suppress the reference spur but the PLL loop bandwidth will degrade.

For both settling time and reference spur improvement, increasing the reference frequency is a way to extent the loop bandwidth and suppress the reference spur. In conventional PD the sampling rate is defined as the same as the reference frequency and the reference frequency is limited by the applications (channel bandwidth) and crystal. In this thesis, a phase detector doubling the phase difference sampling rate without changing the reference frequency is proposed to improve both settling time and reference spur performance.

1.4 Thesis Organization

The thesis focuses on the design of phase-locked loop for fast settling and low reference spur. Chapter 2 presents a double sampling technique implemented by doubled sampling phase detector (DSPD). Then linear model of the DSPD is developed and the stability, settling time and reference spur analysis of the charge-pump PLL with DSPD is discussed.

Chapter 3 introduces Verilog-AMS timing model for the proposed charge-pump PLL design. The timing model with non-idea effect is built to verify the settling time reduction and the reference spur suppression. The comparison of the proposed PLL with DSPD to that with conventional phase detector is performed through the Verilog-AMS timing models.

In Chapter 4 presents the implementation of the charge-pump PLL with DSPD and conventional phase detector. The simulation and measurement results will be discussed.

Chapter 5 comes out the conclusions and the future work.

Chapter 2 Double Sampling Phase Detector

2.1 Double Sampling Technique

As discussion in Chapter 1, the settling time of the phase-locked loop is determined by the loop bandwidth of the PLL. According to the equation (1.12) and (1.19), increasing the reference frequency to raise the sampling rate of phase difference of the phase detector can improve the settling time and reference spur performance. In order to increase sampling rate of the phase detector without changing the reference frequency, the double sampling technique is proposed

2.1.1Settling time

The proposed double sampling technique for fast settling can be illustrated in Figure 2.1. Figure 2.1 (a) and Figure 2.1 (b) show the variation of the VCO control voltage (Vt) during the PLL frequency tracking without and with double sampling technique. In Figure 2.1 (a), the control voltage varies once in one reference cycle. On the other hand, using double sampling technique the control voltage varies twice in one reference cycle as shown in Figure 2.1(b). Comparing the Figure 2.1 (a) and Figure 2.1 (b), the variation of the control voltage with double sampling is more than that without double sampling in one reference cycle. Hence the settling time of the PLL can be reduced by employing double sampling technique.

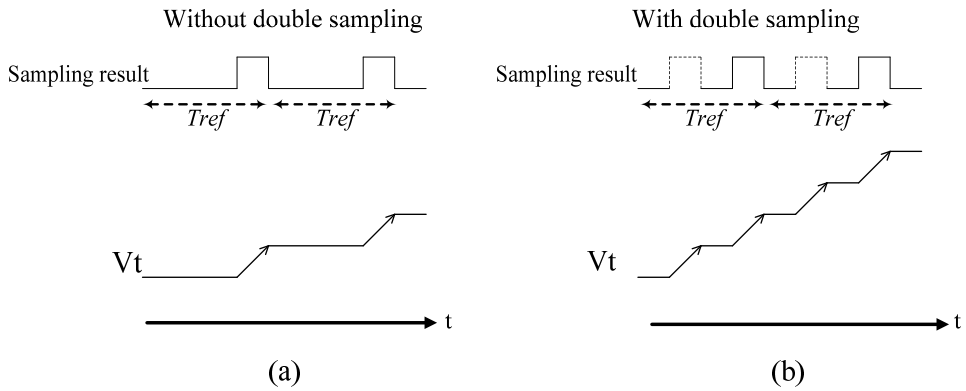


Fig 2.1 Illustration of the settling time
(a) Without double sampling. (b) With double sampling.

2.1.2Reference Spur

Figure 2.2 illustrates the effect of the reference spur on the VCO output spectrum without and with double sampling technique.

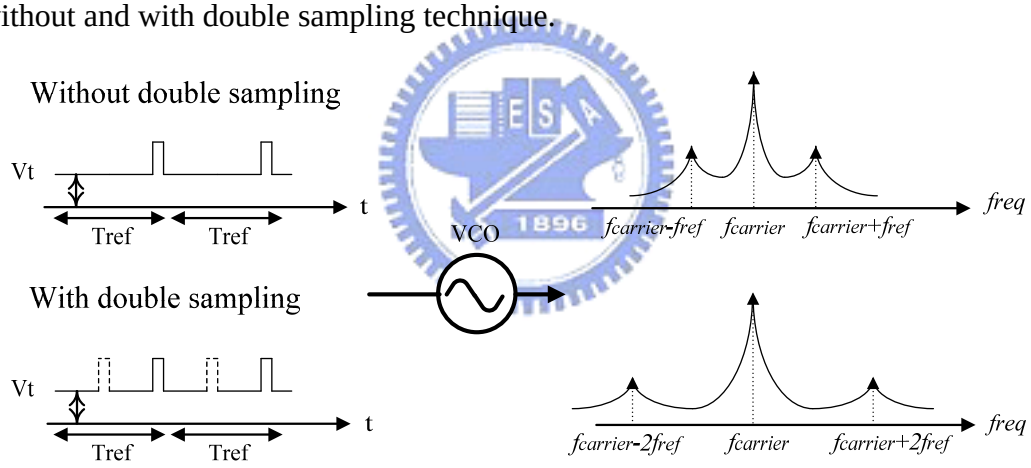


Fig 2.2 Illustration of the reference spur effect on the VCO output spectrum without double sampling technique and with double sampling technique.

As shown in Figure 2.2, using the double sampling technique the frequency of the periodic control voltage ripples can be doubled and the reference spur will be shift to two times of the reference frequency ($2f_{ref}$) away from the carrier. According to the equation (1.19), the amplitude ratio between the carrier and the reference spur is an inverse proportion to the sampling rate (f_{ref}) of the phase detector. Therefore, the

reference spur could be suppressed as the reference spur shift far away from the carrier frequency.

2.2 Double Sampling Phase Detector Architecture

The PLL with double sampling technique to achieve fast settling and low reference spur is implemented by replacing the conventional phase detector (CON_PD) to the double sampling phase detector (DSPD) as shown in Figure 2.3. The DSPD is built with two common mode logic divide-by-two circuits (CML_D2), four PFDs, two charge pumps with the same current (Icp=Icp1=Icp2), two four-input OR gates and two compensation circuits (COM_ckt).

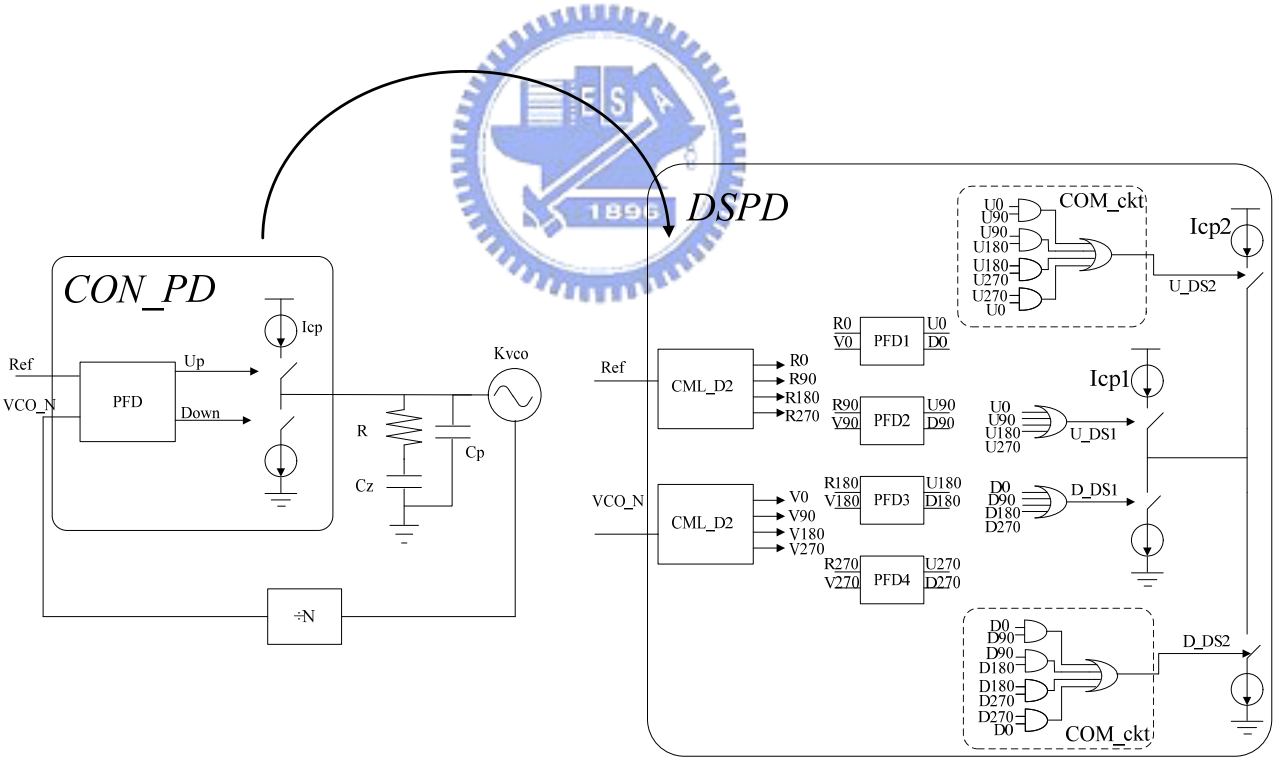


Figure 2.3 The DSPD replaces the conventional PD in the PLL to achieve double sampling technique.

The conventional PD injects the average current proportional to the phase difference in the loop filter. The linear gain of the conventional PD (K_{CON_PD}) architecture can be defined as

$$\overline{I_{CON\_PD}} = \frac{I_{CP} q_e}{2p} = K_{CON\_PD} q_e \tag{2.1}$$

Comparing to the conventional PD, the DSPD injects two times of the average current proportional to the phase difference in the loop filter and the control voltage varies twice in one reference cycle. The linear gain of the DSPD architecture (K_{DSPD}) can be defined by the detail DSPD circuit operation discussion according to the phase difference as follows.

2.2.1 Phase Difference Smaller Than π

Figure 2.4 shows the timing diagram of the signals in the DSPD with two input signals (Ref and VCO_N) with phase difference (θ_e) is smaller than π. Each CML_D2 will produce four half-frequency and quadrature-phase output signals (R0~R270 and V0~V270). Then four phase frequency phase detectors sample the phase difference between the signals (R0/V0, R90/V90, R180/V180, R270/V270) of two CML-D2s in order to generate four sampling results (U0, U90, U180, U270). Each sampling result is proportional to the phase difference θ_e. The OR gate combines the U0, U90, U180 and U270 to create one signal pulse, U_DS1 whose total pulse width is two times of the phase difference θ_e in one reference cycle. The output signal of the COM_ckt (U_DS2) will be always at low voltage in this region. Then the charge pump1 (Icp1) will be turned on twice in one reference cycle and the charge pump2 (Icp2) will always be turned off. The linear gain of DSPD in this region can be defined from the average current injected in the loop filter in one reference cycle

$$\overline{I_{DSPD}} = \frac{I_{CP1}(2q_e)}{2p} = K_{DSPD}q_e \quad for \quad q_e < p \tag{2.2}$$

Because the charge pumps in DSPD are designed to be the same as the charge pump in the conventional PD. Equation (2.2) can be expressed as:

$$\overline{I_{DSPD}} = K_{DSPD}q_e = 2K_{CON\_PD}q_e \quad for \quad q_e < p \tag{2.3}$$

2.2.2 Phase Difference Larger Than π

Figure 2.5 shows the timing diagram of the signals in DSPD with two input signals (Ref and VCO_N) with phase difference ($q_e = p + q'_e$) is larger than π. As discussed in previous section, the OR gate will create the U_DS1 signal whose pulse width is $2p$. In addition, the COM_ckt will combine the (U0~U270) to create a signal pulse U_DS2 whose pulse width is proportional to q'_e. Therefore the charge pump1 will be always turned on and the charge pump2 will be turned on twice in one reference cycle. The average current injected in the loop filter in one reference cycle can be given as

$$\overline{I_{DSPD}} = \frac{I_{CP1}(2p) + I_{CP2}(2q_e^{'})}{2p} \tag{2.4}$$

Because of the same charge pump current (Icp=Icp1=Icp2). The linear gain of the DSPD can be defined from

$$\overline{I_{DSPD}} = \frac{I_{CP1}(2p) + I_{CP2}(2q_e^{'})}{2p} = \frac{2I_{CP}(p + q_e^{'})}{2p} = K_{DSPD}q_e = 2K_{CON\_PD}q_e \quad for \quad q_e > p \tag{2.5}$$

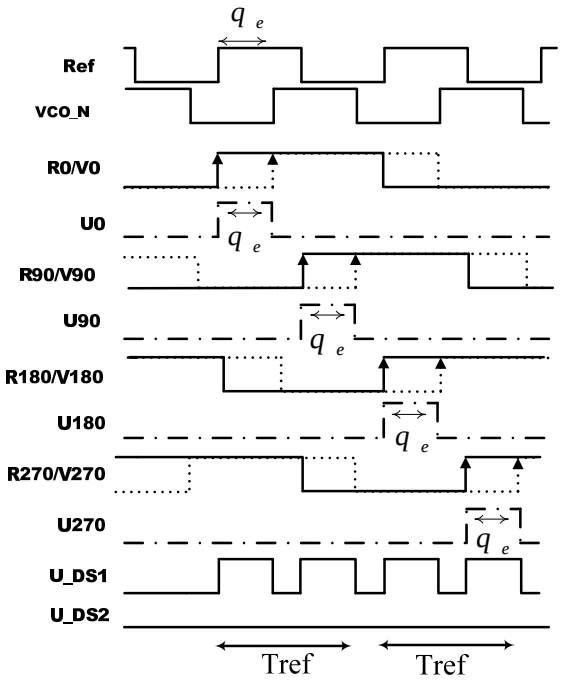


Figure 2.4 The timing diagram of the signals in DSPD with two input signal (Ref and VCO_N) phase difference (θ_e) is smaller than π.

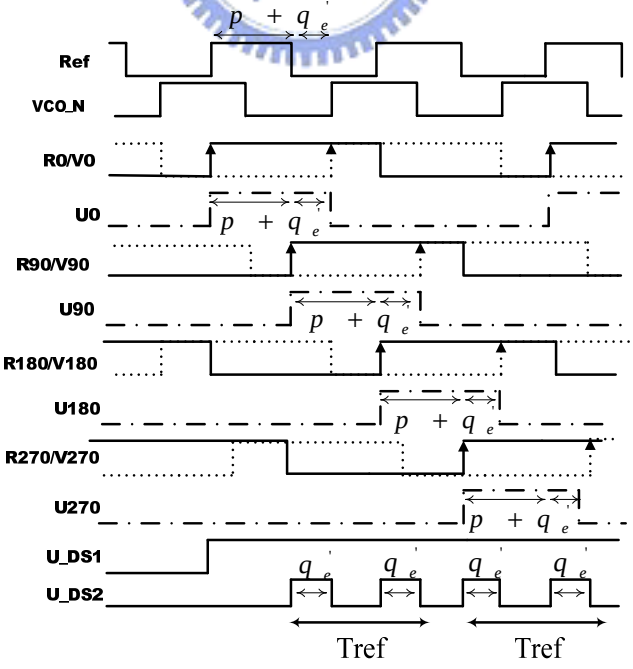


Figure 2.5 The timing diagram of the signals in DSPD with two input signal (Ref and VCO_N) phase difference ($q_e = p + q'_e$) is larger than π.

As the discussion, the linear gain of the double sampling phase detector can be defined from equation (2.3) and (2.5). The Figure 2.6 shows the average current and phase difference characteristic of the conventional PD and the double sampling phase detector. Comparing to the conventional PD, the linear gain of the double sampling phase detector is doubled.

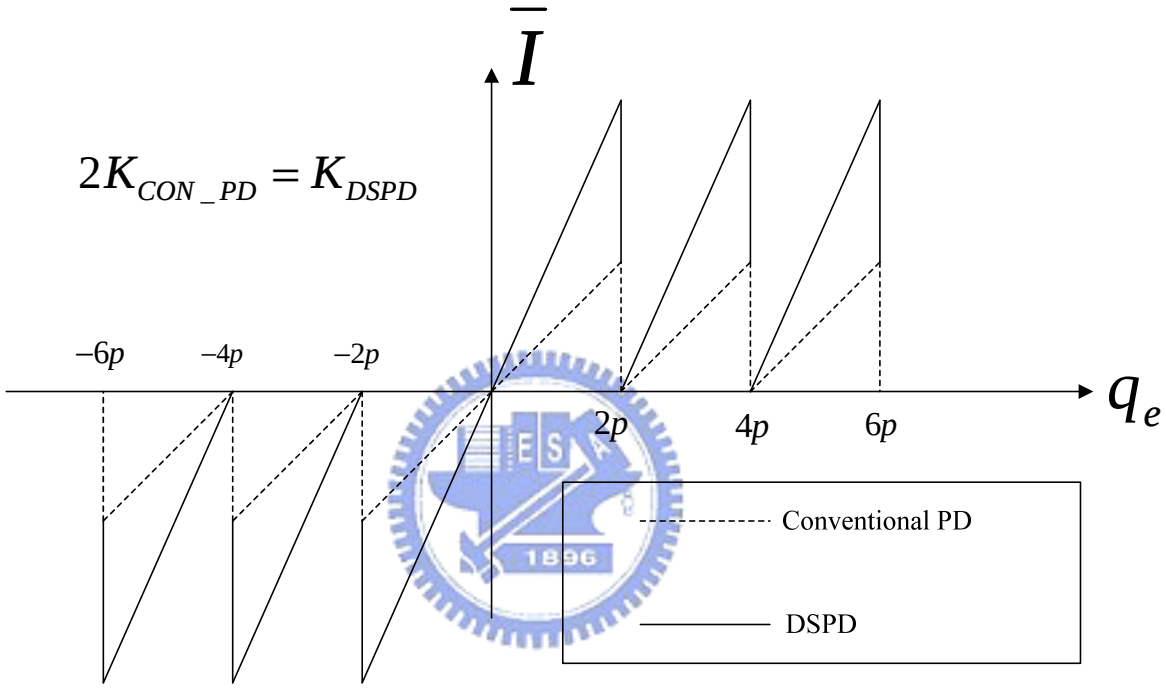


Figure 2.6 The average current and phase difference characteristic of the conventional PD and the double sampling phase detector.

2.3 Linear PLL Model with DSPD

The linear gain of the double sampling phase detector is doubled compared to the conventional PD. According to the equation (1.3), the loop bandwidth of the PLL with DSPD can be expressed as

$$w_{BW\_DS} = \frac{K_{DSPD}K_{VCO}R}{N}\frac{b}{b-1} = \frac{2K_{CON\_PD}K_{VCO}R}{N}\frac{b}{b-1} = \frac{K_{CON\_PD}K_{VCO}R}{N/2}\frac{b}{b-1} \quad (2.6)$$

Therefore the linear model of the DSPD PLL can be regarded as the linear model of the conventional PD PLL using the half feedback divider ratio (*N/2*) with double reference frequency as shown in Figure 2.7.

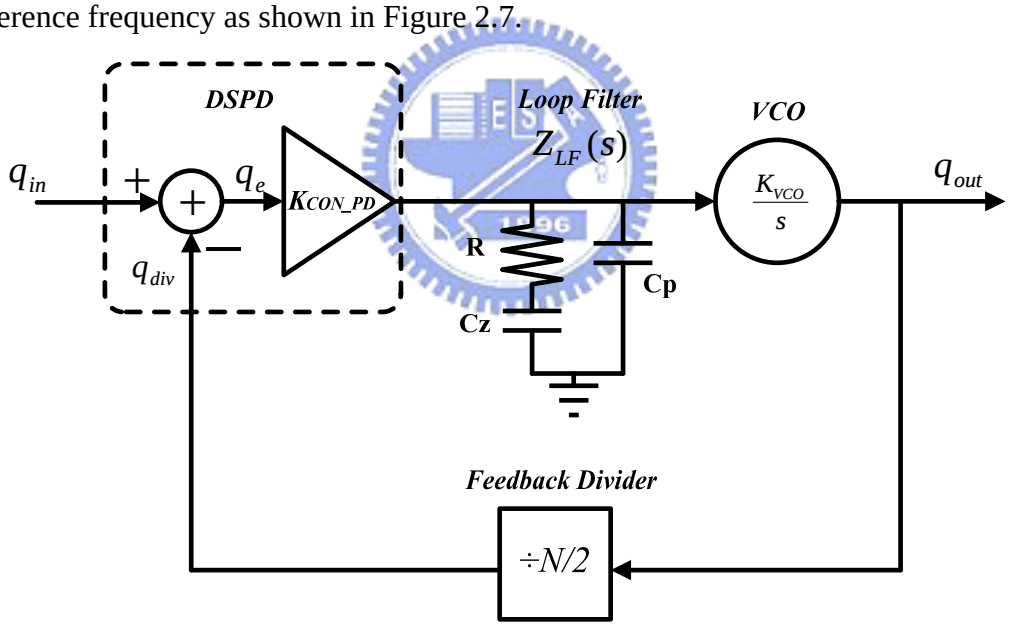


Figure 2.7 The linear model of the DSPD PLL.

2.3.1 Stability Analysis

As describe in Chapter 1, the phase margin of the third order charge-pump PLL can be designed by adjust the relation between loop filter and the loop bandwidth. For the same loop filter design, the PLL with DSPD will degrade the phase margin

because of the increase of loop bandwidth. The illustration of the phase margin degradation can be shown in Figure 2.8 and subsequently Table 2.1shows the phase margin degradation with different ratio of the pole and zero.

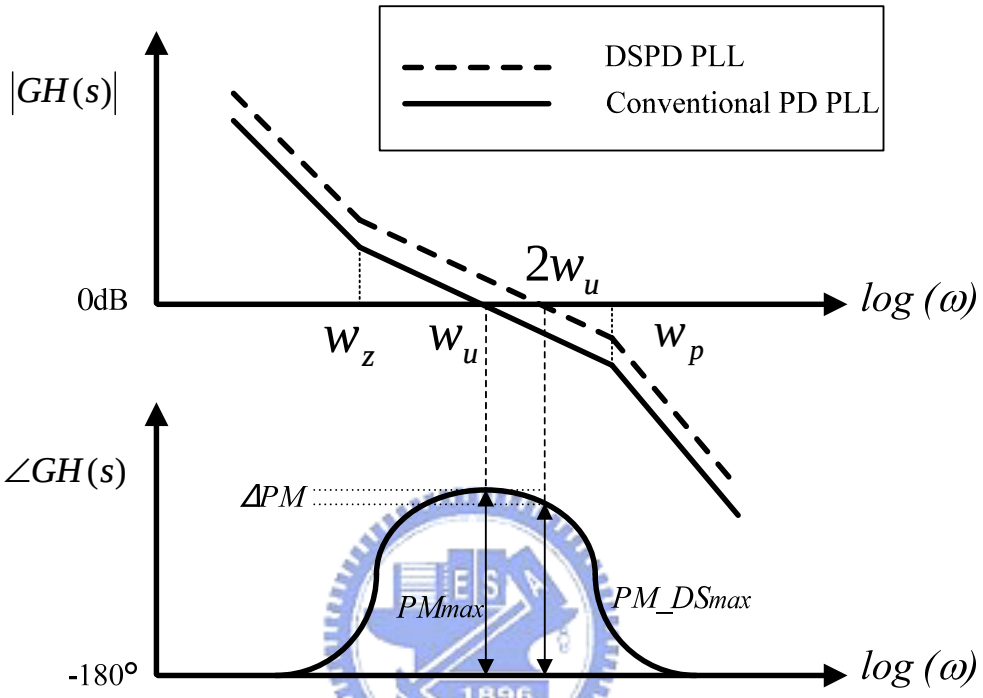


Figure 2.8 The illustration of the phase margin degradation of the DSPD PLL with the same loop filter design.

Table 2.1 The phase margin degradation with different ratio of the pole and the zero.

b	PM_CON	PM_DS	ΔPM
2.04	20°	18°	2°
3.00	30°	27.5°	2.5°
4.59	40°	36.6°	3.4°
5.82	45°	41.2°	3.8°
7.55	50°	45.8°	4.2°
10.06	55°	50.7°	4.3°
13.93	60°	55.6°	4.4°
32.16	70°	66.1°	3.9°
130.64	80°	77.7°	2.3°

To compensate the degradation of the phase margin, the modified loop filter design is proposed. In the conventional PD PLL, the maximum phase margin design satisfied the condition.

$$w_{BW\_CON} = 1/\sqrt{t_z t_p} = \sqrt{w_z w_p} \qquad w_{BW\_CON} = \frac{K_{CON\_PD} K_{VCO} R}{N} \frac{b}{b-1} \tag{2.7}$$

The maximum phase margin of the system can be given as

$$PM_{\max} = \tan^{-1}\left(\frac{b-1}{2\sqrt{b}}\right) \tag{2.8}$$

For DSPD PLL, the loop bandwidth is doubled,

$$w_{BW\_DS} = 2w_{BW\_CON} \,. \tag{2.9}$$

In order to achieve the maximum phase margin design, double the frequency of the pole and the zero can still satisfy equation (2.7).

$$2w_{BW\_CON} = w_{BW\_DSPD} = \sqrt{(2w_z)(2w_p)} \tag{2.8}$$

According equation (2.8), since the simultaneous double of the frequency of the pole and the zero, b is the same and the phase margin can be remained maximum phase margin. The illustration of the loop filter design with phase margin compensation for DSPD PLL is shown in Figure 2.9.

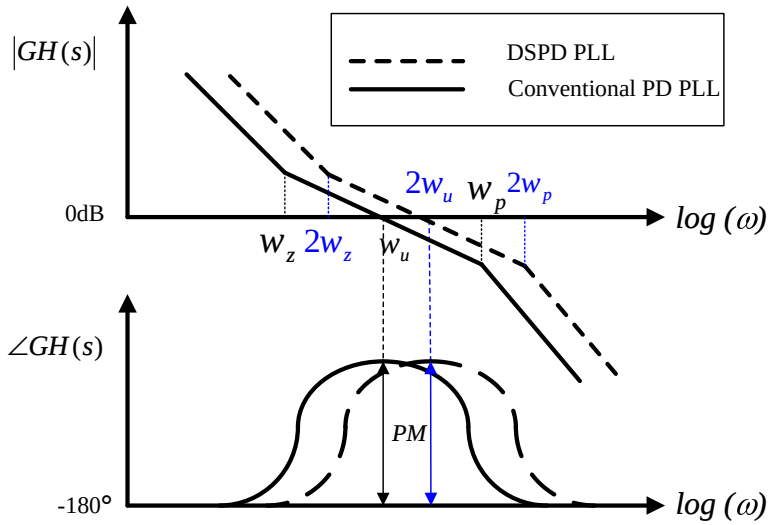


Figure 2.9 The illustration of the modify design of the loop filter for the phase margin compensation for DSPD PLL.

2.3.2 Settling Time

The approximated settling time of the conventional PD PLL can be given as

$$T_{settling\_conventional\_PD} \approx \frac{-2\ln\left(\frac{tol}{f_2 - f_1}\sqrt{1-V^2}\right)}{w_{BW\_CON}} \tag{2.10}$$

For the DSPD PLL, the loop bandwidth is doubled therefore the settling time can be reduced by using the double sampling phase detector.

2.3.3 Reference Spur

For the conventional PD PLL the amplitude ratio between the reference spur and the carrier can be calculated by the approximation equation as

$$\left(\frac{A_{spur}}{A_{carrier}}\right)_{CON\_PD} = \frac{1}{2}\frac{K_{VCO}A_m}{w_{ref}} \tag{2.11}$$

which A_m and ω_{ref} are the amplitude and the frequency of the periodic ripples on the VCO control voltage (the sampling rate of the phase detector). The periodic ripples is due to the non-ideal effects of the phase detector such as mismatch of the charge pump, the leakage current from the control voltage and the timing error of the phase detector. Assume ΔI represents the total current due to the non-ideal effects injected in to the loop filter. The amplitude of the control voltage ripples can be expressed as

$$A_m = \Delta I \times R \tag{2.12}$$

R is the resistance in the loop filter. Then equation (2.11) can be reformulated as equation (2.13) which is related to the loop bandwidth.

$$\left(\frac{A_{spur}}{A_{carrier}}\right)_{CON\_PD} = \frac{1}{2}\frac{w_{BW\_CON}}{w_{ref}}\frac{\Delta I}{I_{CP}}N \tag{2.13}$$

The loop bandwidth of the DSPD PLL is doubled and the linear model of the DSPD PLL can be regarded as the conventional PD PLL using half divider ratio (N/2) with double reference frequency ($2w_{ref}$). Because of the periodic ripples due to the non-ideal effects of the phase effect occur when the PLL is in the lock state, as described in previous section, the charge pump2 is turned off and only the charge pump1 is operated. Then the non-ideal current of the DSPD PLL can be assumed the same as that of the conventional PD PLL. The approximation equation of the ratio between the reference spur and the carrier can be expressed as

$$\left(\frac{A_{spur}}{A_{carrier}}\right)_{DSPD} = \frac{1}{2}\frac{w_{BW\_DSPD}}{2w_{ref}}\frac{\Delta I}{I_{CP}}\frac{N}{2} = \frac{1}{2}\frac{2w_{BW\_CON}}{2w_{ref}}\frac{\Delta I}{I_{CP}}\frac{N}{2} \qquad (2.14)$$

Comparing the equation (2.13) and (2.14), the reference spur can be suppressed about 6.02 dB by using double sampling phase detector even the loop bandwidth is doubled.

Chapter 3 System design and Verilog-AMS PLL Timing Model Verification

3.1 Phase Locked Loop System Design

Table 3.1 summarizes the loop parameter of the phase locked loop with the conventional phase detector. The VCO gain is 120 (MHz/V). The charge pump current is 100 uA. The feedback divider ratio is 128. In this work, the loop bandwidth and phase margin are chosen to be 60 kHz and 60°. Then the value of the components in the loop filter can be designed as R=4.33 kΩ, Cz= 2.28 nf, Cp= 176 pf.

Table3.1 The summary of the loop parameter of the phase locked loop with conventional phase detector.

Parameters	**Values**
Loop bandwidth	60 kHz
Phase margin	60°
VCO gain	120 MHz/V
Charge pump current	100uA
R	4.33 kΩ
Cz	2.28 nf
Cp	176 pf
Feedback divider ratio	128

The PLL using the double sampling phase detector needs to modify the loop filter design to compensate the phase margin degradation. According to the proposed loop filter modification in Chapter 2. Doubling the frequency of the pole and zero can remain the same maximum phase margin. Table 3.1 summarizes the loop parameters of the phase locked loop with the double sampling phase detector. As introduced in Chapter 2, the DSPD PLL can be regarded as conventional PD PLL with half divider ratio. The feedback divider ratio is 64. The charge pump current is 100 uA. The VCO gain is 120 (MHz/V) .Comparing to the conventional PD PLL, the loop bandwidth can achieve 120 kHz and phase margin remains 60°.

Table3.2 The summary of the loop parameter of the phase locked loop with double sampling phase detector.

Parameters	**Values**
Loop bandwidth	120 kHz
Phase margin	60°
VCO gain	120 MHz/V
Charge pump current	100uA
R	4.33 kΩ
Cz	1.14 *nf*
Cp	88 *pf*
Feedback divider ratio	64

Figure 3.1 shows the magnitude and phase response of the open loop transfer function for the conventional PD PLL with the loop filter design in Table 3.1 and the DSPD PLL with the compensational loop filter design in Table 3.2.

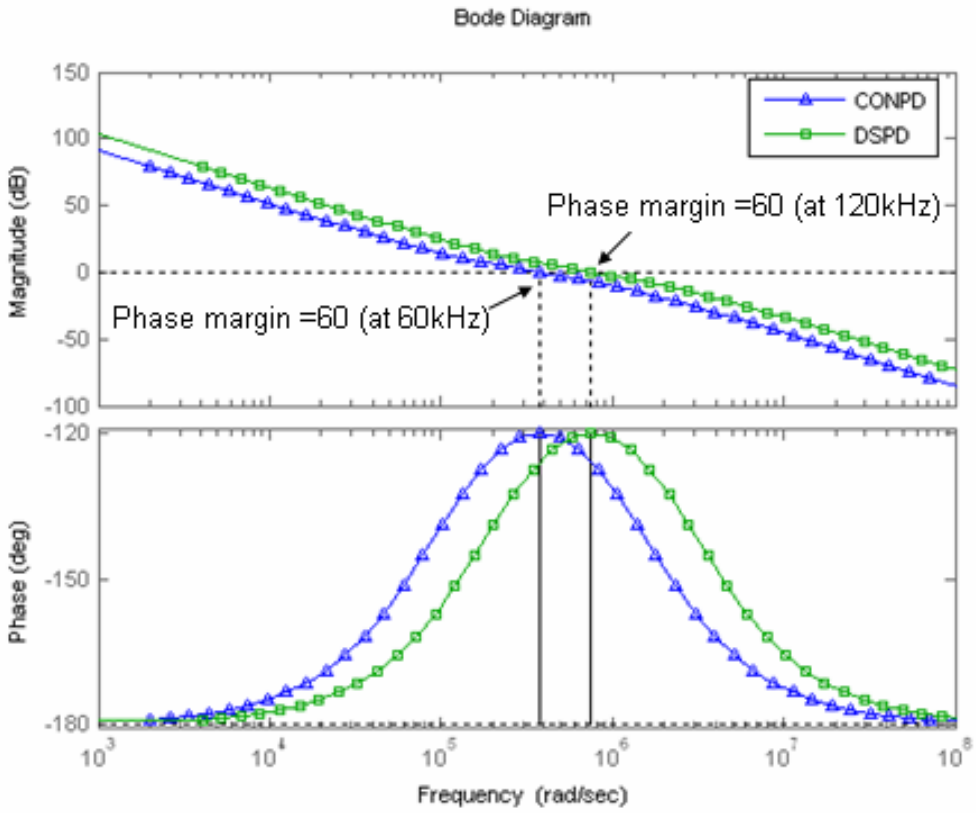


Figure 3.1 The open loop transfer function magnitude and phase response for the loop filter of the conventional PD PLL (CONPD) and DSPD PLL (DSPD).

3.2 Verilog-AMS Timing Model

To verify that the phase locked loop with double sampling phase detector can achieve fast settling and suppress the reference spur, a Verilog-AMS PLL timing model is developed. Verilog-AMS is a model language for Mixed-Mode system to describe the digital and analog circuits. For example the reference spur is generated by the non-ideal effects of the phase detector in time domain, the information then is transferred to the analogical quantity in the control voltage of the VCO. Therefore the Verilog-AMS PLL timing model with the phase detector non-ideal effects can be easily and efficiently described to illustrate the reference spur and transient behavior of the phase-locked loop.

3.2.1 Phase Detector

The conventional phase detector in charge-pump PLL is implemented by the phase frequency detector and the charge pump. The non-ideal effects of the phase detector will create the reference spur due to the leakage current from the control voltage, the charge pump current mismatch and the Up/Down signals timing skew effect [4]. The block diagram of the Verilog-AMS model of the PFD and the charge pump with the non-ideal effects can be shown in Figure 3.2. The leakage current from the control voltage is modeled as a current source ($I_{leakage}$). The charge pump mismatch can be modeled with two current sources with different current I_{up} and I_{down}. The signals (Up/Down) to control the switch of the charge pump with a delay block (Tu, Td) for modeling the skew effect.

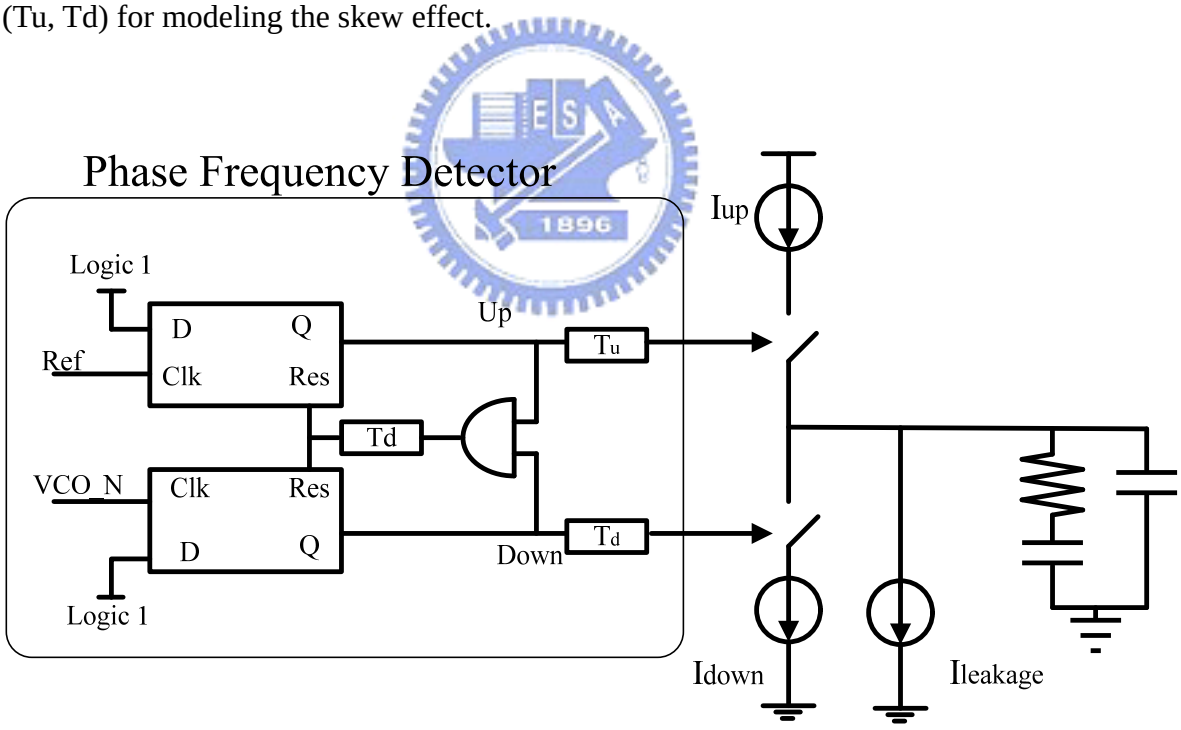


Figure 3.2 The block diagram of the Verilog-AMS model of the PFD and the charge pump with the non-ideal effects.

3.2.2 Voltage Control Oscillator

The voltage control oscillator is modeled as a mathematical model that generates a periodic output whose frequency is a linear function of the control voltage, *Vt*.

$$w_{out} = w_{free} + K_{VCO}V_t \tag{3.1}$$

The ω_{free} and *Kvco* are the free running frequency and the gain of the VCO. Since the phase is the integral of the frequency with respect to time, the VCO output can be modeled as a sinusoidal function:

$$V_{out}(t) = A\cos(w_{free}t + K_{VCO}\int_{-\infty}^{t} V_t dt) \tag{3.2}$$

3.2.3 Feedback Divider

The feedback divider employs 7 stages divide-by-two to achieve the feedback divider ratio, 128, as shown in Fig 3.3(a). Each divider-by-two is implemented by the D-FF as shown in Figure 3.2(b).

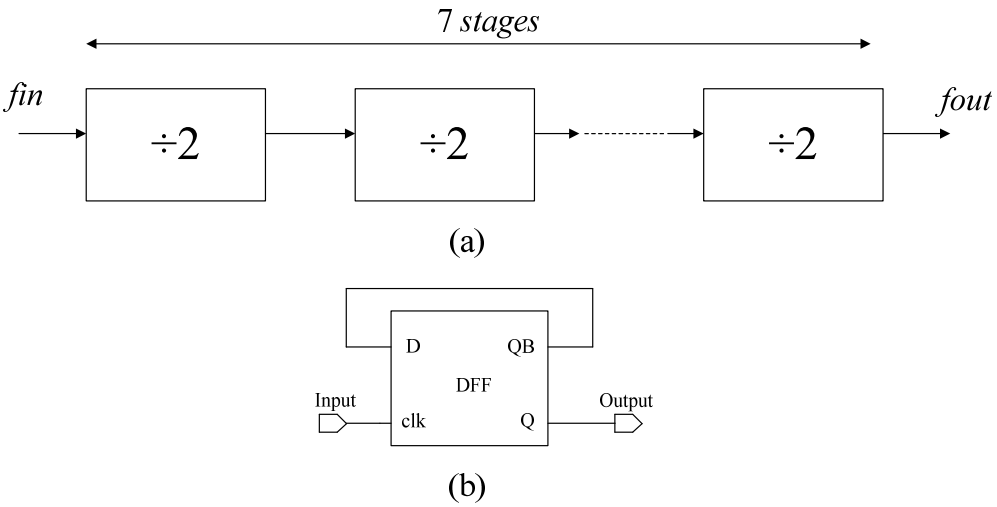


Figure 3.3 (a) The block diagram of the feedback divider model. (b) D-FF divider-by-two circuit

3.2.4 CML divide-by-two

The CML divide-by-two circuit can be modeled as two latches as shown in Figure 3.4. The divider-by-two circuit provides quadrature-phase outputs to implement the double sampling phase detector.

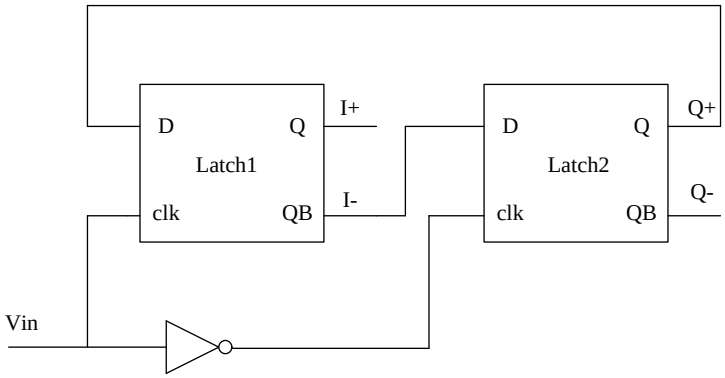


Figure 3.4 The block diagram of the CML divide-by-two model.

3.3 Vreilog-AMS Phase Locked Loop Simulation

The Verilog-AMS PLL model with conventional phase detector and double sampling phase detector is developed. For the conventional PD, set the delay block in PFD (Td=0.1nsec, Tu=0.1nsec, Td=0.2nsec) to model the skew effect. The charge current (Iup=100uA) and discharge current (Idown=90uA) to model the charge pump with 10% mismatch. The leakage current is 100nA. For DSPD, the delay block of the PFDs are settled the same as the PFD in the conventional PD. In addition the mismatch between charge current and discharge current of the two charge pumps in the DSPD are also considered the same as the charge pump in the conventional PD. Because of the DSPD has two charge pumps, the leakage current is settled as 200nA. In addition to the different phase detector, the PLL with conventional PD uses the loop filter design in Table 3.1 and the PLL with DSPD uses the loop filter design in

Table 3.2 to eliminate the phase margin degradation. The VCOs and feedback dividers in two PLLs are the same. The free running frequency is 2.45 GHz and the VCO gain is 120 MHz. The reference frequency is 20MHz and the feedback divider ratio is 128, therefore the output frequency will be locked at 2.56 GHz.

Figure 3.5 shows the control voltages of the VCO in the proposed Verilog-AMS PLL model with the conventional PD and DSPD as the frequency jump from 2.45GHz to 2.56GHz. The reduction of the settling time is 50% in the 30-ppm frequency accuracy.

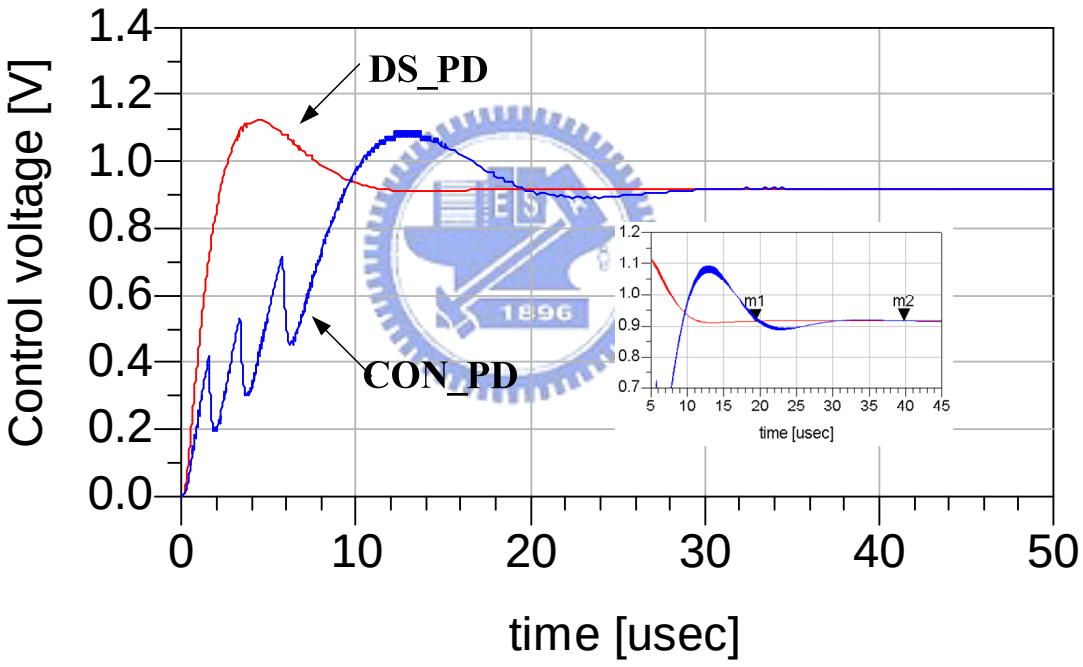
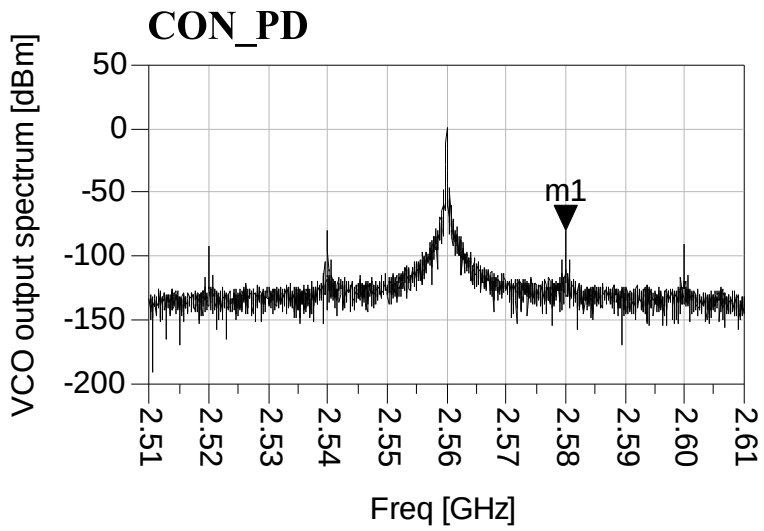
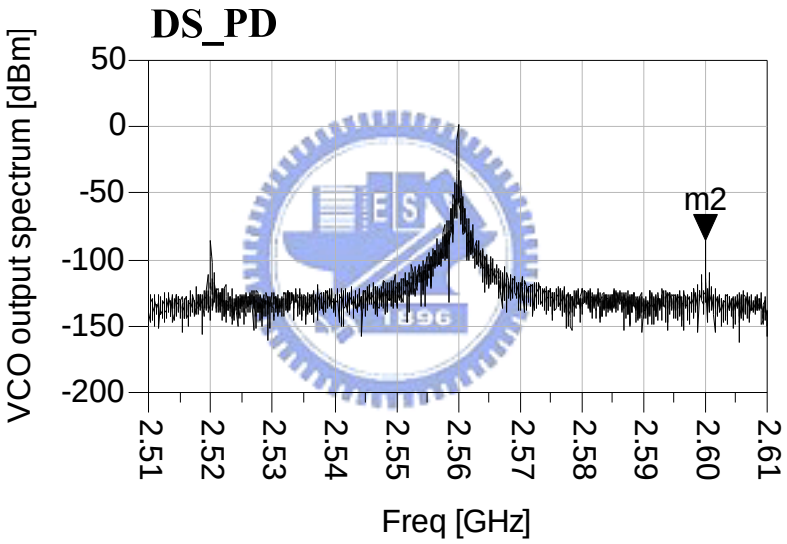


Figure 3.5 Control voltage of the VCO for frequency jump from 2.45GHz to 2.56GHz. In the 30-ppm frequency accuracy, the DSPD PLL (DS_PD) is locked at 20usec (m1) and the conventional PD PLL (CON_PD) is locked at 40usec (m2).



(a)



(b)

Figure3.6 Output spectrum of the PLL with the double sampling phase detector and the conventional phase detector. (a) Reference spur is -79.09dBm at 2.58GHz (m1). (b) Reference is -82dBm at 2.6GHz (m2)

Figure 3.6 shows the output spectra of the two Verilog-AMS PLL models with different phase detectors. The reference spur of the proposed PLL with double sampling phase detector is moved to two times of reference frequency from the carrier and is suppressed 5.9 dB more. DS_PD and CON_PD represent the PLL with double sampling phase detector and the conventional phase detector, respectively.

Chapter 4 Circuit Design and Implementation Results

4.1 Circuit Design

The reference spur suppression and the fast settling for the double sampling technique were verified by the linear model analysis and Verilog-AMS behavior model simulation in the previous chapters. In order to verify the performance improvement in real circuit, the process variation must be concerned. The PLL implementation must include both DSPD and conventional PD with the same VCO, feedback divider and the same quantity of the non-ideal effects of the phase detector. Figure 4.1 and Figure 4.2 show two digital signals, V_{switch} and V_{PFD}, to control the PLL for two operation modes, DSPD and conventional PD. The loop filter is off chip for different modes.

4.1.1 Phase Detector

Figure 4.1 shows schematic of the PLL operates in DSPD mode. The V_{switch} controls the outputs of the 2-to-1 MUXs and the V_{PFD1} and V_{PFD234} control the PFDs. For the DSPD mode, first the V_{switch} selects the outputs of MUXs (R0 and V0) to be output of the CML divide-by-two, then V_{PFD1} and V_{PFD234} the will turn on all the PFDs.

Figure 4.2 shows the control signals control the PLL with the DSPD architecture but operates like the conventional PD. First the V_{switch} selects the outputs of MUXs (R0 and V0) to be the signals Ref and VCO_N and only PFD1 is turned on. In this mode, the charge pump1 is operated and the charge pump2 is off. The PLL will operate in the conventional PD mode.

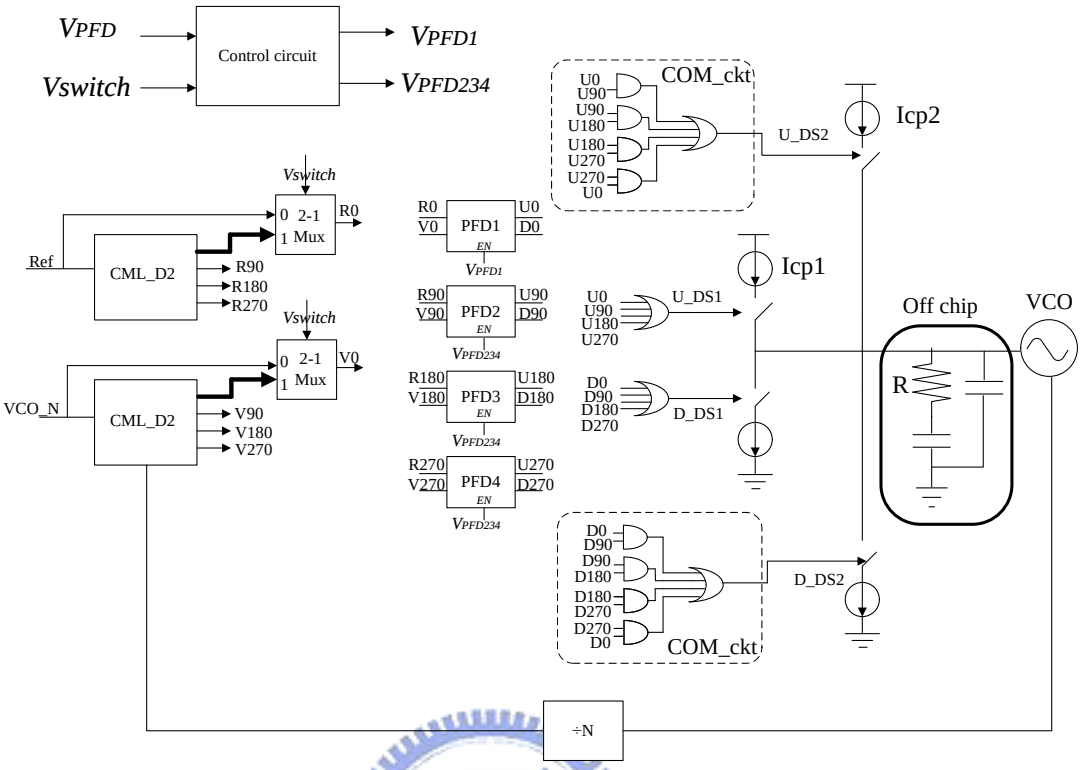


Figure 4.1 The schematic of the PLL operates in the DSPD model with control circuit.

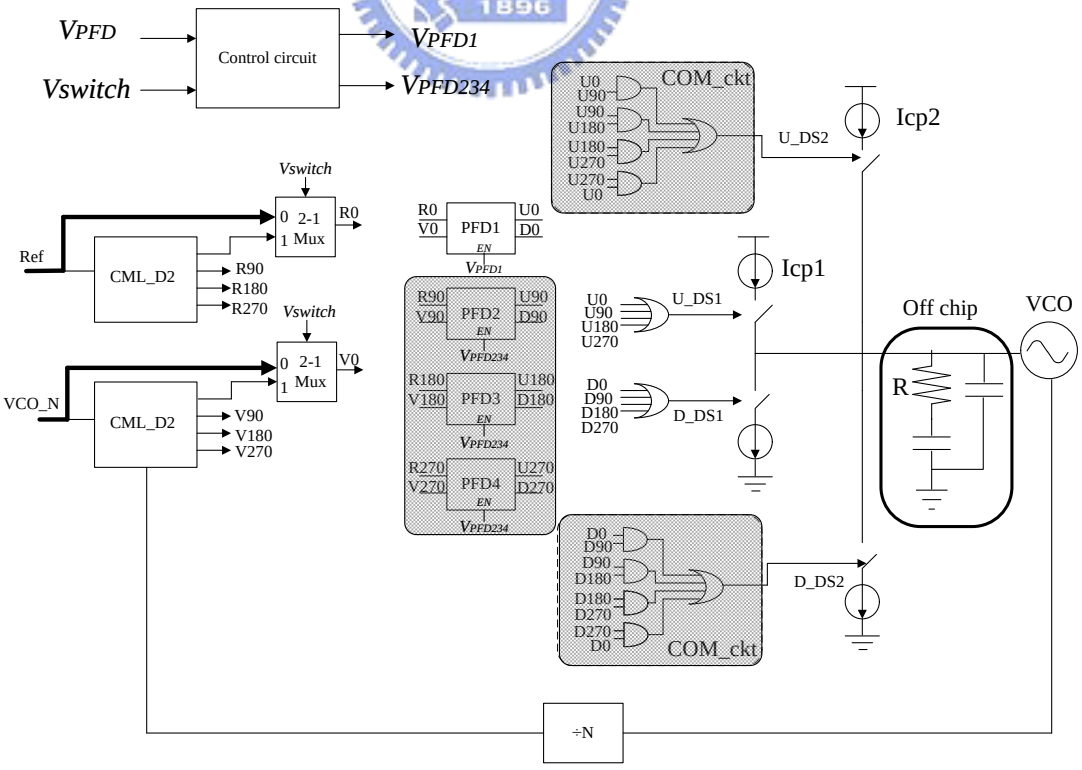


Figure 4.2 The schematic of the PLL operates in the conventional PD model with control circuit.

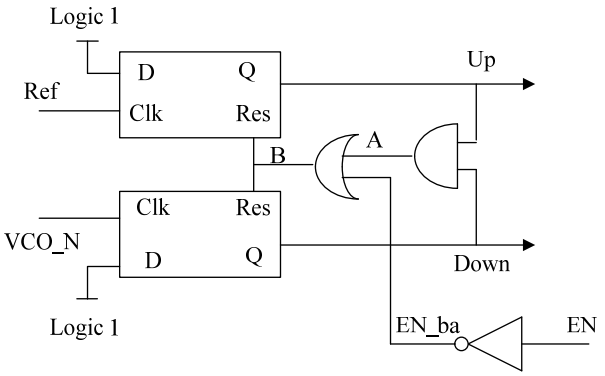
The control circuit is designed according to the truth table as shown in Table 4.1. The OFF mode is defined as the PFDs are all turned off before the V_{switch} is defined. To control the PFDs, the outputs signals of the control circuit V_{PFD1} and V_{PFD234} can be defined as the Boolean functions:

$$V_{PFD1} = V_{PFD}$$
$$V_{PFD234} = V_{PFD} V_{switch}$$

Table 4.1 Control circuit truth table.

mode	Input		Output	
	Vswitch	VPFD	VPFD1	VPFD234
OFF	0	0	0	0
Conventional PD	0	1	1	0
OFF	1	0	0	0
DSPD	1	1	1	1

Because of the operation of the PFDs is controlled by the V_{PFD1} or the V_{PFD234}, the PFDs are designed with a disable operation as shown in Figure 4.4. The EN signals of the PFDs are connected to the V_{PFD1} or V_{PFD234}, so when the EN=0 then B=1 and the PFD is turned off otherwise when EN=1 then B=A the PFD is turned on.



EN=0	EN_ba =1	B=1 PFD turn off
EN=1	EN_ba =0	B=A PFD turn on

Figure 4.3 The PFD with an EN signal.

4.1.2 Charge pump

The charge pump transfer the pulse of the phase detector to the charge injected in to the loop filter. The charge pump circuit is shown in Figure 4.5. The M1, M2, M5 is to generate the bias current. The current mirror M3, M4, M5, M6 is to generate the I_2 is as same as the I_1. The charge pump1 is composed by M10, M11, M12, M13 and the charge pump 2 is composed by M14, M15, M16, M17. In charge mode, the charge pump1 and the charge pump2, the M6, M7, M10, M11, M14 and M15 are designed to set $I_2=I_{up1}=I_{up2}$. In discharge mode for the charge pump1 and the charge pump2, the M8, M9, M12, M13, M16 and M17 are to let $I_2=I_{down1}=I_{down2}$.

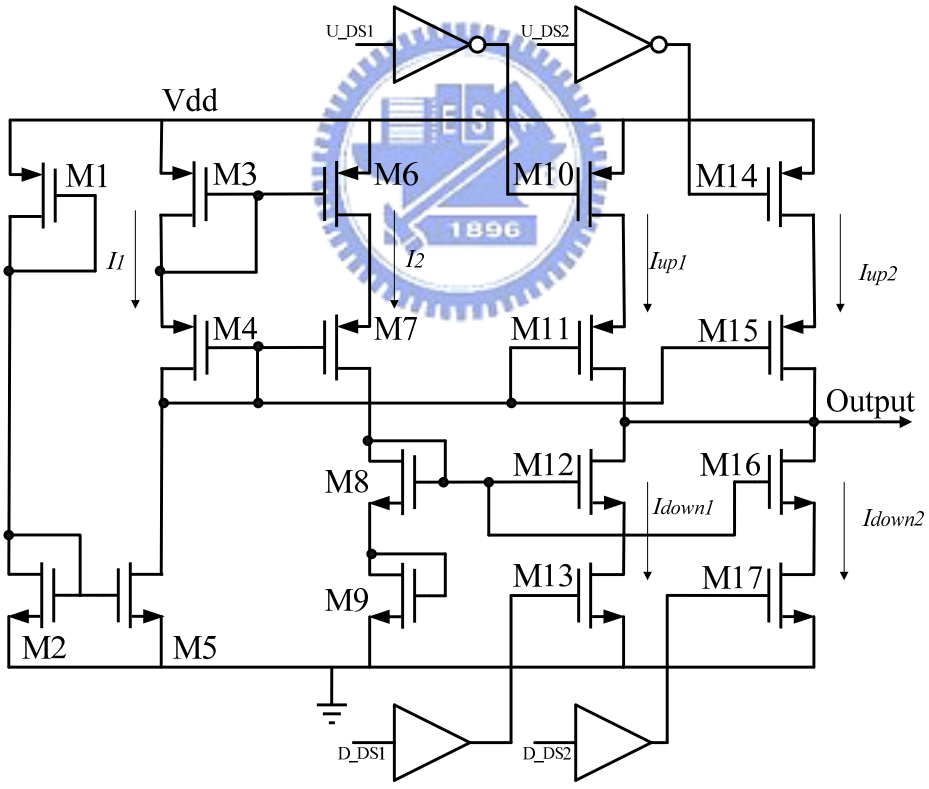


Figure 4.4 The schematic of the charge pump.

4.1.3 Voltage control oscillator

In this PLL design the VCO is implemented by the LC-tank voltage control oscillator because of the high frequency accuracy and low phase noise performance and it is shown in Figure 4.6. The NMOS M1 and M2 make up the cross-coupled pair to provide a negative resistance (R_n=-2/$gm_{1,2}$) to compensate the loss of the LC tank. The NMOS M4 acts as a varactor, the capacitance ($\Delta C(V_{tune})$) between gate and drain can be control by the V_{tune}. The switch-capacitance (C1 and C2) are used to enlarge the tuning range and remain the small VCO gain at the same time [4].

The output frequency can be expressed as

$$w_{out} = \frac{1}{\sqrt{L\left(C_L + C_L^{'} + \Delta C\left(V_{tune}\right)\right)}}$$

$C_L^{'}$ is related to the ON/OFF of the switch D1 and D0.

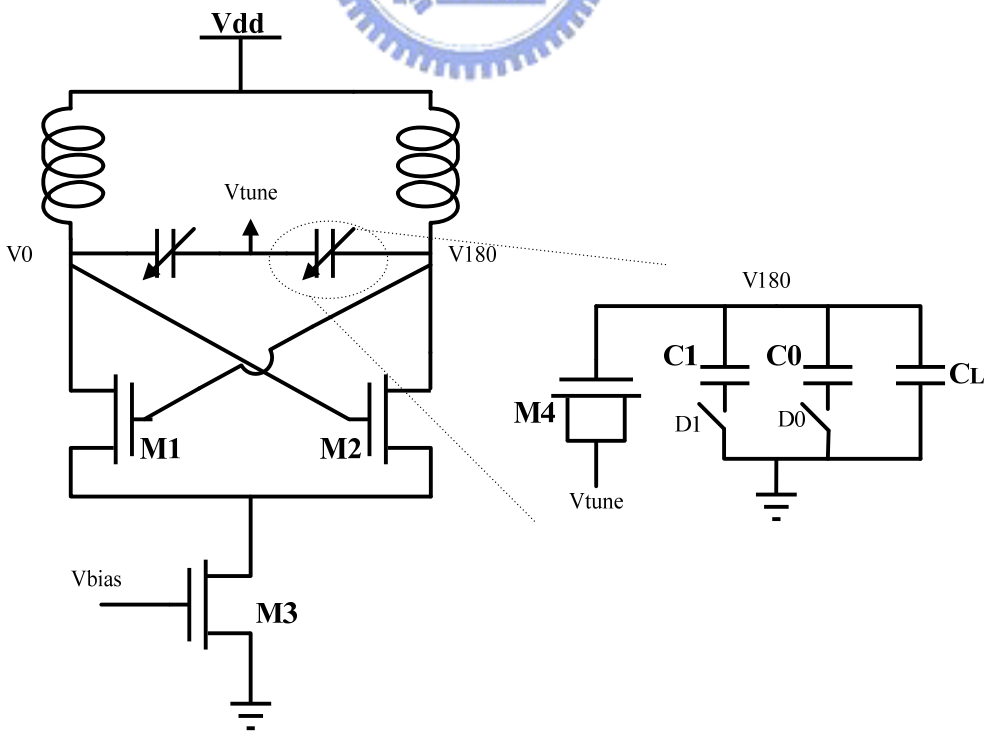


Figure 4.5 LC-tank voltage control oscillator.

The VCO simulation results including the time domain VCO output waveform, VCO output spectrum, phase noise and tuning range are shown in Figure 4.6, Figure 4.7, Figure 4.8 and Figure 4.9, respectively. Figure 4.8 shows the phase noise at the one and two times reference frequency (18MHz and 36 MHz) offset from the carrier are -135.3dBc and -143dBc.

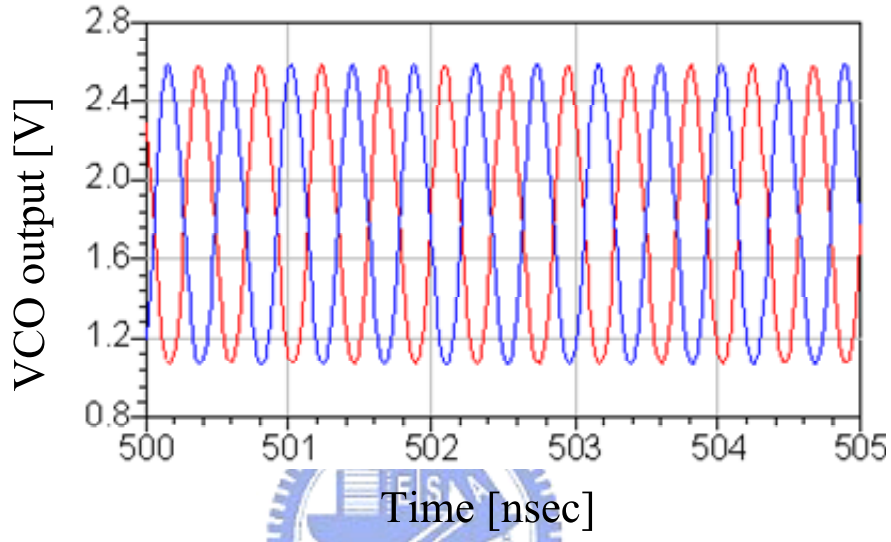


Figure 4.6 VCO output waveform

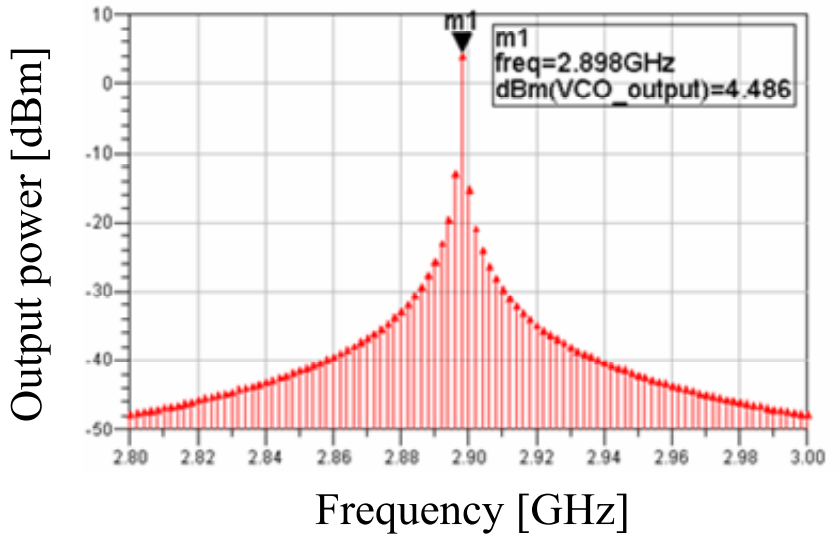


Figure 4.7 VCO output spectrum

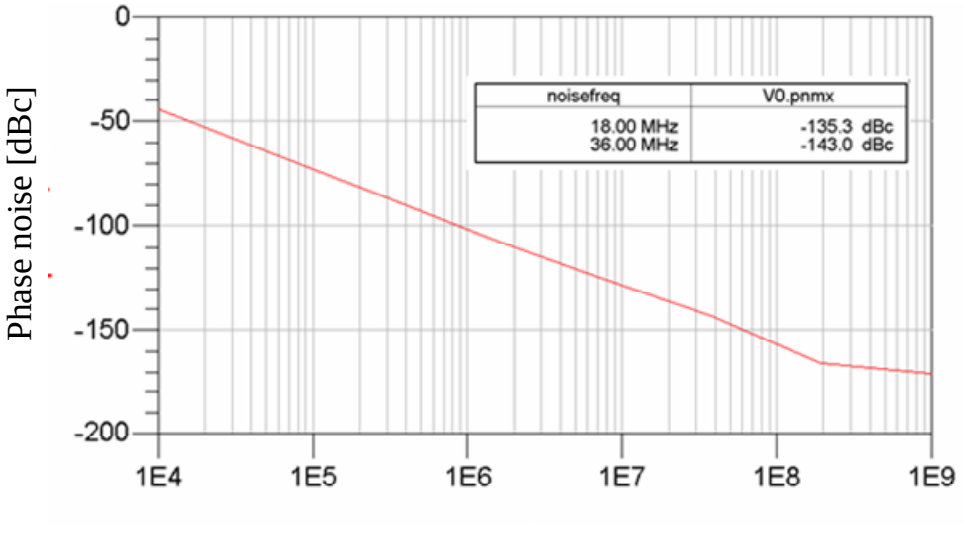


Figure 4.8 VCO output phase noise

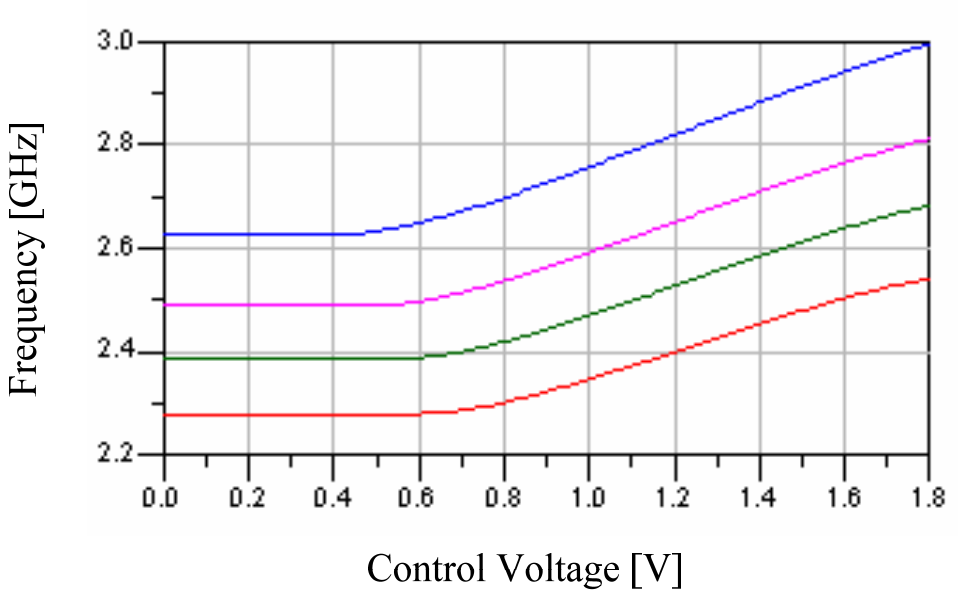
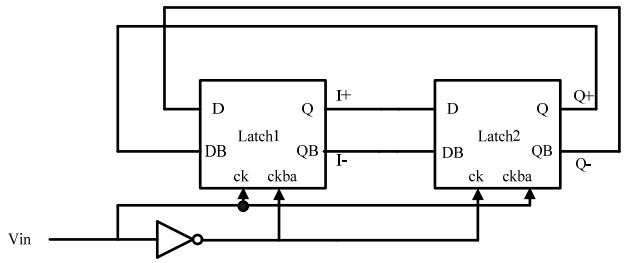


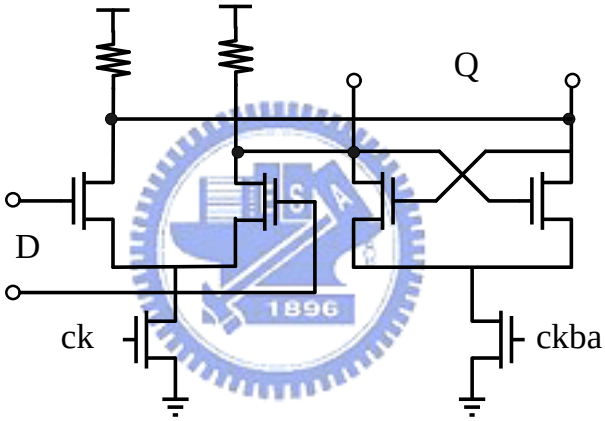
Figure 4.9 Tuning range

4.1.4 Divider–CML divide-by-two

The CML divide-by-two [5] is realized as two latches in a negative feedback loop as shown in Figure 4.11 (a). Figure 4.11 (b) is the latch circuit implemented in CMOS technology.



(a)



(b)

Figure 4.10 (a) Divide-by-two circuit (b) implementation of the latch in CMOS technology.

4.1.5 Divider–Feedback divider

The block diagram of the feedback divider is designed as shown in Figure 4.11 (a). The divider ratio can be 128 or 160 with the control signal MC. The first stage of the feedback divider is implemented by four cascade DFF divide-by-two to achieve divider ratio 16 as shown in Figure 4.11 (b). The first two DFF dividers are implemented by TSPC divide-by-two [6] for high frequency operation and the last

two stages are implemented by the CMOS logic. The second stage of the feedback divider is designed as a dual divider ratio (÷4/÷5) divider as shown in Figure 4.11 (c). The last stage of the feedback divider is implemented by the DFF as shown in Figure 4.11 (d).

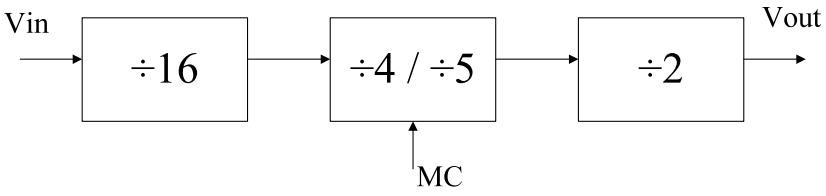


Figure 4.11 (a) The feedback divider diagram.

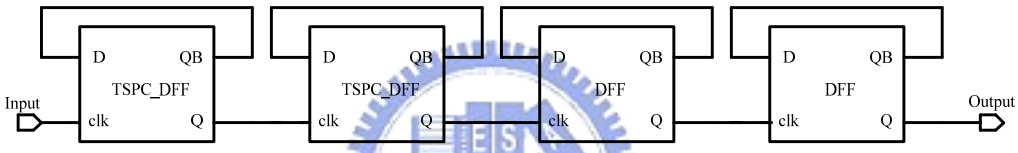


Figure 4.11 (b) Four cascade DFF divide-by-two achieve divider ratio 16.

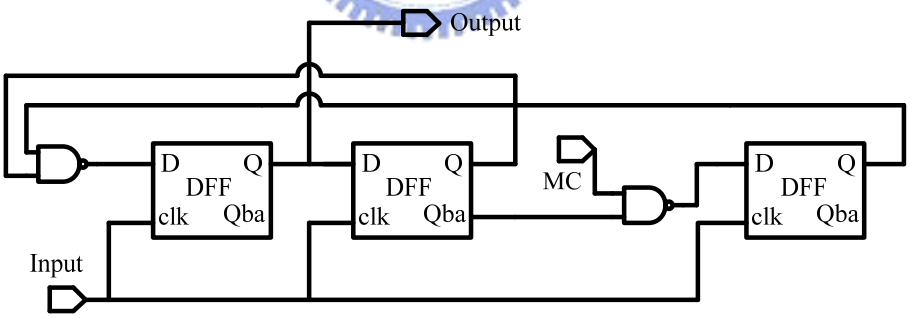


Figure 4.11 (c) Dual divider ratio (÷4/÷5) divider.

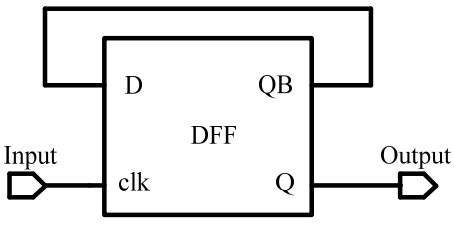


Figure 4.11 (d) DFF divide-by-two

4.2 Simulation

The post layout simulation results of the PLL are shown in Figure 4.12 and Figure 4.13, including the control voltage of the VCO and the VCO output spectrum. DS_PD and CON_PD denote the PLL with double sampling mode and the conventional phase detector mode, respectively.

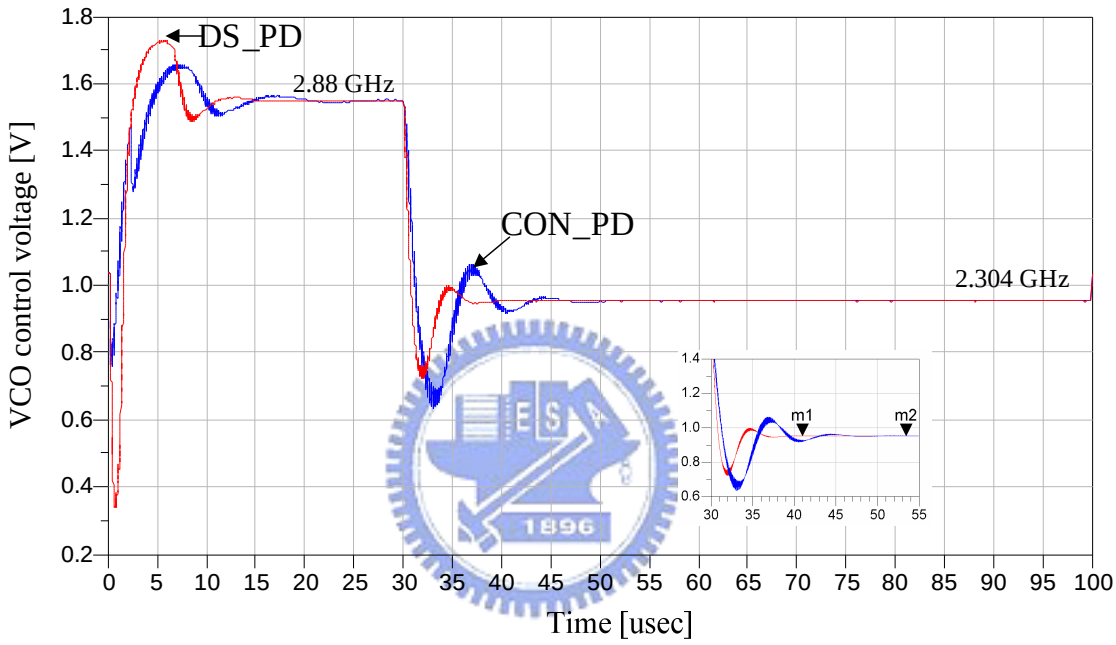
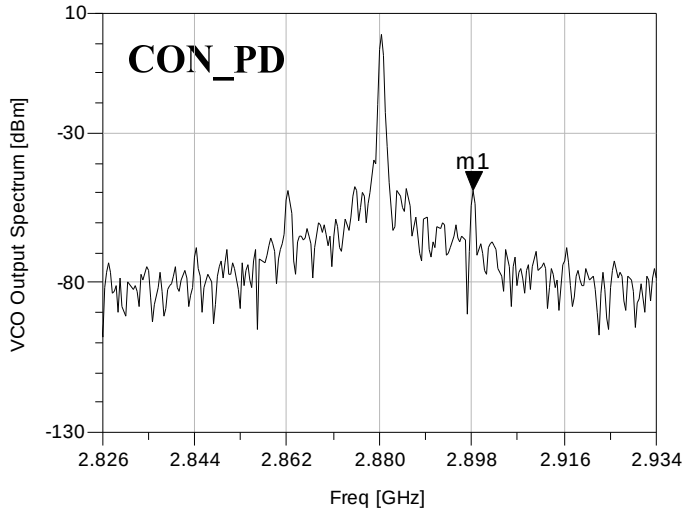
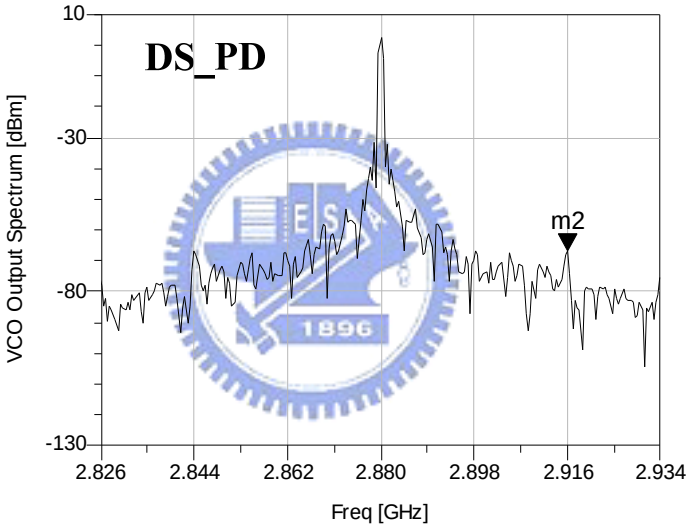


Figure 4.12 VCO control voltage

The PLL locks to 2.88 GHz first then switch to 2.304 GHz at 30usec. From the post-simulation result, in the 30-ppm frequency accuracy the PLL with DSPD mode is locked at 42usec (m1) and the PLL with conventional PD mode is locked at 54usec. Hence the settling time is reduced 50% with the proposed DSPD technique.



(a)



(b)

Figure 4.13 Output spectrum of the PLL with the DSPD mode and the conventional PD mode. (a) Reference spur is -52dBm at 2.898GHz (m1). (b) Reference is -68dBm at 2.916GHz (m2).

The reference spur of the PLL with DSPD mode is moved to two times of the reference frequency away from the carrier and is suppressed 16 dB. Comparing to the linear model analysis the reference spur can be suppressed more than 6.2 dB because of the suppression of the LC-tank.

4.2 Measurement

PLL design 1

Figure 4.14 shows layout photo of the PLL design 1 using the PMOS LC-tank VCO. The PLL is fabricated in UMC CMOS 0.18um technology.

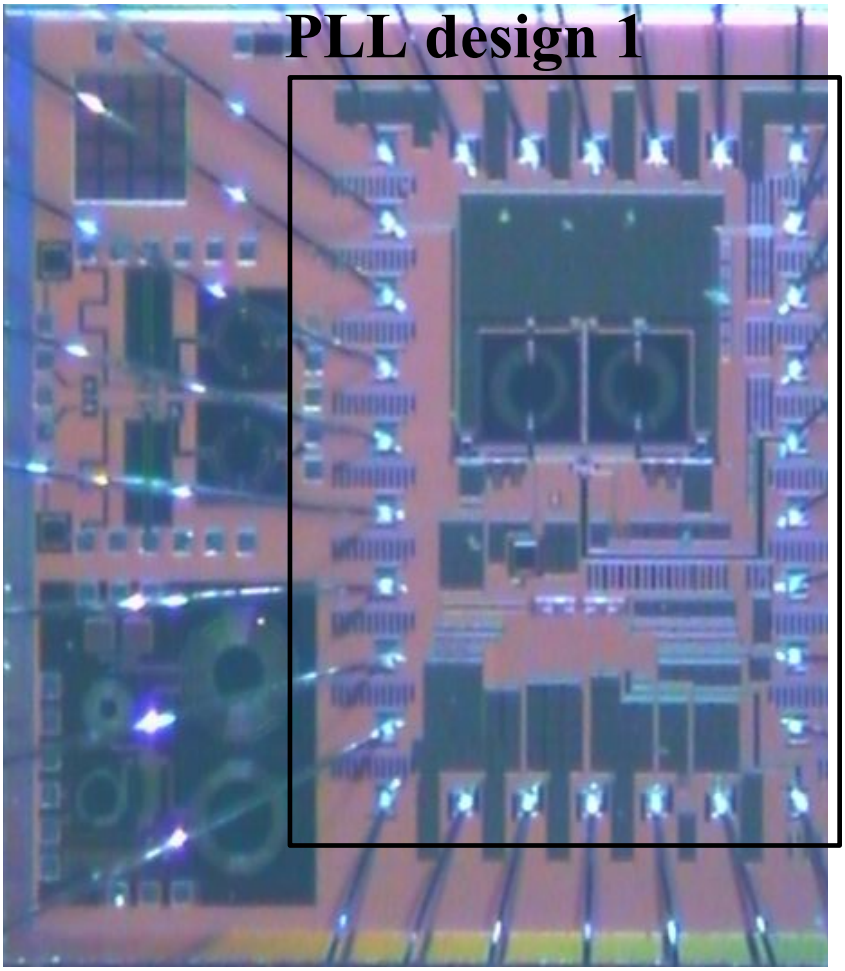


Figure 4.14 Layout view of PLL design 1.

VCO measurement

Figure 4.15 shows the testing setup for the phase noise and the spectrum measurement of the voltage control oscillator. It consists a spectrum analyzer, a power supply and two open drain matching network. One of the VCO outputs is terminated by a load having impedance of 50Ω and the other is connected to the spectrum analyzer.

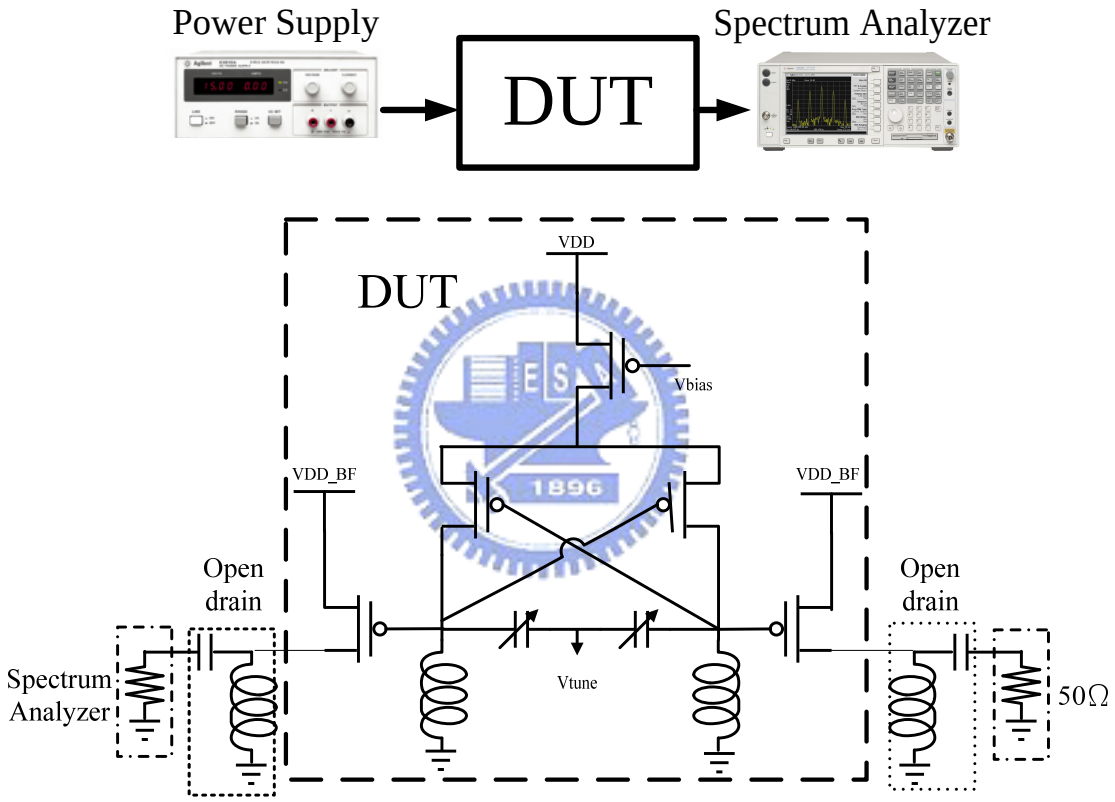


Figure 4.15 VCO testing setup

The measured output spectrum at 2.528 GHz is shown in Figure 4.16. The output power including the cable loss is -8.76dBm. Figure 4.17 shows the phase noise measurement result of the voltage control oscillator with the carrier frequency 2.528 GHz. The measured phase noise is -102.85 (dBc/Hz) at 1-MHz frequency offset.

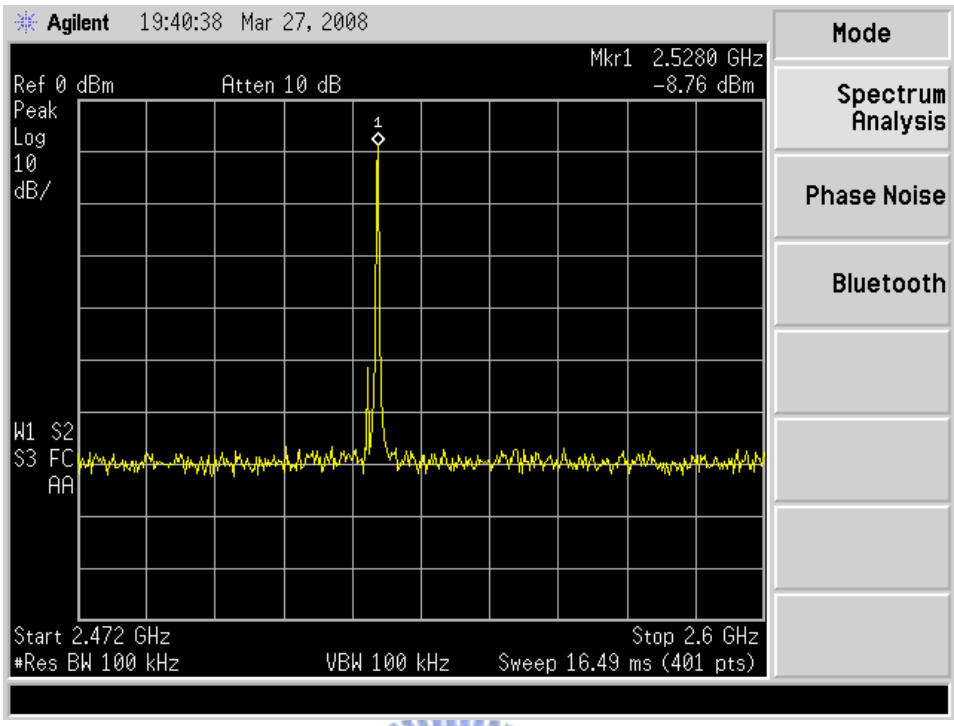


Figure 4.16 Output spectrum of the VCO

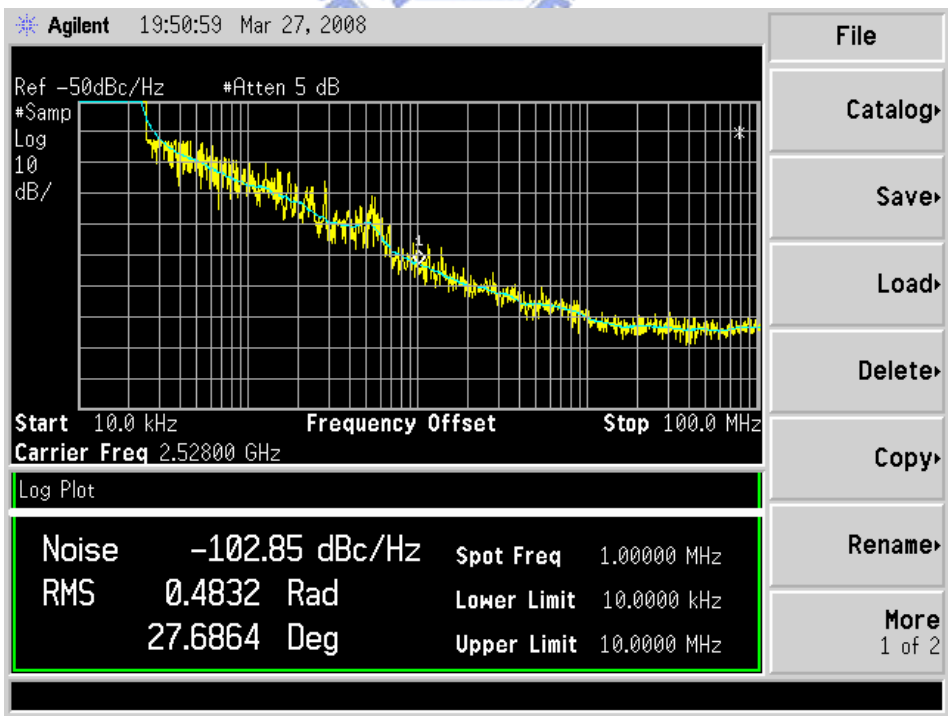


Figure 4.17 Phase noise of the VCO

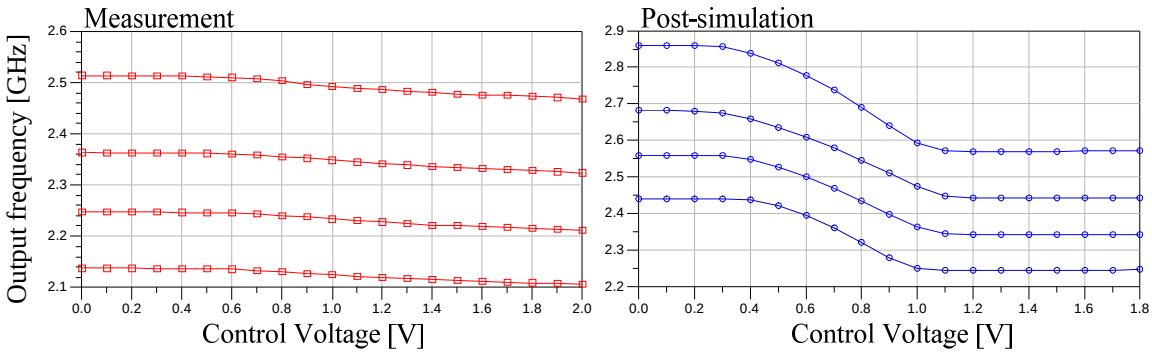


Figure 4.18 Tuning range of the VCO

Comparing to the measurement and post-simulation of the tuning range results, the carrier frequency is degraded and the tuning range of the measurement is about 40 MHz/V and the post-simulation results is about 200 MHz/V. The performance degradation is caused by the parasitic capacitance.

DSPD measurement

Figure 4.18 shows the testing setup for the DSPD. It consists a 2 MHz crystal, a power supply and a oscilloscope. The power supply provides not only VDD power but also the control signals V_{switch} and V_{PFD} to select the PLL operation mode. The crystal and delay block which is implemented by a RC circuit create two input signals with different phase (Ref and VCO_N). The oscilloscope can measure the outputs including the outputs of the MUXs, U_DS1, U_DS2, D_DS1 and D_DS2.

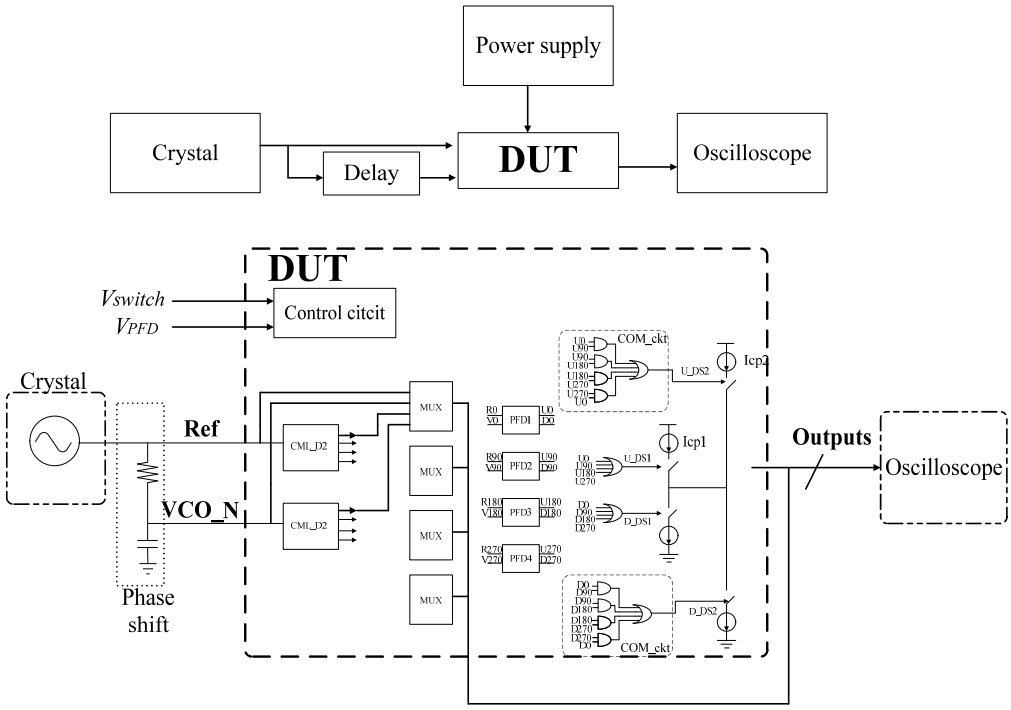


Figure 4.19 DSPD testing setup

Figure 4.19 shows the measurement results for conventional PD mode (V_{switch}=0 V and V_{PFD} =1.8 V). The DSPD is operated in conventional PD mode by the control signal.

Figure 4.20 Conventional PD mode

For DSPD mode (V_{switch}=1.8 V and V_{PFD} =1.8 V), the control signal node V_{switch} has a leakage current about 5mA and the DSPD mode can not operate correctly.

PLL design 2

Figure 4.21 shows layout photo of the PLL design 2 using the NMOS LC-tank VCO. The PLL is fabricated in UMC CMOS 0.18um technology.

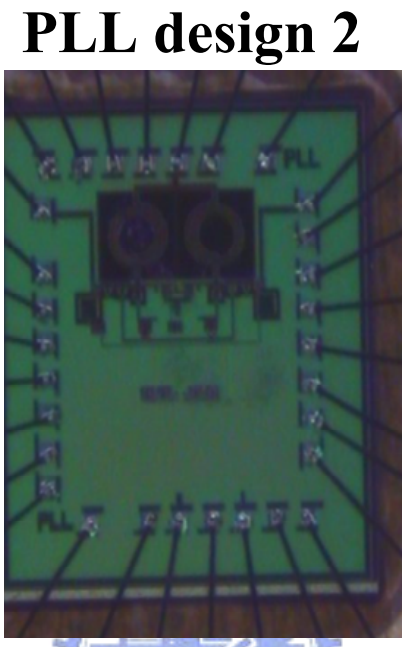


Figure 4.21 Layout view of PLL design 2.

VCO measurement

The VCO testing setup is as same as that for the PLL design 1. The measured output spectrum is 2.336 GHz as shown in Figure 4.22. The output power including the cable loss is 4.9dBm. Figure 4.23 shows the phase noise measurement result of the voltage control oscillator with the carrier frequency 2.36 GHz. The measured phase noise is -84.23 (dBc/Hz) at 1-MHz frequency offset. The measurement and post-simulation results of the tuning range are shown in Figure 4.24, the measurement is about 60 MHz/V and the post-simulation is about 200 MHz/V. The performance degradation is caused by the parasitic capacitance.

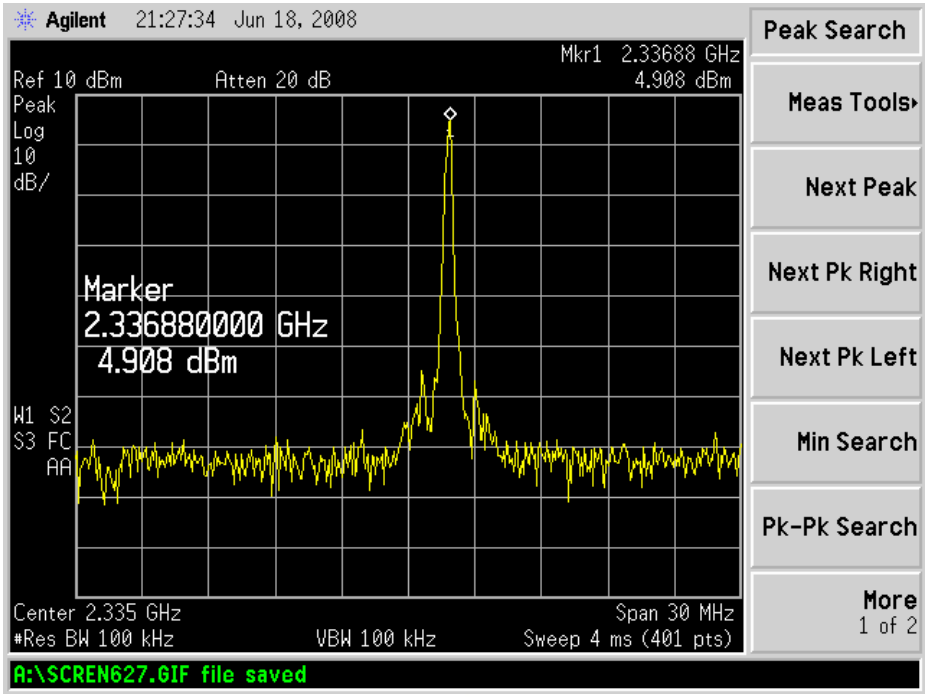


Figure 4.22 Output spectrum of the VCO

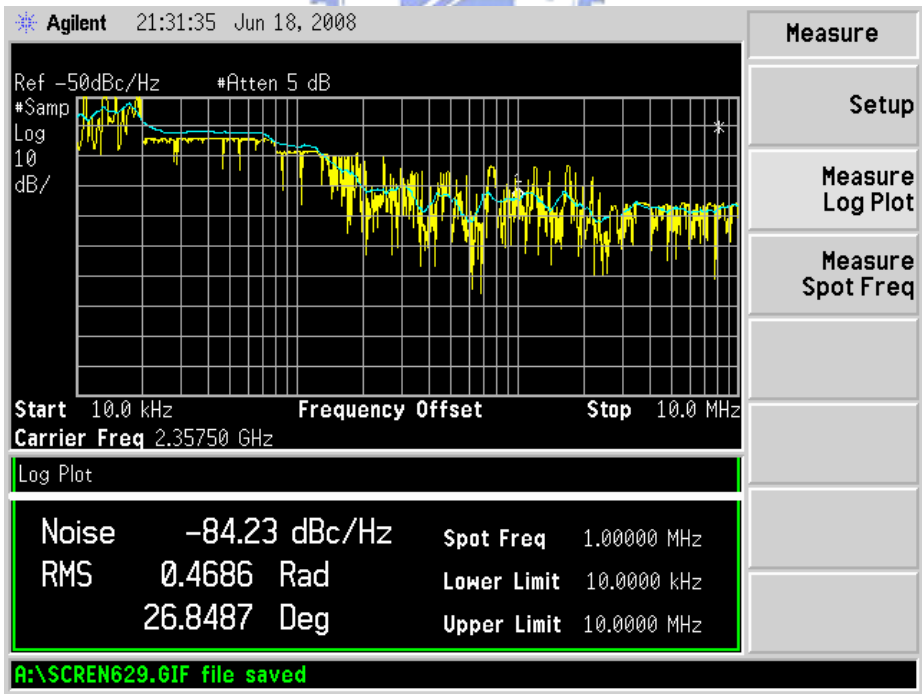


Figure 4.23 Phase noise of the VCO

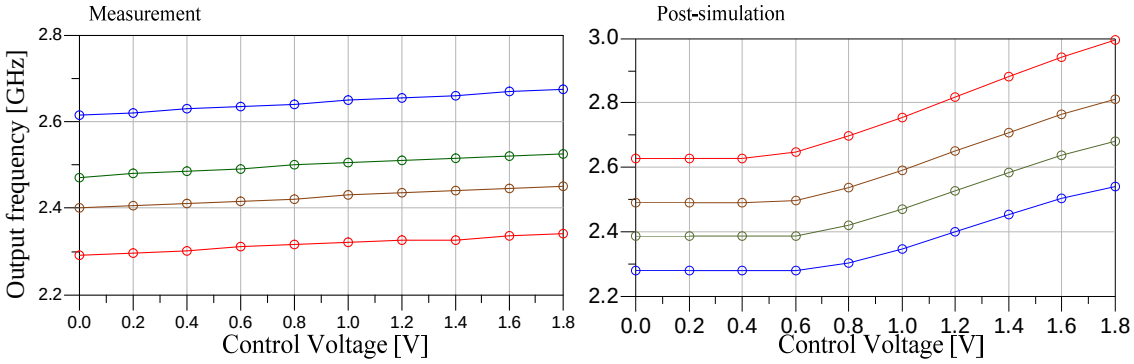


Figure 4.24 Tuning range of the VCO

Chapter 5 Conclusions and Future Works

5.1 Conclusions

In this thesis, a novel PLL architecture with double sampling phase detector is proposed to achieve both fast settling time and low reference spur. Comparing with the conventional phase detector, the double sampling phase detector doubles the sampling rate of the phase detector without changing the reference source.

The linear model of the third order charge-pump PLL with DSPD is developed. The linear gain of DSPD is doubled to achieve wider PLL loop bandwidth to reduce the settling time meanwhile the reference spur can be suppressed by the sampling rate of the phase detector is doubled. To compensate the phase margin degradation, the compensational loop filter design for PLL with DSPD is proposed.

The PLL system with conventional PD and DSPD are designed and the Verilog-AMS PLL timing model with phase detector non-ideal effects is developed to verify the settling time and reference spur improvement. From the timing model simulation results, the settling time can be reduced 50% in 30-ppm frequency accuracy and the reference spur shifts to two times reference frequency from carrie.r

In order to eliminate the process variation, a 2.304GHz/2.88GHz PLL with the conventional PD and DSPD operation modes is deigned. Simulation results show the settling time can be reduced 50 % in 30-ppm frequency accuracy and the reference spur can be shift to two times reference frequency from carrier and suppress 16 dB.

5.2 Future works

Since increasing the sampling rate of the phase detector can improve both settling time and reference spur performance, the DSPD architecture can be modified to achieve over sampling phase detector. The over sampling ideal is to increase the phase detector sampling rate without changing the reference source. The architecture for over sampling phase detector (OSPD) can be shown in Figure 5.1. To achieve over sampling, the delay blocks (Td = Tref/(n+1)) can be employed to generate multiphase of Ref and VCO_N signals, and n PFDs generate the phase difference from the multiphase outputs (R0/V0, R1/V1…Rn/Vn). Then the n-input OR gate combines the sampling results to be one output signal (U1/D1). The COM_ckt will generate signals (U2/D2) to control the charge pump2.

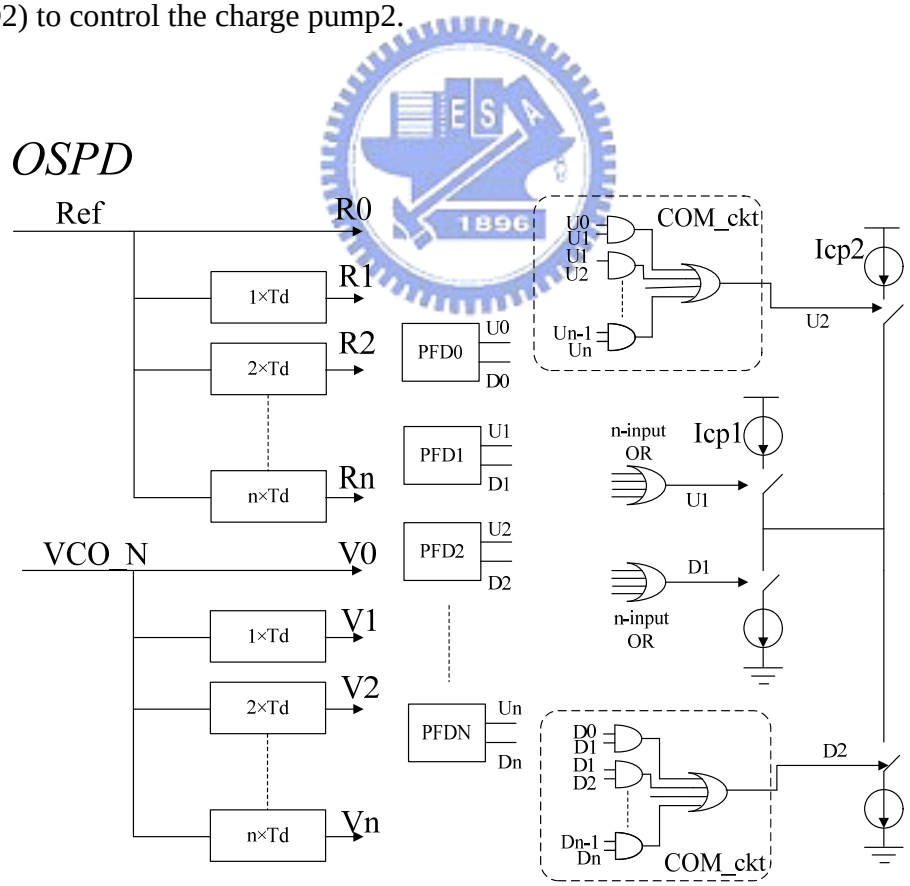


Figure 5.1 Over sampling phase detector.

The limitation of the OSPD is the detection region of the phase detector will be narrow as the n is increase. For example OSPD for n=2, the circuit is shown in Figure 5.2.

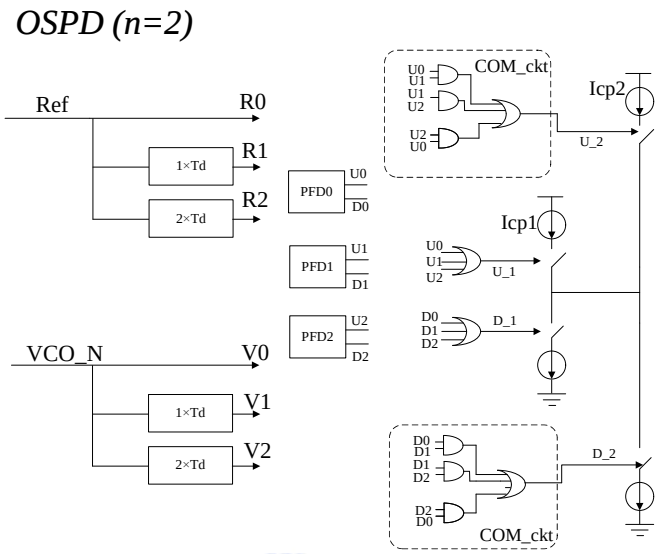


Figure 5.2 OSPD (n=2)

The linear gain can be defined from the signals time diagram in OSPD (n=2) as shown in Figure 5.3. Assume the charge pump current are the same. For the phase difference smaller than the 2π/3, the average current injected in the loop filter in one reference cycle can be given as

$$\bar{I} = \frac{I_{CP1}(3q_e)}{2p} = \frac{I_{CP}(3q_e)}{2p} \quad for \quad 2p/3 < q_e \tag{5.1}$$

For 2π/3 < phase difference ($q_e = 2p/3 + q_e'$) < 4π/3, the average current injected in the loop filter in one reference cycle can be given as

$$\bar{I} = \frac{I_{CP1}(2p) + I_{CP2}(3q_e')}{2p} = \frac{3(2p/3 + q_e')I_{CP}}{2p} \quad for \quad 2p/4 < q_e < 4p/3 \tag{5.2}$$

For 4π/3 < phase difference ($q_e = 4p/3 + q_e'$) < 2π, the average current injected in the loop filter in one reference cycle can be given as

$$\bar{I} = \frac{I_{CP1}(2p) + I_{CP2}(2p)}{2p} = \frac{4p\, I_{CP}}{2p} \quad for \quad 4p/3 < q_e < 2p \tag{5.3}$$

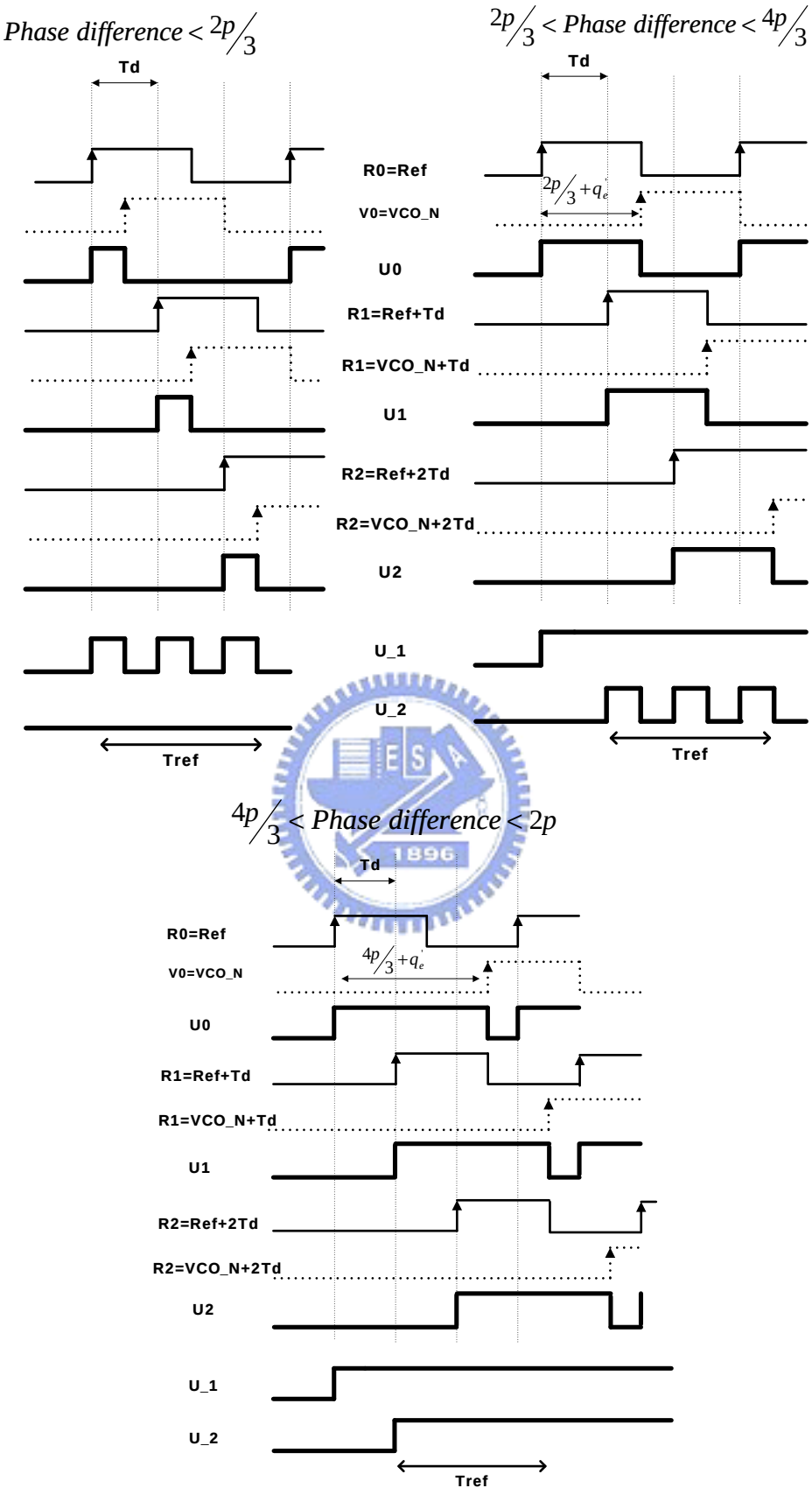


Figure 5.3 The signals in the OSPD (n=2).

The average current and phase difference characteristic of the OSPD (n=2) can be shown as Figure 5.4. The detection range of the OSPD (n=2) is $-4\pi/3 < q_e < 4\pi/3$. For more deep sampling technique, the logic circuit must be modified to extend the detection region. The process variation of the delay block will cause the phase noise performance degradation as discuss in reference [7]. In order to estimate the performance degradation due to the process variation more accuracy multiphase generator circuit is needed.

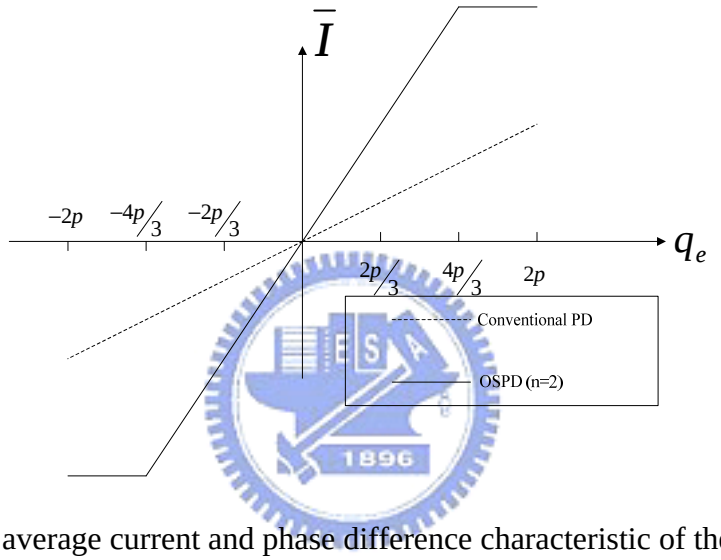


Figure 5.4 The average current and phase difference characteristic of the OSPD (n=2).

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Appendix

Feedback Delay Effect in PLL

Figure A-1 (a) and Figure A-1 (b) show the PLL linear model with the feedback delay for different phase detector architectures. In Figure A-1 (a), the delay effect in the feedback path is modeled as e^{-sT_D}, T_D is the delay time of feedback divider. In Figure A-2 (a), the delay effect in the feedback path is modeled as $e^{-s(T_D+T_{CML\_D2})}$ including the delay time of CML divider-by-two (T_{CML_D2}).

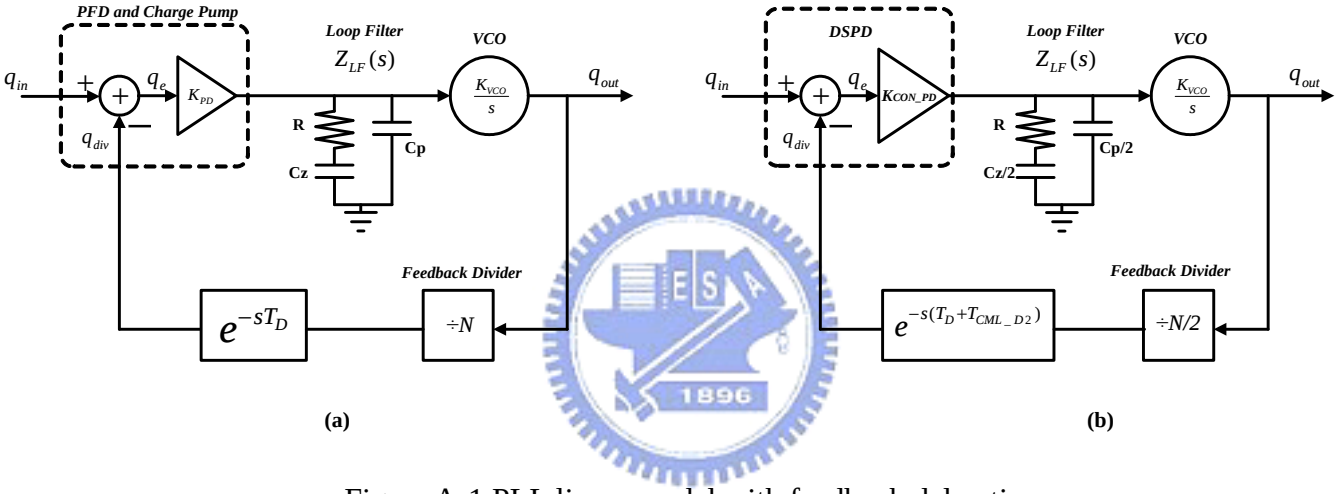

Figure A-1 PLL linear model with feedback delay time

In real circuit, the signal delay degrades the system phase margin [12] and the can be shown as

$$PM' = PM - w_{BW}T \tag{A.1}$$

w_{BW} and T are the PLL loop bandwidth and the delay time of the feedback divider.

In Figure A-1, the phase margin degradation due to delay effect can be expressed as

$$\begin{aligned} PM'_{CON} &= PM_{CON} - w_{CON\_BW}T_D \\ PM'_{DSPD} &= PM_{DSPD} - w_{DSPD\_BW}(T_D + T_{CML\_D2}) \end{aligned} \tag{A.2}$$

DSPD PLL doubles the PLL loop bandwidth and the modified loop filter design can remains the same phase margin (PM_{CON}=PM_{DSPD}). However, the phase margin is

degraded by the additional delay time of the CML divide-by-two and can be expressed as

$$\begin{aligned} & PM'_{DSPD} - PM'_{CON} \\ &= \left[PM_{CON} - w_{CON\_BW} T_D \right] - \left[PM_{CON} - 2w_{CON\_BW} (T_D + T_{CML\_D2}) \right] \\ &= w_{CON\_BW} (T_D + 2T_{CML\_D2}) \end{aligned} \quad \text{(A.3)}$$

According to feedback divider and CML_D2 circuit design in Chapter 5, the delay time of the feedback divider and CML divide-by-two are 0.2542nsec and 0.5nsec. The phase margin degradation is

$$PM'_{DSPD} - PM'_{CON} = 2p \times 60k \times (0.2542n + 0.5n) \approx 2.8 \times 10^{-4} (rad / \sec) = 0.0162^\circ \quad \text{(A.4)}$$

The phase margin degradation due to the feedback delay is small and can be neglected.

Noise Consideration of PLL

The transfer function from the noise sources to the output of the PLL can be obtained by the linear model as shown as Figure A-2.

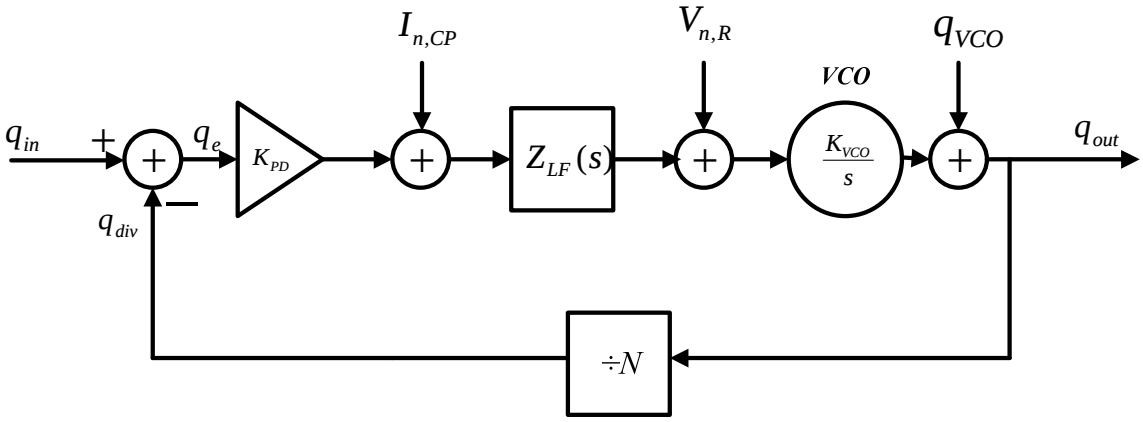

Figure A-2 PLL linear model with noise sources.

The transfer function from the input phase (q_{in}) to the output phase (q_{out}) can be expressed as following equation and is a low-pass function.

$$\frac{q_{out}}{q_{in}} = \frac{K_{PD} Z_{LF}(s) \frac{K_{VCO}}{s}}{1 + \frac{K_{PD} Z_{LF}(s) K_{VCO}}{Ns}} \tag{A.5}$$

Therefore, the phase noise of the reference is attenuated at large frequency offset.

The transfer function from the VCO noise (q_{VCO}) to the output phase can be expressed as the following equation and is a high-pass function.

$$\frac{q_{out}}{q_{VCO}} = \frac{1}{1 + \frac{K_{PD} Z_{LF}(s) K_{VCO}}{Ns}} \tag{A.6}$$

The far-offset phase noise of the PLL is dominated by the VCO phase noise.

The transfer function from the charge pump noise ($I_{n,CP}$) to the output phase can be expressed as the following equation and is a low-pass function.

$$\frac{q_{out}}{I_{n,CP}} = \frac{Z_{LF}(s) \frac{K_{VCO}}{s}}{1 + \frac{K_{PD} Z_{LF}(s) K_{VCO}}{Ns}} \tag{A.7}$$

The charge pump noise can be represented as [12]

$$I_{n,CP} = 2 \frac{t_{on}}{T_{ref}} 4kT \frac{2I_{CP}}{V_{od\_cp}} \tag{A.8}$$

where the t_{on} is the turn-on time of the charge pump and V_{od_cp} is the overdrive voltage (V_{GS}-V_t) of the transistor in charge pump circuit as shown in Figure 4.4. In DSPD, the noise of the charge pump 2 can be neglected because of charge pump current noise is dependent to the turn-on time.

The transfer function from the thermal noise of R ($V_{n,R}$) to the output phase can be expressed as the following equation and is a band-pass function.

$$\frac{q_{out}}{V_{n,R}} = \frac{\frac{K_{VCO}}{s}}{1 + \frac{K_{PD} Z_{LF}(s) K_{VCO}}{Ns}} \tag{A.9}$$

The phase noise simulations are performed in Advanced Design System (ADS). The

simulation result is shown in Figure A-3 (a). Since the transfer function from VCO phase noise to output phase noise indicated in equation 4.22 is a high-pass characteristic. The far-offset phase noise of the PLL is dominated by VCO. The close-in offset phase noise of the PLL is dominated by the reference source. The phase noise reduction of the DSPD PLL comparing to the conventional PD PLL can be shown in Figure A-3 (b). The close-in offset phase noise can be reduced 6dB due to the loop bandwidth extension of the DSPD PLL.

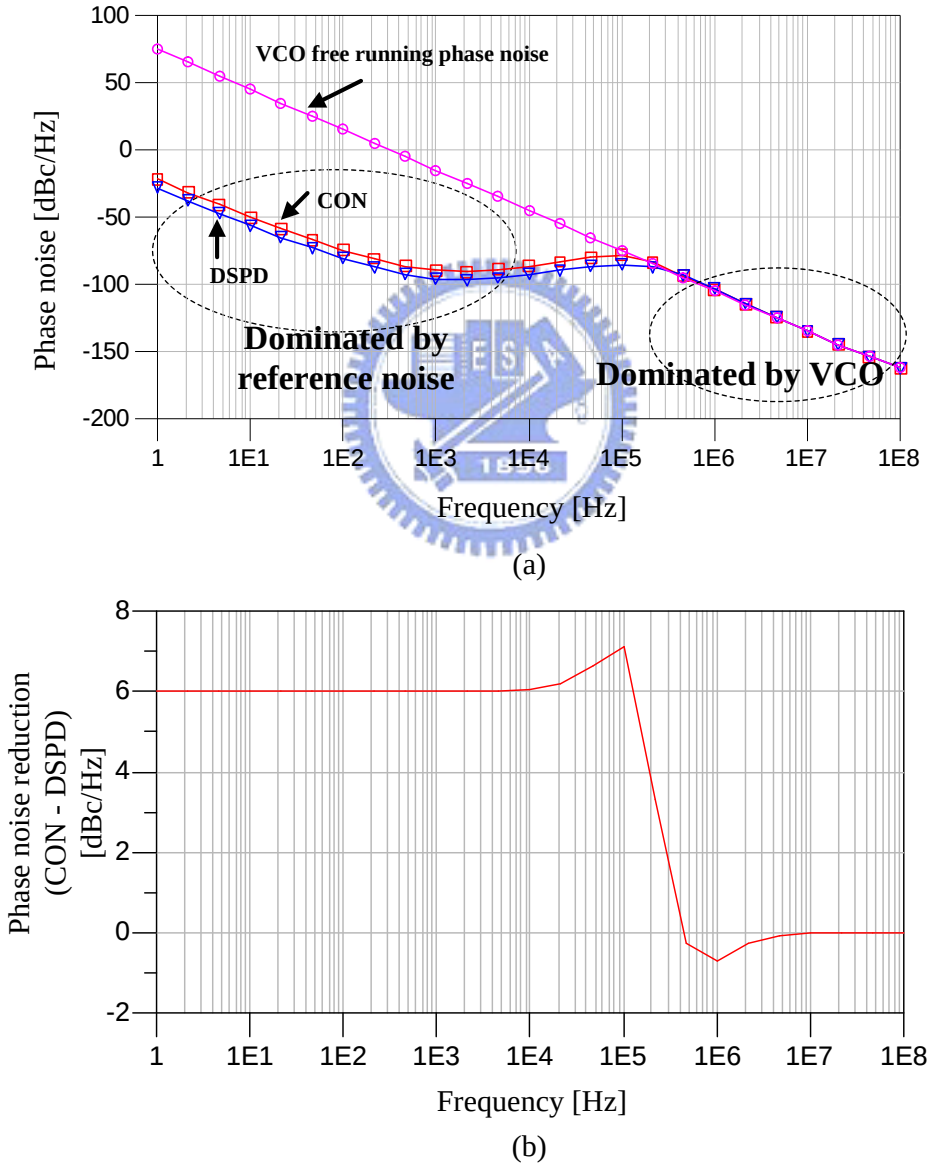

Figure A-3 Phase noise simulation.

Vita

姓名：黃國爵

性別：男

出生地：桃園縣

生日：民國七十二年九月二十七日

地址：桃園縣中壢市自忠二街 188 號

學歷：國立交通大學電子工程研究所碩士班　　2006/09~2008/06

國立中興大學電機工程學系　　2002/09~2006/06

桃園縣國立中壢高級中學　　1999/09~2002/06

論文題目：Phase-Locked Loop Design with Double Sampling Phase detector

應用倍頻取樣相位偵測器之鎖相迴路設計