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碩 士 論 文

具干擾偵測功能之 WiMAX 射頻前端接收器設計

An Interference Aware RF Receiver Front-End Design for WiMAX Applications

研 究 生：林佳欣　　Chia-Hsin Lin

指導教授：溫瓌岸　博士　　Dr. Kuei-Ann Wen

共同指導：溫文燊　博士　　Dr. Wen-Shen Wuen

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摘要

本論文主要討論應用於 WiMAX 系統之具干擾偵測功能射頻前端接收器設計。本文提出一個干擾偵測的機制，可應用於偵測干擾訊號的大小相對於系統想要的訊號。同時也提出具有可控制的雙模線性度(高線性度: 高耗電 ; 低線性度: 低耗電)的射頻前端接收器。將上述電路整合，可在環境干擾大於某個程度時，干擾偵測機制可控制射頻前端接收器於高線性度模式; 反之，則控制於低線度模式。高線性度模式比低線性度模性在射頻接收器的系統模擬上，多增加了 5.5dB 的干擾容忍值。此系統架構電路是以 0.18 微米 CMOS 製程實現。

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Department of Electronics Engineering
Institute of Electronics
National Chiao-Tung University

Abstract

In this paper, an interference aware scheme is proposed with RF receiver front-end design for WiMAX application. The interference level can be sensed via the proposed scheme for the adjustment of RF front-end linearity performance which corresponds to the system interference tolerance hence avoids unnecessary power consumption. A RF receiver front-end including a low noise amplifier and a mixer with dual modes of high linearity and low linearity are applied to demonstrate the proposed interference aware scheme for WiMAX application. By applying the proposed interference aware scheme with dual modes RF front-end, 5.5dB improvement of system interference tolerance can be achieved. These circuits are fabricated in 0.18um CMOS process.

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Chapter 1

Introduction

WiMAX (Worldwide Interoperability for Microwave Access) is based on IEEE 802.16 standard for Metropolitan Area Networks (MAN). Its goal is to deliver wireless broadband access to customers using base stations with coverage distances in the order of miles. In a WiMAX system, not all users' applications are of the same. Browsing the web, emailing, sending/receiving video, downloading files, or using VOIP are all activities that might be performed simultaneously within the population of users. In the case of WiMAX, the signal levels received at the mobile and base station terminals are important since mobile terminals that confront better power ratios of the carrier signal over interference signal can be reached using higher order modulation schemes (such as 64QAM) therefore increasing the capability of users.

1.1 Motivation

The mobile equipments in WiMAX system is designed to keep high quality of data transferring in the system coverage area. Most users use the wireless system in the urban area, and the toughest situation for data transferring usually occurs here, due to buildings shielding and interferences from many other users. On the other hand, because many users access WiMAX system at the same time and place in urban area, it is a serious problem in signal interference. Thus the linearity of receiver is an important issue. For increasing the data rate and capability, the high order modulation is required but it is sensitive to interference. Combining these conditions, high linearity is needed for receivers, and this is a great challenge for RF front-end receiver circuit design.

Several circuit techniques have been proposed to improve linearity of receiver front-end circuits. However, [1], [2], and [3] have the drawback of higher power consumption compared to the conventional structure and [4] has reliability issue. For these reasons, this thesis proposes a new architecture named interference aware scheme and receiver front-end (LNA and Mixer) with higher reliability linearity technique to release the trade-off between linearity performance and power consumption.

The research goal in this thesis is to implement receiver front-end circuits with dual linearity modes (high and low linearity). An interference aware scheme is also implemented to collocate with dual linearity modes front-end circuit. Combining these two circuits could have suitable linearity performance according to different adjacent/nonadjacent interference level.

1.2 Receiver Specifications

From the naming of WiMAX system, the major characteristics of this system are “worldwide” and “interoperability”. With these two characteristics, WiMAX open the technology to a wide variety of applications. In this section, we first decide the frequency band. The receiver specification and architecture are introduced in following two subsections. The specification of the receiver front-end is calculated from requirements of receiver, and it is presented on the last of this section.

1.2.1 Frequency Band Selection

There are two interesting frequency bands of WiMAX application, one is 10-66GHz for the line-of-sight (LOS) environment and the other is 2-11GHz for non-LOS environment. In the 2-11GHz operation band, IEEE 802.16e adds mobility and enables applications on notebooks and PDAs in the frequency range of 2-6GHz. The band range does not unified from country to country, but there are some usually referenced bands from USA as Table 1.1:

Table 1.1 WiMAX reference bands in 2-6GHz range

	Bands	Frequencies
Licensed Band	Wireless Communication Services (WCS)	2.305-2.320GHz 2.345-2.360GHz
	Multichannel Multipoint Distribution Service (MMDS)	2.5-2.69GHz
	Fixed Wireless Access (FWA)	3.4-3.7GHz
License-exempt	Industrial Scientific Medical (ISM)	2.4-2.4835GHz
	Unlicensed National Information Infrastructure (U-NII)	5.25-5.35GHz 5.725-5.825GHz

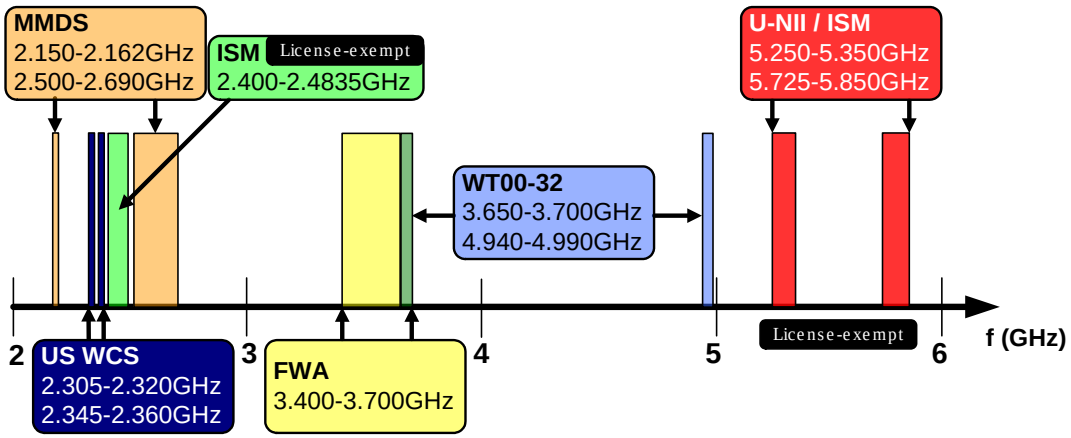


Figure 1.1 Bands for WiMAX Applications in 2-6GHz range

In this thesis, we focus on the first band of the WiMAX 2.3-2.7GHz and its range is shown in Figure 1.1. In this band, the WCS, ISM and higher part of MMDS applications are covered.

1.2.2 Receiver Specifications

In the IEEE 802.16-2004 standard [5], there are four air interfaces which operates in frequency band below 11GHz: WirelessMAN-SCa, WirelessMAN-OFDM, WirelessMAN-OFDMA and WirelessHUMAN. In this thesis, WirelessMAN-OFDM interface is focused.

A. Sensitivity

From the IEEE 802.16-2004 document, the required BER (bit error ratio) shell be less than 10^{-6} in WirelessMAN-OFDM interface. The receiver maximum input signal is -30dBm in both two interfaces, too. But other receiver requirements, such like sensitivity and adjacent channel rejections, are different between interfaces.

Following the IEEE 802.16e-2005 document [6], assuming 5dB implement margin and 8dB NF for receiver chain, the input sensitivity specifications in OFDM interface shell be:

$$R_{SS} = -101 + SNR_{Rx} + 10 \cdot \log(F_s \cdot \frac{N_{used}}{N_{FFT}} \cdot \frac{N_{subchannels}}{16}) \quad (1.1)$$

Where

SNR_{Rx}: the receiver SNR in dB, depends on modulation scheme and coding rate.

F_s: sampling frequency in MHz, $F_s = floor(n \cdot BW/8000) \times 8000$.

N_{used}: Number of used subcarriers, default is 200.

N_{FFT}: Smallest power of two greater than Nused.

$N_{subchannel}$: the number of allocated subchannels (default 16 if no subchannelization used)

From Table 1.2, when the BPSK modulation and 1/2 coding rate are used, the SNR reaches a minimum number as 3dB. The minimum channel bandwidth is 1.5MHz, n=86/75 for 1.5MHz BW. Combine these conditions into Eq. (1.1), we can derive the minimum input signal shall be -96.7dBm.

Table 1.2 Receiver SNR assumptions of WirelessMAN-OFDM interface

Modulation	Coding Rate	Receiver SNR of OFDM (dB)
BPSK	1/2	3.0
QPSK	1/2	6.0
	3/4	8.5
16-QAM	1/2	11.5
	3/4	15.0
64-QAM	1/2	N/A
	2/3	19.0
	3/4	21.0

B. Adjacent and non-adjacent channel rejection

The adjacent and non-adjacent channel rejection requirement of both interfaces is listed in Table 1.3. The requirement is identical in both interfaces.

Table 1.3 Adjacent and non-adjacent channel rejection

Modulation	Adjacent Channel Rejection (dB)	Nonadjacent Channel Rejection (dB)
16-QAM 3/4	11	30
64-QAM 2/3	4	23

The input third order intercept point (IIP3) is a linearity factor of receiver, and it can be derived from:

$$IIP3 = \frac{3 \cdot P_{blocker} - P_{desired} + SNR_{required}}{2} \quad (1.3)$$

Where

$P_{blocker}$: the adjacent or non-adjacent channel blocker level in dB.

$P_{desired}$: the desired signal, which is 3dB above the sensitivity.

From Eq. (1.3), the normal IIP3 of receiver in OFDM 16QAM 3/4 modulation is -18dBm for NCR = 23 dB. If the NCR = 30 dB for extreme situation, the maximum IIP3 is -9dBm. The maximum IIP3 requirement for the overall receiver is difficult to achieve with traditional circuits. Hence the thesis proposes new architecture to meet the linearity requirement at different interference situation.

1.2.3 Receiver Architecture

Figure 1.2 illustrates the system architecture of WiMAX receiver. Recently the direct conversion architecture for receiver is very popular and has been presented in many literatures. This architecture is also adopted in this research. There are many advantages of direct conversion receivers, such as reducing image rejection devices and simplifying integration of blocks, which can help to save power consumptions and to realize the system-on-chip integration. On the other hand, the drawbacks of direct conversion receiver are problems of DC-offset, I/Q mismatch, even-order distortion and flicker noise.

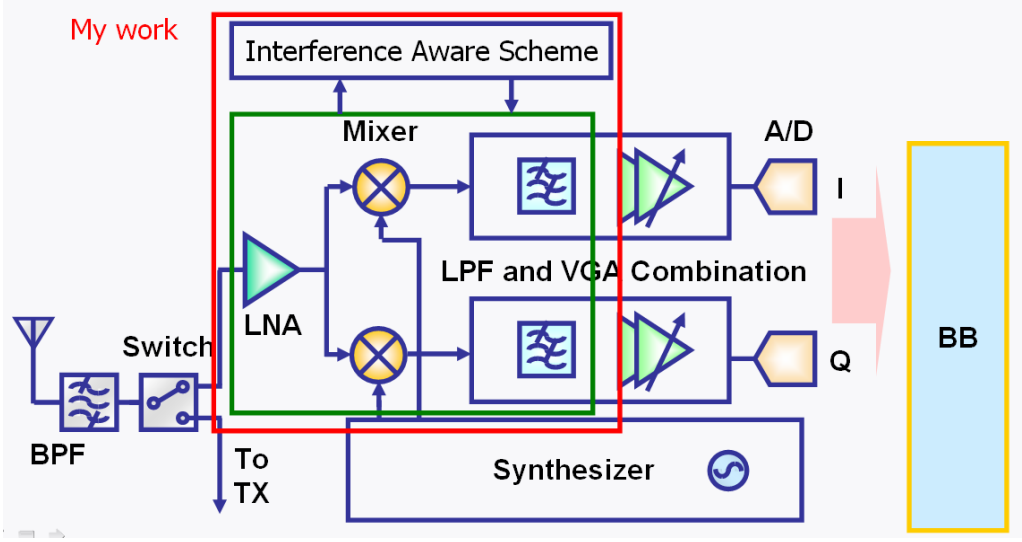


Figure 1.2 System architecture of WiMAX receiver

In the receiver architecture, a band pass filter and a Transmit/Receive switch are the first two blocks. The proposed receiver front-end is the next block. LNA, mixer, IAS, and LPF are implemented in the thesis.

1.2.4 RF Receiver Front-End Specifications Calculation

Since the receiver sensitivity is -102dBm, and the maximum input signal is -30dBm, the receiver dynamic range can be derived as -102-(-30) = 72dB. This range is derived on the condition of NF<8dB. IIP3 of receiver is also derived as -18dBm. By introducing dual gain mode method to receiver front-end, the dynamic range can be split into two modes: high gain mode for small input power signal, and low gain mode for large input power one. The specifications of blocks list on Table 1.4.

Table 1.4 The receiver block specifications

	BFP	Switch	LNA	Mixer	HPF	LPF	VGA	Unit
Gain(H)	-1	-1	**17**	8	10	-3	70	dB
Gain(L)	-1	-1	**8**	8	0	-3	25	dB
NF	1	1	**2.5**	10	15.1	21	21	dB
IP1dB(H)			**-15**	0.25V	0.31V	0.5V	0.35V	dBm/V
IP1dB(L)			**-5**	0.25V	0.31V	0.5V	0.35V	dBm/V
IIP3(H)			**-4.5**	0.84V	1.02V	1.68V	1.17V	dBm/V
IIP3(L)			**5.5**	0.84V	1.02V	1.68V	1.17V	dBm/V
NF, cas	6.86	5.86	4.86					dB
IIP3(H), cas			-24.54					dBm
IIP3(L), cas			-8.89					dBm

If the WiMAX receiver confronts severe interference situation (NCR = 30dB), the linearity performance of the front-end (LNA + Mixer) must be better than -9 dBm. That is a tremendous design challenge for conventional receiver front-end circuit.

1.3 Previous Techniques for the Linearity Improvement

The continuous scaling of CMOS technology makes the design of high gain, low noise, and low power consumption of CMOS LNA and mixer achieve great success. Nowadays high performance wireless receivers require high linearity, however, the receiver circuit impairments, such as inter-modulation distortion (IMD) and gain compression can seriously limit the receiver linearity. In addition, the linearity of MOS transistors still can not meet the strict requirements of WiMAX system without the cost of high power consumption. This evokes the requirement of linearization technique for CMOS LNA and mixer. Several circuit techniques have been proposed to improve IIP3 linearity of RF receiver front-end circuits as in [1],[2],[3] and they will be discussed in following sections.

1.3.1 Degeneration of the Input Gm-Stage

Either resistive or inductive degeneration can be used for the linearization of the LNA and mixer input stage. Resistive degeneration consumes less chip space but increase noise. In low-power applications and low-voltage processes the voltage drop over the resistance reduces the headroom of the transistors. By using inductive source degeneration these problems can be avoided at the cost of increased silicon area. In Figure 1.3 the IIP3 as a function of the gate voltage is presented with degeneration inductances for a simple common-source MOS amplifier.

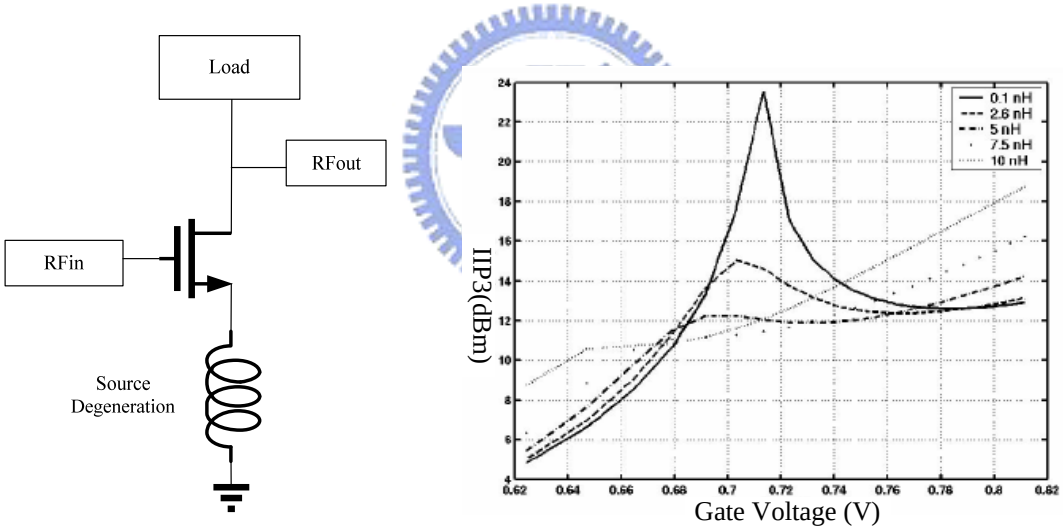


Figure 1.3 The IIP3 of a simple MOS amplifier with degeneration inductance [1]

With larger degeneration inductance, higher IIP3 is possible to achieve. From the Figure 1.3, for higher IIP3 higher gate-source bias voltage is required, which consumes more power at the same time.

1.3.2 IM3 Cancellation Techniques

Several literatures presented circuit topologies to improve the linearity by using IM3 cancellation [2] and [3]. Usually these approaches achieve higher IIP3 by means of splitting one signal path into two parallel signal and auxiliary paths that have different qualities. When the resulting signals are combined, the wanted signals have an equal phase and the IM3 tones are in opposite phase canceling each other.

A. Active Post-Distortion Technique

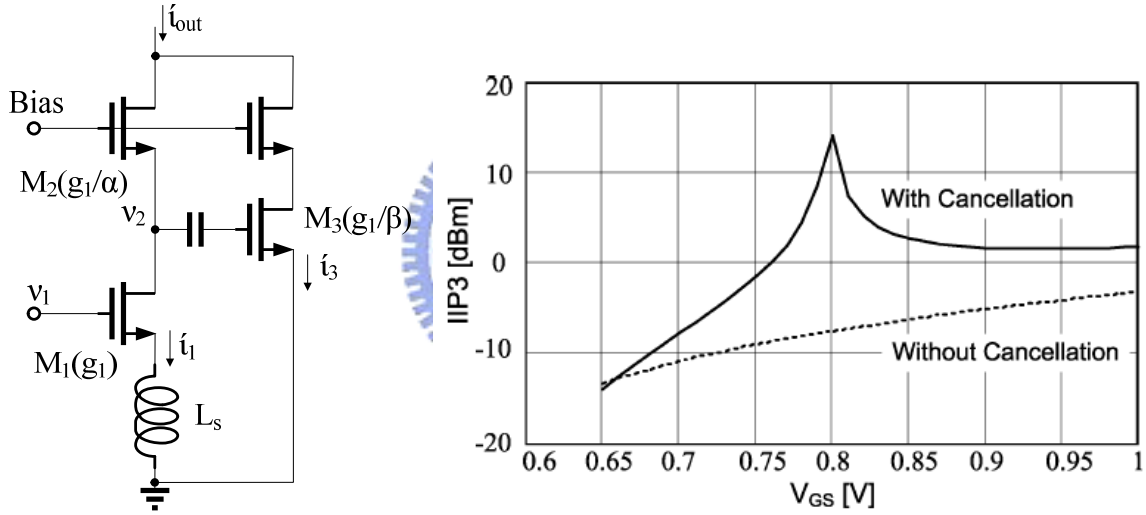


Figure 1.4 Schematic diagram of APD technique and its linearity performance[2]

The linearization technique is shown in Figure 1.4, where M1 and M2 form the main signal path, and M3 and M4 form the auxiliary path used for distortion cancellation. Where g_1 is the small-signal transconductance, g_2 is the first order derivative of g_1, and g_3 is the second-order derivative of g_1. From the conventional representation of time-invariant memoryless nonlinear system, the g_{3_out} can be derived as follows:

$$g_{3\_out} = g_3\left(1-\frac{a}{b}-\frac{a^3}{b}\right)+\frac{2\cdot(g_2\cdot a)^2}{g_1\cdot b} \tag{1.4}$$

By adjusting α and β values, the amplitude and phase of these nonlinearity can be optimized such that the maximum IIP3 can be achieve. However, the auxiliary path needs to consume extra power and the "sweet spot" of the IIP3 performance is sensitive to the process variation.

B. IM3 Cancellation by Duplicate Circuit

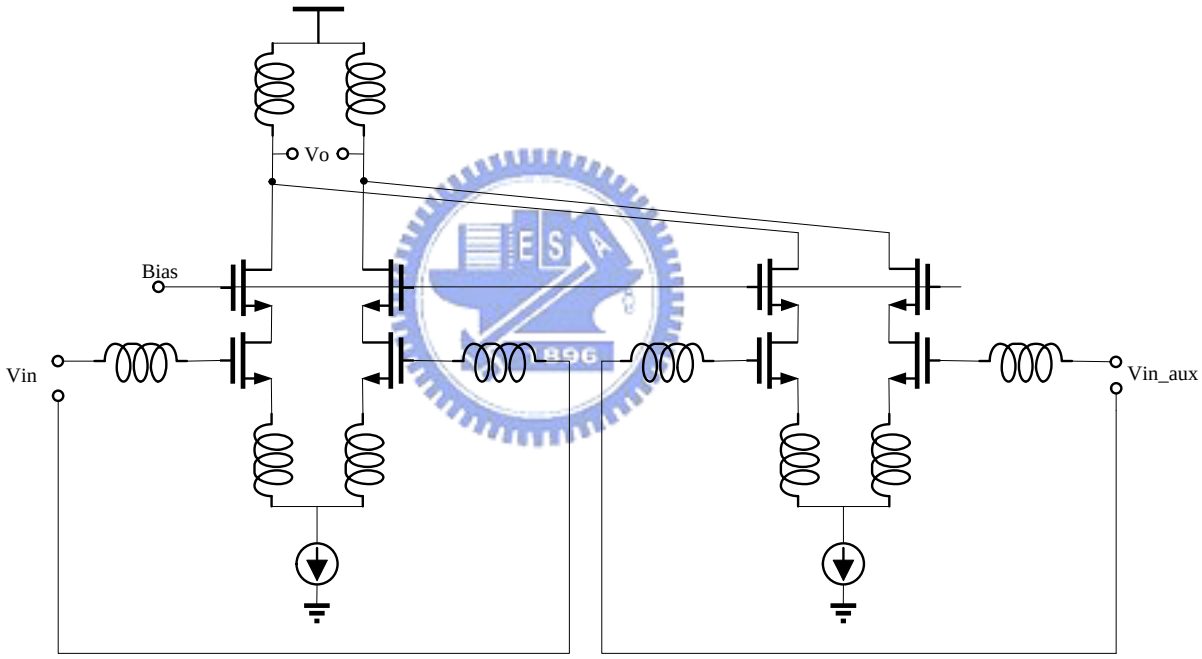


Figure 1.5 High linearity LNA circuit [3]

The second linearity enhancement topology is illustrated in Figure 1.5. The same structure is used for the main LNA and for an additional auxiliary LNA to cancel the 3rd harmonic. But the auxiliary LNA must consume power that is the same as main one.

1.3.5 Summary

Table 1.5 Reference performance of the linearization techniques

Reference	[2] Active Post-Distortion		[3] IM3 Cancellation by Auxiliary Path	
	Linearized	without Linearized	Linearized	without Linearized
Gain(dB)	16.2	16	15.5	18
NF(dB)	1.2	1.2	2.8	2.6
IIP3(dBm)	10.25	-2.5	18	5
Power (mW)	31.2	13	30	15
Ratio (mW/mW)	0.34	0.043	2.10	0.21
Process	0.25um CMOS		0.35um CMOS	
Operating Frequency	869~894 MHz		900MHz	

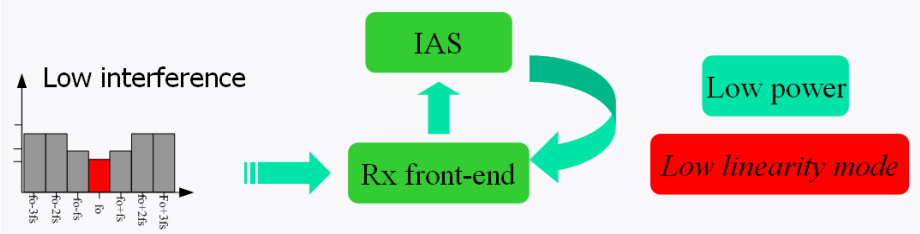
*Ratio = IIP3 (mW)/Power(mW)

In order to compare the efficiency of the linearization techniques, the performance measure for linearity enhancement can be expressed by the IIP3/Power Dissipation, since IIP3 is usually proportional to DC power consumption. According to Table 1.5, these linearization techniques discussed above not only improve the IIP3/Power with linearization but also consume more power compared to conventional circuit without linearization For the reason, this thesis proposes a new architecture named interference aware scheme to release the trade-off between linearity performance and power consumption.

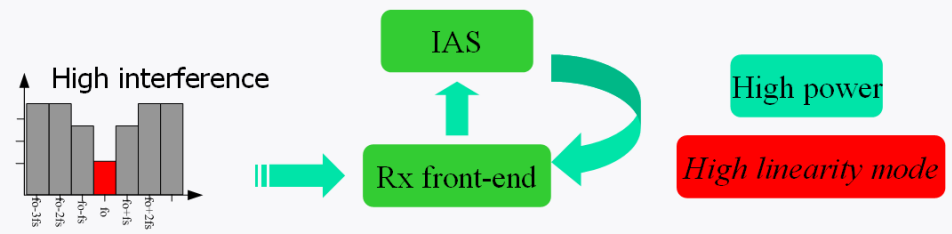
1.4 The Concept of Rx Front-End with IAS

According to specification calculation for WiMAX system, the linearity requirement for IIP3 is -9 dBm for the most interference situation. It is difficult to achieve with conventional receiver front-end circuit design. With aforementioned linearization techniques, receiver front-end circuits might meet the linearity requirement but would consume extra power to fulfill system interference rejection performance.

Because of the trade-off of these linearization technique, this thesis proposes a receiver front-end circuits (LNA and Mixer) with dual linearity modes (high and low) where high linearity mode consumes more power than low linearity mode, and an interference aware scheme to adaptively control the linearity modes of the receiver front-end circuits according to the interference situation. With the aid of interference aware scheme (IAS), the adjacent channel interference can be sensed and a signal can be created to control the RF front-end operation modes to meet system linearity requirement.



(a)



(b)

Figure 1.6 (a) lower interference situation (b) higher interference situation

The Figure 1.6 explains the behavior of the combination with IAS and RF front-end. If the receiver is in lower interference condition, the IAS will control the RF front-end to be at low linearity mode to save the power consumption. If system is in higher interference condition, the IAS will control the RF front-end to be at high linearity mode to meet the severe situation. So the combination with IAS and RX front-end design could release the trade-off between linearity performance and power consumption.

1.5 Power Efficiency Analysis

A power efficiency equation is proposed to determine whether the architecture is suitable for specified channel condition.

$$P_H \cdot x + P_L \cdot (1-x) + P_{IAS} \le P_R \cdot 1 \tag{1.5}$$

$$x \le \frac{P_R - (P_L + P_{IAS})}{P_H - P_L} = X_{TH} \tag{1.6}$$

P_H : power consumption of RF receiver front-end at high linearity mode

P_L : power consumption of RF receiver front-end at low linearity mode

P_{IAS} : power consumption of the IAS architecture

P_R : reference design power consumption

x : the probability of high interference condition

When the probability of high interference condition is less than X_{TH}, the IAS architecture is suggested to be adopted

1.6 Organization

The organization of this thesis is overviewed as following: Chapter 2 presents the design methodology of the interference aware scheme. In this chapter, a new architecture for sensing interference is proposed. Chapter 3 presents the circuit designs of the IAS and RF receiver front-end. Chapter 4 has the measurement results of the IAS and RX front-end circuits. Chapter 5 concludes with a summary of contributions and the future works.

Chapter 2

Interference Aware Scheme

In this chapter, the architecture of the interference aware scheme is introduced and each block of the IAS is explained in detail. The design flow of the IAS is also presented.

2.1 Design Concepts of RX Front-end with IAS

The IAS can sense the carrier signal and interference signal at the same time and compare these two signals. If the interference signal is great than some degree compared to carrier signal, the IAS sends a signal to make RF receiver front-end circuit (Mixer) be at high linearity mode. On the contrary, RF receiver front-end is at low linearity mode. That is, the proposed interference aware scheme can sense the interference level and then switch the modes of the RF receiver front-end circuit accordingly for better system interference tolerance or low power operation.

2.1.1 Determine Threshold S

Before describing the behavior of the IAS, we first discuss the threshold S. The relationship of EVM spec vs. interference with fixed carrier signal for dual linearity modes are shown in Figure 2.1. For a fixed carrier signal power, the low linearity mode can tolerance S dBm interference power and high linearity mode can tolerance more interference power than S dBm. According to the Figure 2.1, three conditions are defined as follows:

C-I < S High linearity mode

C-I > S Low linearity mode

C-I = S Holding mode

C: Carrier signal (dBm); I: Interference (dBm); S: threshold value (dB)

The proposed IAS should differentiate the three conditions and sends adaptive control signal to RF receiver front-end.

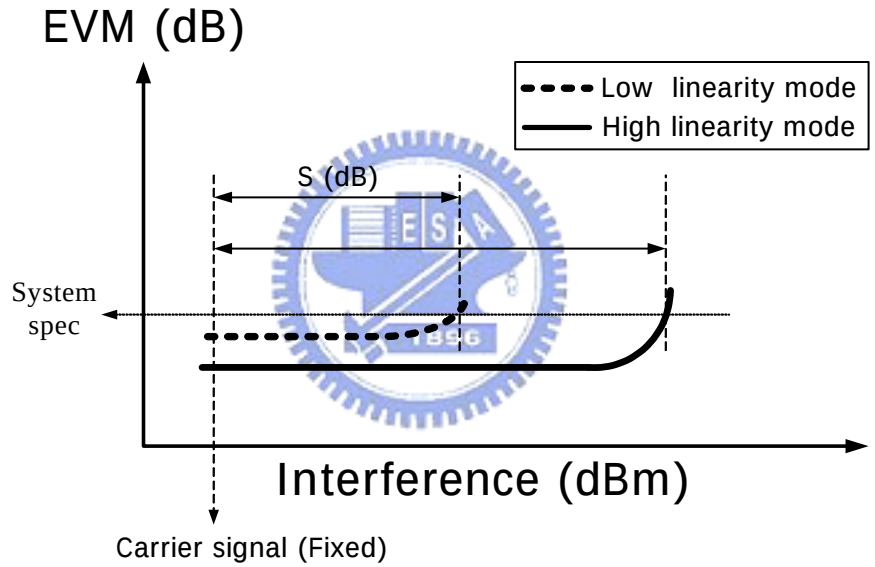


Figure 2.1 EVM vs. Interference with fixed carrier signal

2.1.2 The Behavior of the IAS

Figure 2.2 shows the behavior of the IAS. The carrier and interference signals first get into the receiver path and next into signal distinction. They are separated into two paths: Path_I (interference path) and Path_S (carrier path) and the gain difference of Path_I and Path_S is designed to be equal to S (dB). And then, these signals after signal distinction are sensed by peak detector and transfer amplitudes into peak levels for comparison. The error protection could avoid power wasted issue due to saturation

of amplifier. Finally, the mode selection sends a suitable controlled bias to RF receiver front-end according to the comparative results.

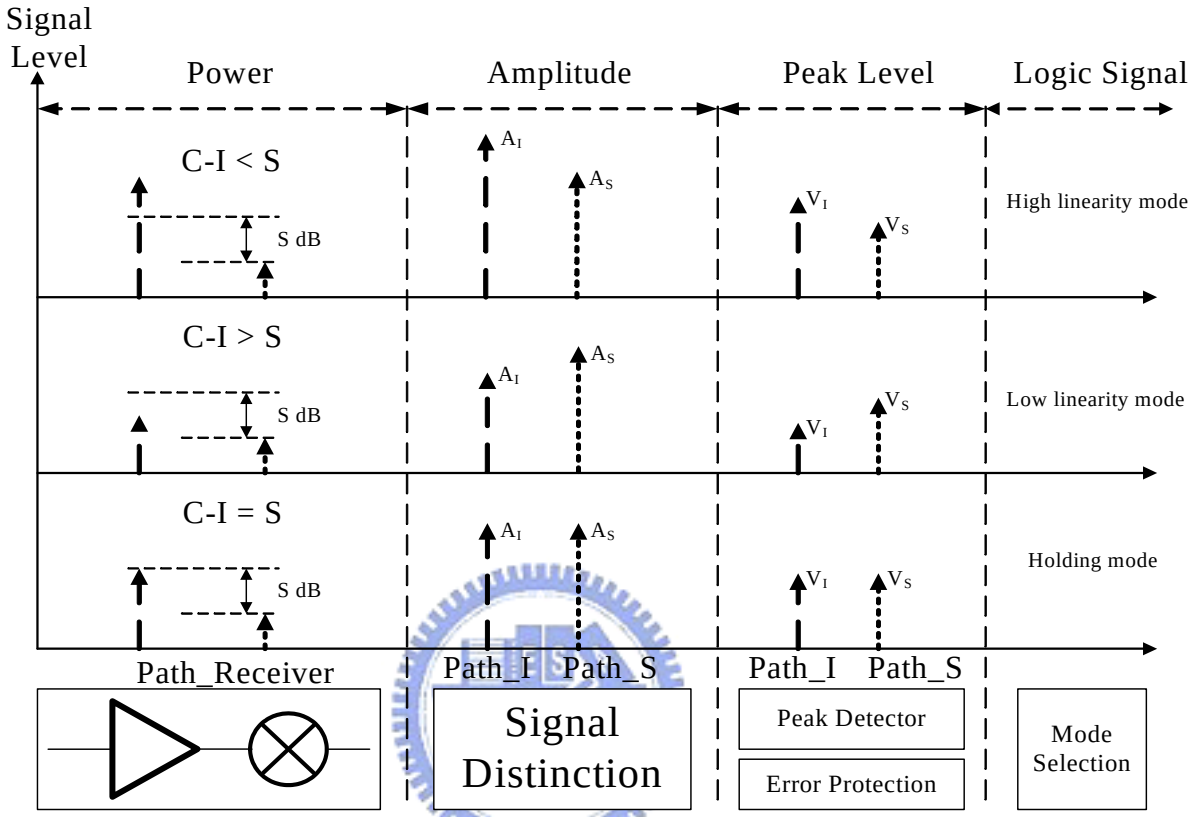


Figure 2.2 The behavior of the IAS

Dash line: interference signal

Dot line: carrier signal

2.2 The Components of the IAS

Figure 2.3 shows the architecture of the proposed interference aware scheme with RF receiver front-end. Building blocks of signal distinction, envelop detection, mode selection, and error correction are developed and designed under the system specifications and the performance of the receiver front-end circuit. Proposed interference aware scheme can sense the interference level and then switch the modes of the RF front-end circuit according channel conditions (C-I > S; C-I < S; C-I = S)

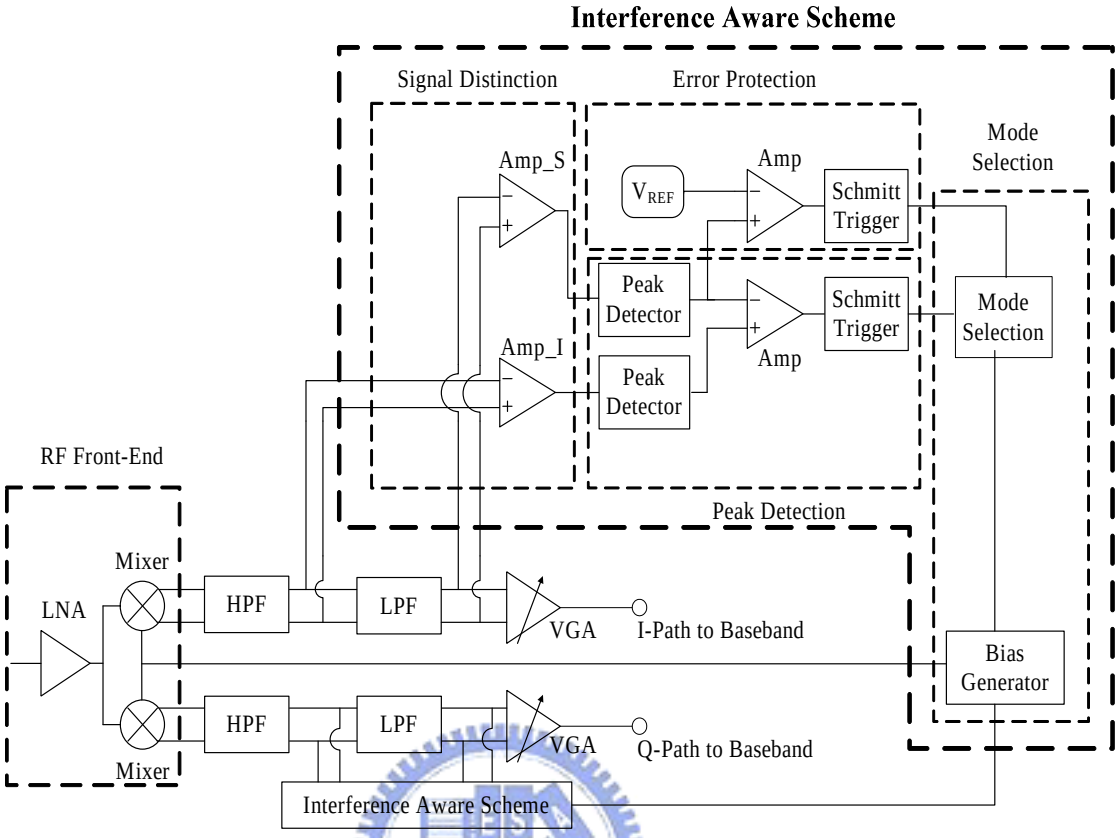


Figure 2.3 The proposed interference aware scheme with RF receiver front-end

Details of the four building blocks for the proposed interference aware scheme are being discussed as follows:

A. Signal Distinction

Three main components including a low pass filter and two amplifiers with different gain between carrier path and interference path are required to perform the signal distinction as shown in Figure 2.4(a).

In Figure 2.4(b), the signal distinction is built by the reject performance of LPF. In carrier path, the interference is filtered out by out-band rejection and carrier signal is reduced by in-band insertion loss. So the signal distinction could be achieved.

Gain response of carrier path: G_S + Loss
Gain response of interference path: G_I

For matching up the defined threshold S, the GI – (GS + Loss) = S must be satisfied.

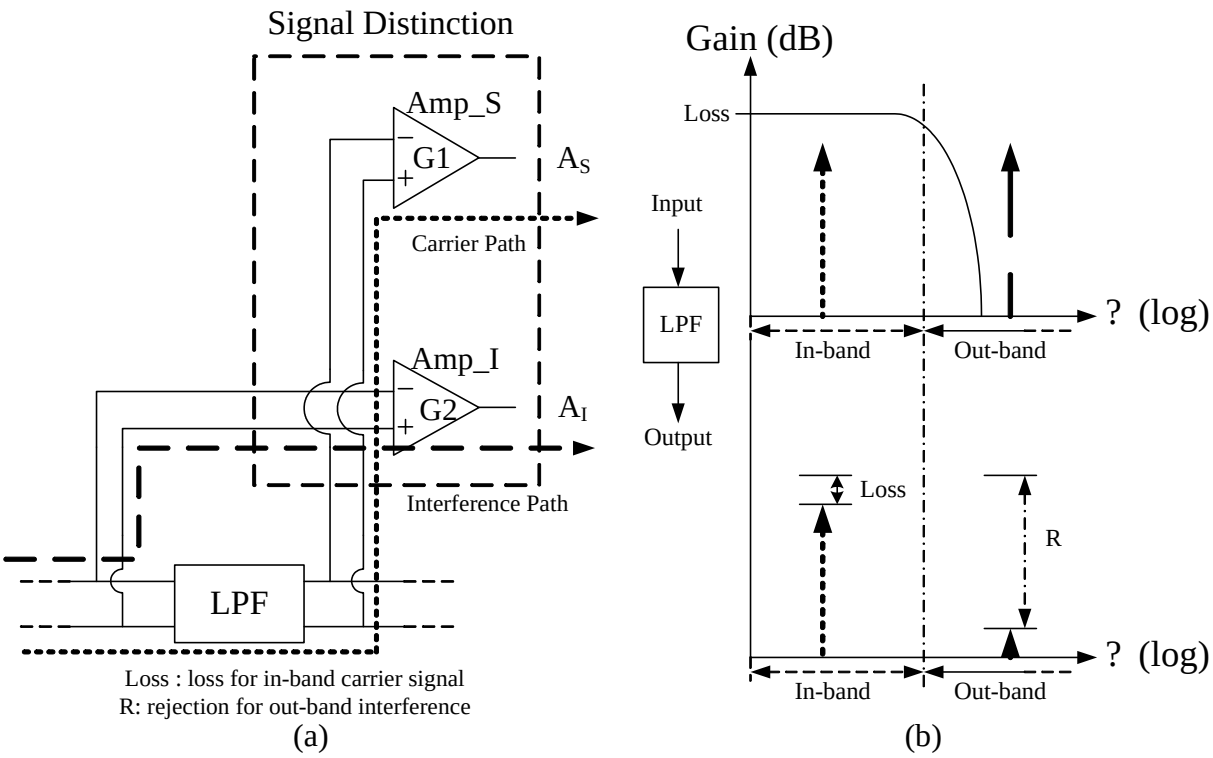
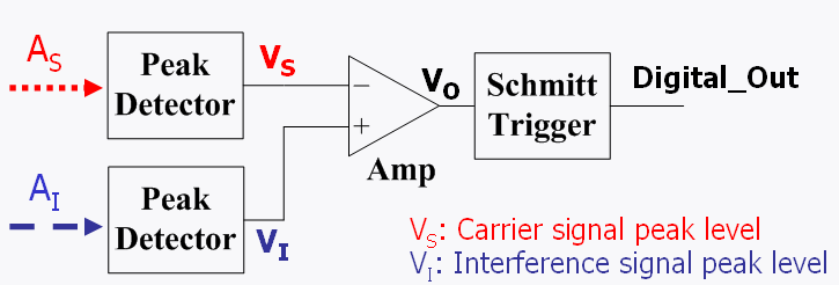


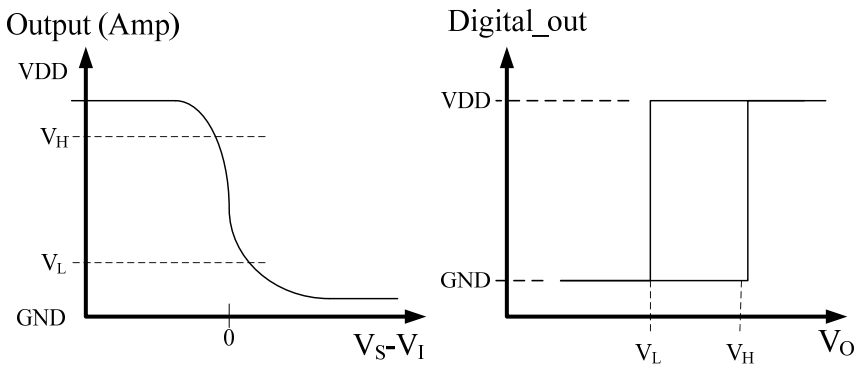
Figure 2.4 (a) The diagram of the Signal Distinction. (b) The behaviour of LPF Long dash: interference ; short dash: carrier

B. Envelop Detection

The output of the two paths from Amp_S and Amp_I are sent to the peak detectors for the peak level detection of the carrier signal and interference. A differential amplifier Amp is applied to compare the peak level difference and convert it into near VDD or GND with the transfer characteristic of Amp as shown in Figure 2.5 (b). However, an unstable state arises as the peak levels of the two signals are close, which may results in an uncertainty condition for the following stage of mode selection. This problem can be fixed by employing a Schmitt trigger after the Amp to remove the unstable state with its transfer characteristic as shown in Figure 2.5 (c).



(a)



(b) (c)

Figure 2.5 (a)The diagram of the envelop detector.
(b) The transfer characteristic of Amp and (c) Schmitt trigger

C. Error Correction

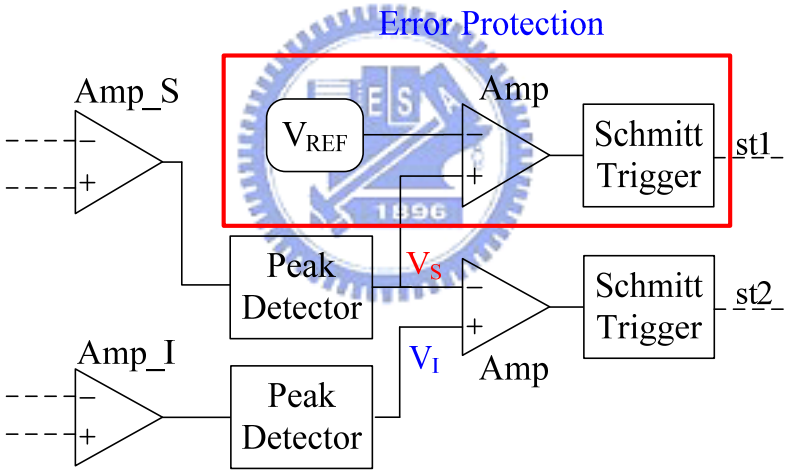


Figure 2.6 The diagram of the error correction

For the condition of both carrier signal power and interference power larger than a certain level that saturates Amp_S and Amp_I. The output peak levels from two paths' peak detector are the same and maximum values ($V_{S\_max} = V_{I\_max}$). According to the Schmitt trigger's characteristic, the IAS stays on sending the controlled signal of the previous mode called "locking mode." If the previous mode is high linearity mode and the channel condition is C-I > S (low interference), the RF receiver front-end has power wasted issue (low interference but in high linearity mode) when the IAS is in locking mode.

An error protection is proposed to solve the power wasted issue. The V_{REF} is slightly small than V_{S_max} (Amp_S is at saturation). When the $V_S > V_{REF}$, the Amp_S is at near saturation and the controlled bias signal of the low linearity mode is sent to RF receiver front-end to avoid power wasted issue.

D. Mode Selection

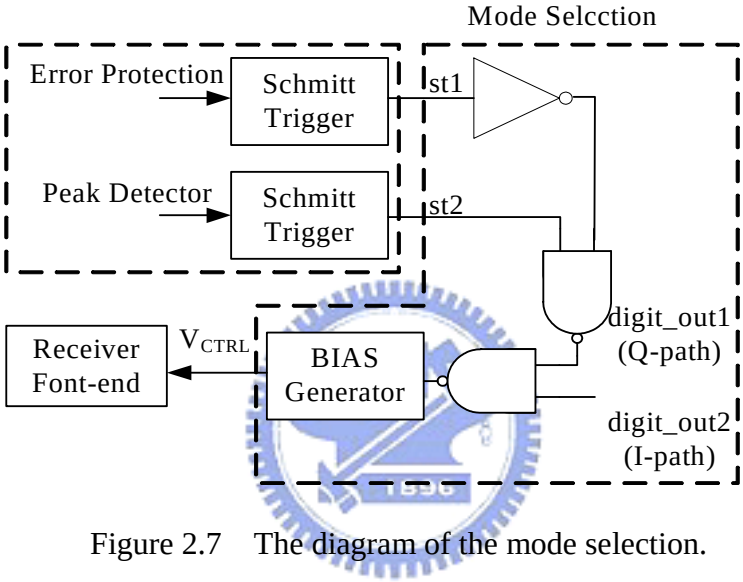


Figure 2.7 The diagram of the mode selection.

The mode selection circuit not only performs the Boolean operation for the signals from peak detection and error protection but also generates control voltages to RF front-end circuit from bias generator for the mode switching.

The Boolean operation for mode selection in shown in Eq. (2.1), where the inputs are from the outputs of Schmitt triggers, st1 and st2 which are in the peak detection and error protection circuits and a digital output of digit_out is created for the bias generator.

$$digit\_out = \overline{\overline{st1} \bullet st2} \tag{2.1}$$

After that, a bias generator creates a designed control voltage V_{CTRL} for the RF front-end circuit to bias the RF front-end at the selected mode. The summary for the mode selection operated in all conditions is shown in Table 2.1.

Table 2.1 Summary of mode selection

Condition	Saturation	st1	st2	digit_out	
C/I < S	VS >VREF	0	0	1	Low
	VS <VREF	0	1	0	High
C/I > S	VS >VREF	1	0	1	Low
	VS <VREF	1	1	1	Low

2.3 The Design Flow of the IAS

The design flow of the IAS is dependant on the main three parts: adaptive threshold S, sensitivity issues, and gain difference between interference path and carrier path. They are described in detail as followed:

A. Adaptive Threshold S

The ACI maximum requirement for the gap between WiFi and WiMAX is -15 dB from co-simulation (baseband and analog). For WiMAX 64QAM-3/4, the ACI requirement is -4 dB. From these two requirements, we can define the adaptive threshold S is the value between -4 dB and -15 dB.

B. Sensitivity Issues

1. WiMAX signal has the sensitivity level denoted by $W_{sensitivity}$.

2. The IAS also has the sensitivity issue caused from peak detector.

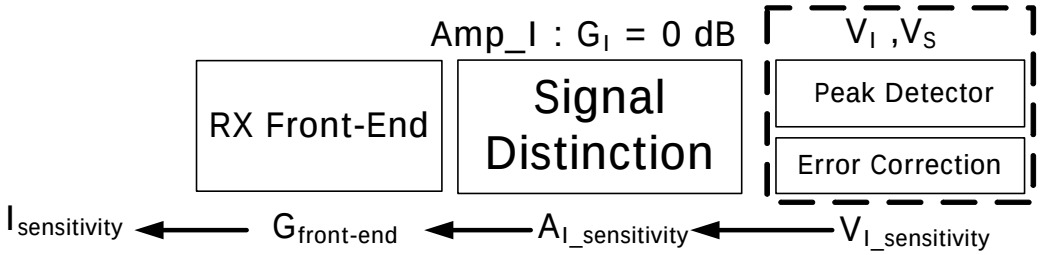


Figure 2.8 The sensitivity of the IAS

Because the IAS mainly focuses on the interference signal, the peak level's sensitivity of the interference path from peak detector is $V_{I\_sensitivity.}$ From Figure 2.8, the $I_{sensitivity}$ could be derived when G_I (the Amp_I's gain) is 0 dB. If the IAS wants to operate correctly when the carrier signal is at sensitivity level, the followed equation must be achieved.

$$G_I = I_{sensitivity} - (W_{sensitivity} - S) \quad (2.2)$$

C. Gain Difference

The gain difference is used to match up the threshold S and the following equation should be met.

$$S = G_I - (G_S + Loss) \quad (2.3)$$

Loss = -1 dB for LPF's design margin and the GS could be derived with followed equation.

$$G_S = G_I - S - Loss \quad (2.4)$$

Chapter 3

Circuit Design

In this chapter, these circuit designs of the proposed IAS and RF front-end are elaborated. Section 3.1 describes the circuit design of the RX front-end (LNA and Mixer) with dual linearity modes. In section 3.2, the designed RF receiver front-end is used to simulate the EVM performance on the co-simulation platform. Section 3.3 describes each circuit designs of the IAS. These circuits are designed in 0.18μm CMOS process.

3.1 RX Front-End Circuit Design

3.1.1 System View

In the system analysis, we will refer to the RF receiver front as to the system consisting of a LNA and Mixer, as shown in Figure 3.1. If G, NF and IP3 are the power gain, the noise figure and the third order intercept point of the corresponding circuits, as indicated in Figure 3.1, the equivalent noise and the linearity performance can be expressed by the Friis formulae, as given by Eq. (3.1) and Eq. (3.2).

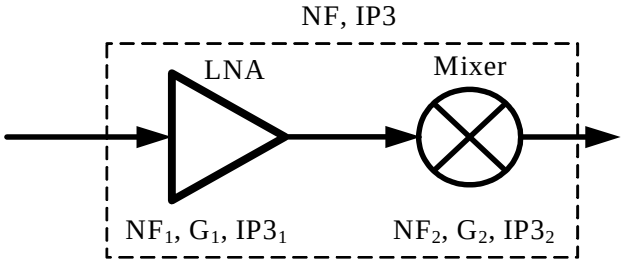


Figure 3.1 Simplified RX front-end model.

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} \tag{3.1}$$

$$\frac{1}{IP3^2} = \frac{1}{IP3_1^{\ 2}} + \frac{G_1}{IP3_2^{\ 2}} \tag{3.2}$$

where $IIP3_2$ is the mixer third-order interception point and G_1 is the gain of the LNA. With typical LNA gain values the mixer is usually limiting the linearity of the whole receiver. Meanwhile, the NF is dominated by LNA.

For the architecture of RX front-end with IAS, a RX front-end with dual linearity modes is needed. Because of above discussion, the function of dual mode linearity is achieved by the mixer with some linearity improvement techniques and the NF performance is optimized by LNA.

3.1.2 Circuit View

For the design of mode switching, a linearity analysis has been studied [7] and Eq. (3.3) shows the relation between IIP3 performance and power consumption for a simplified input stage.

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} = \sqrt{\frac{32}{3}\frac{I_D}{K_{RF}}} \tag{3.3}$$

where (α_1, α_2) is the first- and third-order intermodulation coefficients, I_D is the drain current, and K_{RF} is the transconductance parameter of the transistor. It can be seen that the IIP3 is mainly determined by the current and the size of the transistor. Hence, IIP3 is proportional to the square root of the current flowing in the input MOSFET.

From reference [1], an input amplifier stage with adaptive source inductive degeneration increases IIP3 performance.

3.1.3 Circuits and Summary

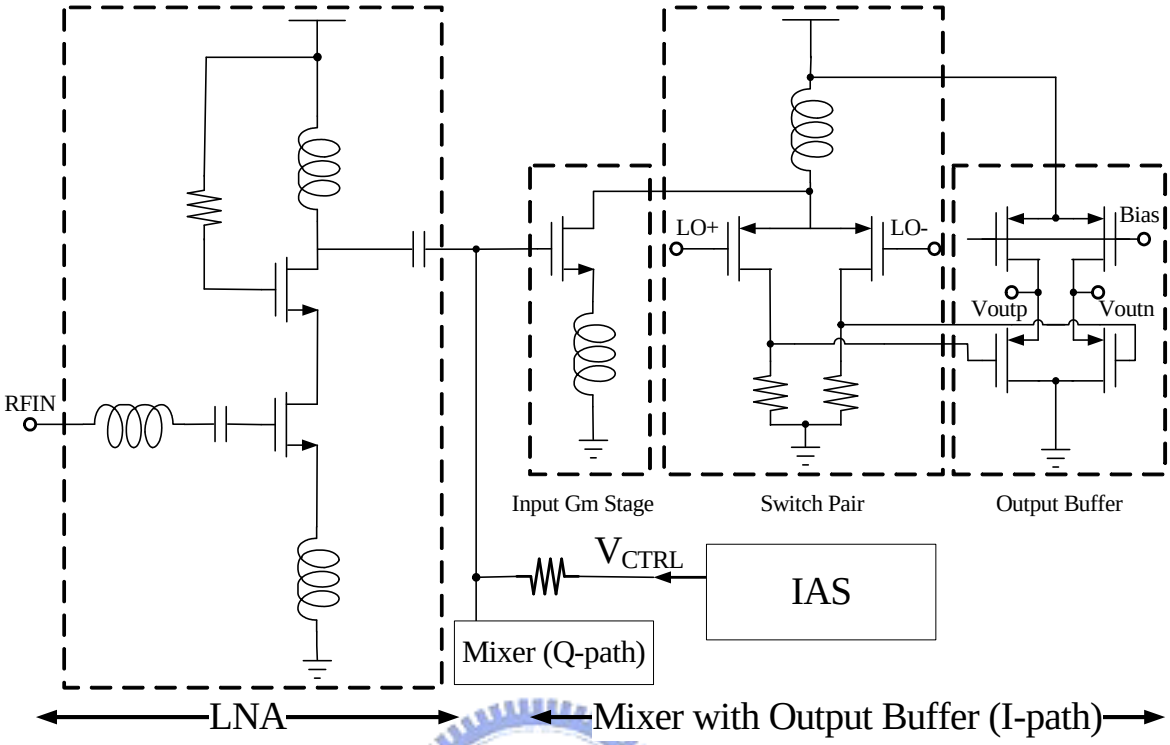


Figure 3.2 Simplified schematic of the RF front-end circuit

Figure 3.2 shows the receiver front-end circuits such as LNA and Mixer with output buffer. The folded mixer is adopted because it can decouple the trade off between noise figure and linearity [8]. Input gm stage in mixer is designed to be switchable for dual linearity modes by adjusting the bias voltage V_{CRTL} according to above linearization technique. The LNA is designed to reduce the noise figure and the cascode topology is adopted, because it uses less MOSFET and can be easily optimized for noise figure by reference [9]. Cascode topology also offers the highly reverse isolation (S12) performance.

The simulation results are shown in follows:

Table 3.1 The Performance of RF receiver front-end

Parameters	High linearity mode	Low linearity mode
Gain (dB)	25.2	25.7
NF (dsb) (dB)	2.6	2.56
IIP3 (dBm)	-7.7	-15.5
Power (mW)	28.1	13.7
Ratio (mW/mW)	0.6%	0.22%

* One LNA and two mixers for IQ-path

* Buffer's power consumption isn't included

V_{CTRL} is the bias voltage from IAS:

1. V_{CTRL} = 1.4 V high linearity mode (IIP3 = -7.7 dBm)
2. V_{CTRL} = 0.5 V low linearity mode (IIP3 = -15.5 dBm)

3.1.4 System Co-simulation

The co-simulation platform includes the baseband part and analog part. Using the platform can evaluate the EVM value the receiver performance under different channel conditions. The platform helps to evaluate how much interference can be tolerant under the system specification in the dual linearity modes.

A. Co-simulation Platform

The signal considered is WiMAX 64QAM-3/4 modulation signal and 20 MHz bandwidth for its highest IIP3 requirement. The carrier frequency is 2.6 GHz. The interference block is built and has the same modulation type as the desired signal. But its center frequency is 2.58 GHz as the adjacent channel interference. The platform is showed in Figure 3.3.

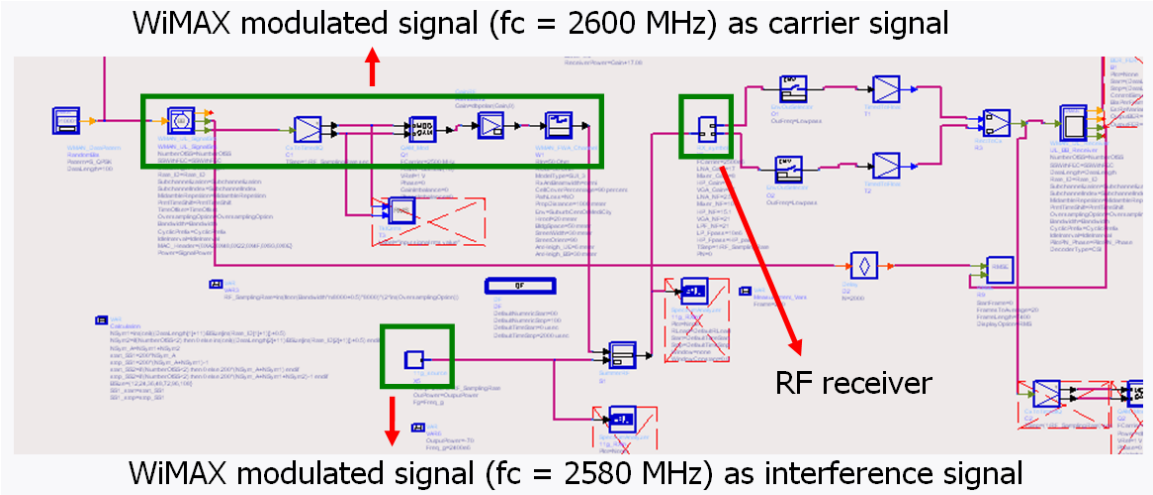


Figure 3.3 Co-simulation platform

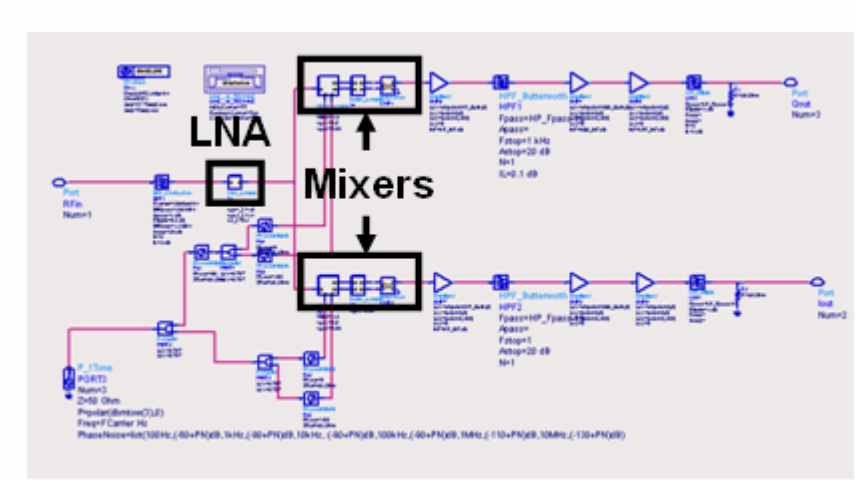


Figure 3.4 The RF receiver

Receiver front-end:

1. LNA and mixers are replaced with schematic level.
2. Others are the behavior model for reducing simulation time.

B. Simulation Results

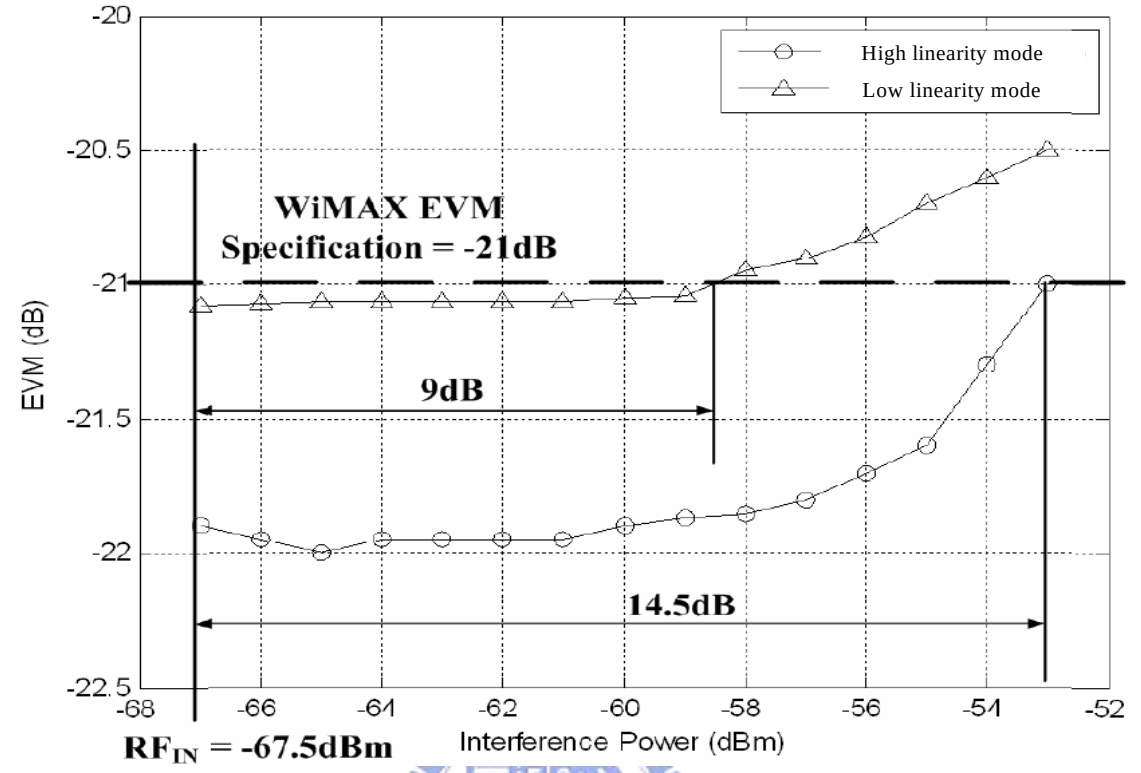


Figure 3.5 EVM vs. Interference with sensitivity carrier signal

System interference tolerance:

1. High linearity mode : 14.5 dB
2. Low linearity mode : 9 dB

S = -9 dB (Between -4 dB ~ -15 dB)

3.2 The Circuit Design of the IAS

The architecture of the IAS is composed of these circuits including amplifiers, peak detector, Schmitt trigger, and low pass filter (belong to RF receiver system). These circuit designs are described as follows.

3.2.1 Peak Detector, Schmitt Trigger, and Ampifier

The circuit design of envelop detection and error correction circuits are discussed together here.

A. Peak Detector

The schematic of the peak detector and the transfer characteristic are shown in Figure 3.6 (a) and (b).

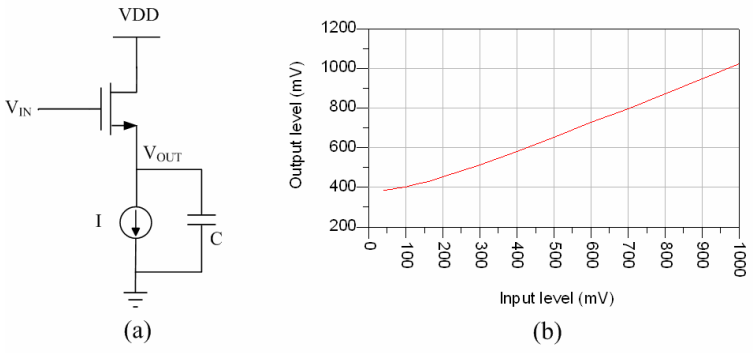


Figure 3.6 (a) Schematic (b) transfer characteristic of the peak detector

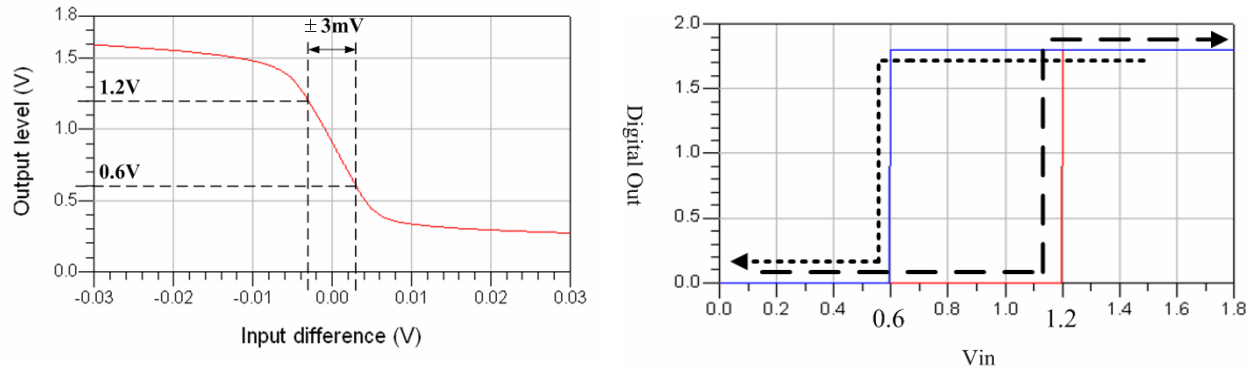
The peak level of the input signal is sensed by the peak detector and a corresponding output level is generated with a capacitor load to hold the value as the input for the following stage of a differential amplifier, Amp.

The value of the capacitor load is determined by the following equation [10]

$$C = I \times \frac{\Delta t}{\Delta Vo} \tag{3.4}$$

Where ΔVo is the lowest voltage level which can be sensed by the following differential amplifier, Δt is half the period of the slowest AC input signal and the current I is determined under the power budget.

B. Schmitt Trigger and Amplifiers



(a) Amplifier (b) Schmitt trigger

Figure 3.7 The transfer characteristic of the (a) differential amplifier (b) and Schmitt trigger

Figure 3.7 shows the transfer characteristic of the differential amplifier of the output level versus the peak level difference (desired signal minus interference). Based on the transfer characteristic of the differential amplifier, the Schmitt trigger in the following stage is designed with two trigger points of 0.6V and 1.2V that either converts the signal to VDD/GND or holds the last state for input difference larger or less than ± 3mV, respectively.

C. Sensitivity Issue

The IAS has a sensitivity issue. When the IAS has no input signal, the $V_I = V_S =$ 385 mV. From the Figure 3.7 (a), if the IAS wants to operate correctly, the $|V_I-V_S|$ should be great than 3 mV. With above analysis, the sensitivity value $V_{I\_sensitivity}$ is 388 mV and this value could help to calculate the G_I (Amp_I) and G_S (Amp_S) in next topic.

3.2.2 The Design Flow of the IAS

From the design flow of the 2.3 and the adaptive G_I and G_S can be derived.

A. Adaptive Threshold S

S = -9 (dB)

it meet the requirement discussed in 2.3 (S = -4 dB ~ -15 dB).

B. Sensitivity Issues

1. WiMAX 64QAM-3/4 sensitivity level = -67.5 dBm

$W_{sensitivity}$ = - 70 dBm with design margin 2.5 dB.

2. The IAS sensitivity $V_{I\_sensitivity}$ = 388 mV, it can be translated to $I_{sensitivity}$ = -59 dBm with G_I = 0.

$G_I = I_{sensitivity} - (W_{sensitivity}-S)$ = **20 (dB)**

C. Gain Difference

$G_S = G_I – S – Loss = 20 + 9 + 1$ = **30 (dB)**

From these result, the Amp_S and Amp_I can be determined.

3.2.3 Amplifiers with CMFB (Amp_I & Amp_S)

From above discussion, Amp_I and Amp_S with gains of 30dB and 20dB are used to enlarge the signal level to meet the sensitivity of the peak detection circuit. They should also have wide output range to enlarge the sensed range of the IAS. In addition, they must keep the output DC level constant to let the followed peak detectors sense the peak amplitudes based on the same DC level from Amp_I and Amp_S

For wide output range design consideration, a conventional differential pair with active load that generates a single-ended output is herein chosen for its simplicity. To

keep the output DC level constant, a current steering common mode feedback circuit is applied to overcome the process variation and small DC offset problems to improve the signal accuracy. The circuit is showed in Figure 3.8.

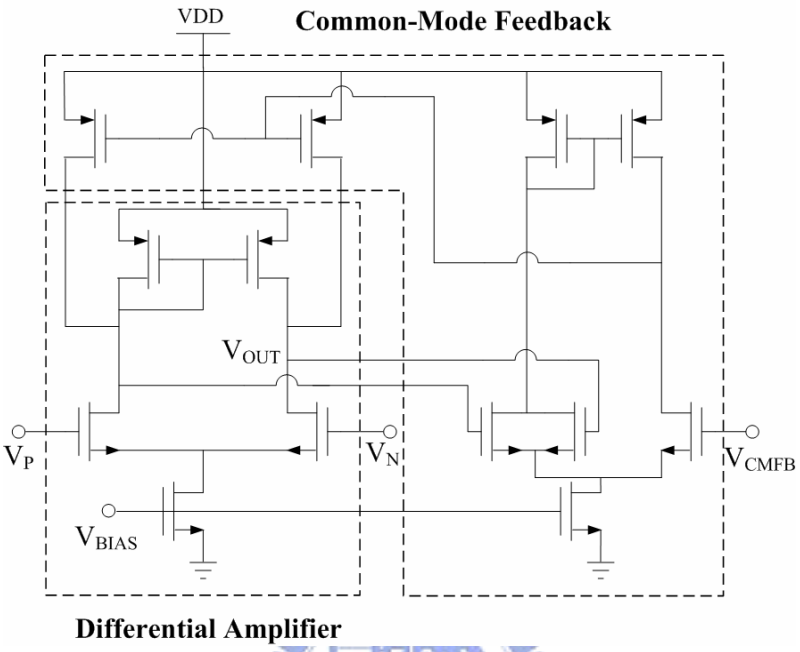
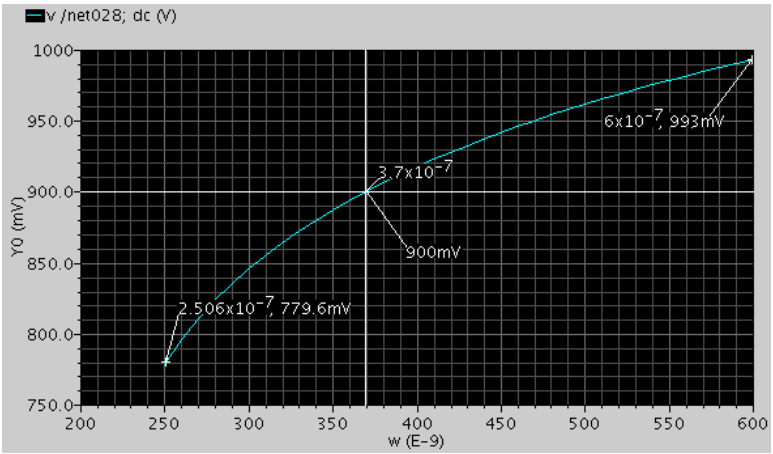


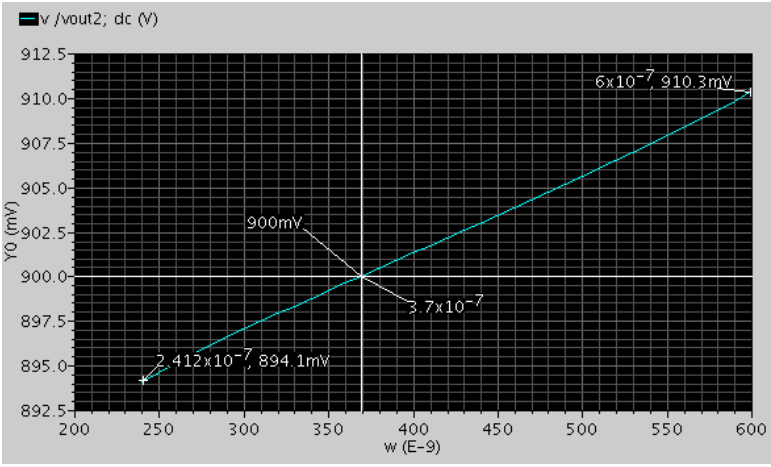
Figure 3.8 The circuit design of the Amp1 and Amp2 with CMFB

Table 3.2 Simulation result of the circuits

Components	Gain	Power	PM	F_{3dB}
Amp_S	30 dB	80uA/1.8V	75^{o}	12MHz
Amp_I	20 dB	80uA/1.8V	82^{o}	32MHz



(a) Without CMFB



(b) With CMFB

Figure 3.9 The DC level of the amplifiers' output with different process variation (The width size of the active load PMOS 250 nm ~ 600 nm)

From Figure 3.9 (a), the amplifier without CMFB has a varied DC output level from 779.6mV to 993mV with different width due to process variation. From Figure 3.9 (b), the amplifier with CMFB has a varied DC output level from 894mV to 910.3mV with different width. Based on a common mode dc 0.9V, the CMFB circuit is really effective to overcome the process variation.

3.2.4 5th-order Elliptic Filter

This LPF is used to filter out the adjacent interference. For the architecture of the IAS, highly rejection performance is required because of the differentiability of the desired signal and interference signal.

A 5th-order elliptic Gm-C LC ladder filter [11] is chosen for it's highly rejection ability of narrow transition band characteristic to filter the interference out. The filter employs a passive ladder type to have high dynamic range. The Gm cells are connected to gyrator with different values to reduce internal node peaking. The circuit diagram is show in Figure 3.10.

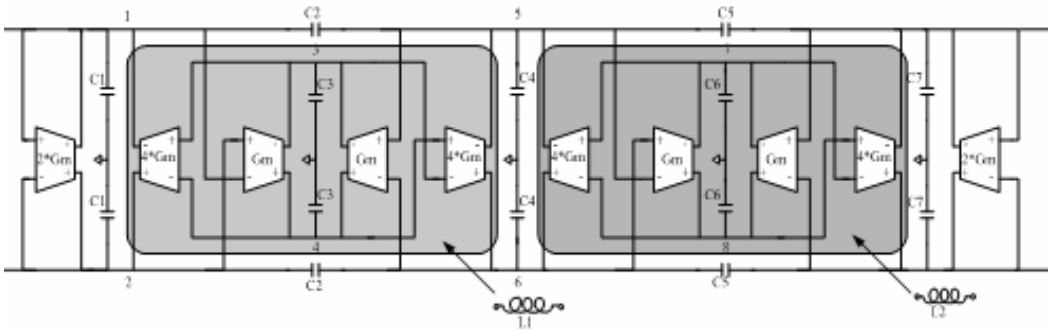


Figure 3.10 The architecture of the 5th-order elliptic Gm-C LC ladder LPF

The Gm cell is composed of two mainly techniques.

A. 1. Linearity Technique:

The linearity technique can combine two skills in order to further improve its linearity. Using cross-coupling and unbalance differential pairs together, then the gm core is called “Symmetric & Un-symmetric differential pairs” [12].

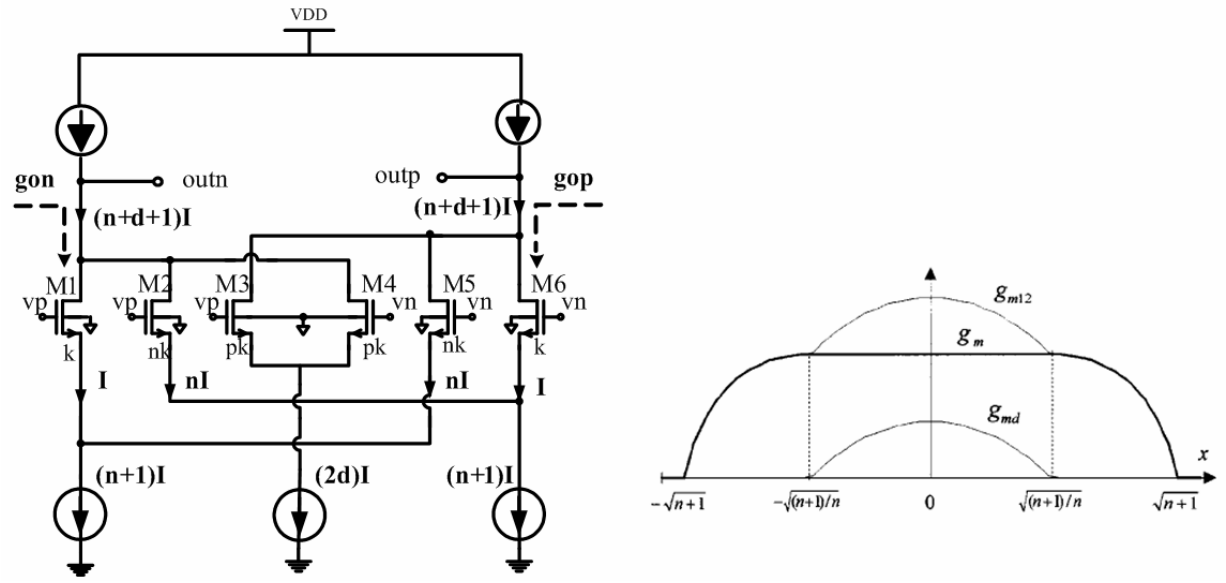


Figure 3.11 Symmetric & Un-symmetric pairs

Figure 3.11 shows the Gm cell by using symmetrical & unsymmetrical differential pair with negative impedance. NMOS M_5&M_1, M_2&M_6 have unsymmetrical aspect ratio n, and symmetrical pair M_3&M_4 makes gm as flat as possible. The transistors and current have different ratios:

$$M1:\ M2\ :\ M3\ =\ M6\ :\ M5\ :\ M4\ =\ 1:\ n\ :\ p \tag{3.5}$$

The gm can be obtained [12]:

$$gmd = \frac{4n}{(n+1)} \frac{n-1}{\sqrt{n(n+1)}} \sqrt{\frac{I}{k}} \tag{3.6}$$

where n is aspect ratio , I is normalized current, and $k = \frac{1}{2} mCox \frac{W}{L}$.

By choosing appropriate transistor ratio n, p, and d, the range of flat gm:

$$vid \le \left| \frac{(n+1)}{n} \sqrt{\frac{I}{k}} \right| \tag{3.7}$$

B. High Output Impedance Technique for Gm cell

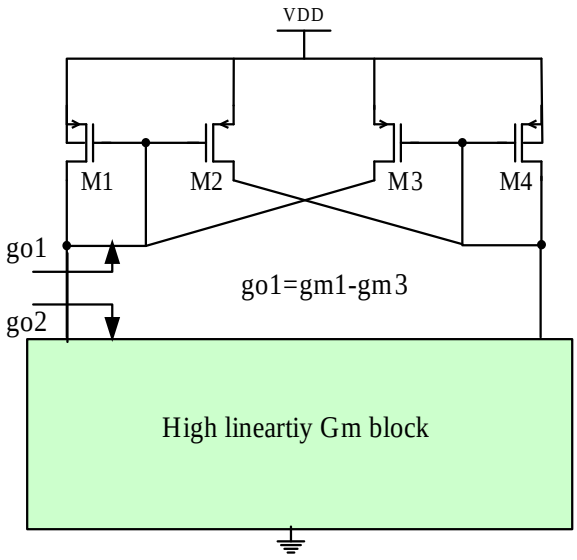


Figure 3.12 Negative Impedance Load

Considering the negative resistance load (NRL)[13] in Figure 3.12, M3 & M4 introduce local positive feedback between the output terminals m & n in Figure 3.11 which generate a negative resistance to compensate the parasitic output resistance of the whole transconductance circuit. The negative impedance load can be combined with the differential gm to increase their output impedance and design $g_o1=-g_o2$, then the output impedance is infinite (ideally). The advantage of NRL is that it only needs to bias at same current string, so it saves power.

The simulation results are showed as follows:

1. Gm-cell performance:

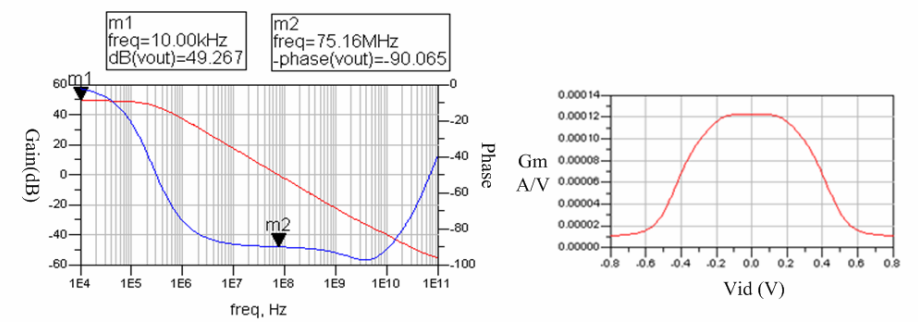


Figure 3.13 (a) Gain and Phase (b) Flat gm

2. 5th-order LC ladder elliptic filter:

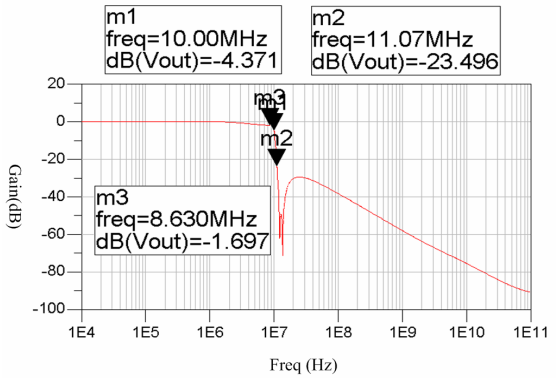


Figure 3.14 Frequency response of the LPF

Overall DC current is 2.571mA with power supply voltage = 1.8V. From Figure 3.14, the LPF has highly rejection performance (~ -19 dB) from 10 MHz to 11 MHz.

3.2.5 Summary

Table 3.3 Performance list of IAS

Components	Gain	power
AMP 1	30 dB	80uA/1.8V
AMP 2	20 dB	80uA/1.8V
AMP 3 & 4		40uA/1.8V
PD*2		30uA/1.8V
2*IAS power =0.828 mW for IQ-path		

As shown in Table 3.3, the power consumption is less than the RF receiver front-end. On the other hand, RF receiver front-end with IAS doesn't consume more extra power for detecting the interference level.

From the result of the system simulation discussed in Chapter 4, if the C/I sensed is less or equal to -9dB, the high linearity mode of RF receiver front-end will be activated by the mode selection circuit. Simulation results for C/I smaller than -9 dB with circuits saturated or not are demonstrated in Figure 3.15 (a) and (b), respectively; which agree with Table 2.1. The simulation results show that the functions are corrected worked for the proposed interference aware scheme. The settling time is about 10μs less than the channel coherence time (300μs).

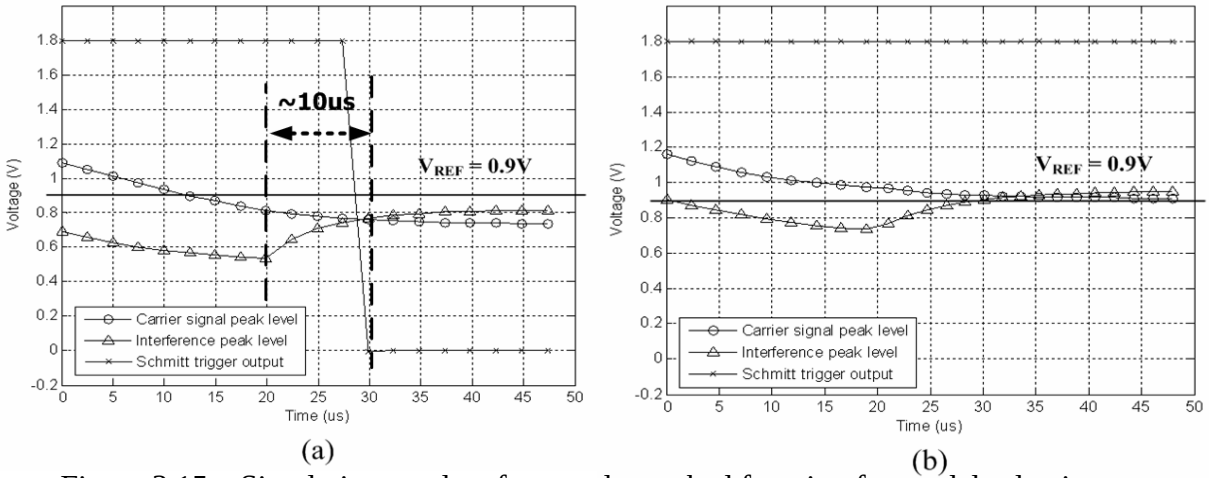


Figure 3.15 Simulation results of correctly worked function for model selection as (a) circuit saturated and (b) circuit not saturated

3.3 Analysis of the I/Q Mismatch Due to IAS

The quadrature RF receiver front-end has I-path and Q-path. Each path has an IAS circuit and it is possible to detect different interference levels at each path. In Figure 2.7, the mode selection uses the NAND gate for I and Q paths to avoid the I-Q mismatch issue. Any path that detects higher interference level will leads the RF receiver front-end into high linearity mode.

An interesting question is, if the IAS_I and IAS_Q detect different interference channel levels, do the unbalanced I/Q IAS conditions affect the quadrature receiver and generate I/Q mismatch issue?

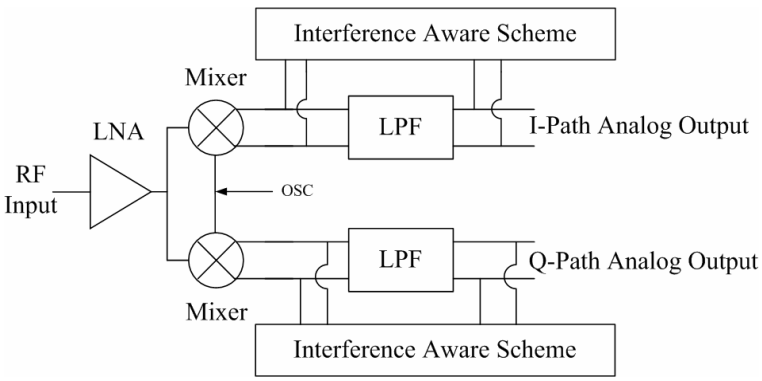


Figure 3.16 I/Q-mismatch test platform.

In Figure 3.16, assume the RF input signal and interference level are C-I > -9 dB or C-I < -9 dB and observe the analog outputs of the two types. The possible I/Q-mismatch due to IAS can be observed by comparing the amplitude and phase of the analog outputs.

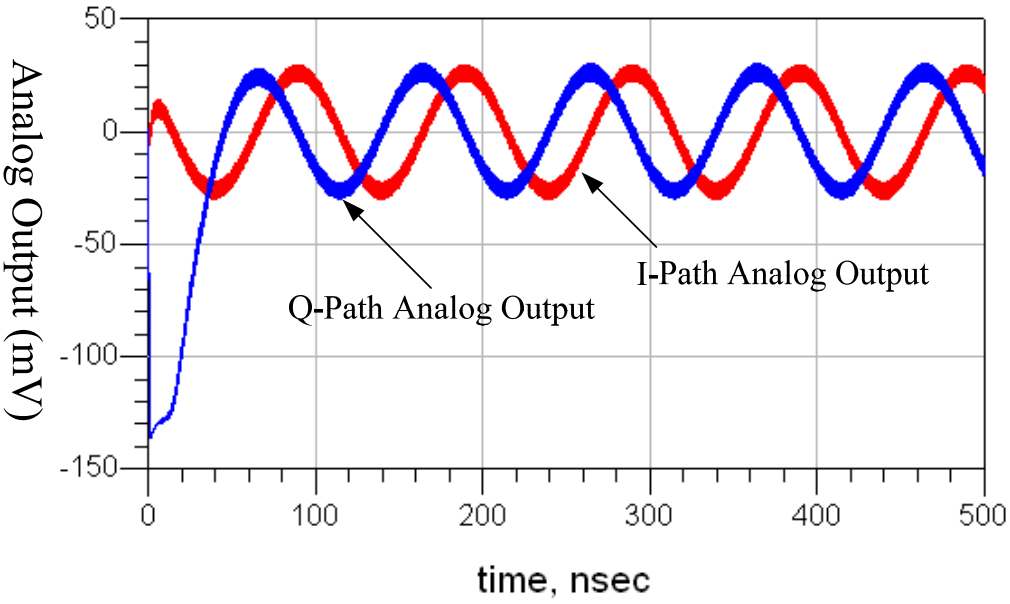


Figure 3.17 Simulation results at C-I < -9 dB

From Figure 3.17, for C-I < -9 dB, the analog outputs exhibit the same amplitude and quadrature phase; the situation is the same for C-I > -9 dB. Hence, there is no I/Q mismatch due to I and Q path IAS if they are matched.

3.4 Voltage Offset Analysis

Amp_S and Amp_I in the IAS have voltage offset (V_{OS}) issue due to the process variation which might cause that the signal from mixer cannot be amplified when the V_{OS} is great than the signal. In Figure 3.17, Mote Carlo simulation is performed to estimate the V_{OS} and to observe whether this V_{OS} affects the IAS seriously.

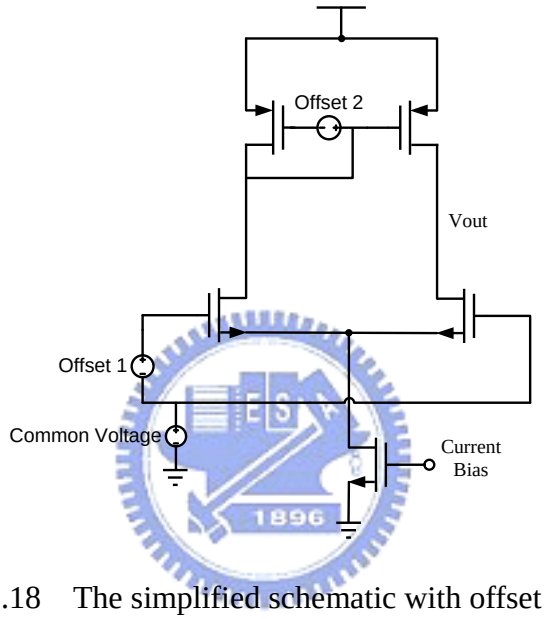


Figure 3.18 The simplified schematic with offset voltage

$$s(\Delta V_t) = \frac{A_{V_t}}{L \cdot \sqrt{\frac{W}{L}}} \tag{3.8}$$

$$s(\Delta W) = \frac{W \cdot A_b}{L \cdot \sqrt{\frac{W}{L}}} \tag{3.9}$$

A_{Vt} and A_β are the mismatch parameters for process variation and A_{Vt} = 2.2 mV and A_β = 0.4 for 0.18 um CMOS technology. The V_{OS} of the Amp_S is equal to 2.1 mV and V_{OS} of the Amp_I is equal to 2.3 mV in the range of three times sigma estimation. The sensitivity of the 64-QAM 3/4 modulation signal is equal to -67.5 dBm and the power gain of the RF receiver front-end is equal to ~25 dB. We can

know that the lowest amplitude of the mixer's output is about 2.37 mV. According to above results, the sensitivity of the IAS is affected slightly by voltage offset for the sensitivity of the 64-QAM 3/4 modulation signal.

3.5 Power Efficiency Analysis

The power efficiency of the designed IAS is analyzed here to verify whether the architecture is suitable for channel interference condition.

According to the power consumption of the circuits:

P_H = 28.1 mW

P_L = 13.7 mW

P_{IAS} = 0.828 mW

P_R = 20 mW (reference design power consumption)

x = the probability of higher interference condition (C-I < S)

$$28.1 \cdot x + 13.7 \cdot (1 - x) + 0.828 \leq 20 \tag{3.10}$$

$$x \leq 1 - \frac{20 - (13.7 + 0.828)}{28.1 - 13.7} = 0.62 \tag{3.11}$$

When the probability of higher interference condition is less than 0.62, the IAS architecture is suggested to be adopted

Chapter 4

Implementation and Measurement

In this chapter, these circuits including RF receiver front-end and IAS are implemented with UMC 0.18μm technology and these measurement results are shown.

4.1 RF Receiver Front-End

4.1.1 Layout Consideration

RF circuit is very sensitive to the parasitic effects. The signal path shall be carefully arranged with following considerations.

1. The parasitic resistance should be avoided. The narrow path generates more parasitic resistance, and thus they may seriously degrade the noise performance.
2. The distance between two paths or components should be larger to avoid mutual inductance or parasitic capacitance.
3. To avoid the coupling noise from noisy substrate, the top metal layer is used for signal path.

No matter the chip or PCB layout, the above three points must be taken into consideration.

A. Chip Layout

The layout of RF receiver front-end is shown in Figure 4.1 and the photograph of the chip with bonding wires is shown in Figure 4.2.

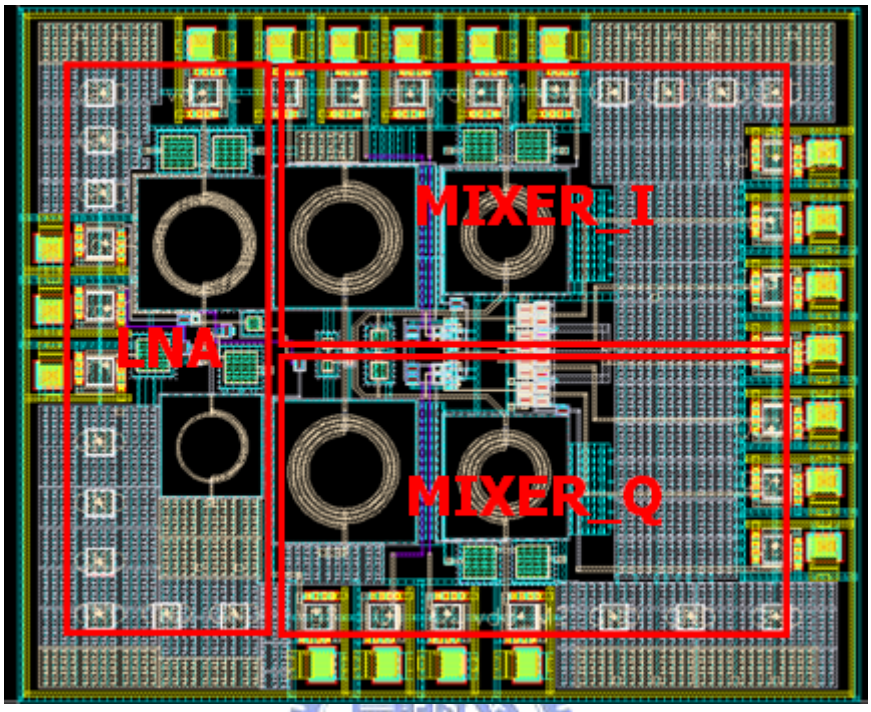


Figure 4.1 The layout view of RF receiver front-end

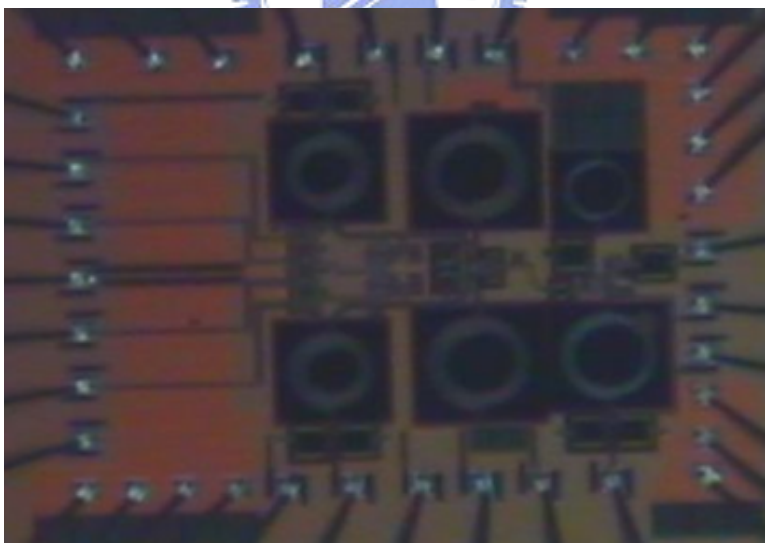


Figure 4.2 The photograph of RF receiver front-end

B. PCB Layout

In designing PCB layout, the characteristic impedance on RF signal path is considered.

Figure 4.3 The layer stack on PCB

$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{w+t}\right) \tag{4.1}$$

Z_0: characteristic impedance

w: the width of RF signal line

t : the thickness of RF signal line

h : the thickness of the medium under RF signal line

ϵ_r: the relative permittivity of the medium

From Figure 4.3 and Eq. (4.1), we can derive the proper width of RF signal path to get the Z_0 = 50 ohm is determined and the designed PCB board is shown below.

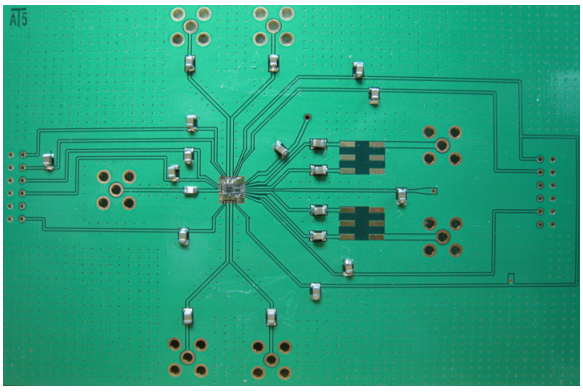


Figure 4.4 The PCB layout of RF receiver front-end

4.1.2 Measurement

The measurement setting is shown in Figure 4.5. The measured results for DC analysis, S-parameter, Power gain, IIP3, and NF are discussed.

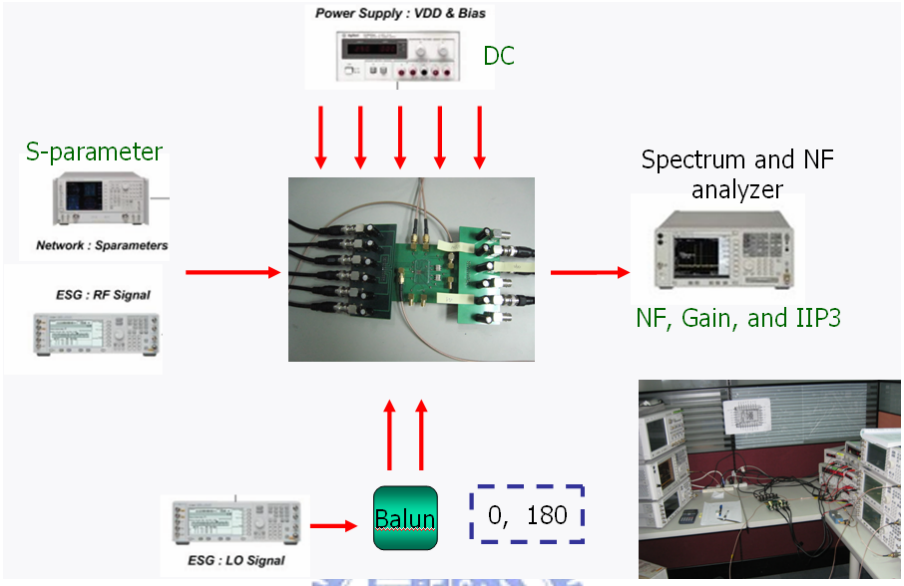
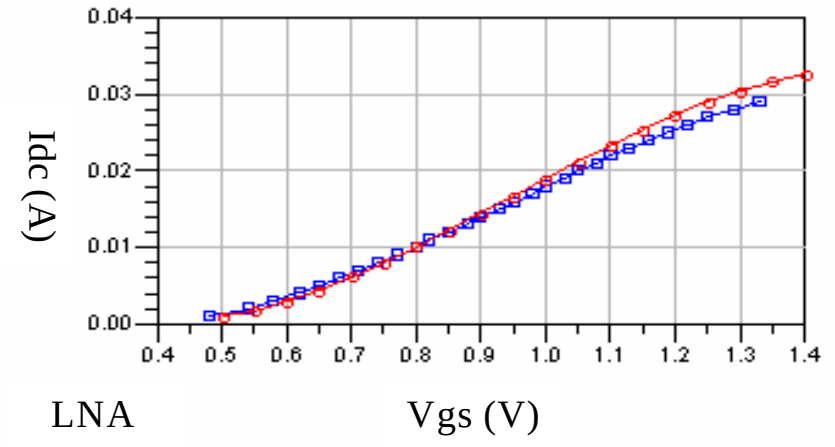


Figure 4.5 Measurement setting

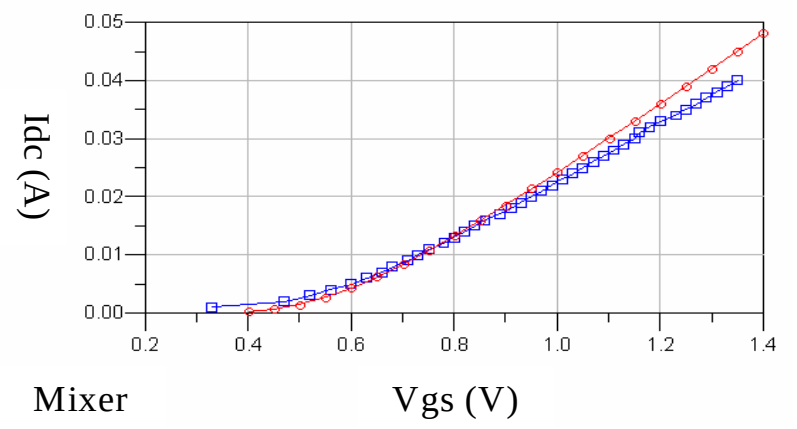
A. DC

Post-sim : square

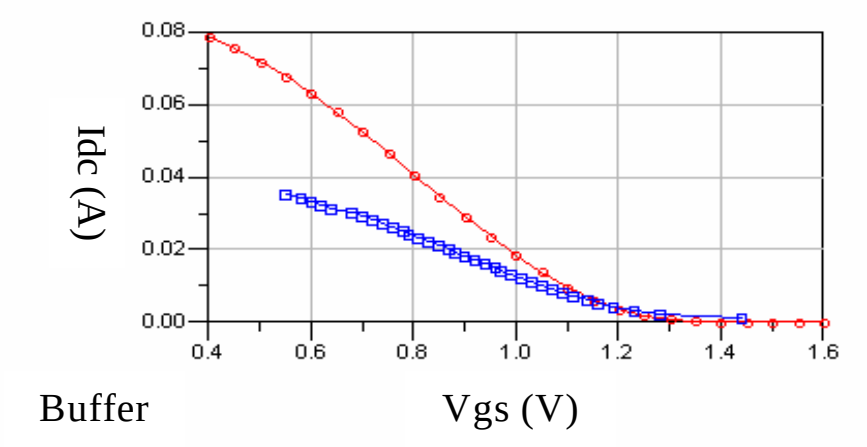
Measurement : circle



(a)



(b)

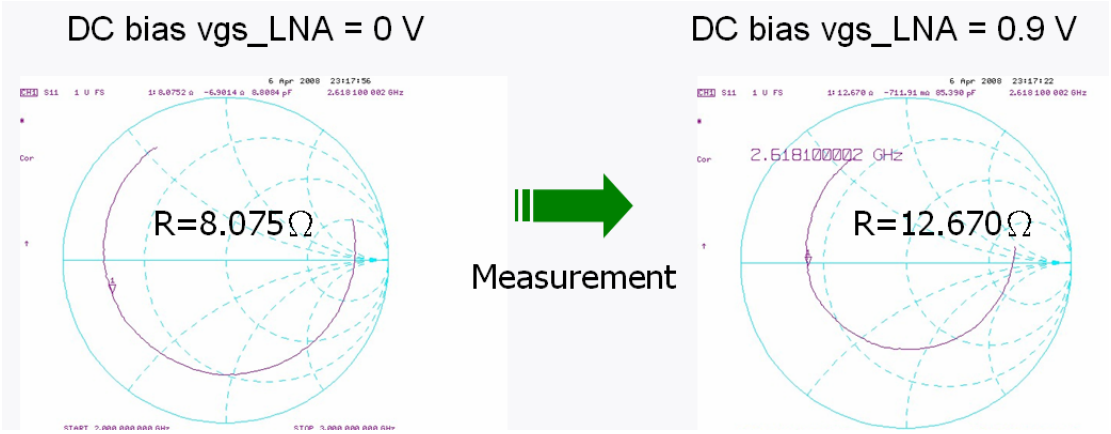


(c)

Figure 4.6 Gate bias sweep of (a) LNA (b) Mixer (c) Output buffer

From the Figure 4.6, the measured dc currents of LNA and mixer are closed to post-simulation but the measured dc currents of output buffer is less then post-simulation due to process variation.

B. S-parameter



(a)

(b)

Figure 4.7 S11 (a) Measurement (b) Post-simulation (range: 2 GHz ~ 3GHz)

In the Figure 4.7, the measured S11's Smith chart has different real part value compared to post-simulation.

$$Zin = \frac{gm}{Cgs} \times Ls + (jw(Lg + Ls) + \frac{1}{jwCgs}) \tag{4.2}$$

The real part of the S11 is composed of gm, Cgs, and Ls shown in Eq. 4.2. The measured S11 can be fitted by post-simulation results with Smith chart to fine the cause of the input matching variation.

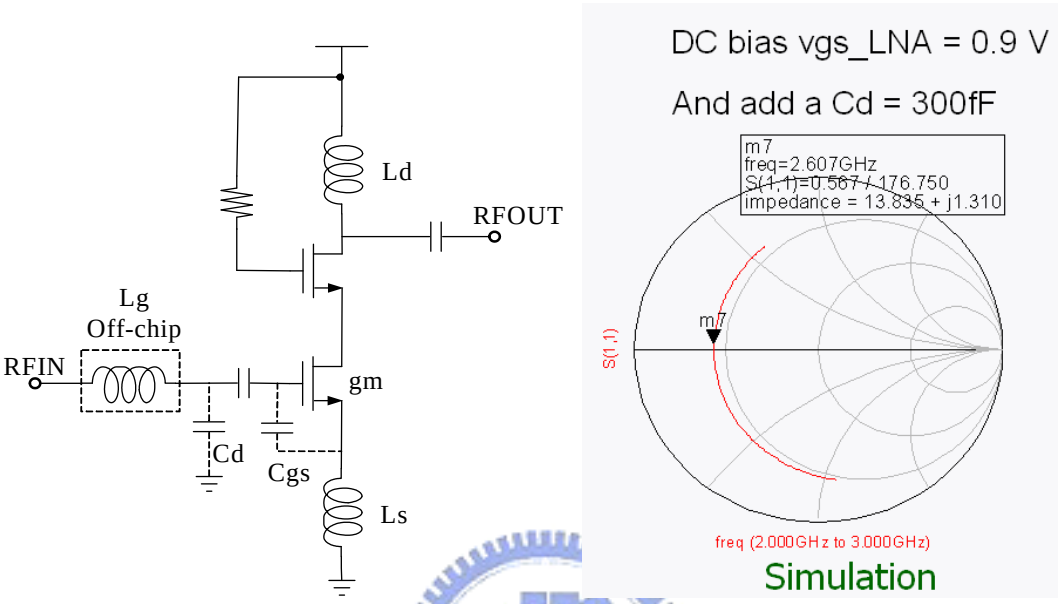


Figure 4.8 Simplified LNA schematic and fitted S11's Smith chart

The measured Smith chart with LNA gate bias equal to 0.9V can be fitted in post-simulation with an additional capacitor Cd = 300fF as can be seen in Figure 4.8. The Cd is results form parasitic capacitance of ESD pad and PCB.

C. Power Gain

Measurement setting:

1. Sweep Frequency : 2.4 GHz ~ 2.7 GHz
2. DC condition : Idc_LNA = 6mA ; Idc_Mixer = 4mA ; Idc_Buffer = 18 mA
3. LO power = 3.48 dBm (fixed IF = 10 MHz)
4. RF power = -50 dBm

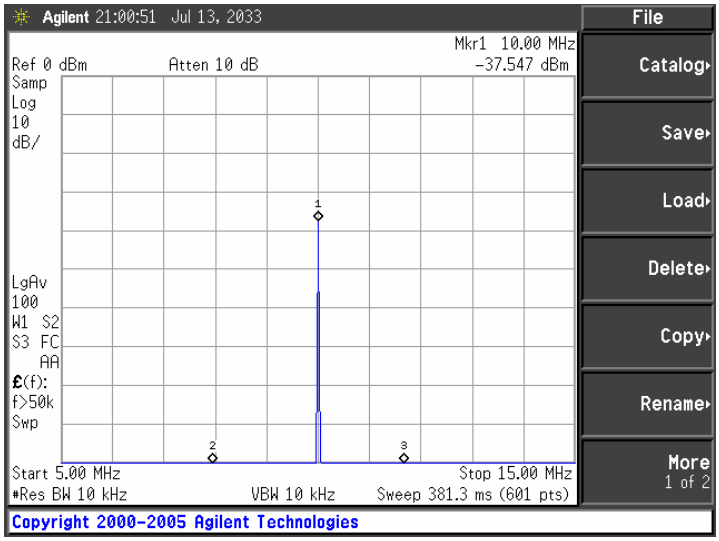


Figure 4.9 Spectrum analyzer with BW resolution 10kHz and average time 100

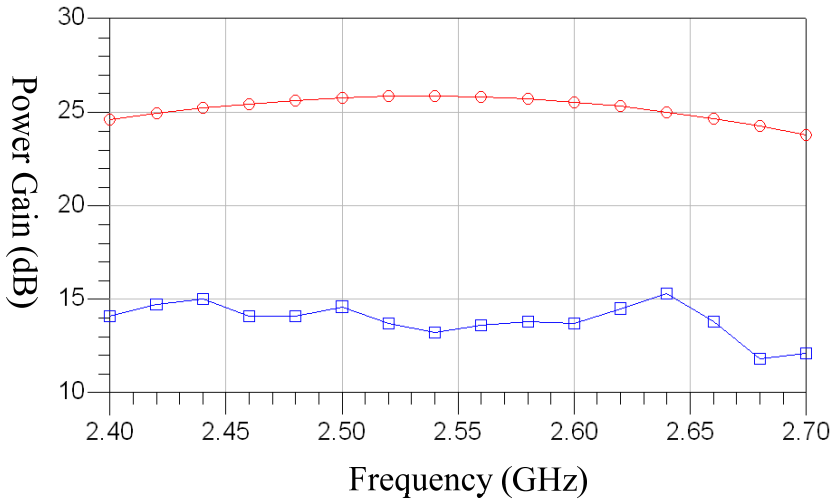


Figure 4.10 Power gain with different frequency

Post-sim : square

Measurement : circle

In Figure 4.10, the gain reduction is observed compared to post-simulation. According to above measurement results, the gain degradation is mainly affected by the variation of input matching and output buffer's DC current.

D. IIP3

Measurement setting:

1. Sweep bias of the input gm stage in mixer: vgs_Mixer = 0.6 ~ 1.1 V, step 0.05 V
2. RFin = -41.5 dBm at 2.6 GHz
3. RFin_delta = -41.5 dBm at 2.61 GHz
4. LOin = 4.74 dBm at 2.55 GHz
5. IF out : 50 MHz and 60 MHz
6. AIM3 : 40 MHz and 70 MHz

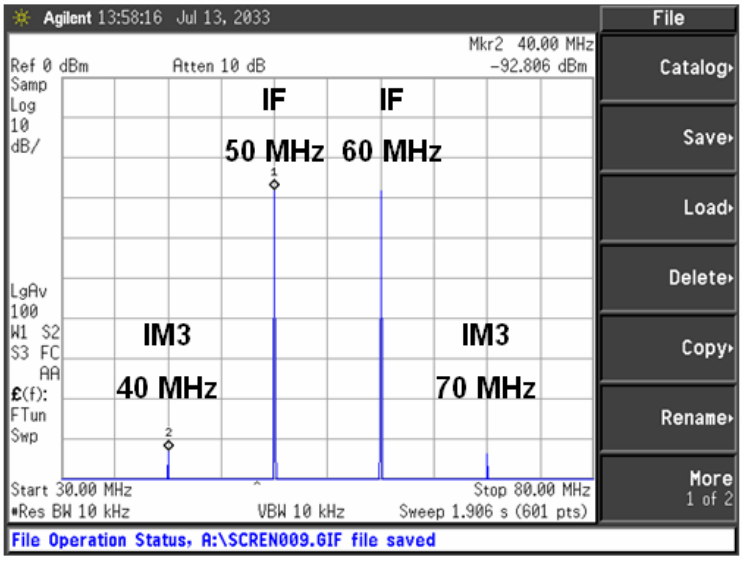


Figure 4.11 Spectrum analyzer for two-tone test

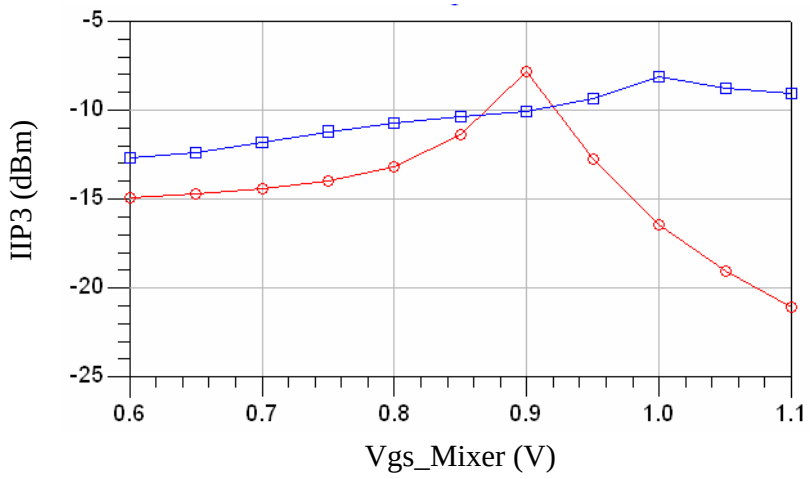
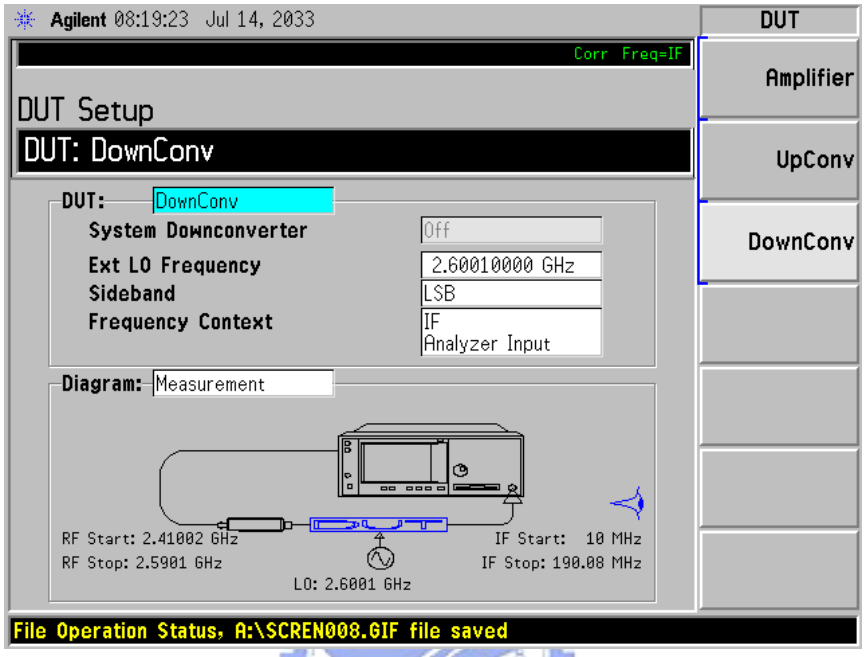


Figure 4.12 IIP3 performance with different vgs of input gm stage

From Figure 4.11, the IIP3 increases with raising Mixer gate bias voltage (Vgs_Mixer) and this trend meet the discussion in chapter 3.1.

E. NF

Measurement setting:



(a)

Frequency	Noise Figure
10.00000 MHz	15.7647 dB
19.47789 MHz	14.6054 dB
28.95579 MHz	14.3133 dB
38.43368 MHz	14.5296 dB
47.91158 MHz	14.8202 dB
57.38947 MHz	14.9105 dB
66.86737 MHz	14.8567 dB
76.34526 MHz	14.7494 dB
85.82316 MHz	14.7579 dB
95.30105 MHz	14.7955 dB
104.77895 MHz	14.7365 dB
114.25684 MHz	14.3200 dB
123.73474 MHz	13.7796 dB

(b)

Figure 4.13 (a) NF analyzer (b) Measured result (LSB) with different IF

Because of the gain degradation, the measured NF performance is also higher than post-simulation result. (about 5.6 dB with LSB mode)

4.1.3 Summary

Table 4.1 Comparison table

parameters	[14]	[15]	[16]	post-high	post-low	meas-high	meas-low
technology CMOS [um]	0.18	0.18	0.13	0.18	0.18	0.18	0.18
conversion gain [dB]	21.4	30	24.2	25.24	25.7	13.8	13.3
NF [dB]	13.9	7.3	4.2	2.6	2.56	11.3	11.8
IIP3 [dBm]	-18	-8	-2	-7.77	-15.5	-9.8	-12.9
power [mW]	6.5	6.3	12	28.1	13.7	32.4	19.8
architecture	Low-IF	DCR	DCR	DCR	DCR	DCR	DCR
frequency [GHz]	2.4	2.4	4.15	2.6	2.6	2.6	2.6
FOM	11.55	37.6	39.29	33.92	29.79	1.044	-0.717

*DCR : direct conversion

A figure of merit (FOM) which normalizes dynamic range to power dissipation is employed to compare the performance of the front-end circuits.

$$FOM_{dB} = 10\log\left(\frac{IIP_3(mW)\times Gain}{(NF-1)\times power}\right) \tag{4.3}$$

Table 4.1 summarizes the measurement and post-simulation results. Because of the gain degradation, the FOM is obviously different value between post-simulation and measurement.

4.2 Interference Aware Scheme

In this chapter, these circuits of the IAS are implemented with UMC CMOS 0.18um technology. Measurement results are also shown here.

4.2.1 Layout Consideration

The circuits of the IAS deal with the analog signal (frequency is lower than 100 MHz), so the characteristic impedance is less important than RF signal line. For analog signal, the device layout symmetry is the main consideration.

A. Chip Layout

In Fig 4.14, the layout of two IASs for I and Q path include the LPFs are illustrated.

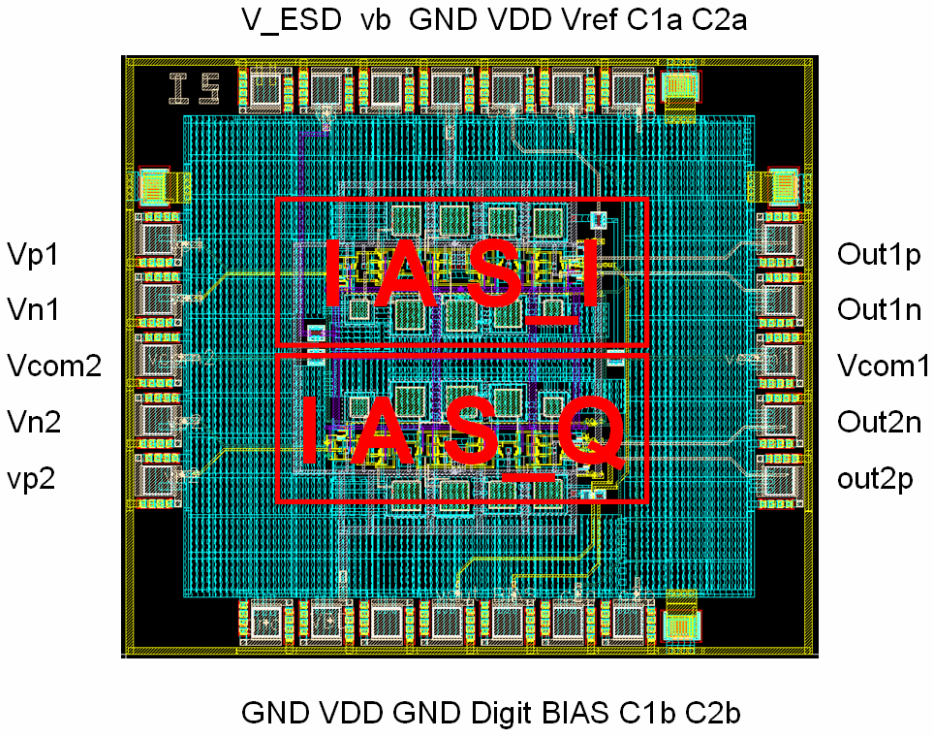


Figure 4.14 Layout view of the IAS with two paths (I and Q)

1. Vp and Vn: the input of LPF
2. Outp and Outn : the output of LPF
3. C1 (a/b) and C2 (a/b) : the two paths' output of peak detectors
4. Digit : digital output
5. Vcom : the reference voltage of CMFB

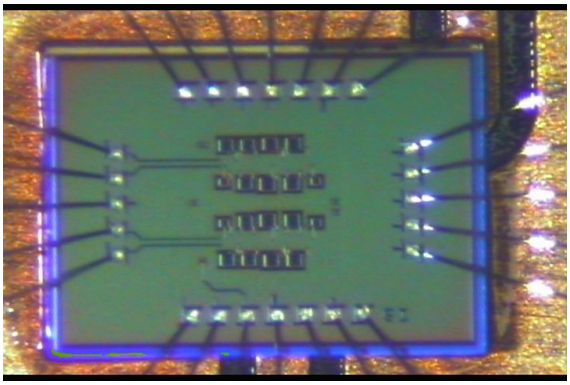


Figure 4.15 The photograph of the IAS

B. PCB Layout

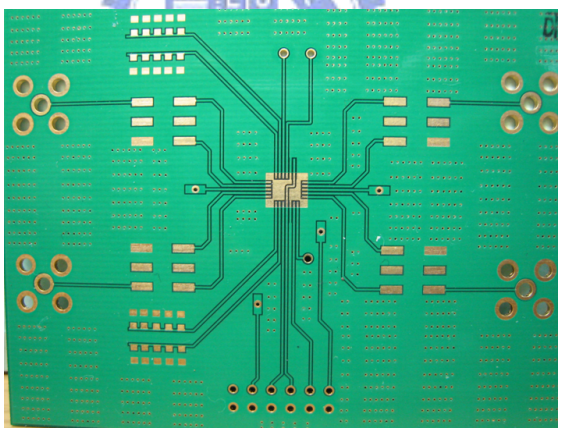


Figure 4.16 The PCB layout of IAS with two paths

4.2.2 Measurement

In Figure 4.17, the IAS measurement setting uses ESG to generate the carrier signal and interference. The instrument setup is employed to the output DC voltages of peak detector, LPFs, and digital.

Figure 4.17 The IAS measurement setting

A. DC

The dc voltage is measured with no input signal stimulating.

1. Post-simulation Idc_IAS (I-Q path) = 5.267 mA (include two LPFs)

   Measurement Idc_IAS (I-Q path) ~ 8 mA

2. The output dc voltages of peak detectors:

   Post-simulation:

   V_{C1} and V_{C2} = 0.385 mV

   Measurement:

   V_{C1} ~ 0.35 mV ; V_{C2} ~ 0.85 mV

3. The output DC voltages of LPF:

   Post-simulation:

   $V_{outp} = V_{outn}$ = 0.9 V

   Measurement:

   V_{outp} ~ 1.12 V ; V_{outn} ~ 1.43V

5. Vcom could be changed to adjust the peak voltage (V_S and V_I) in circuit design but it doesn't work in this implementation.

According to above measured results, the IAS suffers from mismatch due to process variation.

B. Two-Tone Test

Two ESG instruments are used to generate the carrier signal and interference signal.

Measurement setting:

1. Sweep the interference power : -30 dBm to 15 dBm (fixed frequency 20MHz)
2. fixed carrier signal power : -30 dBm (fixed frequency 5 MHz)

Post-simulation: when interference power > -21 dBm, the digital out is equal to VDD.

Measurement: the digital out is always equal to VDD in the sweep range.

The implemented IAS doesn't work correctly because of the variation of DC bias points.

Chapter 5
Conclusions

5.1 Summary

An interference aware scheme composed of four building blocks including signal distinction, envelope detection, error correction and mode selection is proposed and designed.

A CMOS RF receiver front-end with dual linearity modes including LNA and mixer for WiMAX standard is implemented in a 0.18um CMOS tech. At high linearity mode it has IIP3 of -9.8 dBm and consumes 32.4mW; at low linearity mode it has IIP3 of -12.9 dBm and consumes 19.8 mW. The power gain is about 14 dB and NF is about 11 dB for dual modes.

By combining with the proposed interference aware scheme and dual-mode RF receiver front-end, the operation mode of the receiver front-end can be automatically selected according to the interference condition by the low-power IAS and 5.5dB improvement of system interference tolerance is achieved from co-simulation results.

5.2 Future Works

5.2.1 Fully Integrated Chip

In this thesis, the IAS and RF front-end are implemented separately. But fully integration of RF receiver front-end and IAS has the cost benefit for realistic implementation. The DC offset must be taken into consideration for combining these two blocks because it can corrupt the signal and, more importantly, saturate the following stages, such as IAS and LPF. DC offset cancellation (DCOC) technique [17]

can be employed to compensate the DC offset due to direct conversion architecture.

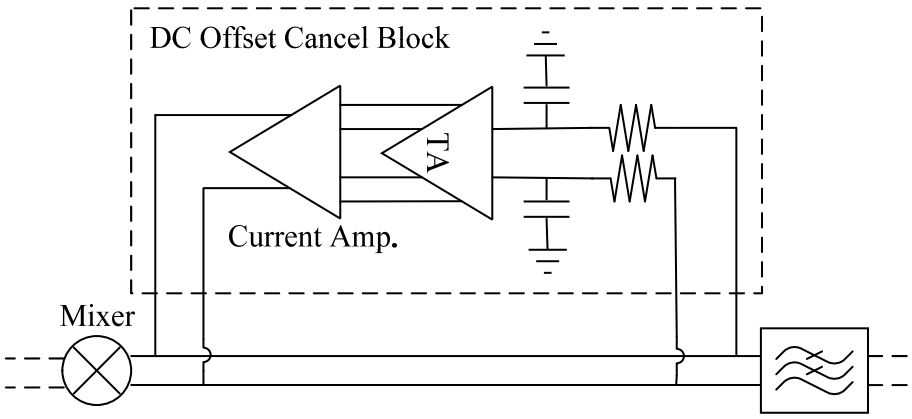


Figure 5.1 DC offset cancel block

In Figure 5.1, the DC offset cancel block consists of passive LPF, a transconductance amplifier, and a current amplifier.

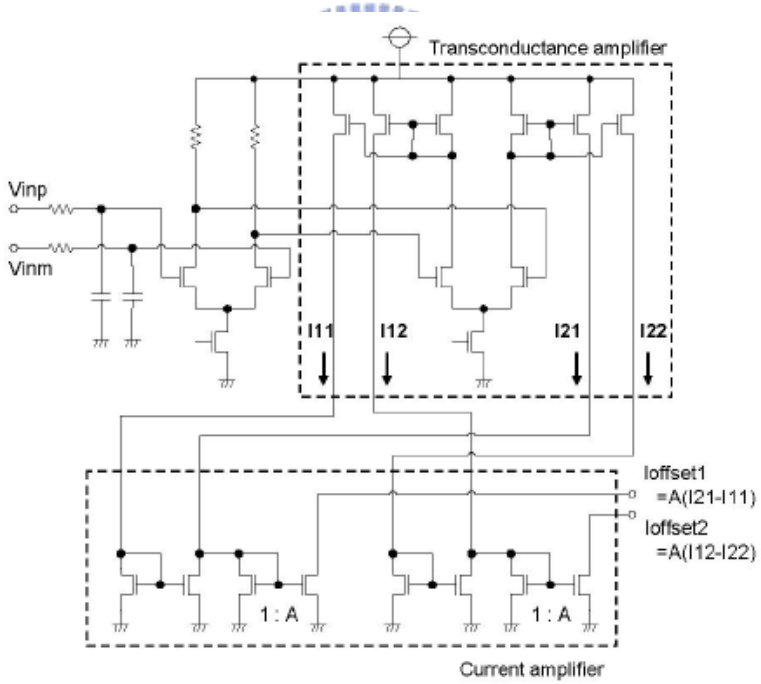


Figure 5.2. DC offset cancel circuit (DCOC)

The operation of this DCOC circuit in Figure 5.2 is as follows. First, DC offset voltage detected by passive LPF is amplified and is converted to the differential currents (I11, I12, I21, and I22) by the transconductance amplifier. Then, these differential currents flow into the single-ended differential current amplifiers where

the differential components are amplified and the common currents are subtracted with perfect matching of the input pairs. Therefore, only DC offset component is extracted and is used for DC offset correction.

5.2.2 Dynamic Range of the IAS

The sensitivity of the designed IAS in this thesis focus on carrier signal that is equal to -67.5 dBm witch is the sensitivity of 64QAM-3/4 modulation in WiMAX system. For the lowest order modulation such as BPSK-1/2, the designed IAS cannot detect the sensitivity level (-96.7 dBm) of the BPSK-1/2 due to the two amplifiers (Amp_S and Amp_I) in signal distinction. For the lowest sensitivity level (BPSK-1/2), these two amplifiers need higher gain to make IAS work correctly. On the contrary, for the highest sensitivity level (64QAM-3/4), lower gain amplifiers are need. Here, we propose a modify IAS to overcome this issue.

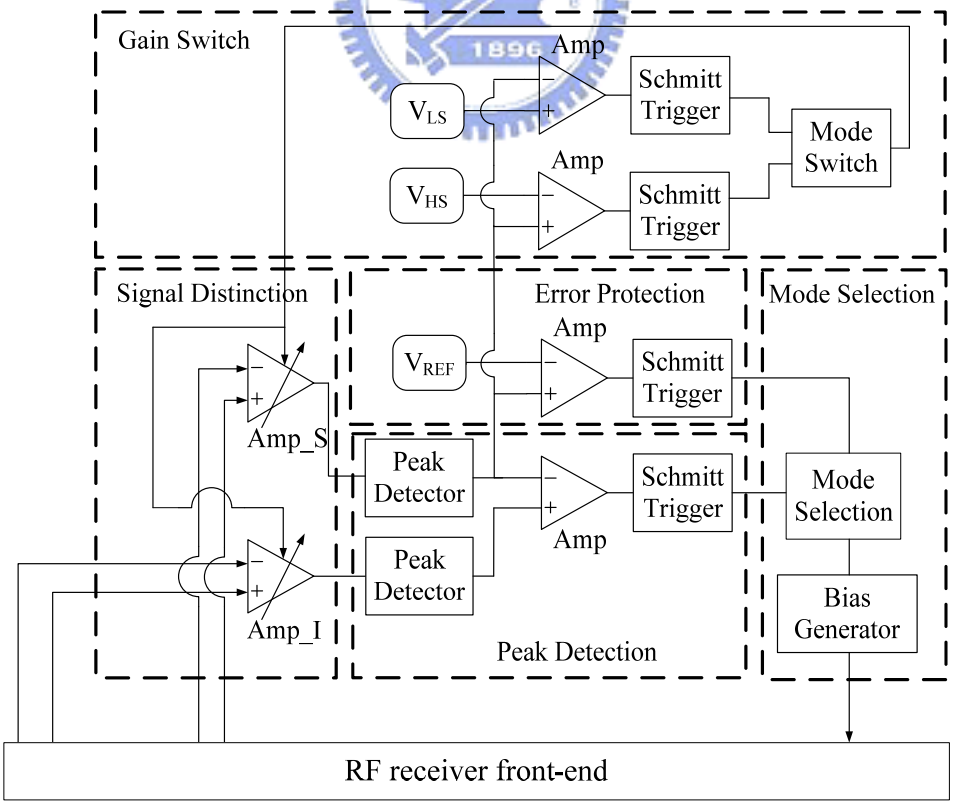


Figure 5.3 Modified IAS

In Figure 5.3, the modified IAS has a block called “Gain Switch”. When carrier signal isn’t detected by IAS, the gain switch can change the gain of Amp_S and Amp_I to high gain mode. On the contrary, when carrier signal is higher enough, the gain switch can change the gain of Amp_S and Amp_I to low gain mode. Using the gain switch can increase the dynamic range of the IAS.

$V_{S\_maximum}$ (Amp_S is at saturation) > V_{REF} > V_{switch}

(These values are closed to each others.)

V_L > $V_{S\_minimum}$ (No input signal)

(V_L is slightly more than $V_{S\_minimum}$)

1. Highest sensitivity mode è Lowest sensitivity mode

At initial condition, the IAS is in low gain mode. When carrier path peak level is less than V_L, the IAS can be changed to high gain mode by gain switch and detects the lowest sensitivity signal.

2. Lowest sensitivity mode è Highest sensitivity mode

At initial condition, the IAS is in high gain mode. When carrier path peak level is more than V_{switch}, the IAS can be changed to low gain mode.

For advanced discussion, the lower sensitivity of some type modulation signal such as BPSK-1/2 (-96.7 dBm), the V_{OS} of the modified IAS should lower than 89 uV at the lowest sensitivity mode.

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Vita

姓名 ： 林佳欣

性別 ： 男

出生地 ： 宜蘭縣

生日 ： 民國七十二年十月二十五日

地址 ：263 宜蘭縣壯圍鄉過嶺村一巷十一弄十二號

學歷 ： 國立交通大學電子工程研究所碩士班 2006/09~2008/06

國立中正大學電機工程學系 2002/09~2006/06

國立宜蘭高級中學 1999/09~2002/06

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