

薄膜電晶體的溫度係數模型以及玻璃基板上具溫度補償功能之參考電壓電路設計

**Temperature Coefficient Model of Poly-Silicon TFT and its Application on Voltage Reference Circuit with Temperature Compensation in LTPS Process**

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# 薄膜電晶體的溫度係數模型以及玻璃基板上具溫度補償功能之參考電壓電路設計

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## ABSTRACT (CHINESE)

低溫複晶矽 (low temperature poly-silicon, LTPS) 薄膜電晶體 (thin-film transistors, TFT) 已被視為一種材料廣泛地應用於可攜帶式系統產品中，例如數位相機、行動電話、個人數位助理 (PDA)、筆記型電腦等等，這是由於低溫複晶矽薄膜電晶體的電子遷移率 (electron mobility) 約是傳統非晶矽 (amorphous silicon) 薄膜電晶體的百倍大。此外，低溫複晶矽技術可藉由將驅動電路整合於顯示器之週邊區域來達到輕薄、巧小且高解析度的顯示器。這樣的技術也將越來越適合於系統整合型面板 (system-on-panel/system-on-glass) 應用之實現。本論文首先針對了低溫多晶矽電晶體製程下玻璃基板上的薄膜電晶體作了分別對改變其偏壓電流、雷射能量以及通道寬度等相關的溫度量測，並提出了薄膜電晶體的溫度係數模型，使用此模型為基礎，設計出一在玻璃基板上具溫度補償功能之參考電壓電路設計，並使用三微米的低溫多晶矽薄膜電晶體製程來做驗證。此新提出的具溫度補償之參考電壓電路的實驗結果，證實在操作電壓為十伏時其溫度係數為一百九十五 ppm/°C。此新提出的具溫度補償功能之參考電壓電路可以應用於面板系統上，提供類比電路設計之精準電壓基礎。

# **Temperature Coefficient Model of Poly-Silicon TFT and its Application on Voltage Reference Circuit with Temperature Compensation in LTPS Process**

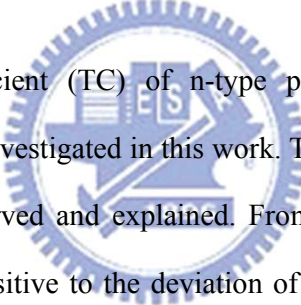
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## **ABSTRACT (ENGLISH)**



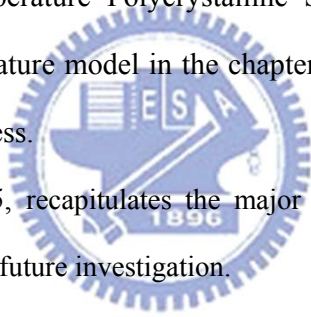
The temperature coefficient (TC) of n-type polycrystalline silicon thin-film transistors (poly-Si TFTs) is investigated in this work. The relationship between TC and the activation energy is observed and explained. From the experimental results, it is also found that TC is not sensitive to the deviation of the laser crystallization energy. On the contrary, channel width can effectively modulate the TC of TFTs. Furthermore, the temperature coefficient model has been advanced in the thesis. By using the diode-connected poly-Si TFTs with different channel widths, the first voltage reference circuit with temperature compensation for precise analog circuit design on glass substrate is proposed and realized. From the experimental results in a LTPS process, the output voltage of voltage reference circuit with temperature compensation exhibits a very low TC of 195 ppm/°C, between 25°C and 125°C. The proposed voltage reference circuit with temperature compensation can be applied to design precise analog circuits for System-on-Panel (SoP) or System-on-Glass (SoG) applications, which enables the analog circuits to be integrated in the active matrix LCD (AMLCD) panels.

The first chapter, chapter 1, includes the motivation and the thesis organization of this thesis. The chapter 2 of this thesis introduces some background knowledge of thin-film transistor liquid crystal displays, the liquid crystal display structure in TFT-LCD panel, System on Panel (SOP), System on Glass (SOG), and the bandgap reference circuit (BGR).

In the chapter 3, this thesis introduces the temperature coefficient of different kind of devices, the P-I-N diodes, P-type diode-connected TFTs and N-type diode connected TFTs, on glass substrate. From the measurement results of above, we present the temperature model of N-type diode-connected TFTs.

In the chapter 4, a new voltage reference circuit with temperature compensation designed with the Low-temperature Polycrystalline Silicon (LTPS) TFTs on glass substrate by using the temperature model in the chapter 3 is proposed, which has been verified in a 3- $\mu\text{m}$  LTPS process.

The last chapter, chapter 5, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.



## ACKNOWLEDGEMENTS

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#### 有心栽花花不開，無心插柳有成蔭

碩士生涯真的如一轉眼就過去了，從一進實驗室沒半個人認識和世範兩個人相依為命，到現在和一大群人幾乎是形影不離的生活，還真的很如夢如幻，恍如隔世的感覺。在這兩年的求學過程當中，首先感謝柯明道教授不辭辛苦的三更半夜寄信針對學生論文指正，以及凡事針對細節滔滔不絕的對學生犯的錯誤鉅細靡遺的辛勤指教，都令學生印象深刻，感佩老師認真負責的教誨。

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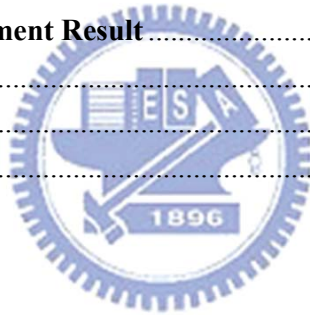
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# Chapter 1

## Introduction

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### 1.1 MOTIVATION

Polycrystalline silicon thin-film transistors (Poly-Si TFTs) have been widely investigated for active-matrix liquid-crystal displays (AMLCDs) and their peripheral driving circuitry due to the increased carrier mobility [1], [2]. The CPU, memory, timing controller, digital-to-analog converter (DAC), and driving buffer had been implemented on glass substrate with the low-temperature polycrystalline silicon (LTPS) TFT process. LTPS AMLCDs integrated with driver and control circuits on glass substrate have been practically applied in portable systems, such as mobile phone, digital camera, and notebook, etc. [3], [4] However, even with the advanced crystallization technologies such as the excimer laser annealing (ELA) or the sequential laser solidification (SLS) process, it is still observed that the carrier transport in poly-Si TFTs is dominated by the thermionic emission effect [5], [6]. The energy barriers at grain boundaries confine the carrier movement, reduce the field-effect mobility, and make the device characteristics to be strongly dependent on temperature. As a result, to reduce the impact of temperature variation on the performance of analog circuits in the low-temperature polycrystalline silicon (LTPS) process is a very important design challenge.

In CMOS technology, the voltage reference circuit with temperature compensation is the major design to provide a stable voltage reference with low sensitivity to temperature and supply voltage. The bandgap reference circuit is one of

the most famous and widespread voltage reference circuits with temperature compensation [7]-[10]. The key idea is to use the temperature-dependent voltage drop across the diode-connected bipolar junction transistors (BJTs) or across the diodes to modulate and stabilize the output voltage. The BGR circuit has been widely used in analog and digital circuits, such as dynamic random access memory (DRAM), flash memory, analog-to-digital converter (ADC), operational amplifier (OPAMP), buffer and so on. As the entire TFT-LCD panel circuits which is shown in Fig. 1-1, we know that the ADC and buffer are the indispensable part in the data driver circuit shown in Fig. 1-2. Therefore, the BGR circuit is critical point in the development for the System-on-Panel (SoP) or System-on-Glass (SoG) applications.

Though the BGR circuit is important to provide a stable output voltage, the LTPS BGR circuit on glass substrate was never reported in the past. The conventional CMOS BGR circuit incorporated with BJTs or p-n junction diodes is a great challenge for LTPS process since the characteristics of the poly-Si BJTs or the poly-Si p-n junction diodes are still unknown or lack of reliable control. On the contrary, the characteristics of LTPS TFTs are strongly dependent on temperature even when the devices are operated in saturation region [3,4]. Therefore, the LTPS BGR circuit can be realized by using only LTPS TFT devices.

## **1.2 THESIS ORGANIZATION**

The first chapter, chapter 1, includes the motivation and the thesis organization of this thesis.

The chapter 2 of this thesis introduces some background knowledge of thin-film transistor liquid crystal displays, the liquid crystal display structure in TFT-LCD panel, System on Panel (SOP), System on Glass (SOG), and the bandgap reference circuit (BGR).

In the chapter 3, this thesis introduces the temperature coefficient of different kind of devices, the P-I-N diodes, P-type diode-connected TFTs and N-type diode connected TFTs, on glass substrate. From the measurement results of above, we present the temperature model of N-type diode-connected TFTs.

In the chapter 4, a new voltage reference circuit with temperature compensation designed with the Low-temperature Polycrystalline Silicon (LTPS) TFTs on glass substrate by using the temperature model in the chapter 3 is proposed, which has been verified in a 3- $\mu\text{m}$  LTPS process.

The last chapter, chapter 5, recapitulates the major consideration of this thesis and concludes with suggestions for future investigation.



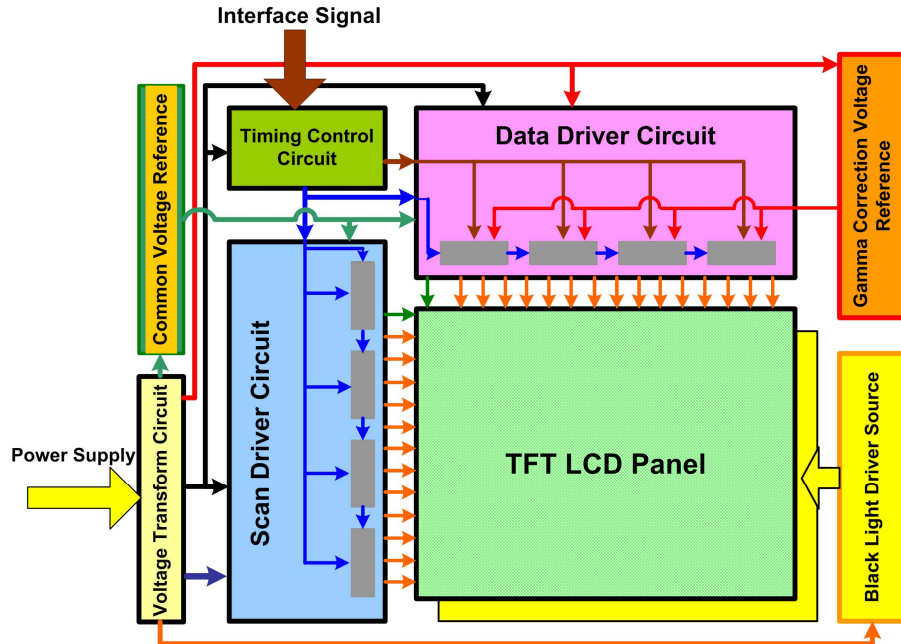


Fig. 1.1 The block diagram of the entire TFT-LCD panel circuits.

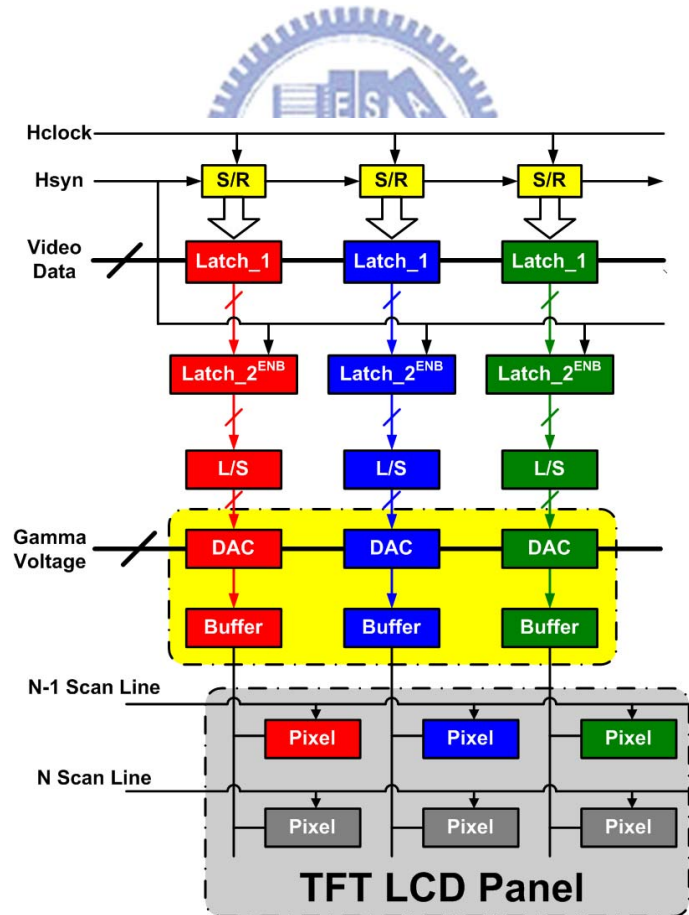


Fig. 1.2 The basic diagram of data driver circuit.

## Chapter 2

# Background of Thin-Film Transistor Liquid Crystal Displays and Bandgap Reference Circuit

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### 2.1 OVERVIEW OF LIQUID-CRYSTAL DISPLAY

The liquid-crystal display (LCD) is a thin, flat display device made up of any number of color or monochrome pixels arrayed in front of a light source or reflector. It is often utilized in battery-powered electronic devices because it uses very small amounts of electric power.

Each pixel of an LCD which is shown as Fig.2.1 typically consists of a layer of molecules aligned between two transparent electrodes, and two polarizing filters, the axes of transmission of which are (in most of the cases) perpendicular to each other. With no liquid crystal between the polarizing filters, light passing through the first filter would be blocked by the second (crossed) polarizer. The surfaces of the electrodes that are in contact with the liquid crystal material are treated so as to align the liquid crystal molecules in a particular direction. This treatment typically consists of a thin polymer layer that is unidirectional rubbed using, for example, a cloth. The direction of the liquid crystal alignment is then defined by the direction of rubbing. Electrodes are made of a transparent conductor called Indium Tin Oxide (ITO).

Before applying an electric field, the orientation of the liquid crystal molecules is determined by the alignment at the surfaces. In a twisted nematic device (still the

most common liquid crystal device), the surface alignment directions at the two electrodes are perpendicular to each other, and so the molecules arrange themselves in a helical structure, or twist. Because the liquid crystal material is birefringent, light passing through one polarizing filter is rotated by the liquid crystal helix as it passes through the liquid crystal layer, allowing it to pass through the second polarized filter. Half of the incident light is absorbed by the first polarizing filter, but otherwise the entire assembly is reasonably transparent.

When a voltage is applied across the electrodes, a torque acts to align the liquid crystal molecules parallel to the electric field, distorting the helical structure (this is resisted by elastic forces since the molecules are constrained at the surfaces). This reduces the rotation of the polarization of the incident light, and the device appears gray. If the applied voltage is large enough, the liquid crystal molecules in the center of the layer are almost completely untwisted and the polarization of the incident light is not rotated as it passes through the liquid crystal layer. This light will then be mainly polarized perpendicular to the second filter, and thus be blocked and the pixel will appear black. By controlling the voltage applied across the liquid crystal layer in each pixel, light can be allowed to pass through in varying amounts thus constituting different levels of gray.

The total cross section structure of TFT-LCD panel is shown in Fig.2.2 particularly. It can be roughly divided into two parts, TFT array substrate and color filter substrate, by liquid crystal filled in the center of LCD panel. We still need a backlight module including an illuminator and a light guide since liquid crystal molecules cannot light by themselves. However, it usually consumes the most power of the system, some applications such as mobile communications try to exclude or replace it from the system. In TFT array substrate, we need a polarizer, a glass substrate, a transparent electrode and an orientation layer. In color filter substrate, we also need an

orientation layer, a transparent electrode, color filters, a glass substrate and a polarizer. Most transparent electrodes are made by ITO, and they can control the directions of liquid crystal molecules in each pixel by voltage supplied from TFT on the glass substrate. Color filters contain three original colors, red, green, and blue (RGB). As the degree of light, named “gray level”, can be well controlled in each pixel covered by color filter, we will get more than million kinds of colors.

Nowadays, there are two ways which are passive matrix drive and active matrix drive liquid crystal which are shown in Fig.2.3 to exert the electrical field. The ways to drive the passive matrix drive and the negative matrix drive are almost the same.

This type of display is called passive-matrix addressed which is shown in Fig.2.3 (a) because the pixel must retain its state between refreshes without the benefit of a steady electrical charge. As the number of pixels (and, correspondingly, columns and rows) increases, this type of display becomes less feasible. Very slow response times and poor contrast are typical of passive-matrix addressed LCDs.

High-resolution color displays such as modern LCD computer monitors and televisions use an active matrix structure shown as Fig.2.3 (b). A matrix of thin-film transistors (TFTs) is added to the polarizing and color filters. Each pixel has its own dedicated transistor, allowing each column line to access one pixel. When a row line is activated, all of the column lines are connected to a row of pixels and the correct voltage is driven onto all of the column lines. The row line is then deactivated and the next row line is activated. All of the row lines are activated in sequence during a refresh operation. Active-matrix addressed displays look "brighter" and "sharper" than passive-matrix addressed displays of the same size, and generally have quicker response times, producing much better images. Fig. 2.4 shows the largest LCD TV produced by Sharp in the world in 2008.



## 2.2 LCD INDUSTRY AND LTPS TECHNOLOGY

The LCD industry has shown rapid growth in five market areas, namely, notebook computers, monitors, mobile equipment, mobile telephones, and televisions. For high-speed communication networks, the emerging portable information tools are expected to grow in following on the rapid development of display technologies. Thus, the development of higher specification is demanded for LCD as an information display device. Moreover, the continual growth in network infrastructures will drive the demand for displays in mobile applications and flat panels for computer monitors and TVs. The specifications of these applications will require high-quality displays that are inexpensive, energy-efficient, lightweight, and thin.

Amorphous silicon (a-Si) thin-film transistors (TFTs) are widely used for flat-panel displays. However, the low field-effect mobility (ability to conduct current) of a-Si TFTs allows their application only as pixel switching devices; they cannot be used for complex circuits. In contrast, the high driving ability of polycrystalline Si (p-Si) TFTs allows the integration of various circuits such as display drivers. Eliminating LSI (large-scale integration) chips for display drivers will decrease the cost and thickness of displays for various applications. There are high-temperature and low-temperature poly-Si TFTs, defined by the maximum process temperature they can withstand. The process temperature for high-temperature poly-Si can be as high as 900°C. Hence, expensive quartz substrates are required, and the profitable substrate size is limited to around 6 in. (diagonal). Typical applications are limited to small displays. The process temperature for low-temperature poly-Si (LTPS) TFTs, on the other hand, is less than 600°C, which would allow the use of low-cost glass substrates. This makes possible direct-view large-area displays—for example, UXGA (ultra extended graphics array) monitors of up to 15.1 in. (diagonal) with a resolution of 1600 x 1200 pixels. For this reason, LTPS technology has been applied successfully to

not only small-sized displays, but also medium- and large-screen products. To take the iPhone 3G shown in Fig. 2.5 for instance, the glass substrate of the product by Apple made in the LTPS process, hence, the cost compared with the iPhone can be reduced about 100 US dollars

### ***2.2.1 System-on-Panel/System-on-glass Displays***

LTPS TFT-LCD technology has some features of system integration within a display. It can make a compact, high reliable, high resolution display. Because of this property, LTPS TFT-LCD technology is widely used for mobile displays. Fig. 2.5 shows the system integration roadmap of LTPS TFT-LCD [4], [12].

System-on-panel (SOP) displays are value-added displays with various functional circuits, including static random access memory (SRAM) in each pixel, integrated on the glass substrate [4]. Fig. 2.6 shows the basic concept of pixel memory technology. When SRAMs and a liquid crystal AC driver are integrated in a pixel area under the reflective pixel electrode, the LCD is driven by only the pixel circuit to display a still image. It means that no charging current to the data line for a still image. This result is more suitable for ultra low power operation. Eventually, it may be possible to combine the keyboard, CPU, memory, and display into a single “sheet computer”. The schematic illustration of the “sheet computer” concept and a CPU with an instruction set of 1-4 bytes and an 8b data bus on glass substrate are shown in Fig. 2.7, respectively [11], [12]. Fig. 2.8 shows the roadmap of LTPS technologies leading toward the realization of sheet computers. Finally, all of the necessary function will be integrated in LTPS TFT-LCD. Although the level of LTPS is as almost the same as the level of the crystal Si of 20 years ago, actual operation of 50MHz with 1 $\mu$ m design will be realized near future [13].

### ***2.2.2 The Advantages of the SOP/SOG LTPS TFT-LCD Displays***

The distinctive feature of the LTPS TFT-LCD is the elimination of TAB-ICs (integrated circuits formed by means of an interconnect technology known as tape-automated bonding). LTPS TFTs can be used to manufacture complementary metal oxide semiconductors (CMOSs) in the same way as in crystalline silicon metal oxide semiconductor field-effect transistors (MOSFETs). Fig. 2.5 shows the cross sectional structure of a LTPS TFT CMOS. In the LTPS process, a buffer oxide and an  $\alpha$ -Si:H film were deposited on glass substrate by plasma enhanced chemical vapor deposition (PECVD) system and then the XeCl excimer laser was used to crystallize this film [14]. The thickness of  $\alpha$ -Si film deposited in this work is about 50 nm. After active islands were defined, the ion doping process was carried out to the  $N^+$  regions, Following, double gate insulator films, SiOX and SiNX, were deposited by PECVD system. The gate metal Mo was deposited and then patterned. Subsequently, the  $N^-$  and  $P^+$  ion dopings were implanted in the lightly doped drain (LDD) region and the  $P^+$  region of LTPS TFT device on panel, respectively. Here, the  $N^-$  doping is a self-aligned process without extra mask. All ion doping processes were completed; the doping activation was performed by rapid thermal annealing (RTA). After the inter-metal dielectric (IMD) layer was deposited, the contact holes and the metal pads were formed for interconnection, as shown in Fig. 2.5 Moreover; hydrogenation was used to improve the device performance [15]. Finally, all LTPS thin-film devices, including diodes and transistors, were finished after their contact holes and metal pads formation.

For a-Si TFT-LCDs, TAB-ICs are connected to the left and bottom side as the Y driver and the X driver, respectively. Integration of the Y and X drivers with LTPS

TFTs requires PCB (printed circuit board) connections on the bottom of the panel only. The PCB connection pads are thus reduced to one-twentieth the size of those in a-Si TFT-LCDs. The most common failure mechanism of TFT-LCDs, disconnection of the TAB-ICs, is therefore decreased significantly. For this reason, the reliability and yield of the manufacturing can be improved. Decreasing the number of TAB-IC connections also achieves a high-resolution display because the TAB-IC pitch (spacing between connection pads) limits display resolution to 130 ppi (pixels per inch). A higher resolution of up to 200 ppi can be achieved by LTPS TFT-LCDs. Therefore, the SOP technology can effectively relax the limit on the pitch between connection terminals to be suitable for high-resolution display. Furthermore, eliminating TAB-ICs allows more flexibility in the design of the display system because three sides of the display are now free of TAB-ICs [11]. Fig. 2.9 shows a comparison of a-Si and LTPS TFT-LCD modules. The 3.8" SOP LTPS TFT-LCD panel has been manufactured successfully and it is shown in Fig. 2.10.



### **2.3 BRIEF INTRODUCTION OF BANDGAP REFERENCE CIRCUIT**

Voltage reference is a pivotal building block in mixed signal and radio-frequency systems. For example, a generic mixed-signal system, as shown in Fig. 2.11[16]-[18], has more than one voltage reference due to different voltage reference requirements and also to avoid crosstalk through a single reference circuit. In such a system, a voltage reference is needed for the power-management block, which includes many on-chip DC-DC power converters to provide regulated power. Some other voltage references are utilized in ADCs and DACs, which need high-accuracy reference voltages to provide high-resolution high-speed data conversions even in low supply-voltage conditions.

The concept of bandgap reference circuit in CMOS technology is shown in Fig.2.12. In this circuit, the output voltage ( $V_{REF}$ ) is the sum of a voltage ( $V_D$ ) of the p-n junction diode and the thermal voltage  $V_t$  ( $= kT/q$ ). Hence, by using the circuit design the output voltage  $V_{REF}$  of the fundamental bandgap reference circuit can be expressed by

$$V_{REF} = V_D + KV_t \quad (2-1)$$

Where the voltage  $V_D$  is generated from a p-n junction diode with a negative temperature coefficient of  $-2.2\text{mV}/^\circ\text{C}$  at room temperature, and the thermal voltage  $V_t$  is proportional to absolute temperature (PTAT), which is used to compensate the negative coefficient  $V_D$ , has a temperature coefficient of  $+0.085\text{mV}/^\circ\text{C}$ . After multiplying the PTAT voltage with an appropriate factor and summing with  $V_{EB}$ , the bandgap reference would result in very low sensitivity to temperature. Consequently, if a proper ratio of resistors is kept, the output voltage with very low sensitivity to temperature can be obtained. In general, the  $V_{REF}$  is about 1.25 V in CMOS process.

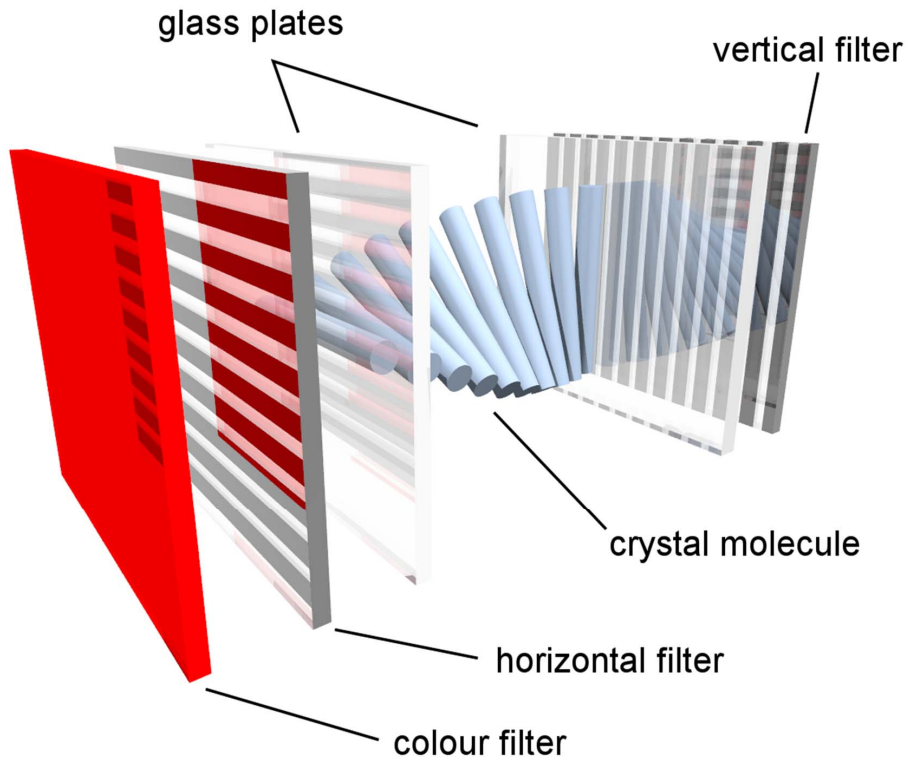


Fig. 2.1 The pixel of a liquid crystal display.

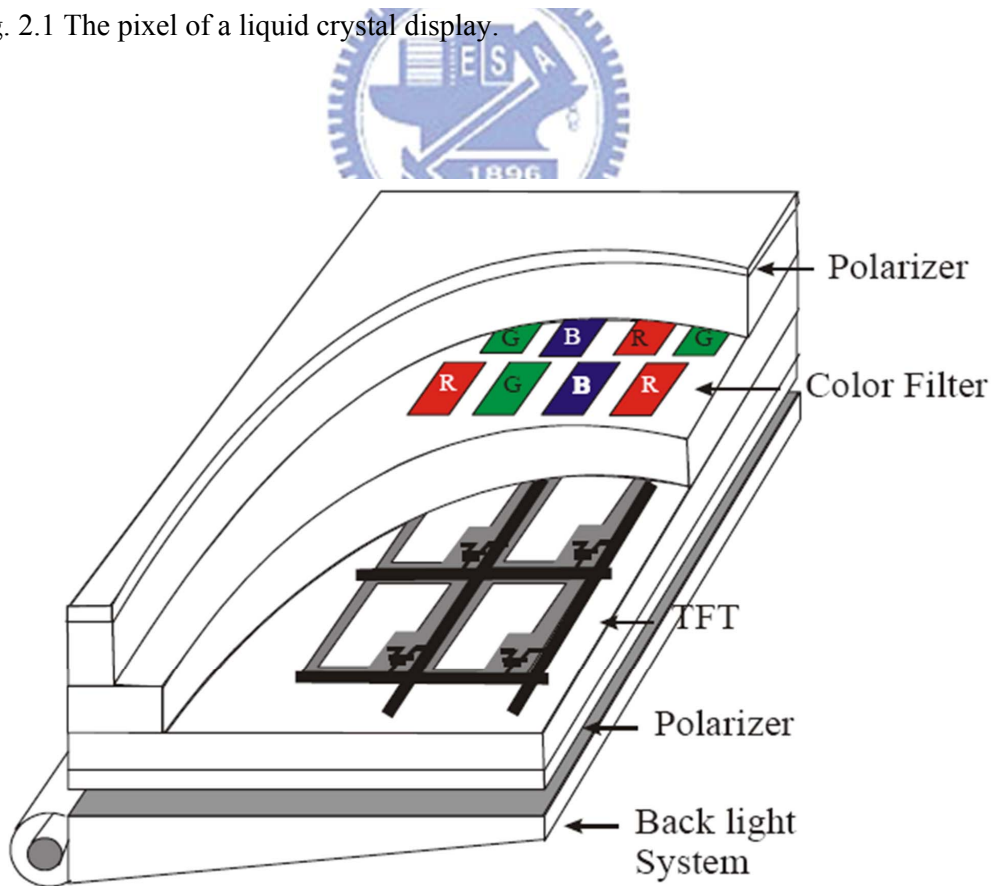


Fig. 2.2 The total cross section structure of a TFT-LCD panel.

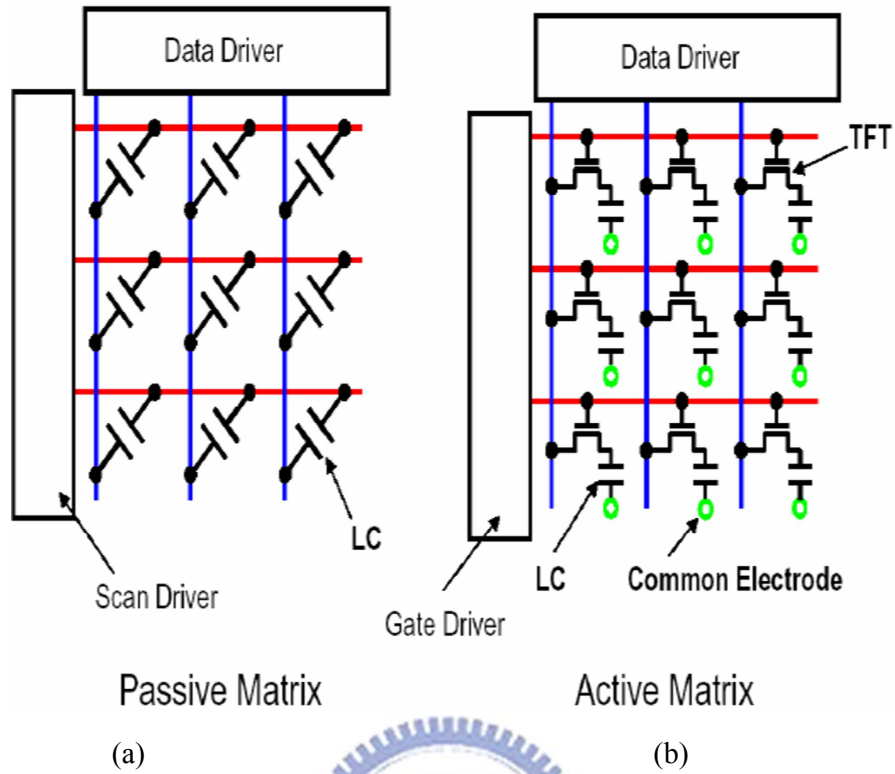


Fig. 2.3 (a) The passive matrix driving liquid crystal and (b) the active matrix driving liquid crystal.



Fig. 2.4 The largest LCD TV produced by sharp in the world in 2008.



Fig. 2.4 The iPhone 3G made by Apple in 2008.

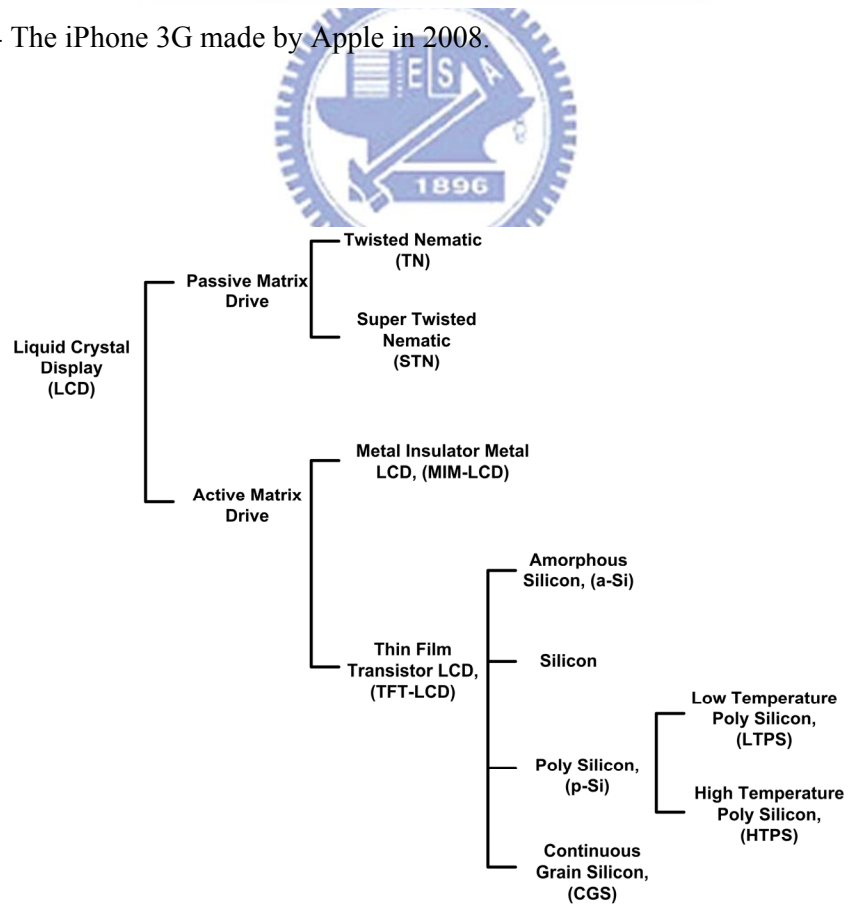


Fig. 2.4 System integration roadmap of LTPS TFT-LCD.



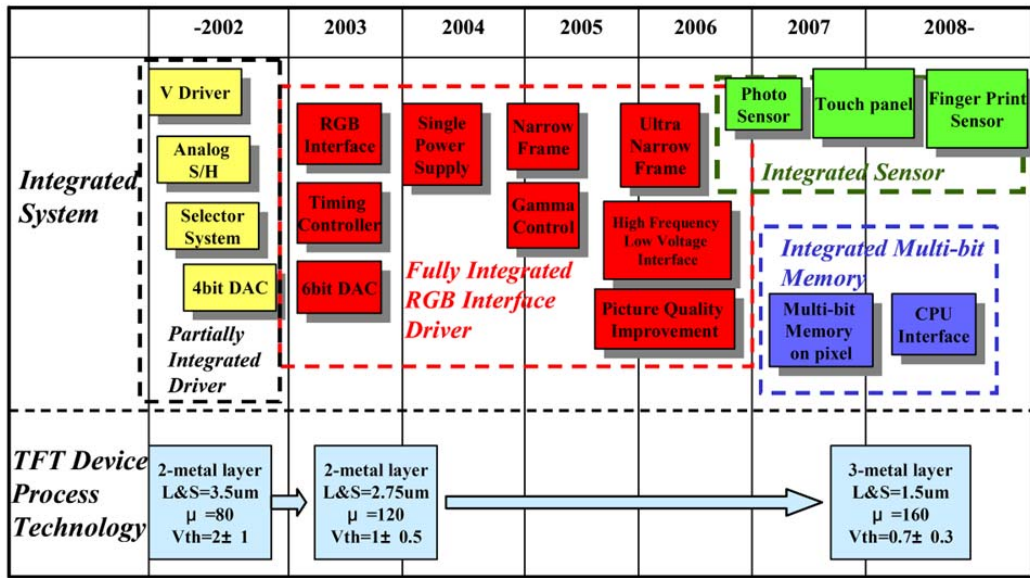


Fig. 2.5 System integration roadmap of LTPS TFT-LCD.

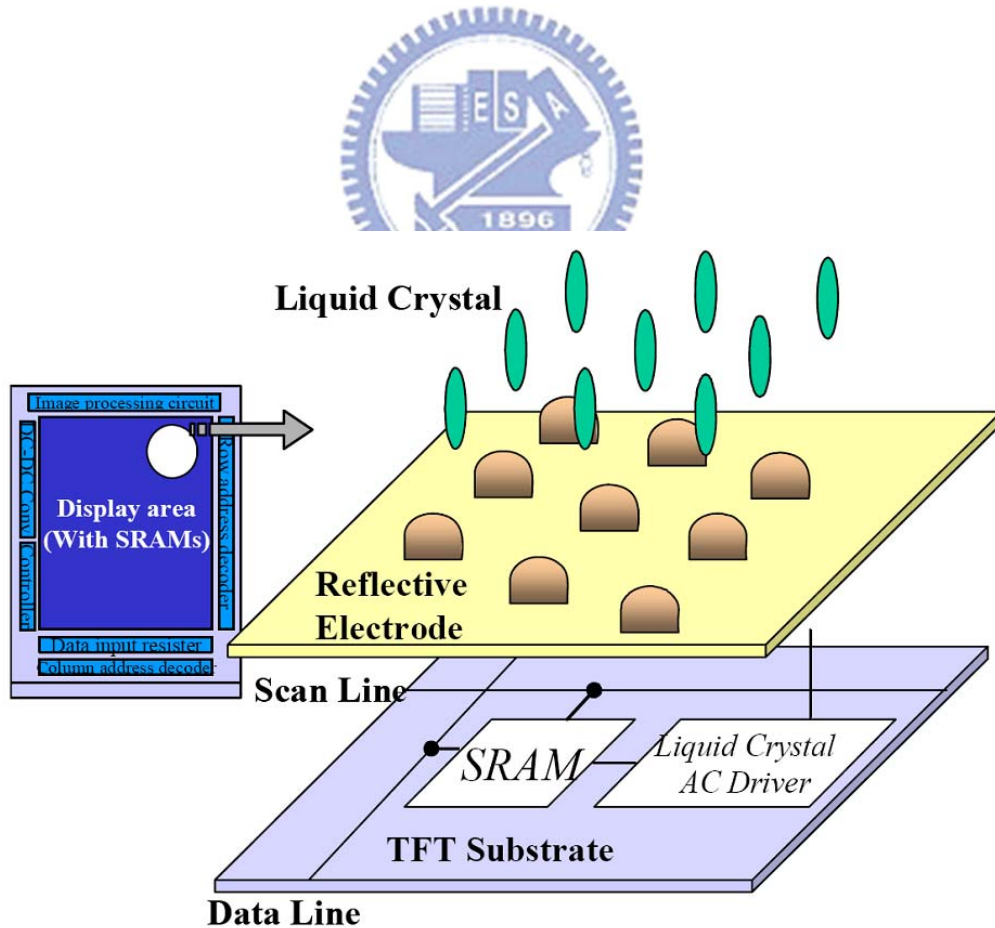
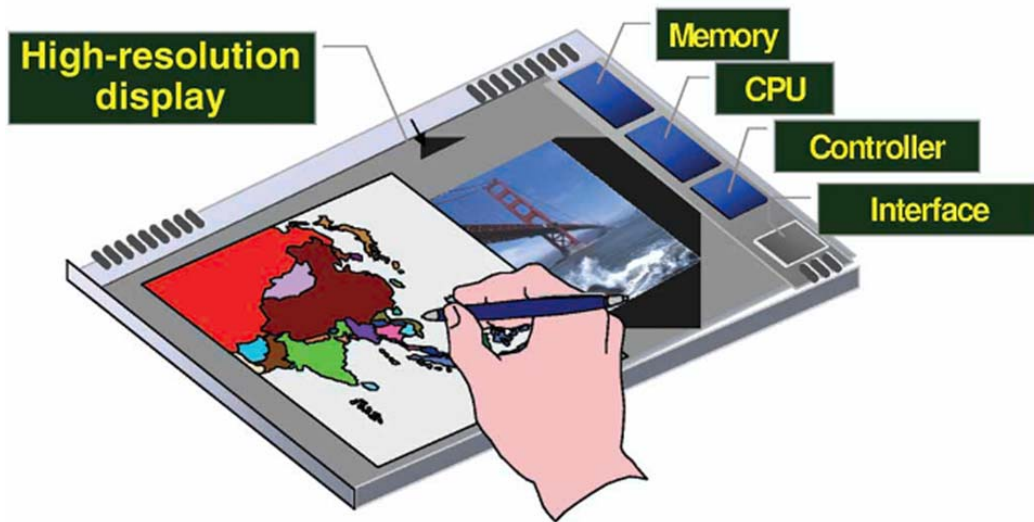
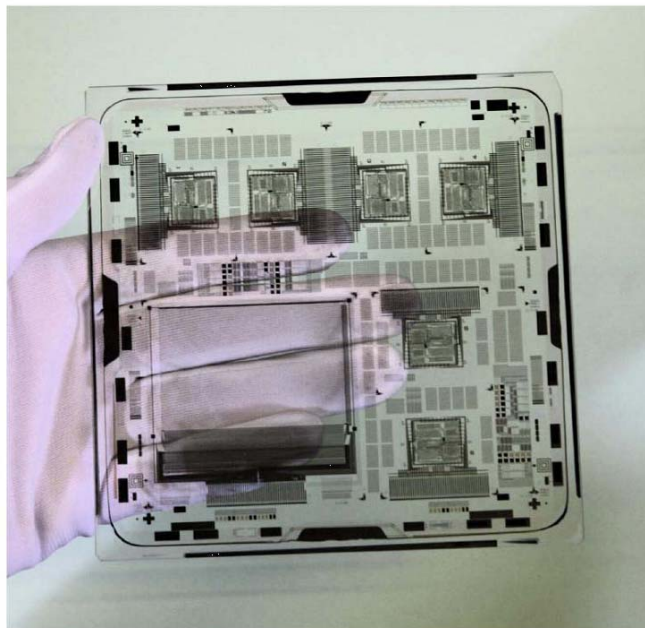
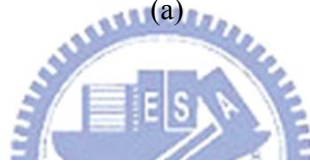


Fig. 2.6 Basic concept of pixel memory technology.



(a)



(b)

Fig. 2.7 (a) The schematic illustration of the “sheet computer” concept and (b) a CPU with an instruction set of 1-4 bytes and an 8b data bus on glass substrate.

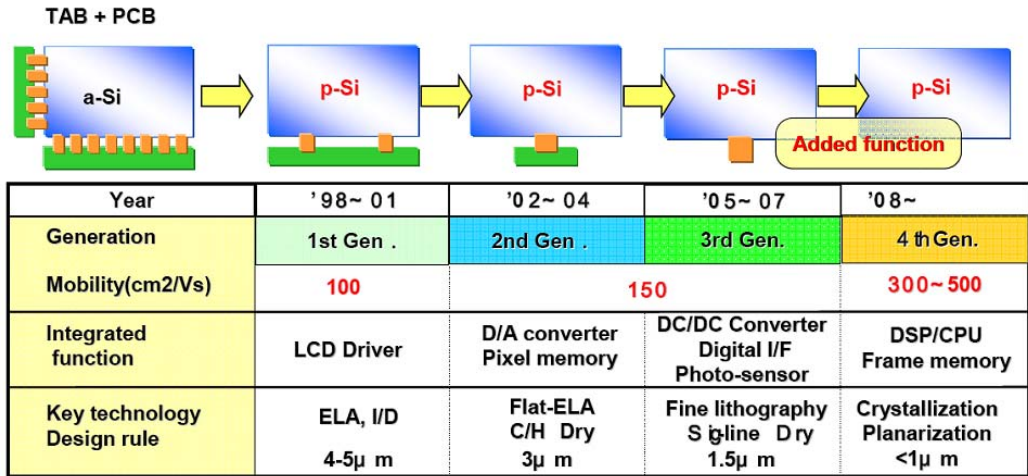


Fig. 2.8 The roadmap of LTPS technologies leading toward the realization of sheet computers.

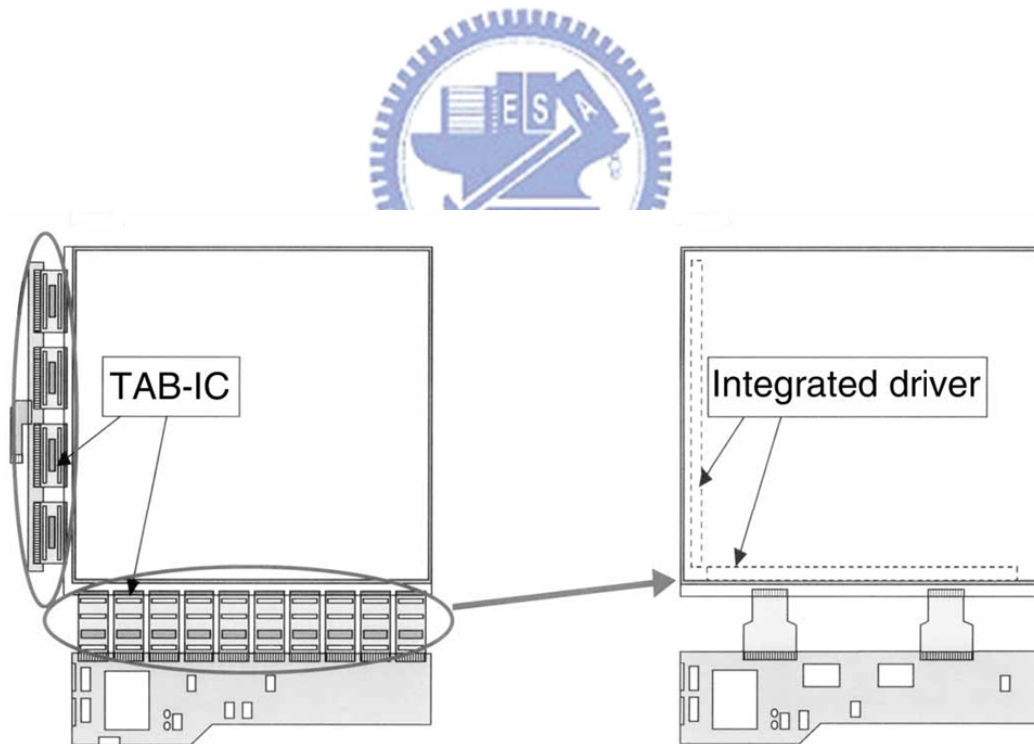


Fig. 2.9 (a) Comparison of an amorphous silicon TFT-LCD module and (b) a low-temperature polycrystalline silicon TFT-LCD module.

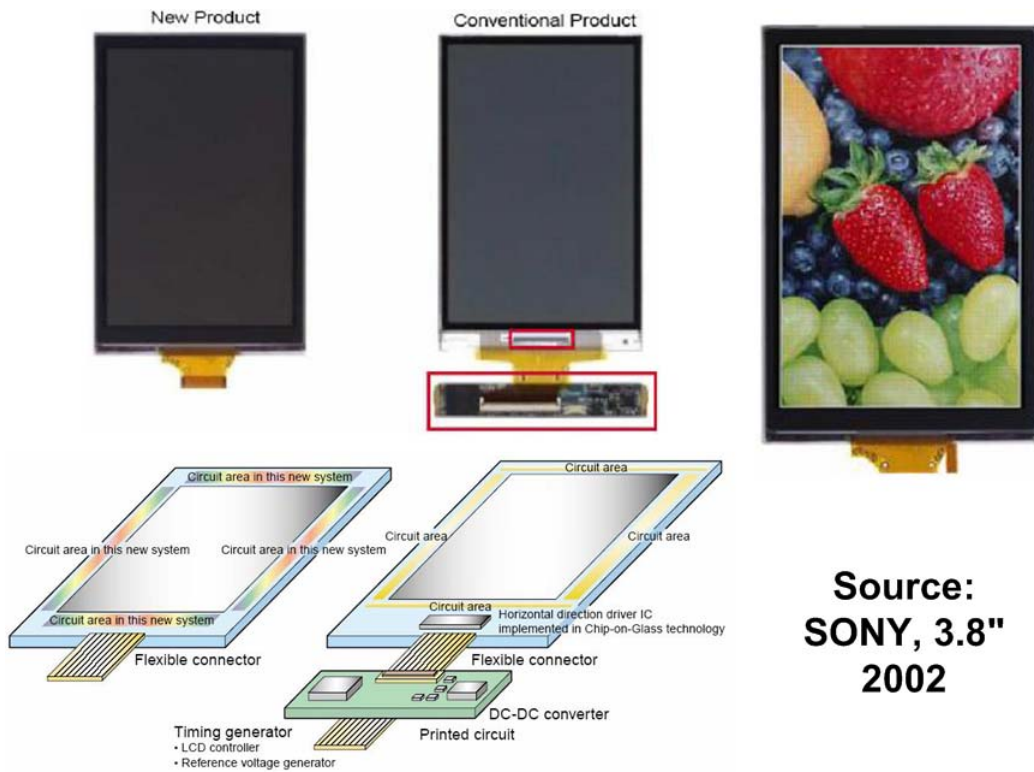


Fig. 2.10 The comparison of new SOP/SOG technology product and conventional product. The new 3.8" SOP LTFS TFT-LCD panel has been manufactured by SONY corp. in 2002.

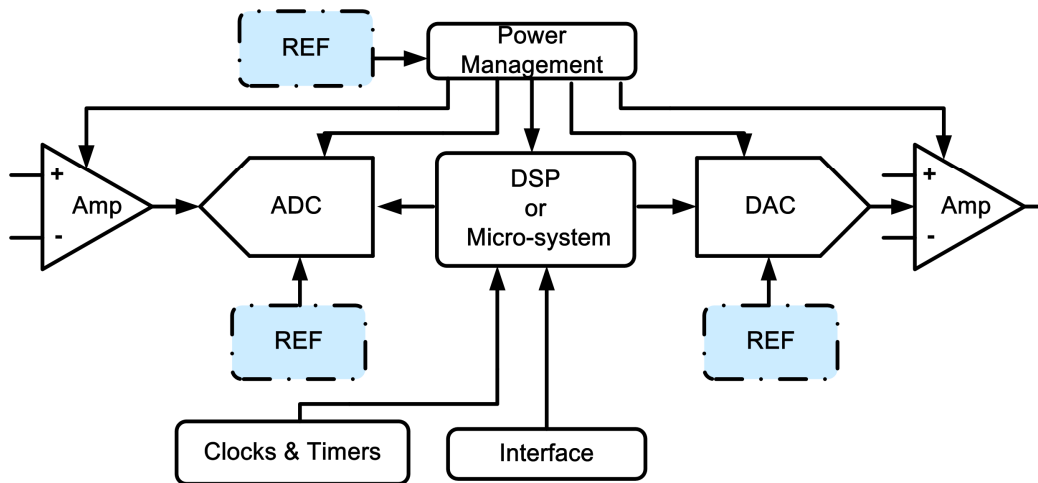


Fig. 2.11 System integration roadmap of LTFS TFT-LCD.

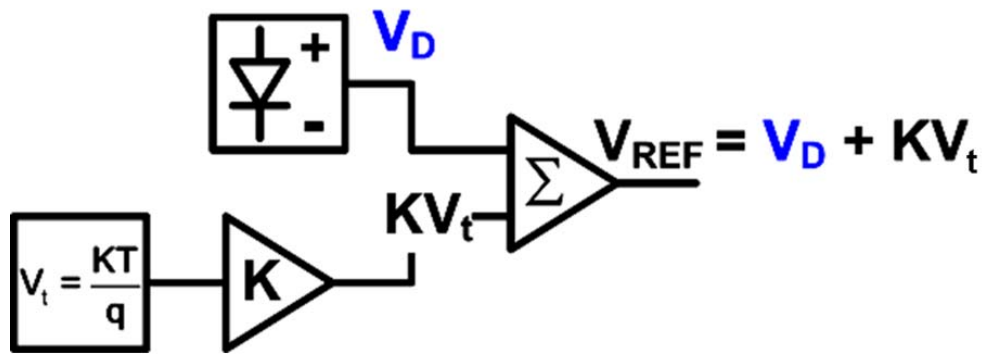


Fig. 2.12 The fundamental concept of bandgap reference circuit in CMOS technology.



# Chapter 3

## Temperature Coefficient of LTPS Devices

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### 3.1 INTRODUCTION

Polycrystalline silicon thin-film transistors (Poly-Si TFTs) have been widely investigated for active-matrix liquid-crystal displays (AMLCDs) and their peripheral driving circuitry due to the increased carrier mobility. However, even with the advanced crystallization technologies such as the excimer laser annealing (ELA) or the sequential laser solidification (SLS) process, it is still observed that the carrier transport in poly-Si TFTs is dominated by the thermionic emission effect. The energy barriers at grain boundaries confine the carrier movement, reduce the field-effect mobility, and make the device characteristics to be strongly dependent on temperature. As a result, to reduce the impact of temperature variation on the performance of analog circuits in the low-temperature polycrystalline silicon (LTPS) process is a very important design challenge.

### 3.2 DEVICE FABRICATION

#### 3.2.1 N-TYPE POLY-SILICON TFT

For device analysis, the typical top-gate, coplanar self-aligned n-type poly-Si

TFT devices which is shown in Fig. 3.1.(a) with 1.25- $\mu\text{m}$ -length LDD structure were used in this study. First, the buffer layer was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density varied from 340  $\text{mJ}/\text{cm}^2$  to 420  $\text{mJ}/\text{cm}^2$ . The lowest laser energy density of the thesis, 340 $\text{mJ}/\text{cm}^2$ , is lower than that in the general LTPS TFT process about 400  $\text{mJ}/\text{cm}^2$ . The measured range is suitable for the general situation. Although the driving ability of the lowest laser energy density is low, the temperature coefficient of the devices have similar tendency with other TCs.

The recrystallized poly-Si films were patterned into the active islands. Afterward, the 60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick Molybdenum was deposited and patterned as the gate electrode. The  $n^-$  doping was performed self-aligned to the gate electrode. The  $n^+$  source/drain region was defined by an additional mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick Titanium/Aluminum/Titanium tri-layer metal was deposited and patterned to be the metal pads. The channel length of the devices keeps as 6  $\mu\text{m}$  while the channel width changes from 30  $\mu\text{m}$  to 6  $\mu\text{m}$ . For the BGR circuit verification, the devices ( $L = 6 \mu\text{m}$ ) fabricated by the 3- $\mu\text{m}$  LTPS process are used.

### **3.2.2 P-TYPE POLY-SILICON TFT**

As shown in Fig. 3.1(b), the structure of P-type poly-Si TFT devices had been measured in this paper. Unlike N-type poly-Si TFT, the LDD structure does not exist in the P-type poly-Si TFT. First, like N-type poly-Si TFT, the buffer layer was deposited on the glass substrate. Then, the undoped 50-nm-thick a-Si layer was deposited and crystallized by XeCl excimer laser with a laser energy density. The recrystallized poly-Si films were patterned into the active islands. Afterward, the

60-nm-thick oxide layer was deposited as the gate insulator. Then, the 200-nm-thick Molybdenum was deposited and patterned as the gate electrode. The  $p^-$  doping was performed self-aligned to the gate electrode. The  $p^+$  source/drain region was defined by an additional mask. The dopants were activated by thermal process. After the deposition of nitride passivation and the formation of contact holes, the 550-nm-thick Titanium/Aluminum/Titanium tri-layer metal was deposited and patterned to be the metal pads.

### 3.3 MEASURED RESULTS AND TEMPERATURE

#### COEFFICIENT MODEL

The measurement setup of devices is shown in Fig.3.2, where the HP 4156 semiconductor and DC probe station are used to measure the I-V characteristic, and temperature controller is used to change the temperature. Fig.3.3 (a) shows the setup to measure voltage  $V_{GS}$  of diode-connected NTFTs under the bias of  $I_{SD}$ , and voltage  $V_{SG}$  of diode-connected PTFTs under the bias of  $I_{DS}$  in Fig 3.3 (b).

First of all, the IV characteristics of devices which are shown in Fig. 3.4 have been measured with changing the temperature, and it's found that the voltage decreases as temperature increases. Hence, the formula of temperature coefficient (TC) can be expressed as

$$\text{Temperature Coefficient (TC)} = \frac{\Delta V_{GS}}{\Delta T}. \quad (3-1)$$

Therefore, the relationships between voltage and temperature of diode-connected PTFTs and diode-connected NTFTs have been shown in Fig. 3.5 and Fig. A.3 individually. Fig. 3.5(a) shows the relationship between  $V_{GS}$  and temperature with identical current  $I_{DS}$  by changing the device dimensions ( $W/L = 10\mu\text{m}/8\mu\text{m}$ ,



30 $\mu\text{m}/8\mu\text{m}$ , and 60 $\mu\text{m}/8\mu\text{m}$ ). It can be found that the TCs increase as the device dimensions increase. The results are similar to TC of the devices which are used to design the BGR circuit in the silicon process. However, the TCs of diode-connected PTFTs which are shown in Fig. 3.5(a) decrease as the device dimensions increase. Furthermore, the relationship between  $V_{SG}$  and temperature by changing current with the same device dimension of the diode-connected NTFT devices have been shown in Fig. 3.5(b). It can be also found that the bias current levels are strong impact on temperature coefficient. The TCs of the diode-connected PTFT devices have the similar results.

The temperature coefficient of these structures of devices have been measured simply, however, the variation of TC is most significant to establish the temperature coefficient model. Besides, the characteristic of TCs of the diode-connected NTFT are suitable for the voltage reference circuit with temperature compensation design. Therefore, we choice the diode-connected NTFT devices to establish the temperature coefficient model and the detail are shows as below amply.

Since the temperature response of the LTPS devices is mostly influenced by the thermionic emission effect with an activation energy associated with the grain boundary barrier height, the relationship between the activation energy and the temperature coefficient is first investigated in this paper. As shown in Fig. 3.7, the activation energy ( $E_a$ ) extracted from the Arrhenius plot of the drain current is depicted as a function of the gate bias ( $V_{GS}$ ). The drain bias ( $V_{DS}$ ) is equal to  $V_{GS}$  for the diode-connected TFT devices. Devices with three different channel widths are measured in Fig. 3.7. Devices are fabricated in the same run with identical crystallization laser energy density. It is found that, similar to the three-terminal LTPS devices,  $E_a$  of the diode-connected devices is strongly dependent on  $V_{GS}$ . Under small

gate bias,  $E_a$  is high. When  $V_{GS}$  is increased,  $E_a$  decreases drastically. It is well known that, for the 3-terminal LTPS TFT devices, the measured activation energy represents the grain boundary energy barrier of the poly-Si film which is sensitive to the poly-Si thin film properties [5], [6]. Channel width has no influence on the thin film properties, so devices with different channel widths exhibit similar  $E_a$  characteristics as those measured in Fig. 3.7.

Then, to extract the temperature coefficient, the setup to measure  $V_{GS}$  of the fabricated devices under the bias of three different current levels (1  $\mu\text{A}$ , 10  $\mu\text{A}$ , and 50  $\mu\text{A}$ ) is shown in Fig. 3.3(a). The measured  $V_{GS}$  of the fabricated device with channel width of 30  $\mu\text{m}$  is plotted as a function of temperature in Fig. 3.8. As shown in Fig. 3.8,  $V_{GS}$  is decreased while the temperature increases. Almost linear relationship between  $V_{GS}$  and temperature can be observed in Fig. 3.8, the slope represents the temperature coefficient (TC). For the diode-connected NTFT with channel width of 30  $\mu\text{m}$  under different current levels, the TC is negative. Additionally, the magnitude of TC decreases when the bias current is increased. When the bias current increases from 1  $\mu\text{A}$ , 10  $\mu\text{A}$ , to 50  $\mu\text{A}$ , the TC varies from -6.04 mV/ $^{\circ}\text{C}$ , -5.04 mV/ $^{\circ}\text{C}$ , to -2.96 mV/ $^{\circ}\text{C}$ . It is noted that for one identical diode-connected device, the increase of bias current gives rise to the increase of operation voltage. As a result, the larger bias current makes the devices operated under larger  $V_{GS}$  with smaller  $E_a$  and smaller magnitude of TC. This result clearly demonstrates the relationship between the activation energy and the TC. Furthermore, the aforementioned discussion can be expressed by the following derivation.

For LTPS TFTs, the drain current  $I_{DS}$  of devices operated in saturation region can be expressed as [19], [20]

$$I_{DS} = \frac{W}{2L} \mu_0 C_{ox} (V_{GS} - V_{TH})^2 \exp\left(-\frac{V_B}{V_T}\right), \quad (3-2)$$

where  $\mu_0$  is the carrier mobility within the grain,  $L$  denotes the effective channel length,  $W$  is the effective channel width,  $C_{ox}$  is the gate oxide capacitance per unit area,  $V_{TH}$  is the threshold voltage of TFT device, which  $V_{GS}$  is the gate-to-source voltage of TFT device.  $V_B$  is the potential barrier at grain boundaries which is associated with the crystallization quality of the poly-Si film. When the activation energy is extracted from the Arrhenius plot of the drain current, it is equal to  $qV_B$ . Fig. 3.15 shows the Arrhenius plot of log drain current  $I_{DS}$  versus  $1/T$  (K) gives the activation energy  $qV_B$  under different gate bias  $V_{GS}$ . The negative slopes ( $-m$ ) represent the activation energy  $qV_B$ , and the different potential barrier of grain boundary  $V_B$  could be calculated with different  $V_{GS}$ . Under small  $V_{GS}$ ,  $V_B$  is large. When the  $V_{GS}$  increases,  $V_B$  decreases rapidly. When the device in circuit is operated under small  $V_{GS}$ , the drain current  $I_{DS}$  of device is dominated by the exponential term and can be simplified by

$$I_{DS} = W\alpha \exp\left(-\frac{V_B}{V_T}\right), \quad (3-3)$$

where  $\alpha$  is only weakly dependent on  $V_{GS}$  but it is insensitive to temperature. Then, the equation of  $V_B$  can be derived as

$$V_B = V_T \ln\left(\frac{W\alpha}{I_{DS}}\right) = \frac{kT}{q} \ln\left(\frac{W\alpha}{I_{DS}}\right). \quad (3-4)$$

When there is a variation of temperature  $\Delta T$ , the corresponding variation on  $V_B$  is

$$\Delta V_B = \frac{k\Delta T}{q} \ln\left(\frac{W\alpha}{I_{DS}}\right). \quad (3-5)$$

Fig. 3-9 shows the measured dependence between potential barrier of grain boundary  $V_B$  and gate-to-source voltage  $V_{GS}$  of diode-connected NTFT with device dimension  $W/L$  of  $30\mu\text{m}/6\mu\text{m}$ , whereas the laser energy density is kept at  $340 \text{ mJ}/\text{cm}^2$ . As shown in Fig. 3-9, the variation of  $V_B$  is related to the variation of  $V_{GS}$ . Assume that the variation of  $V_{GS}$  ( $\Delta V_{GS}$ ) is very small, and a negative linear approximation can

be given between  $\Delta V_B$  and  $\Delta V_{GS}$  as

$$\Delta V_{GS} = -\frac{1}{m} \Delta V_B = -\frac{k\Delta T}{mq} \ln\left(\frac{W\alpha}{I_{DS}}\right), \quad (3-6)$$

where  $m$  is the absolute slope of the linear approximation between  $\Delta V_B$  and  $\Delta V_{GS}$  in

Fig. 3-9. Finally, the temperature coefficient (TC) can be found as

$$TC = \frac{\Delta V_{GS}}{\Delta T} = -\frac{k}{mq} \ln\left(\frac{W\alpha}{I_{DS}}\right) = -\frac{\Delta V_B}{m\Delta T}. \quad (3-7)$$

Even though the increase of  $V_B$  accompanies with the increase of  $m$ , the variation of  $V_B$  can be more significant than that of  $m$  under a proper design.

The activation energy, as well as the grain boundary barrier, should be related to the grain structure and the grain boundary property where shown in Fig.3.10. It is therefore presumed that the laser energy density of the ELA process influences the grain structure and affects the TC of the devices. The laser energy density has the great impact on grain boundary barrier. Fig. 3.10(a) shows the activation energy of the diode-connected devices with the poly-Si film crystallized under different laser energies (340, 400, and 420 mJ/cm<sup>2</sup>). The temperature coefficients can't be changed significantly by laser energy density in the thesis because the measured results under constant current make the devices have toleration of laser energy density. The channel width of the TFT device studied in Fig. 3.10(a) is 30  $\mu\text{m}$ . The activation energy is found to be reduced with increasing laser energy density. As a result, the TC of the devices with higher laser energy density is also smaller than those with lower laser energy density as shown in Fig. 3.10(b). However, the influence of laser energy density on the TC is not significant. When the laser energy density changes  $\pm 10\%$ , the temperature coefficient changes only about  $\pm 2.75\%$ . The reason can be explained by identifying the biasing points of three devices in Fig. 3.10(a). The operation voltages of three devices under the bias of 10- $\mu\text{A}$   $I_{DS}$  which are indicated by the arrow symbols

in Fig. 3.10(a). It is found that the activation energies of the three biasing points are similar. This makes the TC insensitive to the deviation of the laser energy density in the ELA process. Similar results can be also observed for the devices with small channel width of 6  $\mu\text{m}$  in Fig. 3.11(a) and Fig. 3.11(b), where the laser energies for poly-Si film crystallized are also 340, 400, and 420  $\text{mJ}/\text{cm}^2$ .

The influence of the channel width on the TC, however, is found to be significant. When the diode-connected devices are biased under a constant current of 10  $\mu\text{A}$ ,  $V_{GS}$  of TFT devices with channel widths of 6  $\mu\text{m}$  and 30  $\mu\text{m}$  are plotted as a function of temperature in Fig. 3.12, whereas the laser energy density is kept at 400  $\text{mJ}/\text{cm}^2$ . Obviously, the wide-channel-width device exhibits more negative TC than the narrow-channel-width device. From Fig. 3.7, it has been observed that the channel width has only little influence on the device activation energy. However, when all the devices are biased by identical current source, the wide-channel-width devices are operated under small  $V_{GS}$  and the narrow-channel-width devices are operated under large  $V_{GS}$ . When  $V_{GS}$  is reduced, the activation energy is drastically enlarged as shown in Fig. 3-7. As a result, the absolute value of the temperature coefficient is significantly enlarged by increasing the channel width. Such a phenomenon can be also explained by Eq. (3.7).

Eq. (3-7) shows the relationship between temperature coefficient and the slope (m).  $V_{GS}$  is strongly dependence of the channel width  $W$ . Fig. 3.4 shows that the  $V_{GS}$  decreases as  $V_B$  increases. Therefore, the width channel width corresponds to the high temperature coefficient. The channel width can be obtained by  $V_{GS}$  for integrate circuit design.

Finally, the TC of the diode-connected NTFT devices biased under a 10- $\mu\text{A}$  current are plotted in Fig. 3.13. The influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices are compared. It can be

concluded that the influence of ELA laser energy density or the poly-Si thin film property on the TC is relatively small. This makes the voltage reference circuit with temperature compensation not sensitive to the deviation of the laser annealing process in the LTPS technology. On the contrary, changing the device channel width can effectively change the TC of the diode-connected device. This enables the designer to modulate the TC of the diode-connected devices easily. Furthermore, Fig.3.14 shows the comparison between the measurement and calculated results of Eq. (3-7). The potential barrier of grain boundary  $V_B$  could be calculated by the Arrhenius plot shown in Fig. 3.15. Therefore, the temperature coefficient could be calculated by Eq. (3-7), and the compared results are almost similar.

### 3.4 CONCLUSION

The temperature coefficient of TFT devices in LTPS technology is strongly dependent on the activation energy of the devices. With a suitable control, higher activation energy gives rise to higher absolute value of the temperature coefficient. The influence of the laser energy density in ELA process on the temperature coefficient of the devices is not significant. On the other hand, the bias current level and the channel width have a strong impact on the device temperature coefficient. As a result, the temperature coefficient of devices can be controlled by regulating the channel width of the devices. With an appropriate circuit design, a positive temperature coefficient can be generated by using the voltage drop between devices those have different temperature coefficients (different channel widths). Then, the positive temperature coefficient can be used to compensate the negative temperature coefficient from the devices.

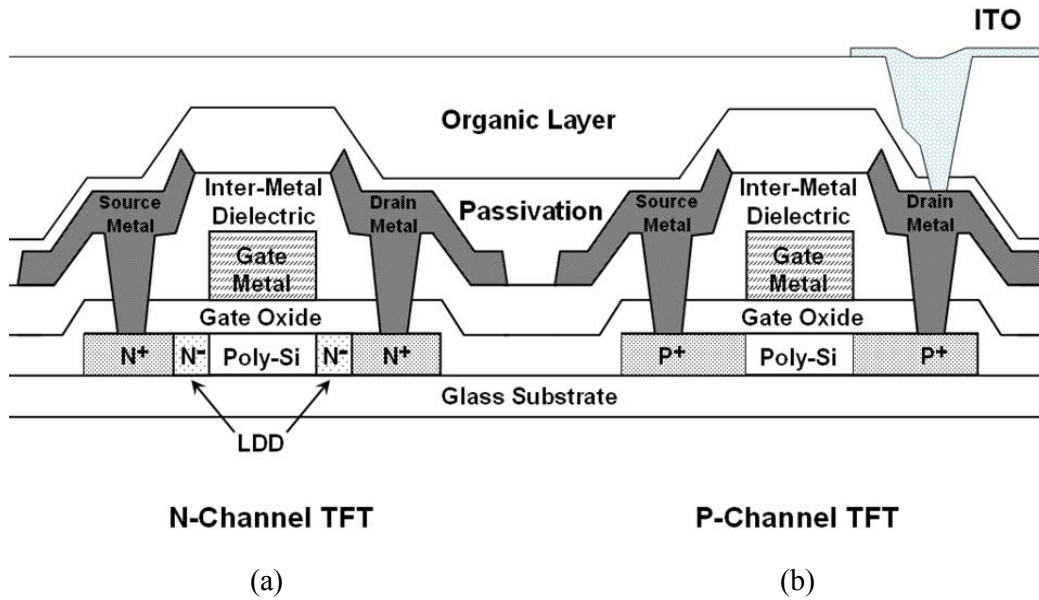


Fig. 3.1. (a)The structure of N-Channel TFT, and (b) P-Channel TFT devices in LTPS process.

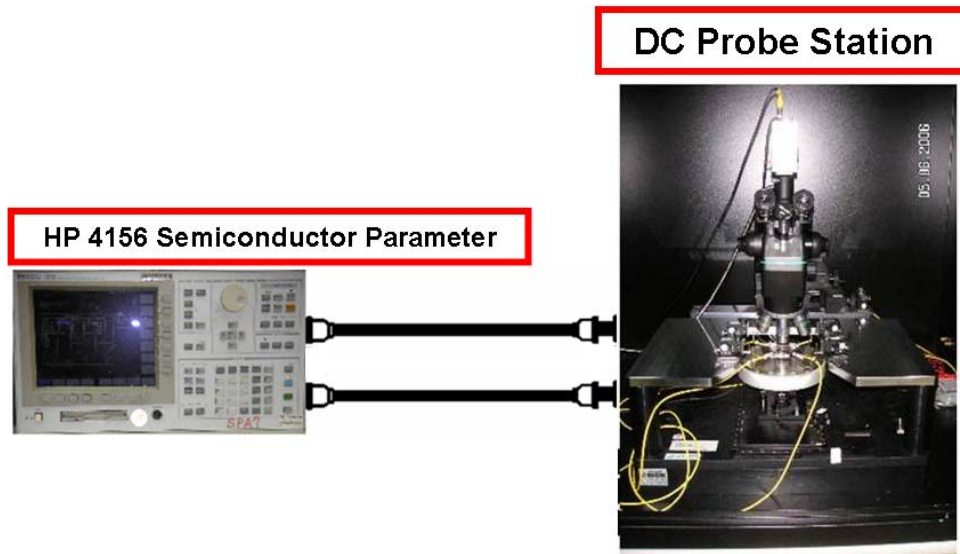


Fig. 3.2. (a)The measurement setup which including temperature controller, HP 4156 semiconductor, and DC probe station.

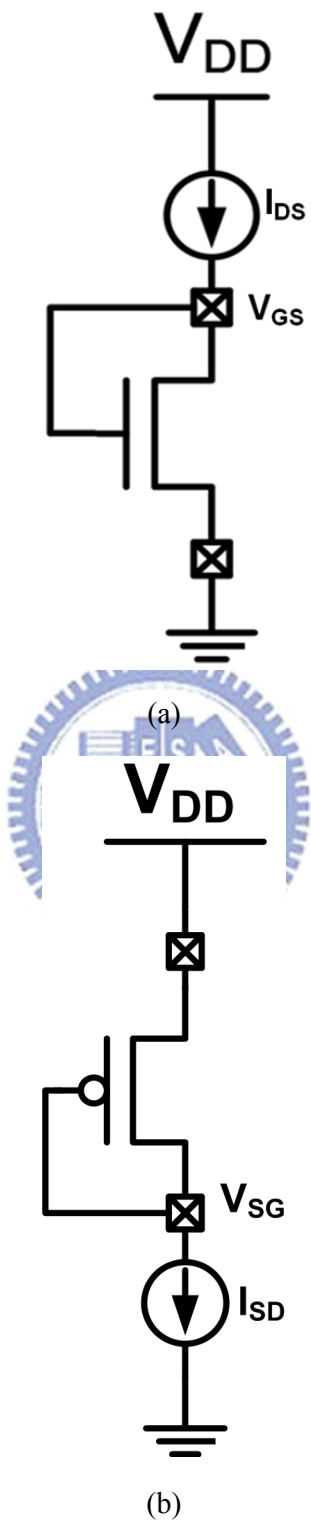
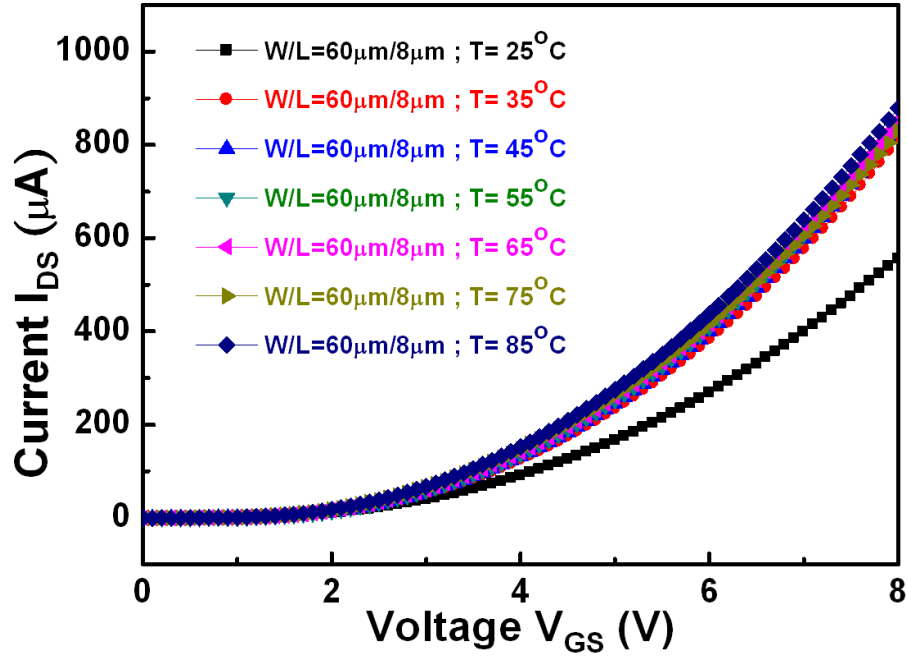
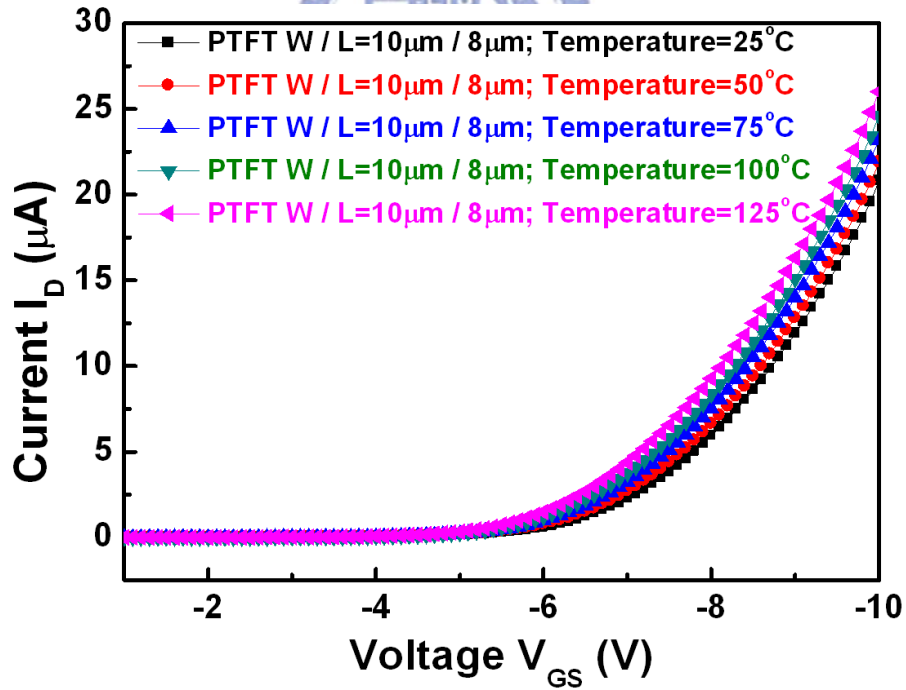


Fig. 3.3. (a)The setup to measure voltage  $V_{GS}$  of diode-connected NTFTs under the bias of  $I_{SD}$ , and voltage  $V_{SG}$  of diode-connected PTFTs under the bias of  $I_{DS}$ .



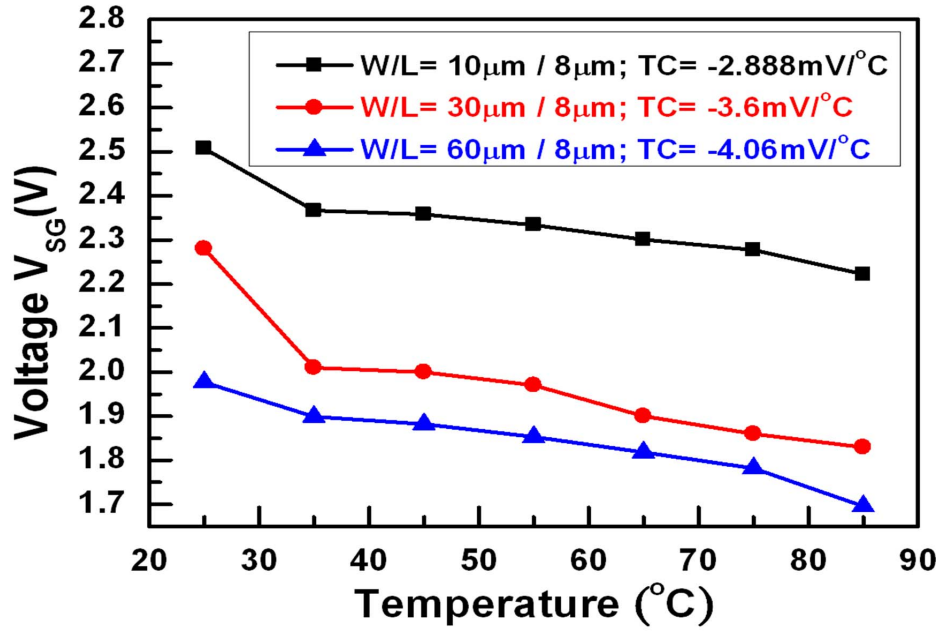


(a)

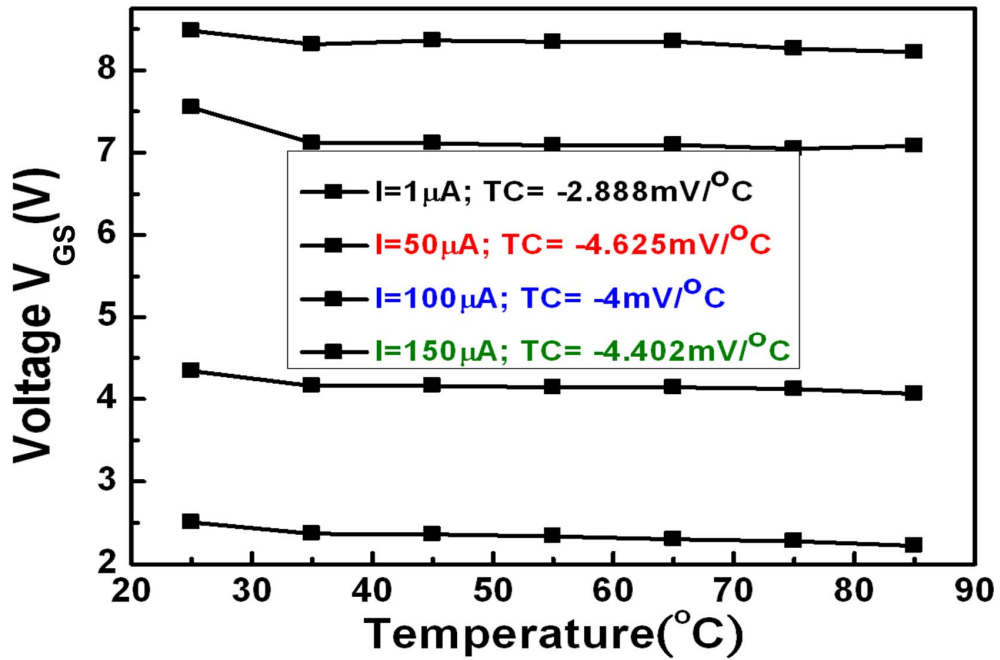


(b)

Fig. 3.4. (a) The I-V characteristic with changing the temperature of NTFT devices, and (b) PTFT devices.



(a)



(b)

Fig. 3.5. (a) The relationship between  $V_{SG}$  and temperature under identical  $I_{DS}$  (b) with the same device dimension of the diode-connected NTFT device.

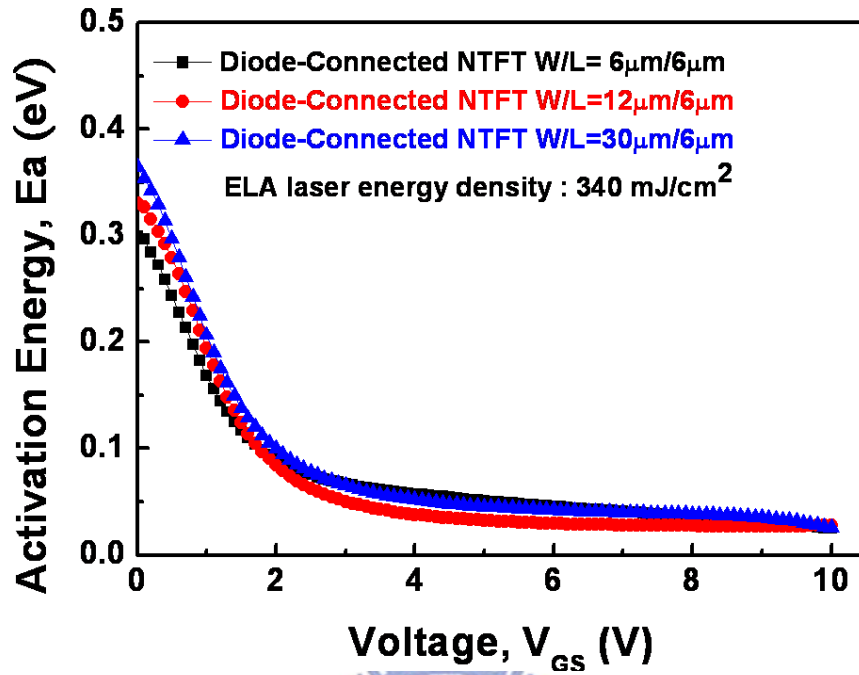


Fig. 3.6. The activation energy as a function of  $V_{GS}$  for diode-connected NTFTs with W/L as 6 $\mu$ m/6 $\mu$ m, 12 $\mu$ m/6 $\mu$ m, and 30 $\mu$ m/6 $\mu$ m.

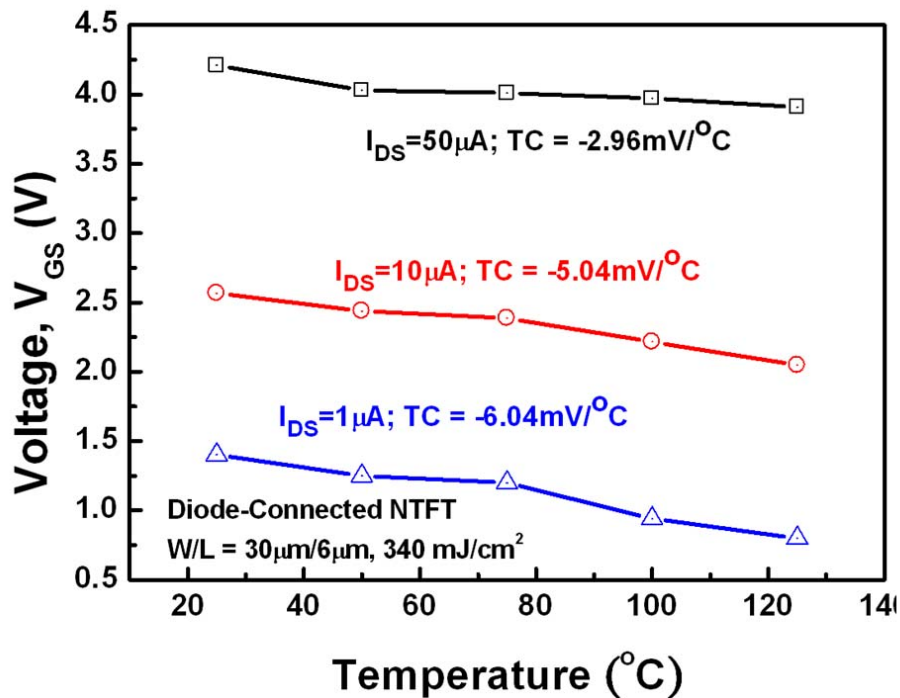


Fig. 3.7. The relationship between  $V_{GS}$  and temperature under three different current levels (1  $\mu$ A, 10  $\mu$ A, and 50  $\mu$ A).

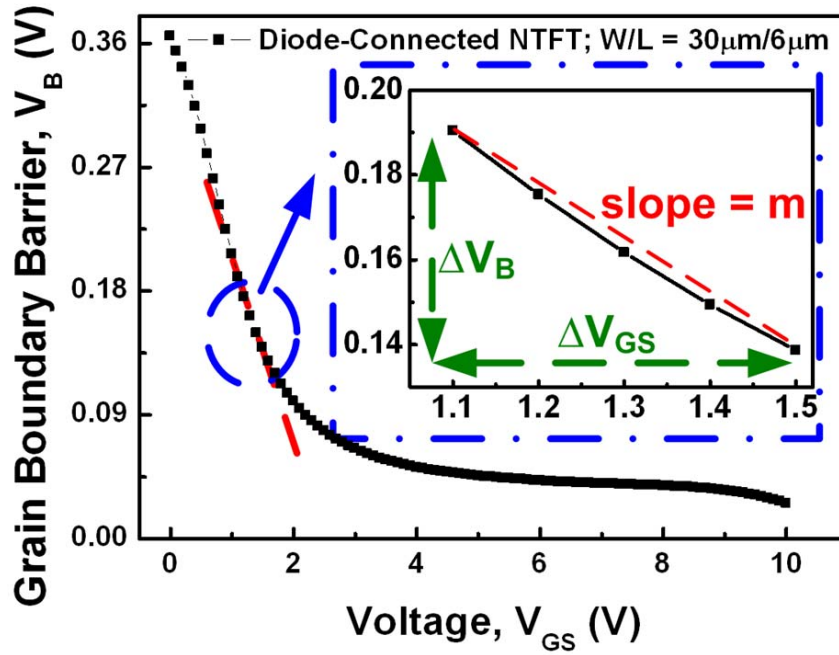
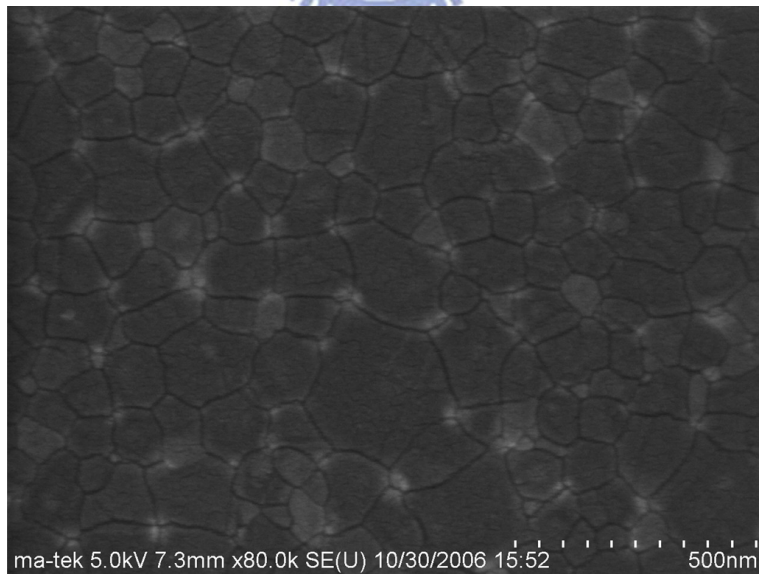
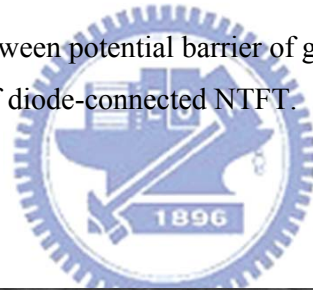
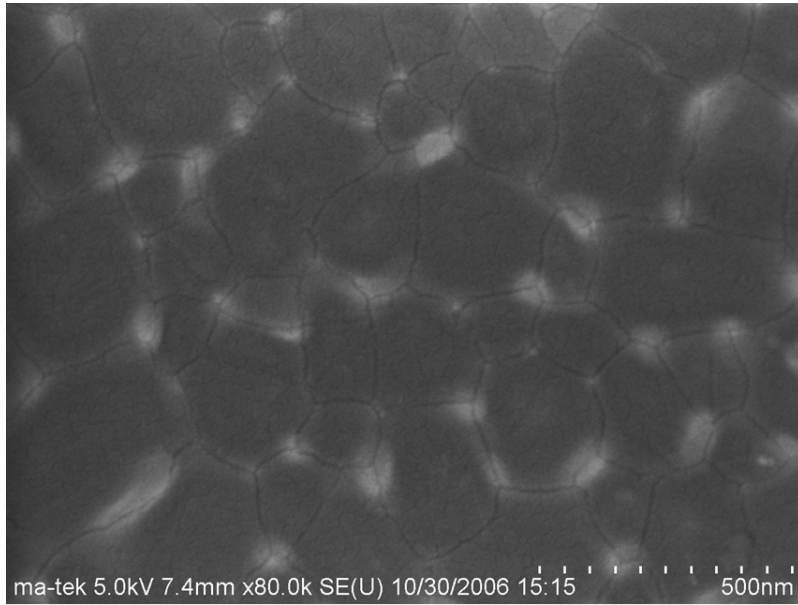


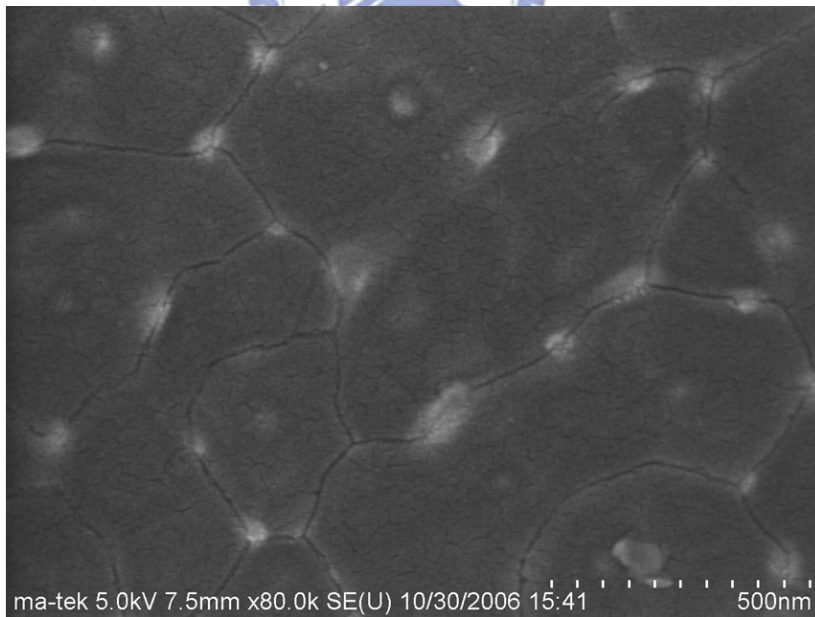
Fig. 3.8. The dependence between potential barrier of grain boundary  $V_B$  and gate-to-source voltage  $V_{GS}$  of diode-connected NTFT.



(a)

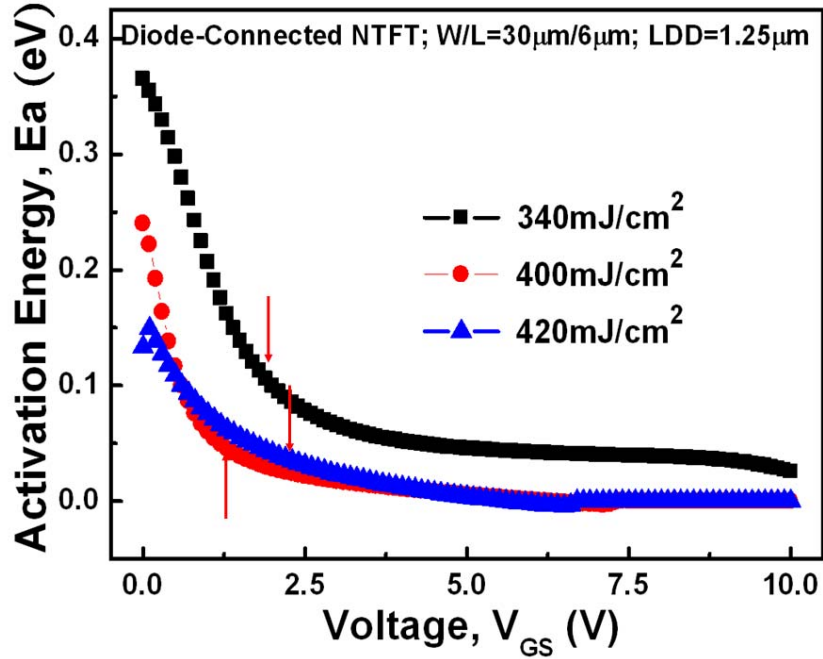


(b)

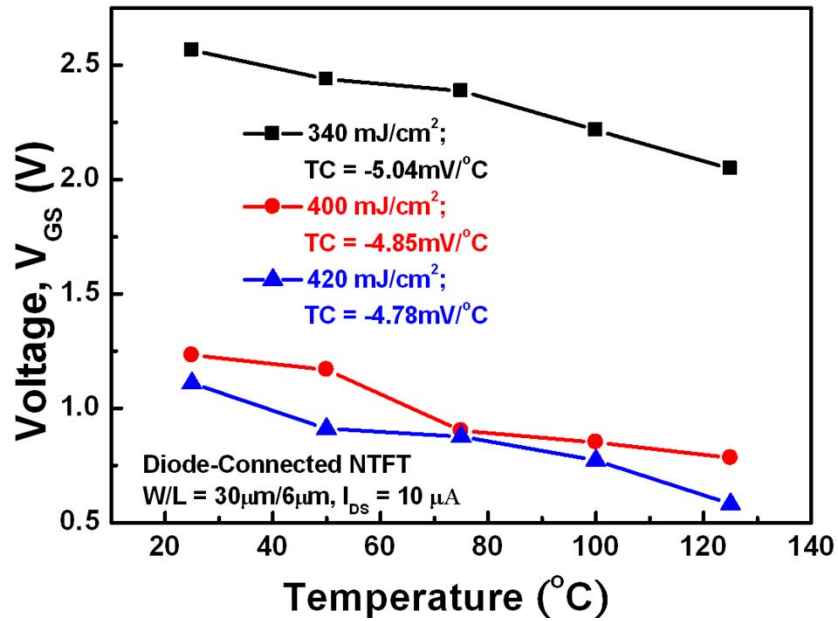


(c)

Fig. 3.9. The grain size with poly-Si film crystallized by laser energy density as (a) 340, (b) 380, and (c) 420 mJ/cm<sup>2</sup>.

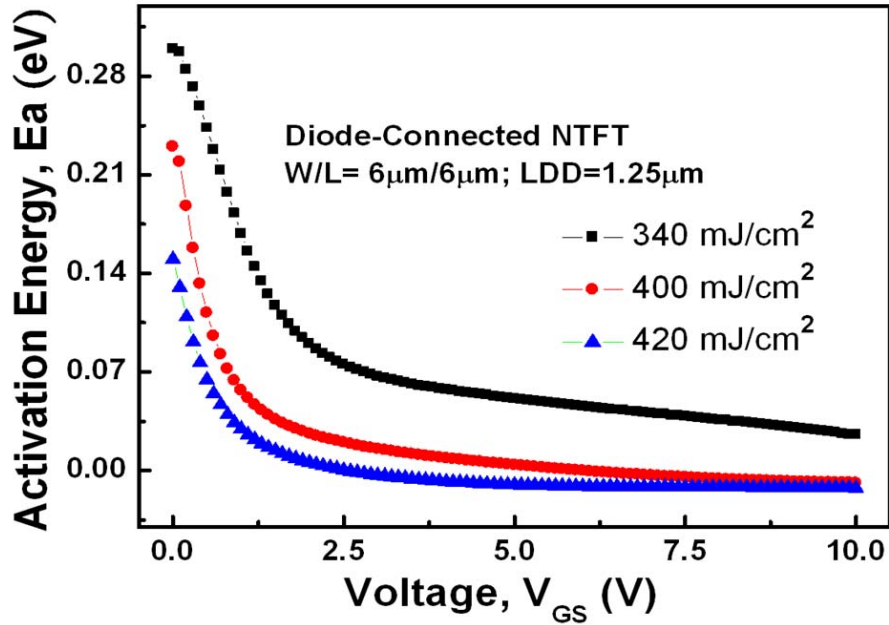


(a)

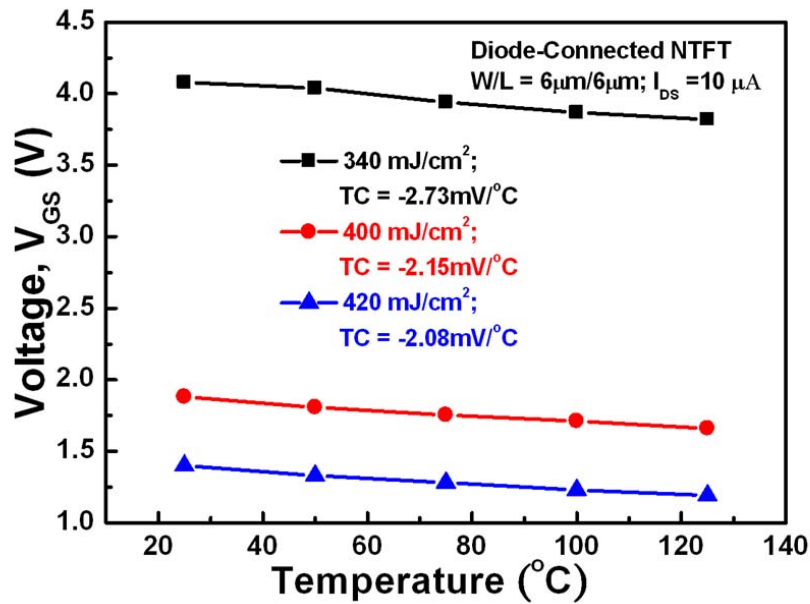


(b)

Fig. 3.10. (a) The activation energy as a function of  $V_{GS}$  for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm<sup>2</sup>. (b) The relationship between  $V_{GS}$  and temperature under identical  $I_{DS}$  of 10  $\mu$ A. Devices W/L are 30 $\mu$ m/6 $\mu$ m.



(a)



(b)

Fig. 3.11. (a) The activation energy as a function of  $V_{GS}$  for diode-connected NTFTs with poly-Si film crystallized by laser energy density as 340, 400, and 420 mJ/cm<sup>2</sup>. (b) The relationship between  $V_{GS}$  and temperature under identical  $I_{DS}$  as 10  $\mu$ A. Devices W/L are 6 $\mu$ m/6 $\mu$ m.

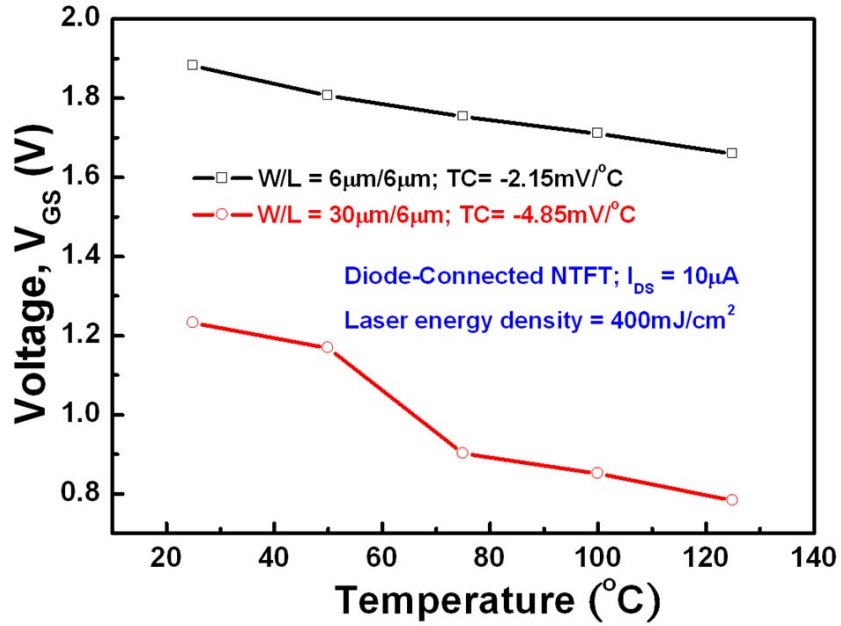


Fig. 3.12. The relationship between  $V_{GS}$  and temperature of devices with different channel widths under identical  $I_{DS}$  of 10  $\mu$ A.

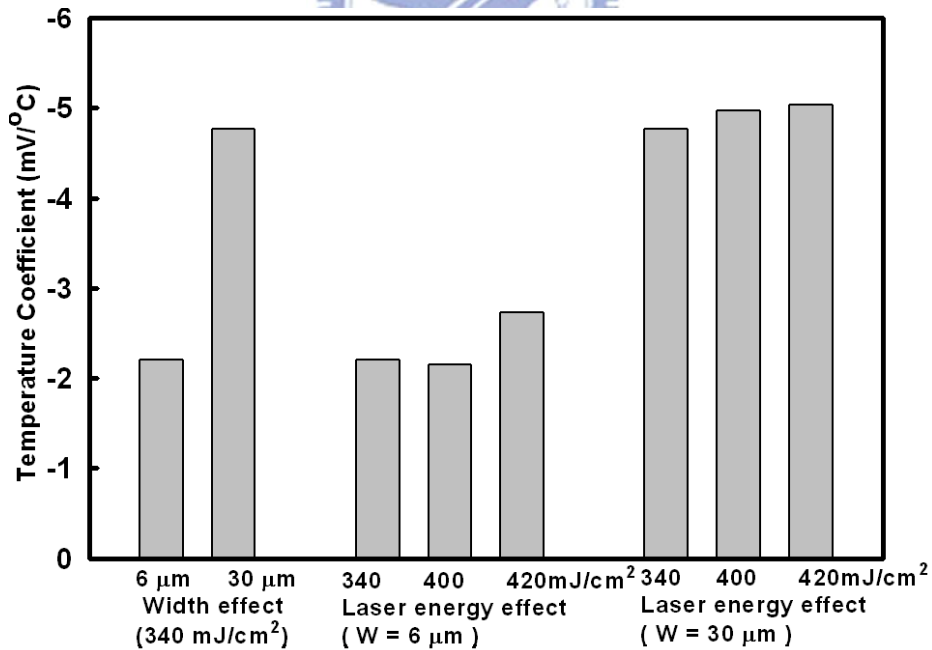


Fig. 3.13. The TC of the diode-connected NTFT devices biased under a 10- $\mu$ A current source to investigate the influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices.



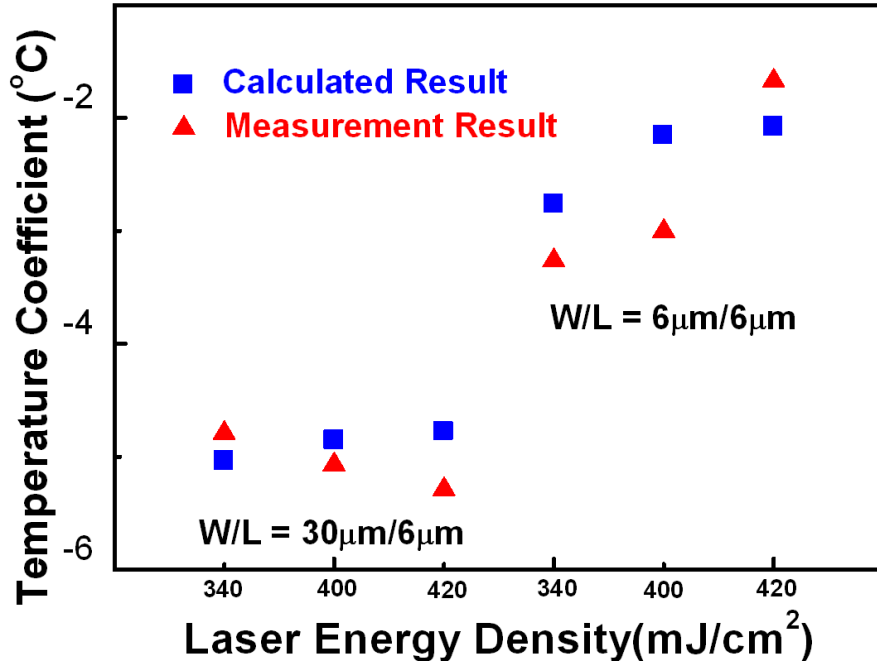


Fig. 3.14. The TC of the diode-connected NTFT devices biased under a 10- $\mu$ A current source to investigate the influences of channel width and crystallization laser energy on the TC of the diode-connected NTFT devices.

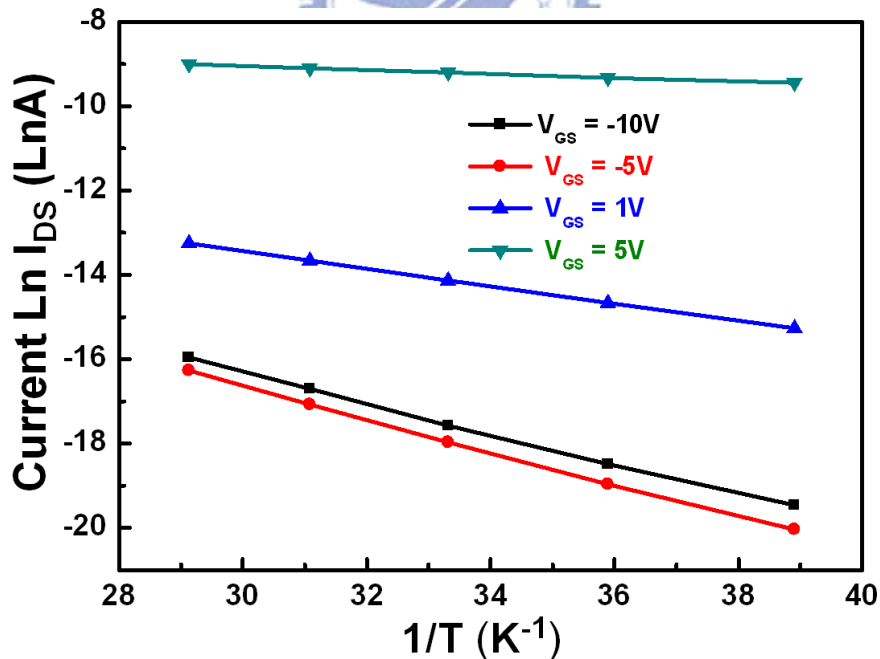


Fig. 3.15. The Arrhenius plot of  $\log(\text{Current})$  versus  $1/T(\text{K})$  gives the activation energy under different  $V_{GS}$ .

# Chapter 4

## On-Glass Voltage Reference Circuit with Temperature Compensation in LTPS process

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### 4.1 INTRODUCTION

Reference voltage generators are widely used in analog and digital circuits, such as DRAM, flash memory, analog-to-digital converter (ADC), and so on. The voltage reference circuit with temperature compensation is the major design to provide a stable voltage reference with low sensitivity to the temperature and the supply voltage. However, the BGR circuit is one of the most famous and widespread voltage reference circuits with temperature compensation. So far, many techniques in CMOS process have been proposed to develop voltage or current references, which can be almost independent of temperature and power-supply voltage.

### 4.2 TRADITIONAL BANDGAP CIRCUIT DESIGN

#### 4.2.1 TRADITIONAL BANDGAP REFERENCE CIRCUIT IN CMOS TECHNOLOGY

The working principle of a bandgap voltage reference can be illustrated by Fig. 4.1[21], [22]. Since  $V_{BE}$  decreases approximately linear with temperature while  $VT$

increases linearly with temperature, a low-temperature-dependence  $V_{MF}$  can be obtained by scaling up  $V$ , and summing it with  $V_{BE}$ . The above-mentioned concept can be implemented as shown in Fig. 3 [22] by using parasitic vertical BJTs.

A traditional implementation of bandgap reference circuit in CMOS technology is shown in Fig. 1 [11]. In this circuit, the output voltage ( $V_{REF}$ ) is the sum of a base-emitter voltage ( $V_{EB}$ ) of BJT Q3 and the voltage drop across the upper resistor R2. The BJTs (Q1, Q2, and Q3) are typically implemented by the diode-connected vertical parasitic PNP bipolar junction transistors in CMOS process with the current proportional to  $\exp(V_{EB}/V_T)$ , where  $V_T (=kT/q)$  is the thermal voltage. Under constant current bias,  $V_{EB}$  is strongly dependent on  $V_T$  as well as temperature. The current mirror is designed to bias Q1, Q2, and Q3 with identical current. Then, the voltage drop on the resistor R1 can be expressed by

$$V_{R1} = V_T \ln\left(\frac{A_1}{A_2}\right), \quad (4-1)$$

where  $A_1$  and  $A_2$  are the emitter areas of Q1 and Q2. It is noted that  $V_{R1}$  exhibits a positive temperature coefficient when  $A_1$  is larger than  $A_2$ . Besides, since the current flows through R1 is equal to the current flows through R2, the voltage drop on the resistor R2 can be expressed by

$$V_{R2} = \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right). \quad (4-2)$$

Hence, the output voltage of the traditional bandgap reference circuit can be written as

$$V_{REF} = V_{EB3} + \frac{R_2}{R_1} V_T \ln\left(\frac{A_1}{A_2}\right). \quad (4-3)$$

The second item in Eq. (3) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of  $V_{EB3}$ . In general, the

PTAT voltage comes from the thermal voltage  $V_T$  with a temperature coefficient about  $+ 0.085 \text{ mV}/^\circ\text{C}$  in CMOS technology, which is quite smaller than that of  $V_{EB}$ . After multiplying the PTAT voltage with an appropriate factor ( $R_2/R_1$ ) and summing with  $V_{EB}$ , the bandgap reference circuit would result in very low sensitivity to temperature. Consequently, if a proper ratio of resistors is kept, the output voltage ( $V_{REF}$ ) with very low sensitivity to temperature can be obtained.

From the analysis on traditional BGR circuit, it is known that the realization of BGR circuit in CMOS process strongly depends on the temperature coefficient of BJTs ( $Q_1$ ,  $Q_2$ , and  $Q_3$ ). In other words, the exponential term  $\exp(V_{EB}/V_T)$  in the I-V relationship of BJTs makes it possible to obtain a PTAT voltage from the voltage difference of a large-area BJT and a small-area BJT. The voltage across MOSFETs was not sensitive to temperature, so MOSFETs were seldom used in BGR circuit directly. Unlike MOSFETs, the characteristics of LTPS TFTs are strongly dependent on temperature even when the devices are operated in saturation region [5], [6]. Therefore, it is expected that the BGR circuit can be realized by using only LTPS TFT devices on glass substrate.

## 4.2.2 BANDGAP REFERENCE CIRCUIT BASED ON SUBTHRESHOLD MOSFETS

A pure MOSFET BGR circuit was realized only when the MOSFETs are biased in subthreshold region [9], [23]. In this circuit, the active load of the bandgap reference circuit is shown in Fig. 4.2. Assuming that all transistors of the active load work in the saturation region, the output reference voltage would be given by

$$V_{REF} = V_{th10} + \sqrt{\frac{2I_0}{k_{10}}} \quad (4-4)$$

where  $I_0$  is the bias current of  $M_{10}$ . The temperature coefficient of the output reference voltage consists of a first component due to the temperature dependence of the threshold voltage and a second component due to the temperature dependence of mobility and of the bias current. Since  $I_0$  is proportional to mobility, a bias current proportional to mobility would completely suppress the effect of the temperature dependence of mobility on the output reference voltage.

As a first approximation, we can assume that the threshold voltage of an nMOS transistor linearly decreases with temperature, as shown below:

$$V_{th}(T) = V_{th}(T_0) - K_{t1}(T - T_0) \quad (4-5)$$

where  $T$  is the absolute temperature and  $T_0$  is the absolute temperature at which  $K_{t1}$  is evaluated. As a consequence, in order to achieve the temperature compensation with a perfect cancellation of the temperature dependence of mobility at *any* temperature, the bias current proportional to mobility and to the temperature squared is need, that is,  $I_0 \propto \mu(T)T^2$ . We have found a solution to generate such a current based on MOS transistors operating in the saturation and the subthreshold regions, as will be explained as below.

A circuit formed by transistors numbered from  $M_1$  to  $M_8$  generates a current  $I_0$  as independent as possible of the supply voltage  $V_{DD}$ . Such current is then injected into the diode-connected NMOS transistor  $M_{10}$ . The temperature dependence of  $I_0$  is compensated by the temperature dependence of the gate-source voltage of  $M_{10}$ , generating a temperature-compensated reference voltage  $V_{REF}$ .

The core of the current generator circuit is represented by transistors  $M_1$ – $M_4$ , which determine the value of the current  $I_0$ , whereas transistors  $M_5$  and  $M_6$  impose equal current  $I_1$  in  $M_1$  and  $M_3$  and transistors  $M_7$  and  $M_8$  impose equal current  $I_0$  in  $M_2$  and  $M_4$ . Transistors  $M_1$  and  $M_3$  (indicated with a symbol having a thicker line for the

gate) are 5-V nMOS transistors with a threshold voltage of 0.7 V; all the other transistors are 3.3-V MOS transistors with a threshold voltage of 0.498 V and 0.75 V for nMOS and pMOS, respectively. The two different threshold voltages allow us to bias and in the subthreshold region  $M_1$  and  $M_3$ , at the same time, to bias  $M_2$  and  $M_4$  in the saturation region. Such behavior is achieved by setting the gate-source voltages of  $M_1$ ,  $M_2$  and  $M_3$ ,  $M_4$  to a value between 0.498 V and 0.7 V. The  $I$ - $V$  characteristics of an nMOS transistor that operates in the saturation and the subthreshold regions can be approximated by (1) and (10), respectively.

$$I_D = \mu C_{ox} V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right) [1 - \exp(-\frac{V_{DS}}{V_T})] \quad (4-6)$$

where  $V_T$  is the thermal voltage and  $m$  is the subthreshold slope parameter. In the following, the integer subscript  $i$  will be added to quantities referred to transistor  $M_i$ . The gate-source voltages of  $M_1$  and  $M_2$  ( $M_3$  and  $M_4$ ) are identical and can be extracted from (1) and (10) by considering and in subthreshold with drain current  $I_1$  and  $M_2$  and  $M_4$  in saturation with a drain current  $I_0$ . Then, by enforcing  $V_{GS1} = V_{GS2}$  and  $V_{GS3} = V_{GS4}$ , the thermal voltage of  $M_1$  and  $M_2$  ( $V_{th1}$  and  $V_{th2}$ ) can be expressed as

$$V_{th1} + mV_T \ln\left(\frac{I_1}{\mu C_{ox} V_T^2 W_1 / L_1}\right) = V_{th2} + \sqrt{\frac{2I_0}{\mu C_{ox} W_2 / L_2}} \quad (4-7)$$

$$V_{th3} + mV_T \ln\left(\frac{I_1}{\mu C_{ox} V_T^2 W_3 / L_3}\right) = V_{th4} + \sqrt{\frac{2I_0}{\mu C_{ox} W_4 / L_4}} \quad (4-8)$$

where we have neglected channel length modulation ( $\lambda = 0$ ) and have set the term between square brackets in (10) to unity. Apparently, since the source terminals of all nMOS transistors are grounded, the body effect plays no role and  $V_{th1} = V_{th2}$  and  $V_{th3} = V_{th4}$ . By subtracting (12) from (13), the expression of the current  $I_0$  can be written as

$$I_0 = \frac{\mu C_{ox} W_4 / L_4}{2(N-1)^2} m^2 V_T^2 \ln^2\left(\frac{W_3 / L_3}{W_1 / L_1}\right) \quad (4-9)$$

where  $N \equiv \sqrt{(W_4/L_4)/(W_2/L_2)}$ , Therefore, the output voltage  $V_{REF}$  can be expressed as

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1} \sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}} \ln\left(\frac{W_3/L_3}{W_1/L_1}\right) \quad (4-10)$$

The design of the bandgap reference circuit based on subthreshold region achieves a complete cancellation of the effects of the temperature dependence of carrier mobility for any temperature. Besides, channel length modulation and body effect are compensated, providing very good temperature compensation.

### 4.3 NOVEL ON-GLASS VOLTAGE REFERENCE CIRCUIT WITH TEMPERATURE COMPENSATION

The incorporation of BJTs or diodes into CMOS technology somehow makes the process control difficult. Moreover, to precisely bias the devices in subthreshold region is quite difficult with consideration of process variation. The variation of carrier mobility is also a great challenge in LTPS process.

However, the I-V characteristics of LTPS TFT devices have been found to be strongly dependent on temperature when the devices are operated in the saturation region. Furthermore, as we know that the difference of TCs between the wide-channel-width device and the narrow-channel-width device is very useful if a positive TC can be extracted from the  $V_{GS}$  of the wide-channel-width device to the  $V_{GS}$  of the narrow-channel-width device. This positive TC can be used to compensate the negative TC in the  $V_{GS}$  of TFT devices. Hence, the concept can be applied to design the bandgap reference in LTPS process.

### 4.3.1. Implementation

The new proposed voltage reference circuit with temperature compensation designed and fabricated by a 3- $\mu\text{m}$  LTPS technology is shown in Fig. 4.4. In this circuit, the TFTs  $M_1$ ,  $M_2$ ,  $M_3$ ,  $M_4$ , and  $M_5$  are biased in saturation region. The diode-connected NTFT devices  $M_6$ ,  $M_7$ , and  $M_8$ , which replace the diode-connected BJTs in traditional CMOS BGR circuit (Fig. 4.1) [11], are also biased in saturation region. The nodes  $n_1$  and  $n_2$  are designed to have equal potential by the current mirror circuit.

The channel width of  $M_6$  ( $W_6$ ) is larger than the channel width of  $M_7$  ( $W_7$ ), so the TC of  $M_6$  is more negative than the TC of  $M_7$ . The voltage drop on the resistor  $R_1$  ( $V_{R1}$ ) therefore exhibits a positive TC. If the dependence of  $m$  on  $V_{GS}$  is neglected, the variation of  $V_{R1}$  ( $\Delta V_{R1}$ ) as a function of  $\Delta T$  can be expressed as

$$\Delta V_{R1} = \frac{k\Delta T}{mq} \ln\left(\frac{W_6}{W_7}\right) = \frac{k\Delta T}{mq} \ln N. \quad (4-11)$$

Obviously,  $\Delta V_{R1}$  is proportional to the absolute temperature (PTAT). Hence, a PTAT loop is formed by  $M_6$ ,  $M_7$ , and  $R_1$ . The PTAT current variation  $\Delta I_1$  can be written as

$$\Delta I_1 = \frac{k\Delta T}{mqR_1} \ln N, \quad (4-12)$$

where  $N$  ( $=W_6/W_7$ ) is the channel width ratio of  $M_6$  and  $M_7$ . The current mirror, which is composed of  $M_1$ ,  $M_2$ , and  $M_3$ , imposes equal currents in these three branches  $I_1$ ,  $I_2$ , and  $I_3$  of the circuit. The output voltage ( $V_{REF}$ ) is the sum of a gate-source voltage of TFT  $M_8$  ( $V_{GS8}$ ) and the voltage drop across the upper resistor ( $V_{R2}$ ). Therefore, the output voltage variation ( $\Delta V_{REF}$ ) of the new proposed voltage reference circuit with temperature compensation can be expressed as



$$\Delta V_{REF} = \Delta I_3 R_2 + \Delta V_{GS8} = \frac{R_2}{R_1} \frac{k\Delta T}{mq} \ln N + \Delta V_{GS8}, \quad (4-13)$$

where  $R_1$  and  $R_2$  are the resistances shown in Fig. 9. The first item in Eq. (4-13) with positive TC is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of  $\Delta V_{GS8}$ . After multiplying the PTAT voltage with an appropriate factor (proper ratio of resistors) and summing with  $\Delta V_{GS8}$ , the output voltage of voltage reference circuit with temperature compensation would result in very low sensitivity to temperature.

The proposed voltage reference circuit with temperature compensation has been fabricated in a 3- $\mu\text{m}$  LTPS technology. Figure 4.5 shows the chip photo of the new proposed voltage reference circuit with temperature compensation fabricated on glass substrate. The chip size of the proposed voltage reference circuit with temperature compensation is  $400 \times 380 \mu\text{m}^2$ . The resistance  $R_1$  and  $R_2$  implemented by the poly resistance are also included into the layout.

#### 4.3.2. Measurement Results

First, the measurement of the TC of diode-connected LTPS TFT devices with channel width of  $6 \mu\text{m}$  is performed by changing the temperature from  $25^\circ\text{C}$  to  $125^\circ\text{C}$ . Under a constant driving current of  $10 \mu\text{A}$ , the  $V_{GS}$  as a function of temperature is plotted in Fig. 4.3(a). It can be observed that when temperature increases from  $25^\circ\text{C}$  to  $125^\circ\text{C}$ , the  $V_{GS}$  decreases from  $1.88 \text{ V}$  to  $1.66 \text{ V}$ . In Fig. 4.3(a), the temperature coefficient of this TFT device with channel width of  $6 \mu\text{m}$  is approximated as  $-2.15 \text{ mV}/^\circ\text{C}$ . Furthermore, the TC of diode-connected LTPS TFT devices with a wide channel width of  $30 \mu\text{m}$  is measured. Under a constant driving current of  $10 \mu\text{A}$ , the  $V_{GS}$  as a function of temperature is plotted in Fig. 3.8. As temperature changes from

25°C to 125°C, the  $V_{GS}$  decreases from 1.23V to 0.78V, significantly. In Fig. 3.8, the temperature coefficient of this TFT device with 30- $\mu\text{m}$  channel width is approximated as -4.85 mV/°C. As predicted, the LTPS TFT device with a larger channel width exhibits a larger absolute value of TC.

Fig. 4.6. shows the measurement setup of the voltage reference circuit with temperature compensation in the 3- $\mu\text{m}$  LTPS process. The threshold voltage of TFT devices in a 3- $\mu\text{m}$  LTPS technology is  $V_{thn} \approx V_{thp} \approx 1.25$  V at 25 °C. The total gate area of  $M_6$  is 480  $\mu\text{m}^2$  and that of  $M_7$  is 80  $\mu\text{m}^2$  in this fabrication. The resistors in this chip, formed by poly resistors with minimum process variation, are used to improve the accuracy of resistance ratio. The power supply voltage  $V_{DD}$  is set to 10 V, and the total operating current is 8.97  $\mu\text{A}$ . The measured results of the output voltage ( $V_{REF}$ ) from 25 to 125°C are shown in Fig. 4.7, where the R2 is drawn with different values in the test chips. As R<sub>2</sub> is equal to 500 k $\Omega$ , the measured temperature coefficient of the fabricated voltage reference circuit with temperature compensation on glass substrate is around 195 ppm/°C (without laser trimming after fabrication), whereas the output voltage ( $V_{REF}$ ) is kept at 6.87 V. Furthermore, Fig. 4.8 which are the other tape-out results show the relationship between the output voltage ( $V_{REF}$ ), the voltage drop across the upper resistor ( $V_{R2}$ ), and the voltage drop across the diode connected NTFT ( $V_{M8}$ ). Apparently, the output voltage ( $V_{REF}$ ) is the sum of the voltage drop across the diode connected NTFT ( $V_{GS8}$ ), where is the PTAT voltage, and the voltage drop across the upper resistor ( $V_{R2}$ ) with the negative temperature coefficient.

#### 4.4. DISCUSSION

The measurement results of temperature range shown in the thesis are from 25°C to 125°C, however, the standard of the temperature range for the on-glass analog

circuit design haven not be established up to the present. Nonetheless, the standard of the temperature range for the on-glass circuit design can refer to that for the traditional CMOS analog IC circuit design. The temperature range for CMOS process is from 25°C to 80°C [16]. The temperature range in the thesis is up to 125°C because of considering the thermionic emission effect and hot carrier effect.

## 4.5 SUMMARY

The new proposed voltage reference circuit with temperature compensation realized by all TFT devices has been successfully verified in a 3- $\mu\text{m}$  LTPS process. The measurement results of the voltage reference are  $V_{\text{REF}}$  of 6.87 V with temperature coefficient of 195 ppm/°C, which consumes an operating current of 8.97  $\mu\text{A}$  under supply voltage of 10 V on glass substrate. The new proposed bandgap voltage reference circuit can be used to realize the precise analog circuits in LTPS process for System-on-Panel (SoP) or System-on-Glass (SoG) applications.

Name	Type	Single Finger Size	Multiply	Total Size
$M_1$	PTFT	$10\mu\text{m}/6\mu\text{m}$	1	$10\mu\text{m}/6\mu\text{m}$
$M_2$	PTFT	$10\mu\text{m}/6\mu\text{m}$	1	$10\mu\text{m}/6\mu\text{m}$
$M_3$	PTFT	$10\mu\text{m}/6\mu\text{m}$	1	$10\mu\text{m}/6\mu\text{m}$
$M_4$	NTFT	$10\mu\text{m}/6\mu\text{m}$	6	$60\mu\text{m}/6\mu\text{m}$
$M_5$	NTFT	$10\mu\text{m}/6\mu\text{m}$	6	$60\mu\text{m}/6\mu\text{m}$
$M_6$	NTFT	$6\mu\text{m}/6\mu\text{m}$	8	$48\mu\text{m}/6\mu\text{m}$
$M_7$	NTFT	$6\mu\text{m}/6\mu\text{m}$	1	$6\mu\text{m}6\mu\text{m}$
$M_8$	NTFT	$6\mu\text{m}/6\mu\text{m}$	1	$6\mu\text{m}/6\mu\text{m}$
$R_1$	Resistor	$150\text{K}\Omega$	1	$150\text{K}\Omega$
$R_2$	Resistor	$500\text{K}\Omega$	1	$500\text{K}\Omega$

Table I. The device dimensions of the proposed voltage reference circuit with temperature compensation.

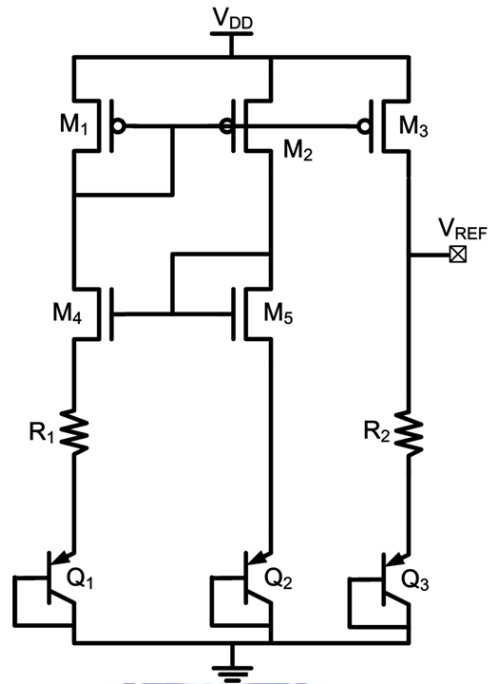


Fig.4.1 The traditional bandgap reference circuit in CMOS technology.

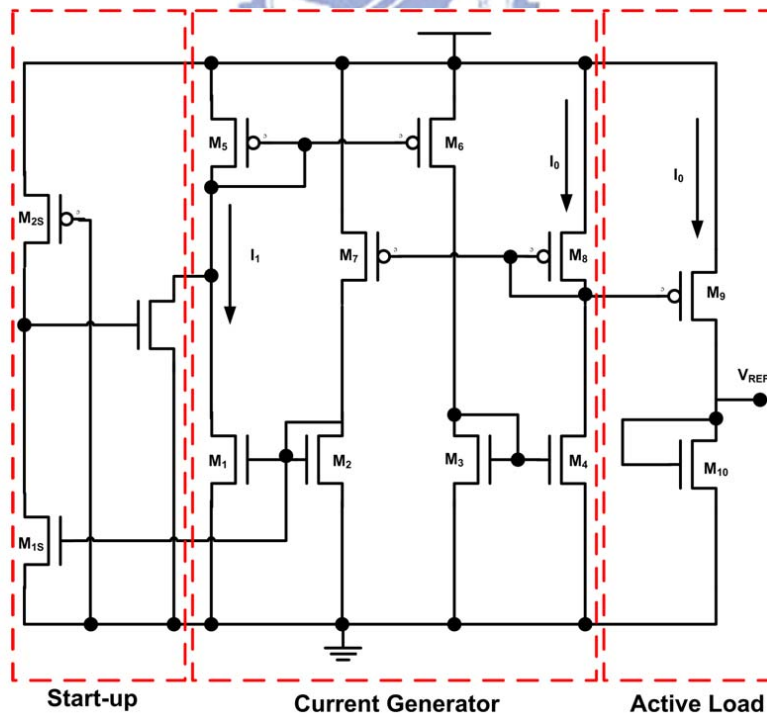
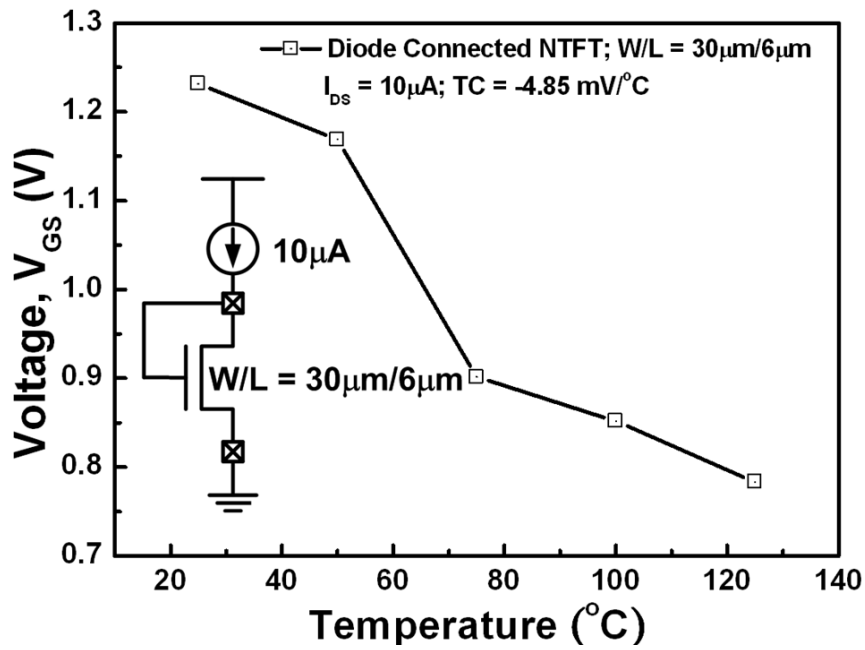
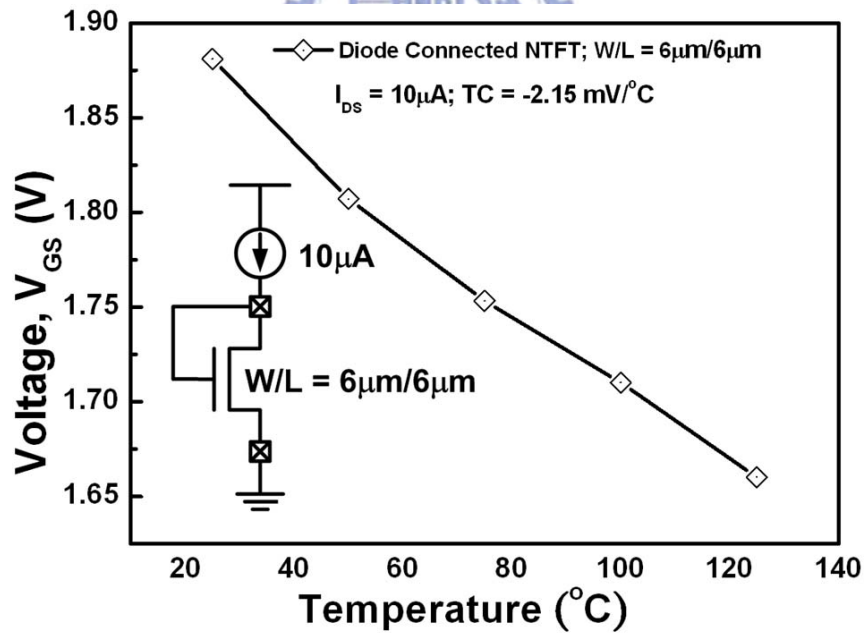


Fig.4.2 The bandgap reference circuit based on subthreshold MOSFETs.



(a)



(b)

Fig. 4.3. The comparison on temperature coefficient (TC) of diode-connected TFTs under a constant drain current of  $10\mu\text{A}$  with (a) channel width of  $6\mu\text{m}$ , and (b) channel width of  $30\mu\text{m}$  in LTPS process.

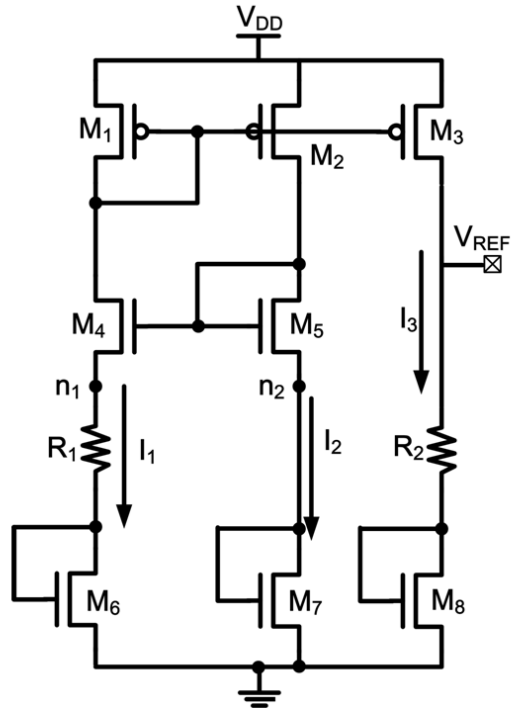


Fig. 4.4 The implementation of the new proposed bandgap reference in a 3- $\mu\text{m}$  LTPS process

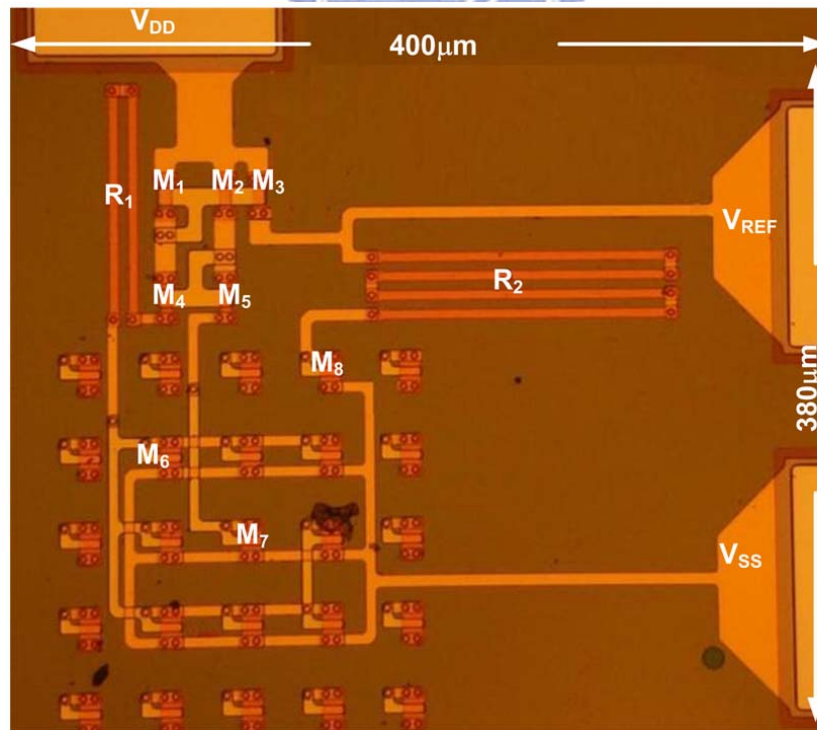


Fig. 4.5. The chip photo with PAD of the new proposed voltage reference circuit with temperature compensation fabricated in a 3- $\mu\text{m}$  LTPS process.

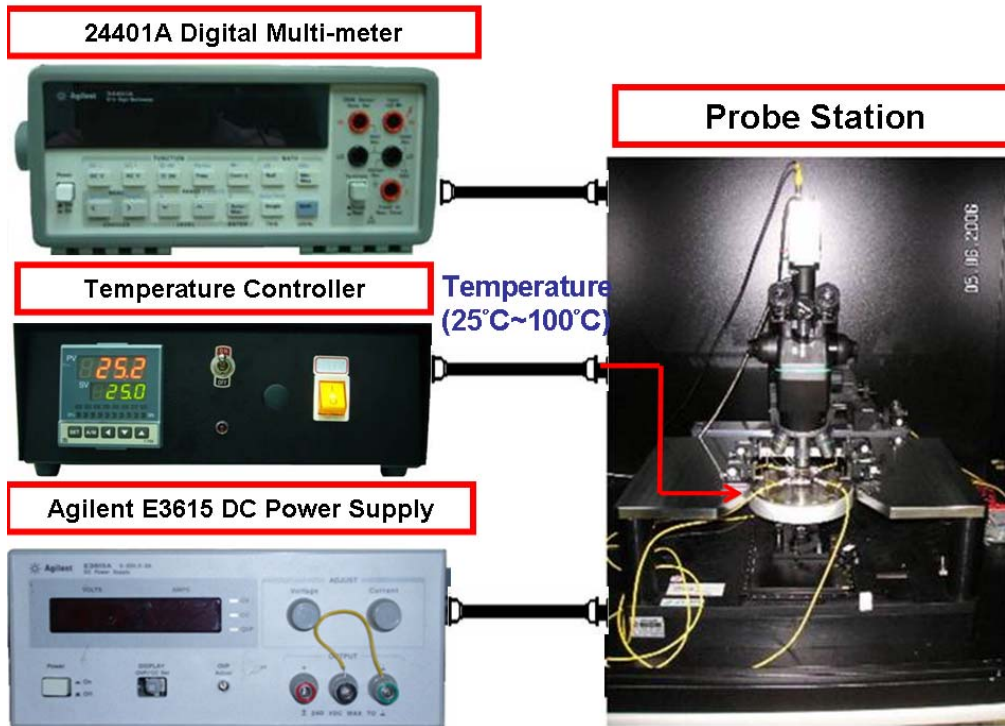


Fig. 4.6 The measurement setup of the voltage reference circuit with temperature compensation in the 3- $\mu\text{m}$  LTPS process.

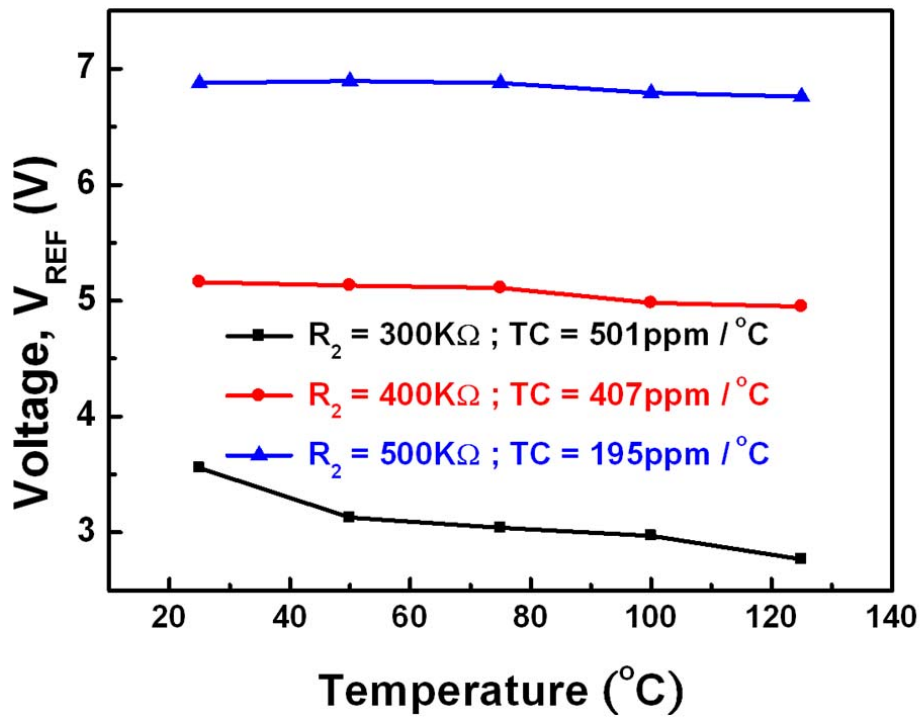
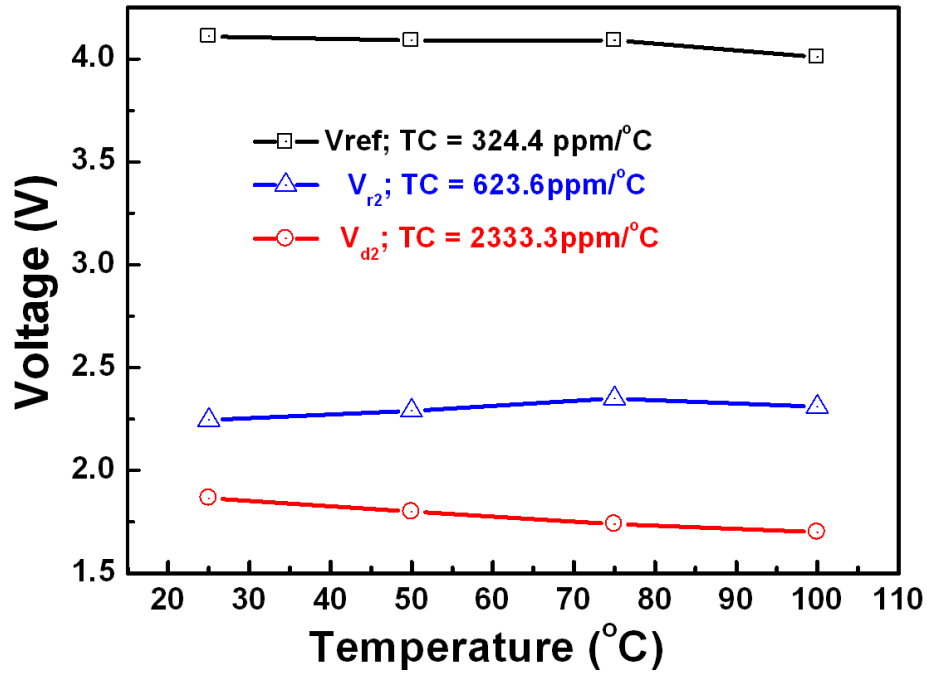
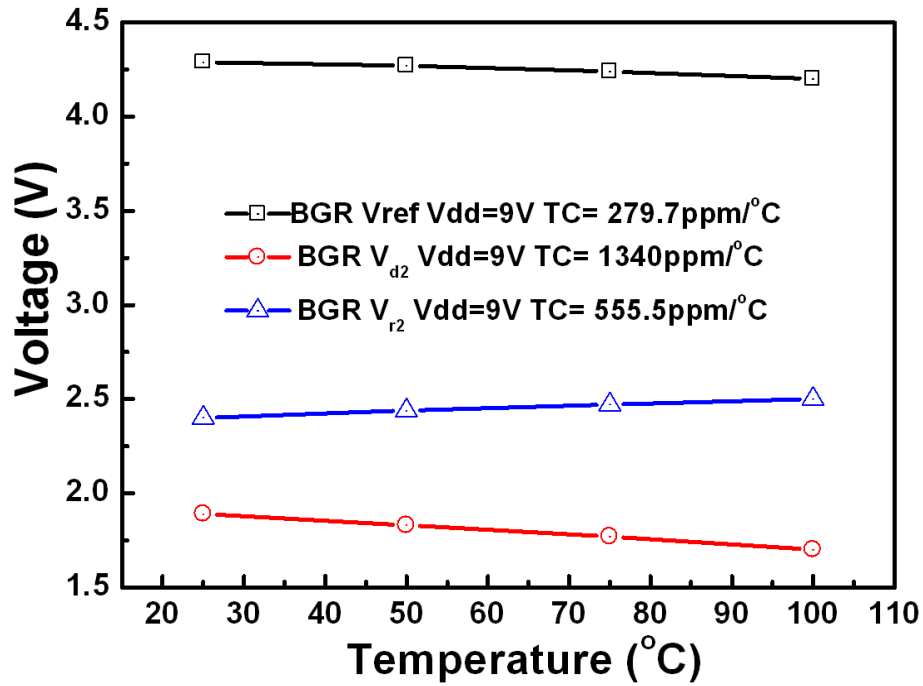
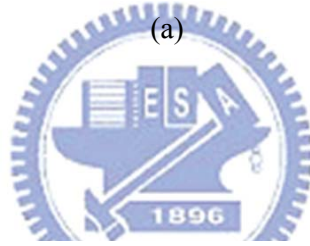


Fig. 4.7 The measurement results of the novel voltage reference circuit with temperature compensation with different resistance in the 3- $\mu\text{m}$  LTPS process.

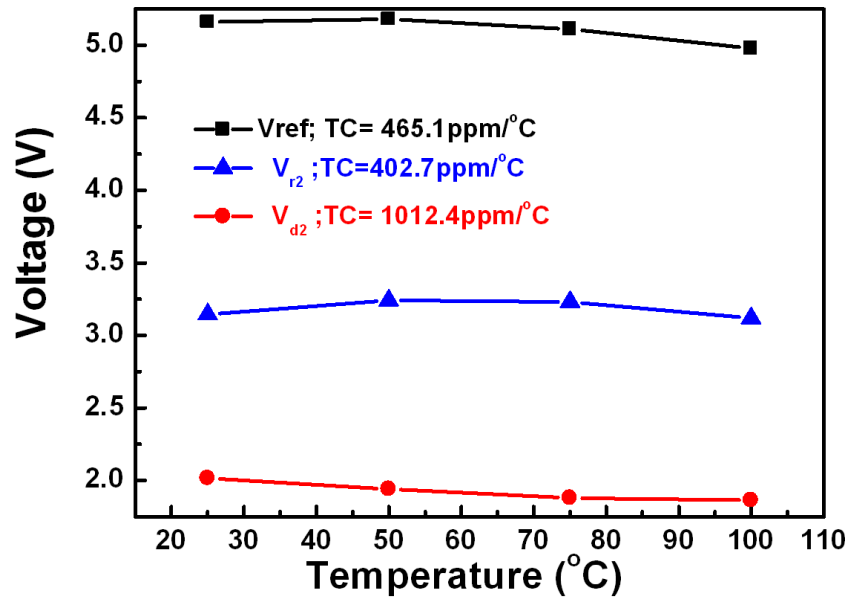




(a)

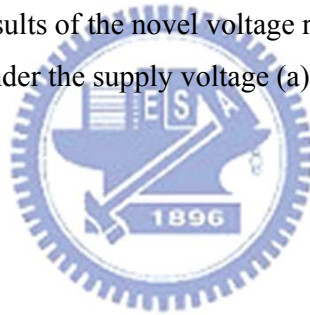


(b)



(c)

Fig. 4.8 The measurement results of the novel voltage reference circuit with temperature compensation under the supply voltage (a) 8V, (b) 9V, and (c) 10V in the 3- $\mu$ m LTPS process.



# Chapter 5

## Conclusion

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### 5.1 CONCLUSION

The temperature coefficient of TFT devices in LTPS technology is strongly dependent on the activation energy of the devices. With a suitable control, higher activation energy gives rise to higher absolute value of the temperature coefficient. The influence of the laser energy density in ELA process on the temperature coefficient of the devices is not significant. On the other hand, the bias current level and the channel width have a strong impact on the device temperature coefficient. As a result, the temperature coefficient of devices can be controlled by regulating the channel width of the devices. With an appropriate circuit design, a positive temperature coefficient can be generated by using the voltage drop between devices those have different temperature coefficients (different channel widths). Then, the positive temperature coefficient can be used to compensate the negative temperature coefficient from the devices.

The first voltage reference circuit with temperature compensation has been successfully verified without any trimming procedure in a 3- $\mu\text{m}$  LTPS process. The measured reference output voltage is 6.87 V with a temperature coefficient of 195 ppm/ $^{\circ}\text{C}$ . The proposed voltage reference circuit with temperature compensation consumes an operating current of only 8.97  $\mu\text{A}$  under the supply voltage of 10 V on glass substrate. This new voltage reference circuit with temperature compensation can

be used to realize precise analog circuits in LTPS process for System-on-Glass (SoG) applications.

#### **4.4. FUTURE WORKS**

##### ***5.2.1 VOLTAGE REFERENCE CIRCUIT WITH TEMPERATURE AND PSRR COMPENSATION***

For precise analog circuits design, reference voltage variation is the most careful consideration. Power-supply rejection ratio (PSRR) which is the common indicator can be expressed as [24]-[27]

$$PSRR = \frac{\Delta V_{REF}}{\Delta V_{DD}}, \quad (5-1)$$

where ( $\Delta V_{REF}$ ) and ( $\Delta V_{DD}$ ) are the output voltage variation and supply voltage variation individually. To consider about the PSRR of the voltage reference circuit with temperature compensation, the measurement results are shown in Fig.5.1. However, as the result shows, the PSRR is pretty high for the proposed voltage reference circuit with temperature compensation. The critical point is that the structure for reducing PSRR had not been considered in proposed circuit yet. Hence, the common reference voltage circuits with temperature compensation for reducing PSRR are shown in Fig. 5.1. Fig. 5.1(a) makes use of the feedback technology by using OP amplifier, and the cascade structure is also applied to reduce PSRR.

##### ***5.2.2 VOLTAGE REFERENCE CIRCUIT WITH TEMPERATURE COMPENSATION BY USING DIFFERENT TEMPERATURE COEFFICIENT***

From the analysis of TC for LTPS devices in chapter 3, there exist differences between different devices. Hence, the novel voltage reference circuit with

temperature compensation which is shown in Fig.5.3 has been proposed by using the concept of different temperature coefficient. The output Therefore, the output voltage variation of the new proposed voltage reference circuit with temperature compensation can be expressed as

$$V_{REF} = I_3 R_2 + V_{D2} = \frac{R_2}{R_1} V_{R1} + V_{D2}, \quad (5-2)$$

where the first item in Eq. (5-2) is proportional to the absolute temperature (PTAT), which is used to compensate the negative temperature coefficient of  $V_{D2}$ . The concept to design the positive temperature coefficient is shown in Fig. 5.4. The difference of TC between different LTPS devices can be designed to the PTAT terms for the voltage reference circuit with temperature compensation.



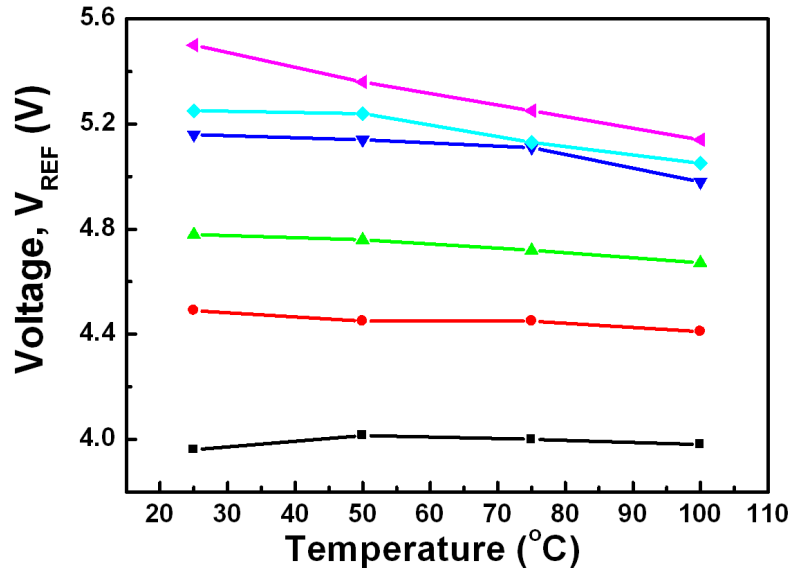
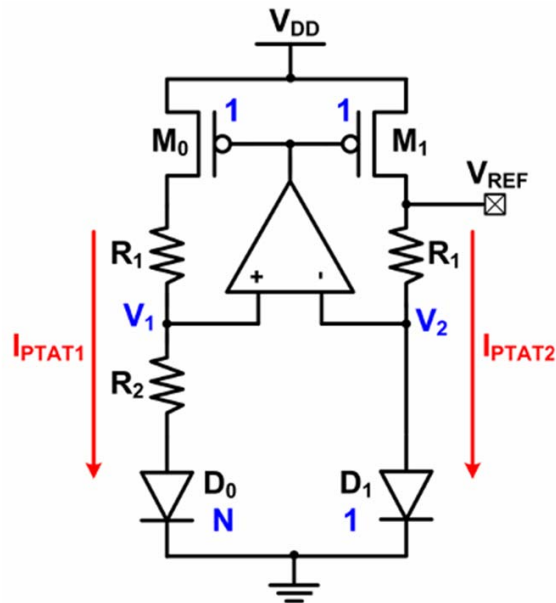


Fig. 5.1. The measurement results of the voltage reference circuit with temperature compensation in the 3- $\mu\text{m}$  LTPS process.



(a)

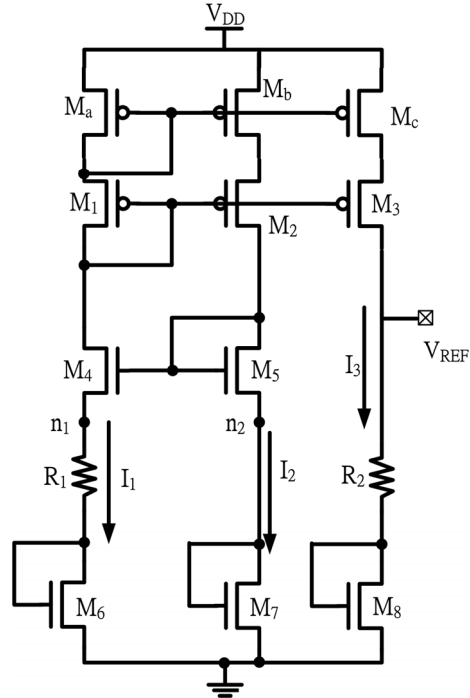


Fig.5.2 (a)The voltage reference circuit with temperature and PSRR compensation in CMOS technology with OP Amplifier, (b) with cascade structure.

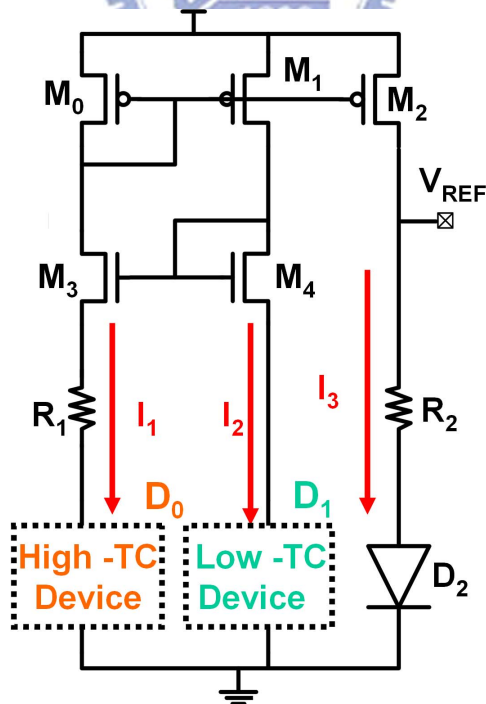
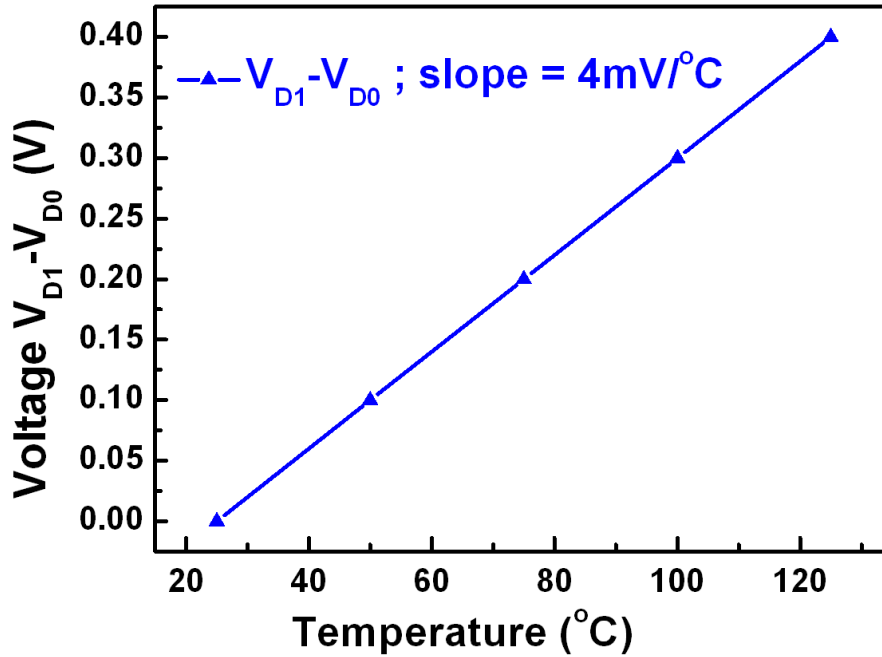
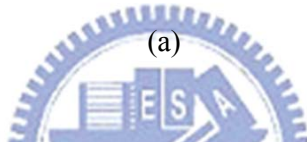
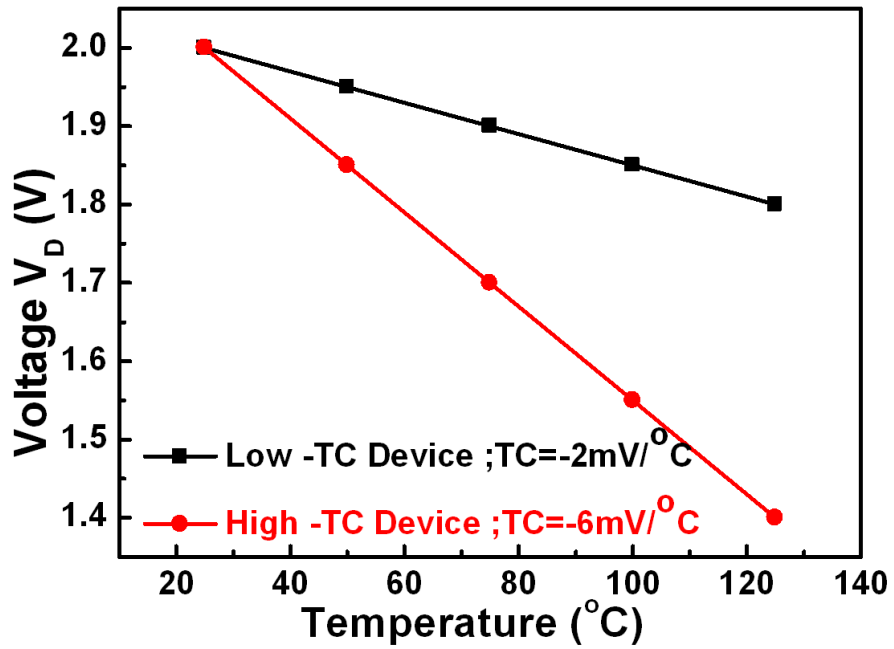


Fig.5.3 (a)The novel voltage reference circuit with temperature compensation in LTPS technology with OP Amplifier, (b) with cascade structure.



(b)

Fig.5.4 (a)The voltage reference circuit with temperature compensation in CMOS technology with OP Amplifier, (b) with cascade structure.



# Appendix

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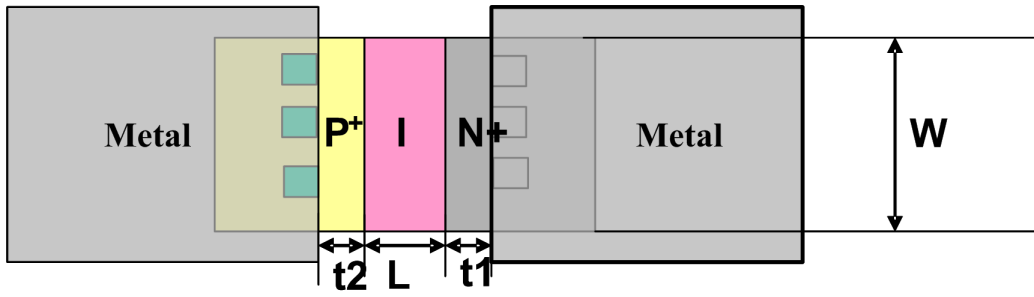
## A.1. P-I-N DIODE

### A.1.1. DEVICE FABRICATION

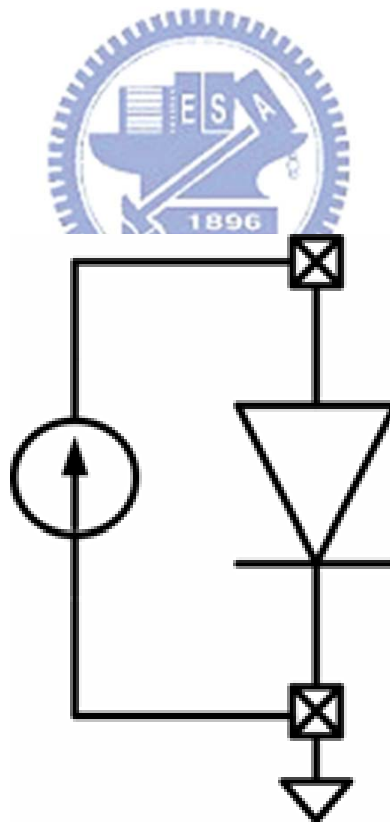
A PiN diode is a diode with a wide, lightly doped 'near' intrinsic semiconductor region between a p-type semiconductor and an n-type semiconductor region. The p-type and n-type regions are typically heavily doped because they are used for ohmic contacts. The wide intrinsic region is in contrast to an ordinary PN diode. The wide intrinsic region makes the PIN diode an inferior rectifier (the normal function of a diode), but it makes the PIN diode suitable for attenuators, fast switches, photo-detectors, and high voltage power electronics applications. The structure of PIN diode is shown in Fig.A.1. (a)., and  $t_1 = t_2 = 2\mu\text{m}$ .

### A.1.2. Measurement Result

First, the measurement of the TC of LTPS PIN diodes with channel width changing of  $50\mu\text{m}$ ,  $100\mu\text{m}$ ,  $150\mu\text{m}$ ,  $200\mu\text{m}$ , and  $400\mu\text{m}$  are performed by changing the temperature from  $25^\circ\text{C}$  to  $125^\circ\text{C}$ . Under a constant driving current of  $1\mu\text{A}$ , the  $V_D$  as a function of temperature is plotted in Fig. A. 2(a). It can be observed that when temperature increases from  $25^\circ\text{C}$  to  $125^\circ\text{C}$ , the  $V_{GS}$  varies from  $1.98\text{ V}$  to  $1.65\text{ V}$ . In the same way, under a constant driving current of  $10\mu\text{A}$ , the  $V_D$  as a function of temperature is plotted in Fig. A. 2(b). As temperature changes from  $25^\circ\text{C}$  to  $125^\circ\text{C}$ , the  $V_{GS}$  decreases from  $2.23\text{V}$  to  $1.5\text{V}$ , significantly. The relationship between channel width and temperature is not pretty significant for LTPS PIN diodes.

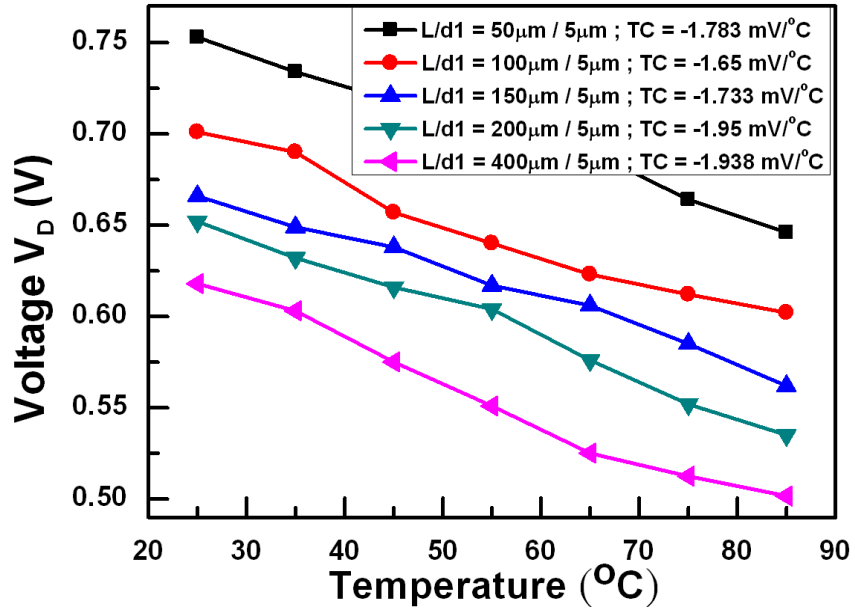


(a)

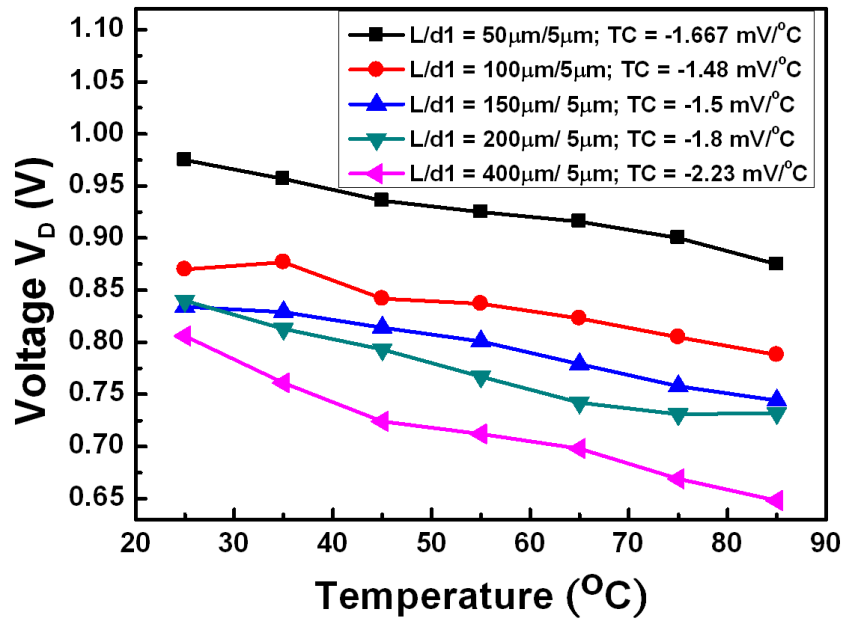


(b)

Fig. A.1. (a)The structure of PIN diode device, and (b) the setup to measure voltage  $V_D$  under the bias of  $I_D$ .

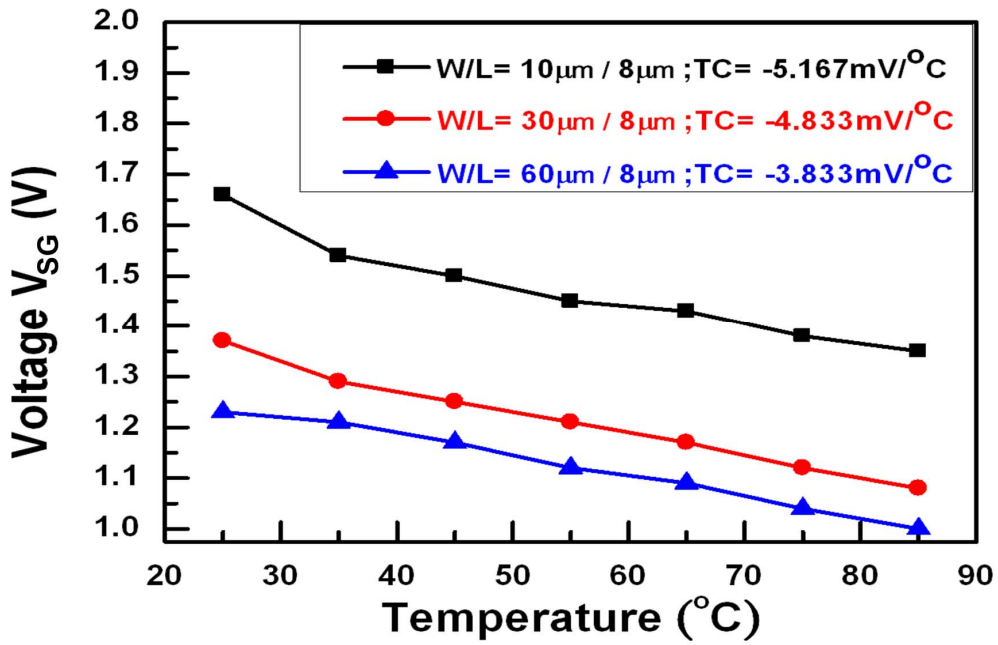


(a)

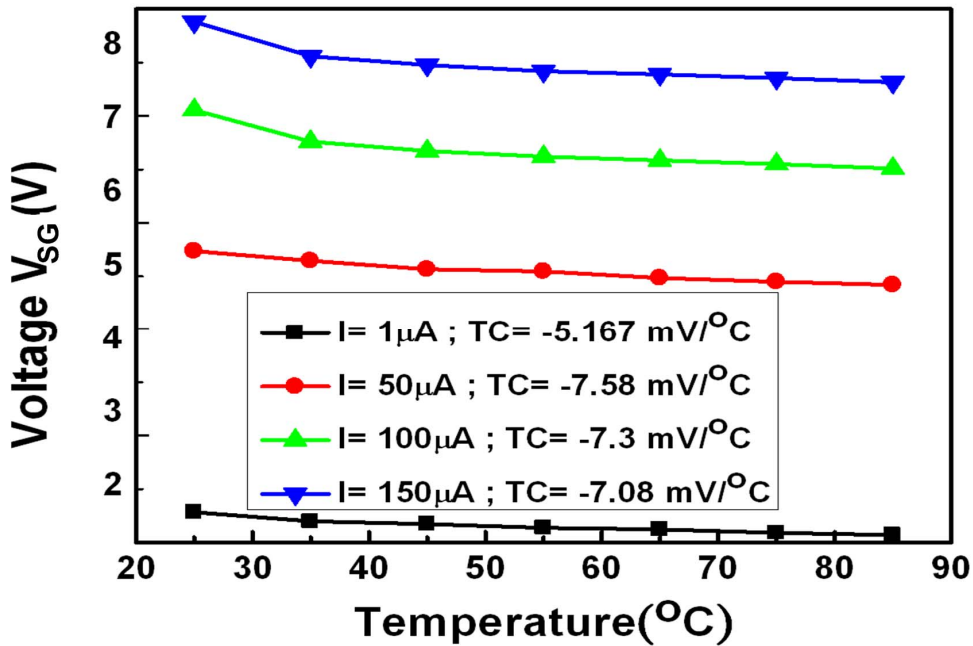


(b)

Fig. A.2. (a) The relationship between  $V_D$  and temperature with the identical current ( $I_D = 1 \mu\text{A}$ ) and (b) ( $I_D = 10 \mu\text{A}$ ).



(a)



(b)

Fig. A.3. (a) The relationship between  $V_{SG}$  and temperature under identical  $I_{DS}$  (b) with the same device dimension of the diode-connected PTFT device.

## REFERENCES

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- [1] H. G. Yang, S. Fluxman, C. Reita, and P. Migliorato, "Design, measurement and analysis of CMOS polysilicon TFT operational amplifiers," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 727–732, Jun. 1994.
- [2] T. Matsuo and T. Muramatsu, "CG silicon technology and development of system on panel," in *SID Tech. Dig.*, 2004, pp. 856–859.
- [3] Y. Nakajima, Y. Kida, M. Murase, Y. Toyoshima, and Y. Maki, "Latest development of "System-on-Glass" display with low temperature poly-Si TFT," *SID, Dig. Tech. Papers, 2004*, vol. 21, No. 3, pp. 864–86.
- [4] Y. Nakajima, "Ultra-low-power LTPS TFT-LCD technology using a multi-bit pixel memory circuit," in *SID Tech. Dig.*, 2006, pp. 1185–1188.
- [5] M. Jacunski, M. Shur, A. Owusu, T. Ytterdal, M. Hack, and B. Iniguez, "A short-channel DC spice model for polysilicon thin-film transistors including temperature effects," *IEEE Trans. Electron devices*, vol. 46, no. 6, pp. 1158-1146, Jun. 1999.
- [6] A. Hatzopoulos, D. Tassis, N. Hastas, C. Dimitriadis, and G. Kamarinos, "On-state drain current modeling of large-grain poly-Si TFTs based on carrier transport through latitudinal and longitudinal grain boundaries," *IEEE Trans. Electron Devices*, vol. 52, no. 8, pp. 1727-1733, Aug. 2005.
- [7] K.-N. Leung and K.-T. Mok, "A sub-1-V 15-ppm/<sup>o</sup>C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526-530, Apr. 2002.
- [8] K.-N. Leung, K.-T. Mok, and C.-Y. Leung, "A 2-V 23- $\mu$ A 5.3-ppm/<sup>o</sup>C curvature-compensated CMOS bandgap voltage reference," *IEEE J. Solid-State*

*Circuits*, vol. 38, no. 3, pp. 561-564, Mar. 2003.

- [9] G. Vita and G. Iannaccone, "A sub-1-V, 10-ppm/ $^{\circ}$ C, nanopower voltage reference generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 7, pp. 1536-1542, July 2007.
- [10] M.-D. Ker and J.-S. Chen, "New curvature-compensation technique for CMOS bandgap voltage reference with sub-1-V operation," *IEEE Trans. Circuits and Systems II: Express Briefs*, vol. 53, no. 8, pp. 667-671, Aug. 2006.
- [11] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," in *MRS Bulletin*, pp. 881-886, Nov. 2002.
- [12] B. Lee, Y. Hirayama, Y. Kubota, S. Imai, A. Imaya, M. Katayama, K. Kato, A. Ishikawa, T. Ikeda, Y. Kurokawa, T. Ozaki, K. Mutaguch, and S. Yamazaki, "A CPU on a glass substrate using CG-silicon TFTs," *Tech. Dig. of IEEE International Solid-State Circuit (ISSCC)*, 2003, vol. 9, No. 4, Feb. 2003.
- [13] T. Nishibe and H. Nakamura, "Value-added circuit and function integration for SOG (System-on-Glass) based on LTPS technology," *SID, Dig. Tech. Papers*, 2006, vol. 16, No. 4, pp. 1091-1094.
- [14] K. Sera, F. Okumara, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, "High-performance TFTs fabricated by XeCl excimer laser annealing of hydrogenated amorphous-silicon film," *IEEE Trans. Electron Devices*, vol. 36, pp. 2868-2872, Dec. 1989.
- [15] K. Pangal, J. C. Sturm, and S. Wagner, "Hydrogen plasma-enhanced crystallization of amorphous silicon for low-temperature polycrystalline silicon TFT's," in *IEDM Tech. Dig.*, 1998, pp. 261-264.
- [16] K.T. Mok and K.-N. Leung, "Design considerations of recent advanced low-voltage low-temperature-coefficient CMOS bandgap voltage reference," *Proc. of IEEE Custom Integrated Circuits Conf. (CICC)*, Sept. 2008, pp. 635-642.

- [17] A.P. Brokaw, "A simple three-terminal IC bandgap reference," *IEEE Journal of Solid-State Circuits*, vol. SC-9, pp. 388-393, Dec. 1974.
- [18] K.E. Kuijk, "A precision voltage source," *IEEE Journal of Solid-State Circuits*, vol. SC-8, pp. 222-226, Jun. 1973
- [19] K. Mourgues, A. Rahal, T. Mohammed-Brahim, M. Sarret, J. P. Kleider, C. Longeaud, A. Bachroui, and A. Romano-rodriguez, "Density of states in the channel material of low temperature polycrystalline silicon thin film transistors," *J. Non Crystalline Solids*, pp. 1279-1283, 2000.
- [20] Yue Kuo, *Thin Film Transistors: Materials and Processes*, Kluwer Academic Publishers, vol. 2, pp. 35-38, 2004.
- [21] G. Rinconmora, *Voltage Reference from Diodes to Precision High-Order Bandgap Circuits*, Wiley Publishers, pp. 23-28, 2002.
- [22] R.J. Widlar, "New developments in IC voltage regulators," *IEEE Journal of Solid-State Circuits*, vol. SC-16, pp. 2-7, Feb. 1971.
- [23] G. De Vita and G. Iannaccone, "A 300nW, 12ppm/°C voltage reference in a digital 0.35µm CMOS process" *Dig. of VLSI Circuits* , vol. 26, pp. 51-54, Jan. 2006.
- [24] P. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th Edition, Wiley, 2001.
- [25] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, New York: Oxford University Press, 2002.
- [26] Y.-H. Tai, *Design and Operation of TFT-LCD Panels*, Wu-Nan Book, Inc., Apr. 2006.
- [27] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill Companies, Inc., 2001.

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# PUBLICATION LIST

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- [1] **T.-C. Lu**, H.-W. Zan, and M.-D. Ker, "Temperature coefficient of poly-Si TFT and its application voltage reference with temperature compensation in LTPS process," *IEEE Trans. Electron Devices*, in press, 2008.
- [2] **T.-C. Lu**, M.-D. Ker, H.-W. Zan, C-H Kuo, C.-H. Li, Y.-J. Hsieh, and C.-T. Liu, "Design of Bandgap Reference Circuit with all TFT Devices on Glass Substrate in a 3- $\mu$ m LTPS Process," *IEEE Custom Integrated Circuits Conf. (CICC)*, 2008, in press.
- [3] **T.-C. Lu**, H.-W. Zan, M.-D. Ker, W.-M. Huang, K.-C. Lin, C.-C. Shih, C.-C. Chiu, and C.-T. Liu, "Temperature coefficient of diode connected LTPS poly-Si TFT and its application on the bandgap reference circuit," in *SID Tech. Dig.*, Los Angeles, California, USA, May 18-23, 2008, pp. 1410-1413.
- [4] **T.-C. Lu**, M.-D. Ker, H.-W. Zan, C-H Kuo, C.-H. Li, Y.-J. Hsieh, and C.-T. Liu, "On glass bandgap reference circuit in a 3- $\mu$ m LTPS process," *Dig. of Active Matrix Flatpanel Displays and Devices (AMFPD)*, Tokyo, Japan, Jul. 2-4, 2008, pp. 201-204.
- [5] **T.-C. Lu**, H.-W. Zan, M.-D. Ker, C-H Kuo, C.-H. Li, Y.-J. Hsieh, and C.-T. Liu, "Realization of on-glass bandgap reference circuit with all TFT devices in a 3- $\mu$ m LTPS Process," *Proc. of Taiwan Display Conf.*, Taiwan, June 11-12, 2008, pp.181-184.
- [6] M.-D. Ker, H.-W. Zan, and **T.-C. Lu**, "Liquid crystal display apparatus and bandgap reference circuit," CHN, US, and ROC patent pending.