高效能互補式金氧半導體影像偵測讀出裝置積體電路設計

The Design of High Performance CMOS Image Sensors and Readout Circuits

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ABSTRACT (CHINESE)

影像在人們的生活中，扮演著不可或缺的腳色，舉凡照相機，攝影機以及人造衛星…等，都需要用到影像偵測裝置，隨著科技的進步，人類對於高品質影像的渴望與需求，日與俱增。由於金氧半導體上的影像偵測裝置是用標準半導體製程製作，可以將整個系統整合在同一個晶片上，達到縮小體積，節省成本等優點。在我的論文中研究高效能的互補式金氧半導體影像偵測裝置，主要分成了兩個部份: (1) 互補式金氧半導體電壓傳輸方式的影像偵測裝置(2) 新型互補式金氧半導體電流傳輸方式的影像偵測裝置。

針對互補式金氧半導體電壓傳輸方式的影像偵測裝置，我們對其架構進行了分析，設計以及最佳化。其具有高線性度，低固定圖像雜訊(FPN)等特色，並且實現在 TSMC 0.18 微米的半導體製程上。

在互補式金氧半導體電流傳輸方式的影像偵測裝置部份，我們提出了新型的互補式金氧半導體電流傳輸方式的影像偵測裝置。提出的電路具有高線性度，低功率消耗，可調節的多重增益，寬廣的輸入動態範圍以及相關多重取樣技術(CDS)等特色。多重增益的架構提升了輸入的訊號範圍。利用了簡單而且準確的前級可調節增益的架構來改善訊號雜訊比(SNR)。最後我們利用了 TSMC 0.18 微米的半導體製程將其實現。

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ABSTRACT (ENGLISH)

Image has been played an important role in daily lives recently, like the camera, the video camera, the artificial satellite and so on. The requirement of the high quality image is getting increasing with the advancement of the technology. Due to the usage of the standard CMOS process technology, the CMOS image sensor system can be integrated on a single chip, it can achieve small area and low cost. In my thesis research for high performance image sensor, the main parts of this thesis include: (1) voltage mode CMOS image sensor; (2) new current mode CMOS image sensor.

In the voltage mode CMOS image sensor, we analysis, design and optimize the architecture. The implemented voltage mode sensor features high linearity and low fixed pattern noise. The voltage mode sensor is implemented with TSMC 0.18 um process.

In the current modes CMOS image sensor, we propose a new linear current mode image sensor. The proposed circuit features high linearity, low power consumption, programmable multiple gain stages, wide input swing and correlated

double sampling (CDS) technology. The signal swing of the linear current mode sensor is enhanced by the proposed multiple gain readout structure. A simple and accurate front-end programmable gain structure is proposed to improve the signal-to-noise ratio (SNR) with low power consumption. The current mode sensor is implemented with TSMC 0.18um process.

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春花秋月何時了，花落知多少

碩士生涯過的真的很快，一轉眼就是快三年了，感覺很像一場夢，有種人生如戲的感覺，還記得碩一剛進來什麼都不懂的樣子，現在已經是實驗室中的老人了，一切彷彿都還在昨天。在碩士生涯的求學過程中，首先感謝吳重雨校長不辭辛苦的指導，雖然老師平日校長事務繁重，但是對於學生的指導和學習依然非常的重視，令學生們感佩在心。

謝志成老師，雖然跟老師只有相處一年多，但是對老師內心充滿無限的感激以及尊敬。老師平日以身做則，研究正面的態度，無形中令生性怠惰的我受到老師的感化也變的認真。而且老師耐心的指導，親自教導量測晶片都令人印象深刻，由衷的感佩。

在學習的過程中，感謝國家晶片中心的邱進峰副主任以及台南 CIC 的大力幫忙，讓研究能夠順利。

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感謝兩年多來陪伴著我的夥伴好友們，讓我兩年多來每天都過的很開心，坐在我旁邊兩年的好友北鴨，不管什麼大小事情總是會幫忙我;說好的 360 夠義氣的小州哥;正人君子阿邦哥，總是會介紹美食好玩的給大家;戰神建名，一起摸魚的好伙伴;喜歡白爛最猥褻的馬及示範;正直熱心助人的紹岐;還有一起做研究的大家萬謎、大仔、宗恩、天才嘴砲塔哥、歐陽、國維、區文。另外感謝陪伴我三年的同學和學弟們，讓我碩三的生活不孤單，一樣開心，喜歡扯我後腿兼戰友未來同事的科科;宅中之霸兼戰隊副隊長的戰友宅宅;一起敗家月圓人團圓的蕉哥 low 昀;喜歡開黃槍人前人後兩個樣的林良;負隊長星野獸;天哥，Kitty、阿黛爾、彥偉、叔叔、溫董、佳琪、筱妊、怡歆、哲綸，實驗室的氣氛總是很歡樂，很高興認識大家。

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論文雖然力求完善，但謬誤之處在所難免，尚祈各位讀者不吝惜賜予寶貴意見，使本論文能更加完善。

陳　威　宇

謹 致　於　交大竹塹 **己 丑** 春

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Chapter 1
Introduction

1.1 Background

The earliest solid-state image sensors with the bipolar and MOS photodiode arrays were invented by Westinghouse, IBM, Plessy, and Fairchild in the late 1960s. The CCD devices were invented at Bell Laboratory in 1970, and they immediately became the major image devices in the market [1]. Due to the poor performance and large pixel size (for that time) relative to that of the CCD, since the CCD was invented, the CMOS sensor cannot compete with the CCD completely. Therefore, in the early days, the major image technology is Charge-Couple Devices (CCD). The CCD has many advantages, like low noise and high sensitivity. Besides, the circuit architecture of CCD is simple, and the major operation principle is charge transfer. Therefore, the CCD is still be used in many image application generally today. Until the early 1990s, after the invention of passive pixel sensor (PPS) as shown in Fig. 1.1, the CMOS image sensor was used in the low-end machine vision application [2]. The big push for the development of CMOS sensors came from the introduction of Active Pixel Sensors (APS) in the early ‘90s as shown in Fig. 1.2[3, 4, 5]. It was quickly realized that adding an amplifier to each pixel significantly increases sensor speed and improves its signal-to-noise ratio (SNR), thus overcoming the shortcomings of PPS [6]. Recently, the research has been focusing, mainly, on the improvement of the APS, because APS is the pixel circuit that has shown better performance and flexibility[7].

In order to strongly compete with CCD technology, the aim of researchers has been to obtain higher performance imaging systems based on CMOS technology. Therefore, there have been several reports on improving the fill-factor (FF) with low power consumption, low voltage operation, low noise, high speed imaging and high dynamic range. After the invention of APS pixel, the performance of CMOS image sensor is increasing rapidly. Accompany with the appearance of 3T and 4T CMOS sensor pixel, CMOS image sensor is gradually replacing the CCD in the commercial and science market. Fig. 1.3 shows the readout circuits of CCD and CMOS sensor. Many of the difference between CMOS sensor and CCD arise from their difference in the readout architectures. The readout architecture of CCD is described as following: First, charge is shifted out of the array by vertical and horizontal CCD. Then, the charge is converted into voltage by the source follower, and serially read out. In the CMOS sensor, charge voltage signals are read out one row at a time in a manner similar to a random access memory using row and column select circuits. The advantages comparison of the CCD and CMOS is shown in table I.

The main Advantages of CMOS imagers are:

1. Low power consumption. Estimates of CMOS power consumption range from one-third to more than 100 times less than that of CCDs [8]. Besides, they work at low voltage. CMOS imagers only need one supply voltage, instead of CCDs, which need 3 or 4.

2. Lower cost compared to CCD's technology.

3. On chip functionality and compatibility with standard CMOS technology. CMOS imagers allow monolithical integration of readout and signal processing electronics.

In 2001, a study for Cross Contamination between CMOS Image Sensor and IC product showed no problems [9]. A sensor can integrate various signal and image processing blocks such as amplifiers, ADCs, circuits for colour processing and data compression, etc. on the same chip.

4. Miniaturisation, although important limitations exist, the level of integration is rather high [10].

5. Random access of image data.

6. Selective read-out mechanism [10,11]

7. High-speed imaging. The flexibility and the possibility to acquire images in a very short period of time [12].

8. To avoid blooming and smearing effects, which aretypical problems of CDD technology [13].

As outlined before, despite these advantages, there are still significant Disadvantages of CMOS image sensors compared to CCD technology. Therefore, these problems need to be solved so that CMOS image sensors can compete in any area.

These disadvantages are:

1. Sensitivity: The basic quality criterion for pixel sensitivity is the product of its Fill Factor and its Quantum Efficiency where Fill Factor is the ratio of light-sensitive area to the pixel's total size, and Quantum efficiency is the ratio of photon-generated electrons that the pixel captures to the photons incident on the pixel area. It must be pointed out that Active Pixel Sensors (APS) have reduced sensitivity to incident light, due to a limited Fill Factor, hence, less quantum efficiency.

2. Noise: CMOS Image sensors suffer from different noise sources which set the fundamental limits of their performance, especially under low illumination.

3. Dynamic range (DR): Dynamic Range, which is the ratio of the saturation signal to the rms noise floor of the sensor, is limited by the photosensitive-area size, integration time and noise floor.

4. Less image quality than CCD.

According to the advantages and advantages mentioned above, the research of CMOS image sensor mostly focus on the following directions: low noise, high dynamic range, high sensitivity and high fill factor, low power consumption, low voltage operation and high speed imaging. The overall architecture of CMOS image sensor is shown in Fig. 1.4.

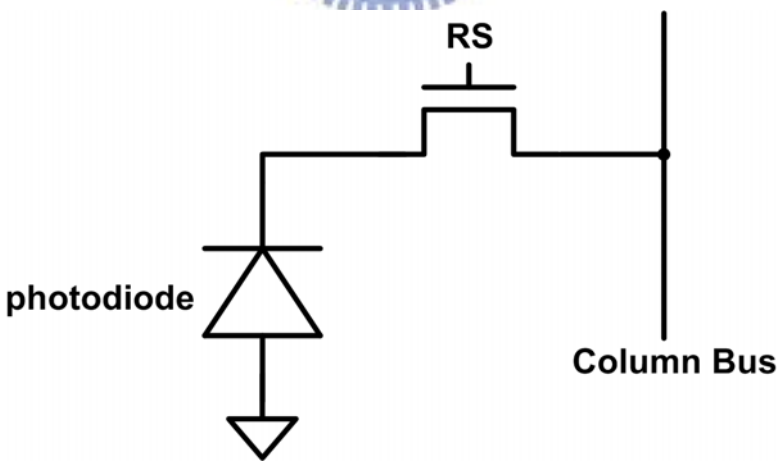


Figure 1.1 PPS schematic

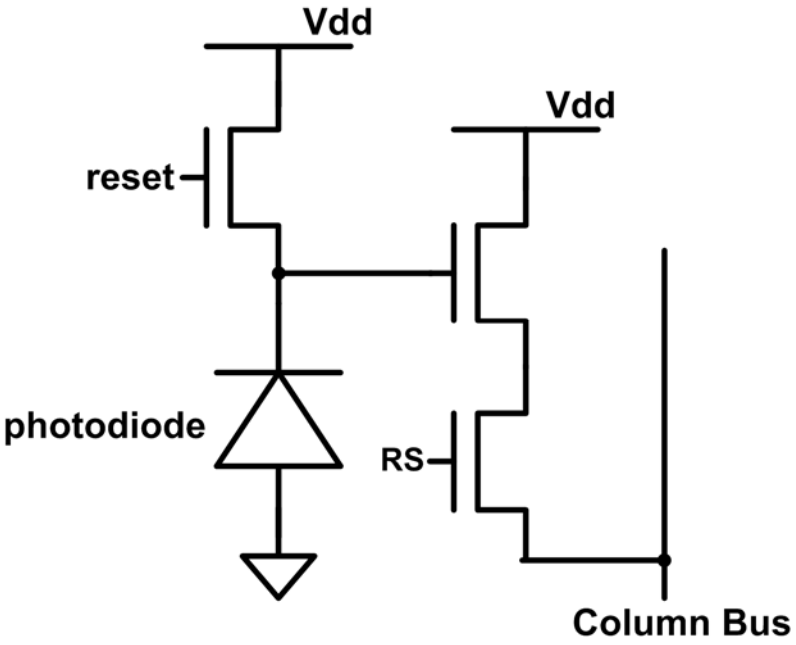


Figure 1.2 APS schematic

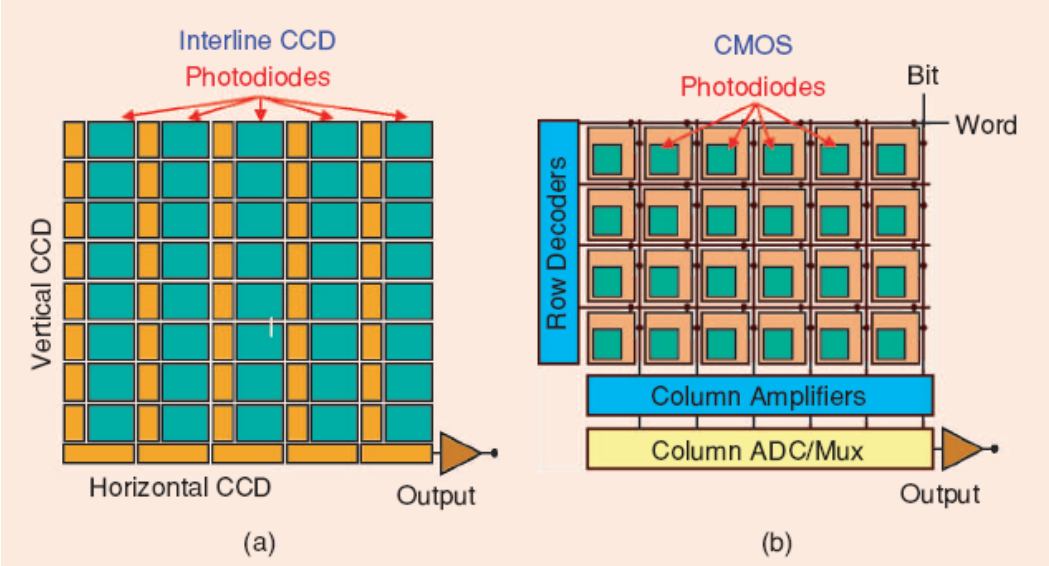


Figure 1.3 (a) readout architecture of CCD (b) readout architecture of CMOS sensor

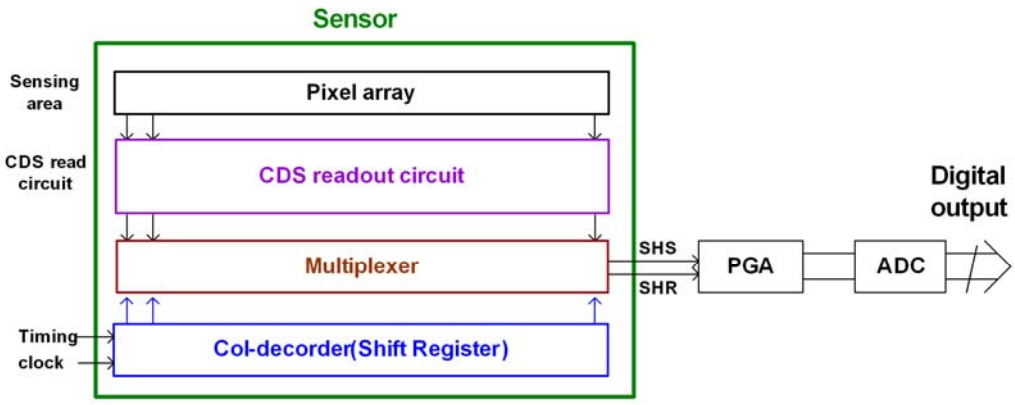
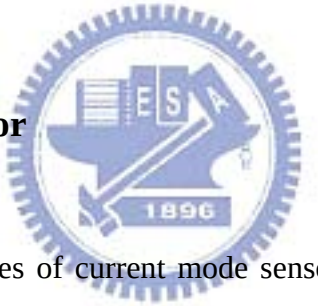


Figure 1.4 The overall architecture of CMOS image sensor

1.2 Review and motivation

1.2.1 Voltage mode sensor

In traditional, the voltage mode sensor usually uses the source follower as the active device. The source follower has worse linearity and worse fixed pattern noise due to the body effect. Since the disadvantages mentioned before, we want to use the operational amplifier to replace the source follower active device to get better linearity and fixed pattern noise. On the other hand, in order to design a CMOS sensor readout circuit for space satellite applications, the voltage mode sensor would be design as 1-D array.



1.2.2 Current mode sensor

The traditional advantages of current mode sensor includes that the arithmetic operation can be easily implemented and that the design complexity of back-end ADC can be reduced. Due to the current operation, the current mode sensor usually has the dc current; this would increases the power consumption. On the other hand, most of sensors need the programmable gain amplifier (PGA) to enhance the low light performance. The PGA block would consume extra power and increase the chip area. Therefore, in order to replace the PGA block, we proposed the new current mode circuit architecture with high programmable gain and no dc current. The sensitivity performance in the low light is also be enhanced.

1.3 Thesis Organization

Chapter1 introduces the background and the review of the CMOS sensor, including the history of CCD and CMOS sensors. The advantages of CMOS sensor is also described in the section 1.1. Besides, the motivation is introduced in section 1.2. The section 1.3 introduces the thesis organization.

In Chapter 2, the section 2.1 shows the architecture of voltage mode sensor and the readout circuit, and the analysis of the circuit is presented completely in detail. The 3T voltage mode sensor is be described in section 2.1.1, and the 4T voltage mode sensor is shown in section 2.1.2. The current mode sensor is proposed and analyzed in section 2.2. The section 2.3 shows the simulation results of voltage mode sensor and current mode sensor.

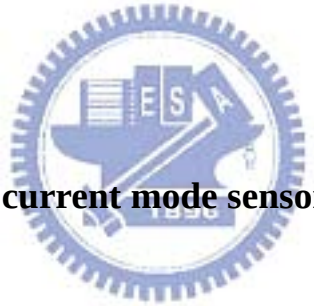
In Chapter 3, section 3.1 shows both the layouts of the current mode and the voltage mode sensors, including the 3T sensor pixel, the 4T sensor pixel, voltage mode sensor and the current mode sensor. Section 3.2 introduces the measurement environment, and the PCB designs of the voltage mode and current mode sensor are also shown. Section 3.3 shows the measurement results of voltage mode sensor and current mode sensor.

Finally, the conclusions and future work are summarized in Chapter 4.

1.4 Main results

1.4.1 Main results of the voltage mode sensor

The voltage mode sensor for space satellite applications have been designed and fabricated in 0.18-um CMOS 3T process. The pixel size of the voltage mode sensor is 6.5um, and the sensor array is 1x704 cells. The image system is implemented and sensing image results are shown. The voltage mode sensor achieves high linearity as 98.71%. The responsibility of the voltage mode sensor is 3.64 V/lux•s. By the CDS operation, the fixed pattern noise of the voltage modes sensor is -2.7%, +2.03% when the input optical power is 6.4251×10^{-2} mW/cm^2. The frame rate of the voltage mode sensor is 8000/sec.



1.4.2 Main results of the current mode sensor

The current mode sensor for space satellite applications have been designed and fabricated in 0.18-um CMOS 3T process. The pixel size of the current mode sensor is 6.5um, and the sensor array is 1x68 cells. By the CDS operation, the fixed pattern noise of the current modes sensor is -10.2%, +12.2% when the input optical power is 8.4127×10^{-2} mW/cm^2. The measured programmable gain is x1~x10 with gain linearity 99.59%. The current mode sensor operates with no dc path. The input signal swing of current mode sensor pixel is 2V.

CCD	CMOS
Lower noise	**High integration capability**
Higher sensitivity	**Low power consumption**
Lower dark current	**Lower cost**
Small pixel size	**Random access**
	High speed

Table I. The comparison of CMOS and CCD

Chapter 2
Circuit Design of CMOS Image Sensors

2.1 Architecture of CMOS voltage mode image sensor

In the following, the architectures of 3T voltage mode sensor and 4T voltage mode sensor would be described in detail.

2.1.1 Architecture of 3T voltage mode sensor

In general, 3T voltage mode sensor pixel is composed of a reset MOS (M_{reset}), a photodiode (sensor) and an active device (M_s) as shown in Fig. 2.1. The active device serves as a voltage buffer which enhances the driving capability of the photodiode output. The fixed pattern noise (FPN) induced by the threshold voltage (V_t) variation caused by active device M_s is found to be significant. In order to suppress the FPN, the threshold voltage must appear as the first order term in the output voltage equation which can be cancelled by the following correlated double sampling (CDS) operation. The source follower operation equation is shown as equation (2-1) and (2-2)

$$V_{out} = V_{pd} - V_{GS} \tag{2-1}$$

$$V_{out} = V_{pd} - \sqrt{\frac{2I}{K_n}} - V_t \tag{2-2}$$

As shown in equation (2-2), the V_t of M_s appears as the first order term in the source follower output. The threshold voltage term can be cancelled by sampling twice (Signal and Reset) and then subtraction, that is, correlated double sampling (CDS).

However, the V_t may encounter body effect due to the difference source voltage of the source follower. It would reduce the performance of the CDS technology. Moreover, the difference source voltage of the source follower would result channel length modulation and it would make some extra voltage error in the output.

The operation of the voltage mode sensor pixel is described as following. First, the V_{pd} is reset to $V_{resetin}$ by device M_{reset}. After a fixed integration period, V_{pd} would be discharged by the photocurrent of the photodiode and decreased from a high potential voltage to a low potential voltage. Then, the voltage of node V_{pd} would be transfer to V_{out} by the voltage buffer, the source follower implemented by M_s and current source, and then sampled in the following capacitor.

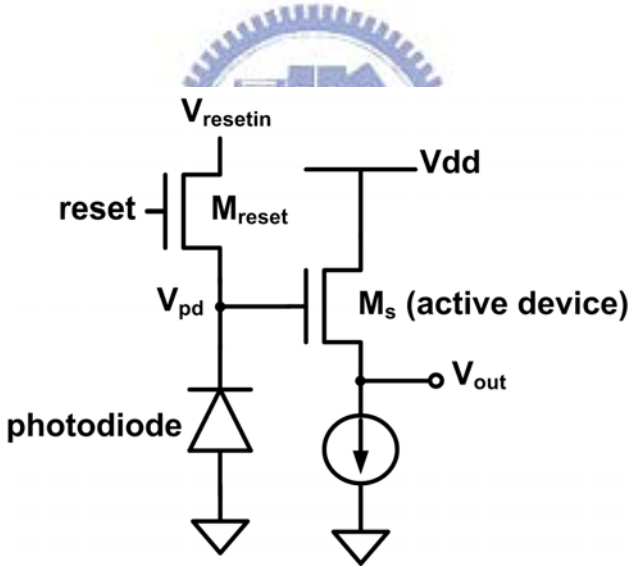


Figure 2.1 The general 3T voltage mode sensor pixel

The Fig. 2.2 shows another voltage mode pixel. It uses operation amplifier to replace the source follower as the voltage buffer, which is composed of a reset MOS (M_{reset}), a photodiode (sensor) and an operational amplifier (OP) with negative feedback as shown in Fig. 2.2. The operation equation of the amplifier in the Fig. 2.2 is shown as equation (2-3).

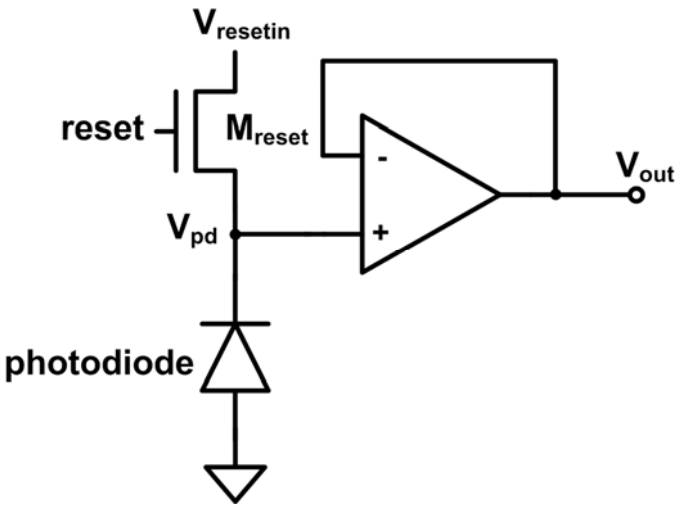


Figure 2.2 The voltage mode sensor pixel with OP

$$V_{out} = V_{pd} \tag{2-3}$$

Now let us analysis the two type voltage buffer. The gain of the source follower is shown in equation (2-4), and the unit gain buffer op is shown in equation (2-5).

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m}{g_m + g_{mb}} = 0.8 \sim 0.9 \quad (g_{mb} = 0.1 \sim 0.3 g_m) \tag{2-4}$$

$$\frac{V_{out}}{V_{in}} = \frac{A}{1+A} \approx 1 \quad (if \quad A = 10000) \tag{2-5}$$

As shown in the equations (2-4) and (2-5), the OP structure provides higher gain than the source follower, therefore, the linearity of the OP structure is much better than that of source follower. Besides, the OP structure is not suffered from the body effect and the channel length modulation. It can achieve a better performance with the CDS technology compared to the source follower structure. The disadvantage of the OP voltage buffer is the input offset voltage; however, it can also be removed by the CDS technology operation. The analysis of CDS operation and the comparison of the two types of voltage buffers would be shown in the following.

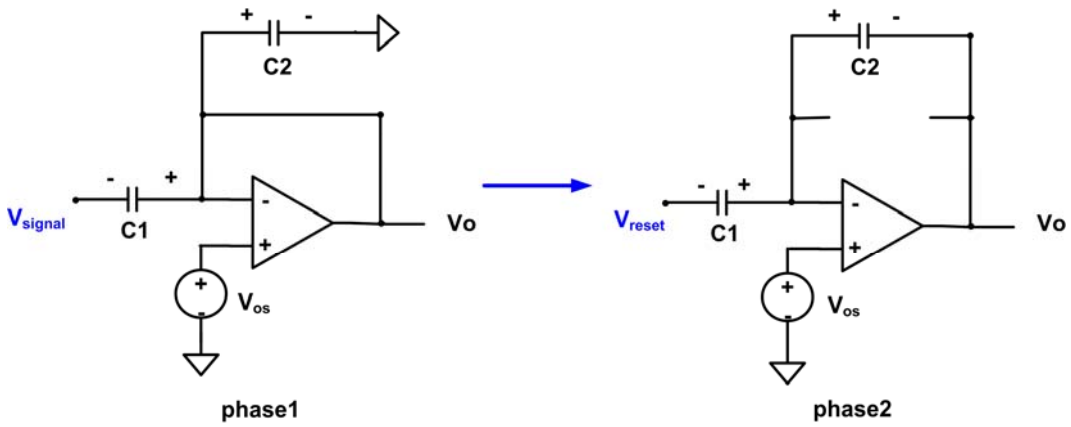


Figure 2.3 The general CDS operation circuit

$$V_o = (V_{sig} - V_{reset})\frac{C_2}{C_1} \tag{2-6}$$

Fig. 2.3 shows the general CDS operation circuit and equation (2-6) is the output function of the Fig 2.3. For the source follower voltage buffer, the CDS operation is described as following equations.

$$V_{signal} = V_i - V_{GS}(V_{t1}) \tag{2-7}$$

$$V_{reset} = V_{resetin} - V_{GS}(V_{t2}) \tag{2-8}$$

$$V_o = V_i - V_{GS}(V_{t1}) - V_{resetin} + V_{GS}(V_{t2}) \tag{2-9}$$

V_i : the voltage after integration

$V_{resetin}$: the reset voltage of the photodiode

$V_{GS}(V_{t1})$, $V_{GS}(V_{t2})$: the V_{GS} during difference body effect

From equations (2-7), (2-8), and (2-9), we can find that the V_t variation of the active device cannot be reduced completely due to the body effect in the source follower case. For the operation amplifier voltage buffer, the CDS operation is described as following equations.

$$V_{signal} = V_i - V_{os} \tag{2-10}$$

$$V_{reset} = V_{resetin} - V_{os} \tag{2-11}$$

$$V_o = V_i - V_{resetin} \tag{2-12}$$

From equations (2-10), (2-11) and (2-12), the OP structure as a voltage buffer shows a better performance in the CMOS voltage mode sensor application. It can provide higher gain and lower error, which results a better linearity and performance. Therefore, the OP structure pixel is implemented in our CMOS voltage mode sensor design. The compare of OP and source follower active device are shown in table II.

Fig. 2.4 shows the schematic of the implemented voltage mode image sensor circuit, which is composed of the sensor pixel and the correlated double sampling (CDS) readout circuit. The pixel is composed of a reset MOS (MR) and a photodiode. The CDS readout circuit is composed of some switches (SHS, SHR, CE, Clamp, Col, Group Column), storage capacitors (Cs, Cr), CDS couple capacitors (Co_s, Co_r), and the current source pairs (Mb3s, Mb3r).

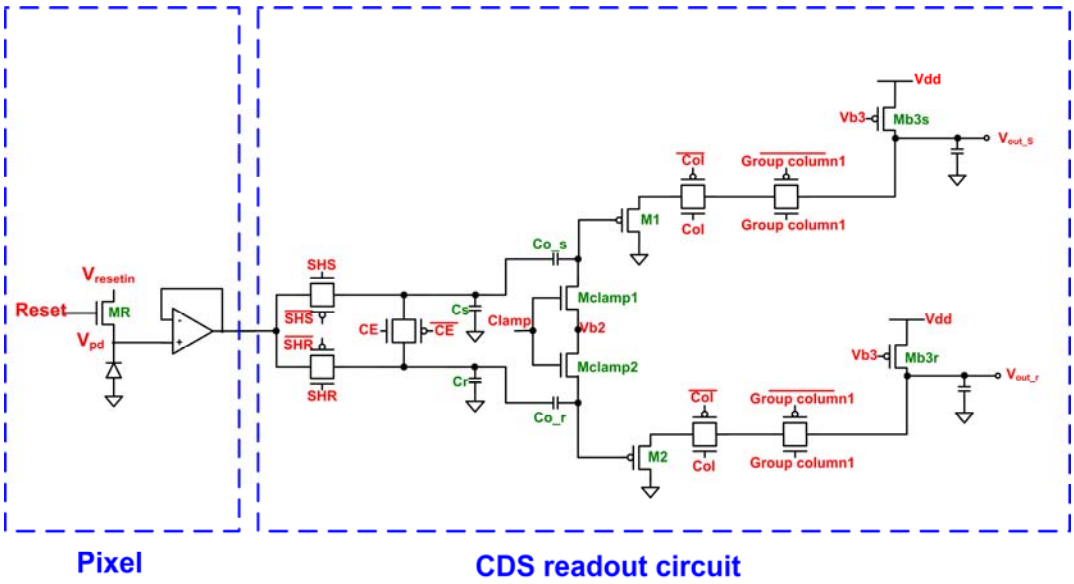


Figure 2.4 The 3T voltage mode sensor circuit

Fig. 2.5 shows the architecture of the operational amplifier in the Fig. 2.4, and Fig. 2.6 is the bias circuit of the amplifier. For low power consideration, the operational amplifier is biased at small dc current. The total dc current of the folded cascade amplifier is 24uA. The bias circuit of the folded cascade OP is designed to consume less dc current for low power, the total dc current of the bias circuit is 16uA. The total power consumption of the folded cascode amplifier is 0.00013 W. The device dimensions of the folded cascode amplifier are shown in table III and the device dimensions of the bias circuit are shown in table IV.

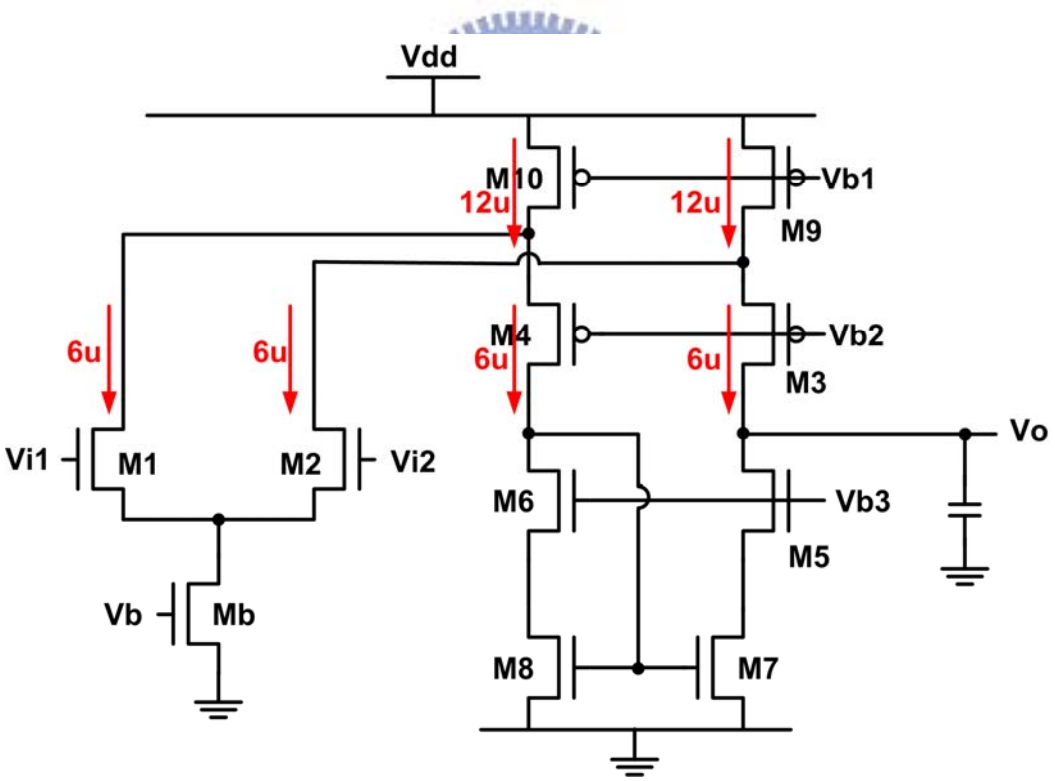


Figure 2.5 The folded cascade amplifier

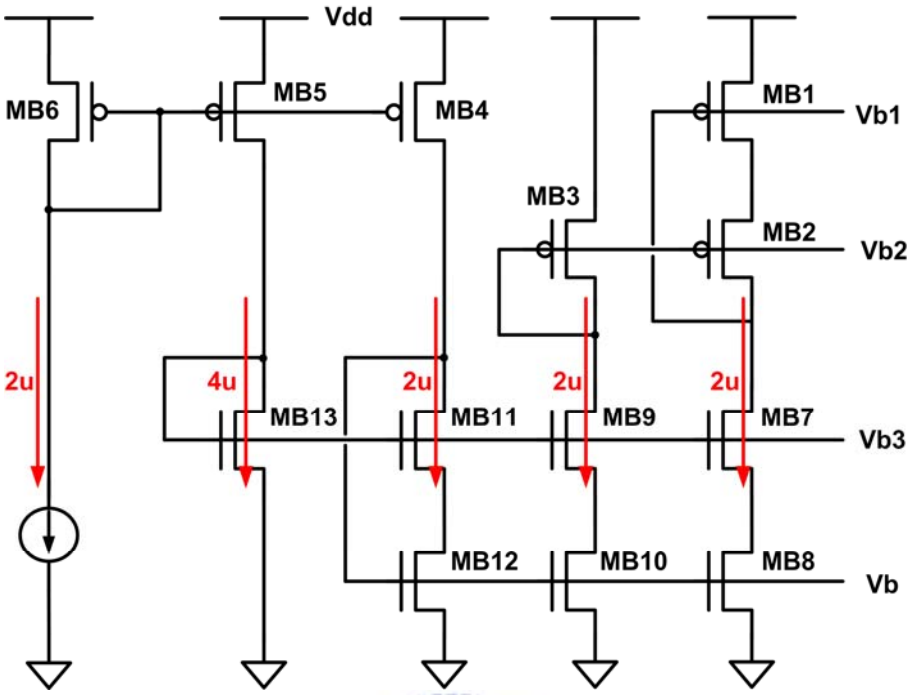


Figure 2.6 The bias circuit of folded cascade amplifier

The sensor readout operation of Fig. 2.4 is described as following and the control clock diagram is shown in Fig 2.7. First, the V_{pd} is reset to $V_{resetin}$ by device MR. After a fixed period of integration time, the V_{pd} (V_{sig}) is readout by the voltage buffer, and is sampled in Cs (SHS is on) as shown in Fig. 2.8. It gives,

$$V_{Cs} = V_{sig} \tag{2-13}$$

Then, MR and SHR are on, and the $V_{resetin}$ is sampled on the Cr, as shown in Fig. 2.9. It gives

$$V_{Cr} = V_{resetin} \tag{2-14}$$

The control signal Clamp is designed as being always on to keep M1 gate and M2 gate voltage in Vb2 during the sampling period of Cr and Cs. By using the designed Clamp operation, we can eliminate the charge injection and clock feedthrough non-ideal effect induced by the switches SHS and SHR.

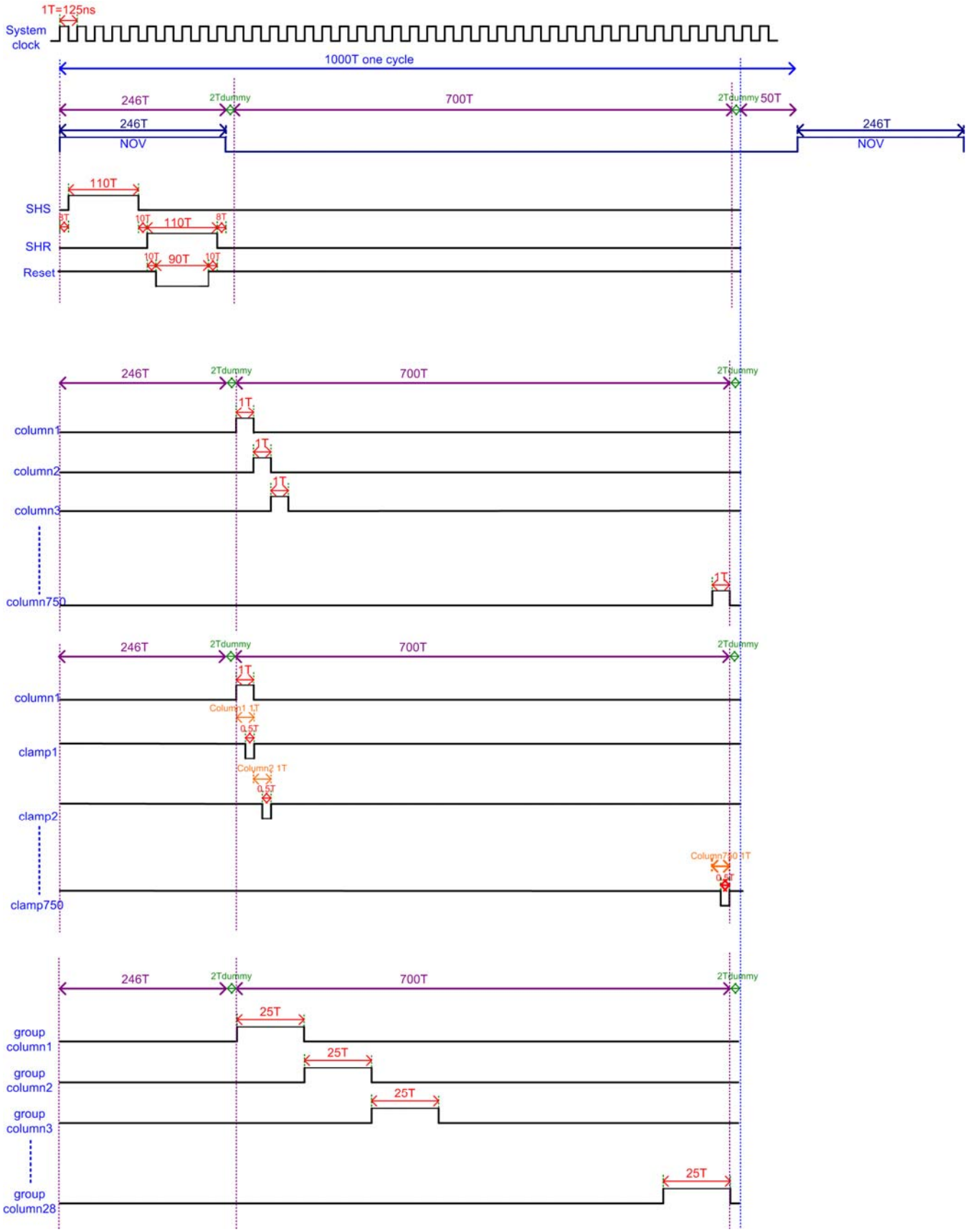


Figure 2.7 The clock diagram of the voltage mode sensor

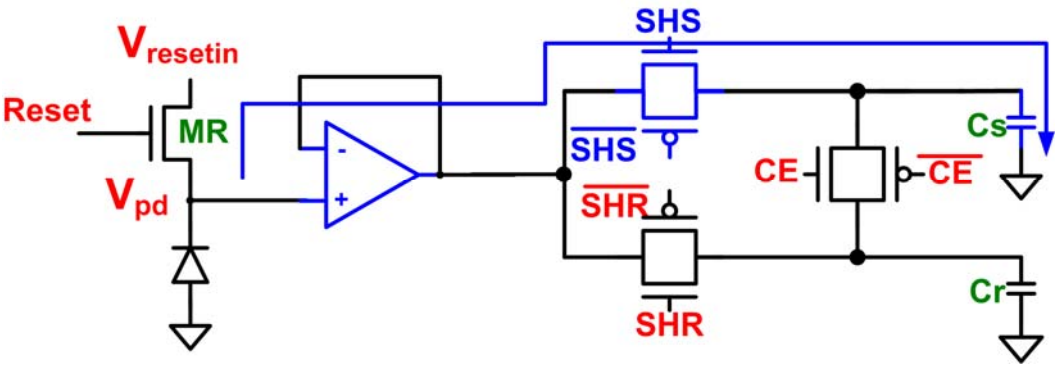


Figure 2.8 The sample-signal operation of voltage mode sensor

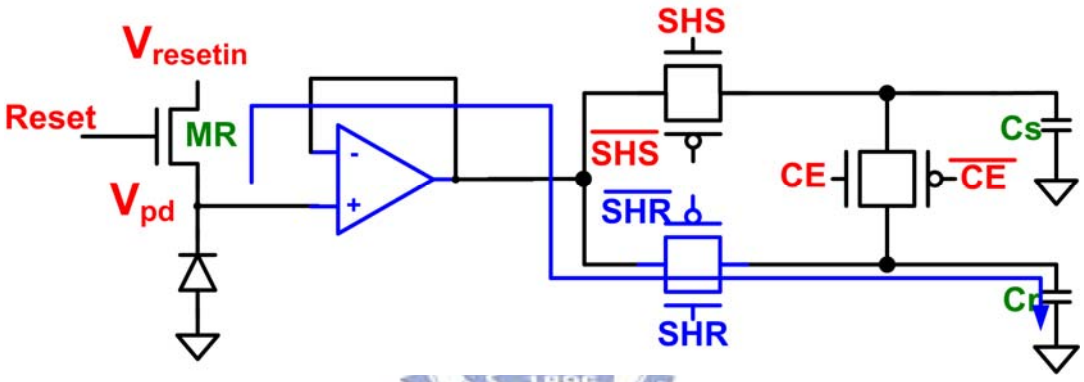


Figure 2.9 The sample-reset operation of voltage mode sensor

After signals being sampled to capacitors Cs and Cr, the switches controlled by signals “Group column” and “Col” are turned on. By turning off the switch controlled by “Clamp” and turning on the switch controlled by “CE”, the result is transferred to the nodes out_s and out_r as shown in Fig. 2.10. it gives,

$$V_{Cs} = \frac{V_{resetin} - V_{sig}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge} \quad (2\text{-}15)$$

$$V_{Cr} = \frac{V_{sig} - V_{resetin}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge} \quad (2\text{-}16)$$

V_{clamp_charge}: the voltage variation result from charge injection and clock feedthrough

induced by switch clamp

V_{CE_charge}: the voltage variation result from charge injection and clock feedthrough induced by switch CE

$$V_A = Vb2 + (\frac{V_{resetin} - V_{sig}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge}) \bullet \frac{Co\_s}{Co\_s + C_{M1\_gate}} \quad (2\text{-}17)$$

$$V_B = Vb2 + (\frac{V_{sig} - V_{resetin}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge}) \bullet \frac{Co\_r}{Co\_r + C_{M2\_gate}} \quad (2\text{-}18)$$

In the above equation, Vb2 is used to adjust the output common mode voltage by the level shift. The level shift is composed of Co_s, Cor, Mclamp1 and Mclamp2. Due to the design of the clock operation, the level shift wouldn't increase extra error in the output.

$$V_{out\_s} = \frac{V_{resetin} - V_{sig}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge} + Vb2 + V_{SG,M1} \quad (2\text{-}19)$$

$$V_{out\_r} = \frac{V_{sig} - V_{resetin}}{2} + \frac{V_{CE\_charge}}{2} + V_{clamp\_charge} + Vb2 + V_{SG,M2} \quad (2\text{-}20)$$

$V_{SG,M1}$: the V_{SG} of M1 MOS device

$V_{SG,M2}$: the V_{SG} of M2 MOS device

$$V_{out\_s} - V_{out\_r} = V_{resetin} - V_{sig} + V_{SG,M1} - V_{SG,M2} \quad (2\text{-}21)$$

From equation (2-21), we can find that the charge injection and clock feedthrough of switches SHS and SHR are eliminated by the CDS operation.

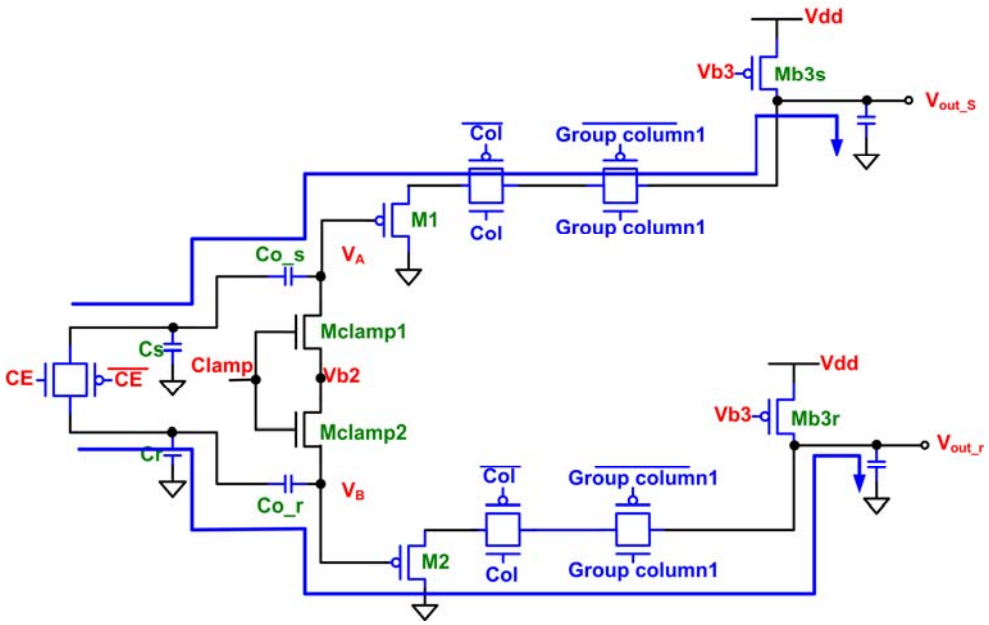


Figure 2.10 The operation of voltage mode sensor with “Col” on, “Clamp” off, and “CE” on,

By the way, the control signal “Group column” is designed to reduce the output loading of output nodes (Vout_s, Vout_r). The operation is described as below. In this work, there is 700 columns in the sensor array. If the control signal “Group column” is not used in the circuit, there will be 700 pairs transmission gate in the output node during the readout period. In the optimized design as shown in Fig. 2.11 and Fig. 2.12, the control signal “Group column” was used in the readout circuit as grouping architecture. It shows there are only 53 pairs of transmission gate loading left in the output node by grouping design. The total loading, represented in number of transmission gates, depends on grouping architecture is shown as equation (2-22).

$$Number\ \ of\ \ transmisson\ \ gates = column\ \ number + group\ \ number \quad (2\text{-}22)$$

By using the grouping architecture controlled by “Group column”, we can minimize the output loading and driving capability as well. Therefore, the power consumption is minimized and optimized in the readout circuit.

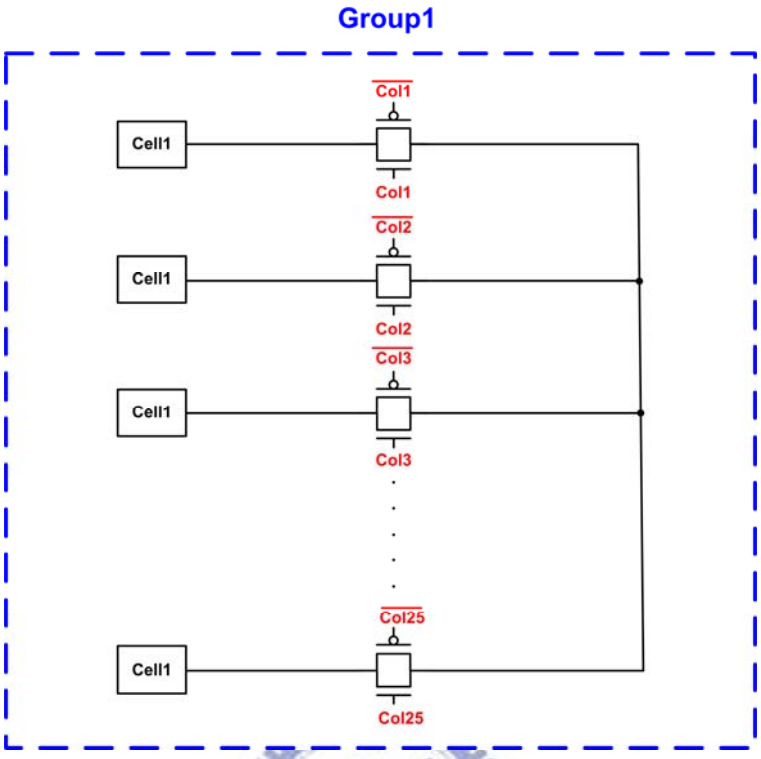


Figure 2.11 The illustration of Group

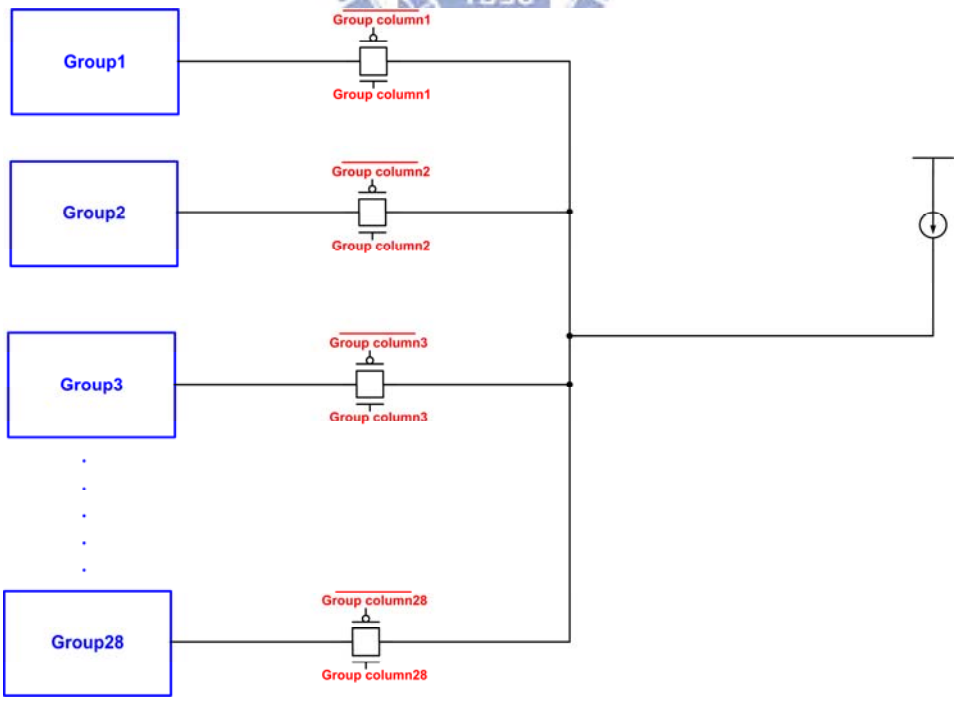


Figure 2.12 The illustration of Group column

	Operation amplifier	Source follower
Channel length modulation	**No**	**Yes**
Body effect	**No**	**Yes**
Offset voltage	**Yes**	**No**
Area	**Big**	**Small**
linearity	**High**	**Low**
Power (in this design about 3 times)	**High**	**Low**
Operation range (if maximum reset voltage 2.8V)	**1.3V~2.8V**	**1.3V~2.8V (V_{ov}=200mV)**

Table II. The compare of two type active device

Name	Type	Single Finger Size	Multiply	Total Size
M_1	NMOS	2μm/1μm	1	2μm/1μm
M_2	NMOS	2μm/1μm	1	2μm/1μm
M_9	PMOS	4μm/2μm	6	24μm/2μm
M_{10}	PMOS	4μm/2μm	6	24μm/2μm
M_3	PMOS	2.4μm/1μm	3	7.2μm/1μm
M_4	PMOS	2.4μm/1μm	3	7.2μm/1μm
M_7	NMOS	2μm/2μm	1	2μm2μm
M_8	NMOS	2μm/2μm	1	2μm/2μm
M_5	NMOS	1μm/2μm	3	3μm/2μm
M_6	NMOS	1μm/2μm	3	3μm/2μm
M_b	NMOS	1μm/2μm	6	6μm/2μm

Table III. The dimensions of the folded cascode operational amplifier

Name	Type	Single Finger Size	Multiply	Total Size
M_{B1}	PMOS	2μm/2μm	2	4μm/1μm
M_{B2}	PMOS	2.4μm1μm	1	2.4μm/1μm
M_{B3}	PMOS	1.2μm/4μm	1	1.2μm/4μm
M_{B4}	PMOS	2μm/2μm	1	2μm/2μm
M_{B5}	PMOS	2μm/2μm	2	4μm/2μm
M_{B6}	PMOS	2μm/2μm	1	2μm/2μm
M_{B7}	NMOS	1μm/2μm	1	1μm2μm
M_{B8}	NMOS	1μm/2μm	1	1μm/2μm
M_{B9}	NMOS	1μm/2μm	1	1μm/2μm
M_{B10}	NMOS	1μm/2μm	1	1μm/2μm
M_{B11}	NMOS	1μm/2μm	1	1μm/2μm
M_{B12}	NMOS	1μm/2μm	1	1μm/2μm
M_{B13}	NMOS	0.5μm/4μm	1	0.5μm/4μm

Table IV. The dimensions of the folded cascode operational amplifier bias circuit

2.1.2 Architecture of 4T voltage mode sensor

The Fig. 2.13 shows the general 4T sensor pixel. It is composed of a voltage buffer (active device).The obviously difference between 3T sensor pixel and 4T sensor pixel is the number of MOS. There is an extra MOS TG in the 4T pixel, and the integration node is not V_{pd}. The readout circuits of 4T voltage mode sensor and 3T voltage mode sensor are the same as shown in Fig. 2.14. The operation of the 4T sensor pixel is described as following. First, the voltage of node V_{pd} is reset to $V_{resetin}$ by M_{reset}, and control signal TG is on to charge the voltage of node A as $V_{resetin}$, too. After a fixed integration period, V_{pd} would be discharged by the photocurrent of the photodiode and decreased from a high potential voltage to a low potential voltage. Then, the control signal reset is on again to reset the node V_{pd} to $V_{resetin}$, and the control signal TG is on to transfer charge from node A to node V_{pd}. After the process of charge transfer, the signal would be transfer to the CDS readout circuit by the voltage buffer. The clock diagram is shown in the Fig. 2.15, and the control signals of Col, Group column and the clamp is the same with 3T sensor.

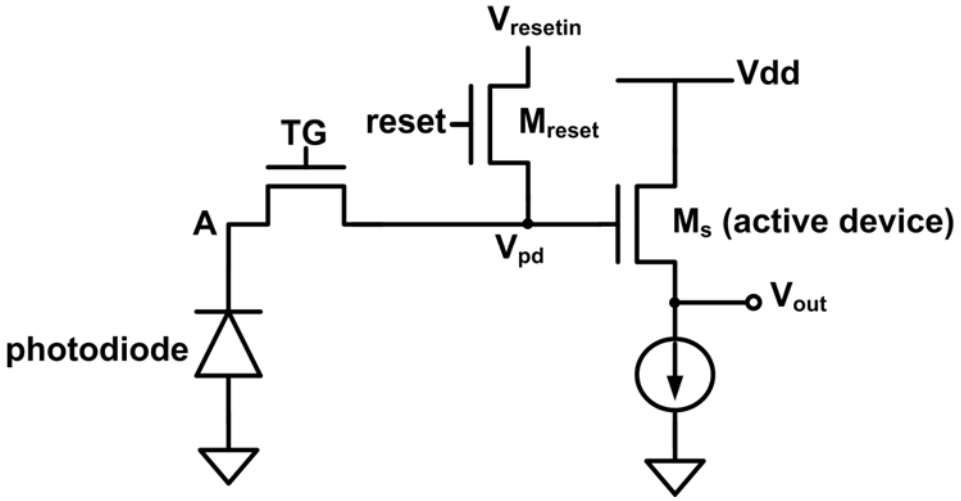


Figure 2.13 The general 4T voltage mode sensor pixel

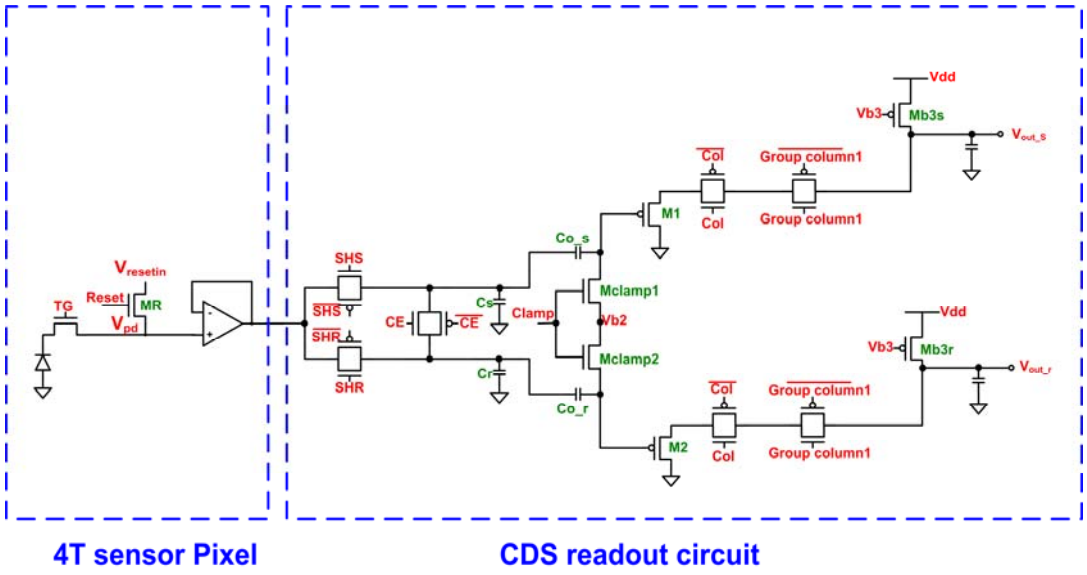


Figure 2.14 The 4T voltage mode sensor circuit

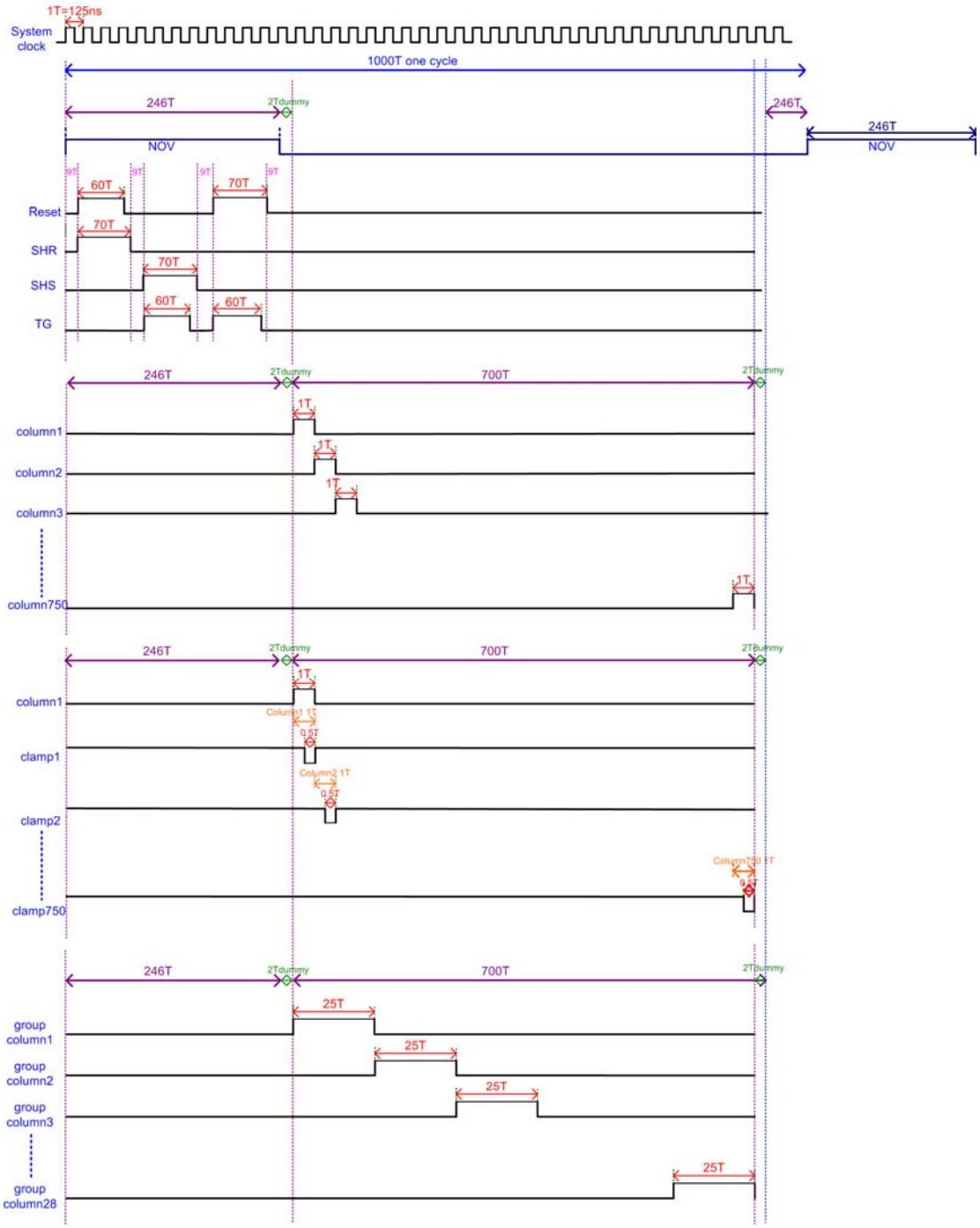


Figure 2.15 The clock diagram of the 4T voltage mode sensor

2.2 Architecture of CMOS current mode image sensor

In the following, the architecture of proposed 3T current mode image sensor would be described.

In general, the current mode sensor pixel is composed of a reset MOS (M_{reset}), a photodiode and an active device (M_{tr}) as shown in Fig. 2.16. The active device serves as a front-end gain stage to amplify the small signal current generated by photodiode. The fixed-pattern noise (FPN) induced by the threshold voltage (V_t) variation is found to be significant. In order to suppress the FPN, the threshold voltage must appear as the first order term in the output current equation. Therefore, the active device is usually designed to operate in the triode region, and the output current equation is shown as equation (1).

$$I_{pix} = \mu_{eff} C_{cox} \frac{W}{L}\left[(V_{sg} - |V_{tp}|)V_{sd} - \frac{1}{2}V_{sd}^{2}\right] \quad (2\text{-}22)$$

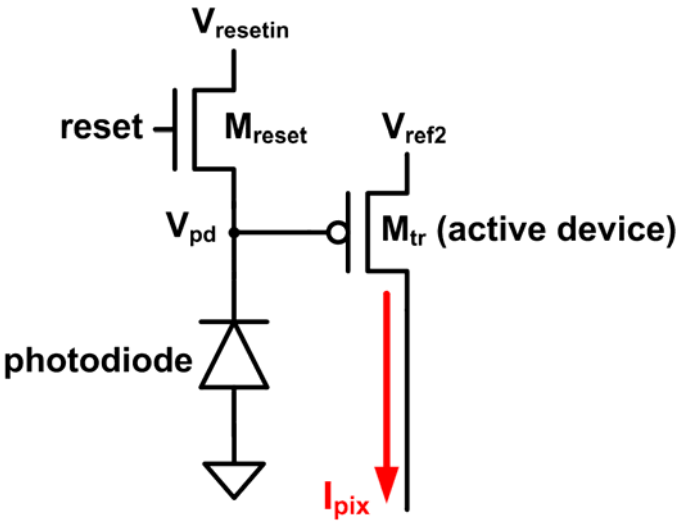


Figure 2.16 The general current mode sensor pixel.

The transconductance of M_{tr} is given by equation (2-23)

$$g_m = \mu_{eff} C_{ox} \frac{W}{L} V_{sd} \tag{2-23}$$

The I_D-V_g characteristic of both n-type and p-type active devices are simulated in the circuit as shown in Fig. 2.17.

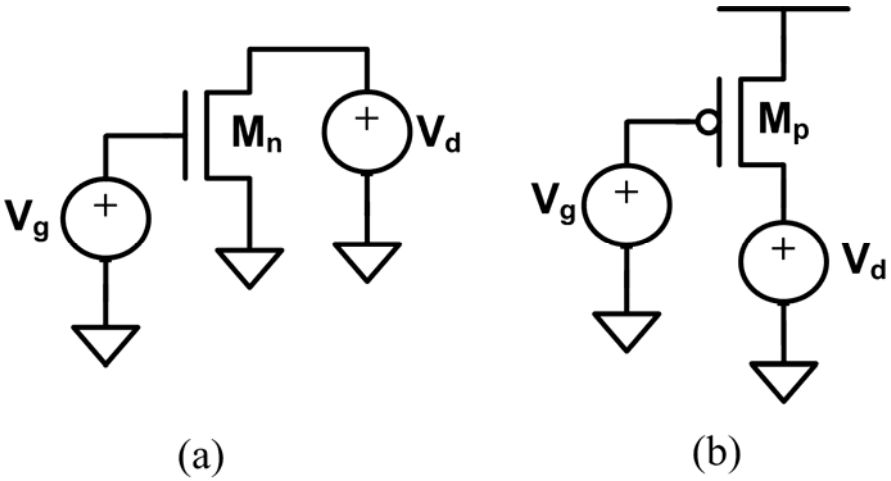


Figure 2.17 (a) NMOS active device (b) PMOS active device.

Fig. 2.18 (a) shows the relation between V_g and output current I_{pix} of the NMOS active device. The similar result can be also observed for the PMOS as shown in Fig. 2.18 (b) .The linearity is degraded when V_{ds} is smaller than 1.8V due to the mobility degradation [7]. With the mobility degradation effect as described in equation (2-24), the drain current I_{pix} in the triode region can be re-written as equation (2-25).

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{sg}-|V_t|)} \tag{2-24}$$

$$I_{pix} = \frac{\mu_0}{1+\theta(V_{sg}-|V_t|)} C_{cox} \frac{W}{L}\left[(V_{sg}-|V_{tp}|)V_{sd}-\frac{1}{2}V_{sd}{}^2\right] \tag{2-25}$$

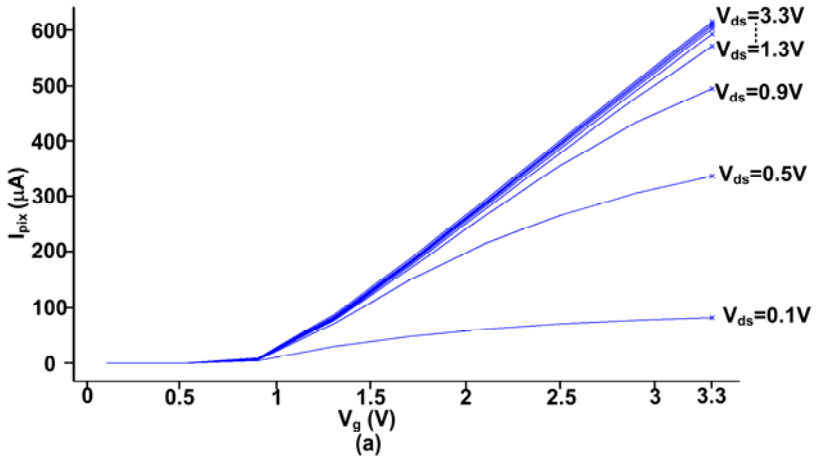


Figure 2.18 (a) NMOS V_g versus I_{pix} with different V_{ds}

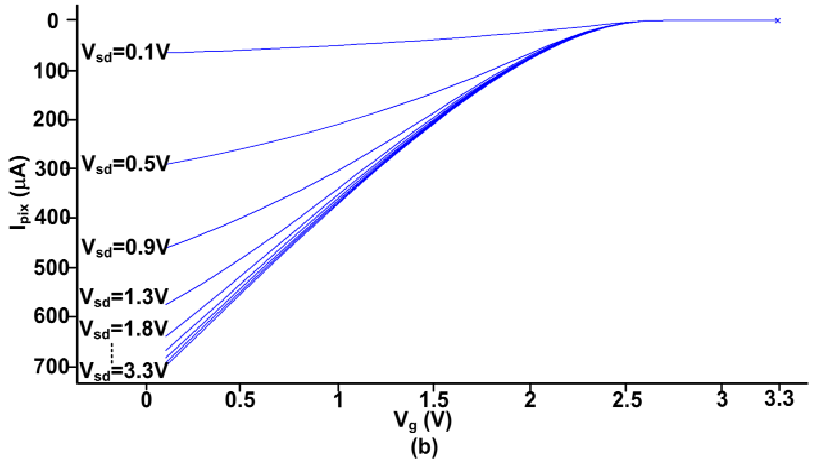


Figure 2.18 (b) PMOS V_g versus I_{pix} with different V_{sd}

As shown in equation (2-25), both the p-type and n-type active device can't convert the V_{pd} to I_{pix} with perfect linearity. It can be improved by utilizing the active device with a long channel length [2]. The Fig. 2.19 shows that g_m is more independent of V_g when the channel length is increased. That is, the V_{pd} — I_{pix} linearity is improved with longer channel length of the active device (M_{tr}). However, there exists a tradeoff between the sensitivity and channel length. The long channel length results in larger capacitance at node V_{pd} and decreases the sensitivity.

The operation of the circuit in Fig. 2.16 is described as following. First, the switch M_{reset} turns on and reset the node V_{pd} to $V_{resetin}$. After a fixed integration period, V_{pd} would be discharged by the photocurrent of the photodiode and decreased from a high potential voltage to a low potential voltage.

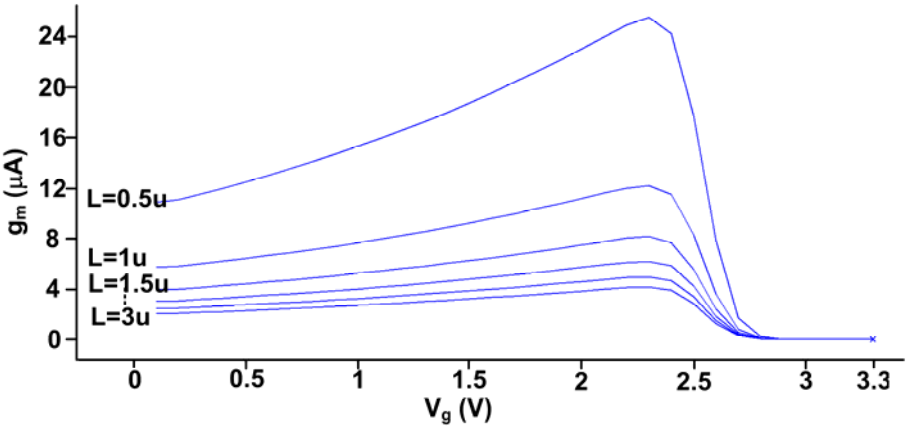


Figure 2.19 V_g versus g_m with different channel length of PMOS active device

During the signal integration, the current gain of the n-type active device is changed from high to low, and the current gain of the p-type active device is changed from low to high. It is found that the PMOS active device can provide a gamma-like transfer curve referred to the input light density. This will result a better sensitivity in the low light and a higher dynamic range. Therefore, the PMOS active device operated with a smaller V_{ds} is chosen to be a better choice in the application of current mode sensor pixel. The Fig. 2.20 shows the analysis result of NMOS and PMOS active device V_{pd} versus I_{pix} when V_{ds} = 0.1V.

From the Fig. 2.18 (a) and (b), the I_{pix} reveals a better linearity when V_{ds} is increased and the active device is operated in the saturation region. It is due to the velocity saturation effect in deep submicron devices. The I_D equation in saturation

region can be rewritten as [7]

$$I_D = \nu_{sat} W C_{ox} (V_{GS} - V_T) \tag{2-26}$$

$$g_m = \nu_{sat} W C_{ox} \tag{2-27}$$

It is shown that the threshold voltage V_t appears as the first order term, and its variation can be eliminated by the following CDS operation. However, the bias current is too large and consumes power when operated in the velocity saturation region. It can be used on those applications need high linearity but with adequate power consumption budget.

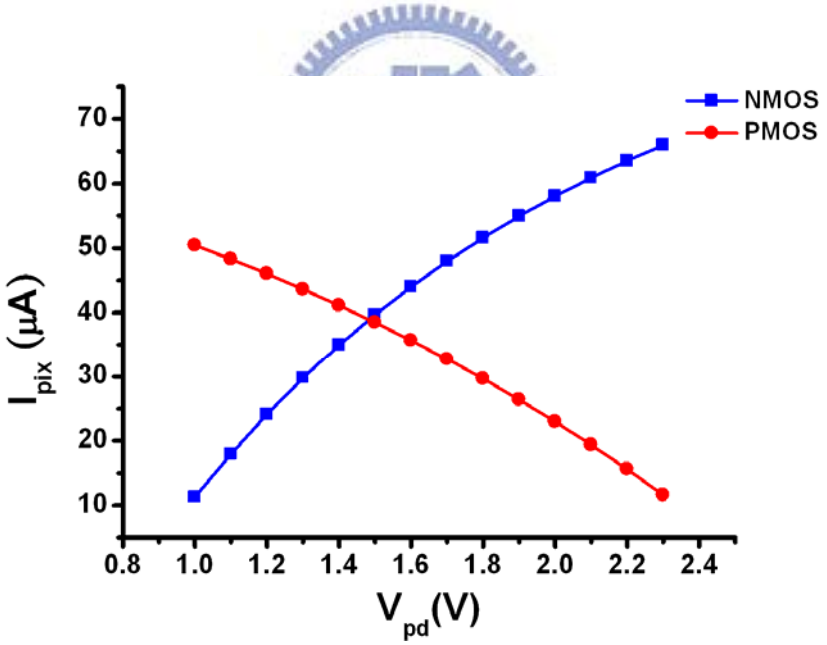


Figure 2.20 NMOS and PMOS active device V_{pd} versus I_{pix} when V_{ds} = 0.1V.

The proposed programmable gain pixel is shown in Fig. 2.21 [3], which is composed of a NMOS transistor, a PMOS transistor, an operational amplifier, and two NMOS transistors. The active device M_{tr} acts as a transimpedance amplifier. It converts and amplifies the diode signal V_{pd} to the output current I_{pix}. The operation

amplifier, M_1 and M_2 establishes a negative feedback configuration and makes Vi^+ equal to V_{ref1}. The output current I_{pix} is given by equation (2-28).

$$I_{pix} = \frac{\mu_0}{1+\theta(V_{sg}-|V_t|)} C_{cox} \frac{W}{L}\left[(V_{sg}-|V_{tp}|)V_{sd} - \frac{1}{2}V_{sd}^{\ 2}\right] \quad (2\text{-}28)$$

$$V_{sg} = V_{ref\,2} - V_{pd} \quad (2\text{-}29)$$

$$V_{sd} \cong V_{ref\,2} - V_{ref\,1} \quad (2\text{-}30)$$

The transconductance of M_{tr} is

$$g_m = \frac{\mu_0}{1+\theta(V_{sg}-|V_t|)} C_{ox} \frac{W}{L} V_{sd} \quad (2\text{-}31)$$

It is shown that the programmable g_m, as well as current gain, can be easily implemented by tuning V_{sd}, without extra hardware. With the front-end gain stage, the signal current is amplified and fed into the following current mirroring and subtraction stage. It can improve the current operation accuracy when the signal is small at low light condition. Moreover, the SNR can be improved by the proposed front-end gain stage.

The swing of V_{pd} is described in equation (2-32). Compared to voltage mode readout, it shows an almost x2 signal swing, that is, x2 full-well capacity based on a specified operating supply voltage. The higher gain, set by a larger V_{sd} bias condition, will decrease the available signal swing at node V_{pd}.

$$0 < V_{pd} < V_{ref\,2} - |V_{tp}| - V_{sd} \quad (2\text{-}32)$$

We propose a current-mode readout circuit with multiple-gain device to solve this design tradeoff.

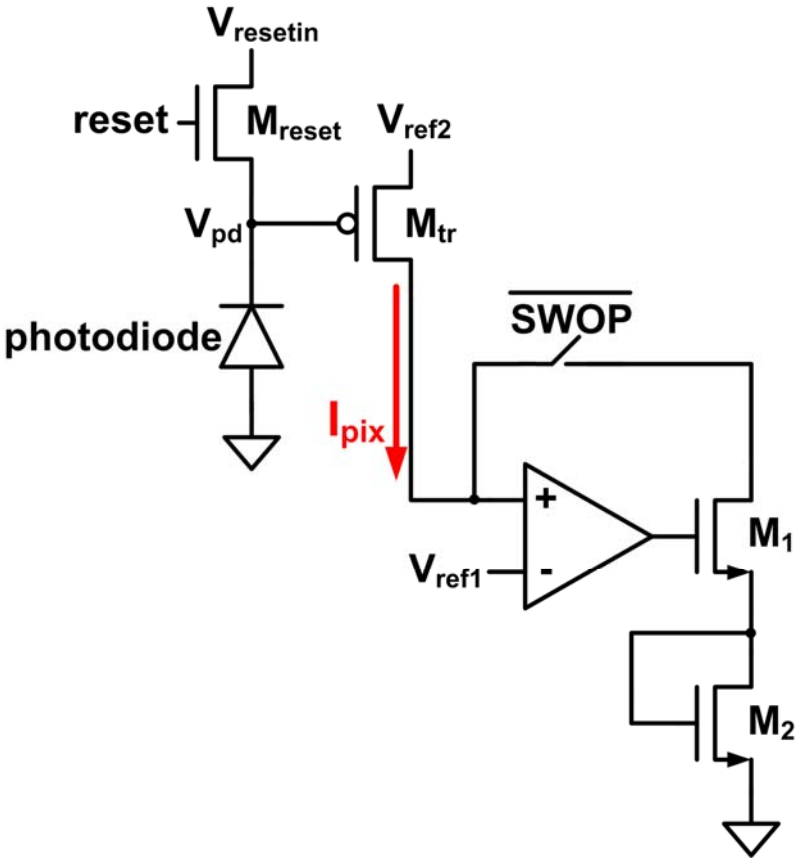


Fig. 2.21 the proposed gain pixel

The architecture of the operational amplifier in the Fig. 2.21 is shown in Fig.2.22. The architecture of the operational amplifier is the two stage operation amplifier. It is designed for high gain to enhance the linearity of the gain pixel. Besides, we also designed the switch swop to turn off the operation amplifier when the readout period. Therefore, the proposed current mode image sensor can consume less power since the OP can consume less power in the sensor readout operation. The dimension of the two stage operation amplifier is shown in table V.

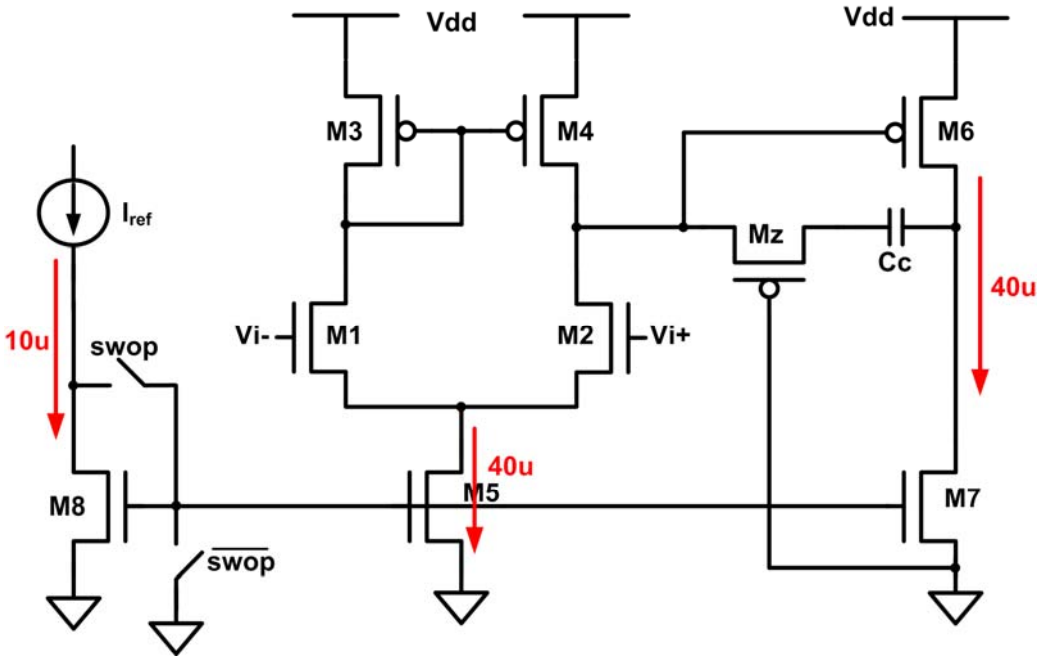


Fig. 2.22 the schematic of two stage operation amplifier

The proposed current mode readout circuit is shown in Fig.2.23. The operation is described as following. First, the V_{pd} is reset to $V_{resetin}$ by device M_{reset}. After a fixed period of integration time, V_{pd} would be discharged by the photocurrent of the photodiode and decreased from a high potential voltage to a low potential voltage due to the different incident light. After the integration time, the amplified signal current I_{sig} is readout and sampled at C_s as shown in Fig. 2.24 .

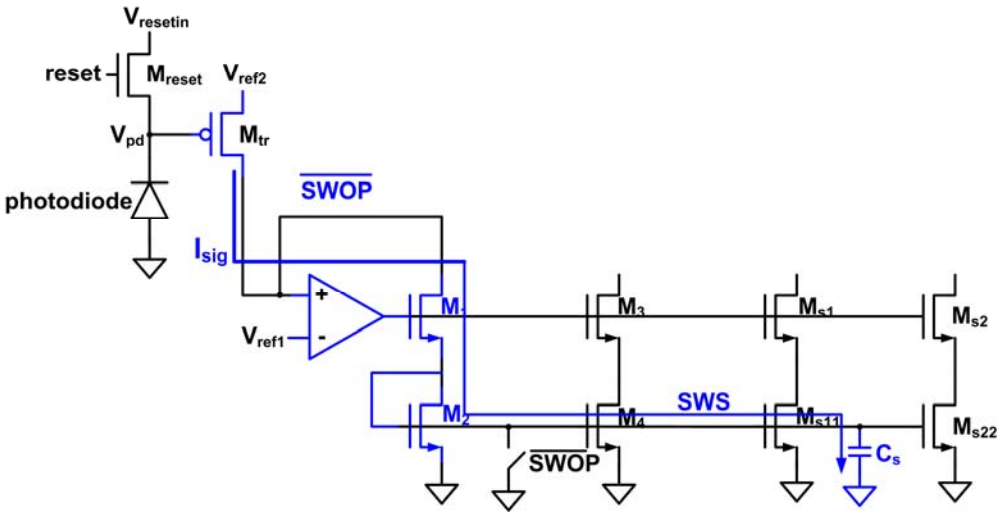


Fig. 2.24 the sample signal operation of current mode sensor

Then, by turning on the reset M_{reset} again, the I_{reset} is output and mirrored to the M_{r11} as shown in Fig. 2.25.

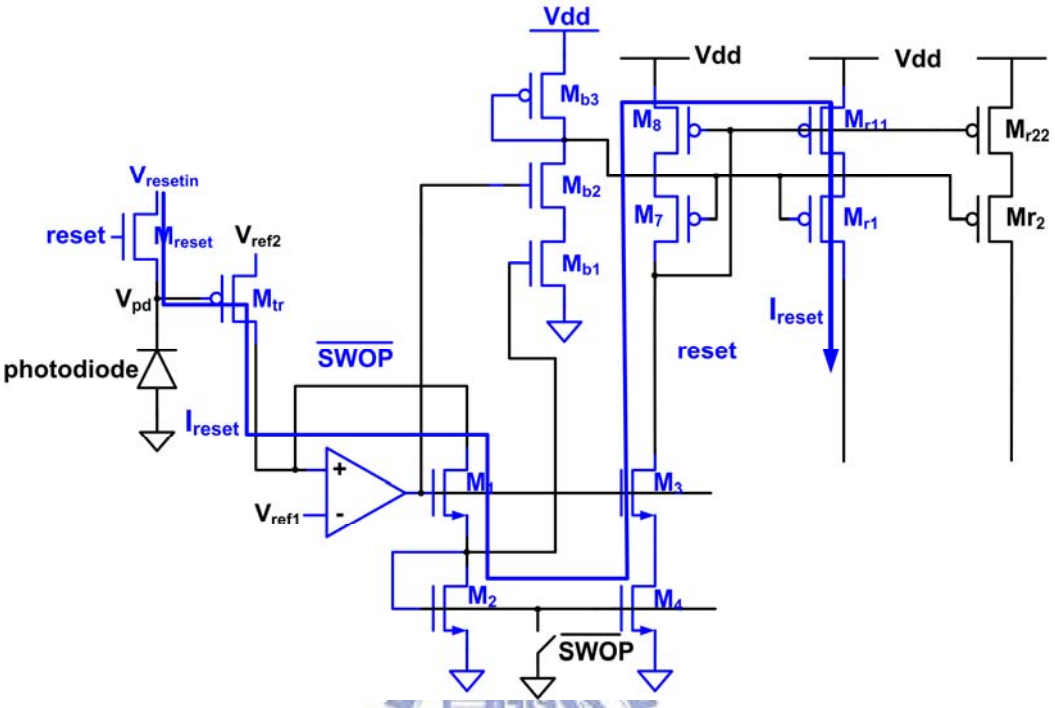


Fig. 2.25 the reset operation of current mode sensor

The correlated double sampling (CDS) is implemented by the current subtraction $I_{out} = I_{sig} - I_{reset}$, and the result is sampled to the current memory $M_o[8]$ and stored on the capacitor C_{out} as shown in Fig. 2.26. After the CDS operation, the output current I_{out} can be described as following.

$$I_{sig} = \mu_p C_{ox} \frac{W}{L}\left[(V_{ref\,2} - V_{sig} - |V_{tp}|)V_{sd} - \frac{1}{2}V_{sd}^{\,2}\right] \tag{2-33}$$

$$I_{reset} = \mu_p C_{ox} \frac{W}{L}\left[(V_{ref\,2} - V_{reset} - |V_{tp}|)V_{sd} - \frac{1}{2}V_{sd}^{\,2}\right] \tag{2-34}$$

$$I_{out} = \mu_p C_{ox} \frac{W}{L}(V_{reset} - V_{sig})V_{sd} \tag{2-35}$$

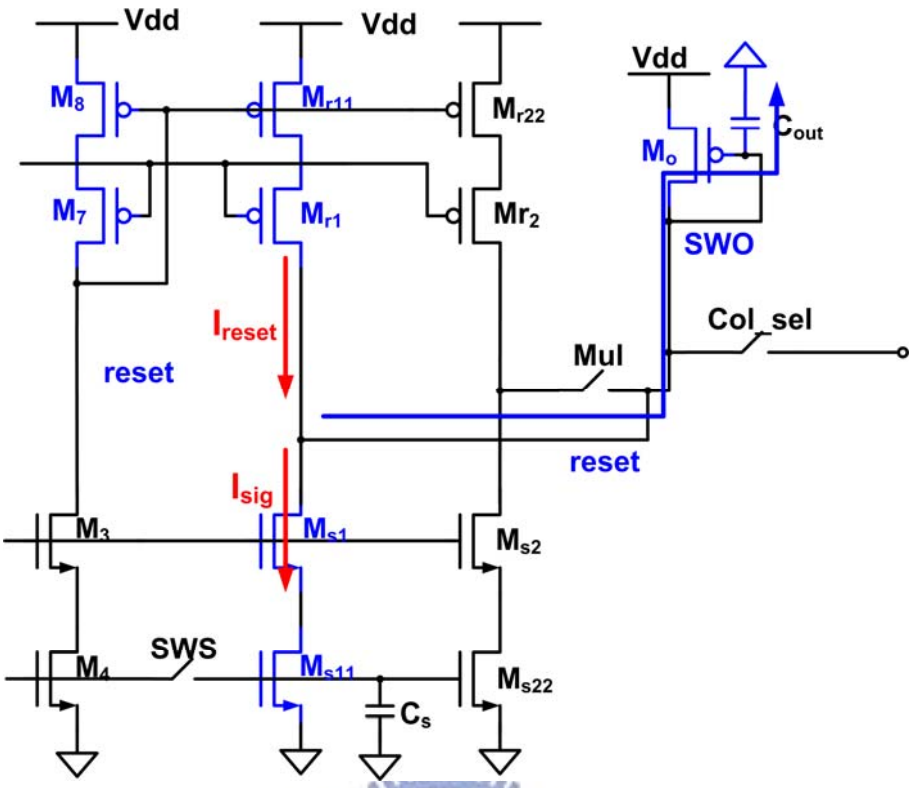


Fig. 2.26 the CDS operation of current mode sensor

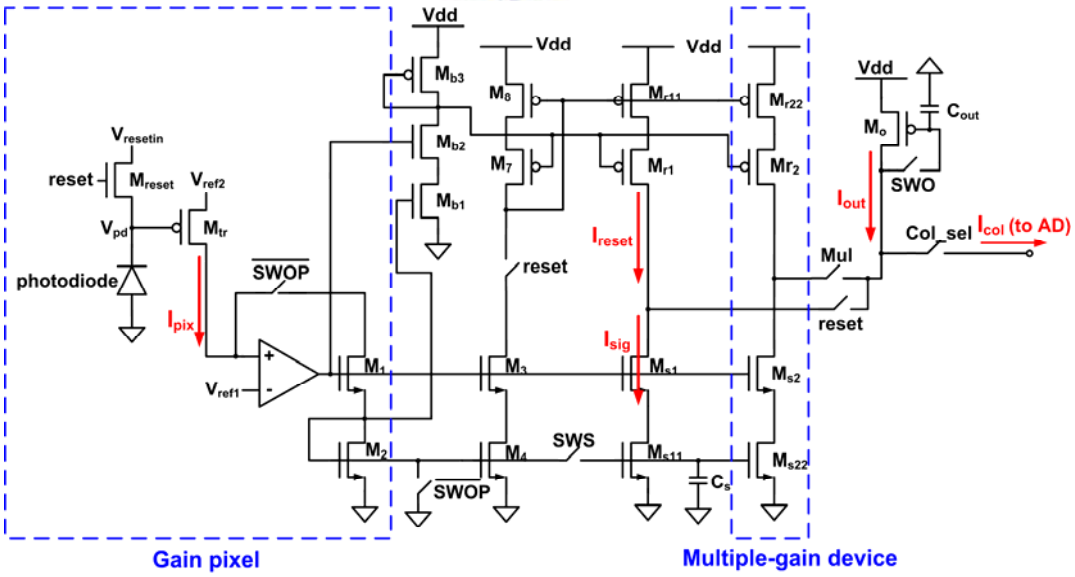


Fig. 2.23 the proposed current mode sensor circuit

The CDS function is used to eliminate the fixed-pattern noise induced by the threshold voltage variation in pixel circuit. It is shown in equation (2-35) that the threshold voltage term is cancelled out by the subtraction of two correlated sampling. The cascode devices are used to enhance the linearity and accuracy of the current mirror.

The bias voltages of cascode devices are self-generated without additional circuit and dc path. Moreover, a low standby power option is implemented by the switch SWOP. All the dc paths of current mirrors can be disabled after CDS operation, and the operational amplifier will be disabled synchronous. Therefore, there is no any dc current path in the readout interval which results in an ultra-low power consumption.

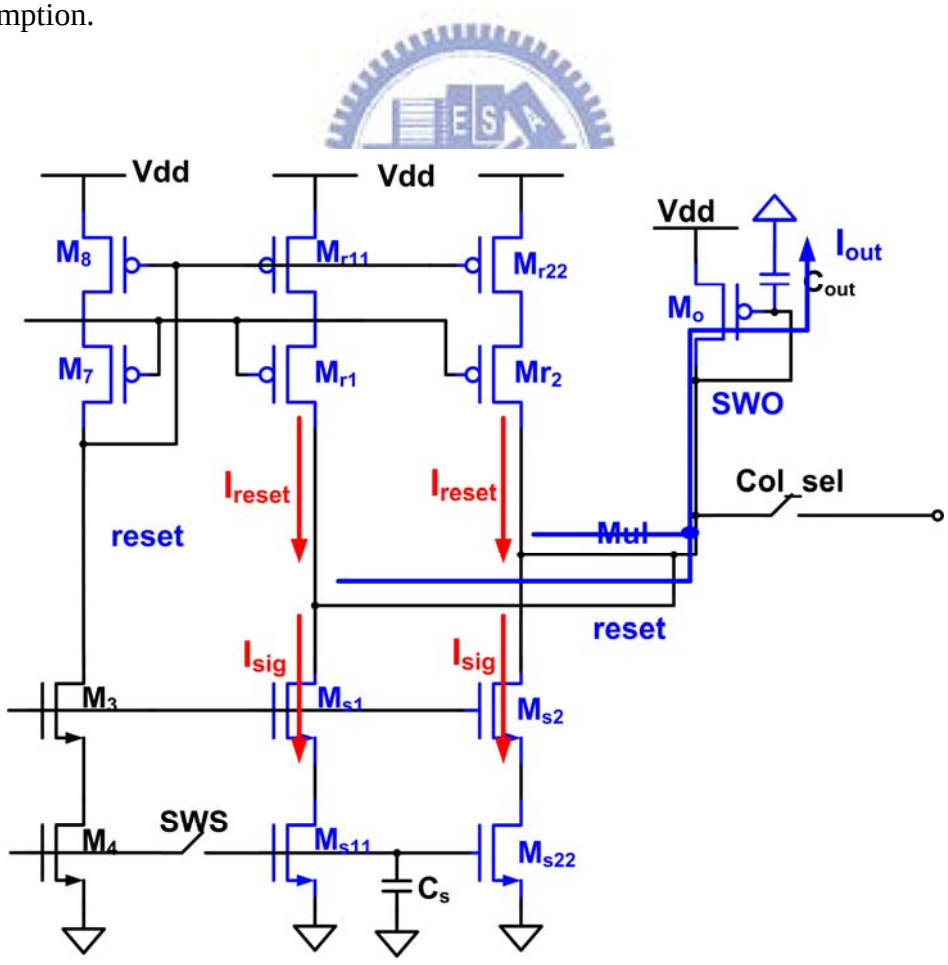


Fig. 2.27 the multiple-gain device operation of current mode sensor

The multiple-gain device is composed of M_{r2}, M_{r22} M_{s2}, M_{s22} and a switch Mul as shown in Fig. 2-23. In the low light level condition, the multiple-gain device can provide an additional gain by switching on Mul. The total gain of the proposed circuit can be enhanced. This additional gain option can release the design tradeoff between front-end gain setting (V_{sd}) and the available signal swing. The operation of the multiple-gain device is shown in Fig. 2.27.

The average power consumption of the proposed current mode sensor depends on the clock period, and it can be described as equation (2-36). P_{CDS} is the average power during CDS period (in this circuit about 3.2×10^{-4} W), T_{CDS} is the time during CDS period, and T_{total} is the total time of a line time. For example, if the CDS interval is 5us and the total time is 125us, the average power is 1.28×10^{-5} W.

$$Average\ \ power = \frac{3.2\times10^{-4}\times T_{CDS}}{T_{total}} \qquad (2\text{-}36)$$

T_{CDS}: the time during CDS period

T_{total}: the total time of a line time

The Fig. 2.28 shows the control signal of the proposed current mode sensor circuit.

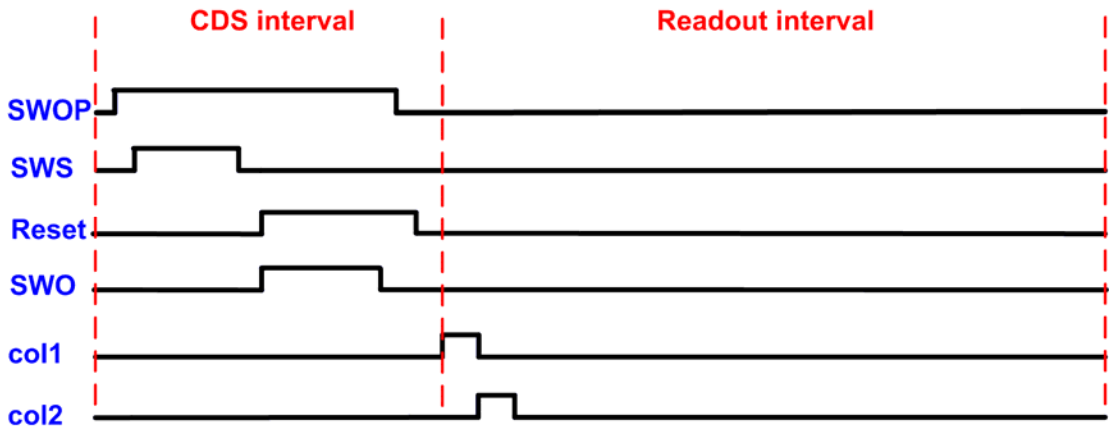


Fig. 2.28 control signal of the current mode sensor

Name	Type	Single Finger Size	Multiply	Total Size
M_1	NMOS	2μm/1μm	2	4μm/1μm
M_2	NMOS	2μm/1μm	2	4μm/1μm
M_3	PMOS	5μm/0.4μm	2	10μm/0.4μm
M_4	PMOS	5μm/0.4μm	2	10μm/0.4μm
M_5	NMOS	2μm/1μm	4	8μm/1μm
M_6	PMOS	5μm/0.4μm	4	20μm/0.4μm
M_7	NMOS	2μm/1μm	4	8μm/1μm
M_Z	PMOS	2μm/2μm	4	8μm/2μm
M_8	NMOS	2μm/1μm	1	2μm/1μm
M_{swop}	NMOS	5μm/0.35μm	1	5μm/0.35μm
C_C	cap	400f	1	400f

Table V. the dimensions of the two stage operational amplifier

2.3 Simulation result

2.3.1 Simulation result of 3T voltage mode sensor

The voltage mode image sensor has been simulated with 0.18um 3.3V CMOS SPICE model. The Fig. 2.29 shows the output voltage from the proposed readout circuit for different photocurrent, and the linearity is near 99.82%.

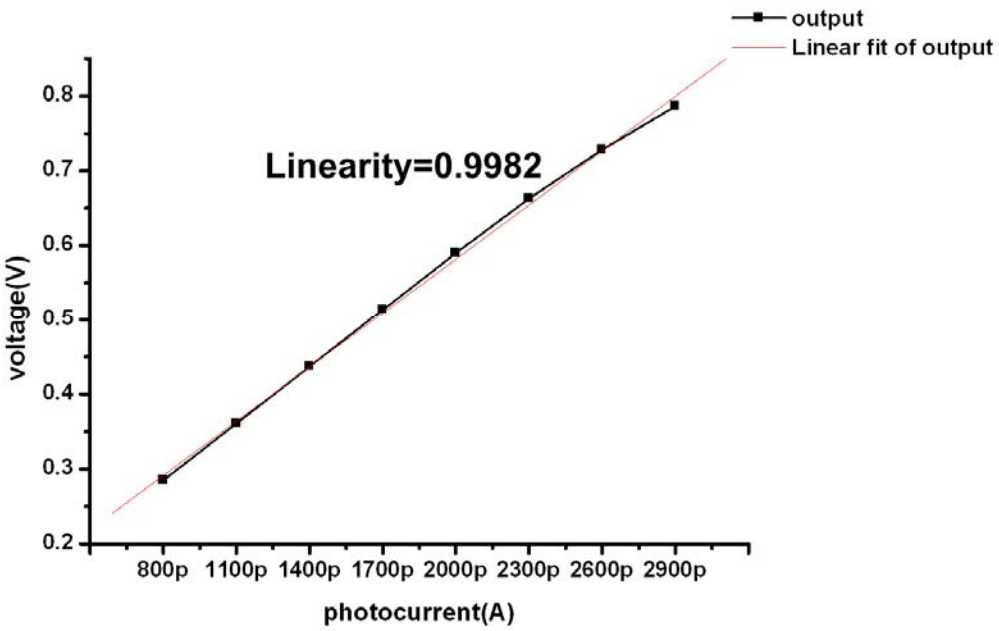


Figure 2.29 The photocurrent versus output voltage

2.3.2 Simulation result of 3T current mode sensor

The proposed linear current mode image sensor has been simulated with 0.18um 3.3V CMOS SPICE model. The Fig. 2.30 shows the output current from the proposed readout circuit for different photocurrent, and the linearity is near 99.17%. The gamma-like response curve is due to the PMOS active device which can improve the dynamic range. The simulated front-end gain with different V_{sd} tuned by V_{ref1} is shown in Fig. 2.31 It shows a x1 ~ x4 programmable current gain with a high linearity as 99.96%. The tunable voltage V_{ref1} can be implemented by a DAC with a resolution depends on applications. Fig. 2.32 shows the additional x2 gain provided by multiple-gain device with a high linearity.

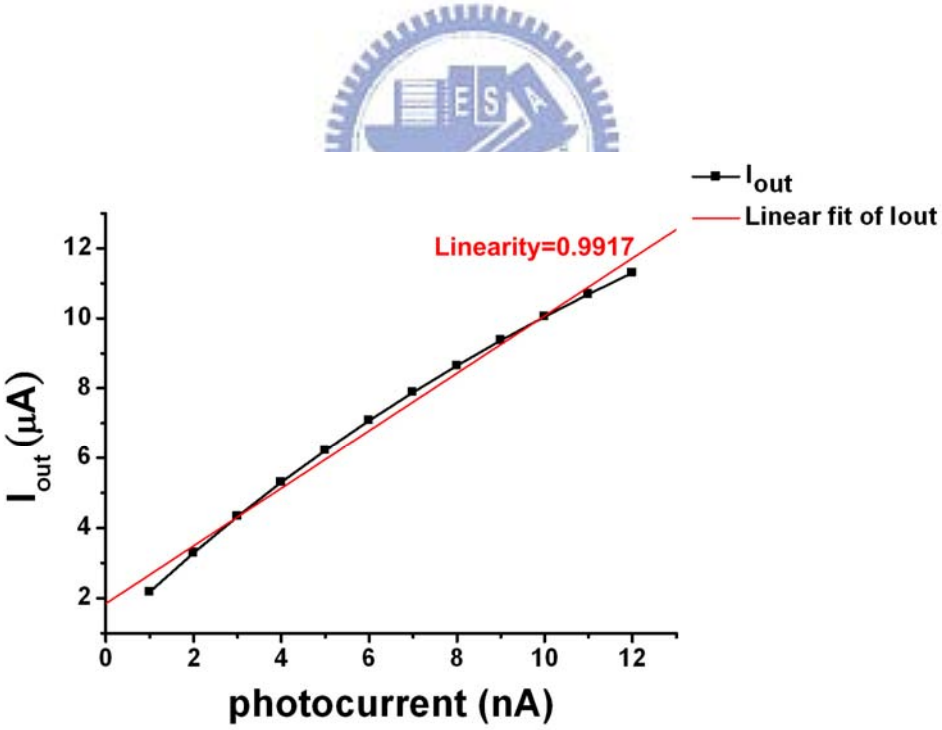


Figure 2.30 The photocurrent versus output current I_{out}.

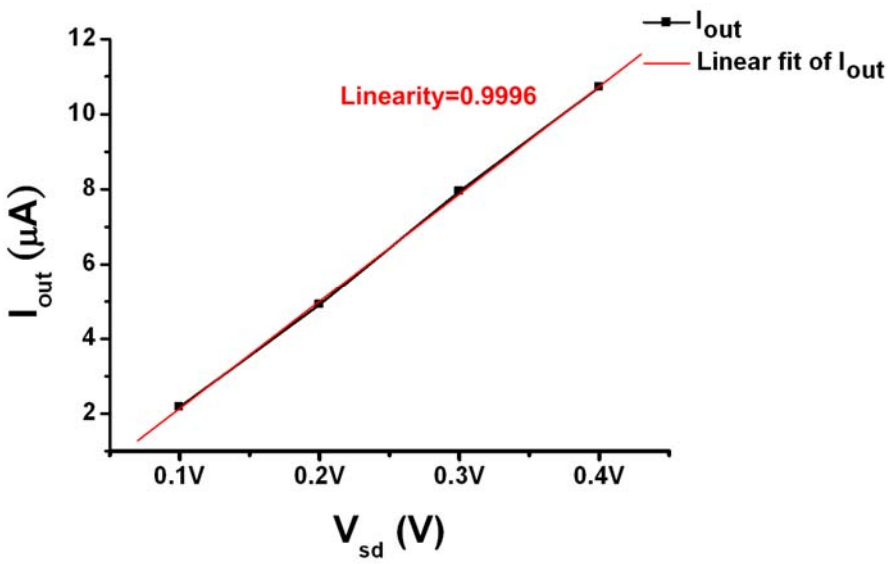


Figure 2.31 The V_{sd} of the M_{tr} versus output current I_{out}.

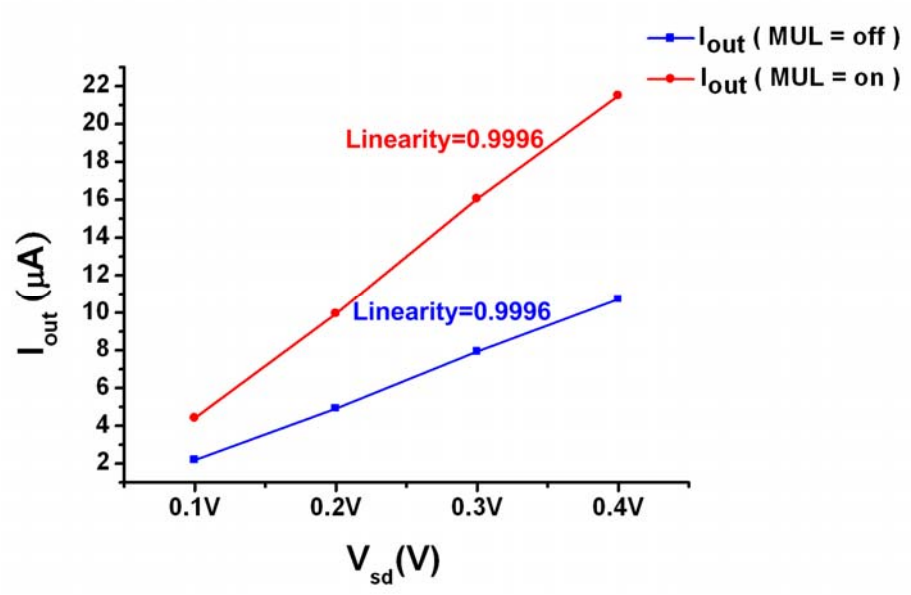


Figure 2.32 The V_{sd} of the M_{tr} versus output current I_{out} with multiple-gain option controlled by Mul.

Chapter 3
Layout Description and Experimental Results

3.1 Layout description

The Fig. 3.1 shows the 3T CMOS sensor pixel layout, the layer is the same with Fig. 2.13. It is composed of a sensor (photodiode) and a reset MOS. Because of the restriction of the design rules, the minimum poly gate width of the reset MOS is 0.6um. The Fig. 3.2 shows 4T CMOS sensor pixel layout, the layer is the same with Fig. 2.17. It is composed of a sensor (photodiode), a TG MOS and a reset MOS. The minimum poly gate width of TG MOS and reset MOS are 0.7 um and 0.4 um due to restriction of the design rules. The Fig. 3.3 is the 3T version of full-chip layout, it includes 704 3T sensor array, 704 readout circuits, the digital control circuit, a programmable gain amplifier, and a analog to digital converter. The Fig. 3.4 shows the 3T version of test-chip layout, it includes one 3T sensor and one readout circuit. The Fig. 3.5 shows the 4T version of full-chip layout, it includes 704 4T sensor array, 704 readout circuits, the digital control circuit, a programmable gain amplifier, and a analog to digital converter. The Fig. 3.6 shows the 4T version of test-chip layout, it includes one 4T sensor and one readout circuit. The Fig. 3.7 shows the 3T version of current mode sensor test-chip layout, it includes one 3T sensor and one current mode CDS readout circuit. The Fig. 3.8 shows the 3T version of 68 cell current mode sensor full-chip layout, and it includes 68 3T sensor and 68 readout circuits.

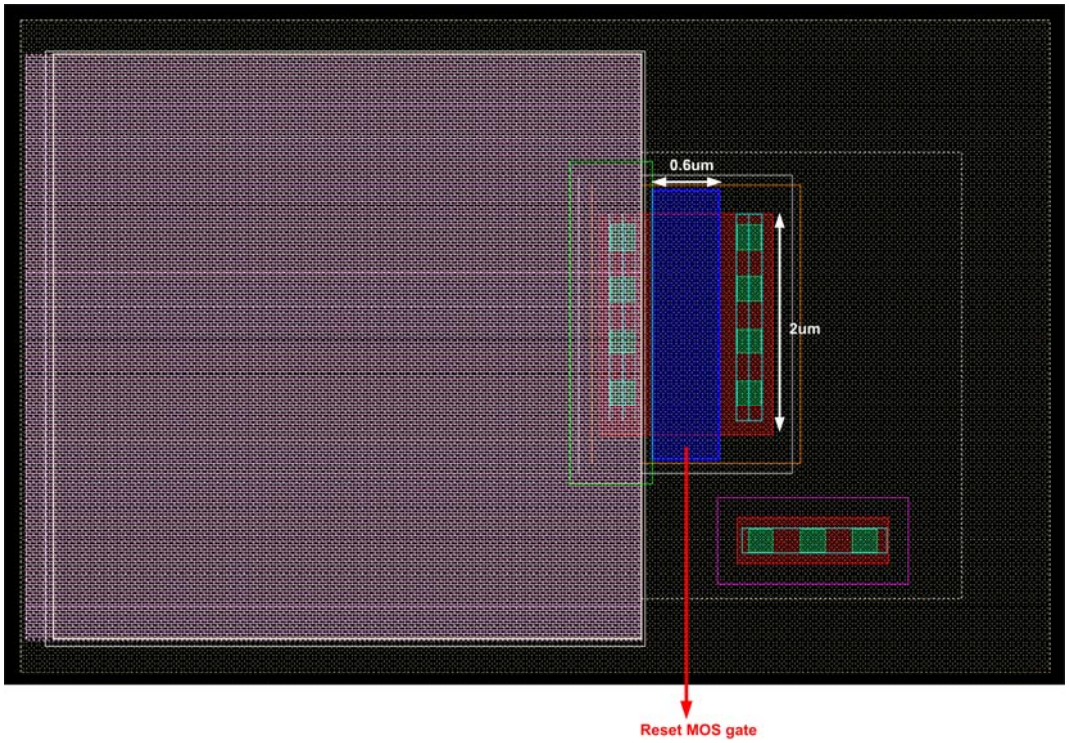


Figure 3.1 The 3T CMOS sensor pixel layout

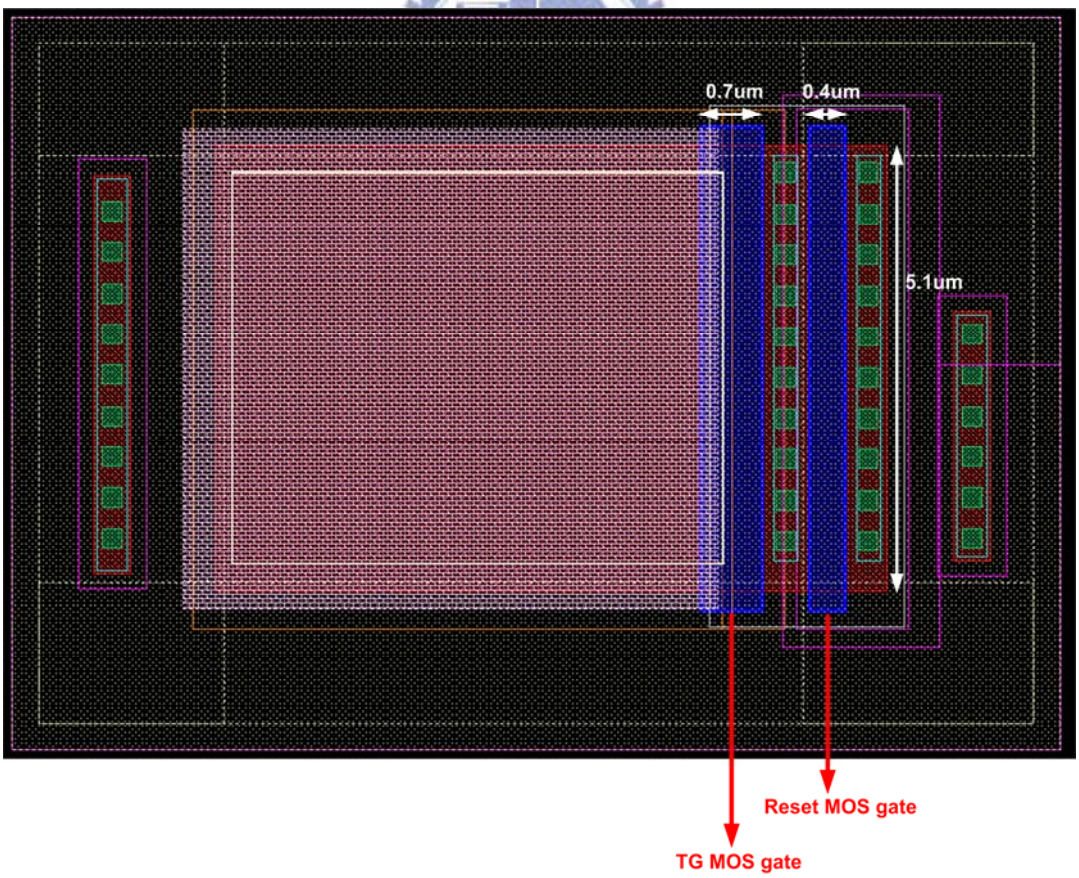


Figure 3.2 The 4T CMOS sensor pixel layout

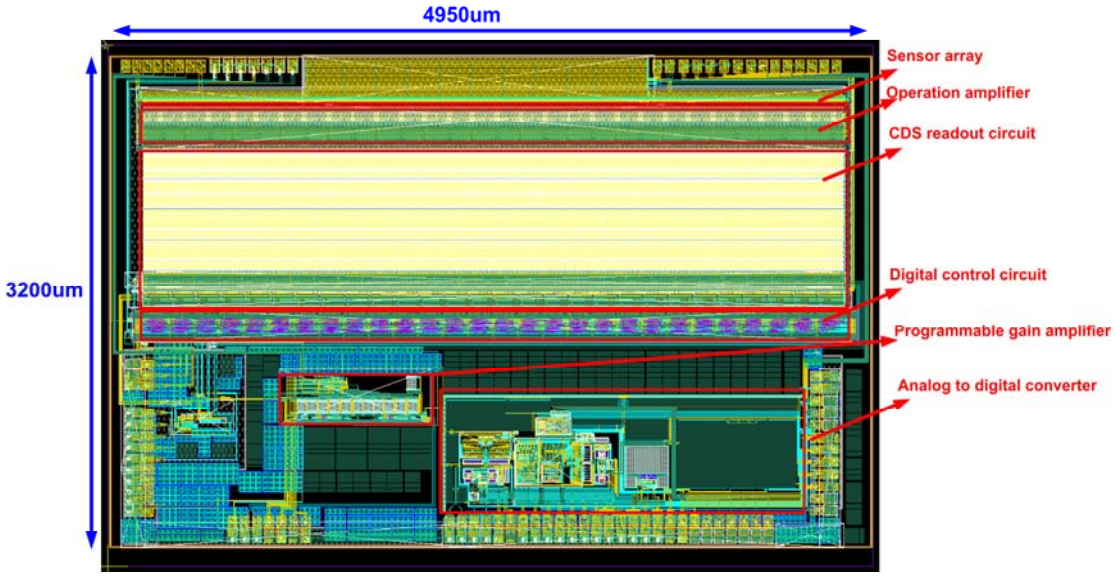


Figure 3.3 3T_full-chip layout

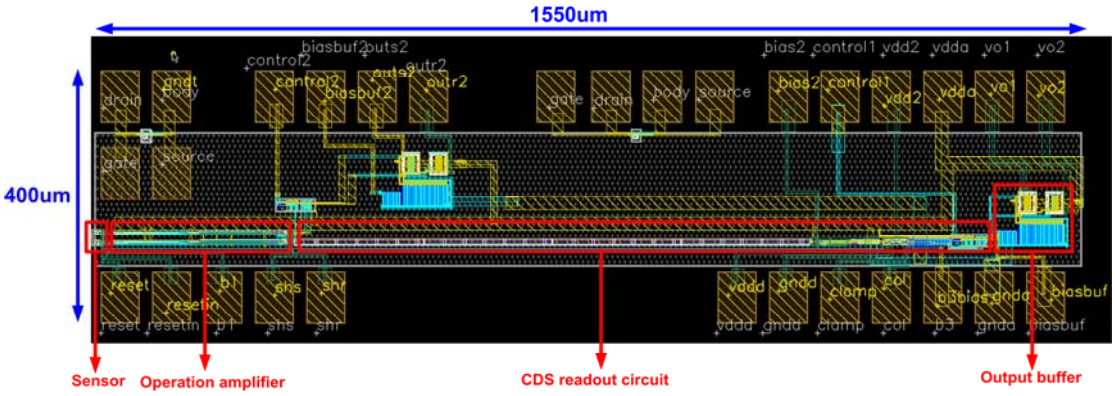


Figure 3.4 3T test-chip layout

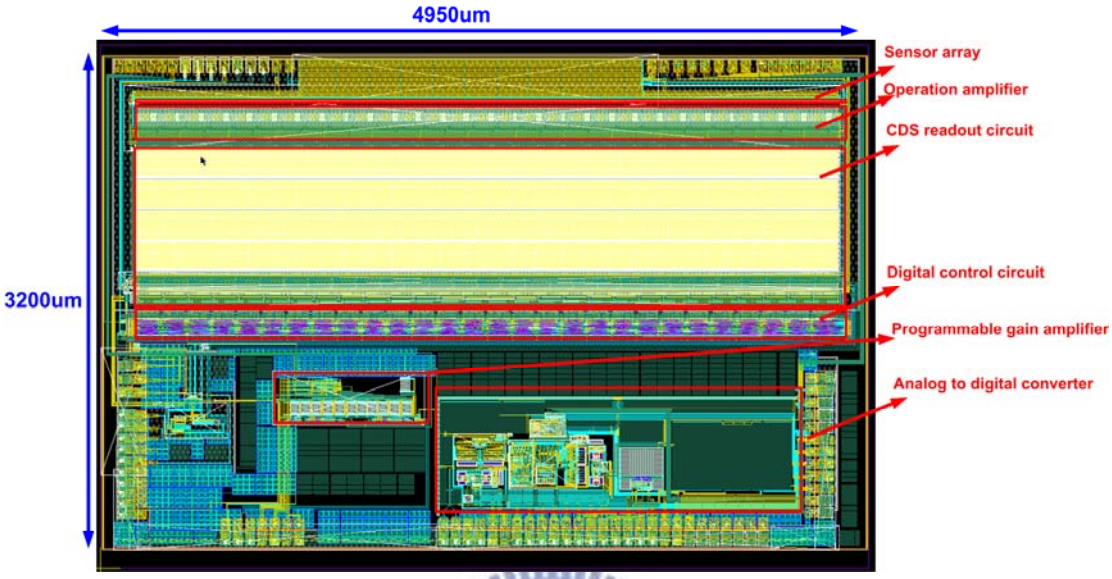


Figure 3.5　4T full-chip

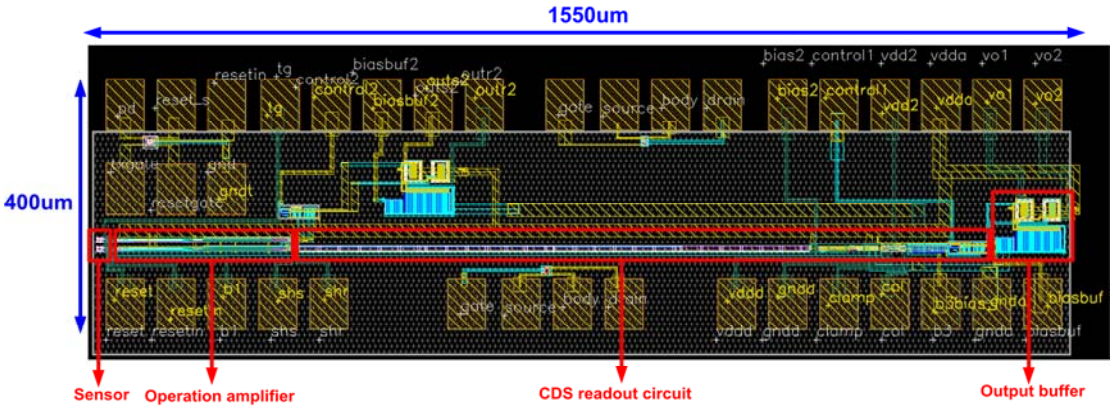


Figure 3.6　4T test-chip

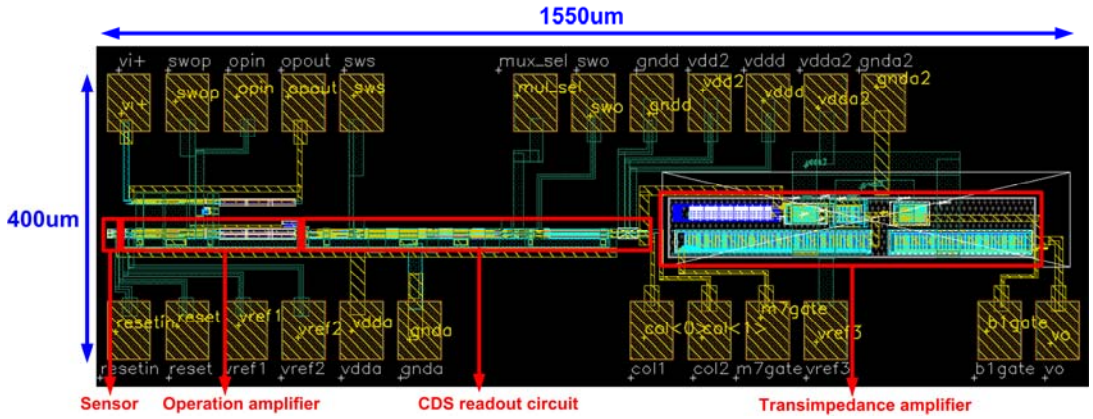


Figure 3.7 3T current mode sensor test-chip

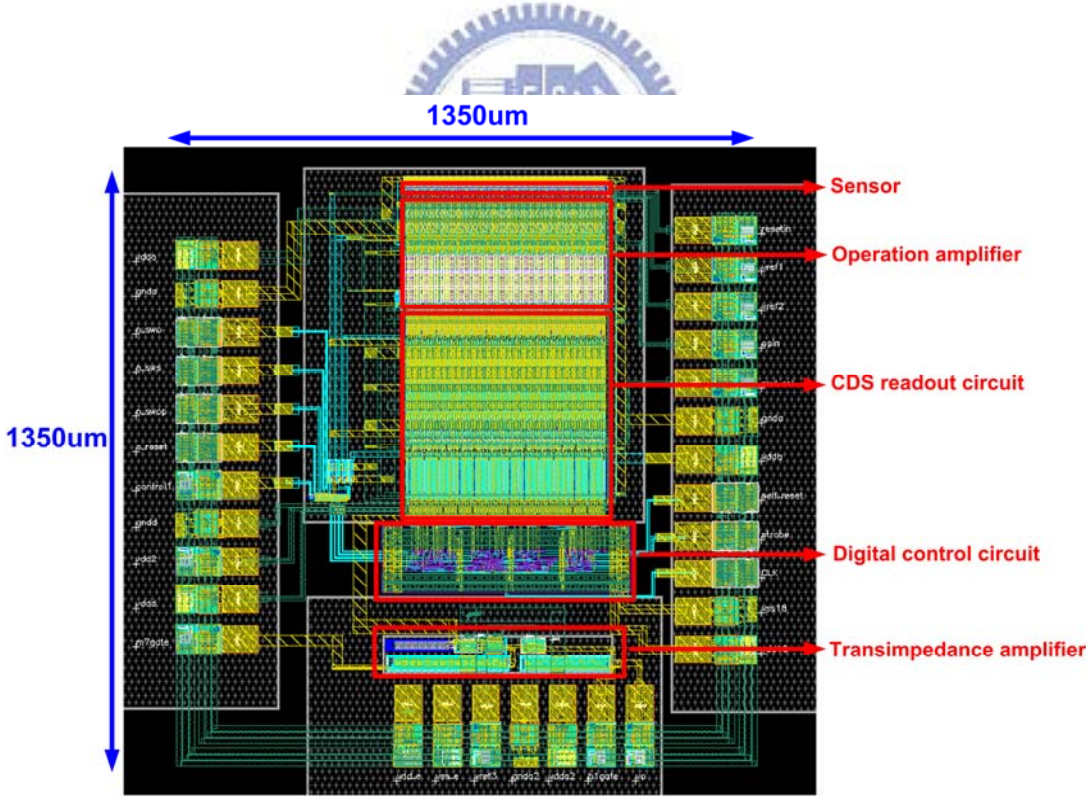


Figure 3.8 3T current mode sensor full-chip

3.2 Experimental environment

Fig. 3.9 shows the PCB design of 3T and 4T voltage mode sensor test-chip. The major DC bias voltage is provided by the regulator LM317. The Fig. 3.10 shows the PCB design of 3T and 4T voltage mode sensor full-chip, it includes the components of sensor, PGA and AD. The PCB designs of current-mode sensor chips are also be shown in Fig. 3.11 and Fig. 3.12. Fig. 3.13 shows the light source system of the measurement, it is composed of light integration sphere and power meter for the light integration sphere. It can provide stable and uniform light source as input signal. Fig. 3.14 shows the measurement environment setup. The clock and digital pattern are provided by the National Instruments Digital IO. The DC voltage is provided by the Agilent power supply. The light source is provided by the light source system as shown in Fig. 3.13. Besides, the Keithley source meter 2400 is used as an accurate power supply; it can provide stable bias voltage and measure current with very high precision. Final, the output of the chip is displayed by the Agilent oscilloscope.

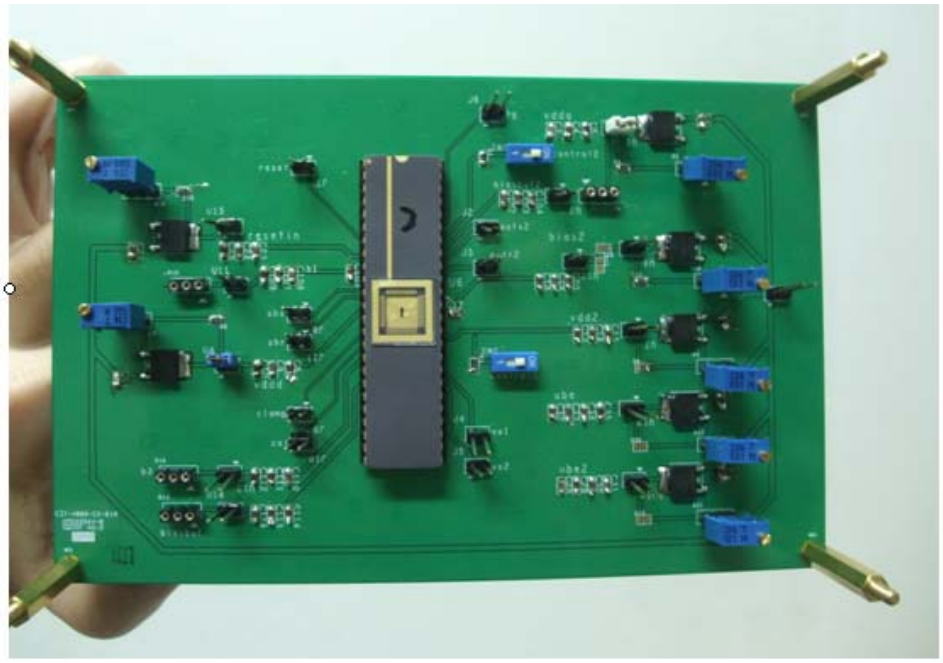


Figure 3.9 The PCB design of 3T and 4T voltage mode sensor test-chip

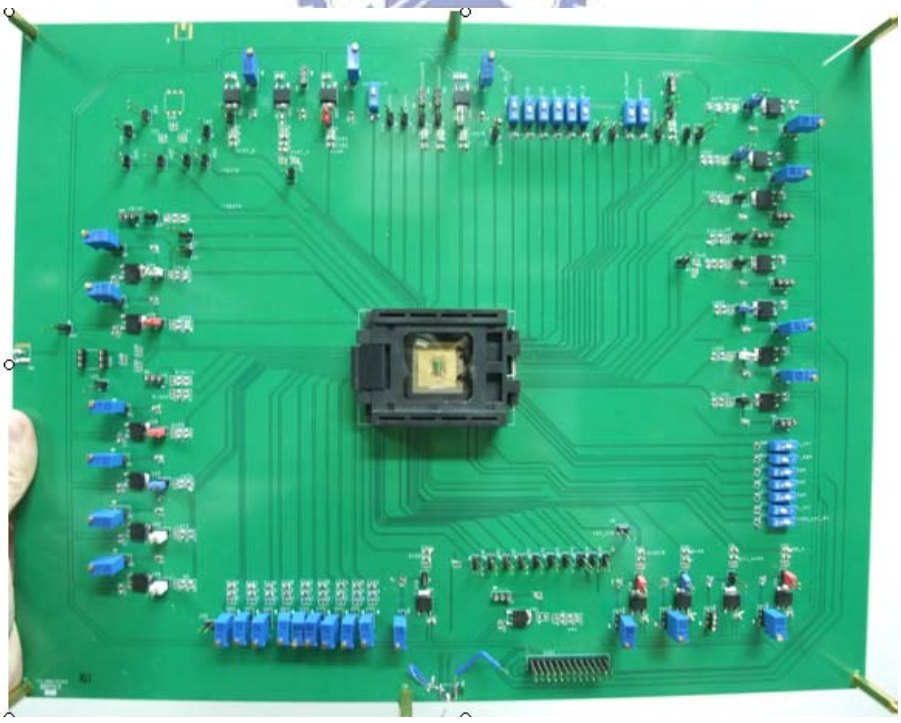


Figure 3.10 The PCB design of 3T and 4T voltage mode sensor full-chip

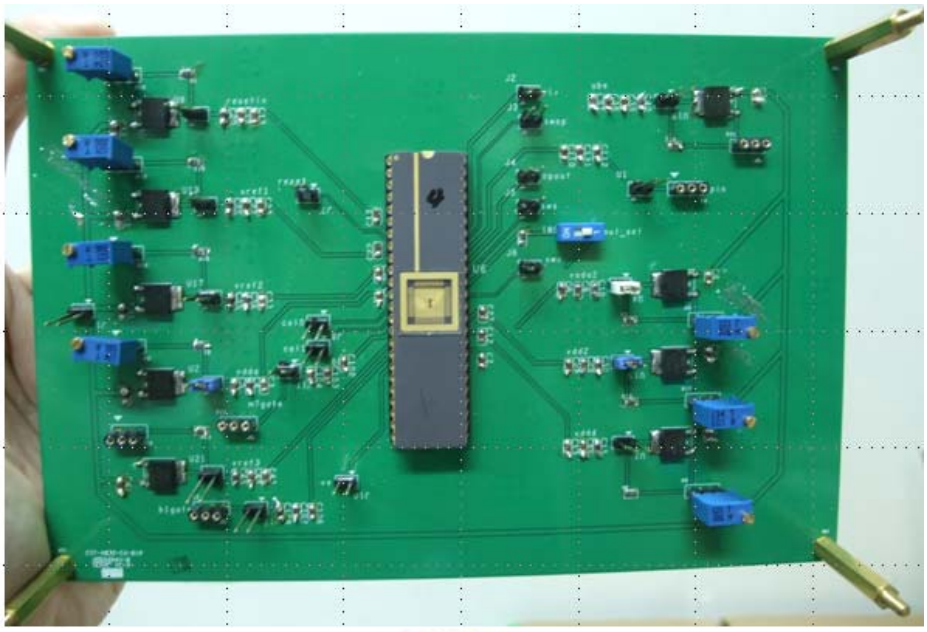


Figure 3.11 The PCB design of 3T current mode sensor test-chip

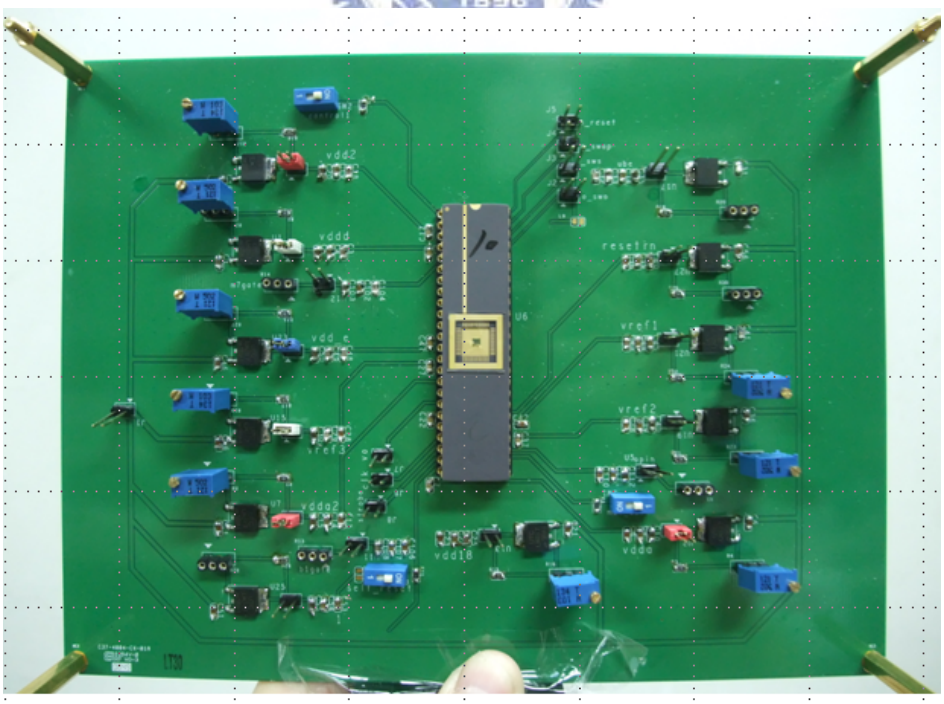


Figure 3.12 The PCB design of 68cell 3T current mode sensor

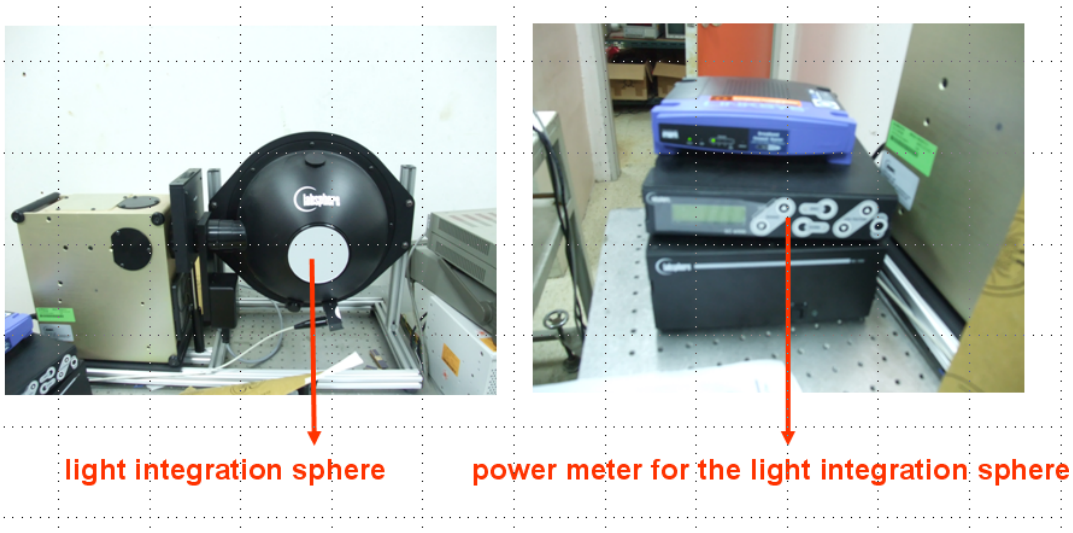


Figure 3.13 The light system

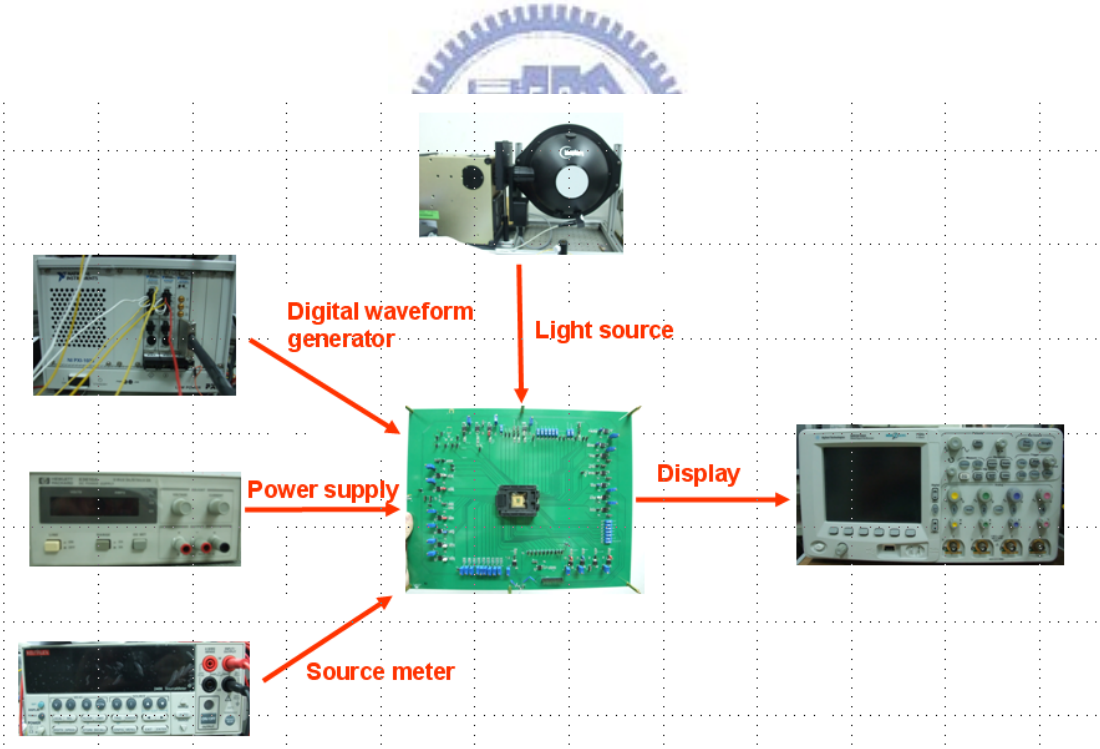


Figure 3.14 The measurement environment setup

3.3 Experimental results

3.3.1 Experimental results of voltage mode sensor

Fig. 3.15 shows the different integration waveform of the 3T CMOS sensor due to the different light intensity. After the reset signal pulse, the V_{pd} is reset to a certain voltage and starting to integrate. From Fig. 3.15 (a)~(e), we can find that the slope of the integration result rises when the light is from low light to high light. Fig. 3.15 (e) shows the saturation result of integration. The similar result of the 4T sensor is shown in the Fig. 3.16. After the reset signal pulse, the V_{pd} is reset to a certain voltage. Then, when the control signal TG is on, the integration charge would be transfer from the sensor node to the reset node. Fig. 3.17 shows the 3T sensor voltage output waveforms due to different incident light from dark to bright, and the saturation output is shown in Fig. 3.19. Fig. 3.18 shows the 4T sensor voltage output waveforms due to different incident light from dark to bright, and the saturation waveform is shown in Fig. 3.20. Fig. 3.21 shows the 3T full-chip measurement result of different incident light power versus different output voltage. It shows good linearity as 98.71%. The linearity is calculated by the R^2 function of Microsoft Excel. Fig. 3.22 shows the 4T full-chip measurement result of different incident light power versus different output voltage. Fig. 3.23 shows the comparison of 3T and 4T full-chip measurement result of different incident light power versus different output voltage. Fig. 3.24 shows the 3T test-chip measurement result of different incident light power versus different output voltage. It shows good linearity as 98.88%. Fig. 3.25 shows the 4T test-chip measurement result of different incident light power versus different output voltage. Fig. 3.26 shows the comparison of 3T and 4T test-chip measurement result of different incident light power versus different output voltage. The Fig. 3.27

shows the fixed pattern noise measurement results for the five different light. The fixed pattern noise in this voltage mode sensor is about +2.73% and -2.7%. The Fig 3.30 shows the different incident light power versus output voltage for the comparison of 3T, 4T full-chip and test-chip sensors. The Fig.3.31 shows the demo result of the voltage mode sensor. The left screen is the original image, and the right screen is the sensing image. The 1-D sensor senses the moving image, and then the ADC converts the sensing signal to digital signal. Finally, the 1-D sensed images are combined to a complete picture by the digital process. Fig.3.32 shows the other demo result of the voltage mode sensor. The left screen is the original image, and the right screen is the sensing image.

From Fig. 3.23 and Fig. 3.26, we can observe that the sensitivity of 3T CMOS sensor is higher than that in the 4T sensor. The analysis of the mentioned result is shown as following. From Fig. 3.28, we can have

$$\Delta V_{pd} = \frac{\Delta I_{3T\_sensor} \times t}{C_{M\_reset} + C_{photodiode} + C_{op}} \quad \textbf{(3-1)}$$

From Fig. 3.29, we can have

$$\Delta V_{pd} = \frac{\Delta I_{4T\_sensor} \times t}{C_{M\_reset} + C_{M\_TG} + C_{op}} \quad \textbf{(3-2)}$$

As shown in Fig. 3.1 and Fig. 3.2., the dimension of 3T reset MOS sensor is 2um/0.6um. The dimension of 4T reset MOS sensor is 5.1um/0.4um, and that for the transfer MOS is 5.1um/0.7um. From above, we can find that the parasitic capacitor of 4T sensor is indeed bigger than 3T sensor. The sensitivity of 3T CMOS sensor is

better than 4T CMOS sensor since that the dimension of 4T reset MOS and TG MOS is much bigger than 3T reset MOS.

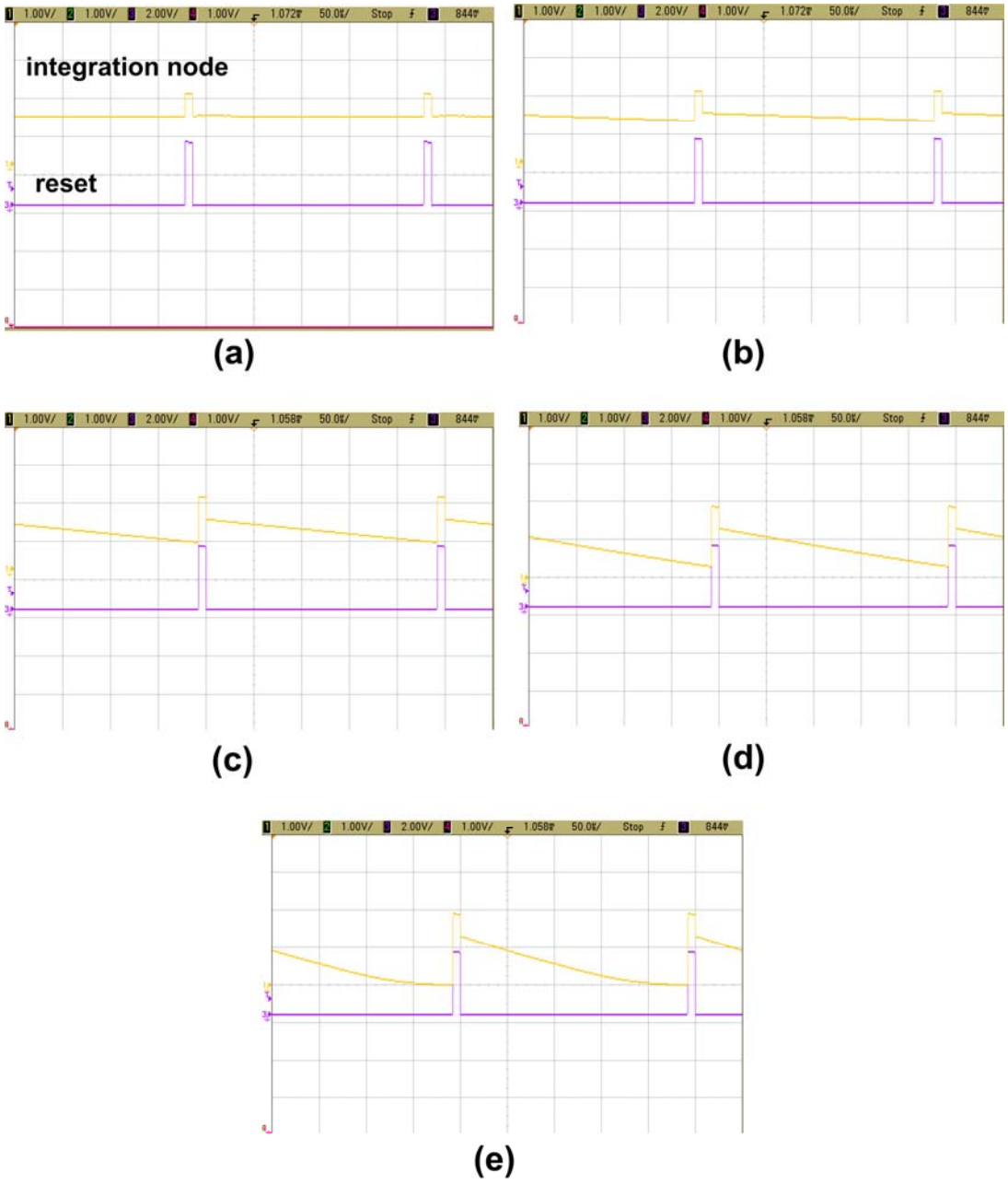


Figure 3.15 (a)~(e) The 3T sensor integration wave for different light from low light to high light

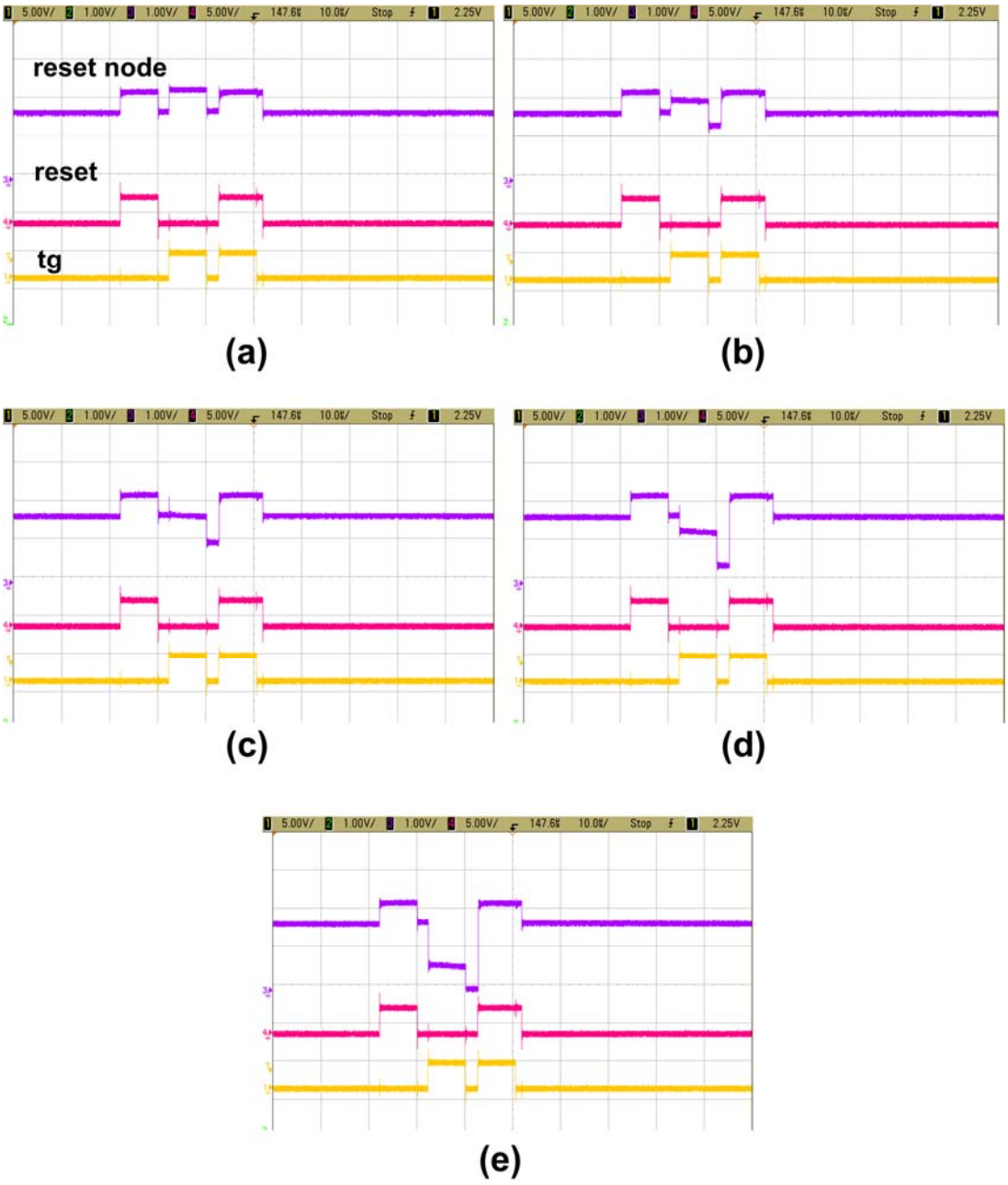


Figure 3.16 (a)~(e) the 4T sensor integration wave for different light from low light to high light

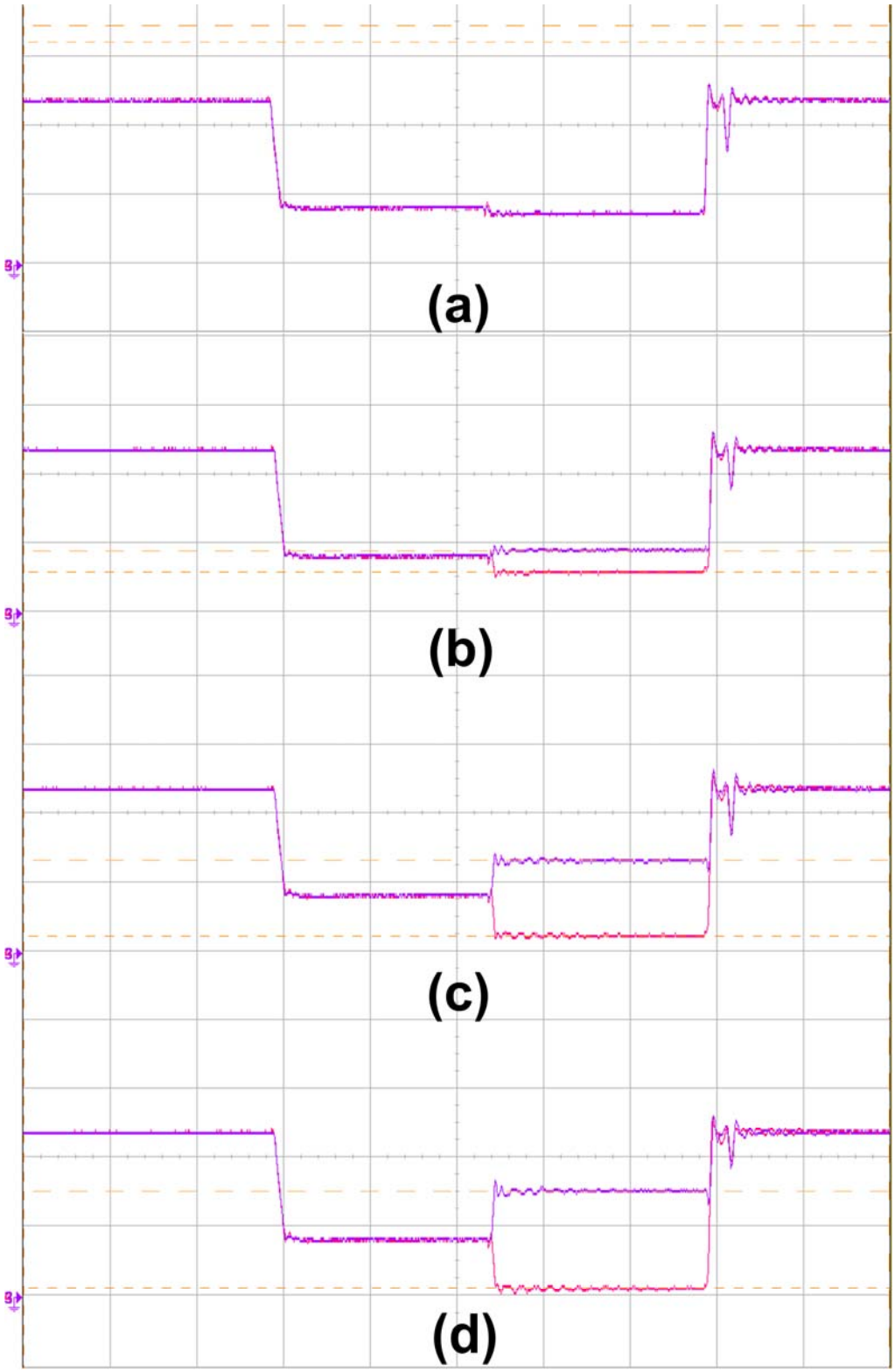


Figure 3.17 (a)~(d) the 3T sensor output wave for different light from low light to high light

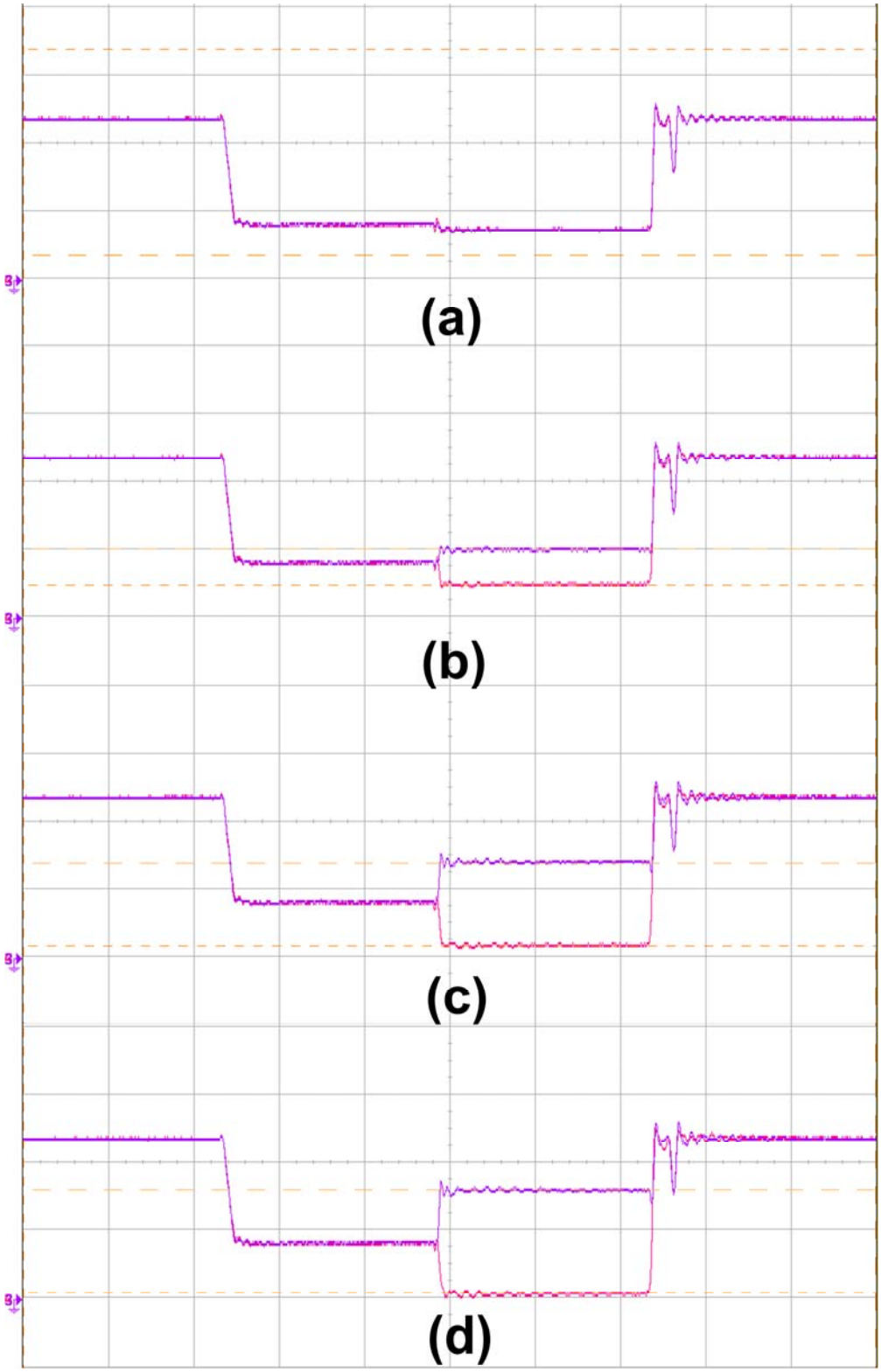


Figure 3.18 (a)~(d) The 4T sensor output wave for different light from low light to high light

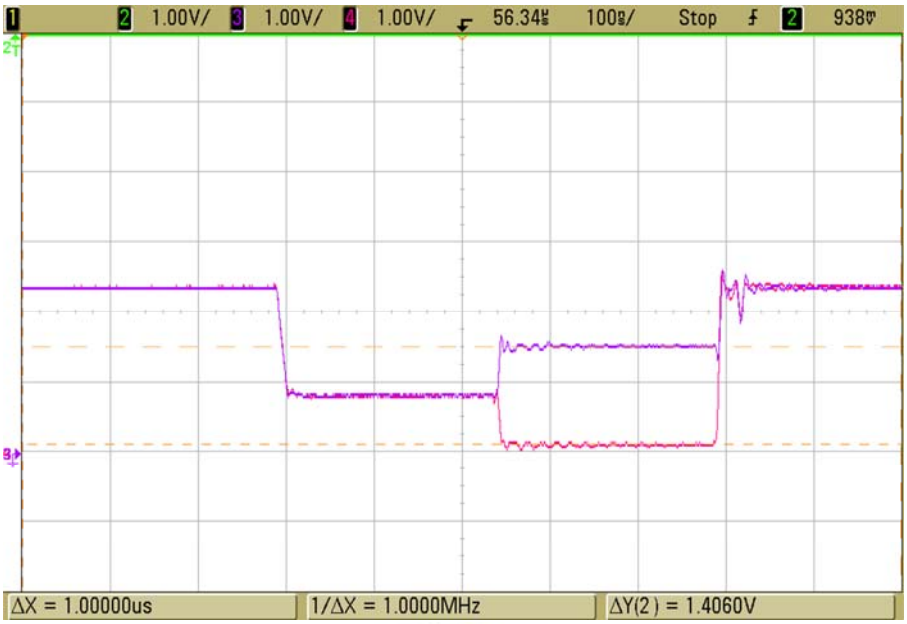


Figure 3.19 The 3T sensor saturation output waveform

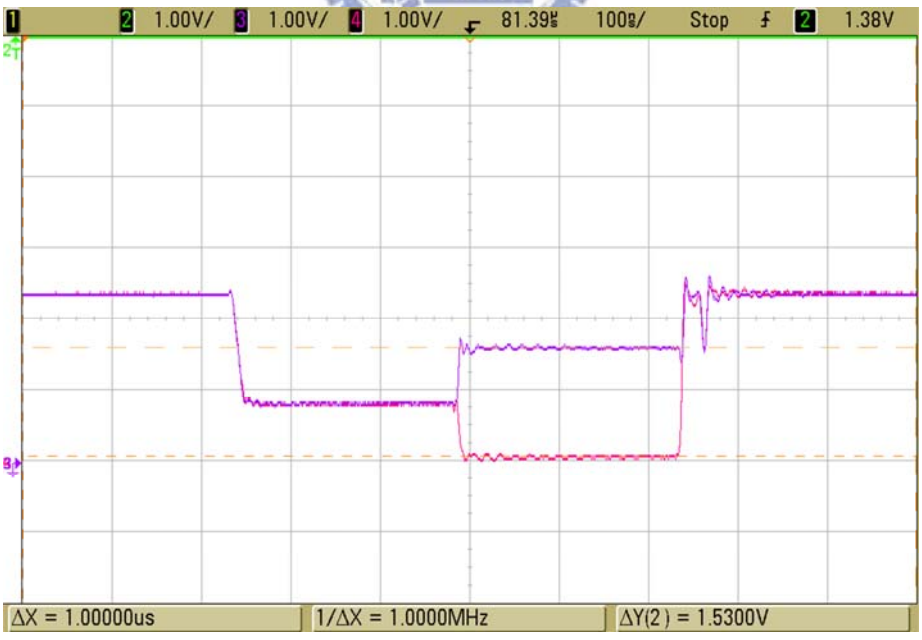


Figure 3.20 The 4T sensor saturation output waveform

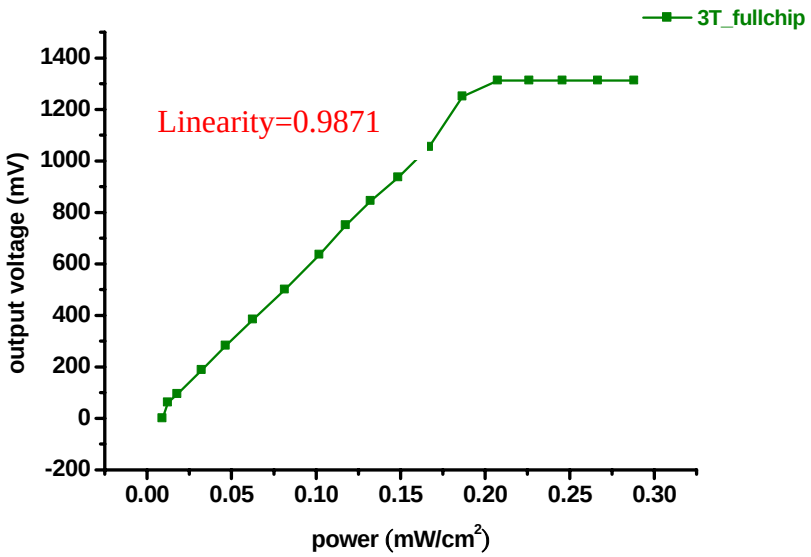


Figure 3.21 The different incident light power versus output voltage for the 3T full-chip sensor

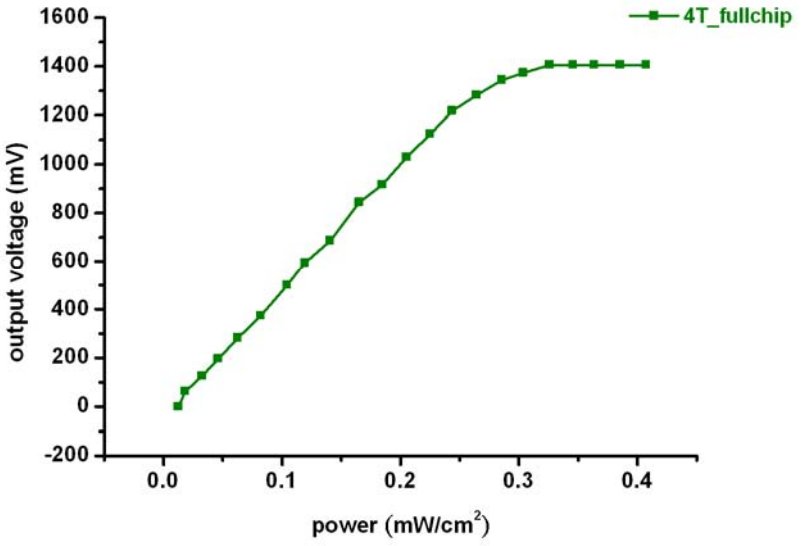


Figure 3.22 The different incident light power versus output voltage for the 4T full-chip sensor

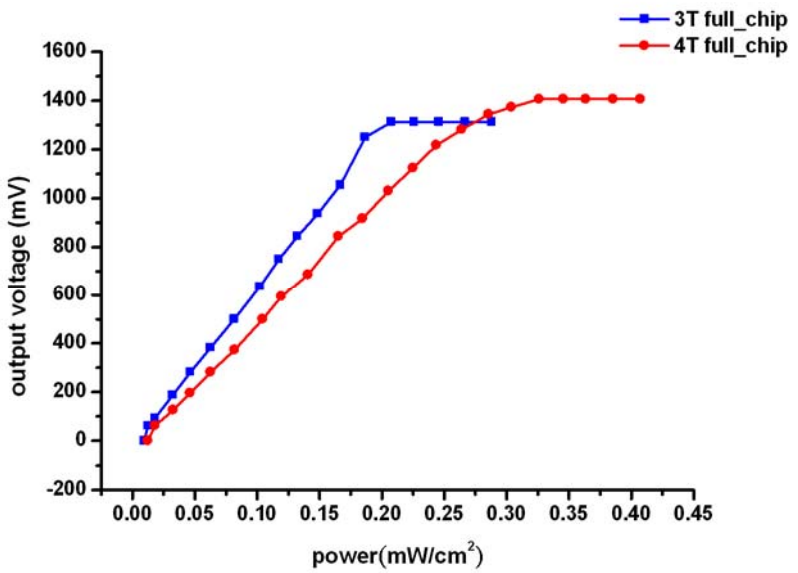


Figure 3.23 The different incident light power versus output voltage for the comparison of 3T and 4T full-chip sensors

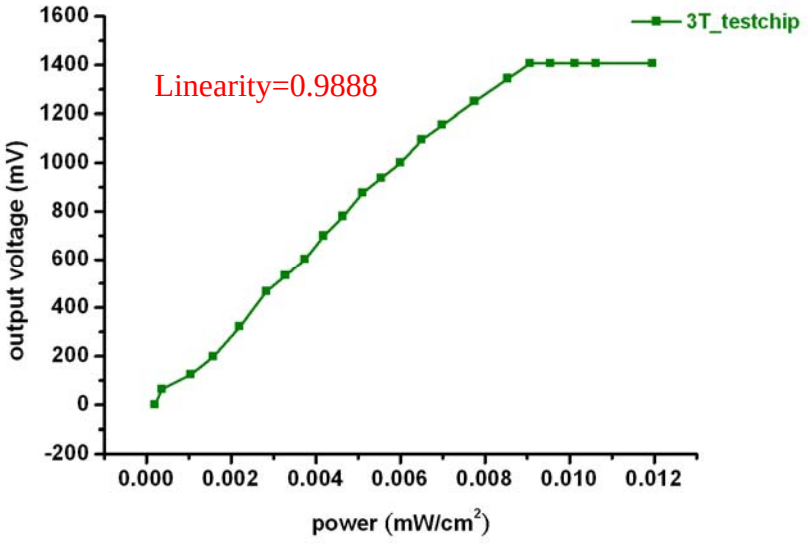


Figure 3.24 The different incident light power versus output voltage for the 3T test-chip sensor

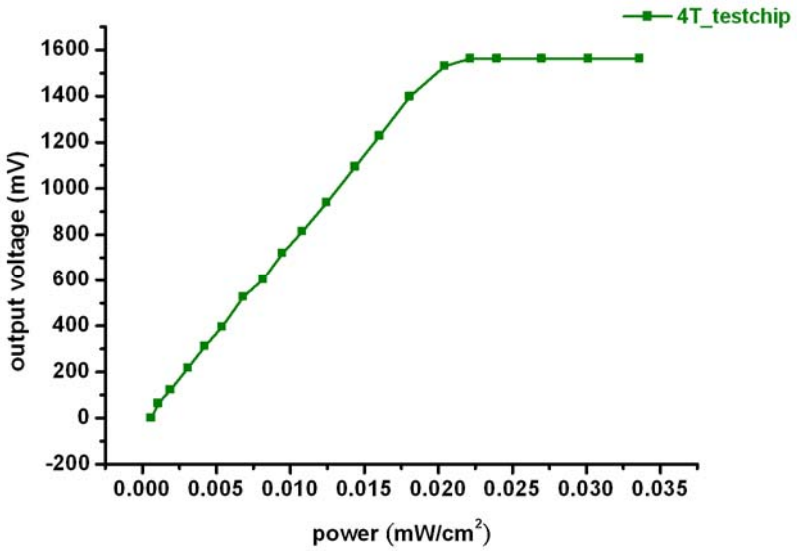


Figure 3.25 The different incident light power versus output voltage for the 4T test-chip sensor

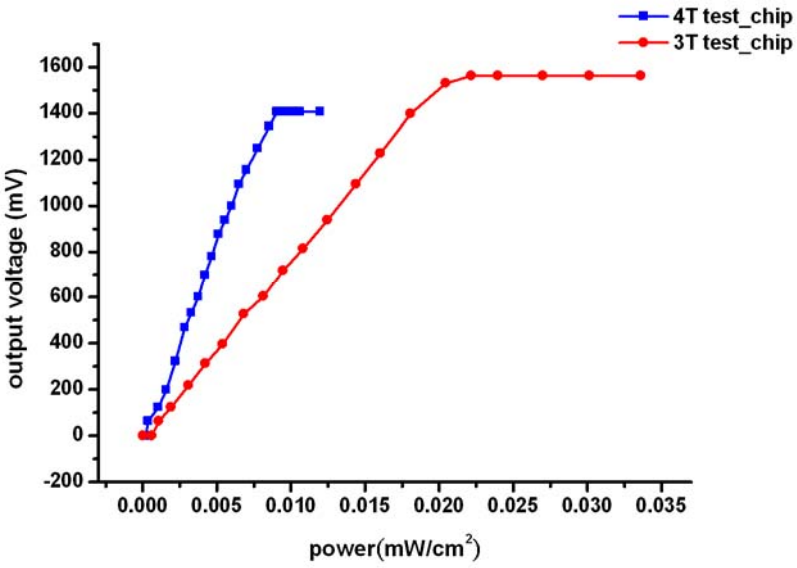


Figure 3.26 The different incident light power versus output voltage for the comparison of 3T and 4T test-chip sensors

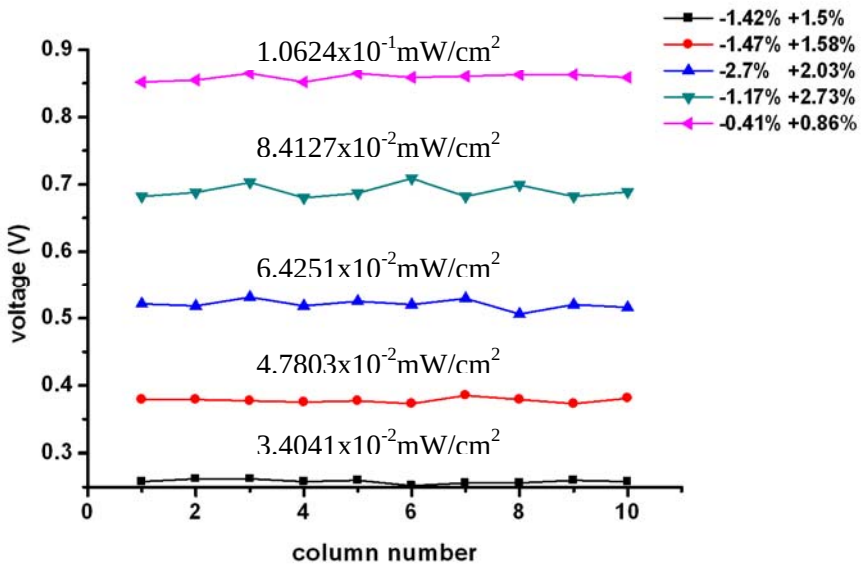


Figure 3.27 The fixed pattern noise measurement for different incident light

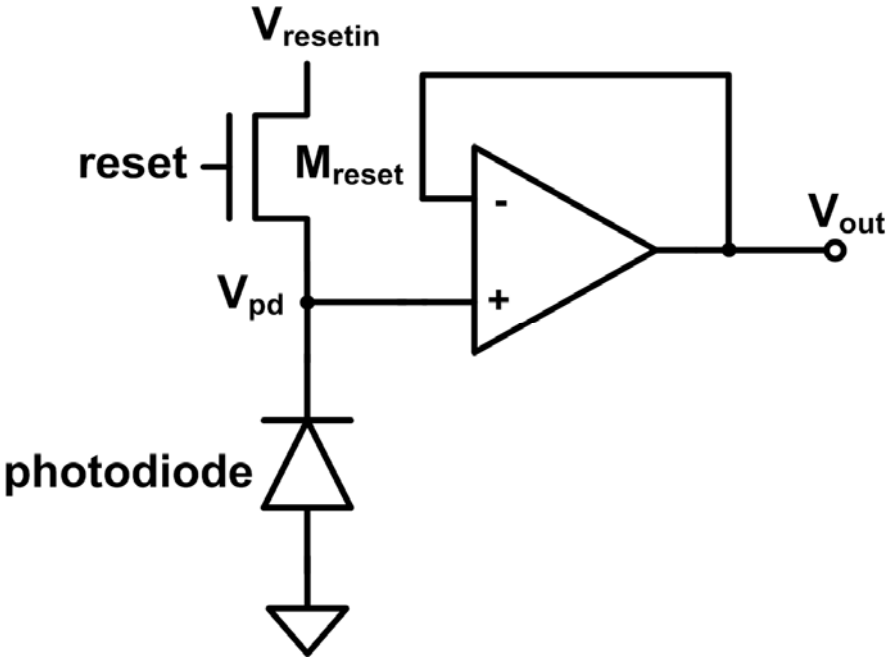


Figure 3.28 The 3T sensor pixel

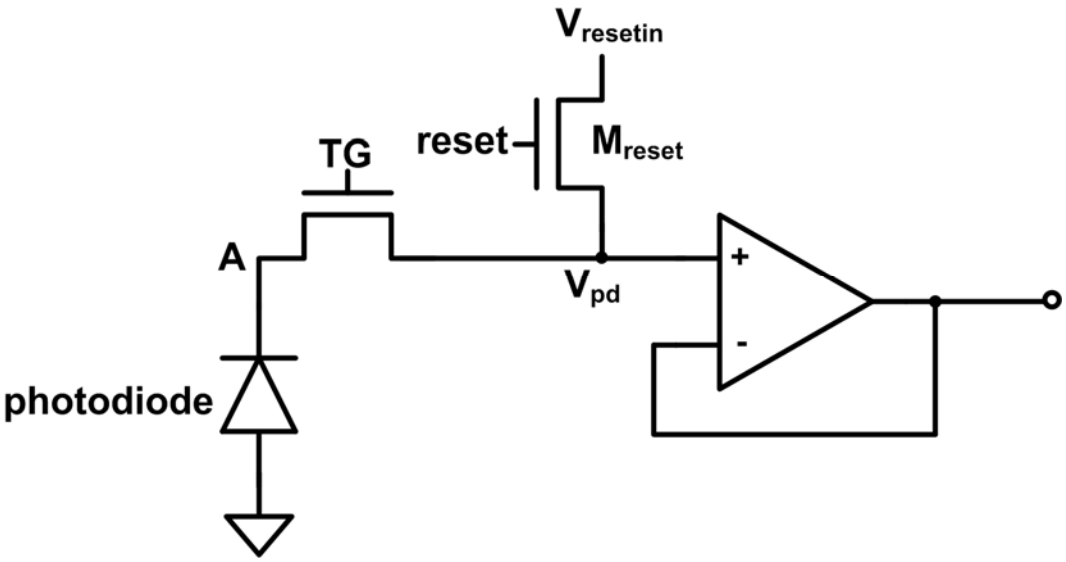


Figure 3.29 The 4T sensor pixel

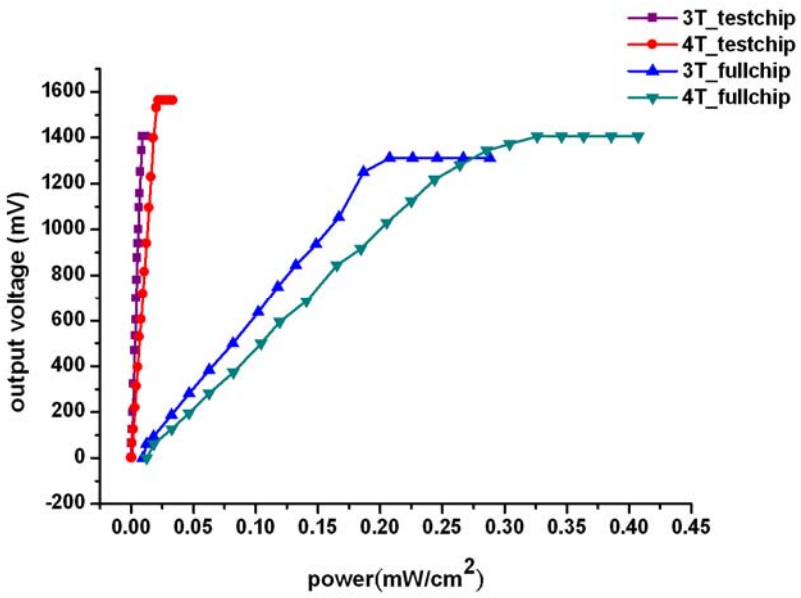


Figure 3.30 The different incident light power versus output voltage for the comparison of 3T, 4T full-chip and test-chip sensors

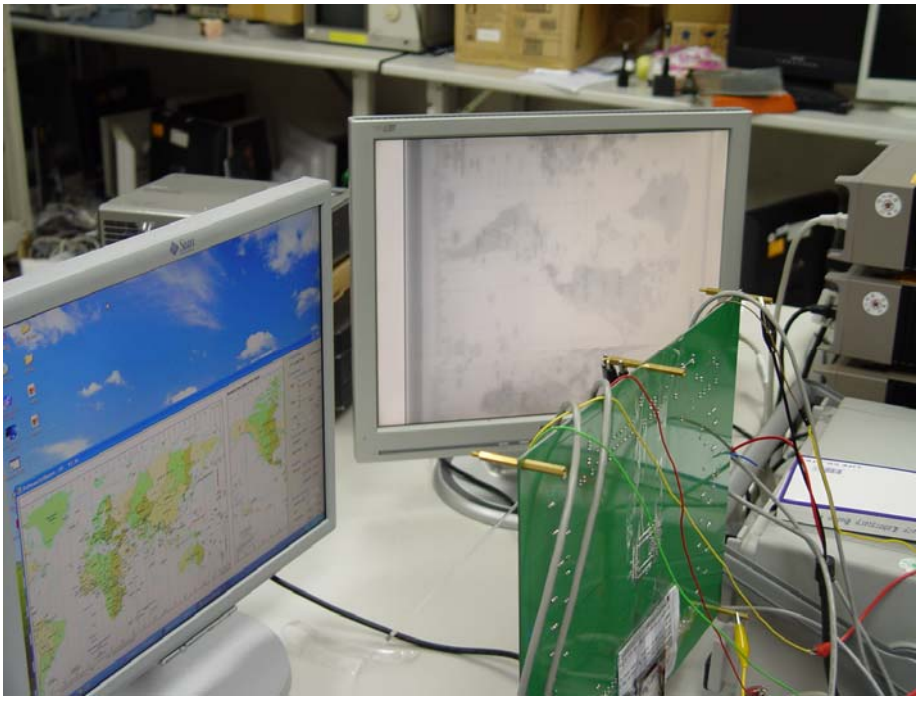


Figure 3.31 The demo result-1 of the voltage mode sensor

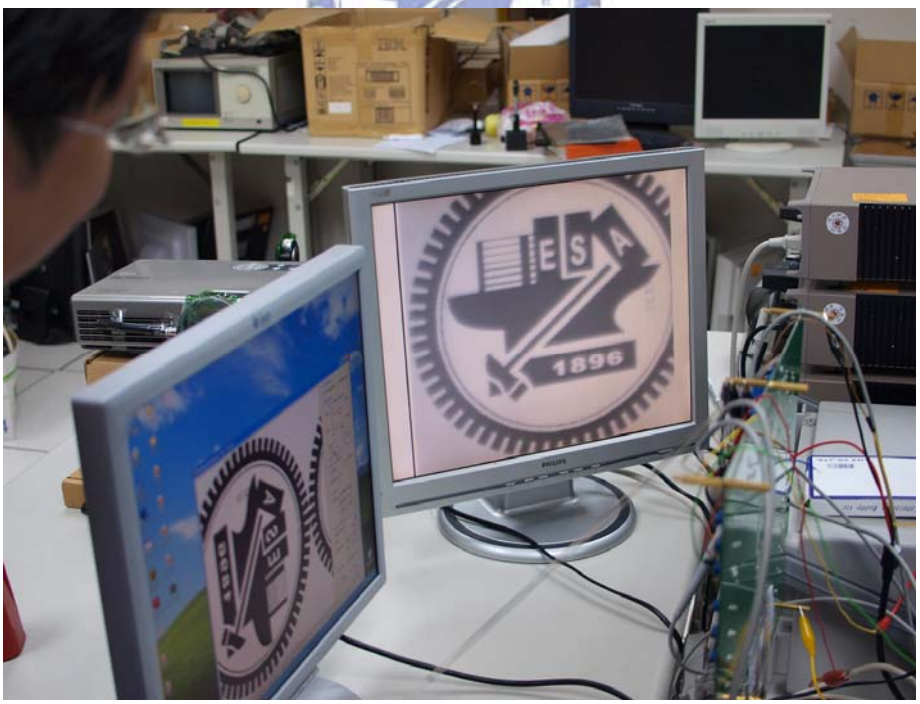


Figure 3.32 The demo result-2 of the voltage mode sensor

3.3.2 Experimental results of current mode sensor

The Fig. 3.33 shows the two columns measurement results of current mode sensor when the V_{ds} is 0.05V. The x-axis represents the different power due to different incident light, and the y-axis represents the corresponding output voltage. The Fig. 3.34 shows the same result with Fig. 3.33 when the V_{ds} is 0.05V. The saturation output voltage is concerned with the V_{ds} of the active device since the output current is controlled by the V_{ds}. The Fig. 3.35 shows the different saturation output with different V_{ds}. Fig. 3.36 shows the comparison result when V_{ds} are 0.1V and 0.05V. The measured front-end gain with different V_{sd} tuned by V_{ref1} is shown in Fig. 3.37. It shows a programmable current gain with a high linearity as 99.88%. The same result of col2 is shown in Fig. 3.38, and the linearity of col2 is 99.67%. The Fig. 3.39 shows the measurement result of the Vds versus output voltage with the multiple gain option. The Fig. 3.40 shows the fixed pattern noise measurement results for the three different light. The fixed pattern noise in this current mode sensor is about +12.2% and -10.2%. Due to the gain mismatch, the output voltage under different incident light have the same variation pattern.

From Fig. 3.33 the output of col1 and col2 is not the same in the same light intensity. Due to the mobility degradation, the CDS can't eliminate the fixed pattern noise completely as shown in Fig. 3.33. Equation 3-33 shows the current output after CDS operation.

$$I_{out} = \frac{\mu_0}{1+\theta(V_{sg}-|V_t|)} C_{ox} \frac{W}{L} (V_{reset} - V_{sig}) V_{sd} \qquad (3\text{-}33)$$

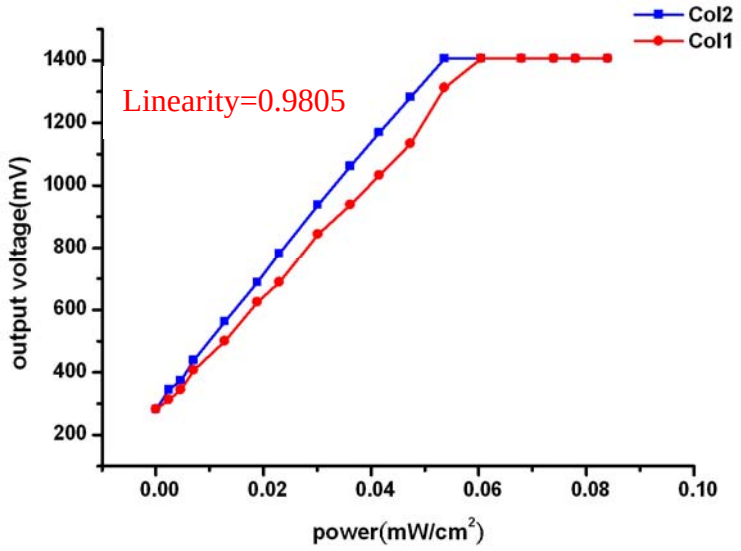


Figure 3.33 the different incident light power versus output voltage when the V_{ds}=0.05V

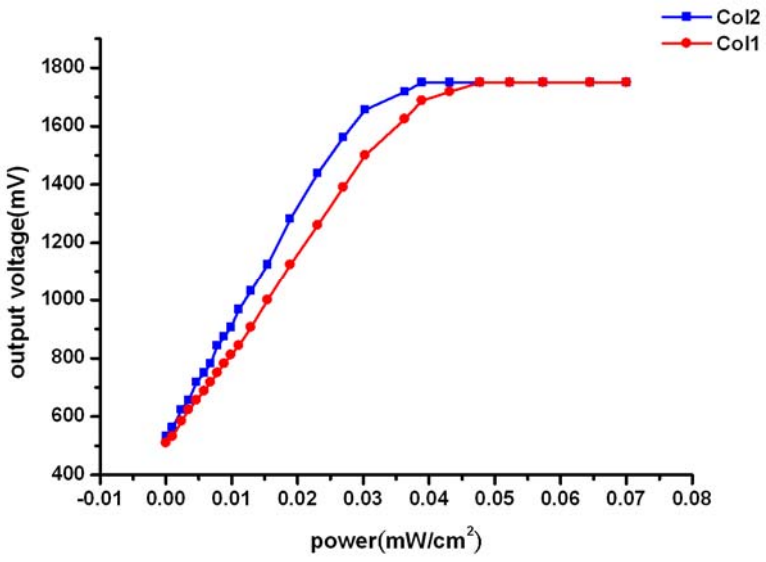


Figure 3.34 the different incident light power versus output voltage when the V_{ds}=0.1V

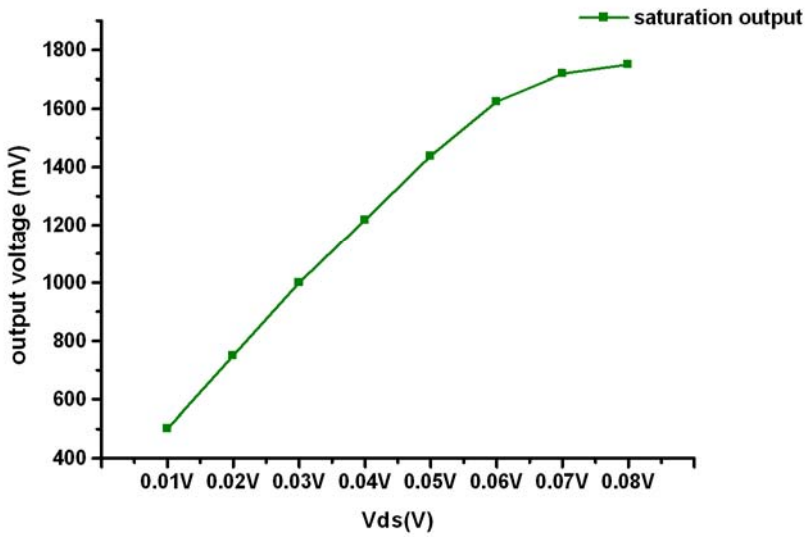


Figure 3.35 the different V_{ds} versus different saturation output voltage with the same strong light

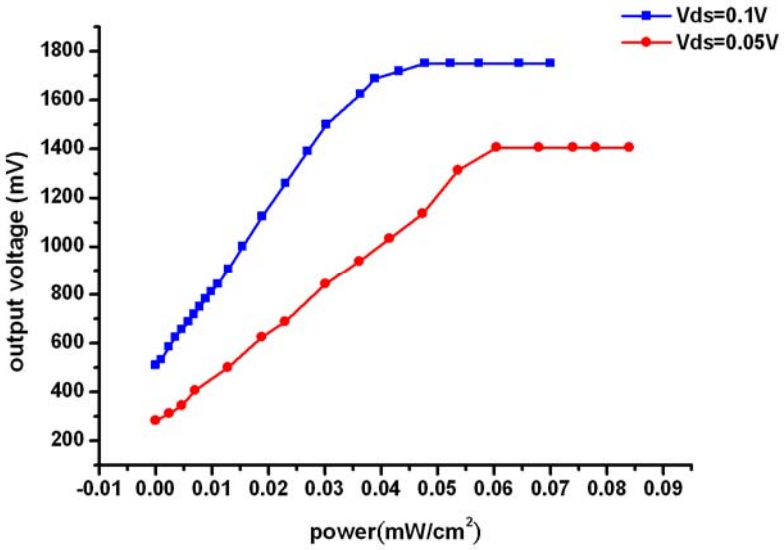


Figure 3.36 the different incident light power versus different output voltage

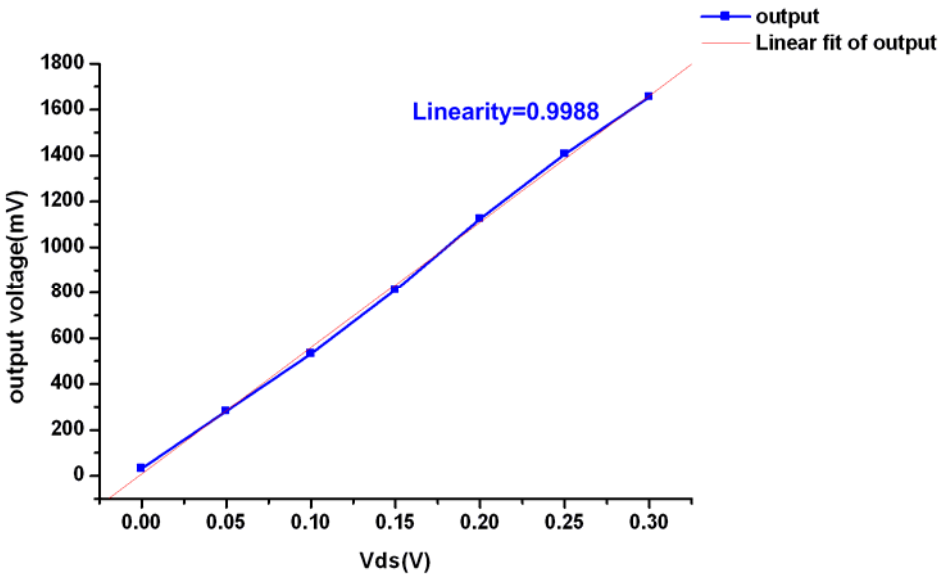


Figure 3.37 the Vds versus output voltage for col1

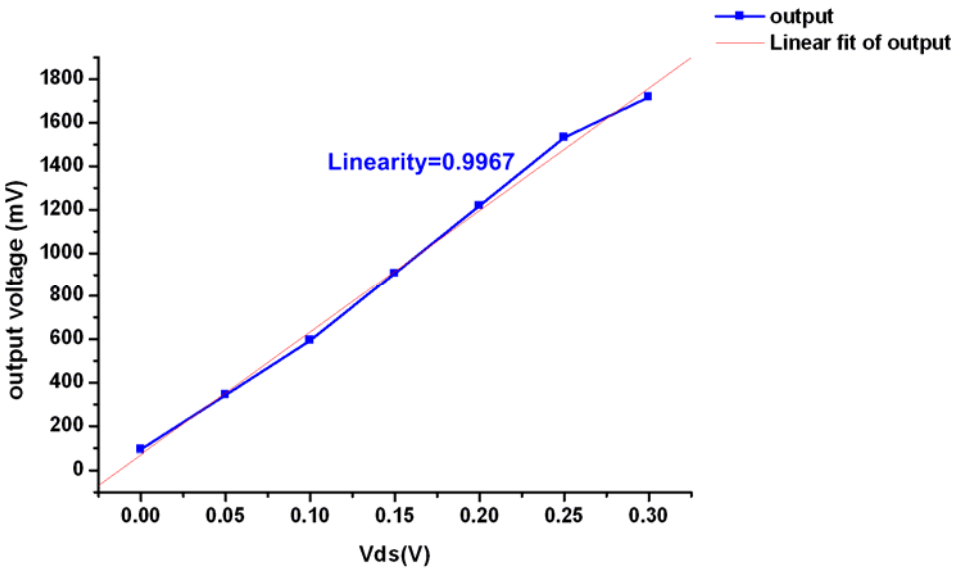


Figure 3.38 the Vds versus output voltage for col2

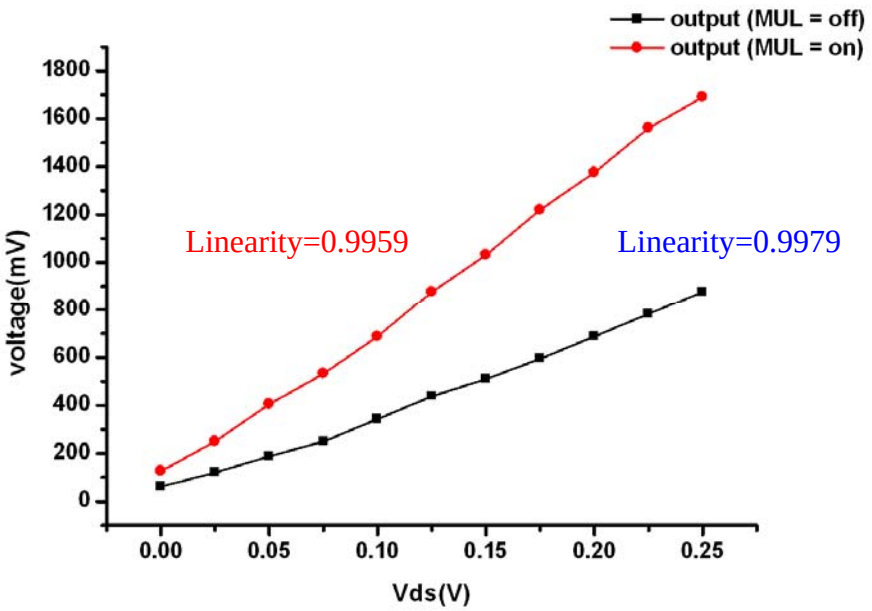


Figure 3.39 The measurement result of V_{sd} versus output voltage with multiple-gain option controlled by Mul.

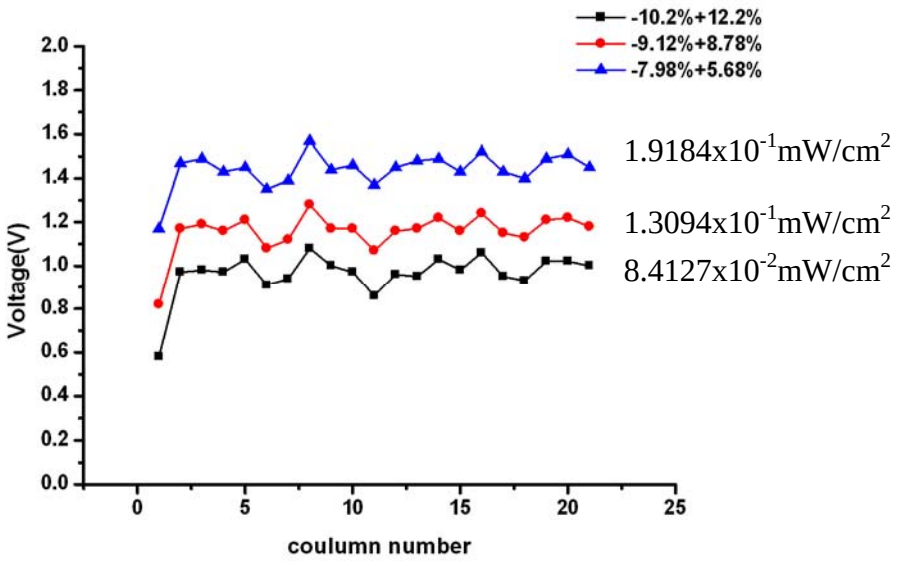


Figure 3.40 The fixed pattern noise measurement for different incident light

	3T fullchip	4T fullchip
Pixel number	**1x704**	**1x704**
Pixel size	**6.5um**	**6.5um**
Sensing area	**4576**	**4576**
Signal swing (full-well capacity)	**1.3V~2.8V**	**-**
Saturation output voltage	**1.312V**	**1.406V**
Saturation exposure	**0.3604 lux.s**	**0.4644 lux.s**
Responsibility	**3.64 V/lux.s**	**3.03 V/lux.s**
Frame rate	**8000**	**8000**
Integration time	**120us**	**120us**
Fix pattern noise (power=$6.4251x10^{-2}$)	**(+2.73% / -2.7%)**	**(+2.73% / -2.7%)**
Power consumption	**27mW**	**27mW**

Table VI. The measurement result of voltage mode sensor

	Current mode sensor
Pixel number	**1x68**
Pixel size	**6.5um**
Signal swing (full-well capacity)	**0~2V**
Saturation output voltage	**1.75V**
Fixed pattern noise (power=$8.4127x10^{-2}$)	**(+12.2%, -10.2%)**
Gain linearity	**99.59%**
Gain	**X1~X10**
linearity	**98.05%**
Frame rate	**4000**
Integration time	**120us**

Table VII. The measurement result of voltage mode sensor

Chapter4
Conclusion and future work

4.1 Conclusion

4.1.1 Conclusion of voltage mode sensor

The voltage mode readout circuits with 3T version and 4T version of CMOS sensors are designed and analyzed. The operation amplifier is used to replace the traditional source follower in the 3T sensor pixel, so that can enhance the linearity and reduce fixed pattern noise error. The linearity of the sensor output is near 98.71, and the fixed pattern noise is +2.73 and -2.7% when the input optical power is 6.4251×10^{-2} mW/cm^2. It shows a good readout performance with high linearity and low fixed patterned noise. The 3T version of CMOS sensor was fabricated with TSMC 0.18 um 1P3M 3T sensor process, and the 4T version of CMOS sensor was fabricated with TSMC 0.18 um 1P3M 4T sensor process. The pixel sizes of the 3T and 4T version of sensors are implemented with 6.5um. The linear output voltage versus different incident is measured. Additionally, the performance of measurement result for the 3T and 4T sensor is measured and compared. Finally, the image system is implemented and the sensing image results are shown.

4.1.2 Conclusion of current mode sensor

A current mode readout circuit for CMOS sensor including gain pixel and the multiple-gain device is proposed, fabricated and measured. A programmable front-end gain and additional multiple-gain option are implemented to solve the design tradeoff

between the signal gain and swing. It shows a good readout performance with high gain, high linearity, high swing and low power. The proposed circuit operates with no dc path and consumes less power than the other circuits. The SNR in the low light level can also be improved. The proposed design is suitable for the linear CMOS image sensor and two-dimensional sensor array as well. The current mode sensor is fabricated with TSMC 0.18 um 1P3M 3T sensor process, and the pixel size is 6.5um. The linearity of the current mode sensor output tuned by Vsd is measured and proved as 99.59%. The fixed pattern noise of the current mode sensor is -10.2% and +12.2% when the input optical power is 8.4127×10^{-2} mW/cm^2. The good linearity of the tunable gain controlled by V_{sd} is measured and proved. The comparison of current mode sensor and voltage mode sensor is shown in table VIII.

4.2 Future works

In this thesis, the voltage mode and current mode sensor and readout circuits are fabricated and measured. They show the linear response to the light. To the current mode sensor, the current mode analog to digital converter is needed to be design to complete the current mode sensor system, and the gain error is needed to be solved. To the voltage mode sensor, the area of the MIM capacitor is too huge to reduce the overall area. We must reduce the use of MIM capacitor.

	Current mode sensor	Voltage mode sensor
Full-well capacity	◎	
Programmable gain	◎	
ADC-complexity	◎	
Fixed pattern noise		◎
Arithmetic operation	◎	

Table VIII. The comparison of voltage mode sensor and current mode sensor

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