國立交通大學

電機與控制工程系

碩士論文

單迴路積分三角類比數位轉換器之積分器充電雜訊與諧波功率模型

Analytical Settling Noise and Distortion Power Models of Sigma-Delta ADCs

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摘要

交換式電容積分器是積分三角轉換器中基本的建構成份。其電容不完全的充放電轉換特性(積分器充放電問題)爲積分三角轉換器中一個主要影響輸出誤差的來源。而因爲積分器充放電問題的高複雜性,相關的誤差和失真的解析模型實際上是不存在的。在此篇論文中,我們的目的在於經由非線性擬合方法和輸出端頻譜預測技術來分析積分器充放電問題。由上法,積分器充放電問題誤差和失真的封閉解可獲得,且可使用積分三角轉換器中的系統參數來組成函數以呈獻出來。同時我們使用了行爲層的模擬以及 HSPICE 電路的模擬來驗證此解析模型的正確性,驗證結果顯示出我們的解析模型是足夠精確的。

Analytical Settling Noise and Distortion Power Models of Single-Loop Sigma-Delta ADCs

Student：Chun-Chieh Huang　　Advisor：Dr. Fu-Chuang Chen

Institute of Electrical and Control Engineering

Nation Chiao Tung University

ABSTRACT

Switch-capacitor (SC) integrator is the basic building component for sigma-delta (ΣΔ) modulators and its incomplete charge transfer (settling problem) constitutes one of the dominant error sources in ΣΔ modulators. Due to the complexity of settling problem, analytic models for related noises and distortions are virtually non-existent. In this paper, we aim to analyze the settling problems by employing nonlinear fitting methods and output spectrum prediction techniques. Closed forms of settling error and settling distortion models are obtained, and are represented as functions of ΣΔ modulator system parameters. Both behavior simulations and HSPICE circuits are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate.

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Symbols

V_{LSB}	Quantizer step size
V_{OS}	Maximum output swing of op-amp
OSR	OverSampling Ratio
n	Order of the Sigma-Delta modulator
B	Number of bits in the quantizer
f_S	Sampling Frequency
f_B	Signal Bandwidth
V_{ref}	Reference Voltage of the quantizer
A_0	Finite Gain of OTA
f_{in}	Frequency of the input signal
ϕ_i	ith phase of a nonoverlap clock
A_{in}	Amplitude of input signal
$\sigma_{jit.}$	standard deviation of clock jitter
C_S	Sampling capacitor
C_I	Integrating capacitor
C_L	Load capacitor of OTA
C_{Logic}	The loading capacitors of CMOS logic gates
C_{gate}	The gate capacitances of all CMOS transmission gates
C_{OX}	The capacitance per unit area of the gate oxide
V_S	Input signal plus feedback DAC signal
τ_1	Time constant of input branch
σ_{VS}	Standard deviation of V_S
τ_2	Time constant of integrator output settling
a_i	gain coefficient of i th integrator

η	percentage of the bottom plate parasitic
T	Absolute temperature
R	Switch ON resistance
N	quantizer levels
gm1	Amplifier transconductance
Pr()	Probability of some condition
$\sigma_{cap.}$	Mismatch of unit capacitance
k	Boltzmann's constant (1.38×10^{-23}) J/K
α	OTA noise factor
$Erf[]$	Error Function
I_{OTA}	Total current of the OTA
I_B	Bias current of each transistor of the input differential pair of OTA
k_{OTA}	The ratio of the total current of the OTA to this bias current
f_{cl2}	The *GBW* of the OTA
V_{reff}	The overdrive voltage of the transistor of the input differential pair of OTA
k_{Cs}	The ratio between the summation capacitance of C_S in all stages and the one in the first stage
ε_0	The permittivity of free space
N_S	The number of the CMOS transmission gate in $\Sigma\Delta$ modulator

1.Introduction

1.1 Current Status and Background

Sigma-delta(ΣΔ) A/D converters have been widely used for implementation of analog-to-digital conversion with high-resolution and low-to-moderate bandwidth ranging from 100Hz to 10MHz like audio [1-3], precision measurement [4], mobile communications [5], worldwide interoperability microwave access (WiMAX) system [6], and broadband wireline application like ADSL [7, 8]. Compared to the traditional converters, ΣΔ modulators have several advantages such as superior linearity and accuracy, simple realization, and low sensitivity to circuit imperfection [9], so ΣΔ modulators have become more suitable for high-resolution and low-power designs.

Switched-capacitor (SC) integrators are basic building components for implementation of ΣΔ circuits. Its incomplete transfer of charge and the slewing effect degrade drastically the performance of ΣΔ modulators and remains as the most crucial factor that restricts the performance of ΣΔ modulators. The influence increases as sampling frequency increases, since higher sampling frequency shortens the operating time of the integrator so that the integrator settling error rises. Due to the complexity of settling problem, analytic models for related noises and distortions are virtually non-existent. Recently papers considered transient transfer of charge in SC integrators and proposed several time-domain-based behavioral descriptions [10-12], which can be used in behavior simulations. Behavior simulations are time-consuming, indirect, and difficult to separate settling noises from other noises. On the other hand, analytical efforts are actually seen before. In [18-20], a detailed transient analysis for the charge-transfer error was carried out, but only for linear systems. In [21], the distortion due to operational transconductance amplifier (OTA) dynamics has been

analyzed and modeled. It uses power expansion and nonlinear fitting to obtain analytical model to represent harmonic distortion as a function of the slew-rate (SR), gain-bandwidth (GBW), and nonlinear DC gain, but the settling noise was not discussed. It is coarsely assumed in [13] that the settling noise is white and the associated power spectral density (PSD) is constant in the sampling interval, but this is far from reality.

1.2 Motivation and Aim

Designing of ΣΔ modulators is a very complex process. Recently ΣΔ modulator designing based on numerical optimization [13-15] (behavior simulation) is becoming popular, which requires many computing iterations until best performance is achieved. If the best performance achieved still can not meet the design specification, this approach can provide little clue about the dominating noise or distortion. In contrast, design and optimization based on analytical noise and distortion models can be a more efficient and dependable approach [16, 17], as long as all of the important noise and distortion models are available. Although many noise and distortion models are well derived for ΣΔ modulators [], analytical model for switched-capacitor(SC) integrators settling noise is never seen in the literature. For the reasons provided in this and previous paragraphs, the major goal of this paper is to provide the settling noise model.

The settling problems of the SC integrators are mainly caused by non-idealities of OTA such as finite dc gain, finite GBW, and SR limitations. Our research shows that these non-idealities create nonlinear transfer characteristics, which not only cause signal distortions, but also reflect high-frequency noises into base band. By employing nonlinear fitting methods and output spectrum prediction techniques, closed forms of settling error and settling distortion analytical models are obtained, and are represented as functions of ΣΔ modulator system parameters. Both behavior simulations and HSPICE circuits are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate.

1.3 Organization

This paper is organized as follows. In section II, the motivation of $\Sigma\Delta$ modulators settling effect and properties of the input for SC integrator are discussed. The formulation of analytical settling noise power model is presented in section III with an analytical discussion. In section IV, we develop the model to the settling distortion and discuss the relevance with system parameters. In section V, simulation results including transistor-level and behavior model are used to validate the model do an analytical discussion. in section VI, we provide some conclusions.

2. Formulation of ΣΔ Modulators Settling Problems

There are two purposes in this section. The first is to clearly define the settling error in switched-capacitor integrators. The second is to explore the properties of V_S, which is the input to SC integrator. Fig. 2.1 indicates a standard architecture of second order sigma-delta modulators, where $H(z) = z^{-1}/(1- z^{-1})$ is the transfer function of switched-capacitor integrator. We only consider the settling error of first stage integrator. Settling errors at later stages are less influential due to noise shaping. Fig. 2.2 shows a typical scheme of switched capacitors integrators with DAC branches. In Fig. 2.2, C_μ is the unit capacitor whose capacitance value is $C_s/2^B$.

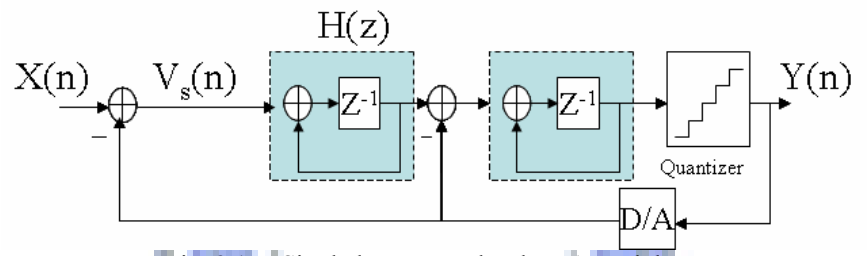


Fig. 2.1. Single loop second order ΣΔ modulator

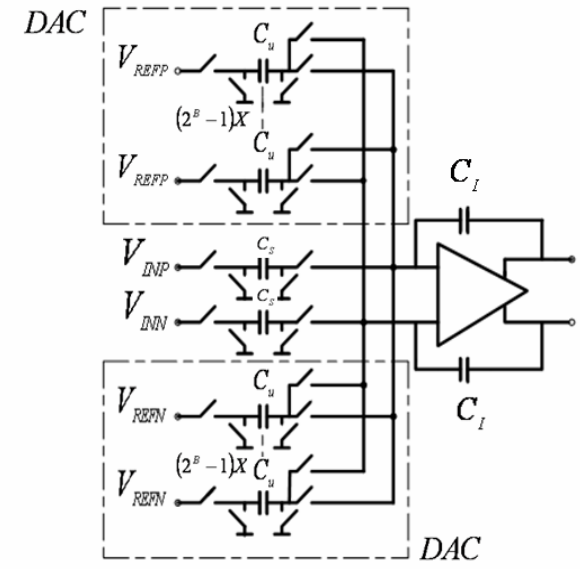


Fig. 2.2. A typical SC integrator with DAC branches

2.1 **Settling Noise of Sampling Phase and Integration Phase**

Sampling and integration phase will be analyzed separately. Fig. 2.3 illustrates sampling and integration phase of SC integrators with the MOS switched on-resistance *R* and the transconductance of OTA, *gm1*. Let the output parasitic capacitor be $C_L \cong \eta \cdot C_I$, where η is the percentage of bottom plate parasitic, assumed to be 20%[22]. In Fig. 2.3(a), the voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC:

$$V_S(z) = X(z) - Y(z) \tag{2.1}$$

In a second-order ΣΔ modulator, modulator output signal $Y(z)$ is the time delay version of $X(z)$ plus high-pass filtered (noise shaped) quantization noise $(1-z^{-1})^2 E(z)$. Therefore,

$$Y(z) = z^{-2} X(z) + (1 - z^{-1})^2 E(z) \tag{2.2}$$

Combining（2.1）and（2.2）, $V_S(z)$ can be written as

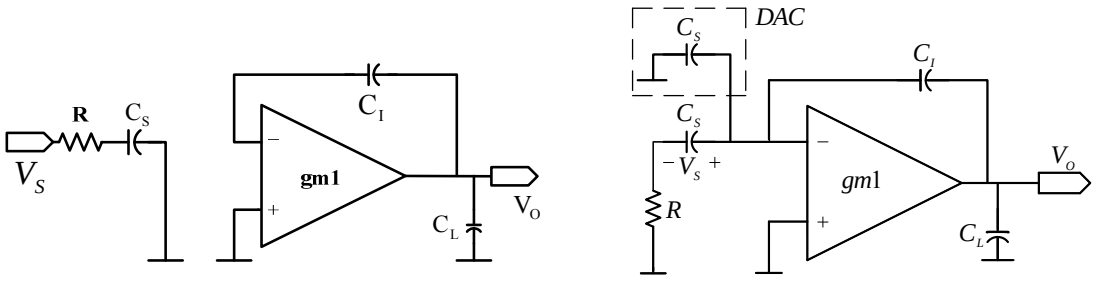
$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1 - z^{-1})^2 E(z) \tag{2.3}$$

It is sampled by C_s, so C_s is charged in the half clock period *T/2* to the voltage V_{CS}:

$$V_{CS} = V_S \cdot [1 - \exp(-\frac{T}{2 \cdot \tau_1})] \tag{2.4}$$

where $\tau_1 = R_s \cdot C_s$ is the time constant of the sampling phase in the input branch. So the setting error during the sampling phase is:

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \tag{2.5}$$



(a) Sampling phase (b) Integration phase

Fig. 2.3 Switched capacitor integrator diagrams

Next, we consider the integration phase shown in Fig. 2.3(b), where the 2^B unit capacitors are combined into C_s, and the 2^B DAC switches are neglected. The charge stored in sampling capacitor will be added to the integration capacitor and this charge current is supplied by OTA. So when the slew rate and gain bandwidth are not large enough, the settling error ε_2 will appear. According to absolute value of V_S, three types of settling conditions can happen in the integrator output during this phase, and the corresponding voltage errors of these three conditions are [11]:

1. Linear settling: When the initial change rate of the integrator output voltage (V_o) is smaller than the OTA slew rate (SR).

   $\varepsilon_2 = a_1 \cdot |V_S| \cdot \exp(-\frac{T}{2 \cdot \tau_2})$,

   when $0 < |V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2$ (2.6)

2. Partial slewing: The initial change rate of V_o is larger than SR, but it gradually decreases until it is below the slew rate.

   $\varepsilon_2 = SR \cdot \tau_2 \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1)$,

   when $\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2)\frac{SR}{a_1}$ (2.7)

3. Fully slewing: The initial change rate of V_o is larger than SR, and it maintains

above SR in the $T/2$ interval.

$$\varepsilon_2 = a_1 \cdot |V_S| - SR \cdot \frac{T}{2}$$

when $|V_S| > \frac{SR}{a_1}(\frac{T}{2} + \tau_2)$ (2.8)

where SR is the slew rate of OTA, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R \cdot Cs}{2\pi \cdot GBW}$ [23] is the time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase. The capacitor loading in OTA output during this phase is heavier than in the sampling phase, and is [17]

$$C_{L2} = 2C_S + C_L \cdot \frac{C_I + (2C_S)}{C_I} \quad (2.9)$$

The GBW is given by

$$GBW = \frac{gm1}{C_{L2} \cdot 2\pi} \quad (2.10)$$

2.2 Properties of V_S

In this section, we separately discuss the time-domain and frequency-domain properties of V_S to find out the time-domain probability distribution and the P.S.D of. These properties will be used to do nonlinear fitting and spectrum construction of settling noise in section III.

Firstly, we need to find the V_S time-domain statistical property. Simulations results (using SIMULINK) on a second-order ΣΔ modulator with $a_1 = 0.5$, $a_2 = 2$, 10-level quantization, reference voltage $V_{ref} = 1$, and a full scale sinusoidal input signal, are shown in Fig. 2.4. The result is close to a Gaussian distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean. The standard deviations σ_{VS} of V_S under different quantizer levels are tabulated in Table 2.1 We observed that when the quantizer level N increases, σ_{VS} decreases. From this table, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{vs} \approx 1.4 \cdot |V_{ref}| \quad (2.11)$$

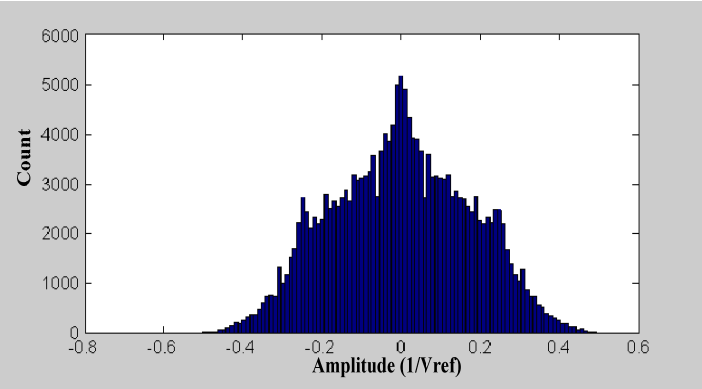


Fig. 2.4. Simulated results of V_S distribution

TABLE 2.1

Standard deviations of V_S vs. different quantizer bit numbers

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.706	0.498	2	1
0.476	0.227	3	1.585
0.282	0.080	5	2.322
0.198	0.040	7	2.808
0.152	0.023	9	3.17
0.124	0.016	11	3.46
0.047	0.002	31	4.95

Next, we must determine the P.S.D of V_S. Am expression for V_S has been given in (2.3)

$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1 - z^{-1})^2 E(z)$$

The PSD of V_S of second order $\Sigma\Delta$ modulator which simulates with OSR = 16, SR = $60_{V/\mu s}$, GBW = 130M, and a 100kHz sinusoidal input signal is plotted in Fig. 2.5. In order to calculate the PSD of V_S, we separately discuss the part of $E(z)$ and $X(z)$. We firstly ignore $X(z)$ in (2.3) and express V_S as

$$V_S(z) = (1 - z^{-1})^2 E(z) \tag{2.12}$$

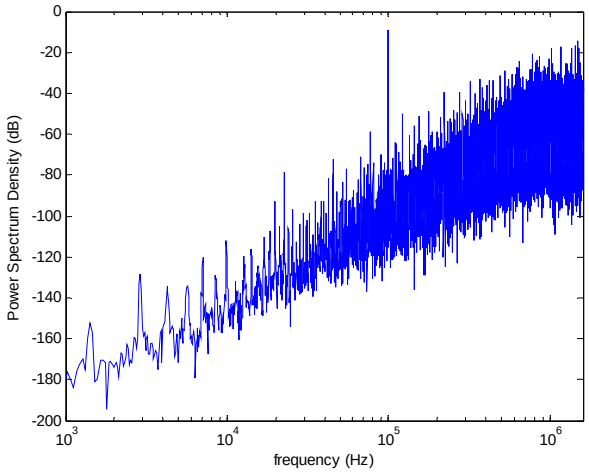


Fig. 2.5. PSD of V_S

Then the magnitude of $E(z)$ must be determine. The range of quantization error is limited in $\pm V_{LSB}/2$, and we assume the probability density function of quantization error is uniformly distributed between $\pm V_{LSB}/2$ and its mean is zero. From this assumption, the total quantization noise power can be calculated as

$$e_q^2 = \frac{V_{LSB}^2}{12} \tag{2.13}$$

$$V_{LSB} = \frac{FS}{2^B} \tag{2.14}$$

FS=Full scale = $V_{ref+} - V_{ref-}$ B：Quantization bit number

Since all the noise power of quantization error is folded into the frequency band $-f_s/2 \sim f_s/2$ and power spectral density is white, we can easily get the height of power spectral density of quantization noise.

$$h_e = \frac{V_{LSB}}{\sqrt{12 f_s}} \tag{2.15}$$

Then we substitute z with $e^{j2\pi f/f_s}$ in (2.12) and magnitude of V_S can be defined as

$$|V_s(f)| = \left[2 \cdot \sin\left(\frac{\pi f}{f_s}\right)\right]^2 \cdot \frac{FS}{2^B \sqrt{12 f_s}} \tag{2.16}$$

So the relationship between the magnitude of V_S and the bits number translates to a gain. Fig. 2.6 shows that the shape of V_S is not related to bits which can only affect the level of quantization noise floor.

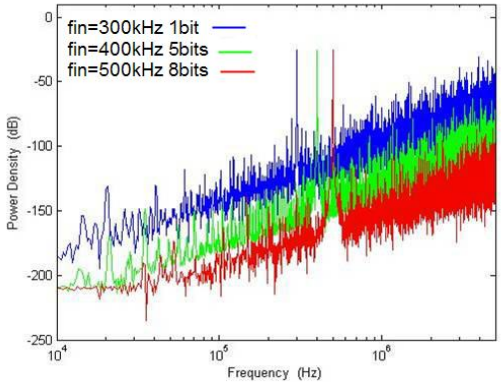


Fig. 2.6. Simulated results of V_S with A_{VS} = 0.5, OSR = 16, and different Bits

Then we consider the part of $X(z)$ and ignore the $E(z)$ in (2.3) to express V_S as

$$V_S(z) = (1 - z^{-2})X(z) \tag{2.17}$$

Take the inverse z-transform to （2.17）

$$V_S(t) = x(t) - x(t - 2T)u(t - 2T)$$

$$= A_{in}\sin(\omega t) - A_{in}\sin(\omega(t - 2T)) \cdot u(t - 2T) \tag{2.18}$$

Then, the amplitude of V_S can be obtained as

$$A_{VS} = V_S(2T) = x(2T) = A_{in}\sin(\omega \cdot 2T) \cong 2A_{in} \cdot \omega \cdot T \tag{2.19}$$

Note that A_{VS} is not related to quantizer bit number B. The result has been verified by behavior simulation under different B values, as shown in Fig. 2.6. From（2.19）, we can see that input signal amplitude A_{in}, input signal frequency ω and sampling time T are the critical parameters to impact the harmonic distortion.

2.3 Performance Metrics for a ΣΔ Modulator

- **Signal to Noise Ratio:** The SNR of a data converter is the ratio of the signal power to the noise power, measured at the output of the converter for certain input amplitude. The maximum SNR that a converter can achieve is called the peak

SNR.

- **Signal to Noise and Distortion Ratio:** The SNDR of a converter is the ratio of the signal power to the power of the noise and the distortion components, measured at the output of the converter for certain input amplitude. The maximum SNDR that a converter can achieve is called the peak SNDR.
- **Dynamic Range at the input:** The DR_i is the ratio between the power of the largest input signal that can be applied without significantly degrading the performance of the converter, and the power of the smallest detectable input signal. The level of significantly degrading the performance is defined as the point where the SNDR is 6 dB bellow the peak SNDR. The smallest detectable input signal is determined by the noise floor of the converter.
- **Dynamic Range at the output:** The dynamic range can also be considered at the output of the converter. The ratio between maximum and minimum output power is the dynamic range at the output DR_o, which is exactly equal to peak SNR.
- **Effective Number of Bits:** ENOB gives an indication of how many bits would be required in an ideal quantizer to get the same performance as the converter. This numbers also includes the distortion components and can be calculated as

$$\text{ENOB} = \frac{SNR - 1.76}{6.02} \tag{2.20}$$

- **Overload Level:** OL is defined as the relative input amplitude where the SNDR is decreased by 6dB compared to peak SNDR

Typically, these specifications are reported using plots like Fig. 2.7. This figure shows the SNR and SNDR of the ΣΔ converter versus the amplitude of the sinusoidal wave applied to the input of the converter. For small input levels, the distortion components are submerged in the noise floor of the converter. Consequently,

the SNDR and SNR curves coincide for small input levels. When the input level increases, the distortion components start to degrade the modulator performance. Therefore, the SNDR will be smaller than the SNR for large input signals. Note that these specifications are dependent on the frequency of the input signal and the clock frequency of the converter. Fig. 2.7 also shows that SNDR curves drop very fast once the overload point is achieved. This is due to the overloading effect of the quantizer which results in instabilities.

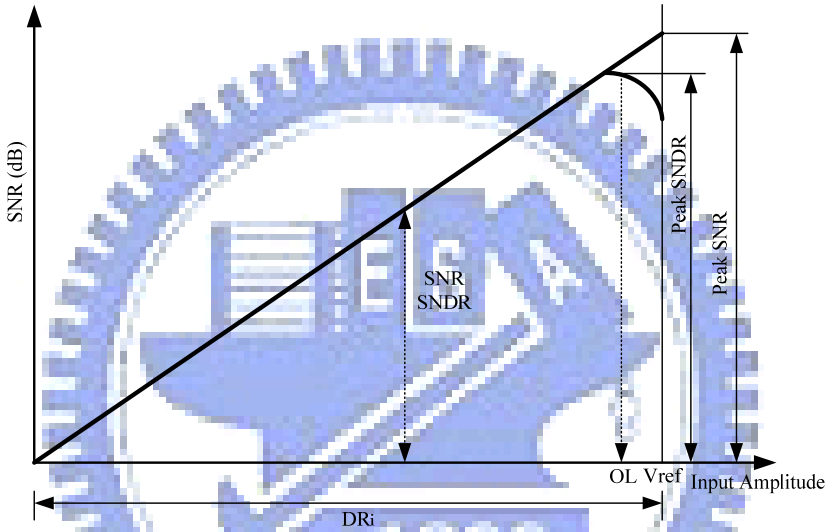


Fig. 2.7 Performance characteristic of a ΣΔ converter

3.

Derivation of Sigma-Delta Modulator Settling noise Power Model

In this section, models of settling noises which appear at ΣΔ modulator output will be derived and expressed in noise power form. This derivation is divided into sampling phase and integration phase.

3.1 Settling Errors of Sampling Phase

From (15) and (17), we can get magnitude of $|N_{TF}(z)|$ in frequency domain. By calculating the sum of in-band noise power, settling error of sampling phase can be acquired.

$$\begin{aligned} P_{\varepsilon_1} &= \int_{-f_B}^{f_B} S_e^{\,2}(f)\left|N_{TF}(f)\right|^2 df \\ &= \int_{-f_B}^{f_B} \frac{V_{LSB}}{12 f_s}\left[4\sin^2\left(\frac{\pi f}{f_s}\right)\times\exp\left(-\frac{T_s}{2\tau_1}\right)\right]^2 df \end{aligned} \tag{3.1}$$

3.2 Settling Errors of Integration Phase

As discussed in section II, there are three settling conditions depending on the absolute value of V_S. The full slewing case is not considered here because it is not significant. Note that V_S at end of each integration interval can be written as

$$g_i(V_S) = \begin{cases} a_1 V_S(1-\beta) \;; & |V_S| \le V_L \\ a_1 V_S\left(1-\dfrac{V_L}{V_S}\beta e^{-1} e^{|V_S|/V_L}\right) ; & |V_S| > V_L \end{cases} \tag{3.2}$$

where $\beta = \exp(-T_s / 2\tau_2)$ and $V_L = SR\tau_2 / a_1$

From（3.2）,the settling error of integration phase can be calculated as following expression:

$$\varepsilon_2(V_S) = \begin{cases} a_1 V_S \beta \ ; & |V_S| \le V_L \\ a_1 \operatorname{sgn}(V_S) V_L \beta e^{-1} e^{|V_S|/V_L} \ ; & |V_S| > V_L \end{cases} \tag{3.3}$$

To approximate (3.3), we apply least square method and neglect the even terms by reasons of symmetry of (3.3). Then (3.3) can be approximated by

$$p_i(V_S) = \alpha_1 V_S + \alpha_3 V_S^{\ 3} + \alpha_5 V_S^{\ 5} \tag{3.4}$$

The $p_i(V_S)$ should be fitted through all the points in that specific interval so that the sum of the squares of the distances of those points from the $p_i(V_S)$ is minimum. The sum of the squares is

$$q = \int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S$$

$$= \int_0^{V_H} [\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^{\ 3} - a_1\alpha_5 V_S^{\ 5}]^2 dV_S \tag{3.5}$$

With above method, the determination of coefficients in （3.4） for q to be minimum becomes the solution of follow equations.

$$\begin{cases} \dfrac{\partial}{\partial \alpha_1}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \\ \dfrac{\partial}{\partial \alpha_3}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \\ \dfrac{\partial}{\partial \alpha_5}[\int_0^{V_H} [\varepsilon_2(V_S) - p(V_S)]^2 dV_S] = 0 \end{cases} \tag{3.6}$$

Note that (3.7) only takes into account the nonlinear curve in (3.7), whereas errors derived from the distribution of V_S are omitted. This may lead to a worse estimation of settling noise, especially in the case of small V_L. The distribution of V_S in (3.6) is

assumed to be uniformed distributed in the specific integral interval. Nevertheless, the distribution of V_S should be defined as Gaussian distribution and the weighting function that indicates the probability of V_S in the specific interval must be considered so that (3.6) should be de revised as:

$$\begin{cases} \frac{\partial}{\partial \alpha_1}\left\{\int_0^{V_H}\left[\varepsilon_2(V_S)-p(V_S)\right]^2 \times W(V_S)dV_S\right\}=0 \\ \frac{\partial}{\partial \alpha_3}\left\{\int_0^{V_H}\left[\varepsilon_2(V_S)-p(V_S)\right]^2 \times W(V_S)dV_S\right\}=0 \\ \frac{\partial}{\partial \alpha_5}\left\{\int_0^{V_H}\left[\varepsilon_2(V_S)-p(V_S)\right]^2 \times W(V_S)dV_S\right\}=0 \end{cases} \tag{3.7}$$

where $W(V_S)$ represents the weighting function of V_S. Since the settling noise is highly depends on the distribution of V_S, the probability of V_S in the specific interval must be defined. As discussed in section II, the V_S can be assumed to be Gaussian distribution and the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{VS} \approx 1.4 \cdot |V_{ref}| \tag{3.8}$$

From（3.8）, the p.d.f of V_S is

$$f(V_s)=\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp\left(-\frac{V_s}{2\sigma_{V_S}{}^2}\right) \tag{3.9}$$

However, since the integral interval is $0 \sim V_H$, the p.d.f of V_S should be redefined as

$$f(V_s)=\frac{1}{\int_0^{V_H}\frac{1}{\sqrt{2\pi}}\exp\left(-\frac{V_s}{2\sigma^2}\right)dV_s}\frac{1}{\sqrt{2\pi}\sigma_{V_S}}\exp\left(-\frac{V_s}{2\sigma_{V_S}{}^2}\right) \tag{3.10}$$

where V_H is defined as $2V_{ref}$. Then (3.11) is normalized and the weighting function can be expressed as

$$k_2 = \frac{V_H}{\int_0^{V_H} \frac{1}{\sqrt{2\pi}} \exp(-\frac{V_s}{2\sigma^2}) dV_s} \frac{1}{\sqrt{2\pi}\sigma_{V_S}} \exp(-\frac{V_s}{2\sigma_{V_S}^2}) \tag{3.11}$$

Taking into account (3.11), (3.8) can be re-written as

$$\begin{cases} \frac{\partial}{\partial \alpha_1} \left\{ \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right]^2 \times k_2 dV_S \right\} = 0 \\ \frac{\partial}{\partial \alpha_3} \left\{ \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right]^2 \times k_2 dV_S \right\} = 0 \\ \frac{\partial}{\partial \alpha_5} \left\{ \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right]^2 \times k_2 dV_S \right\} = 0 \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right] \times (-2a_1 V_S k_2) dV_S = 0 \\ \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right] \times (-2a_1 V_S^3 k_2) dV_S = 0 \\ \int_0^{V_H} \left[\varepsilon_2(V_S) - a_1\alpha_1 V_S - a_1\alpha_3 V_S^3 - a_1\alpha_5 V_S^5 \right] \times (-2a_1 V_S^5 k_2) dV_S = 0 \end{cases}$$

$$\Rightarrow \begin{cases} \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 V_S^3 + a_1\alpha_5 V_S^5 \right] \times (V_S k_2) dV_S = \int_0^{V_H} \varepsilon_2 V_S k_2 dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 V_S^3 + a_1\alpha_5 V_S^5 \right] \times (V_S^3 k_2) dV_S = \int_0^{V_H} \varepsilon_2 V_S^3 k_2 dV_S \\ \int_0^{V_H} \left[a_1\alpha_1 V_S + a_1\alpha_3 V_S^3 + a_1\alpha_5 V_S^5 \right] \times (V_S^5 k_2) dV_S = \int_0^{V_H} \varepsilon_2 V_S^5 k_2 dV_S \end{cases}$$

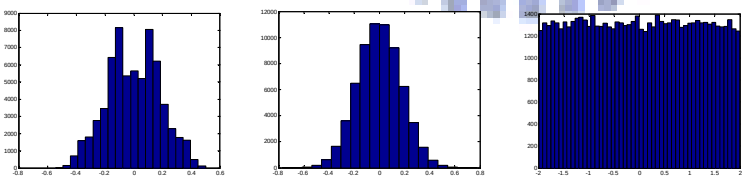
$$\Rightarrow \begin{cases} \int_0^{V_H} \left[\alpha_1 V_S^2 + \alpha_3 V_S^4 + \alpha_5 V_S^6 \right] \times k_2 dV_S \\ \qquad = \int_0^{V_L} \beta V_S^2 k_2 dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} V_S k_2 dV_S \\ \int_0^{V_H} \left[\alpha_1 V_S^4 + \alpha_3 V_S^6 + \alpha_5 V_S^8 \right] \times k_2 dV_S \\ \qquad = \int_0^{V_L} \beta V_S^4 k_2 dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} V_S^3 k_2 dV_S \\ \int_0^{V_H} \left[\alpha_1 V_S^6 + \alpha_3 V_S^8 + \alpha_5 V_S^{10} \right] \times k_2 dV_S \\ \qquad = \int_0^{V_L} \beta V_S^6 k_2 dV_S + \int_{V_L}^{V_H} V_L \beta e^{-1} e^{|V_S|/V_L} V_S^5 k_2 dV_S \end{cases}$$

Then the values of the coefficients are:

$$\begin{bmatrix}\alpha_1\\ \alpha_3\\ \alpha_5\end{bmatrix}=\begin{bmatrix}\int_0^{Vh}k_2V_S{}^2 & \int_0^{Vh}k_2V_S{}^4 & \int_0^{Vh}k_2V_S{}^6\\ \int_0^{Vh}k_2V_S{}^4 & \int_0^{Vh}k_2V_S{}^6 & \int_0^{Vh}k_2V_S{}^8\\ \int_0^{Vh}k_2V_S{}^6 & \int_0^{Vh}k_2V_S{}^8 & \int_0^{Vh}k_2V_S{}^{10}\end{bmatrix}^{-1}\times\begin{bmatrix}\int_0^{V_L}k_2\beta V_S{}^2\,dV_S+\int_{V_L}^{V_h}k_2V_L\beta e^{-1}e^{|V_S|/V_L}V_S\,dV_S\\ \int_0^{V_L}k_2\beta\cdot V_S{}^4\,dV_S+\int_{V_L}^{V_h}k_2V_L\beta e^{-1}e^{|V_S|/V_L}V_S{}^3\,dV_S\\ \int_0^{V_L}k_2\beta\cdot V_S{}^6\,dV_S+\int_{V_L}^{V_h}k_2V_L\beta e^{-1}e^{|V_S|/V_L}V_S{}^5\,dV_S\end{bmatrix}$$

(3.12)

In order to validate (3.12), we apply least square to the V_S in three cases. In case one, simulations was carried for a $\Sigma\Delta$ modulator with 3-Bits, OSR = 120, $SR = 40V/\mu s$, and GBW = 100MHz and the V_S was obtained. The coefficients, α_1, α_3, and α_5, can be determined by applying least square method to above V_S and compare with the ones obtained by another two cases, with Gaussian distribution, and no Gaussian distribution. Fig. 3.1 and Table 3.1 show the V_S and coefficients obtained in three cases. The case applied Gaussian distribution show a good fit when compared to the one by simulation. In Fig 3.2, the fitting results in three cases were illustrated and the case with Gaussian distribution is closer to the one simulated than another case. Note that the V_L in this case is 0.1681 and the probability of nonlinear operation is respectively 0.35, 0.34, and 0.9 in three cases. This result shows that applying Gaussian distribution to V_S plays a crucial role in calculating settling noise.



(a) Behavioral model (b) with Gaussian distribution (c) No Gaussian distribution

Fig. 3.1. Distribution of V_S obtained in three cases

TABLE 3.1

Coefficients obtained in three cases

	Behavioral model	with Gaussian distribution	no Gaussian distribution
α_1	0.958	0.94	835.67
α_3	1.239	1.609	-1532.7
α_5	19.677	16.357	567.25

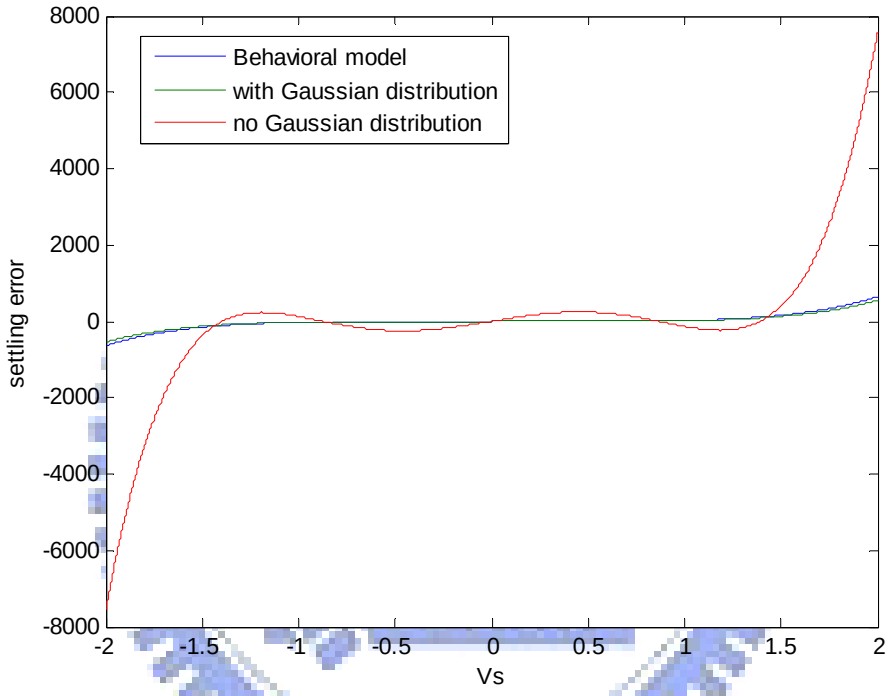


Fig. 3.2. V_S versus settling error in three cases

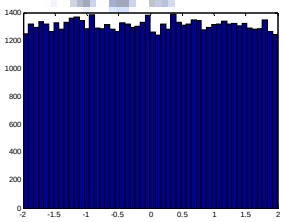


Fig. 3.3. The distribution of angle of V_S

With α_3 and α_5, the next step of calculating settling noise power is the determination of the P.S.D of ${V_S}^3$ by using the P.S.D of V_S.

(2.16) is used to destruct a signal in frequency domain on Matlab to represent it as V_S.

The height of the power spectral density of V_S in frequency domain can be expressed as

$$h_e(f) = \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi f}{f_s}) \right]^2 \times e^{i\alpha} \tag{3.13}$$

where α represents the angle of V_S. In Fig. 3.3, simulation result shows that the angle of V_S is close to a uniform distribution. Therefore, α is considerably assumed to be a arbitrary value in $0 \sim 2\pi$. To demonstrate the P.S.D of $V_S{}^3$, we will begin by considering the square of V_S. Since the P.S.D V_S has been verify in above discussion, we can use modulation of DTFT Theorems and apply circular convolution to realize square of V_S. We can expressed the height of the power spectral density of the square of V_S in frequency domain as

$$\begin{aligned} h_{e2}(f) &= h_e(f) \otimes h_e(f) \\ &= \frac{1}{f_s} \int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi\theta}{f_s}) \right]^2 \\ &\quad \frac{V_{LSB}}{\sqrt{12 f_s}} \left[2\sin(\frac{\pi(f-\theta)}{f_s}) \right]^2 \times e^{i\alpha} d\theta \end{aligned} \tag{3.13}$$

In order to compute the expect value of (3.13), we express (3.13) as a sum of different absolute value with a arbitrary value:

$$\begin{aligned} &\left| Ae^{i\alpha} + Be^{i\beta} + ce^{i\gamma} + .. \right| \\ &= | A(\cos(\alpha) + i\sin(\alpha)) + A(\cos(\beta) + i\sin(\beta)) \\ &\quad + A(\cos(\gamma) + i\sin(\gamma)) + ... | \\ &= \left[A^2 + B^2 + C^2 + ... + AB\cos(\alpha - \beta) \right. \\ &\quad \left. + AB\cos(\beta - \gamma) + AB\cos(\gamma - \alpha) + ... \right]^{0.5} \end{aligned} \tag{3.14}$$

The mean of cosine function is zero and then the expect value of (34) results as

$$\sqrt{A^2 + B^2 + C^2 + \ldots} \tag{3.15}$$

Then the expect value of the height of spectral density of square of V_S can be defined as

$$h_{e2}(f) = \frac{1}{f_s}\int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{16V_{LSB}^4}{9f_s}\sin^4(\frac{\pi\theta}{f_s})\sin^4(\frac{\pi(f-\theta)}{f_s})d\theta \tag{3.16}$$

Fig 3.4 shows that the expect value of (3.16) and behavior model simulation with f_S = 20MHz, Bit = 1.

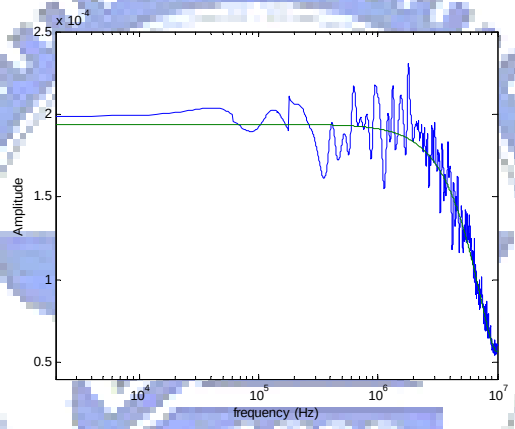


Fig. 3.4. the expect value of (3.16) and the behavior model simulation result

However, when f is zero α, β,and γ are all zero and the expect value is on longer zero. Therefore the height of spectral where f = 0 is

$$h_{e2}(0) = \frac{1}{f_s}\int_{-\frac{f_s}{2}}^{\frac{f_s}{2}} \frac{4V_{LSB}^2}{3f_s}\sin^2(\frac{\pi\theta}{f_s})\sin^2(\frac{\pi(-\theta)}{f_s})d\theta \tag{3.17}$$

Then we can follow the above technique to obtain $V_S{}^3$ and $V_S{}^5$:

$$h_{e3}(f) \cong \frac{1}{2^{3B}} \left\{ \begin{array}{l} \frac{0.879}{\sqrt{f_s}} \sin^2\left(\frac{\pi f}{f_2}\right) + \\ 0.0642 \sqrt{f_s \left[173 - 136\cos^2\left(\frac{\pi f}{f_2}\right) + 8\cos^4\left(\frac{\pi f}{f_2}\right) \right]} \end{array} \right\}$$

$$h_{e5}(f) \cong \frac{0.0396 f_s}{2^{5B}} \left[\begin{array}{l} 9.2 + 16.97\cos^2\left(\frac{\pi f}{f_s}\right)\sin^2\left(\frac{\pi f}{f_s}\right) \\ + 18.11\cos^2\left(\frac{\pi f}{f_s}\right) + 55.6\sin^2\left(\frac{\pi f}{f_s}\right) \\ + 3.23\cos^4\left(\frac{\pi f}{f_s}\right) + 15.8\sin^4\left(\frac{\pi f}{f_s}\right) \end{array} \right]^{0.5}$$

Fig. 3.5 and Fig. 3.6shows that the expect value of $V_S{}^3$ and $V_S{}^5$ compared with simulation results by behavior model.

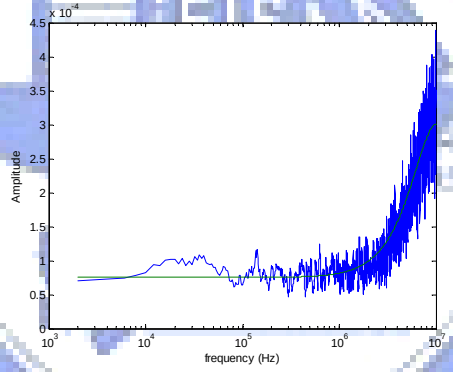


Fig. 3.5 The expect value of $V_S{}^3$ and the simulation result by behavior model

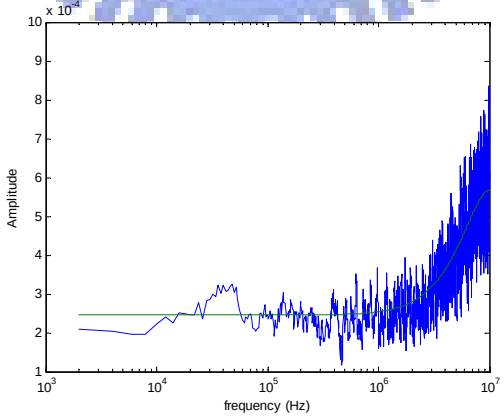


Fig. 3.6 The expect value of $V_S{}^5$ and the simulation result by behavior model

Then the expect value of the height of spectral density of settling noise of integration phase can be defined as

$$h(f) = \alpha_1 h_{e1} + \alpha_3 h_{e3} + \alpha_5 h_{e5} \tag{3.18}$$

So the settling noise in base band $\pm f_B$ of integration phase can be obtained by integrating (38):

$$P_{\varepsilon 2} = \int_{-f_B}^{f_B} (\alpha_1 h_{e1}(f) + \alpha_3 h_{e3}(f) + \alpha_5 h_{e5}(f))^2 df \tag{3.19}$$

Then total settling noise is

$$P_{\varepsilon} = P_{\varepsilon 1} + P_{\varepsilon 2} \tag{3.20}$$

Note the low frequency region of third and fifth power is absolutely flat and means that the in band noise power will increase if the α_3 and α_5 in (3.11) increase. Therefore, the nonlinearity of settling will make an amount increase on noise power. It is worth noting that settling noise is highly dependent on the high frequency noise. Due to the noise shaping nature, the high frequency amplitude of V_S is great and will lead to large settling noise.

4.
Derivations of Sigma-Delta Modulators Settling Distortion

In analysis of settling noise, the input of integrator, V_S, is define as a function of quantization noise and (13) is used to derivate settling noise. However, the V_S in this section is defined as a sinusoid and the quantization noise is ignored.

The technique applied in section 3 will be used to calculate settling distortion. Since the input signal is a sinusoid and the distribution is uniformed distributed in $-A_{VS} \sim A_{VS}$, the weighting function would not be considered and the coefficients were determined by (25). Then the coefficients were expressed as

$$\begin{bmatrix}\alpha_1\\ \alpha_3\\ \alpha_5\end{bmatrix}=\begin{bmatrix}\frac{225}{64\cdot Vh} & \frac{-525}{32\cdot Vh^3} & \frac{945}{64\cdot Vh^5}\\ \frac{-525}{32\cdot Vh^3} & \frac{2205}{16\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7}\\ \frac{945}{64\cdot Vh^5} & \frac{-4725}{32\cdot Vh^7} & \frac{11025}{64\cdot Vh^9}\end{bmatrix}\begin{bmatrix}\int_0^{VL}(1-\beta e)\,dV_S+\int_{VL}^{A_{VS}}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})\,dV_S\\ \int_0^{VL}(1-\beta e)\cdot V_S{}^2\,dV_S+\int_{VL}^{A_{VS}}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S{}^2\,dV_S\\ \int_0^{VL}(1-\beta e)\cdot V_S{}^4\,dV_S+\int_{VL}^{A_{VS}}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})V_S{}^4\,dV_S\end{bmatrix} \tag{4.1}$$

where A_{VS} has defined in (2.19). Note that the validation of the calculation is $|V_L| < A_{VS}$, otherwise, the settling will operate linearly and has no distortion at output node. $|V_S| \le V_L$ can be further derived as:

$$|V_S| \le V_L$$

$$\Rightarrow 2A\omega T \le \frac{SR\tau}{0.5}$$

$$\Rightarrow 2A\cdot 2\pi\cdot f_{in}\cdot\frac{1}{2\times BW\times OSR}\le\frac{SR}{0.5}\cdot\frac{1+2\pi\cdot GBW\cdot RC_S}{2\pi\cdot GBW}$$

$$\Rightarrow OSR\ge\cdot 2A\cdot 2\pi\cdot f_{in}\cdot\frac{1}{2\times BW}\frac{2\pi\cdot GBW}{1+2\pi\cdot GBW\cdot RC_S}\frac{0.5}{SR} \tag{4.2}$$

Assuming $f_{in}=BW$, $R=300\Omega$, $C_S=2\times10^{-12}F$, it leads to the following equation:

$$OSR\ge\frac{\pi}{SR\left(\frac{1}{2\pi\cdot GBW}+6\times10^{-10}\right)} \tag{4.3}$$

We then plot（4.3）as shown in Fig. 4.1 which shows that *OSR* is inverse proportional to *SR* and is almost independent to *GBW*.

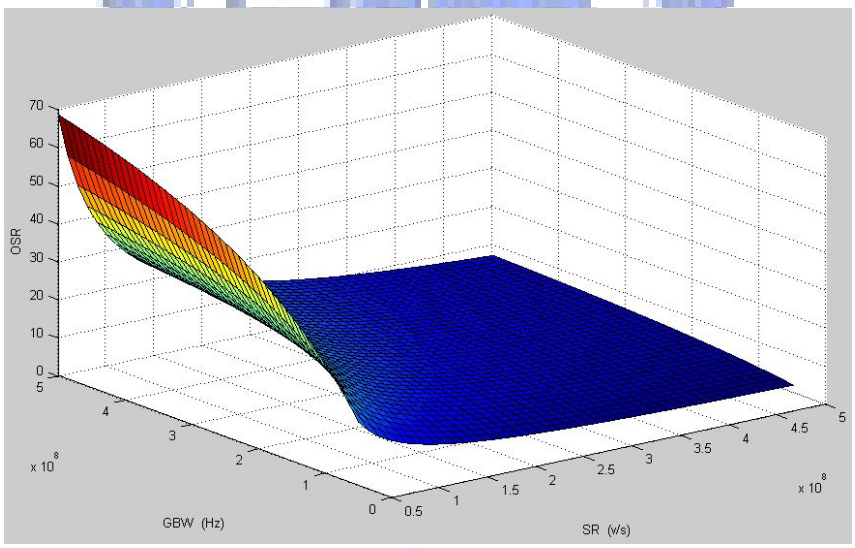


Fig. 4.1 3D plot of（4.3）

Fig. 4.1 indicates that if we design *SR* and *GBW* above the curve with desired *OSR*, the modulator would have no harmonic distortion. It shows that the op-amp slew rate needs to be at least 200V/us, then the modulator can have no harmonic distortions with *OSR* larger than 15. Although op-amps operate in linear region can have no harmonic distortion, it may consume more power dissipation (because large slew rate).

Therefore, there has a trade off between power consumption and harmonic distortion. In general, one can choose smaller slew rate to let power consumption lower and have negligible harmonic distortions.

In order to verify the result in （4.1）, we use SIMULINK to build a second-order ΣΔ modulator with a multi-bit quantizer. The behavioral settling model in [11] is employed. We assume that $SR = 70V/\mu s$, GBW = 100MHz, $R = 300\Omega$, OSR = 16, f_B = 1MHz and C_S = 2pF, and a 1MHz sinusoidal input signal is used. After performing FFT to the output data of the ΣΔ modulator, we obtain the simulated P.S.D which is shown in Fig. 4.2 It shows that HD3 is -115.1dB and HD5 is -119.9dB. The theoretical harmonic powers calculated from（4.1） are HD3 = -116.4dB and HD5 = -120.3dB. The simulated and theoretical results are very close, and this confirms that our settling distortion model is reasonably precise.

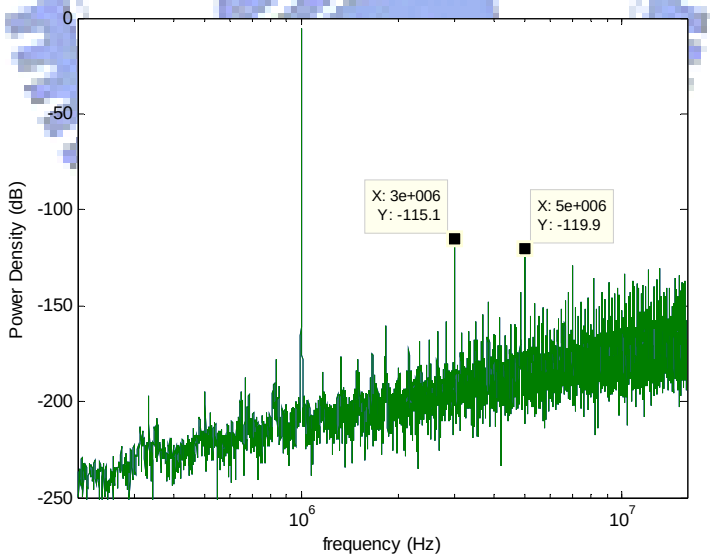


Fig. 4.2 Output spectrum of a second-order ΣΔ modulator with harmonic distortion

In order to provide insight on how settling distortions are related to circuit and system parameters, we further analyze the 3rd and 5th harmonic powers as follows:

$$HD3_{settling}(dB) = 20\log\left(\frac{1}{\sqrt{2}}\left(\frac{|\alpha_3|A_{VS}^3}{4}\right)\right)$$

$$= 20\left[\log|\alpha_3| + \log(2A\omega T)^3 - \log 4\sqrt{2}\right]$$

$$= 20\log|\alpha_3| - 60\log OSR + 30.095 \qquad (4.4)$$

$$HD5_{settling}(dB) = 20\log|\alpha_5| - 100\log OSR + 48.15$$

From （4.4） we can see that *OSR* can effectively influence settling harmonic powers. The (4.4) reveals that α_3 and α_5 are functions of *T*, *GBW*, *R*, C_S and *SR*. In order to place much more emphasis on relationship between GBW and the settling distortion, Fig 4.3 shows HD3 with *SR*=50V/us, $R = 300\,\Omega$, *OSR* = 16, f_B= 1MHz and C_s = 2pF, and a 1MHz sinusoidal input signal. Similarly, Fig. 4.4 shows *SR vs*. HD3 with *GBW*=50MHz.

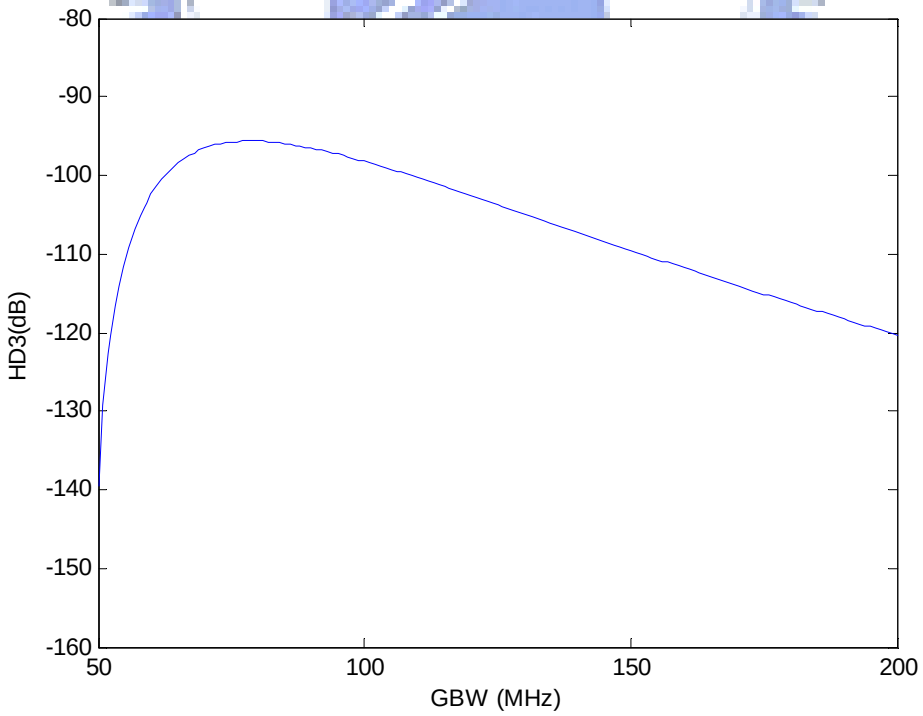


Fig. 4.3 GBW v.s HD3

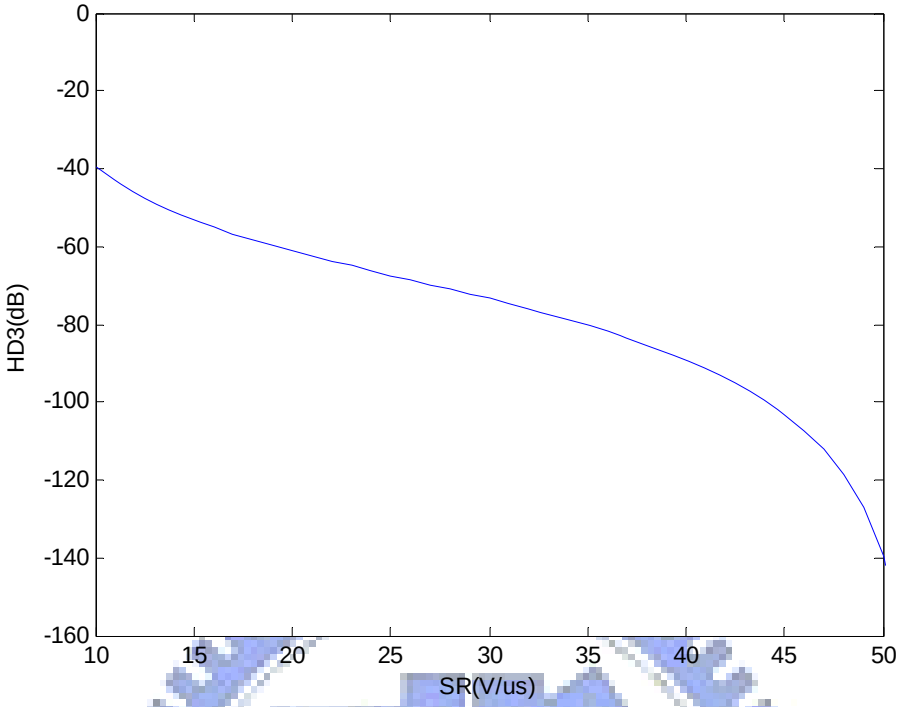


Fig. 4.4 SR v.s HD3

The simulated and theoretical results are very close, and this confirms that our settling distortion model is reasonably precise.

In general, harmonic distortion less than -110dB can be ignored because it is below the noise floor of modulator output spectrum. From(39), Fig. 4.4 and Fig. 4.5, we can obtain the minimum required *SR* and *GBW* w. r. t. a specific *OSR*. The results are summarized in Table 4.4.

It is clear from Table 4.1 that as *OSR* decreases, *SR* have to increase dramatically so that the effect of settling distortion can be contained. This can be explained by（39）, since *T* increases when *OSR* decreases.

TABLE 4.1

Minimum SR and GBW required w. r. t. OSR

OSR	HD3(dB)	*SR* $(V/\mu s)$	*GBW* (MHz)
2	$20\log\|\alpha_3\|$ **-24**	≥ 180	≥ 430
4	$20\log\|\alpha_3\|$ **-42**	≥ 150	≥ 400
8	$20\log\|\alpha_3\|$ **-60**	≥ 120	≥ 370
16	$20\log\|\alpha_3\|$ **-72**	≥ 100	≥ 350
32	$20\log\|\alpha_3\|$ **-78**	≥ 80	≥ 340
64	$20\log\|\alpha_3\|$ **-89**	≥ 50	≥ 320
100	$20\log\|\alpha_3\|$ **-90**	≥ 30	≥ 300

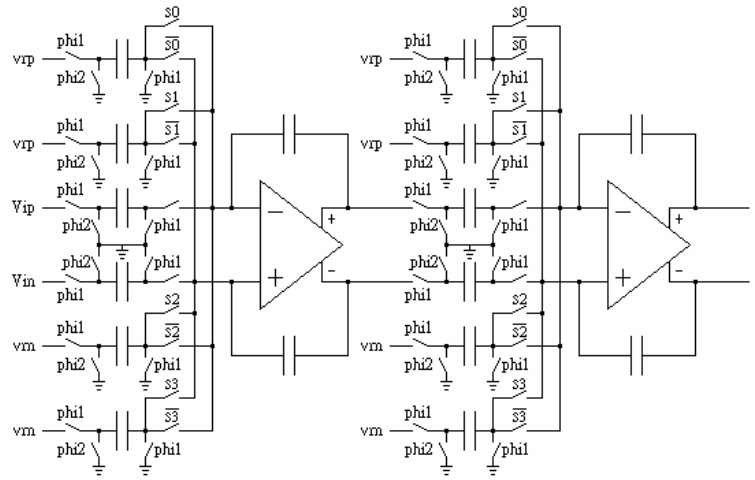


Fig. 5.1 Circuit-level schematic of spice simulation

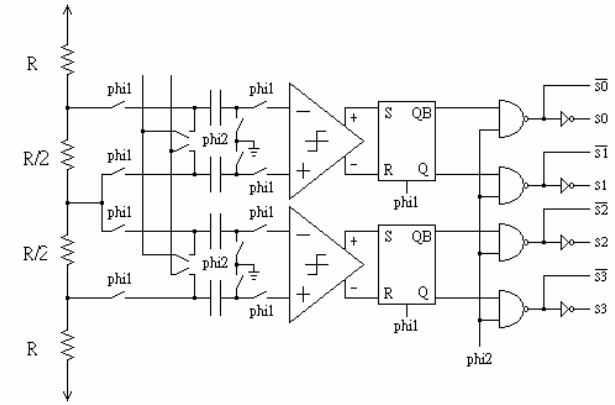
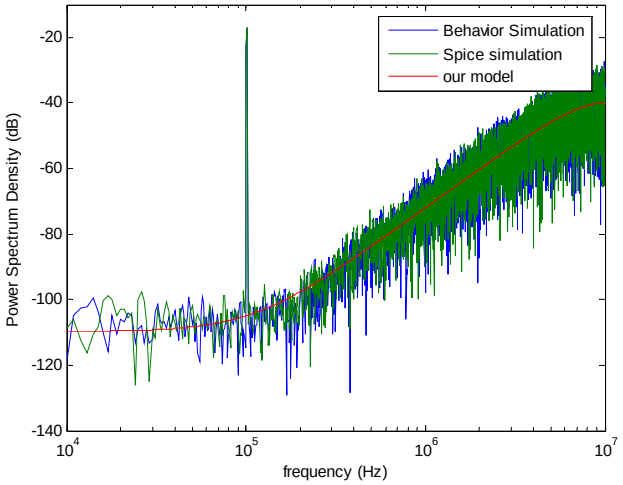
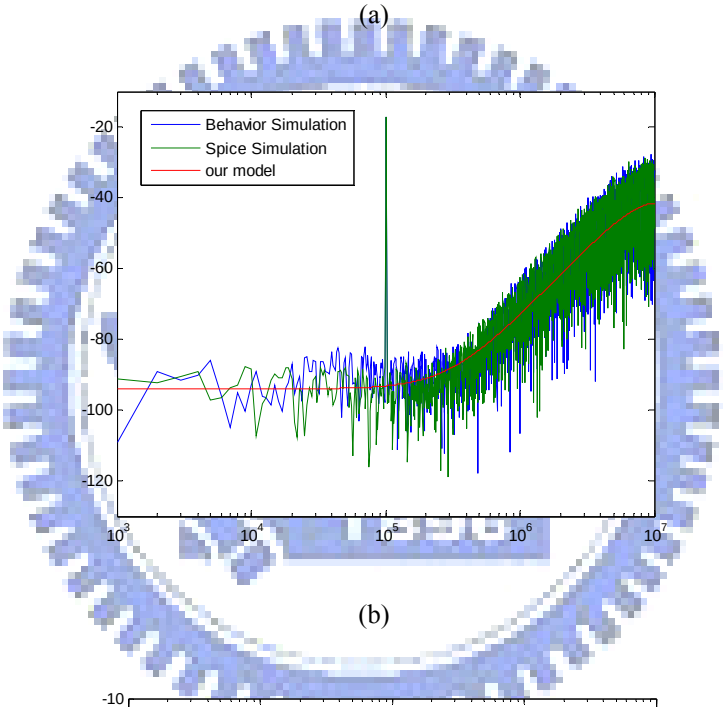


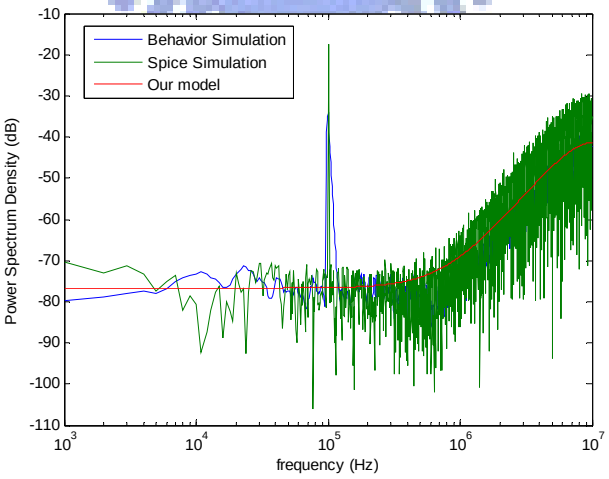
Fig. 5.2 Quantizer of spice simulation



(a)



(b)



(c)

Fig. 5.3 Comparison of our theoretical result with transistor-level and behavior simulation result

5.
Simulation Results and Validation

In order to demonstrate the validity the model presented in previous section, we use the spice simulation shown in Fig. 5.1 and Fig. 5.2 The relevant parameters were: $f_B = 100$kHz, OSR = 100, C_S = 0.5pf, C_i = 1pf, and a 100 kHz sinusoidal input signal. Additional parameters used in the simulation of Fig. 5.3 are listed in Table 5.1. Fig. 5.3 shows the settling noise obtained by presented model and simulated output by transistor-level and behavior model. The theoretical noise power by previous model is obtained by adding the previous settling noise power to the theoretical quantization noise power. The output shows a good agreement between the transistor-level modeled and presented modeled modulator.

Notice that increase OSR will increase settling noise and reduce SNR. Then we do the same simulation with different OSR. Fig. 5.4 indicates the noise power at $\Sigma\Delta$ modulator output, which is a combination of quantization noise and settling noise. Notice that increasing *SR* and *GBW* will reduce settling noise and increase *SNR*, but will also increase analog power consumption and the design challenges. On the other hand, multi-bit quantizers can reduce the slew rate requirement, since a multi-bit structure makes the output feedback signal closer to the input signal.

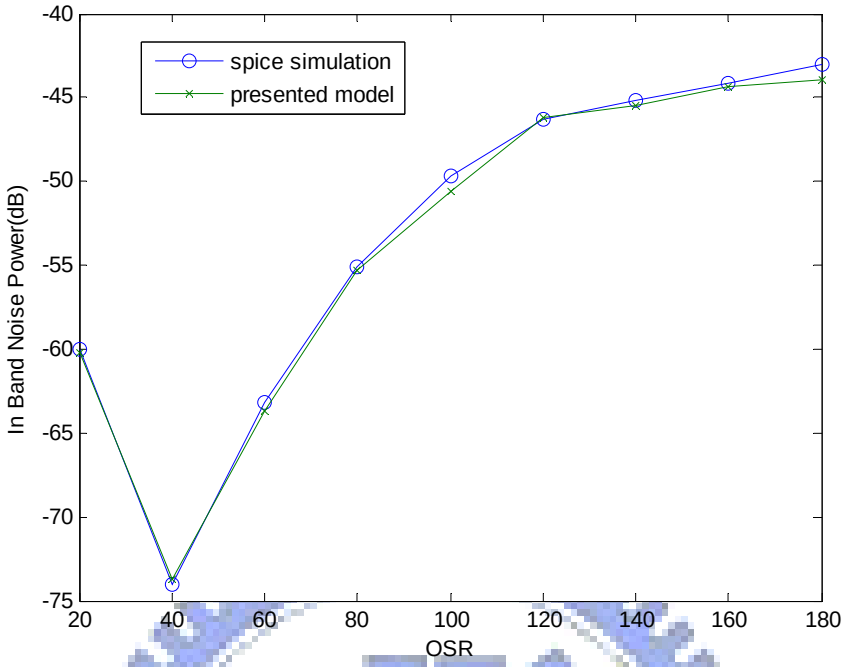


Fig. 5.4 P.S.D of settling noise obtained from transistor-level simulation and previous established model

The previous study reveals that as non-idealities or OSR increases, the settling noise will rise dramatically and degrade the performance of ΣΔ modulator. Because high non-idealities reflect high-frequency noises into base band, first order ΣΔ modulator maybe is a more efficient architecture than second order. In order to make an efficient choice between first and second order, we calculate the minimum required *SR* and *GBW* w. r. t. a specific *OSR*. The results are summarized in Table 5.2. Table 5.1 indicates that as OSR increase, the bigger SR and GBW are needed to cope with the settling noise.

TABLE 5.1

SIMULATION PARAMETERS IN FIG. 5.3

Parameter	Fig. 5.3(a)	Fig. 5.3(b)	Fig. 5.3(c)
SR $(V/\mu s)$	160	80	60
GBW(MHz)	160	127	95
P_ε (dB)	-85.4	-68.48	-49.2

TABLE 5.2

MINIMUM SR AND GBW REQUIRED W. R. T. OSR

OSR	$\mathbf{P_Q}$ of fist order ΣΔ modulator	***SR*** $(V/\mu s)$	***GBW*** **(MHz)**
16	6.69×10^{-5}	≥ 6	≥ 20
32	8.37×10^{-6}	≥ 20	≥ 40
64	1.05×10^{-6}	≥ 50	≥ 75
80	5.35×10^{-7}	≥ 60	≥ 120
100	2.74×10^{-7}	≥ 100	≥ 140
120	1.59×10^{-7}	≥ 140	≥ 160
140	1×10^{-7}	≥ 200	≥ 220

6.
Conclusions and Future Works

The analytical model of settling noise of ΣΔ ADCs is never derived in the literature to date and can only be performed through time-domain behavior simulations due to the complex dynamic behavior. In this paper, we have established an analytical model with nonlinear slewing behavior to adequately estimate the ΣΔ ADCs in-band noise power as a function of ΣΔ modulator system parameters. Once the system parameters such as OSR, GBW, and SR are known, the model gives a expect value of PSD. Both behavior simulations and HSPICE circuits are employed to verify these analytical models, and the results show that our analytical models are sufficiently accurate. Measurement results suggest that for high order ΣΔ ADCs with high OSR and low Bit-number the settling noise will be bigger than other noises and becomes dominate noise source.

References

[1] J. Candy, "A Use of Double Integration in Sigma Delta Modulation," *Communications, IEEE Transactions on [legacy, pre - 1988],* vol. 33, pp. 249-258, 1985.

[2] B. P. Brandt, D. E. Wingard, and B. A. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," *Solid-State Circuits, IEEE Journal of,* vol. 26, pp. 618-627, 1991.

[3] B. E. Boser and B. A. Wooley, "The design of sigma-delta modulation analog-to-digital converters," *Solid-State Circuits, IEEE Journal of,* vol. 23, pp. 1298-1308, 1988.

[4] B. DelSignore, D. Kerth, N. Sooch, and E. Swanson, "A monolithic 20 b delta-sigma A/D converter," in *Solid-State Circuits Conference, 1990. Digest of Technical Papers. 37th ISSCC., 1990 IEEE International*, 1990, pp. 170-171, 293.

[5] J. Grilo, I. Galton, K. Wang, and R. G. Montemayor, "A 12-mW ADC delta-sigma modulator with 80 dB of dynamic range integrated in a single-chip Bluetooth transceiver," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 271-278, 2002.

[6] B. J. Farahani and M. Ismail, "Adaptive Sigma Delta ADC for WiMAX fixed point wireless applications," *Circuits and Systems, 2005. 48th Midwest Symposium on,* pp. 692-695, 2005.

[7] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz, and P. Pessl, "A 85-dB dynamic range multibit delta-sigma ADC for ADSL-CO applications in 0.18-/spl mu/m CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 1105-1114, 2003.

[8] R. del Rio, J. M. de la Rosa, B. Perez-Verdu, M. Delgado-Restituto, R. Dominguez-Castro, F. Medeiro, and A. Rodriguez-Vazquez, "Highly linear 2.5-V CMOS /spl Sigma//spl Delta/ modulator for ADSL+," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on],* vol. 51, pp. 47-62, 2004.

[9] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma data converters: theory, design, and simulation*: New York: IEEE Press: Wiley-Interscience, 1997.

[10] G. Suarez, M. Jimenez, and F. O. Fernandez, "Behavioral Modeling of Switched Capacitor Integrators with Application to 聶聶 Modulators," in *Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on*, 2006, pp. 709-713.

[11] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also*

Circuits and Systems I: Regular Papers, IEEE Transactions on], vol. 50, pp. 352-364, 2003.

[12] G. Suarez, M. Jimenez, and F. O. Fernandez, "Behavioral Modeling Methods for Switched-Capacitor Σ∆ Modulators," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]*, vol. 54, pp. 1236-1244, 2007.

[13] F. Medeiro, A. Perez-Verdu, and A. Rodriguez-Vazquez, *Top-Down Design of High-Performance Sigma-Delta Modulators*: Kluwer Academic Publishers, 1999.

[14] S. Loeda, H. M. Reekie, and B. Mulgrew, "On the design of high-performance wide-band continuous-time sigma-delta converters using numerical optimization," *Circuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on]*, vol. 53, pp. 802-810, 2006.

[15] O. Bajdechi and J. H. Huijsing, *Systematic Design Of Sigma-delta Analog-to-digital Converters*: Springer, 2004.

[16] G. I. Bourdopoulos, *Delta-SIGMA Modulators: Modeling, Design and Applications*: Imperial College Press, 2003.

[17] Y. Geerts, M. Steyaert, and W. M. C. Sansen, *Design of Multi-Bit Delta-SIGMA A/D Converters*: Kluwer Academic Publishers, 2002.

[18] W. M. C. Sansen, H. Qiuting, and K. A. I. Halonen, "Transient analysis of charge-transfer in SC filters-gain error and distortion," *Solid-State Circuits, IEEE Journal of*, vol. 22, pp. 268-276, 1987.

[19] K. L. Lee and R. G. Mayer, "Low-distortion switched-capacitor filter design techniques," *Solid-State Circuits, IEEE Journal of*, vol. 20, pp. 1103-1113, 1985.

[20] J. C. Candy and G. C. Temes, "Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation," *IEEE, New York*, 1992.

[21] F. Medeiro, B. Perez-Verdu, A. Rodriguez-Vazquez, and J. L. Huertas, "Modeling opamp-induced harmonic distortion for switched-capacitor ΣΔ modulator design," in *Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on*, 1994, pp. 445-448 vol.5.

[22] S. Rabii and B. A. Wooley, *The design of low-voltage, low-power sigma-delta modulators*: Kluwer Academic Publishers Norwell, MA, USA, 1998.

[23] R. Rio Fernandez, F. Medeiro, B. Perez Verdu, J. M. Rosa Utrera, and A. Rodriguez Vazquez, "CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design," 2008.

[24] S. Brigati, F. Francesconi, P. Malcovati, D. Tonietto, A. Baschirotto, and F. Maloberti, "Modeling sigma-delta modulator non-idealities in SIMULINK (R)," *Circuits and*

Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on, vol. 2, 1999.