國立交通大學

電機與控制工程系

碩士論文

利用混沌產生器抑制直流-直流轉換器

電磁干擾水平

Suppression of Electromagnetic of DC-DC Converter

with Chaos Generator

研 究 生：沈柏年

指導教授：陳福川　教授

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摘要

在對於電子產品上，DC-DC 電源轉換器是一種電磁干擾源；因此對於開關式電源轉換器的設計，抑制電磁是一個很重要的課題。傳統抑制電磁干擾的方法利用 LC 濾波器跟金屬屏蔽來達到抑制效果，但是此方法會增加系統成本, 體積跟重量。在這此論文裡，我們提出的方法是利用混沌特性來降低由開關式電源轉換器所產生的電磁干擾峰值並且把諧坡的離散頻率分散成連續的多頻特性。此方法主要將依賴混沌特性所調變的時脈來影響一個操作原本正常週期的電源轉換器。最後的穩定度分析與模擬結果證明此方法對於抑制電磁干擾是非常有效的並且不影響電源轉換器的性能。此外，有別於其他方法，此方法可以很容易的應用在 CMOS 技術上。

Suppression of Electromagnetic of DC-DC Converter with Chaos Generator

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ABSTRACT

Power DC-DC converters are notorious sources of electromagnetic interference in electronic products; therefore, suppression of EMI is an important topic in the design of switch-mode power converters. Conventional EMI suppression methods may employ LC filters and metal shielding, but this can significantly increase cost, size, and weight. In this paper we propose a chaos-based method to reduce peak EMI magnitude and spread the energy to a wide range of frequencies. This method is to add a chaos-modulation clock to a converter maintaining in regular period state, in order to create chaotic behaviors in the converter. Our results show that this method is effective in suppressing EMI in DC-DC converters without much impact on the performance of converters. System stability is also analyzed and discussed. Moreover, compared with conventional methods, the method can be easily implemented in CMOS technology.

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沈柏年

2008　夏　於新竹交大

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Chapter1
Introduction

1.1 Significance of the Research

The chaos technique is an important topic for study in power electronics because many applications employ it. At present, there are two study fields applying the chaos technique in DC-DC converters. The first field is the control of chaos. It mainly uses small perturbations to stabilize unstable periodic orbits which are abundant in chaotic attractors. A famous method for chaos control strategy was reported by Ott-Grebogi-Yorke(OGY) [1]. In addition, other methods are also proposed. For example, occasional proportional feedback method[2], versions of OGY method[3], and time-delayed auto-synchronization method [4, 5]. The other study field is that of reducing EMI in switching-mode power supplies which are notorious generator of both conducted and radiated Electromagnetic interference (EMI), owing to high rates of voltages and currents. In the paper, we focus on the problem of reducing EMI for DC-DC converters by chaos technique.

Nowadays, a very large amount of electromagnetic emission exists, so that the problem of designing electromagnetic compatible (EMC) systems has become a great and widespread practical concern. Especially for power electronic designers, the goal of reducing EMI

emission is of paramount importance. Due to the rapid switching of high currents and voltages, interference emission may become severe. Conventional methods to tackle the EMI problems include LC filters and metal shielding for EMI. These solutions generate their own problems like increased cost, size, and weight. Moreover, such designs are not suitable in different EMC norms because each time the application domain of main system changes, filters and screens have to be redesigned even if the converter specifications themselves are unchanged. This incurs additional expenses and increases design time [6]. In addition, a soft-switching technique is one of the methods directly tackling the EMI problems. However, the result that can be achieved by this method is limited[7].

Because of the quality of containing many frequencies in chaos, chaos technique can be applied to expand frequency band in systems[8]. Moreover, it can achieve the purpose of dispersing the energy in spectrum so that the peak values in fundamental frequency and the harmonics are reduced. Compared with the high peak value in a narrow frequency band, the quality of the low peak value in a wider frequency band is easy to conform to various EMC norms. Therefore, operating under the chaos state for switching converters is practical to improve EMC problems.

Up to now, switching converters have two methods to achieve suppression of EMI by chaos technology. The first method is the parameter-controlling method [9-14]. Switching converters are operated under the chaos state by controlling currents, controller parameters,

and reference voltage and loading, etc. For example, converters may operate under the chaos state when output loading is changed. Besides, the properties of converters are affected when parameters are adjusted. Because the controlling condition is very complex, it is difficult to achieve a satisfying design. The second method is variable- frequency-modulation method[15]. It mainly utilizes the broadband nature of clock signal generated by chaotic system to reduce EMI. The main advantage for this method is that the system is forced into the chaos state without changing the properties of the main system. Since the chaos generator affects the clock signal, the proposed method of EMI reduction can be applied to any existing converters. Some methods of spreading the spectrum through chaotic modulation have been proposed in [16-19], However, analyses of stability are not analyzed and discussed further in above papers. Moreover, someone employ Chua's circuit [20-23] as a chaos generator generating chaotic signals, but it has some difficulties in IC design, owing to an inductor element in the circuit.

1.2 Motivation

We propose a circuit frame applying the EMI reduction technique to drive a current-controlled boost converter. The circuit frame mainly employs the characteristic of fast charge and discharge of a capacitance to generate a set of chaotic signals. The main advantage of the circuit frame is to be built and still achieve the purpose of suppression of EMI of a converter by using characteristic of power spectrum of chaos. Besides, compared to Chua's

circuit which oscillates chaotic signal by an inductor and a capacitance, it is appropriate to use the circuit frame in VLSI regime. In the article, we will compare performances of the two mentioned EMI reduction methodologies in terms of PDS peak reduction and the inductor current ripple. Furthermore, in order to estimate the influence of this method on its performance, we particularly analyze the stability of the converter in every quasi-period state by analyzing duty ratio. The results of simulation show that every power of harmonics in an inductor current under chaos state is reduced by more 45%.

1.3 Organization

The rest of the thesis is organized as follows. Chapter1 of the article is a review of the literature. This is followed by the method of studying discrete models for chaos. The Chapter3 section describes the design of chaos generator and analysis of stability. The results for the simulation analysis are presented in the fourth section. Finally, conclusions are presented and suggestions are made for further research.

Chapter2
Basic Theory of Boost Converter and Chaos

2.1 State Analysis of Boost Converter

DC-DC Converters are widely used in regulated switch-mode dc power supplies. The input to these converters is an unregulated dc voltage obtained by rectifying the line voltage; therefore it will fluctuate due to changes in the line-voltage magnitude. Switching DC-DC converters are used to convert the unregulated dc input into a controlled dc output at a desired voltage level.

In DC-DC converters, the average output level can be adjusted to a desired value when input or output loading is varying. Switch-mode conversion concept can be illustrated with Fig.2-1(a). The average output value V_o depends on t_o and t_{off} in Fig.2-1(b).

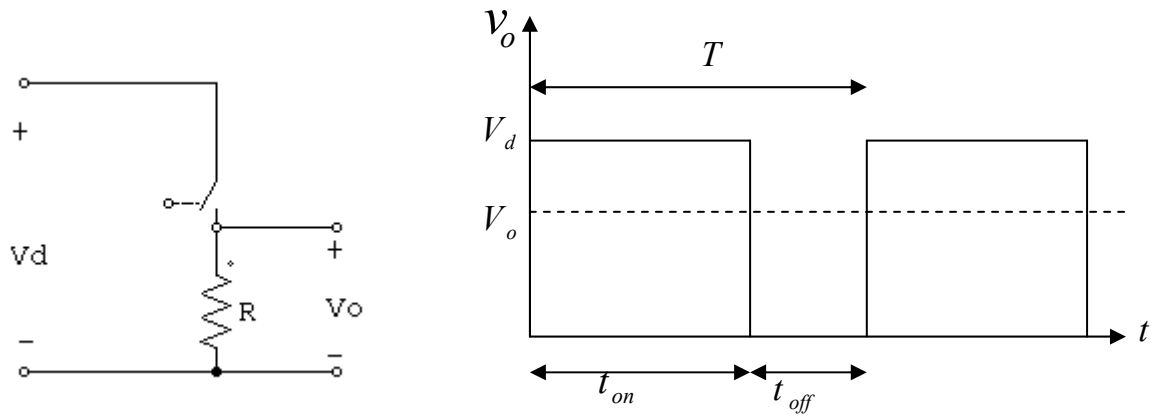


Fig.2-1(a) Switch-mode DC-DC conversion(b) The average output value V_o depends on t_o and t_{off}

DC-DC converters have many types and wide applications including step-down converter, step-up converter, buck-boost converter, Cuk DC-DC converter, full bridge DC-DC converter, etc. In this thesis, a boost converter in Fig.2-2 is employed as the main system. Therefore, the following will expound the fundamental theorem of the boost converter.

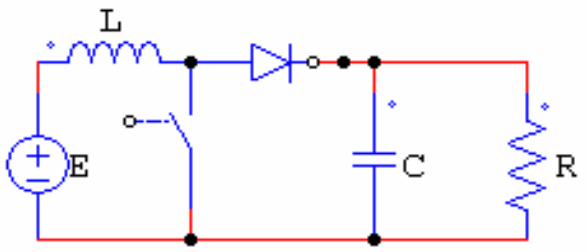


Fig.2-2 Boost Converter circuit

For a boost converter, as the name implies, the output voltage is always greater than the input voltage. When the switch turns on, the diode is revered biased, so isolating the output stage. The input saves energy in the inductor. However, when the witch turns off, the output stage receives energy from the inductor as well as from the input.

2.1.1 Continuous Condition Mode(CCM)

When system is in steady state and the inductor current i_L is all greater than zero, the system operates in continuous condition mode. In Fig.2-3(a), when the switch turns on, the inductor voltage $v_L = E$, and the inductor current i_L increases linearly. Besides, the

capacitance discharges to the resister. In Fig.2-3(b), when the switch is off, the inductor voltage increase $v_L = E - v_o$, and the input voltage and the inductor voltage charge to the capacitance. Besides, the inductor current i_L decreases linearly.

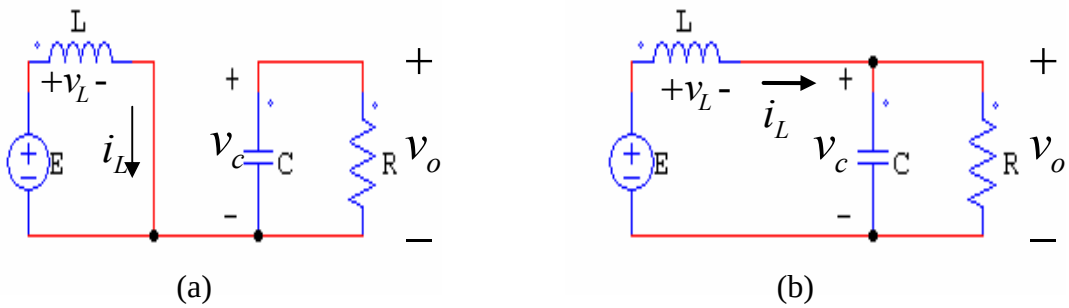


Fig.2-3 Boost converter circuit states (a)switch is on (b)switch is off

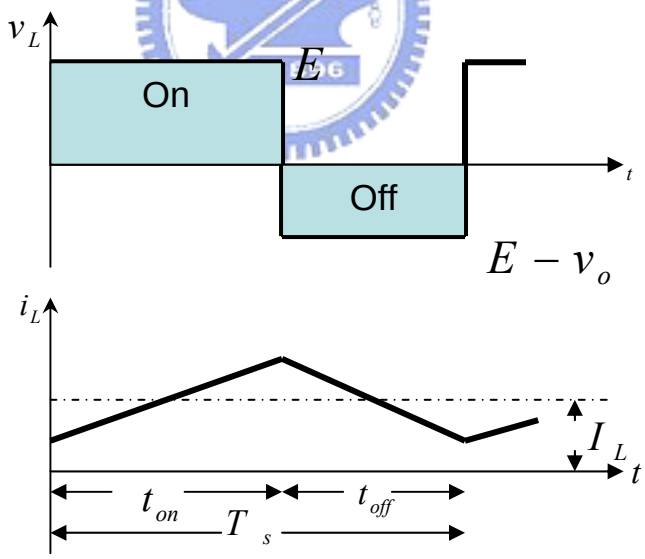


Fig.2-4 Waveforms of voltage and current of inductance

In steady state, because the average value of the inductor voltage at one period is zero, therefore,

$$\int_0^{t_s} v_L dt = \int_0^{t_{on}} v_L dt + \int_{t_{on}}^{T_s} v_L dt = 0 \tag{2.1}$$

In Fig.2-4, the area On is equal to the area Off.

Therefore,

$$Et_{on} = -(E - V_o)t_{off} \tag{2.2}$$

and

$$\frac{t_{on}}{T_s} = D, \frac{t_{off}}{T_s} = 1 - D \tag{2.3}$$

So, the relation of the output voltage and input voltage is

$$\frac{V_o}{E} = \frac{T_s}{t_{off}} = \frac{1}{1-D} \tag{2.4}$$

If the circuit is lossless,

$$P_L = P_o \Rightarrow EI_L = V_o I_o \tag{2.5}$$

Therefore,

$$\frac{I_o}{I_L} = (1 - D) \tag{2.6}$$

2.1.2 Boundary between CCM and DCM

When the inductor current is just equal to zero at end of t_{off} at a period, the boundary between continuous condition mode and discontinuous condition mode is happened.

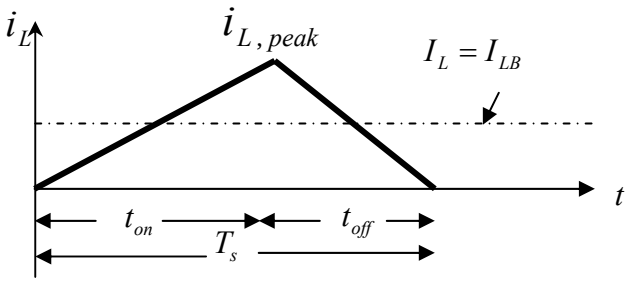


Fig.2-5 The inductor current at the boundary

In Fig.2-5**,** the average value of the inductor current at the boundary is

$$I_{LB} = \frac{1}{2} i_{L,peak} = \frac{E}{2L} D T_s = \frac{V_o}{2L} D(1-D) T_s \tag{2.7}$$

From (2.6)

$$I_{OB} = I_{LB}(1-D) = \frac{V_o}{2L} D T_s (1-D)^2 \tag{2.8}$$

Therefore, if a boost converter is operated in CCM, the condition is as

$$I_o > I_{oB} = \frac{V_o}{2L} D T_s (1-D)^2 \tag{2.9}$$

or the value of the inductor is chosen as

$$L > L_B = \frac{V_o}{2 I_{oB}} D T_s (1-D)^2 \tag{2.10}$$

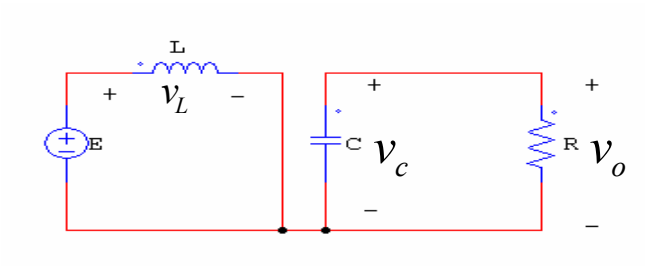
2.1.3 Discontinuous Condition Mode(DCM)

From (2.10), if L is less than L_B, the system is operated under discontinuous condition mode. Fig.2-6 are series of three circuits illustration that there are three conditions at a period under DCM. The first duration is $D_1 T_s$ when the switch is on and the diode is off.

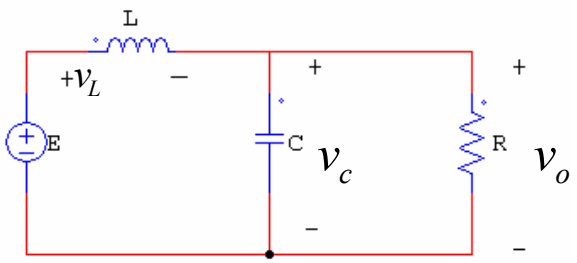
The second duration is D_2T_s when the switch is off and diode is on, and the inductor current is zero. The third duration is D_3T_s when the switch and the diode are off. All of the above have shown the relation of D_1, D_2, D_3 as:

$$D_1 + D_2 < 1 \tag{2.11}$$

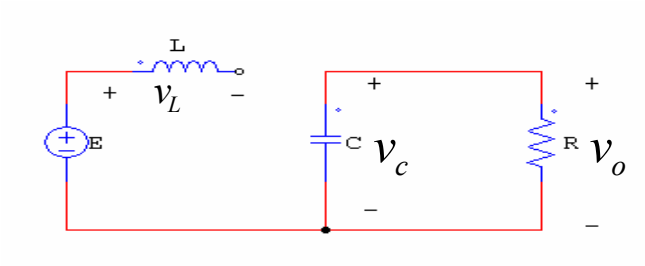
$$D_1 + D_2 + D_3 = 1 \tag{2.12}$$



(a)The witch is on, the diode is off



(a)The witch is off, the diode is on



(c) The witch is off, the diode id off

Fig.2-6 The circuit the boost converter operates under DCM

According as the integral of the inductor voltage over one time period to zero,

$$ED_1T_s = (V_o - E)D_2T_s \tag{2.13}$$

Therefore, from (2.13),

$$\frac{V_o}{E} = \frac{D_1 + D_2}{D_2} \tag{2.14}$$

If the circuit is lossless,

$$P_L = P_o \Rightarrow \frac{I_o}{I_L} = \frac{D_2}{D_1 + D_2} \tag{2.15}$$

From (2.15),

(2.16)

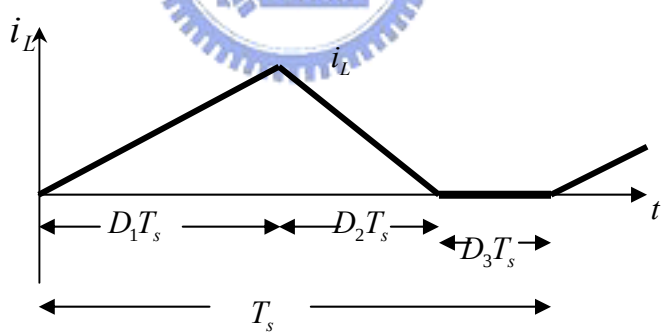


Fig.2-7 The inductor current under DCM

From Fig.2-7, we can get:

$$I_L = \frac{1}{2}\frac{ED_1T_s}{L}(D_1 + D_2) \tag{2.17}$$

From (2.16), (2.17), we can get the relation of D_1, D_2

$$D_2 = (\frac{L}{D_1 R T_s})(1+\sqrt{1+\frac{2D_1^2 R T_s}{L}}) \tag{2.18}$$

Therefore, (2.18) shows that change of D_1, D_2 is relative to loading under DCM. Compared to the condition under DCM, the duty ratio in CCM is simpler.

2.2 Analysis of Discrete Model

The discussion of the chaotic phenomenon of DC-DC converters starts from the modeling of chaotic systems. Chaos and quasi-periodicity are difficult to identify using standard time-domain simulations or frequency-domain measurements. They are usually identified by bifurcation diagrams. In order to capture a certain bifurcation diagram by means of simulation, we need to devise an elaborate procedure which may require the use of specific computational techniques. Some papers have proposed that the discrete modeling is suitable to observe the phenomenon of chaos[24-26]. Before describing the discrete modeling, some expressions are introduced.

2.2.1 Sampled Data

Several discrete time maps have been defined to develop the analysis of nonlinear phenomena in power electronics. The stroboscopic and the S-switching maps have been mostly used in converters. The S-switching map is sampled when a switch changes. Since the

samples of S-switching map are rare, the skipped cycle is ignored. The stroboscopic map is the most widely used discrete time model for DC-DC converters. This map can be obtained by observing the system dynamics every T seconds. Fig.2-8 and Fig.2-9 show the sampling types of waveforms under voltage and current modes respectively.

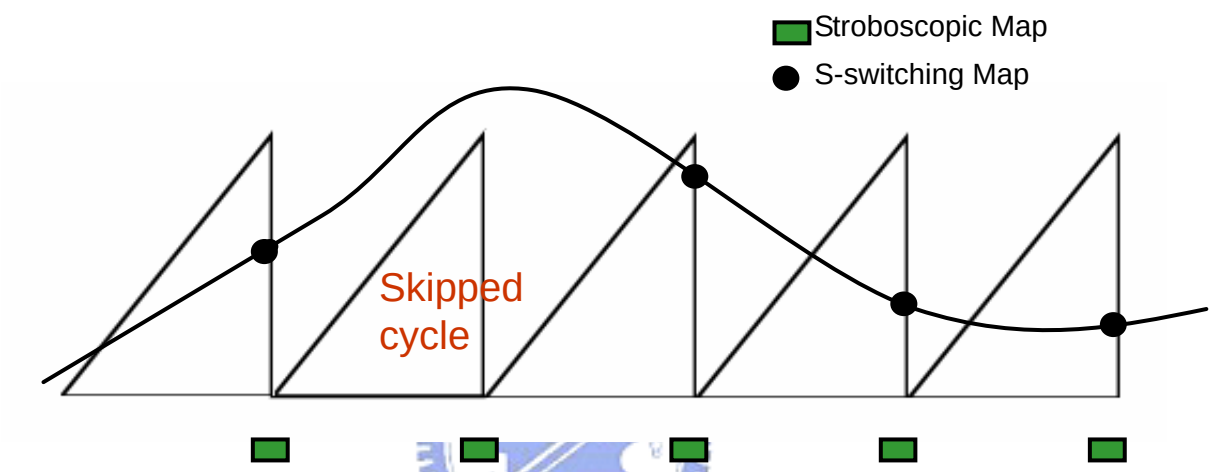


Fig.2-8 Sampling Types of control voltage and ramp waveforms under voltage mode control

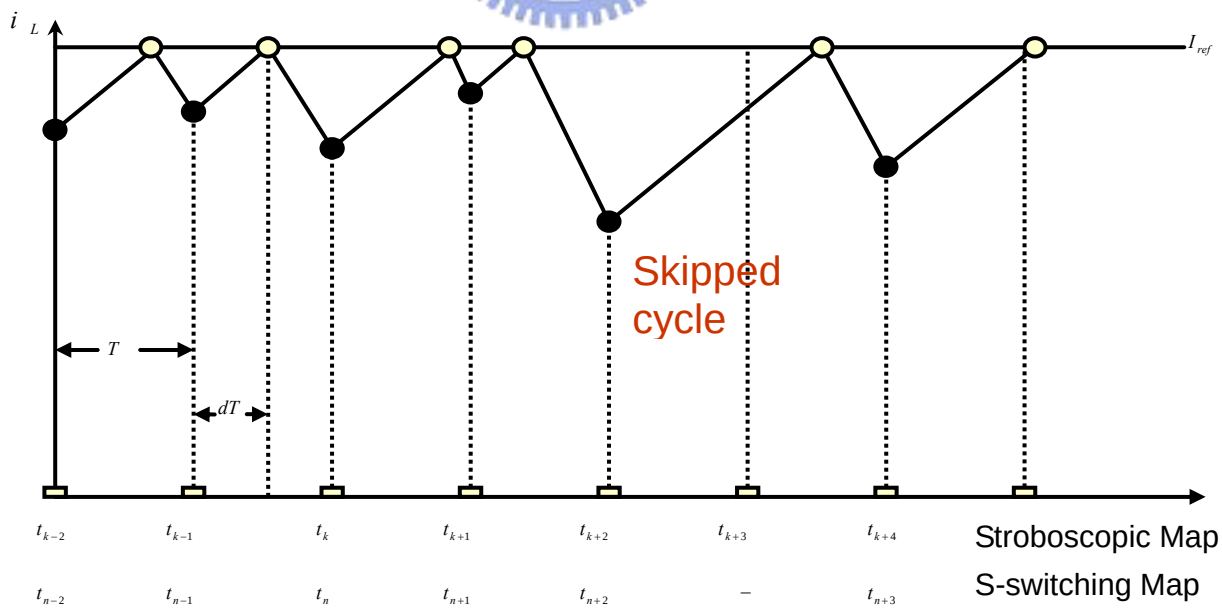


Fig.2-9 Sampling Types of the desired level and inductor current under current mode control

In this study, the model is built by the stroboscopic map. For periodical systems, like most of the fixed frequency switching converters, information can be easily obtained by sampling waveforms at constant intervals. Fig.2-10 illustrates how this sampling process reveals the periodicity of waveforms at period-1 and period-2 states by the stroboscopic map.

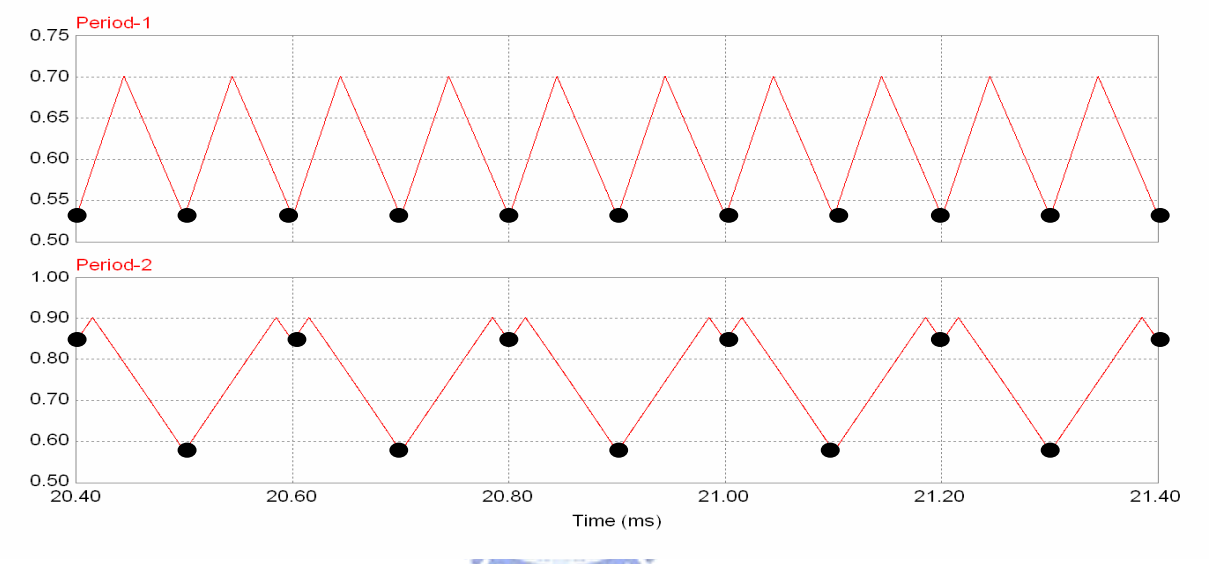


Fig.2-10 Waveform sampled at constant intervals giving (a)one fixed point(b) two fixed points.

2.2.2 Mapping

From Figure Fig.2-11, a mapping is a mathematical function that takes each point of a given space to another point. If a certain point in the space maps to itself, it is said to be a fixed point. A mapping F that converts a point in the n-dimensional real space R^n to another point in the same space can be written $F : R^n \mapsto R^n$, where F is a nonlinear transformation, and R^n is an n-dimensional space. In functional notation,

, where here x_n is the state variable. In this thesis, F is a discrete model of a converter.

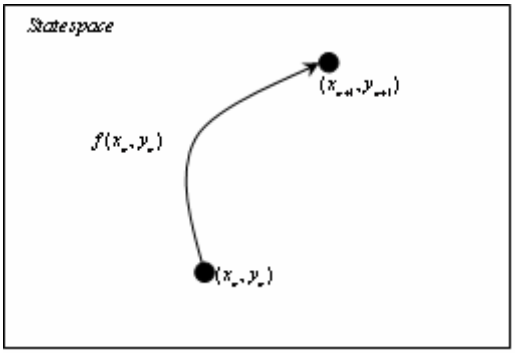


Fig.2-11 Illustration of a discrete mapping

2.2.3 Phase Portrait and Attractor

Suppose that the discrete model of a system is available. We can iterate the map starting from any initial condition and plot the discrete time evolution in the 2-D state space. The picture obtained is called a phase-portrait of the system. It can be a point, or region of the state space. If an initial condition is placed outside this region, in subsequent iterations of the map it moves to the set of points shown in the figure. If points in the state space are attracted to this region in the state space and in this sense the region shown in the figure is called an attractor. We can judge what state the system is by phase portrait and attractor.

Fig.2-12 from [26] presents a phase portrait of the converter at $E = 35V$ obtained from simulation. Because there are many attractors in Fig.2-12, it is under chaos state.

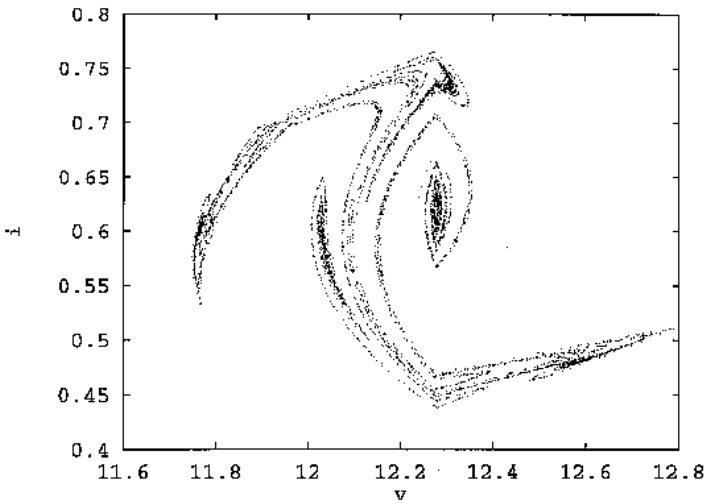


Fig.2-12 The phase portrait of the buck converter $E = 35V$

2.2.4 Bifurcation Diagram

The purpose for using bifurcation diagram is that operating state can be observed easily. In a bifurcation diagram, the characteristics of bifurcation for a system are exhibited by some parameters varying. For example Fig.2-13, most bifurcation diagram consists of an x-y plot, where sampled data are plotted against the chosen parameter.

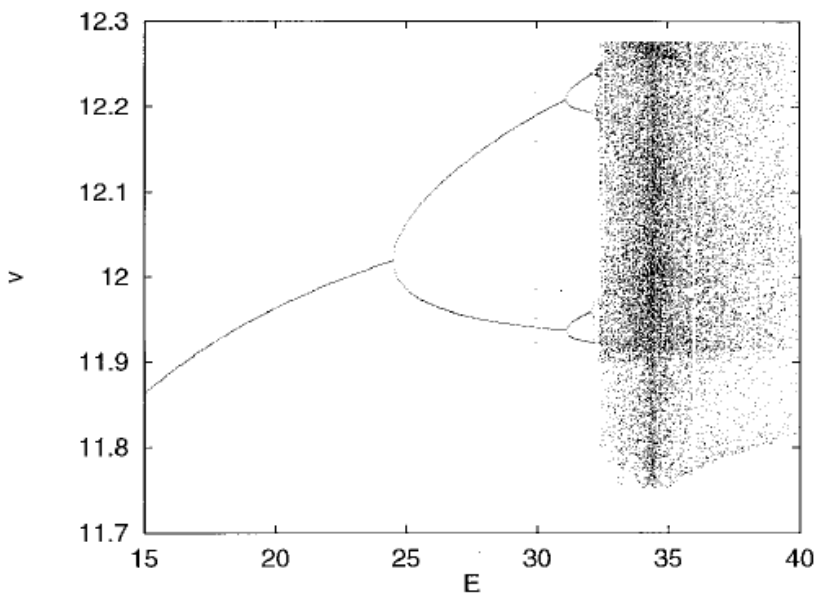


Fig.2-13 The bifurcation diagram of output and the parameter E

2-3 Model of a Boost Converter with Peak Current Control

The discussion of the chaotic phenomenon of DC-DC converters starts from the modeling of chaotic systems. Chaos and quasi-periodicity are difficult to identify using standard time-domain simulations or frequency-domain measurements. They are usually identified by bifurcation diagrams. In order to capture a certain bifurcation diagram by means of simulation, we need to devise an elaborate procedure which may require the use of specific computational techniques. Some papers have proposed that the discrete modeling is suitable to observe the phenomenon of chaos[24-26]. Before describing the discrete modeling, some expressions are introduced.

As the above-mentioned expression, a model of a boost converter with peak current control in CCM mode is discussed in the following example. First, we must build a formula for a boost converter. Fig.2-13 presents the conditions of different switch states for a boost converter. In Fig.2-13, we assume that the switch is on when $t_n \le t \le t'_n$, and the switch is off when $t_n' \le t \le t_{n+1}$. Besides, we assume the state variable are v_c and i_L. In Fig.2-13(a), when the switch is on, the behavior of the circuit is as:

$$\begin{bmatrix} v_c(t) \\ i_L(t) \end{bmatrix} = \begin{bmatrix} v_c(t_n)e^{-(t-t_n)/RC} \\ i_L(t_n) + \dfrac{E(t-t_n)}{L} \end{bmatrix} \quad t_n \le t \le t_n' \tag{2.20}$$

From (2.20), when $t = t_n'$, the following expression can be yielded:

$$v_c(t_n^{'}) = v_c(t_n)e^{-dT/RC}$$
$$i_L(t_n^{'}) = i_L(t_n) + \frac{E(t_n^{'} - t_n)}{L} \quad \text{when} \quad t = t_n^{'} \tag{2.21}$$

In Fig.2-13(b), when the switch is off, (2.21) can be as the initial state in the mode and the following expression can be yielded:

$$\begin{aligned} v_c(t) &= E + K_1 e^{-\frac{1}{2RC}(t-t'_n)} \cos\omega(t - t_n^{'}) + \\ &\quad \frac{k_2 - k_1 * \frac{1}{2RC}}{\omega} e^{-\frac{1}{2RC}(t-t_n^{'})} \sin\omega(t - t_n^{'}) \\ i_L(t) &= \frac{E}{R} + K_3 e^{-\frac{1}{2RC}(t-t_n^{'})} \cos\omega(t - t_n^{'}) + \\ &\quad \frac{k_4 - k_3 * \frac{1}{2RC}}{\omega} e^{-\frac{1}{2RC}(t-t_n^{'})} \sin\omega(t - t_n^{'}) \end{aligned} \tag{2.22}$$

, where

$$\omega = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$
$$k_1 = v_c(t_n^{'}) - E$$
$$k_2 = \frac{1}{C} i_L(t_n^{'}) - \frac{E}{RC}$$
$$k_3 = i_L(t_n^{'}) - \frac{E}{R}$$
$$k_4 = \frac{1}{RC} i_L(t_n^{'}) - \frac{1}{L} v_c(t_n^{'}) + (\frac{R}{L} - \frac{1}{RC})\frac{E}{R}$$

From (2.22), if $t = t_{n+1}$, $t_{n+1} - t^{'}_n = (1-d)T$, the form of this difference equation is

$$x(t_{n+1}) = f(x(t_n), d) \tag{2.23}$$

, where

$$f(x,d) = \begin{bmatrix} A_1 & A_2 \\ A_3 & A_4 \end{bmatrix} x + \begin{bmatrix} B_1 \\ B_2 \end{bmatrix} E \tag{2.24}$$

and

$$A_1 = e^{-\frac{dT}{CR}-\frac{1}{2CR}(1-d)T}[\cos(1-d)wT - \frac{1}{2RCw}\sin(1-d)wT]$$

$$A_2 = \frac{1}{wC}e^{-\frac{1}{2RC}(1-d)T}\sin(1-d)wT$$

$$A_3 = -\frac{1}{wL}e^{-\frac{dT}{CR}-\frac{1}{2RC}(1-d)T}\sin(1-d)wT$$

$$A_4 = e^{-\frac{1}{2RC}(1-d)T}[\cos(1-d)eT + \frac{1}{w}(\frac{1}{RC}-\frac{1}{2RC})\sin(1-d)wT]$$

$$B_1 = 1 - e^{-\frac{1}{2RC}(1-d)T}[\cos(1-d)eT - \frac{1}{w}(\frac{dT}{LC}-\frac{1}{2RC})\sin(1-d)wT]$$

$$B_2 = 1/R\{1 + e^{-\frac{1}{2RC}(1-d)T}[(\frac{RdT}{L}-1)*\cos(1-d)wT + \frac{1}{w}*[(\frac{1}{RC}-\frac{1}{2RC})\frac{RdT}{L} + \frac{R}{L}-\frac{1}{2RC}]\sin(1-d)wT]\}$$

In the open loop for a boost converter under current mode control, the control parameter of interest is the reference current I_{ref}. Furthermore, duty ratio d is a main factor for controlling output voltage, and d_n presents the iteration parameter of d. Therefore, the relation between I_{ref} and d_n can present in following expression:

$$L\frac{di_L}{dt} = L\frac{I_{ref} - i_{L,n}}{d_n T} = E$$

$$=> d_n = \frac{I_{ref} - i_{L,n}}{(E/L)T} \tag{2.25}$$

So the discrete model of the boost converter in open loop is

$$\begin{bmatrix} v_{C,n+1} \\ i_{L,n+1} \end{bmatrix} = \begin{bmatrix} A_1(d_n) & A_2(d_n) \\ A_3(d_n) & A_4(d_n) \end{bmatrix}\begin{bmatrix} v_{C,n} \\ i_{L,n} \end{bmatrix} + \begin{bmatrix} B_1(d_n) \\ B_2(d_n) \end{bmatrix}E \tag{2.26}$$

Table 2-1

E	L	C	R	f_s	I_{ref}
4	$1m$	$120u$	20	$10k$	$0.7 \sim 1.6$

We define a set of specification in Table 1 and employ the Matlab tool to iterate (2.26). When I_{ref} varies, the sampled data of the inductor i_L always change, too. The bifurcation diagram is presented in Fig.2-. We can find the way from a period-1 to chaos. When $I_{ref} \le 0.87A$, the system operates under period-1 state. When $I_{ref} > 0.87A$, the system is under the period-doubling state. Finally, when the reference current I_{ref} increases up to a level, $I_{ref} > 1.52A$, operating state can not be judged. We define the state to be a chaos state.

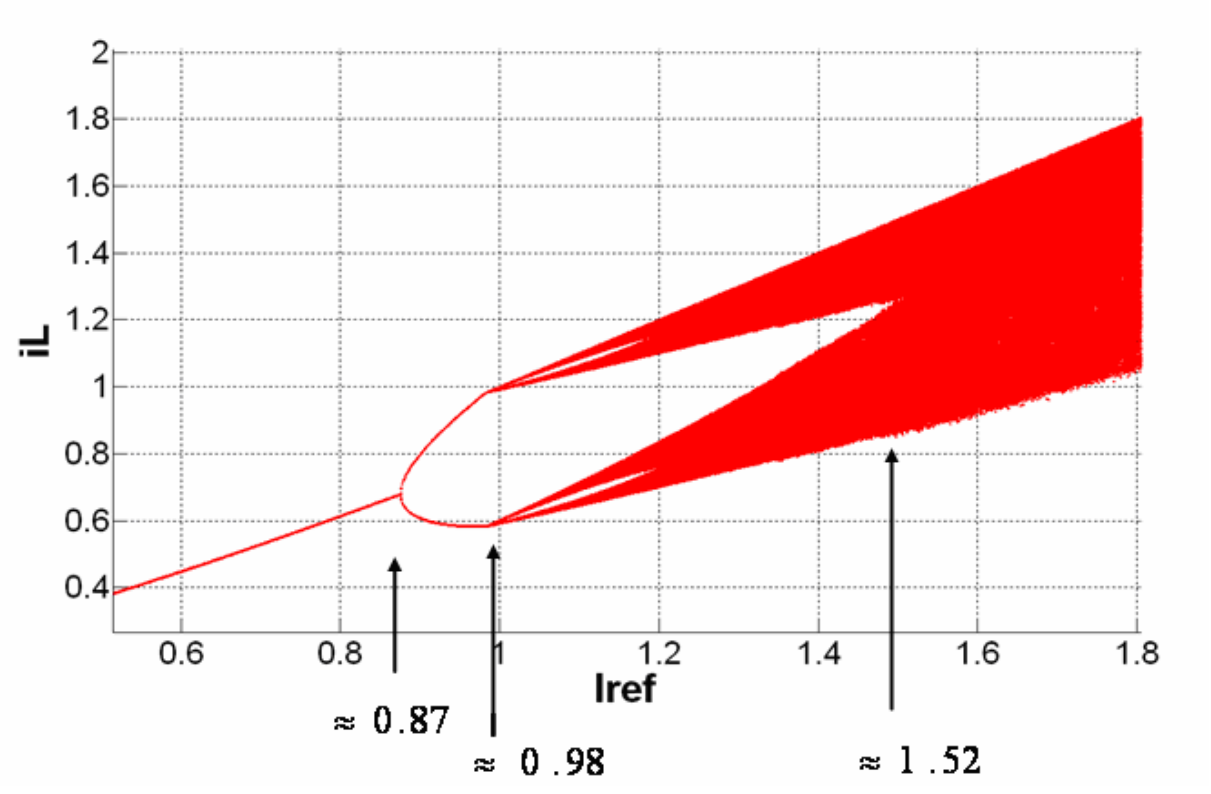


Fig.2-14 The bifurcation diagram of the boost converter by I_{ref} varying

Chapter3
Design of Converters with Chaos Generator

Compared to the Chua's circuit [22, 23], we propose a circuit as a chaotic generator. It is similar to that discussed in[27] for the theory . It does not involve any inductor like other popular chaos generator architectures such as Chua's circuits; hence, it is particularly compatible to fully analog on-chip realization

3.1 Modeling of Chaos Generator

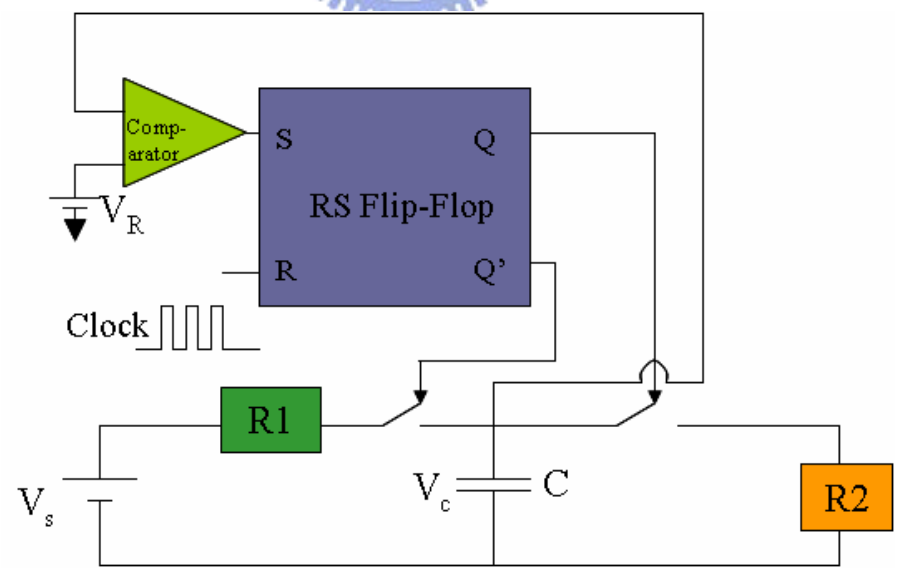


Fig.3-1 Schematic of chaos generating circuit

Fig.3-1 shows the schematic of simple chaotic generator. The circuit mainly consists of a

DC voltage, two resisters, two switches, a comparator, a reference voltage, and a R-S latch. The process is controlled by a set-rest latch. The clock signal is an impulse train at frequency $f_c = \frac{1}{T}$. The impulse train is using a periodic waveform with a period T and a low duty cycle. Firstly, when clock generator sends a high level signal to R edge, $\overline{Q}$ edge is on high level and drives the switch1. The capacitor C is charged by a voltage source V_s through a resister R_1. In addition, the comparator provides a high level signal and sends to S edge when the capacitor voltage reaches a reference voltage V_R which is a desired value. Therefore, Q sends a high level signal and makes the switch2 turn on. The capacitor C is discharged to ground through a resister R_2. Because of the motion of the switches turning on and off repeatedly, a signal of charging and discharging is produced.

Fig.3-2 shows the derivation of the capacitor voltage. When the switch1 is on, the switch2 is off. Thus, the capacitor is charged. The behavior of the circuit is as

$$C\frac{dv_c}{dt} = \frac{V_s - v_c}{R_1} \tag{3.1}$$

,where V_c is the capacitor voltage.

When the switch2 is on, the switch1 is off. So, the capacitor is discharged. The behavior of the circuit is as

$$C\frac{dv_c}{dt} + \frac{v_c}{R_2} = 0 \tag{3.2}$$

From (3.1), (3.2), we get

$$v_c(t) = V_s - (V_s - v_c(n))e^{-\frac{t-t_n}{R_1 C}} \quad t_n < t < t_{\mathrm{R}} \tag{3.3}$$

$$v_c(t) = V_R e^{-\frac{t-t_R}{R_2 C}} \quad t_R < t < t_{n+1} \tag{3.4}$$

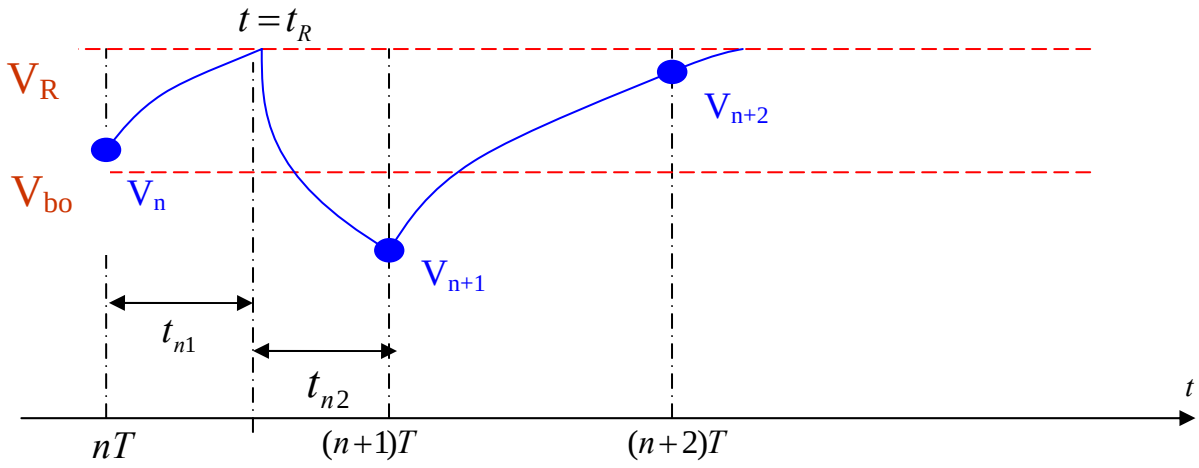


Fig.3-2 The derivation of the capacitor voltage

In order to build a model of the circuit, we employ stroboscopic map to describe the behavior of the circuit. First of all, as shown in Fig.3-2, we define a borderline voltage V_b and V_n which is the value of $v(t)$ at t_n. When $V_n > V_b$, the capacitor charges for a time t_{n1}, and t_{n1} is smaller than a period T. On the other hand, when $V_n < V_b$, the capacitor charges and the waveform has no effect on the next clock pulse until the V_R. The time t_{n1} is over a period T.

From (3.3), assuming that $t = t_R$, $t_{n1} = t_R - t_n$, we can calculate the t_{n1} as

$$V_s - (V_s - v_c(n))e^{-\frac{t_{n1}}{R_1 C}} = V_R$$

$$\Rightarrow t_{n1} = R_1 C \ln\left(\frac{V_s - v_c(n)}{V_s - V_R}\right) \tag{3.5}$$

From (3.5), if $t_{n1} = T$, the capacitor voltage is the borderline voltage V_b,

$$v_c(n) = V_b = V_s - (V_s - V_R)e^{-\frac{T}{R_1 C}} \tag{3.6}$$

Therefore, when $v_c(n) > V_b$, the next sample value of the capacitor voltage is as

$$v_c(n+1) = V_s - (V_s - v_c(n))e^{-\frac{T}{R_1 C}} \tag{3.7}$$

When $v_c(n) < V_b$, assuming $d = \frac{t_{n1}}{T}$ and $1-d = \frac{t_{n2}}{T}$ we can get $v_c(n+1)$ from (3.4)

$$\begin{aligned} v_c(n+1) &= V_R e^{-\frac{t_{n2}}{R_2 C}} \\ &= V_R e^{-\frac{(1-d)}{R_2 C}T} \\ &= V_R e^{-\frac{T}{R_2 C}} \left(\frac{V_s - v_c(n)}{V_s - V_R}\right)^{R_1/R_2} \end{aligned} \tag{3.8}$$

Therefore, from (3.7) and (3.8), the stroboscopic map of the system is as:

$$v_c(n+1) = \begin{cases} V_s - (V_s - v_c(n))e^{-\frac{T}{R_1 C}} & v_c(n) \le V_b \\ V_R e^{-\frac{T}{R_2 C}} \left(\frac{V_s - v_c(n)}{V_s - V_R}\right)^{R_1/R_2} & v_c(n) > V_b \end{cases} \tag{3.9}$$

3-2 Simulation of Numerical Analysis

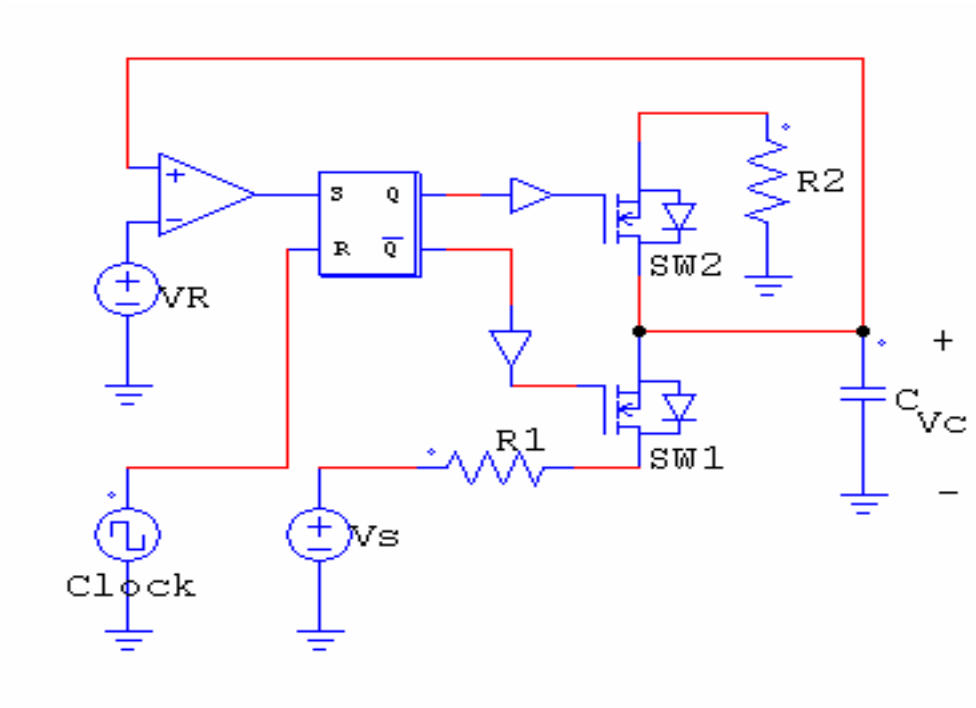


Fig.3-3 The circuit frame of the new chaos generator

Fig.3-3 is the circuit frame of the new chaos generator. The circuit parameters are listed in Table 3-1. Based on the iterating map from (3.9), we can generate the bifurcation diagram handily and fast. By controlling the V_s as the bifurcation parameter, we periodically collect the discrete-time values of v_c with the initial transient discarded. Thus, we have one set of data for each value of V_s. A bifurcation diagram can then be constructed after a sufficient number of data sets are obtained as shown in Fig.3-4.

Fig.3-4 presents the results of the way from period-1 to chaos. The relationship of system states and controlling parameter V_s is shown in Table 3-. It is worth noting that the circuit generates chaotic signal when V_s is less than $11.7V$ from Table 3-. Moreover, the waveforms of different states in time domain are shown in Fig.3-5.

Table 3-1 The specifications of the boost converter

V_s	V_R	C	R_1	R_2	T
15~7V	5	1uF	200	100	1/100K

Table 3-2 The relation of operating states and V_s

V_s	**State**
$>14.28V$	**Period-1**
$13.65V \sim 14.28V$	**Period-2**
$11.71V \sim 13.68V$	**Period-4**
$<11.71V$	**Chaos**

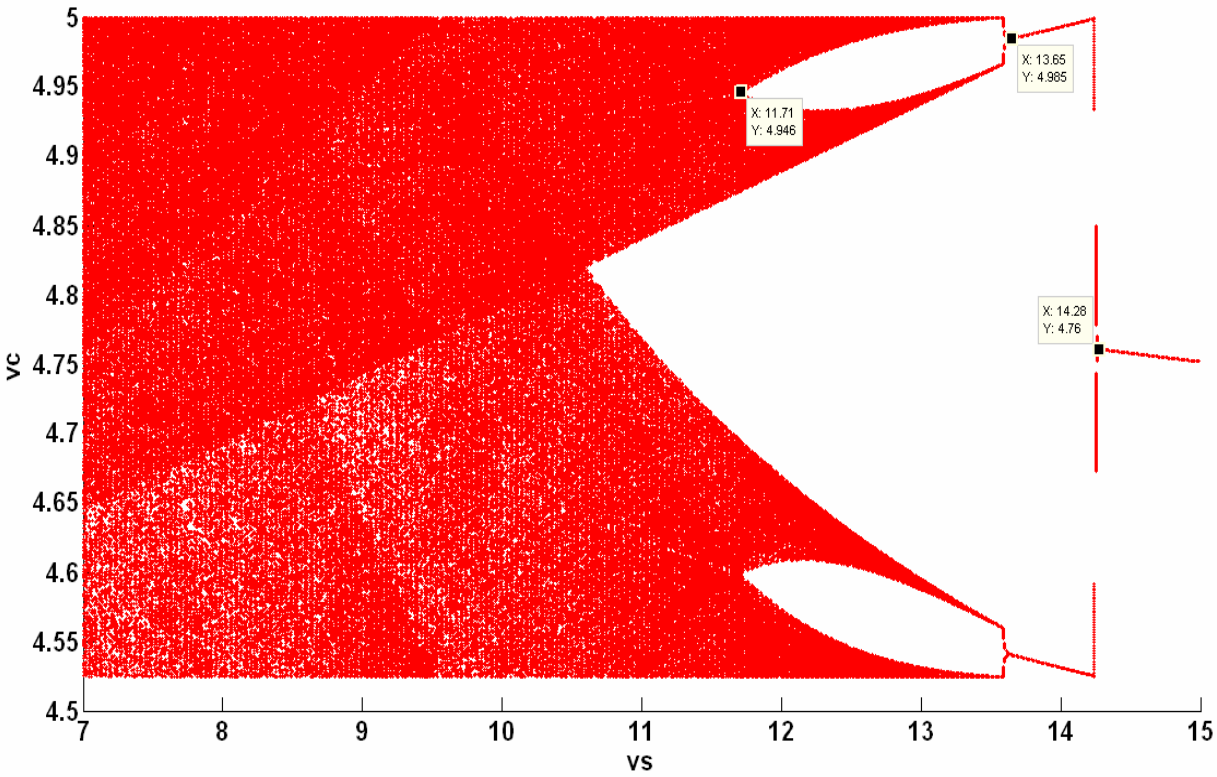
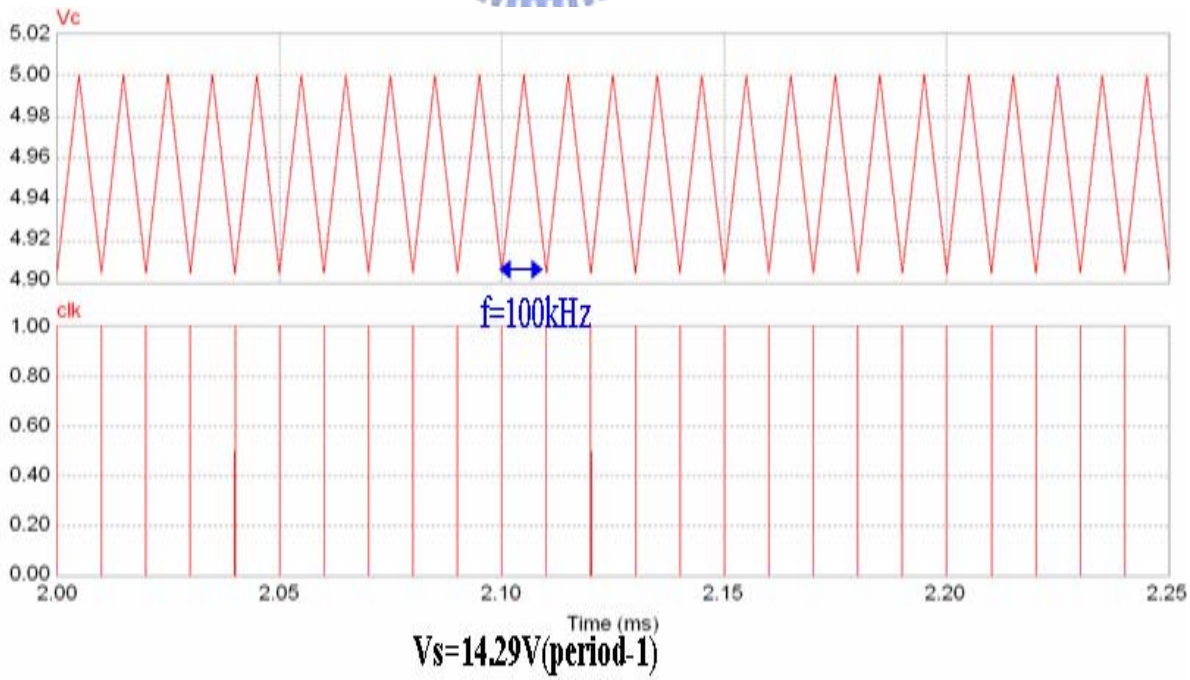
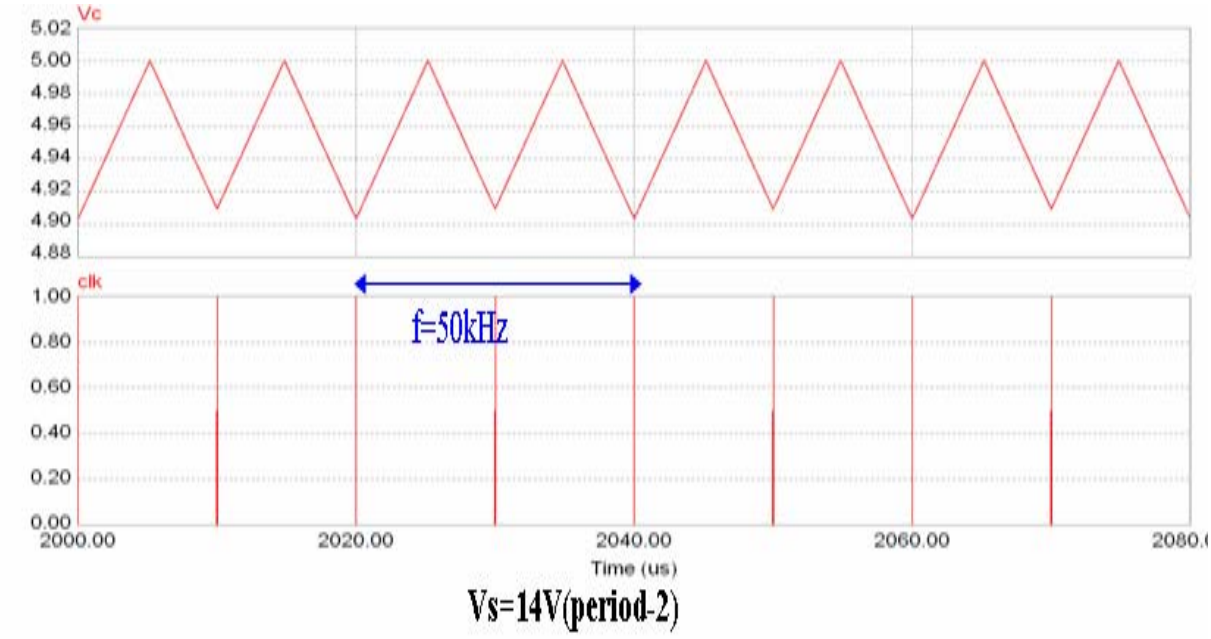


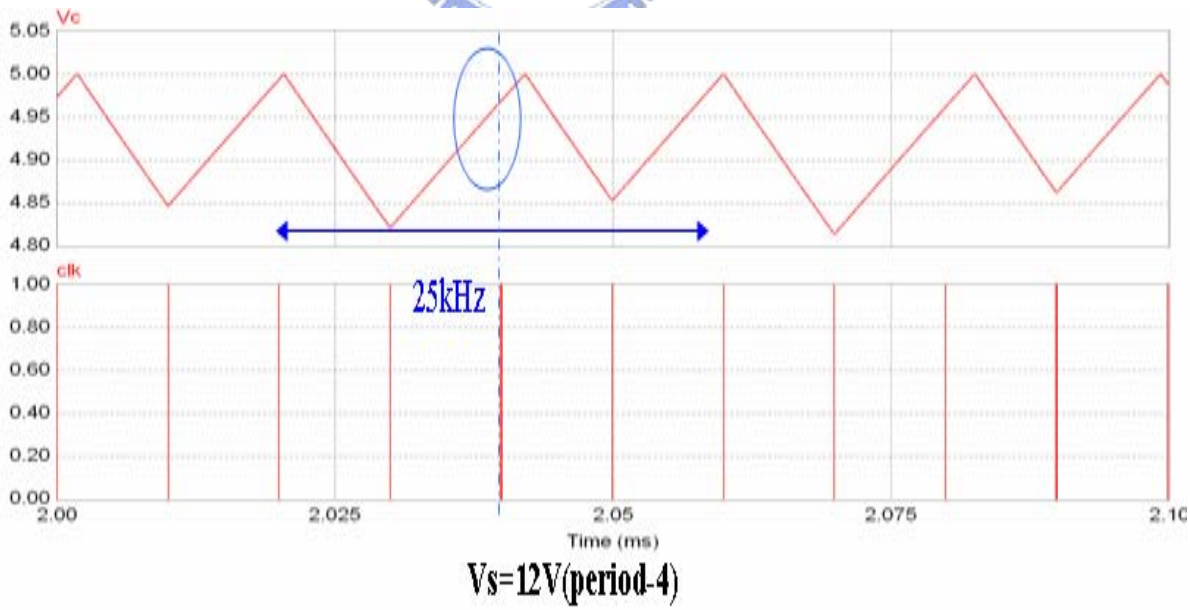
Fig.3- 4 Bifurcation Diagram of the Chaos Generator



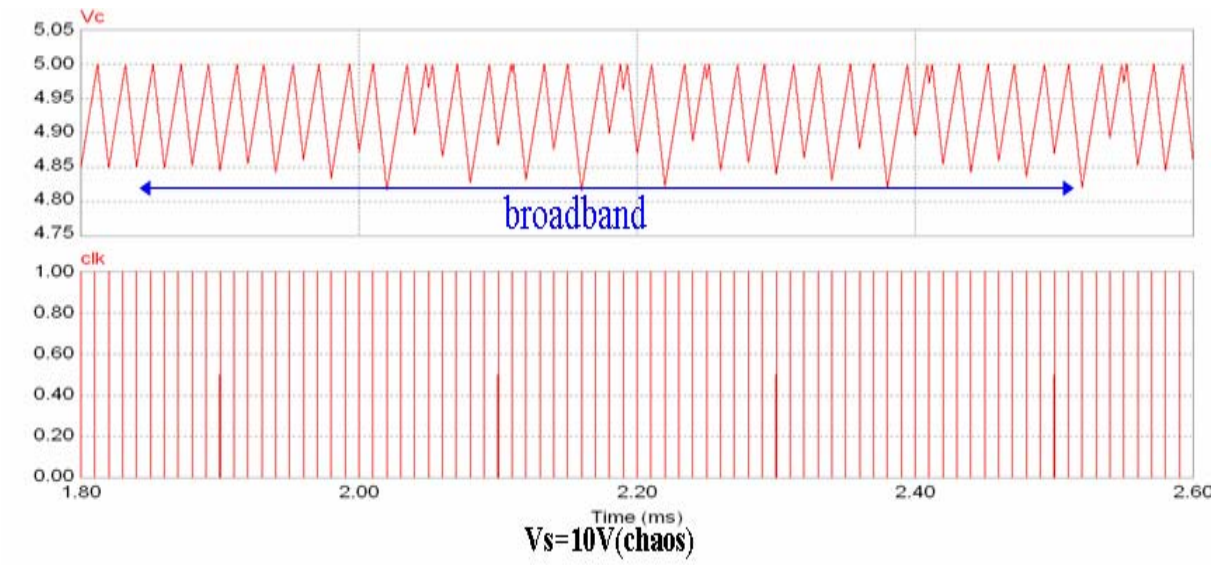
(a) Period-1 (V_s=14.29V)



(b) Period-2 (V_s=14V)



(c) Period-4 (V_s=12V)



(d) Chaos (V_s=10V)

Fig.3-5 The waveforms of different states in time domain

3.3 A Current-Controlled Boost Converter without Chaos Generators

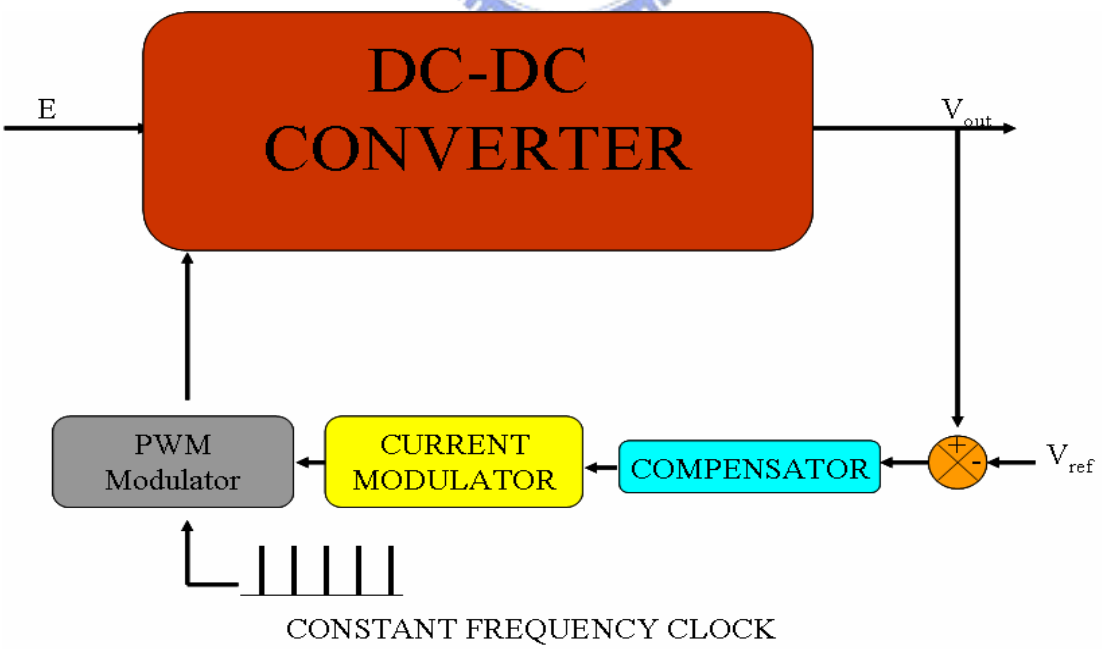


Fig.3-6 blocks of the close loop circuit with constant frequency signal

In order to introduce DC-DC converters with chaos generators, we firstly describe an

operating condition of a boost converter without chaos generators. The system consists of a DC-DC converter, a compensator, a current modulator, and a PWM modulator. Fig.3-6 shows the blocks in close loop. When the system is at transient state, the output voltage and reference voltage are always adjusted to the desired voltage level. The error signal produced by the output voltage and reference voltage passes through the compensator which makes system operate stably in period-1 state. A signal from the compensator becomes a peak level of the inductor current to control the inductor current in current modulator block. Finally, in the driving circuit block, a S-R flip-flop is controlled to generate a switch signal by the constant frequency clock signal and the modulation signal. By adjusting the output voltage continuously, a set of switching signals are produced to make the system stay in steady state.

When duty ratio is small than 0.5 in peak current control, it is stable in period-1 state. Therefore we assume a specification of a boost converter operating in the period-1state:

$$\begin{aligned} V_{in} &= 20 \sim 32V, \\ P_{o-\max} &= 140W, \\ f_s &= 100kHz, \\ V_o &= 40V, \\ Duty &= 0.2 \sim 0.5 \end{aligned} \tag{3.10}$$

In addition, the simulations will be shown in Chapter 4.

3.4 A Current-Controlled Boost Converter with Chaos Generators

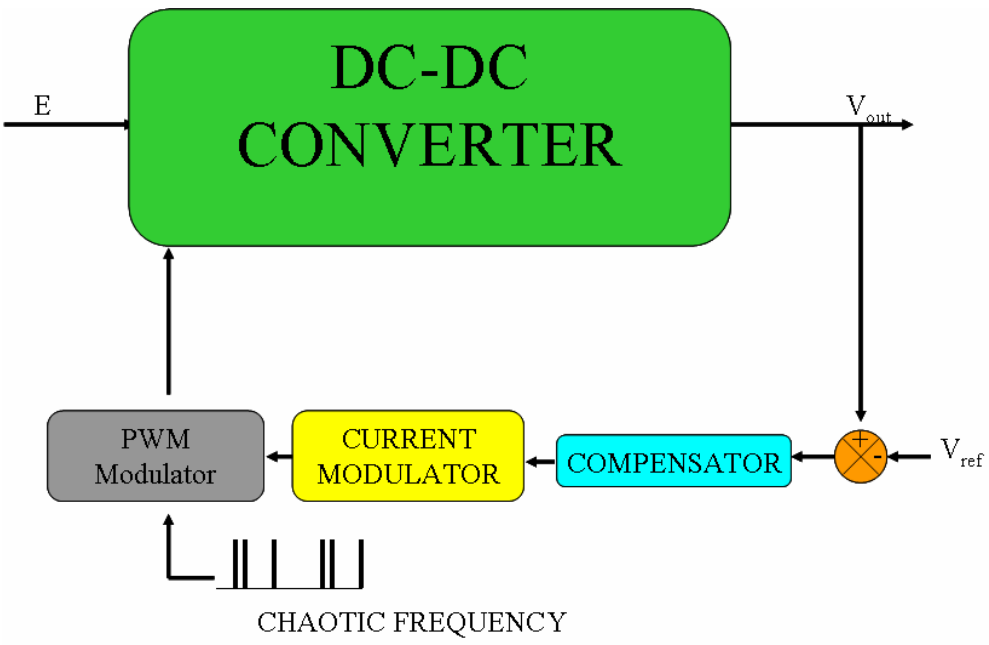
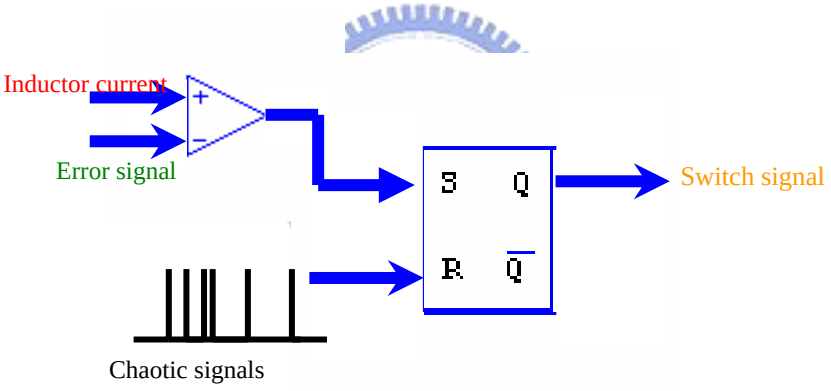
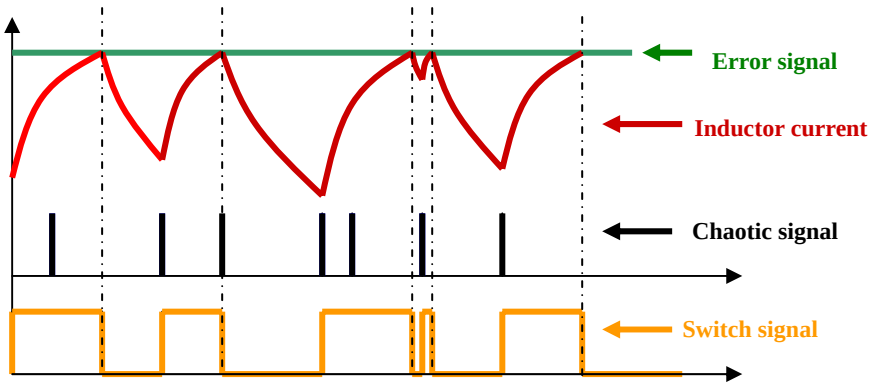


Fig.3-7 blocks of the close loop circuit with chaotic signal



(a)



(b)

Fig.3-8 The behavior of driving circuit (a) the circuit of S-R flip-flop(b) the signals of driving circuit

Compared with Fig.3-6, the main point in Fig.3-7 is the block of driving circuit. A set of chaotic clock signals and modulation signals are used for a S-R flip-flop. In Fig.3-8(a), because the Q signal of S-R flip-flop can control the switch to turn on: therefore a system can be operated to be under the chaos state when the S signal of S-R flip-flop is chaotic. It is worth noting that the switch is still to be on when the inductor current charges and R signal have a pulse at that time. Fig.3-8(b) illustrates the behavior of driving circuit.

3.5 Analysis of Stability of a Boost Converter with Chaos Generators

Because important point is stability for a DC-DC converter, therefore we analyze the stability of a boost converter with chaos generator in the section

3.5.1 The Clopes of Charge and Discharge of an Inductor Current in a Boost Converter under Current Mode Control

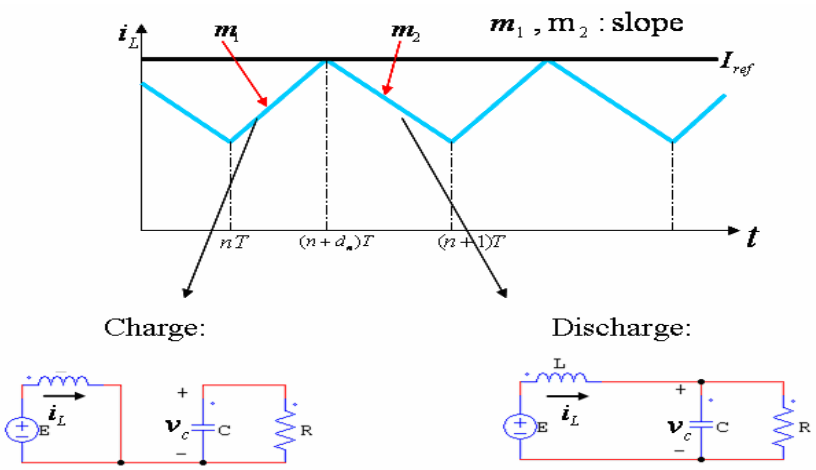


Fig.3-9 Inductor current waveform of the boost converter under current-mode control

Fig.3-9 presents the behavior of the inductor current waveform of the boost converter under current mode control. When the inductor charges, the slope of the inductor is yielded:

$$\frac{I_{ref} - i_{L,n}}{d_n T} = \frac{E}{L} = m_1 \tag{3.11}$$

Where I_{ref} is a reference current, E is the input voltage. When the inductor discharges, the slope of the inductor is yielded:

$$\frac{I_{ref} - i_{L,n+1}}{(1-d_n)T} = -\frac{E - v_c}{L} = m_2 \tag{3.12}$$

When the system is in the steady sate, the v_c is constant. Therefore, from (18) and (19), m_1 and m_2 is constant in the steady state.

3.5.2 The Influence of the Gain of PWM Circuit and Current Modulator

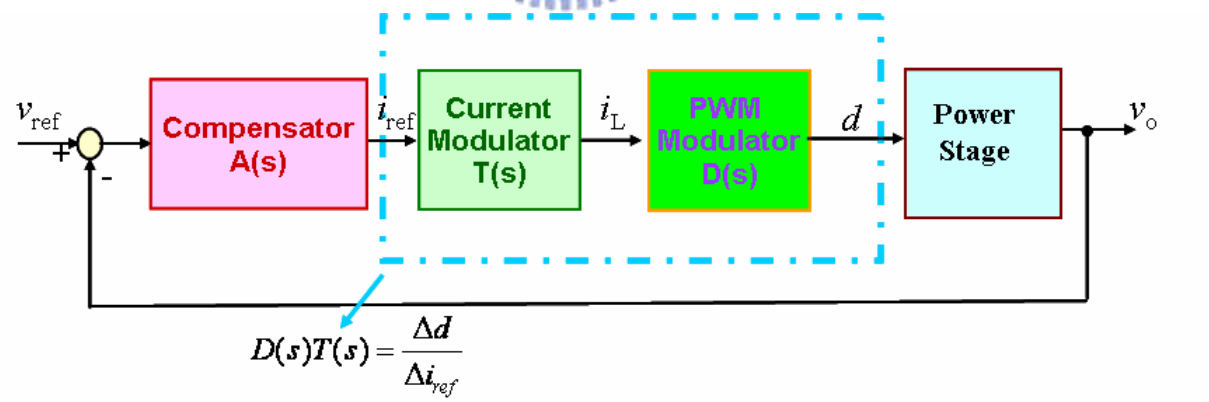


Fig.3-10 Block diagrams of a close-loop for a power converter with current control

In the beginning, we must analyze the influence of the gain of driving circuit and current modulator when the clock signal is varying. Fig.3-10 presents block diagrams of a close loop for a power converter with peak current control. It must be noted for the gain of PWM

modulator and current modulator. Fig.3-11 analyzes in detail the influence. There are an inductor current in the steady state, the rising slope of an inductor current, duty ratios, different currents ,the reference currents I_{ref1} , I_{ref2}, and varying frequency clock signals in Fig.3-11. The relations of duty ratio and the difference of reference current are presented in the following expression:

$$\frac{\Delta d}{\Delta I_{ref}} = \frac{(D_1 - D_2)T_1}{T_1} \frac{1}{I_{ref1} - I_{ref2}} = \frac{1}{m_1} \tag{3.13}$$

$$\frac{\Delta d}{\Delta I_{ref}} = \frac{(D'_3 - D'_3)T_3}{T_3} \frac{1}{I_{ref1} - I_{ref2}} = \frac{1}{m_1} \tag{3.14}$$

When the system is in the steady state, the slopes of charge and discharge of an inductor current are constant. Therefore, (3.13) and (3.14) depict that the gain are not affected in despite of the varying frequency of clock signals.

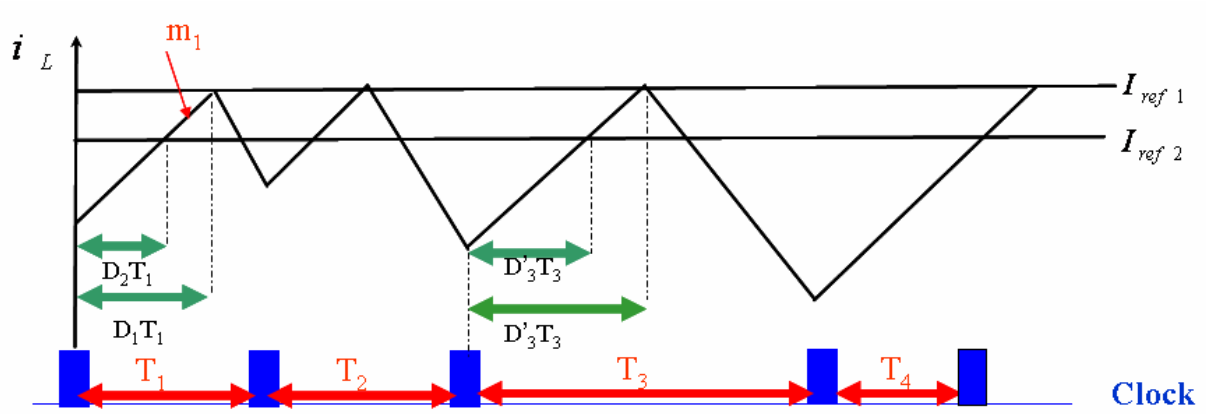


Fig.3-11 The inductor current waveform for different reference currents

3.5.3 Analysis of Period-1

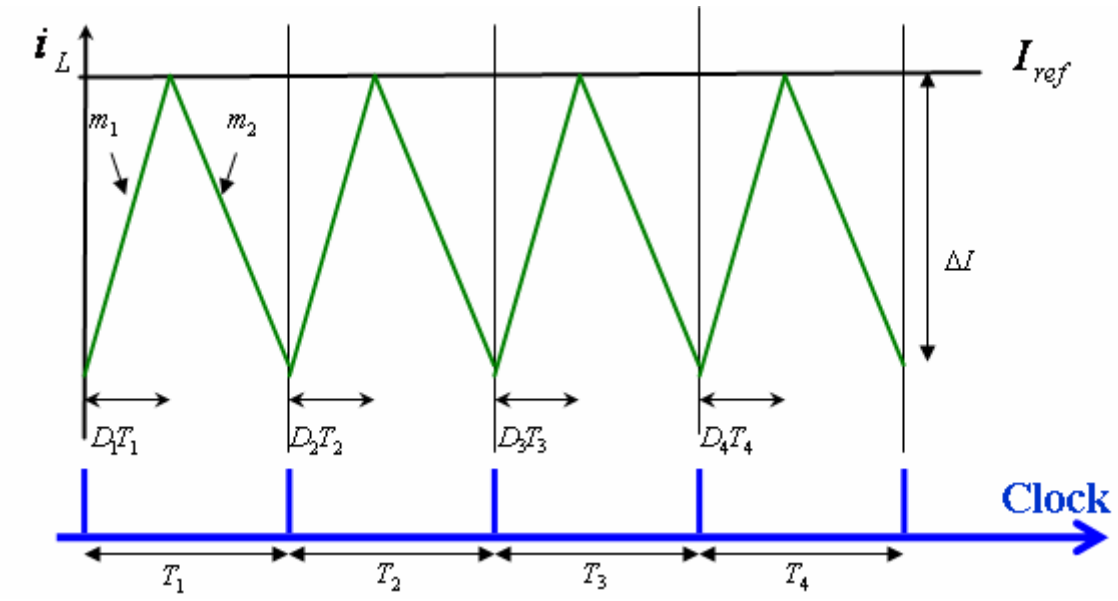


Fig.3-12 The inductor current waveform in period-1

Fig.3-12 indicates the behavior of an inductor current in steady state under period-1 state. We assume the duty ratio D and period T are as:

$$D = D_1 = D_2 = D_3 = D_4 \tag{3.15}$$

$$T = T_1 = T_2 = T_3 = T_4 \tag{3.16}$$

$$D_{ave\_period-1} = \frac{D_1T_1}{T_1} = \frac{D_1T_1 + D_2T_2}{T_1 + T_2} = D \tag{3.17}$$

In addition, because of the slopes of charge and discharge for an inductor current, we can define the peak-to-peak value of the inductor current is ΔI. Thus the slope of charge m_1 and the slope of discharge m_2 are as:

$$m_1 = \frac{\Delta I}{D_1T_1} \tag{3.18}$$

$$m_2 = -\frac{\Delta I}{(1-D_1)T_1} \tag{3.19}$$

$$D_1 = D = \frac{m_2}{m_2 - m_1} \tag{3.20}$$

3.5.4 Analysis of Period-2

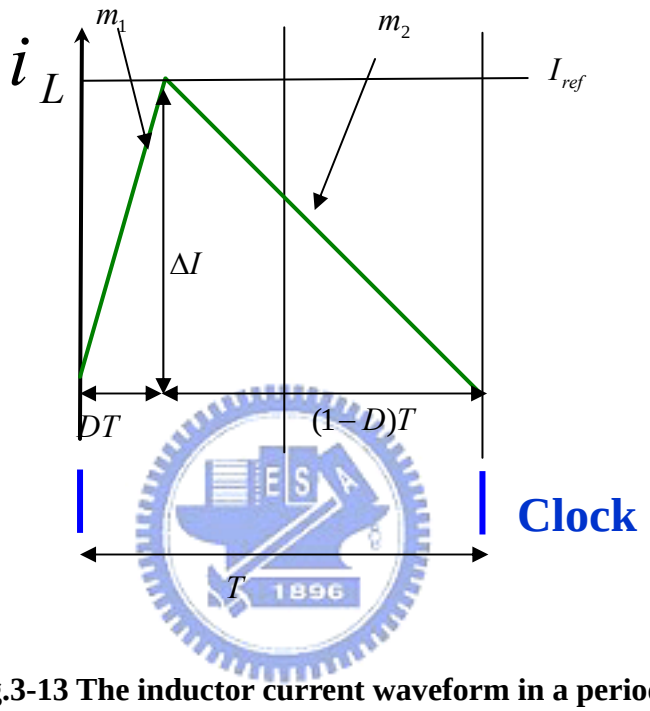


Fig.3-13 The inductor current waveform in a period T

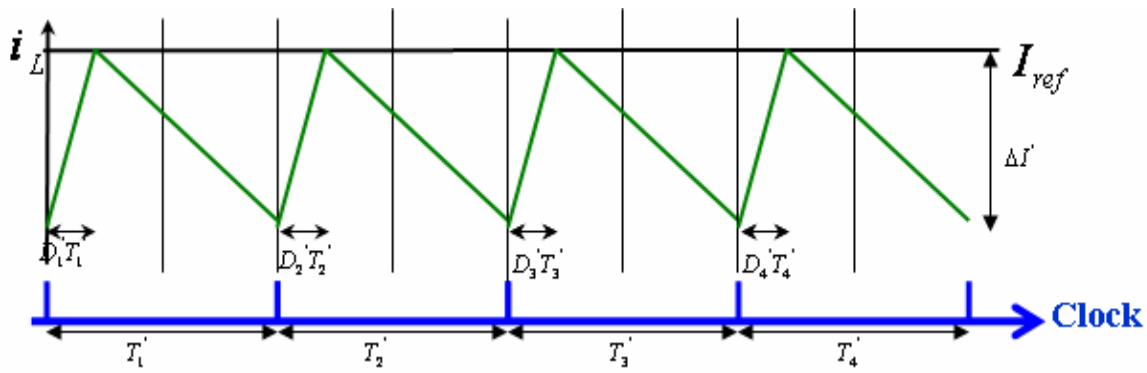


Fig.3-14 The inductor current waveform in period-2

Before analyzing the condition under period-2 state, we discuss the relation of the

peak-to peak value of the inductor current and a period T. From Fig.3-13, (3.18) and (3.19), m_1 and m_2 can be as:

$$\Delta I = \frac{m_1 m_2 T}{m_2 - m_1} \tag{3.21}$$

So, from (3.20), we can know

$$\Delta I \propto T \tag{3.22}$$

Because the clock frequency becomes slower, the duration that an inductor current charge and the period of an inductor current is in the period-2 state. Fig.3-14, we assume the relation of duty ratio $D^{'}$, a period $T^{'}$, and duty ratio in the period-2 state are as:

$$D^{'} = D_1^{'} = D_2^{'} = D_3^{'} = D_4^{'} \tag{3.23}$$

$$2T^{'} = T^{'} = T_1^{'} = T_2^{'} = T_3^{'} = T_4^{'} \tag{3.24}$$

$$m_1 = \frac{\Delta I^{'}}{D_1^{'} T_1^{'}} = \frac{\Delta I^{'}}{D^{'} T^{'}} \tag{3.25}$$

From (3.23), because $T^{'} = 2T$,

$$\Delta I^{'} = 2\Delta I \tag{3.26}$$

From(3.11), (3.18), (3.19), (3.25) and (3.26)

$$m_1 = \frac{E}{L} = \text{constant} = \frac{\Delta I}{DT} = \frac{\Delta I^{'}}{D^{'} T^{'}} \tag{3.27}$$

$$=> D^{'} T^{'} = 2DT \tag{3.28}$$

So, the average duty ratio in period-2 state is as:

$$D_{ave\_period-2} = \frac{D_1^{'}T_1^{'} + D_2^{'}T_2^{'} + D_3^{'}T_3^{'} + D_4^{'}T_4^{'}}{T_1^{'} + T_2^{'} + T_3^{'} + T_4^{'}} = \frac{8DT}{8T} = D \qquad (3.29)$$

3.5.5 Analysis of Period-4

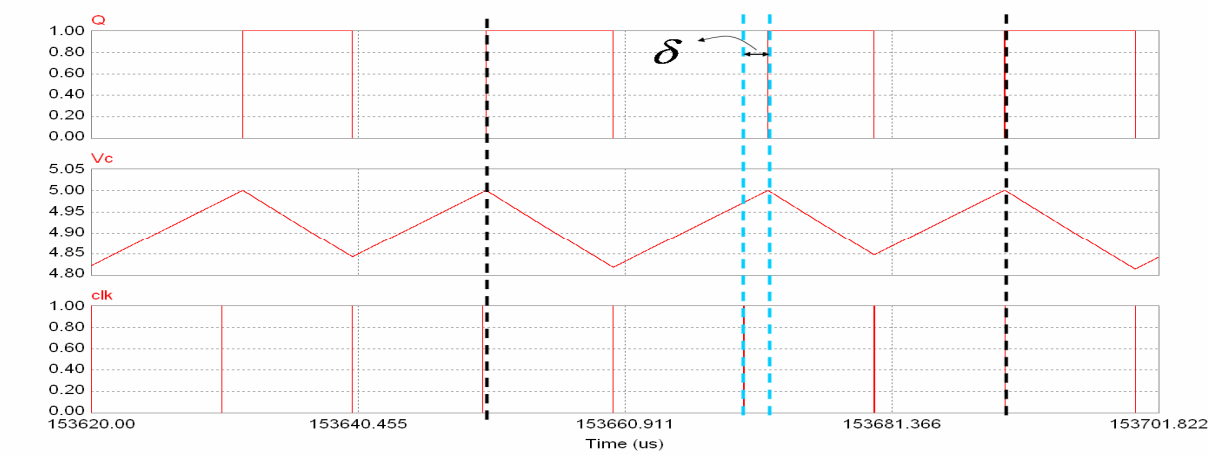


Fig. 3-15 The waveform of Q signal in period-4 state

Because clock signal is mainly generated by Q signal ,we observe the Q signal by chaos signal. From Fig.3-15, because the quality of chaos, a small difference causes period-2 state to be period-4 state.

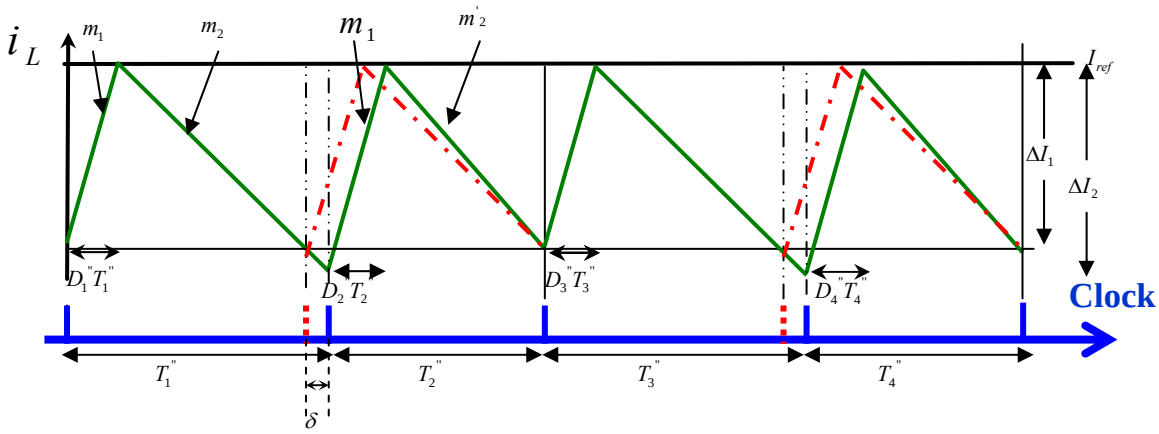


Fig.3-16 The inductor current waveform in period-4

Fig.3-16 presents the inductor current waveform in period-4 state. We define a period in the period-4 state as $T_1^{''} + T_2^{''}$, where $T_1^{''} = T^{'} + \delta$, $T_1^{''} = T^{'} - \delta$ and δ have small differences. The dotted line presents the inductor current in the period-2 state and the solid line presents the inductor current in the period-4 state. Because a pulse of clock signal delays in period-4 state, the duration of the inductor discharged becomes longer. Besides, because the slope of discharge of the inductor current is equal to $m_2 = -\frac{v_{out}(t) - E}{L}$, it results in the inconsistency the slope of discharge of the inductor current. But the slope of charge of the inductor current is still constant. From Fig.3-16, we define the slopes as:

$$m_1 = \frac{\Delta I_1}{D_1^{''} T_1^{''}} = \frac{\Delta I_2}{D_2^{''} T_2^{''}} \tag{3.30}$$

$$m_2 = \frac{-\Delta I_2}{(1 - D_1^{''}) T_1^{''}} \tag{3.31}$$

$$m_2^{'} = \frac{-\Delta I_1}{(1 - D_2^{''}) T_2^{''}} \tag{3.32}$$

, where $m_2 \neq m_2^{'}$

We assume the peak-to-peak values of the inductor current are $\Delta I_1, \Delta I_2$ as shown in Fig.3-16. The relations of ΔI and the slope of inductor current are as:

$$\Delta I_1 = \frac{m_1 m_2}{m_2 - m_1} T^{'} + \frac{-m_1 m_2}{m_2 + m_1} \delta \tag{3.33}$$

$$\Delta I_2 = \frac{m_1 m_2}{m_2 - m_1} T^{'} + \frac{m_1 m_2}{m_2 + m_1} \delta \tag{3.34}$$

From (3.22) and Fig.3-16, we can know

$$\Delta I \propto T \ , \ D''T'' = \frac{\Delta I}{m_1} \tag{3.35}$$

Therefore the expressions can present as:

$$D_1''T_1'' = \frac{m_2}{m_2 - m_1}T' + \frac{-m_2}{m_2 + m_1}\delta \tag{3.36}$$

$$D_2''T_2'' = \frac{m_2}{m_2 - m_1}T' + \frac{m_2}{m_2 + m_1}\delta \tag{3.37}$$

From (3.20), (3.36), and (3.37) the average duty ratio is as:

$$D_{ave\_period-4} = \frac{D_1''T_1'' + D_2''T_2''}{T_1'' + T_2''} = \frac{D_1''T_1'' + D_2''T_2''}{2T'} = \frac{m_2}{m_2 - m_1} = D \tag{3.38}$$

3.5.6 Analysis of Chaos

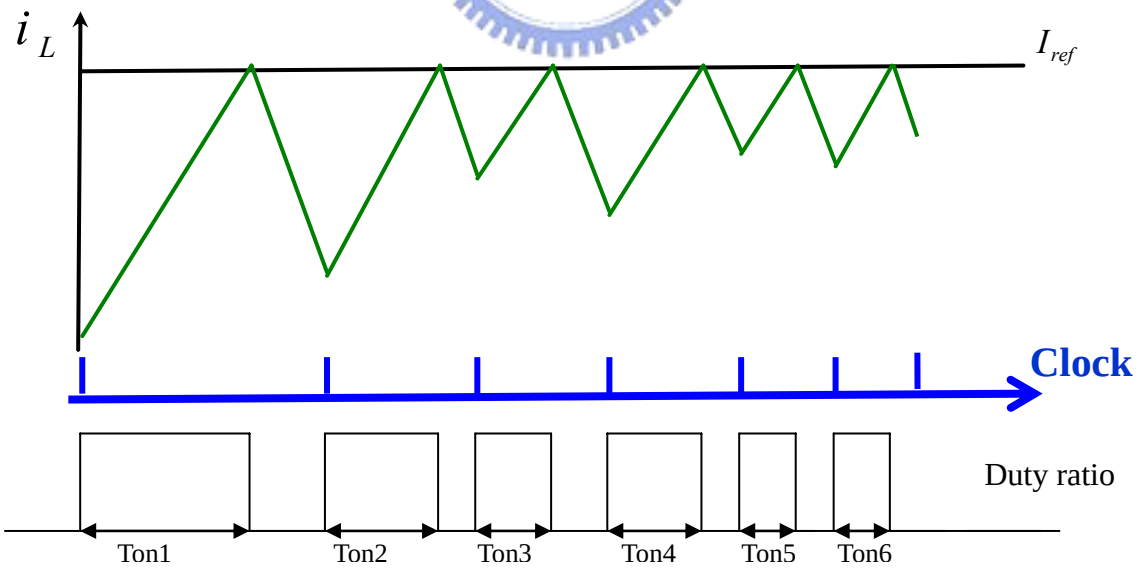


Fig.3-17 The inductor current (clock frequency is increasing)

It is complex to analyze the duty ratio in the chaos state. However, we can divide two parts to observe the behavior in the chaos state. When the frequency of clock signal is

constant, the duration that the switch is on is constant in steady state. However, when the frequency of clock signal is increasing, that is $T_{on2} < T_{on1}$, it results that duration that the switch is on is longer the duration that the switch is off. Fig.3-17 shows that the behavior of the circuit is controlled by T_{on}. In conclusion, the output voltage will be lower when the inductor current is increasing.

On the other hand, the duration that the switch is off is longer when the frequency of clock signal is decreasing. Fig.3-18 presents that the behavior of the circuit is controlled by T_{off} and the behavior of the circuit is controlled by T_{off}.

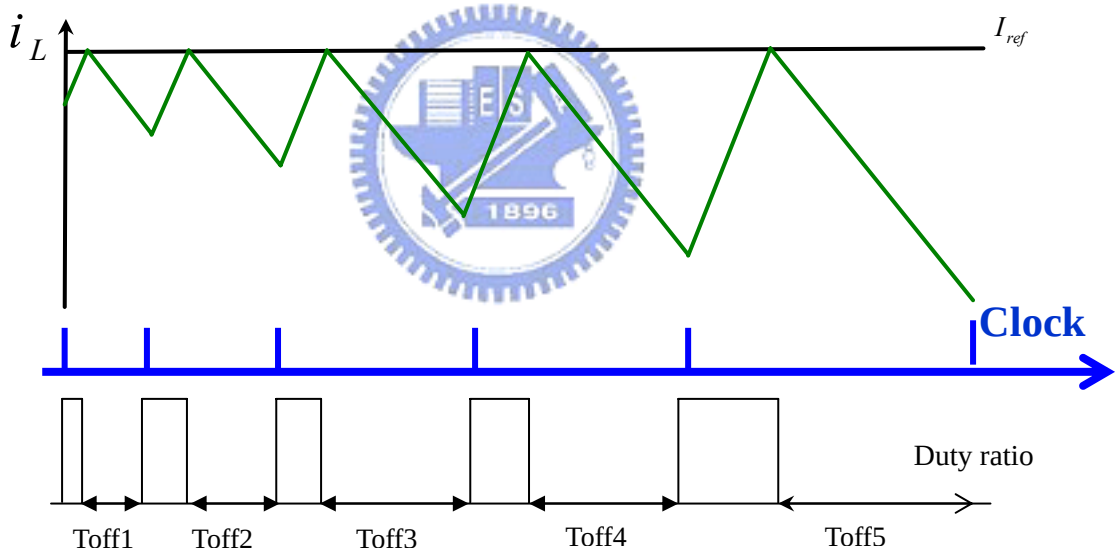


Fig.3-18 The inductor current (clock frequency is decreasing)

From analysis of the above, some conclusions can be known.

1. The gain of the current modulator circuit is constant:

Because the operating frequency of system is changed by chaos clock signals in feedback control, the performance of system seems be affected. Practically, the slopes of charge and discharge of an inductor are constant in steady state. Therefore there is no influence for the

gain of the current modulator circuit by changing the clock frequency.

2. The average output voltage is not affected:

In steady observation, the stability of a converter is decided by duty ratio. From the analysis of quasi-period, we know the average output voltage is the same in despite of period-1, period-2, period-4 or chaos states. In transient observation, because the frequency of clock signal under chaos state is broadband and well mixed, therefore frequency of clock frequency is longer or shorter at different time and it affects the duration of charge or discharge of an inductor and then the output voltage ripple is affected. In chaos analysis of the above, the average value of the voltage ripple is zero. So the average output voltage is not affected.

Chapter 4
Simulation Result and Analysis

To prove accuracy for the analysis of the Chpater3, we employ the PSIM and Matlab numerical tools to accomplish the circuit simulation.

4.1The Circuit Frame of a Current-Controlled Boost Converter

We must build a boost converter in period-1 state to be compared a boost converter under chaos state. Therefore, the parameters must be set by the specifications of (3.10). To make the system operate in CCM, we can know the relation by (2.10):

$$L > \frac{T_s V_o}{2 I_{oB}} D(1-D)^2$$

$$\Rightarrow L > \frac{1/100k * 40}{2 * 3.5} 0.5(1-0.5)^2 = 7.1uH \tag{4.1}$$

,where $$I_{oB} = \frac{140}{40} = 3.5A \tag{4.2}$$

Table 4-2 The specifications of the boost converter

E	$L1$	$C1$	R	C_c	R_f	V_{ref}	V_o	R_a	R_b
$28V$	$195uH$	$2mF$	11.2Ω	$0.23uF$	$72.2k\Omega$	$2V$	$40V$	$40.05k\Omega$	$2.5k\Omega$

The circuit frame of boost converter by PSIM is shown in Fig.4-1. We set a specification that input $E = 28V$ raises to output $V_o = 40V$. Other parameters are shown in Table 4-1.

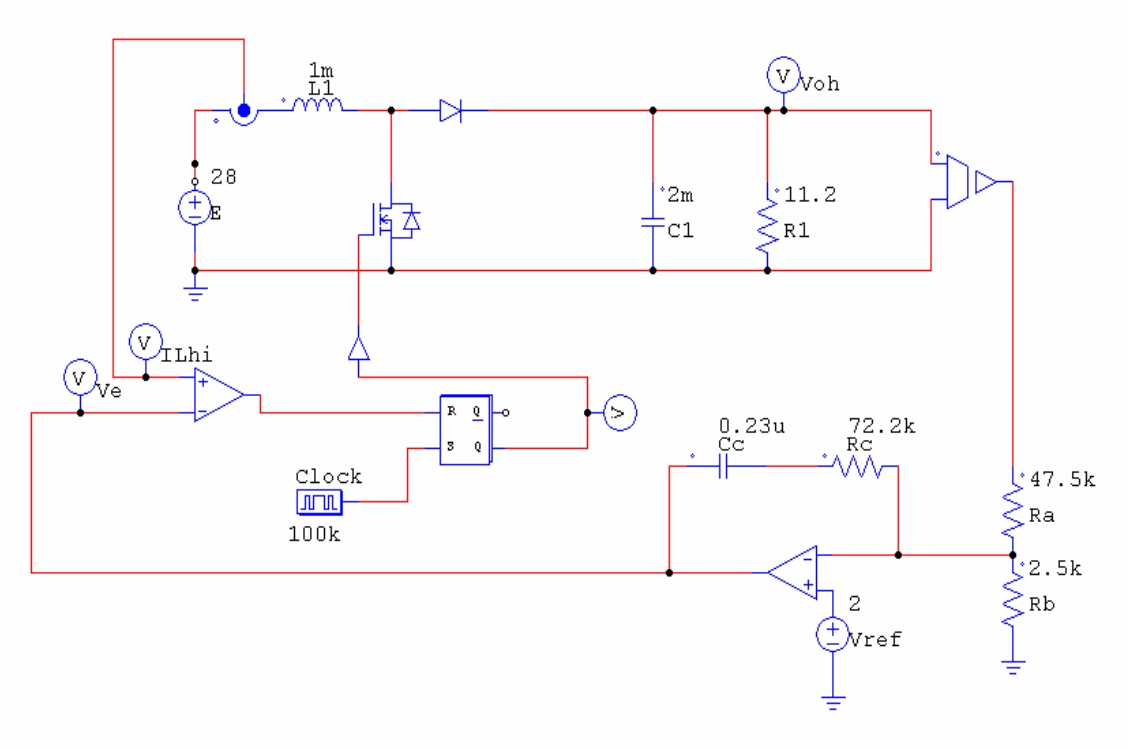


Fig.4-1 Circuit diagram of the current-controlled boost converter

Because we must promise that the boost converter works under the stable period-1 state, we add a compensator in the feedback loop to the system be stable. Fig.4-2 presents the circuit of the compensator. The circuit consists of an Op amplifier, resisters, and a capacitor. One point is worth making about Fig.4-2. A circuit of divided voltage is built to protect Op amplifier from high voltage. Therefore, V_{ref} is not equal to V_o and the relation of V_{ref} and V_o is yielded:

$$V_{ref} = \frac{R_b}{R_a + R_b} V_o \tag{3.12}$$

Because our goal mainly focus on chaos behavior, the compensator of the boost converter considered is described in [28].

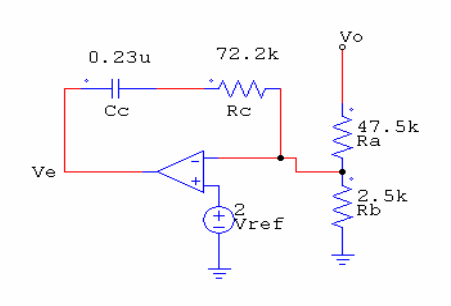
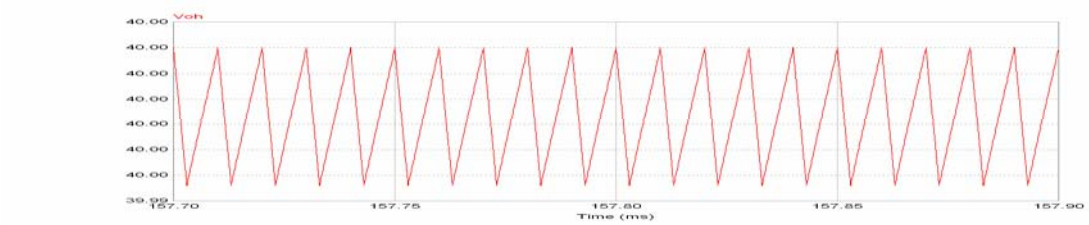
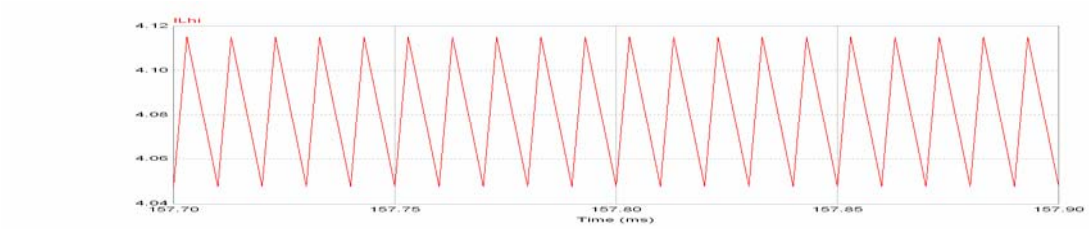


Fig.4-2 The compensator

The simulation of the close loop circuit is generated by PSIM simulation tool. The result is shown in Fig.4-3. Fig.4-3 presents that the system keeps in stable period-1 state and the inductor current is in continuous condition mode.



(a) Simulation of the output voltage



(b) Simulation of the inductor current

Fig.4-3 Simulation of the boost converter by PSIM

Secondly, we employ the PSIM and Matlab numerical tools to accomplish the circuit simulation with new model. Fig.4-4 is the simulation circuit by PSIM. There are four parts

including a boost converter, a compensator, a driving circuit, and a chaos generator. The specification presents in Table 3-1 and Table 4-1.

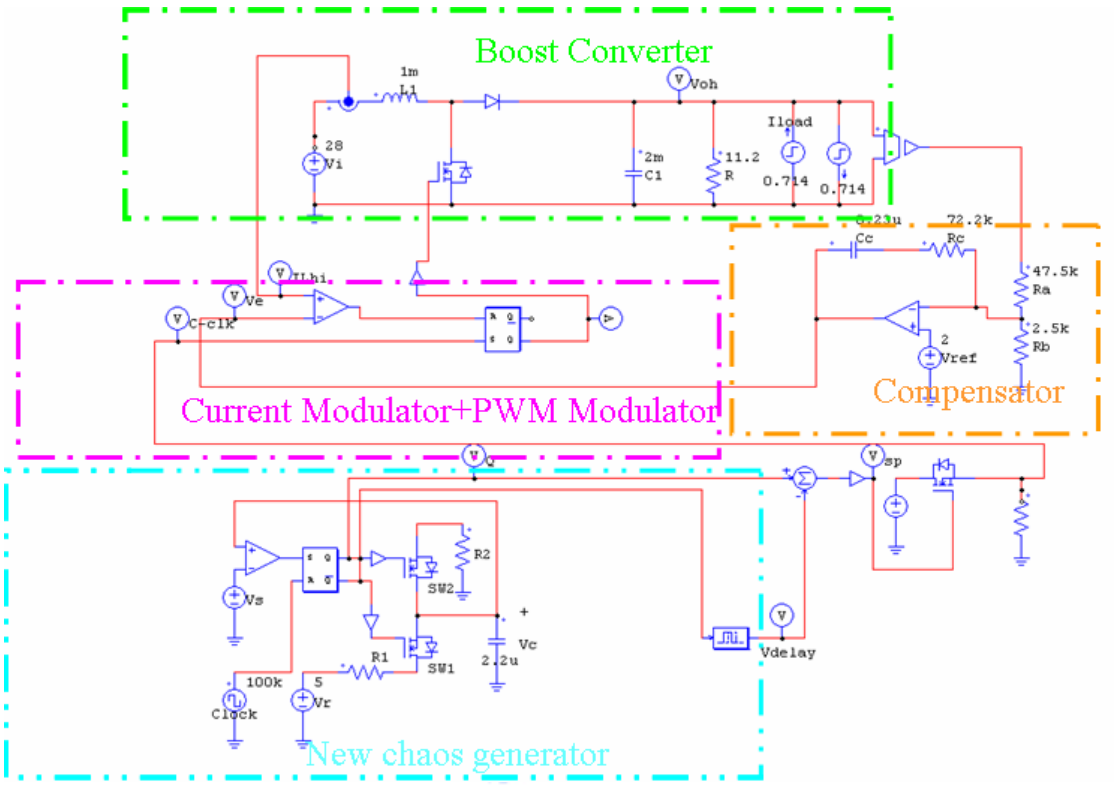


Fig.4-4 The circuit frame of a boost converter with chaos generator

4.2 Simulation of Stability

When the input voltage of chaos generator, V_s, is adjusted to be quasi-period state, the simulations present in following simulation diagrams. From Fig.4-5 to Fig.4-8, every average duty ratio and average output voltage are as:

1. When $V_s = 15V$, the system is in period-1 state

$$D_{ave\_period-1} = \frac{3*10^{-6}}{10^{-5}} = 0.3 \qquad \text{and} \qquad \tilde{v}_o = 40\text{V}$$

2. When $V_s = 12.5V$, the system is in period-2 state

$$D_{ave\_period-2} = \frac{6*10^{-6}}{2*10^{-5}} = 0.3 \qquad \text{and} \qquad \tilde{v}_o = 40\text{V}$$

3. When $V_s = 11.8V$, the system is in period-4 state

$$D_{ave\_period-4} = \frac{5*10^{-6} + 7*10^{-6}}{4*10^{-5}} = 0.3 \quad \text{and} \quad \tilde{v}_o = 40\text{V}$$

4. When $V_s = 10V$, the system is under chaos state

$$D_{ave\_chaos} = \frac{4*10^{-6} + 10^{-5} + 5*10^{-6} + 9*10^{-6} + 10^{-6} + 3*10^{-6} + 5*10^{-6} + 9*10^{-6} ..... + 7*10^{-6}}{2.9*10^{-4}}$$

$$= 0.304.. \approx 0.3$$

and $\tilde{v}_o = 40\text{V}$

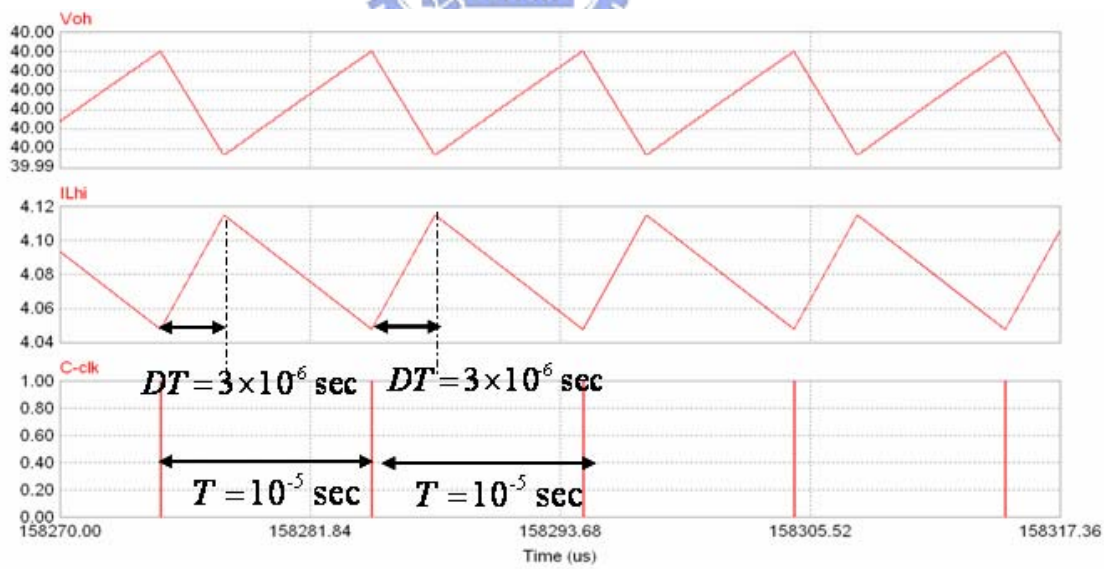


Fig.4-5 Simulation in Period-1(Vs=15V)

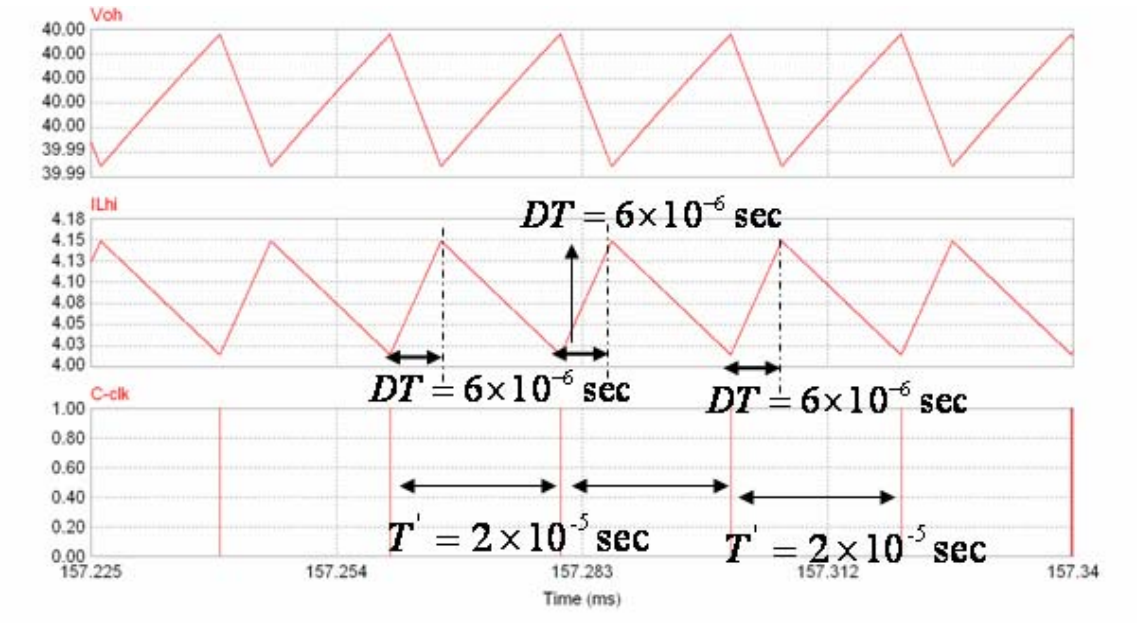


Fig.4-6 Simulation in Period-2(Vs=12.5V)

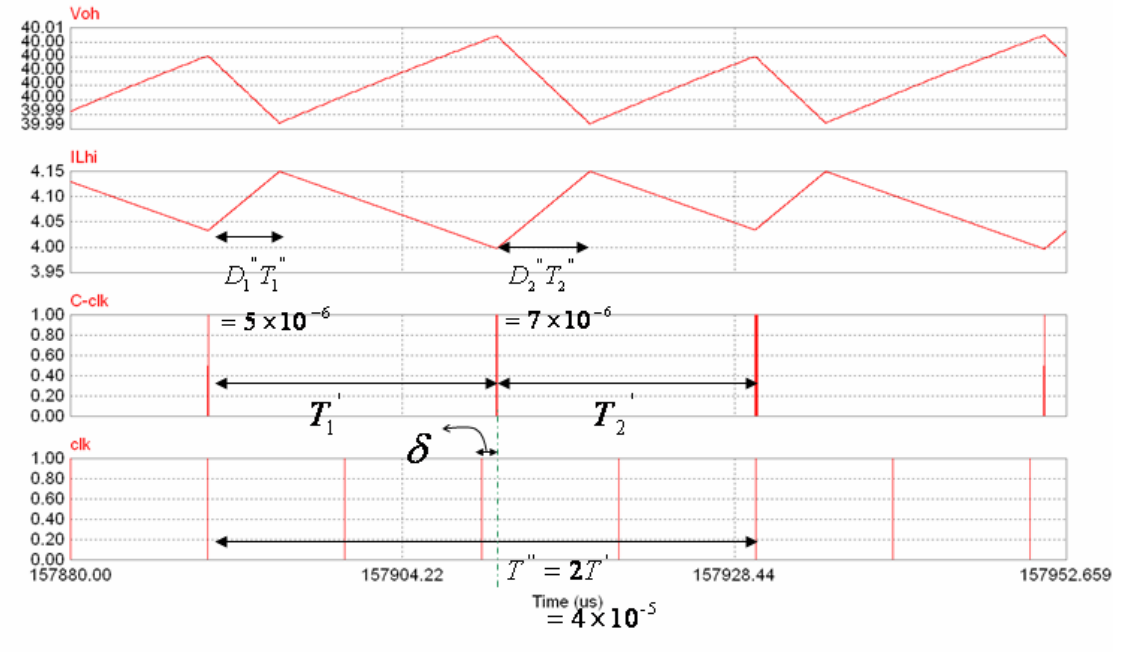


Fig.4-7 Simulation in Period-4(Vs=11.8V)

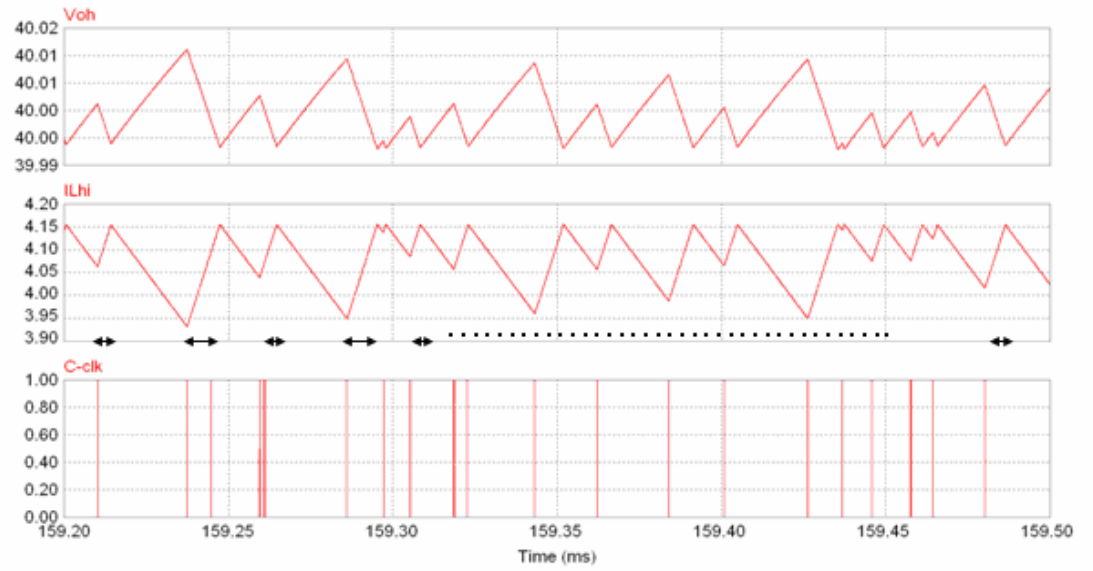


Fig.4-8 Simulation in Chaos(Vs=10V)

In addition, from Fig.4-9, because the frequency is broadband and the time of charge and discharge for the inductor current, therefore the output voltage ripple vibrates slightly. However, the average output voltage is be 40V stably.

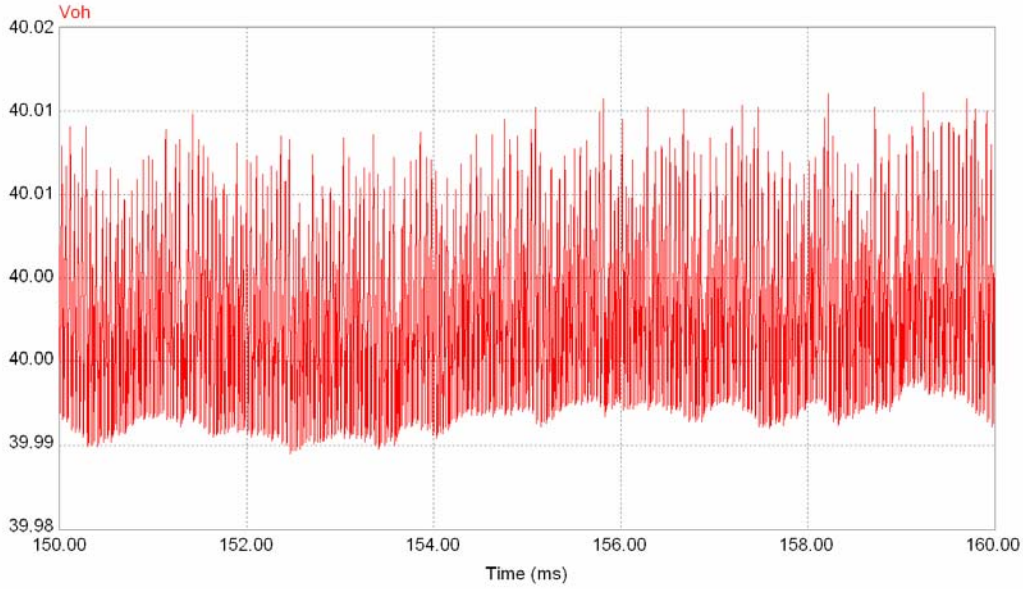


Fig.4-9 Simulation in Chaos during 10ms (Vs=10V)

4.3 Response of Output Voltage to loading current

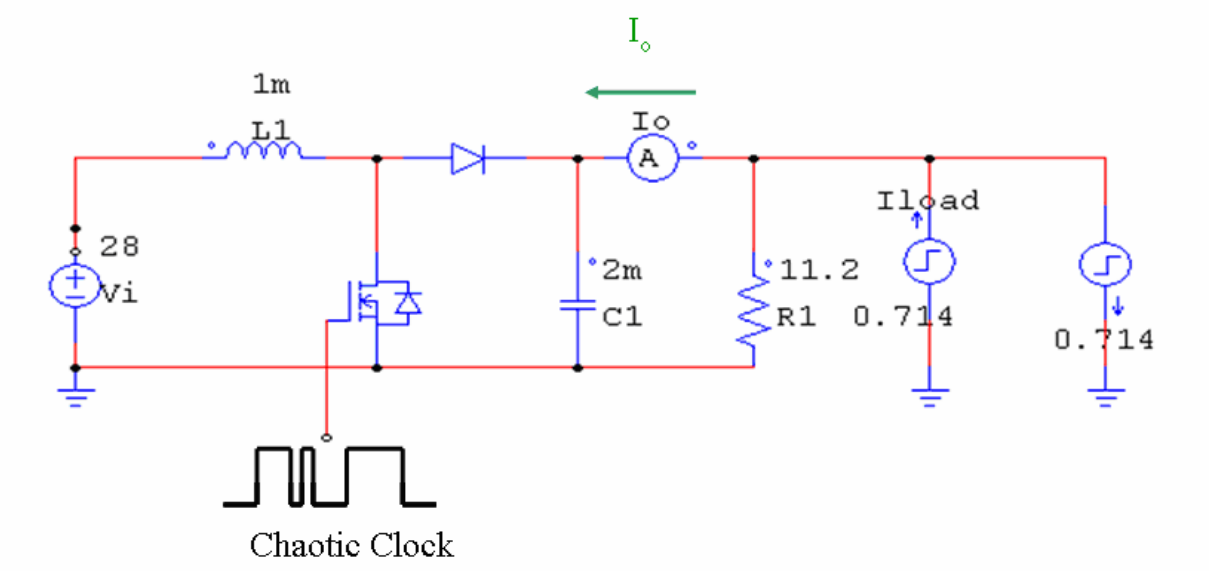


Fig.4-10 The circuit for testing varying loading

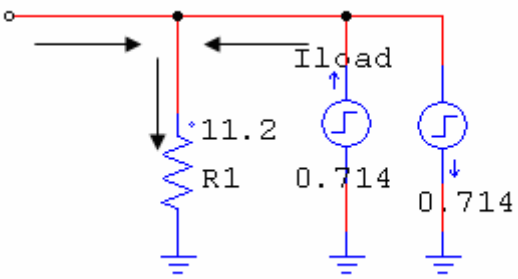


Fig.4-11 The testing circuit of testing varying loading

When loading is varying, the stability may change. We add and pump the loading circuit to test the stability of the boost converter with chaos generator. The simulation circuit is shown in Fig.4-10. The testing circuit is shown in Fig.4-11. We add a loading current of original 20% loading current and then pump it from the converter. From Table 4-1, the original current is yielded:

$$I_o = \frac{V_o}{R_1} = \frac{40}{11.2} = 3.57A$$

The simulation result is shown in Fig.4-12. We can observe that the output voltage still retain to be 40V in the steady state even through loading is varying.

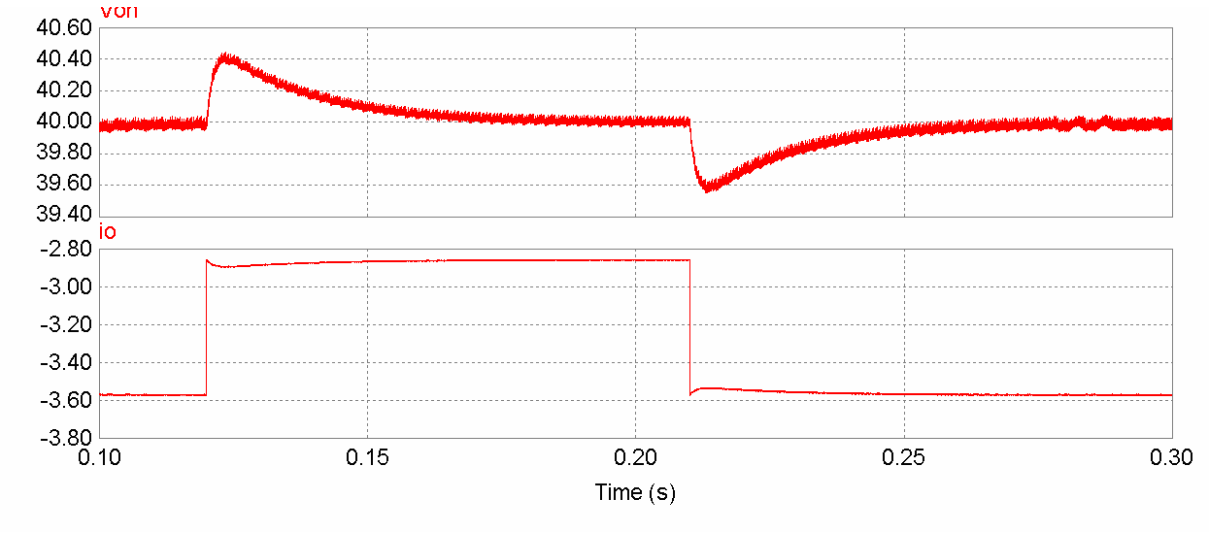


Fig.4-12 Simulation of load current change

4.4 Clock Times of Frequency for the clock signal

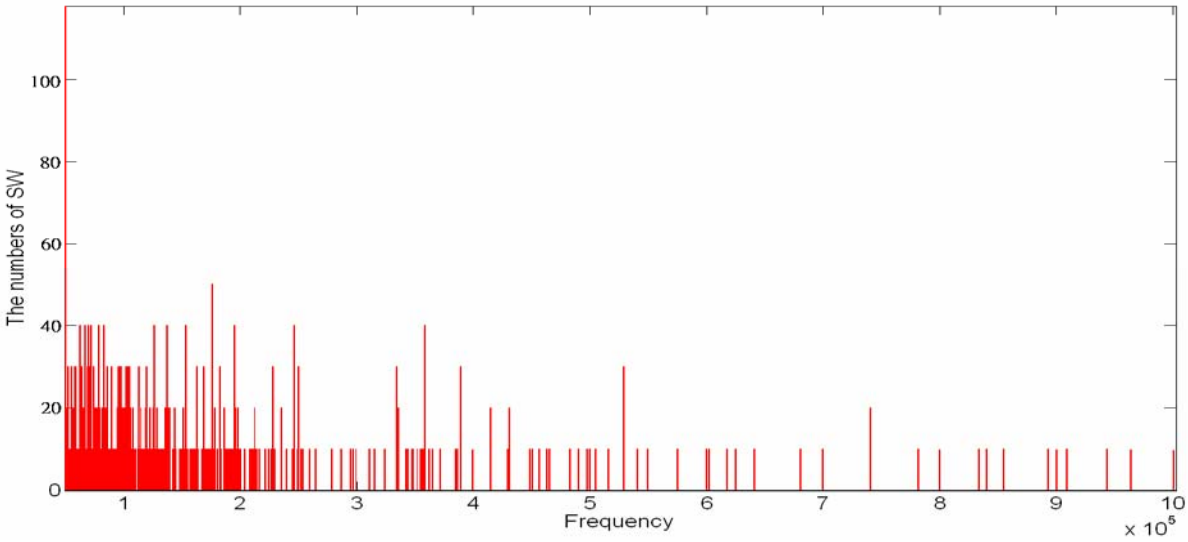


Fig.4-13 The statistical chart of the clock times of frequency for the clock signal

We analyze the clock times of frequencies for the clock signal. The clock times of

different frequencies of chaotic signal by chaos generator for some duration is shown in Fig.4-13. The total times of frequencies are 13400 times. We can observe that the clock times of frequencies for the clock signal are dispersed. In addition, because the characteristic of chaos, the clock times of low frequencies are more and cause the power in low frequency is higher.

4.5 Simulation of PSD

Secondly, we get data of simulation in PSM and calculate PSD by Matlab tool. The following are the simulation diagrams of PSD in quasi-period. The power in quasi-period states calculated by Matlab is shown in Table 4-5. Therefore, in spite of the different operating states, every power is still the same. Compare the period-1 state with different operating state form Fig.4-14 to Fig.4-18, the results present the degree of reduction and are shown in Table 4-2, Table 4-3, and Table 4-4. Table 4-5 shows the power in different states is the same. In Fig.4-14, we can observe that there is obviously discrete spectrum in period-1 state and peak values of harmonics in period-2 state have reduced. Fig.4-15 and Fig.4-16 show the spectrum in period-4 state. There is the continue spectrum under chaos in Fig.4-17. Fig.4-18 shows the obvious difference with period-1 and chaos state. Because power is constant and chaos is broadband, the peak values in harmonics originally are reduced. Therefore, the chaos can improve the question of EMI.

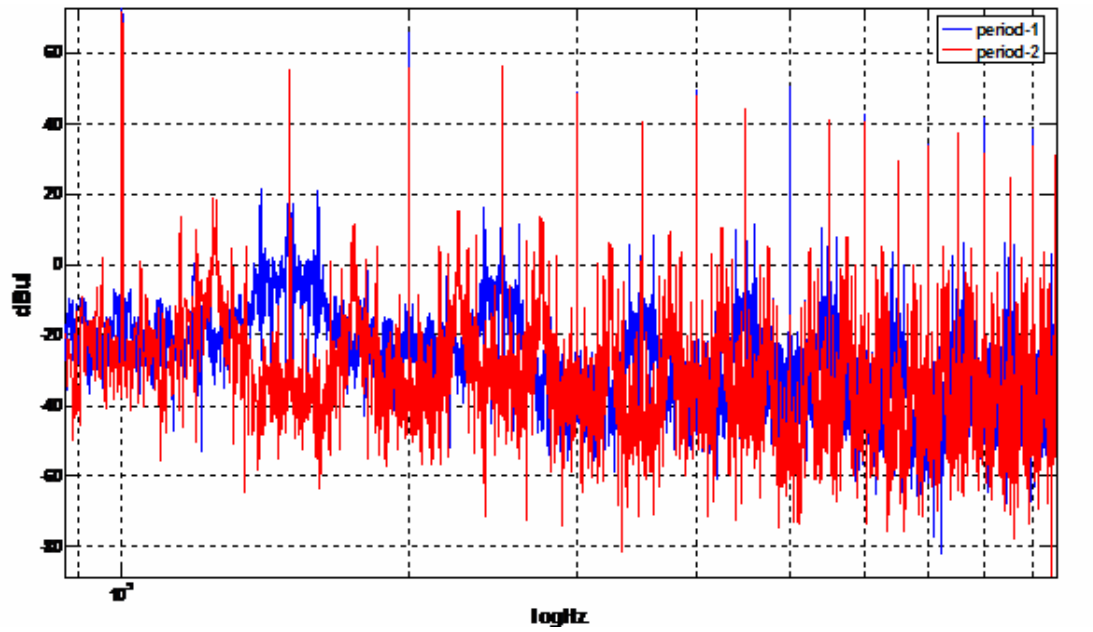


Fig.4-14 Simulation of PSD (Period-1 and Period-2)

Table 4-2 Degree of reduction(Period-1 & Period-2)

f_s	Perios-1 (dBul)	Period-2 (dBul)	Reduction (dBul)
1	76.33384	71.71917	4.614664
2	65.69836	55.49231	10.20604
3	48.59668	48.45855	0.438125
4	49.47079	47.62989	1.840904
5	50.21335	44.3838	5.82955
6	42.43602	40.58597	1.850049
7	34.14725	33.70555	0.441701
8	41.60542	35.41556	6.18986
9	38.15995	33.52151	4.638447

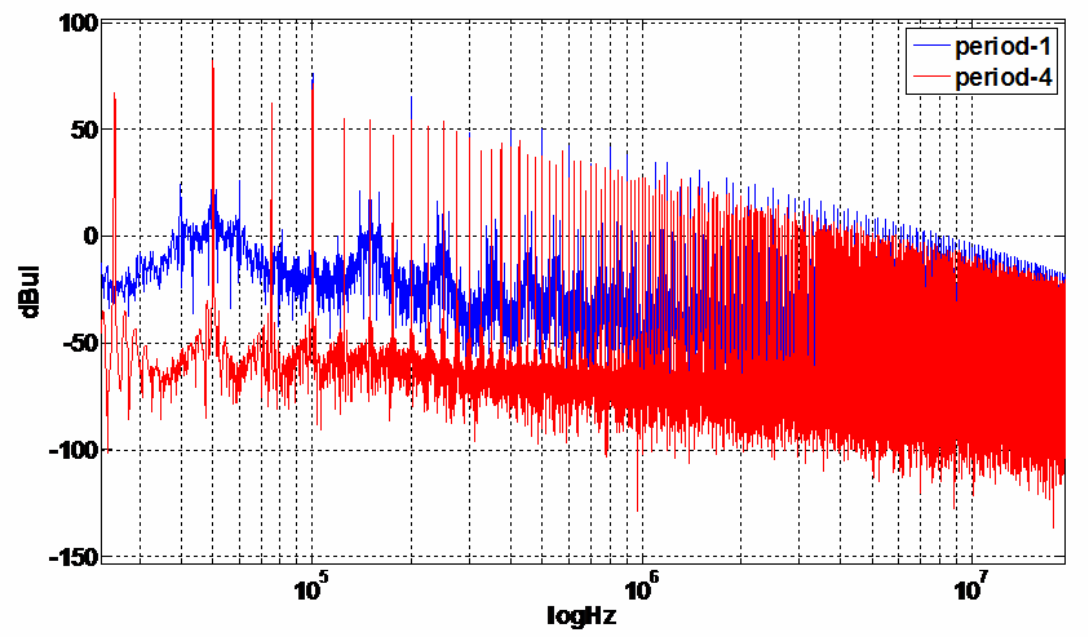


Fig.4-15 Simulation of PSD (Period-1 and Period-4)

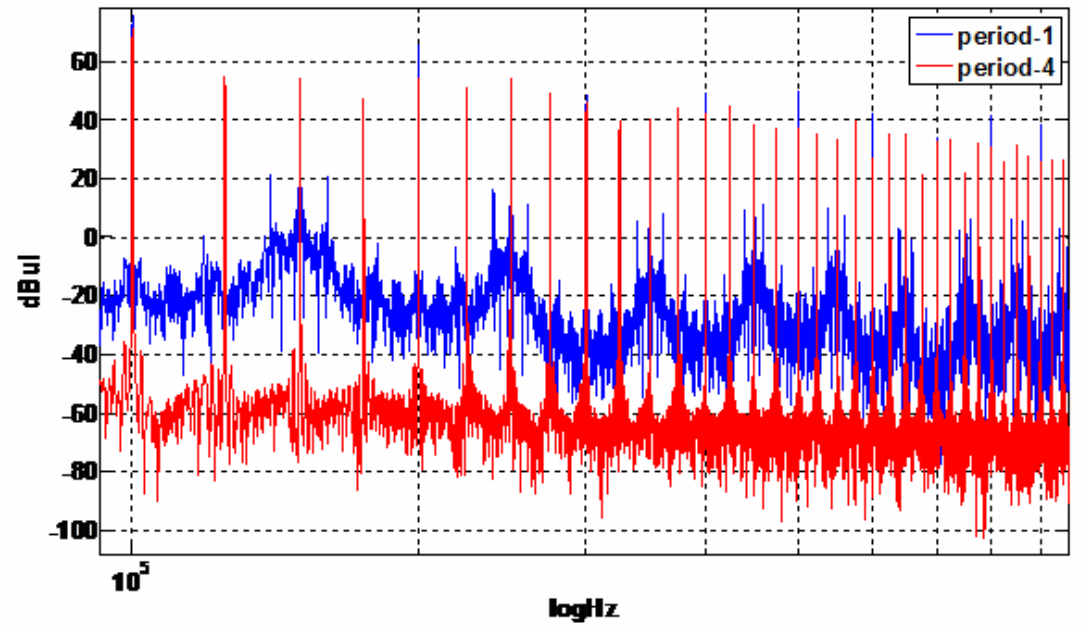


Fig.4-16 Amplification of simulation of PSD (Period-1 and Period-4)

Table 4-3 Degree of reduction(Period-1 & Period-4)

f_s	Perios-1 (dBul)	Period-4 (dBul)	Reduction (dBul)
1	76.33384	71.41194	04.92189
2	65.69836	54.33205	11.36630
3	48.89668	46.1163	02.78038
4	49.47079	42.04028	07.43051
5	50.21335	40.65071	09.56264
6	43.43602	27.06299	15.40903
7	34.14725	33.02843	01.11882
8	41.60542	35.27654	06.32888
9	38.15995	30.63433	07.52562

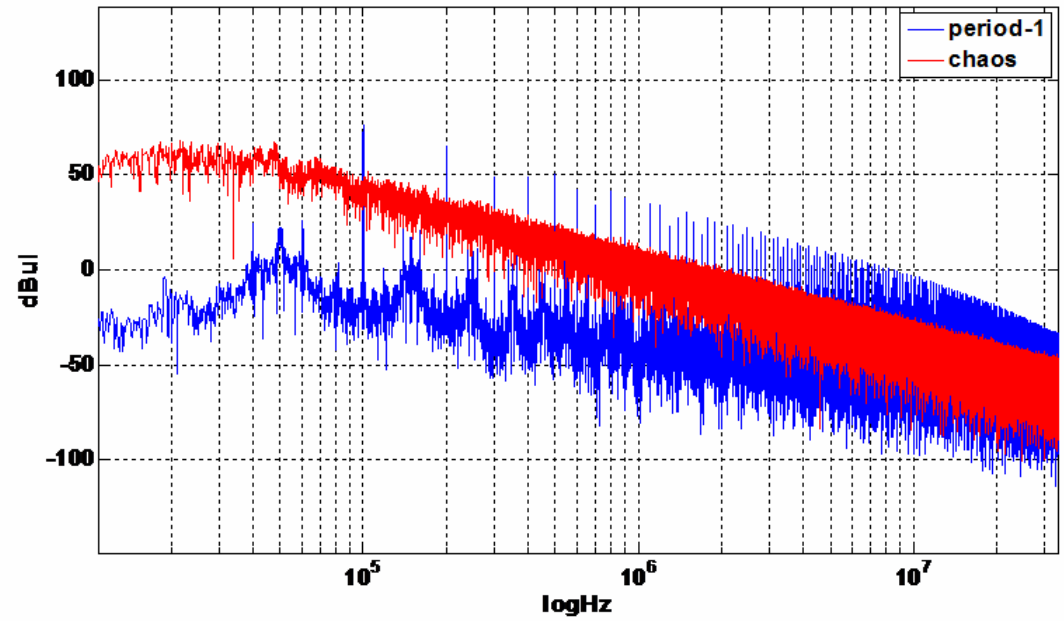


Fig.4-17 Simulation of PSD (Period-1 and chaos)

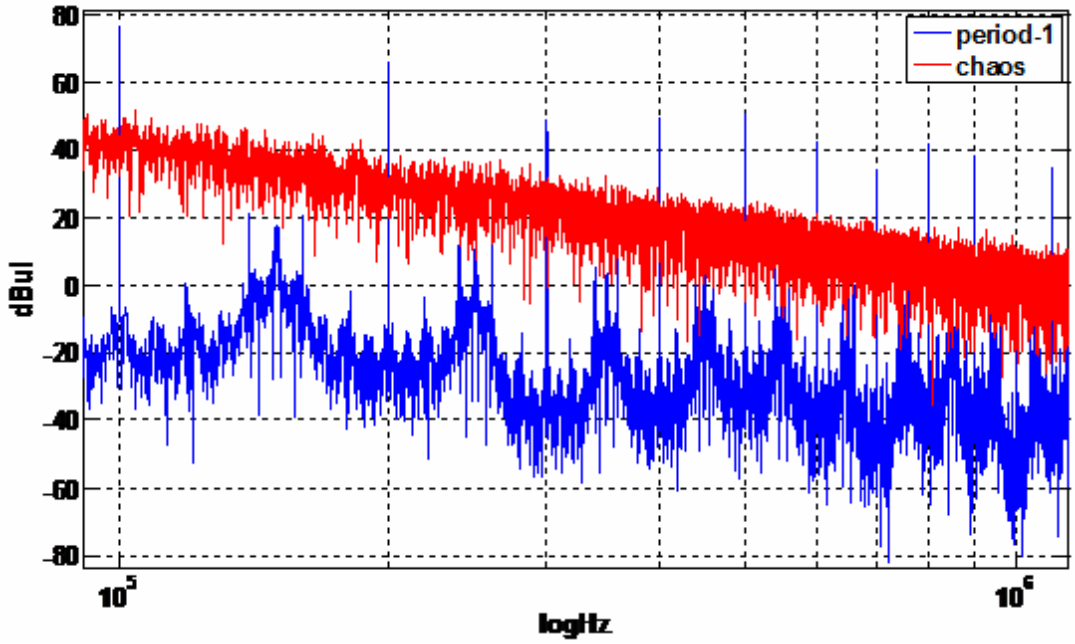


Fig.4-18 Amplification of simulation of PSD (Period-1 and chaos)

Table 4-4 Degree of reduction(Period-1 & Chaos)

f_s	Perios-1 (dBul)	Chaos (dBul)	Reduction (dBul)
1	76.33384	42.2693018	33.06453
2	65.69836	35.7387797	29.95958
3	48.89668	30.656851	18.23982
4	49.47079	25.5436384	23.92715
5	50.21335	26.1424526	24.07089
6	43.43602	20.6228786	21.81314
7	34.14725	14.5116641	19.63558
8	41.60542	16.6259601	24.97945
9	38.15995	13.8021154	24.35783

Table 4-5 The power in different operating states

State	Power(I^2)
Period-1	16.6593W
Period-2	16.6594W
Period-4	16.6593W
Chaos	16.6594W

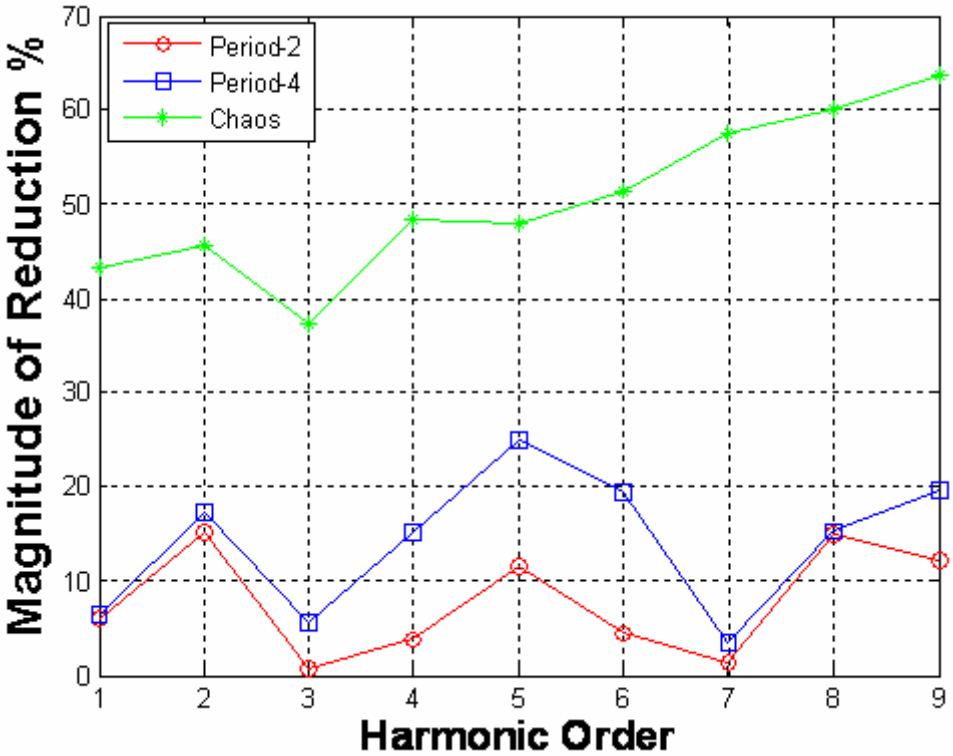


Fig.4-19 The relation of Reduction percent and harmonics

Fig.4-19 presents the relation of reduction percent and harmonics. In period doubling

state, the peak values of operating and harmonics frequencies in the spectrum can be reduced. It must be noted that the operating frequency is reduced to 43% under chaos state and other harmonics are reduced to 35% at least. Therefore, chaos generator has well effects for suppressing EMI of harmonics.

Chapter 5
Conclusion

In this thesis, we mainly employ a new chaos generator to suppress EMI of DC-DC converters. Unlike other chaos technique, our scheme can maintain the performance of DC-DC converters while significantly reduce their EMI. Moreover, the chaos-modulated clock by the new chaos generator can be realized by a simple analog circuit without any inductor. Therefore, it is possible to have inexpensive implementation in CMOS.

This study have given a comparative investigation into the effects of the randomness level on the PSD of a chaos modulation scheme that are applied to classical DC-DC converters operating in CCM. The result has been demonstrated that controlling the degree of chaos can gradually spread the discrete frequency over the frequency spectrum, and harmonic power can be reduced up to 35%. Moreover, according to our theoretical analysis and numerical simulation, the average output voltage is not affected in the chaos state. In conclusion, a DC-DC converter operating in chaos state can effectively suppresses peak values of EMI in a converter, and can conform to several EMI norms.

Reference List

[1] E. Ott, C. Grebogi, and J. A. Yorke, "Controlling chaos," *Physical Review Letters*, vol. 64, pp. 1196-1199, 1990.

[2] E. R. Hunt, "Stabilizing high-period orbits in a chaotic system: The diode resonator," *Physical Review Letters*, vol. 67, pp. 1953-1955, 1991.

[3] V. Petrov, B. Peng, and K. Showalter, "A map-based algorithm for controlling low-dimensional chaos," *The Journal of Chemical Physics*, vol. 96, p. 7506, 1992.

[4] K. Pyragas, "Continuous control of chaos by self-controlling feedback," *Physics Letters A*, vol. 170, pp. 421-428, 1992.

[5] C. Batlle, E. Fossas, and G. Olivar, "Time-delay stabilization of the buck converter," in *Control of Oscillations and Chaos, 1997. Proceedings., 1997 1st International Conference*, 1997, pp. 590-593 vol.3.

[6] Z. Qian, X. Wu, Z. Lu, and M. H. A. P. M. H. Pong, "Status of electromagnetic compatibility research in power electronics," in *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*, 2000, pp. 46-57 vol.1.

[7] Z. Dongbing, D. Y. Chen, and F. C. Lee, "An experimental comparison of conducted EMI emissions between a zero-voltage transition circuit and a hard switching circuit," in *Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE*, 1996, pp. 1992-1997 vol.2.

[8] Z. Jun and W. Xue-Ye, "Study of bifurcation in current-controlling DC/DC converters," in *Machine Learning and Cybernetics, 2002. Proceedings. 2002 International Conference on*, 2002, pp. 2005-2009 vol.4.

[9] D. C. Hamill, J. H. B. Deane, and P. J. Aston, "Some applications of chaos in power converters," in *Update on New Power Electronic Techniques (Digest No: 1997/091), IEE Colloquium on*, 1997, pp. 5/1-5/5.

[10] S. Banerjee, D. Kastha, and S. SenGupta, "Minimising EMI problems with chaos," in *Electromagnetic Interference and Compatibility, 2001/02. Proceedings of the International Conference on*, 2002, pp. 162-167.

[11] J. H. B. Deane and D. C. Hamill, "Improvement of power supply EMC by chaos," *Electronics Letters*, vol. 32, p. 1045, 1996.

[12] R. S. Bueno and J. L. R. Marrero, "Control of DC-DC converters in the chaotic regime," in *Control Applications, 1998. Proceedings of the 1998 IEEE International Conference on*, 1998, pp. 832-837 vol.2.

[13] A. L. Baranovski, A. Mogel, W. Schwarz, and O. A. W. O. Woywode, "Chaotic control of a DC-DC-converter," in *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on*, 2000, pp. 108-111 vol.2.

[14] W. C. Y. Chan and C. K. Tse, "Study of bifurcations in current-programmed DC/DC

boost converters: from quasiperiodicity to period-doubling," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on],* vol. 44, pp. 1129-1142, 1997.

[15] M. Kuisma and P. Silventoinen, "Analyzing Current Ripple in Variable-Frequency Boost Converter," in *Power Electronics Specialists Conference, 2007. PESC 2007. IEEE,* 2007, pp. 1535-1540.

[16] S. Callegari, R. Rovatti, and G. Setti, "Chaos-based FM signals: application and implementation issues," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on],* vol. 50, pp. 1141-1147, 2003.

[17] G. Setti, R. Rovatti, S. Callegari, and M. Balestra, "Control of Chaos Statistics for the Generation of Timing Signals with Improved EMC," *Chaos and Bifurcation Control: Theory and Applications—Part I: Chaos Control*.

[18] S. Callegari, R. Rovatti, and G. Setti, "Chaos Based Improvement of EMI Compliance in Switching Loudspeaker Drivers," *European Conference on Circuit Theory and Design,* 2001.

[19] M. Balestra, A. Bellini, S. Callegari, R. Rovatti, and G. Setti, "Chaos-Based Generation of PWM-Like Signals for Low-EMI Induction Motor Drives: Analysis and Experimental Results," *IEICE TRANSACTIONS on Electronics,* vol. 87, pp. 66-75, 2004.

[20] K. K. Tse, R. W. M. Ng, H. S. H. Chung, and S. Y. R. A. H. S. Y. R. Hui, "An evaluation of the spectral characteristics of switching converters with chaotic carrier-frequency modulation," *Industrial Electronics, IEEE Transactions on,* vol. 50, pp. 171-182, 2003.

[21] T. Kousaka, T. Ueta, Y. Ma, and H. Kawakami, "Bifurcation analysis of a piecewise smooth system with non-linear characteristics," *International Journal of Circuit Theory and Applications,* vol. 33, pp. 263-279, 2005.

[22] O. G. Saracoglu and R. Kilic, "A simulation study on EMI effects in autonomous Chua's chaotic circuit," in *Electromagnetic Compatibility, 2003. EMC '03. 2003 IEEE International Symposium on,* 2003, pp. 280-283 Vol.1.

[23] C. Wei, K. T. Chau, W. Zheng, and J. Z. Jiang, "Application of chaotic modulation to ac motors for harmonic suppression," in *Industrial Technology, 2006. ICIT 2006. IEEE International Conference on,* 2006, pp. 2343-2347.

[24] M. di Bernardo and F. Vasca, "Discrete-time maps for the analysis of bifurcations and chaos in DC/DC converters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on],* vol. 47, pp. 130-143, 2000.

[25] D. C. Hamill, J. H. B. Deane, and D. J. Jefferies, "Modeling of chaotic DC-DC converters by iterated nonlinear mappings," *Power Electronics, IEEE Transactions on,* vol. 7, pp. 25-36, 1992.

[26] M. di Bernardo, F. Garefalo, L. Glielmo, and F. Vasca, "Switchings, bifurcations, and

chaos in DC/DC converters," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on],* vol. 45, pp. 133-141, 1998.

[27] T. Kousaka, T. Kido, T. Ueta, H. Kawakami, and M. Abe, "Analysis of border-collision bifurcation in a simple circuit," *Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on,* vol. 2, 2000.

[28] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*: Kluwer Academic Publishers, 2001.

[29] R. D. Middlebrook, "Modeling current-programmed buck and boost regulators," *Power Electronics, IEEE Transactions on,* vol. 4, pp. 36-52, 1989.