國立交通大學

電機與控制工程學系

碩士論文

具高效能斜率補償器及與輸入電源無關之負載電流識別機制的電流模式直流/直流降壓電源轉換器

High-Efficiency Slope Compensator (HSC) with Input-Independent Load Condition Identification in Current Mode DC-DC Buck Converters

研究生：賴 韋 任

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中 華 民 國 九 十 七 年 十 月

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碩士論文

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摘　　要

在消費性電子產品中，尤以手持式產品的應用上，需求越來越廣泛。擁有高效能與小型化的電源轉換器日趨重要。為了有效使用有限的電池能量，電源管理系統為非常重要的元件。故本文提出一個切換式穩壓器在斜率補償上的應用單元，以期在模式切換時有最好的效能表現。

論文中，降壓式轉換器適當的操作於脈波寬度調變模式(PWM)以及脈波頻率調變模式(PFM)，分別應用於重電流負載及輕電流負載。然而在電流控制模式下，當工作周期大於二分之一的全周期時，會發生所謂的次諧波震盪導致系統不穩定。所以在傳統控制中，加入補償斜率來克服次諧波震盪。然而此一傳統斜率補償電路會造成誤差放大器的輸出電壓(V_C)隨供應電源(V_{IN})而改變，產生控制上的困擾。

利用本文所提出的高效能斜率補償器(HSC)，可達到誤差放大器的輸出電壓(V_C)與供應電源(V_{IN})互為獨利因子，僅與負載電流成正相關。此外為防止電源轉換器有逆向電流的產生，本文使用零電流偵測器(ZCD)來偵測逆向電流的發生，以提高系統效能表現。所以在傳統控制上，是偵測逆向電流保護電路的輸出訊號來判定切入脈波頻率調變模式的時機。然而傳統零電流偵測器的輸入訊號對抗雜訊能力較差，無法操作於高頻切換電路。所以本文利用已提出的誤差放大器的輸出電壓(V_C)當成切換依據，達到克服雜訊以及負載電流識別機制的功能。

本論文所提出的內容，非以逆向電流保護電路的輸出訊號當作判別依據，是以誤差訊號放大器的輸出端訊號(V_C)來判斷。藉由誤差訊號放大器的輸出電壓(V_C)隨負載電流變化而不隨供應電源改變的特性，來達到高效率的模式轉換。

本論文根據不同負載情況適當地切換這於此兩種模式間，整體系統效率可維持百分之八十以上。本電路架構以世界先進股份有限公司點三五微米製程來實現，其模擬結果與效能值亦包含在文中。

High-Efficiency Slope Compensator (HSC) with Input Independent Load Current Identification in Current Mode DC-DC Buck Converters

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ABSTRACT

Today's portable and battery powered products such as cellular phones, personal digital assistant (PDA), tablet PC, etc are increasingly demanded more and more. The system's operation time is an important issue to enhance the worth of electronic devices. Therefore, the power management systems provide solutions to overcome the above problems.

In switching converters especially in current mode systems, there is a slope compensation circuit to prevent the occurrence of sub-harmonic oscillation that caused the system unstable. Designers proposed a sawtooth ramp adding to the sensed inductor current to eliminate the sub-harmonic oscillation. But conventional sawtooth ramp makes the output voltage of error amplifier (V_C) unpredictable as the supply voltage changes.

A high-efficiency slope compensator (HSC) is presented to achieve power reduction in current-mode control and provide input-independent load condition identification for mode switch in hybrid PWM/PFM system. That is, according to load condition, an adaptive mode transition can be decided by the HSC circuit and not varied by the variation of input voltage. Therefore, for a hybrid PWM/PFM system, the power conversion efficiency can be kept high over a wide load range. Besides, the pulse-ramp generator prevents the current-mode DC-DC converter from having the sub-harmonic oscillation problem and reduces power dissipation of the slope compensator. Simulation results show that the mode transition is accurately decided at the optimum point without being affected by the variation of input voltage. The power conversion efficiency is improved about 5% in PWM/PFM transition region.

The proposed technique is based on current-mode dc-dc buck controller. The circuit implementation is fabricated by VIS 0.35-μm CMOS technology and the overall efficiency is larger than 80% at all load conditions.

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韋任 于 拾月 秋

國立交通大學

中華民國九十七年十月

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Chapter 1

Introduction

1.1 Background of Regulators

Today's portable and battery powered products such as cellular phones, personal digital assistants (PDA), tablet PC, etc are increasingly demanded more and more. System's operation time is a factor to enhance the worth of the electronic devices in consumer's market. The longer operation time had higher attraction and the best competitiveness but it had many limitations and difficulties to increase the capacity of stored energy device liked as battery equipments. As a result, how to extend the system operation time is a critical issue that engineers mostly concerned. Moreover, for specific electronic system, there are different supply voltages to make required performance liked VRM techniques. Therefore, power management system provides solutions to overcome the above confusions.

Power management ICs with high conversion efficiency are used to these applications for maximizing the operation time of the portable devices. Furthermore, it is essential for the designers to decrease the size and weight of the power module for the products. In order to accomplish low-cost, high-efficiency and high performance, there are many different kinds of power management architectures could be used. Those power management systems, such as boost converter, buck converter, charge pump, and low drop-out (LDO) linear regulator, operates with step-down, step-up or inverting voltage. For example, the block diagram of personal digital assistant system is shown in Fig. 1. The core system includes processor/memory, user interface and power management ICs.

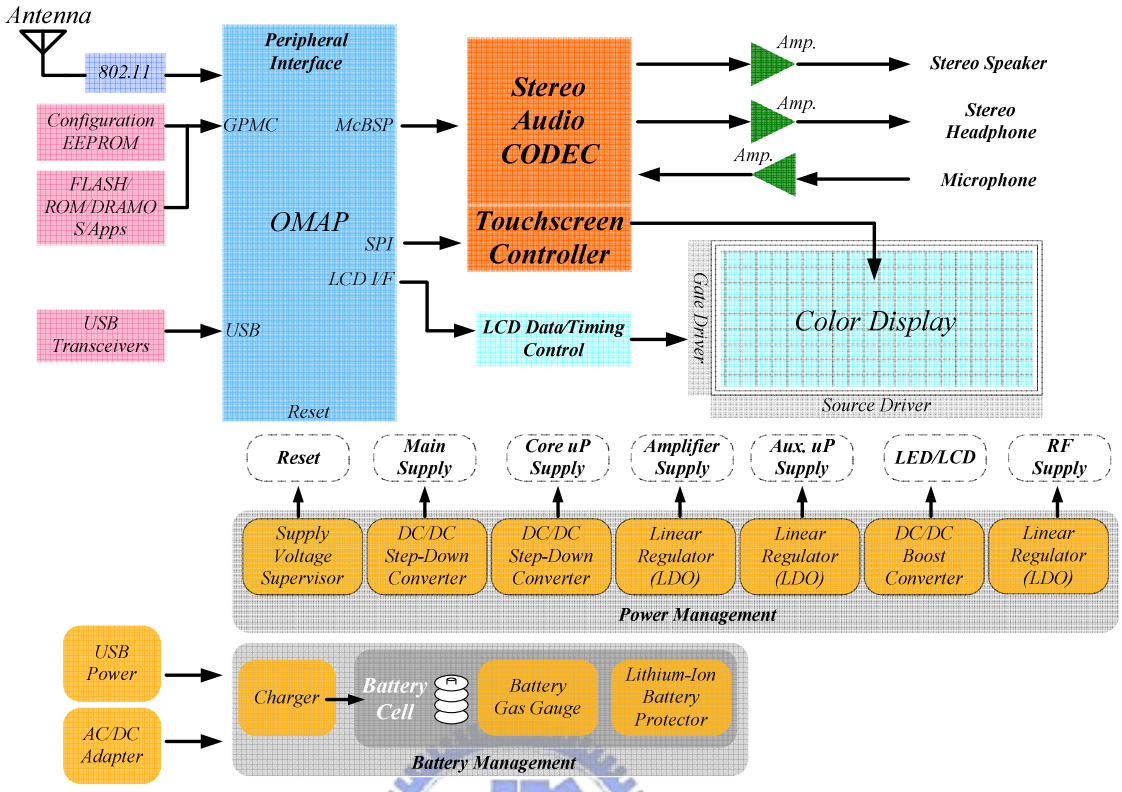


Fig. 1. The block diagrams of personal digital assistant (PDA) with power management ICs

1.2 Classification of Power Supply Circuit

Power management circuits can classify into three different techniques as function works: linear regulators, switching capacitor circuits (charge pumps), and switching regulators. After the following subsections, these techniques are briefly introduced and described.

1.2.1 Linear Regulators

The linear regulator generally used in low load current condition. It had simple architecture and no switching ripple with respect to the other types of power management IC's [1]-[4]. The LDO also requires smaller layout area, footprints and low drop-out voltage to provide high performance and high efficiency.

The linear regulator used a pass device between the input supply voltage and the

regulated output voltage. An error amplifier controls the gate voltage of the pass transistor with respect to a reference voltage. These devices are constructed in a negative feedback configuration to maintain the output voltage irrespective of load current and input voltage variations. As illustrated in Fig. 2. It shows the schematic of a linear regulator that operates linearly to maintain the output voltage according to the reference voltage.

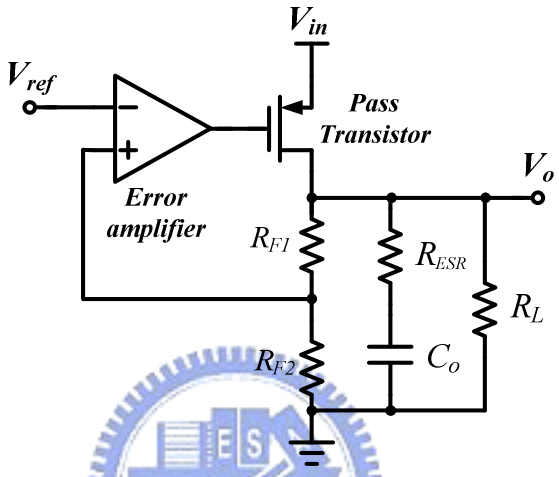


Fig. 2. The schematic of a low drop-out linear regulator

1.2.2 Switching Capacitor Circuits

The switching capacitor circuits, also called as charge pumps, that is usually used to obtain a dc voltage higher or inverting than the supply voltage in low load current applications [5]-[8]. The charge pump circuit uses capacitors as energy storage devices and MOSFET as switches. The control circuit is switched in complementary or differential phases such that the required multiple output voltage were maintained.

Fig. 3 illustrated a closed loop switching capacitor voltage doubler circuit. The voltage control oscillator receives the signal from *Error amplifier* and generates the oscillation frequency that corresponds to difference voltage between feedback node via the divided resistors and the V_{ref} voltage. The switching phase Φ_1 is closed during the first interval of

switching period, connecting to the fly capacitor C_f between the input voltage V_{IN} and ground. In this period, the energy is stored by the fly capacitor C_f and the voltage across the fly capacitor equals V_{in}.

During the second interval of switching period, the switching phase Φ_2 turned on and the fly capacitor has been connected between V_{in} and V_o. The output voltage equals twice of V_{in} because of the voltage across fly capacitor is V_{in}. In order to maintain the output voltage, there are many ways to modulate the voltage of switching capacitor circuits such as Dickson, Makowski, TPVD and MPVD charge pumps.

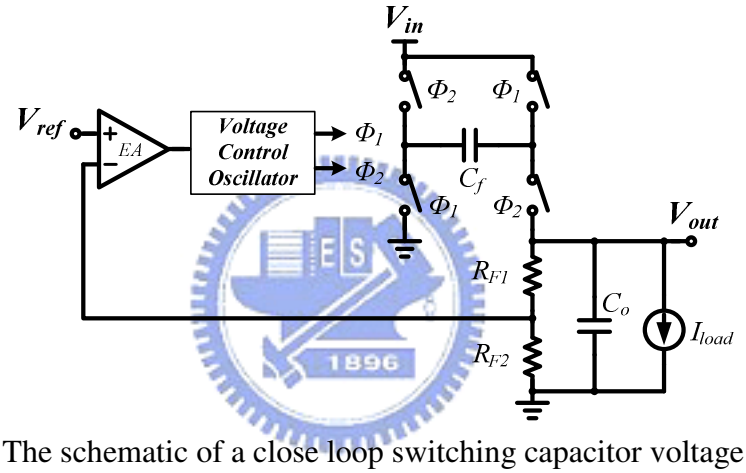


Fig. 3. The schematic of a close loop switching capacitor voltage doubler

The switching capacitor circuits are useful in many different applications such as low-voltage circuits, dynamic random access memory circuits, electrically erasable programmable read-only memory (EEPROM), transceivers and so on.

1.2.3 Switching Regulators

Switching regulators are widely used in power supply systems because it has many excellent advantages such as high power efficiency, high conversion ratio and programmable [9]-[12]. As showed in Fig. 4. The simple architecture of buck converter with two switches that one (S_1) is connected between input node and power stage, the other one (S_2) is connected

between ground and power stage. The power stage is like as low pass filter.

The regulators transfer energy to output node in periodic pulse waveform by turning on/off the semiconductor switches S_1 and S_2, alternately.

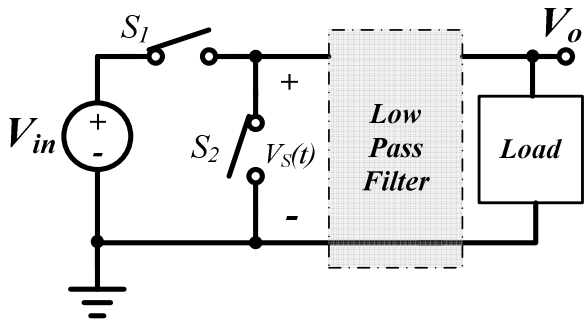


Fig. 4. The simple architecture of buck converter

The pulse signal often formed as Fig. 5. When the S_1 is closed, the $V_s(t)$ equals the input voltage V_{in}. Alternately, when the S_2 is closed, the $V_s(t)$ equals the ground voltage - zero. The periodic pulse waveform is connected with a low pass filter that consisted with an inductor and a capacitor. Recall from Fourier analysis that the dc component of a periodic waveform is equal to its average value. Hence, the dc value of $V_s(t)$ is

$$V_s = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{in} \tag{1}$$

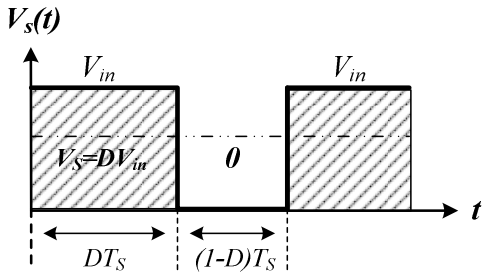
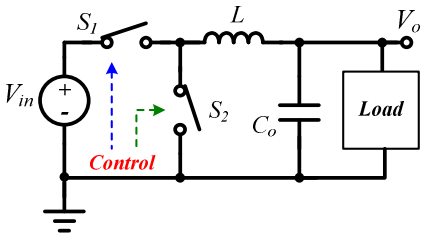
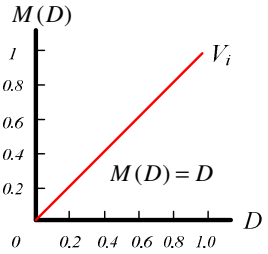
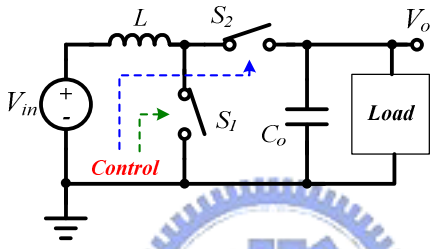
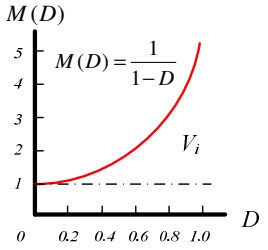
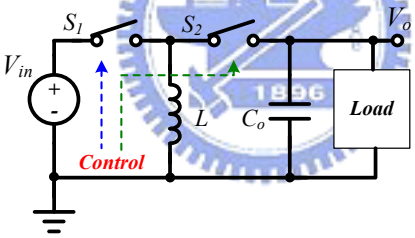
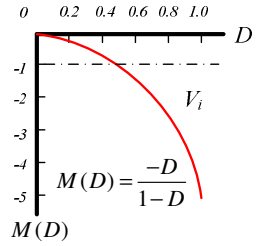


Fig. 5. The periodic waveform in Fourier analysis

Therefore, the switching regulators can classify into three topologies as functional works. Listed in Table 1, are buck, boost and flyback converters.

Table 1. Three architecture of switching regulators

	Architecture	Conversion Curve
Buck		
Boost		
Flyback		

The first regulator called as buck converter because its property that step down the input voltage with respect to output node. The conversion ration *M(D)* is written as $M(D)=D$. The second regulator called as boost converter because its property that step up the input voltage with respect to output node. The conversion ration *M(D)* is written as $M(D)=\frac{1}{1-D}$. The last regulator called as flyback converter also named buck-boost converter because its property that step up or down the input voltage with respect to output node. The conversion ratio *M(D)* is written as $M(D)=\frac{-D}{1-D}$.

Table 2. Comparative table of power supply circuits.

	Linear Regulators	***Charge Pumps***	***Switching Regulators***
Efficiency	Low	Medium	High
Power Capability	Medium	Medium	High
Footprint area	Compact	Moderate	Large
Cost	Low	Medium	High
Complexity	Low	Medium	High
Noise	Low	Medium	High

There are many advantages of switching regulators to compare with the linear regulators and charge pumps. Switching regulator had high current efficiency because it used power MOSFET as switches and inductor, capacitors as energy stored elements. When the switched transistor operated in the cutoff region, it had no power dissipation. When the switched transistor operated in triode region, it was nearly a short circuit with little voltage drop across it, and had little power dissipation. Hence, almost power dissipation was spent in output node; high power efficiency could be achieved numerically in the range 80% to 90%.

Switching regulator also had disadvantages. There were more complexity in circuit design than the linear regulators and also required discrete components such as inductor and capacitors. Furthermore, the transition response time and output noise were larger than the linear regulators.

A comparison table between linear regulators, charge pumps and switching regulators were listed in Table 2. In Table 2, we can realize that switching regulators are the best choices for power supplies driving portable application because of their high efficiency and high power capability.

1.3 Thesis Organization

In the following chapters, the concepts of DC/DC buck converter with current-mode controller were organized in chapter 2. In chapter 3, we proposed the high-efficiency slope compensation (HSC) circuit used to eliminate the sub-harmonic oscillation phenomenon that is different from conventional compensation technique. In this chapter, the diagram accompany the mathematical derivation will be explained in detail. The analysis and designs of the sub-circuit implementation and the HSPICE simulation results were shown in chapter 4. Chapter 5 shows the optimal efficiency transition changing from PWM to PFM mode. The conclusions and results were included in chapter 5.

Chapter 2

Definition and Operation Principle of Current Mode Buck Converters

2.1 General Specifications

DC-DC converter of current-mode controller has been developed a long time. It had many specifications and performances that required recognizing. Current-mode controller of voltage regulator is difficult to analyze because of its multi-loop structure that consisted of voltage feedback loop as well as current feedback loop. There are many differences between voltage mode and current mode controller. In the following sections, we will model and simplify with intuitive method and mathematical derivations of the current-mode controller.

The following subsections include significant specifications such as load regulation, line regulation, transient response, loss and power efficiency were described in detail. Moreover, there are many kinds of operation modes like as CCM and DCM mode also included in this chapter.

Finally, in many applications, the current mode control technique almost had excellent performance with respect to the voltage mode controller. Hence, we will emphasize the current mode controller rather than the voltage mode one.

2.1.1 Load Regulation

Load regulation is a measurement result that estimates the ratio of output voltage variation over load current changes. The equation (2) is written as below. A small load regulation value means that the converter has more immunity from output resistance variation. The design issue about minimizing the load regulation is increasing the system loop gain. Therefore, the load regulation could be improved.

$$\text{Load Regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} \quad (mV/mA) \tag{2}$$

2.1.2 Line Regulation

Line regulation is a measurement result that estimates the ratio of output voltage variation over input voltage changes. The equation (3) is written as below. It can account for the immunity from input noise. A small line regulation value has more robustness against to supply noise.

$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (mV/mV) \tag{3}$$

2.1.3 Transient Response

The transient response is an important measurement result that estimates the performance of converters. A good transient response implies that a small voltage drop and faster settling time on output node when output loading changes with step function. Therefore, the following describes the characteristics of transient response. It analyzed with output capacitor, equivalent series resistor of capacitor, transient time and so on.

System bandwidth is a function of transient response that implies a wide bandwidth having faster transient response and small voltage drop. It can separate into two fields about frequency domain and time domain analysis. In frequency domain, literature about [13]-[16], used to position the pole and zero location when transient was occurred. In transient period, it moved the domain pole to higher frequency to get the higher unit gain bandwidth (UGB). In the same words, the higher unit gain bandwidth had faster transient response.

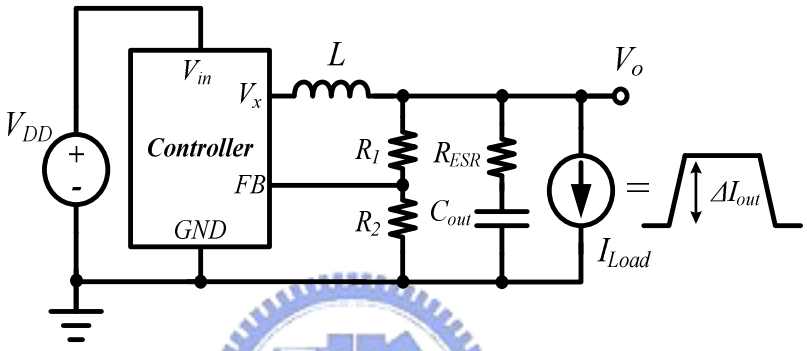


Fig. 6 System diagram of buck converter with dynamic load response

In time domain analysis, the system diagram of buck regulator with dynamic load response shows in Fig. 6. It shows that there are feedback resistor R_1 R_2, output capacitor C_{out} and equivalent series resistor of capacitor R_{ESR}. Fig. 7 shows the transient waveform of output voltage with load current variation. When the transient response was occurred namely load current from light to heavy, the transient period of t_1 had low current drawn from high side transistor. Owing to the system bandwidth restricted the speed of feedback response; the system is too late to extent the duty cycle that caused insufficient inductor current to provide for output node. Therefore, the output capacitor plays the role of current source to sustain the output current requirement. As a result, the voltage drop V_{drop} can be formulated as:

$$V_{drop} = \frac{\Delta I_{out} \cdot t_1}{C_{out}} + V_{ESR} \quad , \quad V_{ESR} = \Delta I_{out} \cdot R_{ESR} \tag{4}$$

The period t_1 almost determined by the system bandwidth. At this transient period, the voltage drop V_{drop} equal the variation of charges on capacitor adds the V_{ESR}. The V_{ESR} represents the quantity of output current variation to multiply the equivalent series resistance of capacitor. The period of t_2 is dependent on the time requirement of the high side transistor to charge the output capacitor to regulated voltage. The summation of t_1 and t_2 is known as "Recovery Time". In opposition side, the voltage peak V_{peak} occurs at the load current from heavy to light. When the transient response was acted, the transient period of t_3 had large current supplied from high side transistor. System bandwidth also restricted the speed of feedback response; the system is too late to reduce the duty cycle that caused much inductor current into output node. As a result, the voltage peak V_{peak} will jump to high and formulated as below.

$$V_{peak} = \frac{\Delta I_{out} \cdot t_3}{C_{out}} + V_{ESR}, \quad V_{ESR} = \Delta I_{out} \cdot R_{ESR} \tag{5}$$

At this transient period, the voltage drop V_{drop} equals the variation of charges on capacitor adds the V_{ESR}.

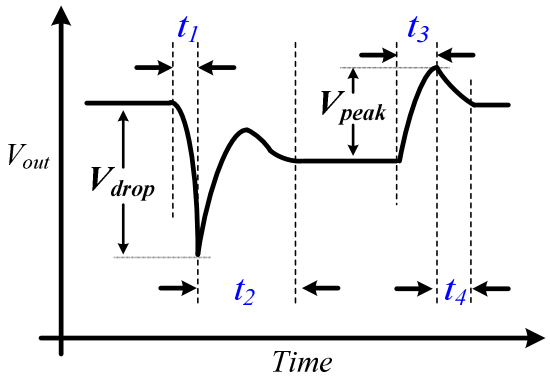


Fig. 7. Transient waveform of output voltage at load current variation.

During the period t_4, the redundant charges stored on output capacitor are discharged through feedback resistor and the output voltage goes back to regulated level gradually.

2.1.4 Losses and Efficiency

2.1.4.1. Conduction Loss

Power loss of regulators is the combination of the switching loss and the MOSFET's conduction loss in equation (6). The conduction loss also can classify into high-side transistor loss and low-side transistor loss.

$$P_{MOSFET} = P_{SW} + P_{COND} \tag{6}$$

Calculating the high-side conduction loss is straightforward that the conduction loss is just the I^2R loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \frac{V_{OUT}}{V_{IN}} \tag{7}$$

Where $R_{DS(ON)}$ is at the maximum operation MOSFET junction temperature ($T_{J(MAX)}$) Low-side loss are also comprised of conduction loss and switching loss. Conduction loss for low-side is given by:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \tag{8}$$

2.1.4.2. Switching Loss

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current power MOSFET's gate to charge its input capacitance. There is no switching

loss until V_{GS} reaches the MOSFET's V_{TH} therefore power loss equal zero.

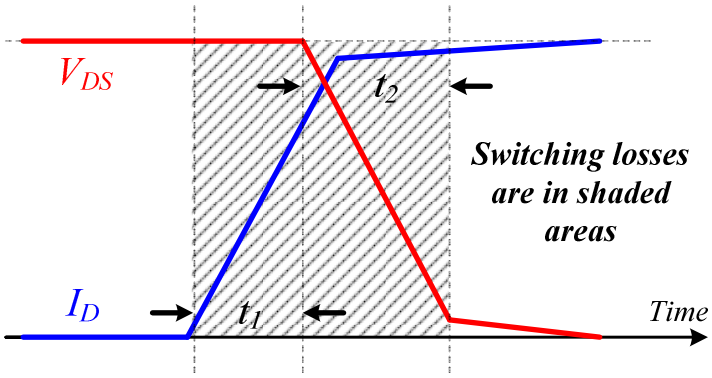


Fig. 8. Transient waveform of V_{DS} and I_D curve in switching losses on power MOSFET

When V_{GS} reaches V_{TH}, the input capacitance (C_{ISS}) is being charged and I_D (the MOSFET's drain current) is rising linearly until it reaches the current I_L which is presumed to be I_{out}. During this period (t_1) the MOSFET is sustaining the entire input voltage across it, the energy in MOSFET during t_1 is:

$$P_{t_1} = t_1 \cdot (\frac{V_{in} \cdot I_{out}}{2}) \tag{9}$$

Now, we enter t_2. At this point, I_{out} is flowing through high-side MOSFET, and the V_{DS} begin to fall. All of the gate current will be going to recharge C_{GD}. C_{GD} is similar to the "Miller" capacitance of transistor, so t_2 could be thought of as "Miller time". During this time the current is constant (at I_{out}) and the voltage is falling fairly linearly from V_{IN} to 0, therefore:

$$P_{t_2} = t_2 \cdot (\frac{V_{in} \cdot I_{out}}{2}) \tag{10}$$

The switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = (\frac{V_{in} \cdot I_{out}}{2}) \cdot (t_1 + t_2) \cdot F_S \tag{11}$$

2.1.4.3. Static Loss

The static loss also called as quiescent loss that was consumed by controllers of switching regulators. The smaller quiescent loss had higher efficiency.

$$P_Q = V_{in} \cdot I_Q \tag{12}$$

The other power losses that don't be mentioned above obeyed the rules of I^2R.

2.1.4.4. Efficiency

The efficiency of switching regulator is defined as the ratio of the output power consumption and input power supplies, formed as below:

$$E_{ff} = \frac{P_O}{P_{in}} = \frac{P_O}{P_O + P_Q + P_{SW} + P_{COND} + P_{Else}} \times 100\% \tag{13}$$

The input power supplies consist of the output consumption (P_O), quiescent loss (P_Q), switching loss (P_{SW}), conduction loss (P_{COND}) and other losses (P_{Else}) in parasitic elements. A high efficiency results in a high performance extending the battery life.

2.2 DC Model for Current Mode Buck Converter in CCM Analysis

The block diagram of DC-DC buck converter with current programmable controller is shown in Fig. 9. The power stage connected to high-side and low-side transistors called as power MOSFET. The gate signal of power MOSFET is drove by driver stage that the drive signal is generated by non-overlap and pulse generator circuit with pulse-width modulation (PWM) or pulse-frequency modulation (PFM) method. The control circuit also contained voltage-reference generator, sawtooth generator, voltage adder and current sensor that used to current programmable circuit only. The control sequence with pulse-width modulation (PWM) is described as follows.

In the first interval of switching period T_S, the clock signal forced the high-side transistor to turn on and the low-side transistor to turn off. At this interval, the inductor current ramped up and sensed by the current sensing circuit. The sensed signal V_{sense} is added with ramp signal V_{ramp} to avoid the sub-harmonic oscillation phenomenon in current mode controller. When the sum of signal V_{sense} and V_{ramp} exceed the error amplifier's signal V_C, the comparator (*COMP*) turns from low to high and changes into the second interval of switching period. In the second interval, the power PMOS turns off and power NMOS turns on. The feedback voltage is forced the same as reference voltage that caused the output voltage is regulated in specified level. Moreover, there are two control loops feeding current signal and voltage signal by current feedback loop and voltage feedback loop, respectively. The current feedback loop constructed by current sense circuit and the voltage feedback loop constructed by error amplifier. In dynamic control, the output voltage variation affects the V_C signal generated by error amplifier to increase or decrease the duty cycle in modulation.

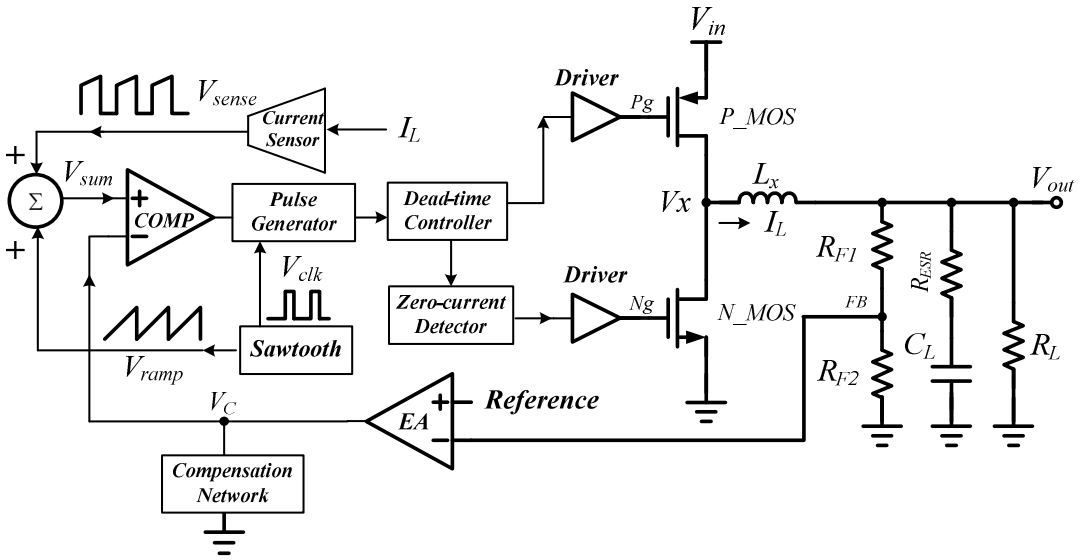


Fig. 9. The block diagram of current mode buck converter

The current programmed controller is unstable when converter operates above 50% duty cycle without compensation that shows in Fig. 10. The unstable problem called as sub-harmonic oscillation phenomena. In other words, the perturbed quantity of inductor current was large more and more during a few periods. The phenomena also occurred in other topologies such as boost and buck-boost converters. To avoid this stability problem, the control scheme is usually modified by adding an artificial ramp to the sensed current in the following descriptions.

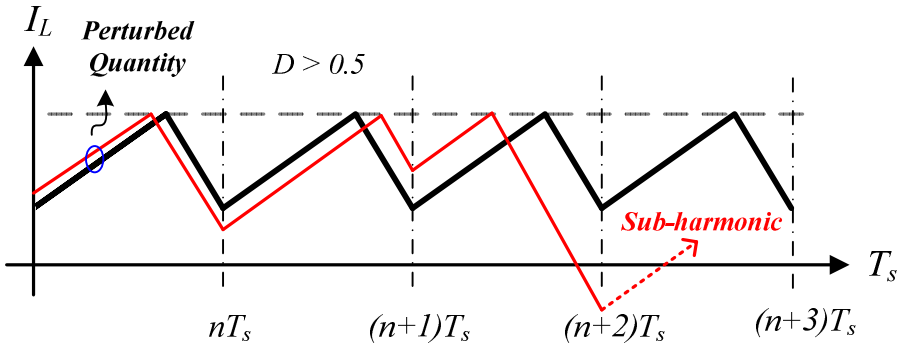


Fig. 10. Inductor current at stable and unstable oscillation in current-mode converter

The steady-state and perturbed waveform of inductor current are illustrated in Fig. 11. We can explain the phenomena of steady-state waveform and perturbed waveform with derived formula. The steady-state waveform of inductor current with m_1 slope ramps up in

first interval and ramps down with m_2 slope in second interval. When the perturbed waveform of inductor current occurred with $\hat{d}T_s$, the current difference was introduced in $m_1 \cdot \hat{d}T_s$ [17][18].

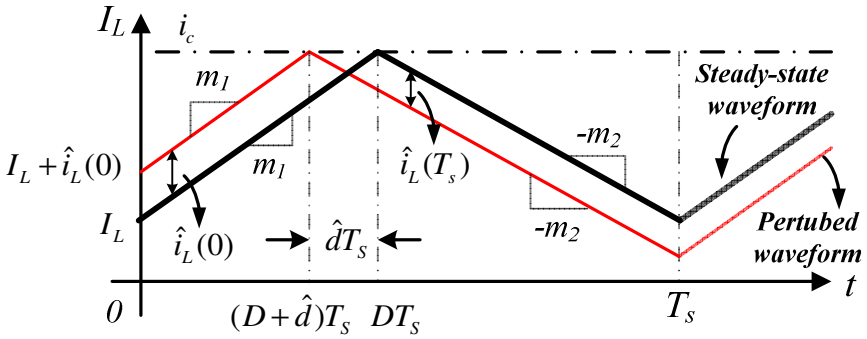


Fig. 11. The perturbation waveform of inductor current

The slope of inductor current equals:

$$m_1 = \frac{V_{in} - V_{out}}{L}, \; m_2 = \frac{V_{out}}{L} \tag{14}$$

According to Fig. 11, we can derive:

$$i_L(T_s) = i_L(DT_s) - m_2 D' T_s = i_L(0) + m_1 DT_s - m_2 D' T_s \tag{15}$$

In steady-state, the above equation $i_L(0) = i_L(T_s)$ and shows as:

$$0 = m_1 DT_s - m_2 D' T_s \;, \; then : \frac{m_2}{m_1} = \frac{D}{D'} \tag{16}$$

From Fig. 11, we can use the steady-state waveform to express the current difference $\hat{i}_L(0)$ $\hat{i}_L(T_s)$ as the slope multiplied by the interval length, Hence:

$$\hat{i}_L(0) = -m_1 \hat{d}T_s \quad , \quad \hat{i}_L(T_s) = m_2 \hat{d}T_s \tag{17}$$

Elimination of the intermediate variable $\hat{d}$ from equation (17) leads to:

$$\hat{i}_L(T_s) = \hat{i}_L(0) \cdot \left(-\frac{m_2}{m_1} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right) \tag{18}$$

A similar analysis can be performed during the next switching period, show that:

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s) \cdot \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right)^2 \tag{19}$$

After *n* switching periods, the perturbation becomes:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1) \cdot T_s) \cdot \left(-\frac{D}{D'} \right) = \hat{i}_L(0) \cdot \left(-\frac{D}{D'} \right)^n \tag{20}$$

Note that, as *n* tends to infinity, the perturbation $\hat{i}_L(nT_s)$ tends to zero provided that the characteristic value *–D/D'* has magnitude less than one. Conversely, the perturbation $\hat{i}_L(nT_s)$ becomes large in magnitude when the characteristic value $\alpha = -D/D'$ has magnitude greater than one:

$$\begin{aligned} \left| \hat{i}_L(nT_s) \right| &\to 0 \quad when \left| -\frac{D}{D'} \right| < 1 \\ \left| \hat{i}_L(nT_s) \right| &\to \infty \quad when \left| -\frac{D}{D'} \right| > 1 \end{aligned} \tag{21}$$

Hence, for the stable operation of the current mode controller, we need *D/D'*<1 or *D*<0.5.

The stable situation with compensation ramp is presented in Fig.12. When the converter operates with *D*<0.5, the perturbation inductor current will lead to be stable. Conversely, the perturbation inductor current will lead to be unstable to cause the sub-harmonic oscillation if converter operates with *D*>0.5 and no compensation.

The sub-harmonic oscillation is a well-known problem of current-mode controller. However, the converter can be stable at all duty cycles by adding the compensated ramp to the sensed inductor current as shown in Fig. 12. This compensated ramp has the qualitative effect of reducing the gain of the current sensing feedback loop to solve the unwanted oscillation problem in current-mode controller of dc-dc converters.

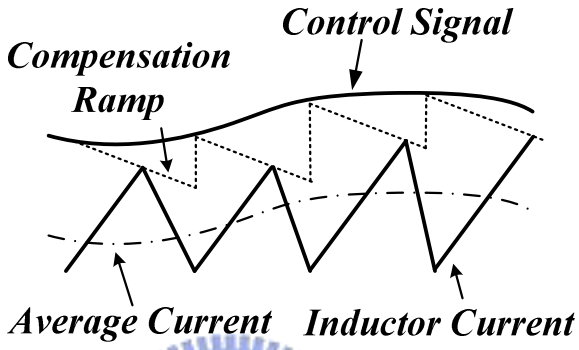


Fig. 12. Current-mode control signal with the compensation ramp and inductor current

The compensation theorem is represented in Fig. 13, the perturbation $\hat{i}_L(0)$ and $\hat{i}_L(T_s)$ can express in terms of the m_1, m_2, m_a and the $-\hat{d}T_s$ as follows:

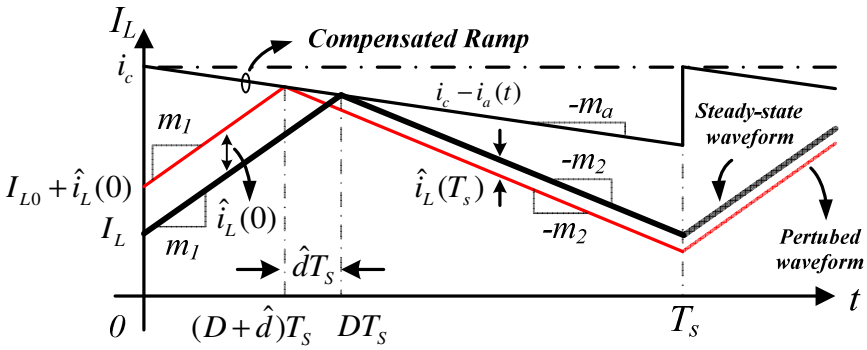


Fig. 13. Steady-state and perturbed inductor current waveforms with compensation

$$\hat{i}_L(0) = -\hat{d}T_s \cdot (m_1 + m_a) \tag{22}$$

$$\hat{i}_L(T_s) = -\hat{d}T_s \cdot (m_a - m_2) \tag{23}$$

Elimination of $-\hat{d}T_s$ yields:

$$\hat{i}_L(T_s) = \hat{i}_L(0) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right) \tag{24}$$

A similar analysis can be used to the n^{th} period, leading to:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1) \cdot T_s) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right) = \hat{i}_L(0) \cdot \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)^n = \hat{i}_L(0) \cdot \alpha^n \tag{25}$$

For larger n periods, the perturbation magnitude $\hat{i}_L(nT_s)$ tends to equations (26). Therefore, for stability of current mode controller in CCM, it needs to choose the slope of the artificial ramp m_a such that the characteristic value α has magnitude less than one. Conversely, the perturbation $\hat{i}_L(nT_s)$ becomes larger when the characteristic value α has magnitude greater than one:

$$\begin{aligned} \left| \hat{i}_L(nT_s) \right| &\to 0 \quad when \ |\alpha| < 1 \\ \left| \hat{i}_L(nT_s) \right| &\to \infty \quad when \ |\alpha| > 1 \end{aligned} \tag{26}$$

One common choice of the compensation ramp slop is

$$m_a = \frac{1}{2} m_2 \tag{27}$$

This compensation ramp results in the characteristic value α to become zero for all duty cycle of the converter. Therefore, $\hat{i}_L(T_s)$ is leading to zero for any $\hat{i}_L(0)$.

Another common choice of m_a is:

$$m_a = m_2 \tag{28}$$

The above characteristic causes the value α to become zero for all duty. As a result, $\hat{i}_L(T_s)$ is zero for any $\hat{i}_L(0)$ that the controller doesn't saturate. This behavior is known as *deadbeat control* when the system corrects all errors after one switching period. And the compensated inductor current shows in Fig. 14.

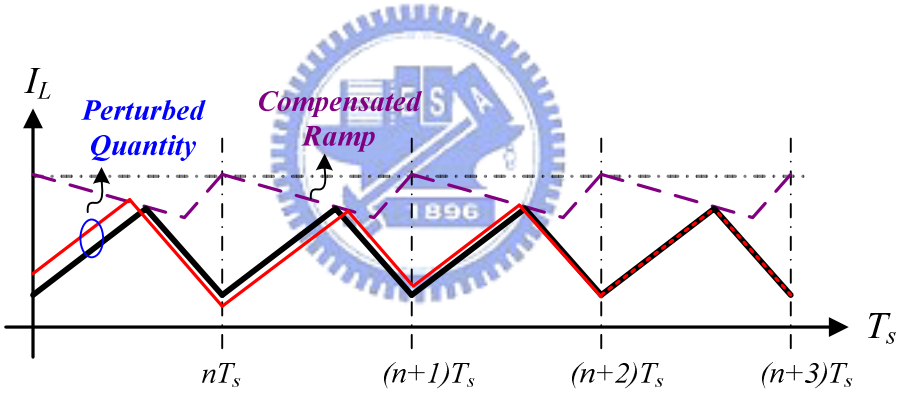


Fig. 14. Inductor current with compensation ramp for few periods

2.3 DC Model for Current Mode Buck Converter in DCM Analysis

When the switches of dc-dc converter are implemented by using current-unidirectional semiconductor, there would be discontinuous conduction mode (DCM) introduced. The discontinuous conduction mode arises when the switching ripple of inductor current is large enough to cause the polarity of the applied switching current to reverse, such that the reversed current occurred. The DCM is commonly observed in dc-dc converters and rectifiers.

Discontinuous conduction mode typically occurs with large inductor current ripple at light loading and contains current-unidirectional switches. Since it is usually required that converters operate with their loads removed, DCM is frequently encountered. Moreover, some converters are purposely designed to operate in DCM mode for all loads.

A simple asynchronous buck converter shows in Fig. 15. The inductor current waveform I_L, diode current waveform I_D and the power MOS current I_{Q_1} of switching regulators are sketched in Fig. 16. The inductor current contains a dc component $I_{L(avg)}$ with an amplitude of switching ripple $\triangle i_L$.

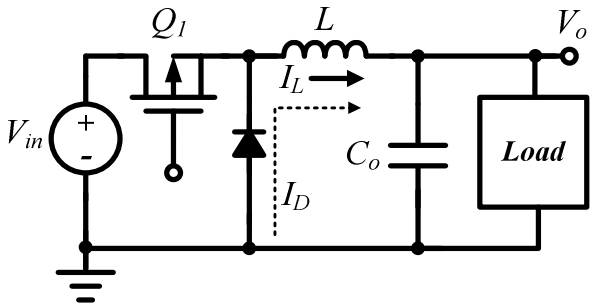


Fig. 15. The asynchronous buck converter

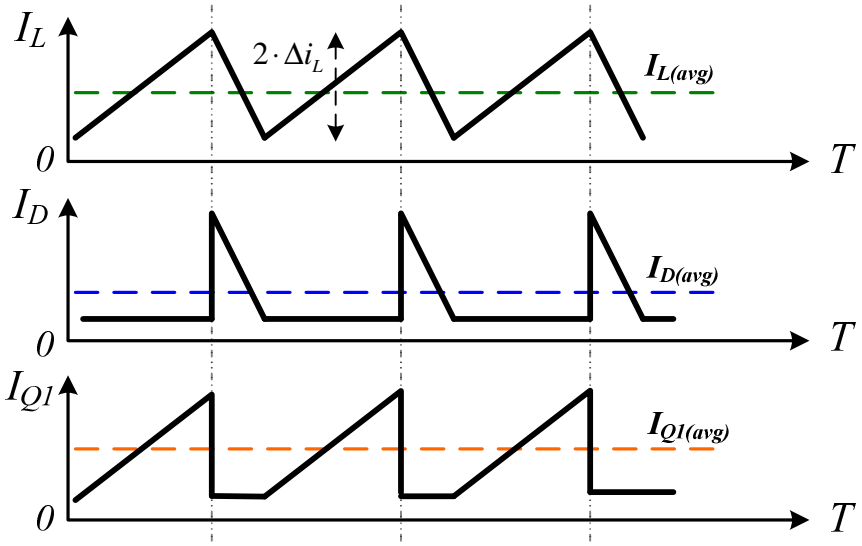


Fig. 16. The current waveform of inductor, diode and power MOS(I_{Q1})

$$I_{L(avg)} = \frac{V_o}{R_L} \tag{29}$$

$$\Delta i_L = \frac{V_{in} - V_o}{2L} DT_s = \frac{V_{in} DD' T_s}{2L} \tag{30}$$

When the load resistance R_L is increased, the dc load current $I_{L(avg)}$ also decreased. As the dc component of inductor current $I_{L(avg)}$ decreased, the ripple magnitude will still remain unchanged. If we continue to increase R_L, eventually the boundary is reached

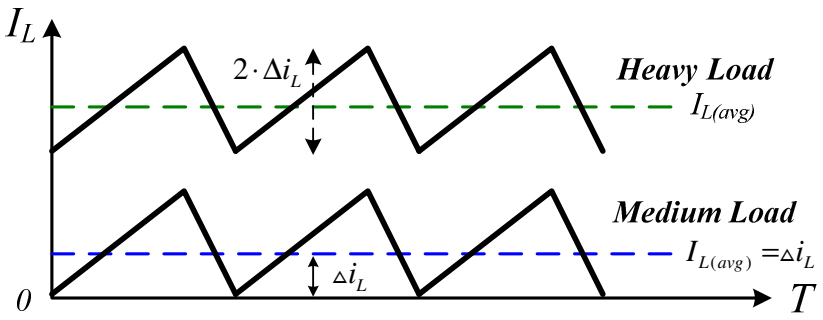


Fig. 17. Inductor current are CCM operation at heavy and medium loads

where $I_{L(avg)} = \triangle i_L$, illustrated in Fig. 17. It can be seen that the inductor current I_L and diode current are both zero at the end of the switching period. Indeed, the load current is positive and nonzero.

When we continue to increase the load resistance R_L, the diode current cannot be negative; because of the diode in reverse-biased before the end of the switching period. As illustrated in Fig. 18, there are three subintervals during each switching period. During the first subinterval D_1T_s, the transistor Q_1 conducts and the diode conducts during the second subinterval D_2T_s. At the end of second subinterval, the diode current reaches zero, and the remainder of the switching period neither the transistor nor the diode conduct. The converter operates in discontinuous conduction mode.

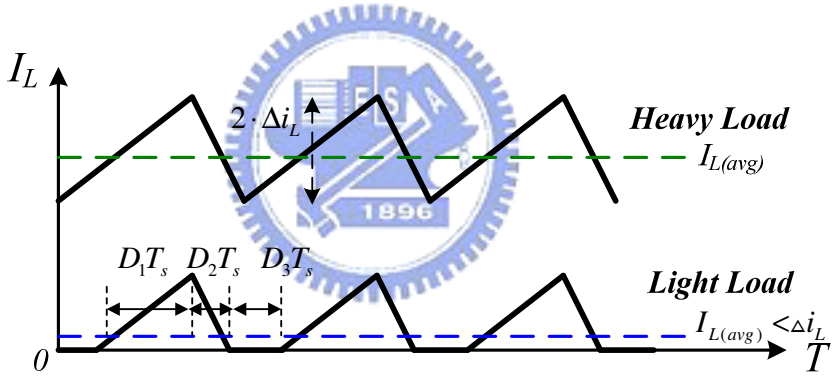


Fig. 18. Inductor current are CCM and DCM operation at heavy and light loads

Formulation (31) suggests a way to fine the boundary between the continuous and discontinuous conduction modes. It can be seen that, for buck converter, the diode current is positive over the entire interval $DT_s < t < T_s$ provided that $I_{L(avg)} > \triangle i_L$. Hence, the conditions for operation in the continuous and discontinuous conduction modes are:

$$\begin{aligned} I_{L(avg)} - \triangle i_L > 0 \quad & \text{without reversed current} \\ I_{L(avg)} - \triangle i_L < 0 \quad & \text{with reversed current} \end{aligned} \tag{31}$$

Where $I_{L(avg)}$ and $\triangle i_L$ are found assuming that the converter operates in continuous

conduction mode. Insertion of Eqs (29) and (30) into Eq. (31) yields the following condition for operation in discontinuous conduction mode:

$$\frac{DV_{in}}{R_L} < \frac{DD^{'}T_sV_{in}}{2L} \tag{32}$$

Simplification leads to:

$$\frac{2L}{R_LT_s} < D^{'} \tag{33}$$

This can also be expressed in:

$$\begin{aligned} &K < K_{crit}(D) \quad for \;\; DCM \\ &where \quad K = \frac{2L}{RT_s} \;\; , \;\; K_{crit}(D) = D^{'} \end{aligned} \tag{34}$$

The dimensionless parameter K is a tendency measure of a converter to operate in discontinuous conduction mode. Large values of K lead to continuous mode operation, while small values lead to the discontinuous mode for different parameters. The critical value $K_{crit}(D)$ is a function of duty cycle, and equals to $D^{'}$ for the buck converter.

The critical value $K_{crit}(D)$ versus duty cycle is plotted in Fig. 19. For the figure shown, it can be seen that the converter operated in DCM at low duty cycle, and CCM at high duty cycle. The Fig. 20 shows the switching converter in CCM mode with heavier loads. Namely, the load resistance R_L is reduced, such that K is larger. If K is greater than one, then the converter operates in continuous conduction mode for all duty cycles.

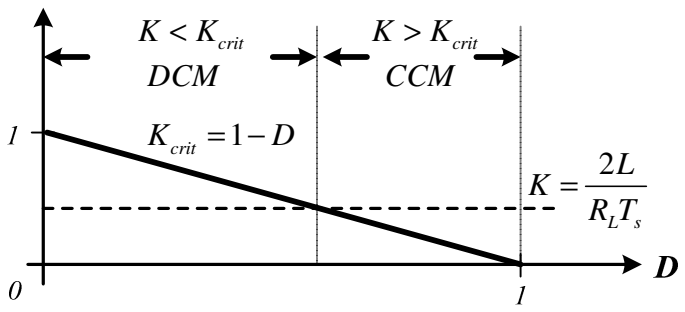


Fig. 19. Operation boundary of CCM and DCM modes

It's simple to express the mode boundary in terms of the load resistance R_L, rather than the parameter K. Equation (34) can be rearranged to expose the dependent of the mode boundary with the load resistance:

$$\begin{aligned} &R < R_{crit}(D) \quad for \;\; CCM \\ &R > R_{crit}(D) \quad for \;\; DCM \end{aligned} \qquad where \;\; R = \frac{2L}{D^{'}T_s} \tag{35}$$

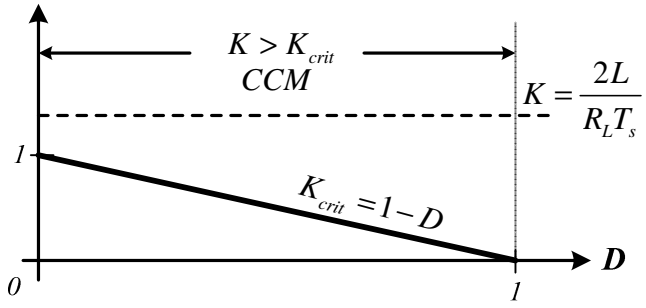


Fig. 20. Switch converter operates in CCM mode for all duty

The conclusion can be formulated as below:

$$\begin{aligned} &K > K_{crit}(D) \quad or \quad R < R_{crit}(D) \quad for \;\; CCM \\ &K < K_{crit}(D) \quad or \quad R > R_{crit}(D) \quad for \;\; DCM \end{aligned} \tag{36}$$

A similar mode boundary analysis can be performed for other converters. The boost and buck-boost converters are analyzed in the same manner. The results are listed in Table 3, for basic dc-dc converters.

Table 3 CCM-DCM mode boundaries for buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0\le D\le 1}(K_{crit})$	$R_{crit}(D)$	$\min_{0\le D\le 1}(R_{crit})$
Buck	$1-D$	1	$\frac{2L}{(1-D)T_s}$	$\frac{2L}{T_s}$
Boost	$D\cdot(1-D)^2$	$\frac{4}{27}$	$\frac{2L}{D\cdot(1-D)T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-Boost	$(1-D)^2$	1	$\frac{2L}{(1-D)T_s}$	$\frac{2L}{T_s}$

Chapter 3

Derivation and Circuit Implementation of High-Efficiency Slope Compensation Technique

So far, we know that the current programmable controlled converter requires the slope compensation technique to eliminate the sub-harmonic oscillation phenomenon. Hence, the use of artificial ramp adding to the sensed inductor current is a useful and popular method in control circuits. As shown in Fig. 21, the *Current-Sensor* circuit connects to the V_x node that located between *High-side PMOS* and *Low-side NMOS* and introduces V_{sense} signal. The *Slope Compensator* circuit introduces V_{slope_comp} signal periodically. The both signals V_{sense} and V_{slope_comp} go through the *voltage-to-current (V-I)* circuits to introduce I_{sense} and I_{slope_comp}

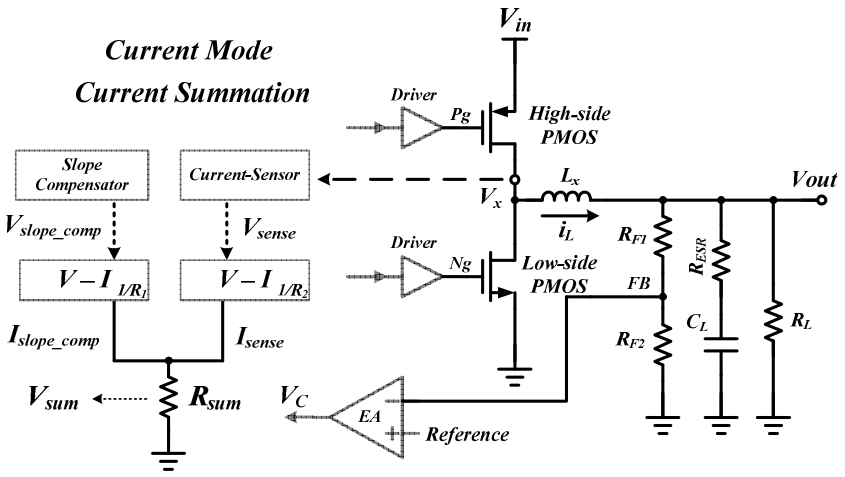


Fig. 21. Slope compensation diagram of current mode buck converter

signal, respectively. The both signals I_{sense} and I_{slope_comp} flow into the resistor R_{sum} and generate the V_{sum} signal. The signal V_{sum} will define the duty cycle of switching converter. This paper introduced the operation modes with pulse width modulation (PWM) and pulse frequency modulation (PFM) in heavy load and light load condition, respectively [19][20]. However, there is a significant problem that how to decide the suitable transition time from PWM to PFM mode. Therefore, in conventional mode-transition method, shown in Fig. 22, there is a *Mode Detector & PFM Controller* circuit that consists of *Zero-Current Detector*, *ZCD Counter*, *Mode Selector* and *PFM Controller*.

When the converter operates in light loading and the inductor current ripple is larger than the average load current, it's occurred reversal flowing. The V_x voltage touched the zero voltage to generate the one-shot signal (*ZCD signal*) in the output of *Zero-Current Detector*. The *ZCD signal* accessed into the *ZCD Counter* to identify, whether the converter changes into PFM mode or not. Then, the signal accesses into *Mode Selector* circuit to decide the operation mode and able or disable the *PFM Controller* immediately.

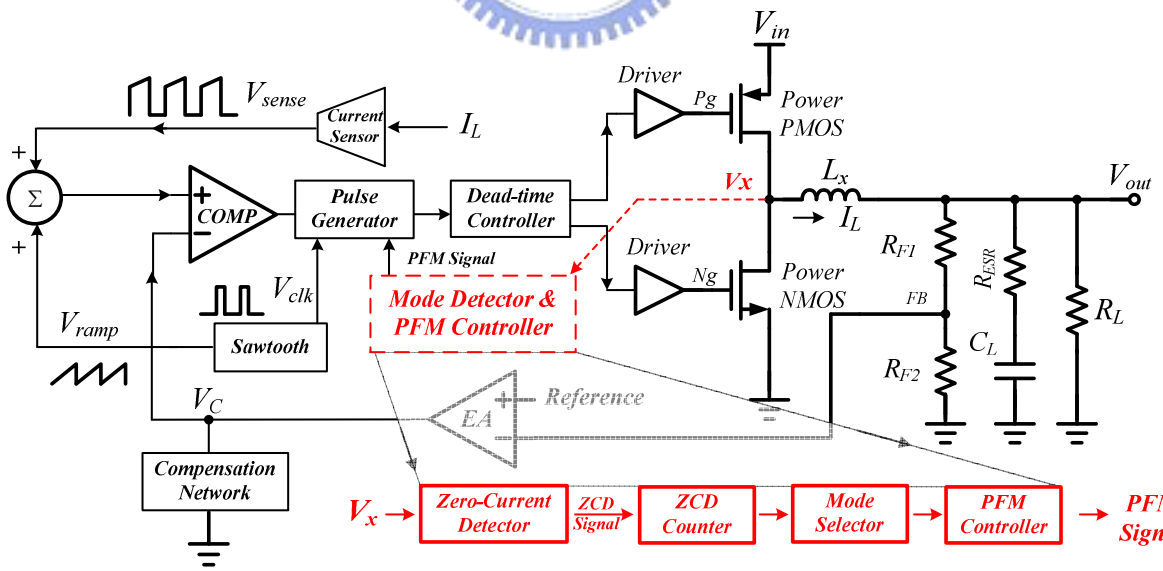


Fig. 22. Conventional mode-transition detection architecture

Unfortunately, the V_X signal has poor noise immunity and is easy to be coupled by turning on/off of power MOSFETs. Especially, this scenario is deteriorated in high switching frequency since the switching noise causes many undesired signal and thus the system

randomly transits between PWM and PFM modes. Therefore, this paper presents a method using the output voltage (V_C) of error amplifier as a detection signal rather than the V_X voltage in Fig. 23. The output voltage of error amplifier can be input independent parameter by means of the proposed *HSC controller*. The signal V_C only depends on load current condition. Thus, the new detection signal V_C with robust immunity to noise contains load current information to identify the operation mode immediately without using the *Zero-Current Detector*. Thus, in the following descriptions, we will introduce the control issues of proposed high-efficiency slope compensation circuit and circuit implementations.

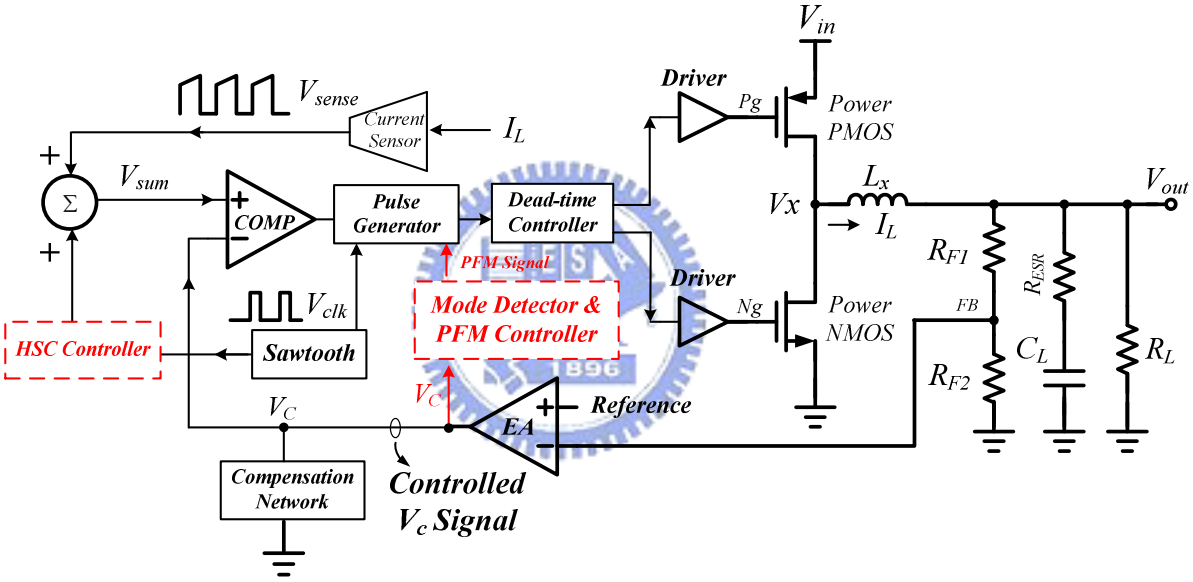


Fig. 23. Conventional mode-transition detection architecture

3.1 Concern Issues of Proposed Slope Compensation Technique

High-efficiency slope compensation technique, shown in Fig. 24, as the supply voltage (V_{IN}) changes from high to low, the duty cycle (D) changes from low to high. Thus, the output voltage (V_C) of error amplifier will raise a voltage difference (ΔV). If we use the V_C voltage as

a detection signal to identify the operation mode, the voltage difference (ΔV) makes the load current identification with wrong state. Figure shows that the duty cycle increases as the supply voltage decreases, the raising voltage difference (the red dash line) touches the boundary of operation mode (V_{PFM_S}) and turns on the PFM mode operation. For example, 200mA of load current is the boundary of mode transition. Due to the voltage difference rising, the load current drops to 150mA to change mode. It implies that the PFM mode is delay to turn on. Oppositely, the duty cycle decreases as the supply voltage increases, the falling voltage difference (the blue dash line) touches the boundary of operation mode (V_{PFM_S}) and turns on the PFM mode operation. It implies that the PFM mode is early to turn on. Owing to the supply voltage variation, the output voltage (V_C) of error amplifier would be disturbed by a voltage difference (ΔV). Therefore, the next section will introduce the proposed high-efficiency slope compensator to overcome the above problems.

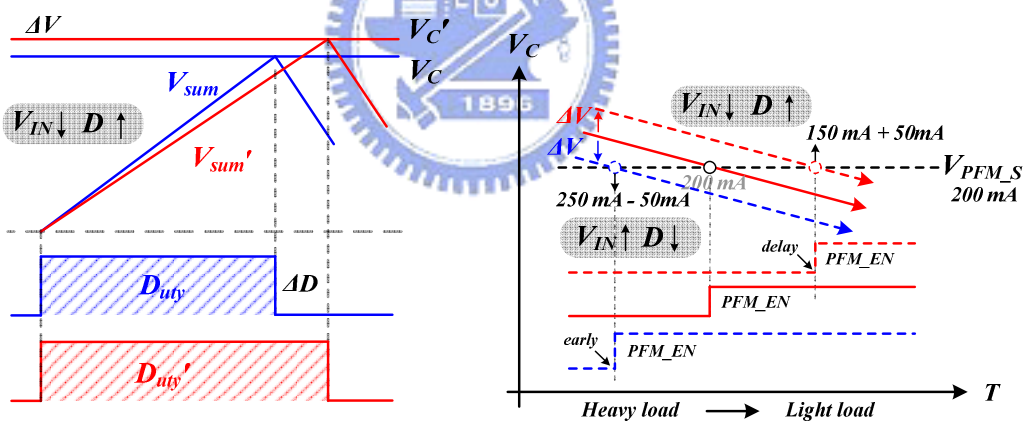


Fig. 24. Duty cycle variation due to supply voltage variation and mode transition diagram

Moreover, the simple architecture of current mode buck converter is shown in Fig. 25. The sensed voltage from current sensing circuit and the compensated ramp from sawtooth generator flow into the *V-I Pair* circuit and introduce the summation signal V_{sum}. The V_{sum} signal and the V_c signal, which comes from error amplifier; connect to the comparator *CMP* to generate the *Reset* signal. The both signal *CLK* and *Reset* feed through the *Pulse-Generator* circuit to define the PWM duty cycle of switching period. When the V_{sum} signal varied with

duty cycle, the V_c signal will also follow the V_{sum} signal to define equivalent duty width as the same previous switching period because of duty cycle is only dependent on V_{in} and V_{out} voltages.

According to theory of the V_c signal varies with the V_{sum} signal, we can use the V_{sum} signal to control the V_c signal on our way. As the V_c signal is changed by output load current variation only, it had current information of heavy or light loadings. Thus, we can use the V_c signal to identify, what is the suitable opportunity for changing the operation mode. Hence, we have to design the V_{sum} signal independently with supply voltage and dependents on load current variations. Therefore, the V_{sum} signal is controlled by the load current variation specifically. We used the V_c signal to decide the suitable transition time from pulse width modulation (PWM) into pulse frequency modulation (PFM) mode.

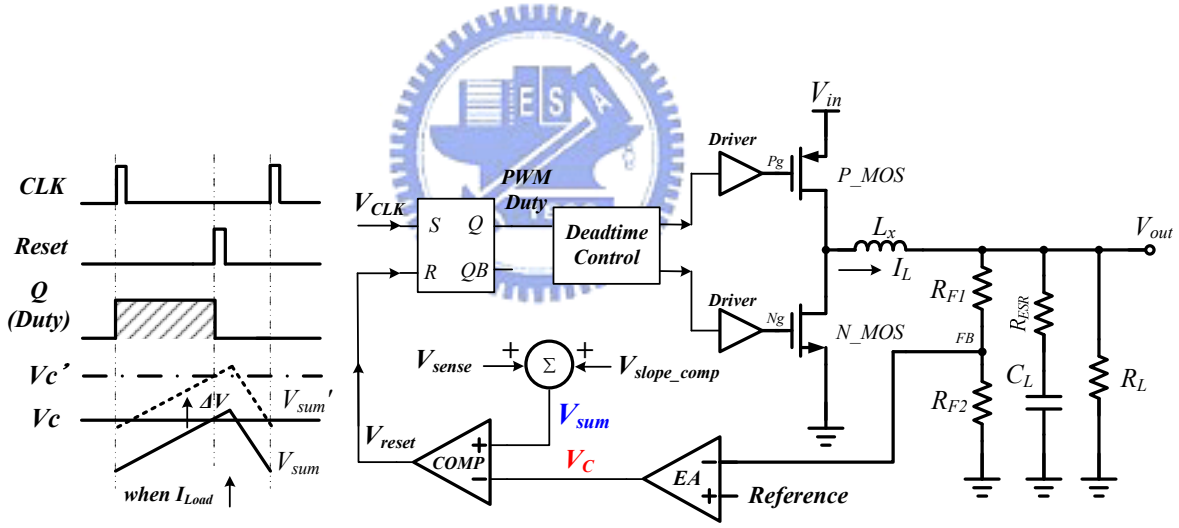


Fig. 25. Simple architecture of current mode buck controller in different loads

3.2 Design Theorem of Proposed Slope Compensation Technique

According to theory of the V_c signal varies with the V_{sum} signal, we have to design the V_{sum} signal independent of input voltage variation and only dependent on load current changes. Thus, in this section, we will derive the mathematical formulas by changing supply voltages from high to low with fixing the output voltage. In other words, the output voltage is identical all the time regardless of input voltage variation.

In Fig. 26, the I_{sense} and I_{ramp} signals is introduced by *current-sense* and *Ramp-Generator* circuits through the *voltage-to-current* (*V-I*) circuits, respectively. The both signals I_{sense} and I_{ramp} flow into the resistor R_{sum} and generate the summation result V_{sum} signal, shown in equation (37).

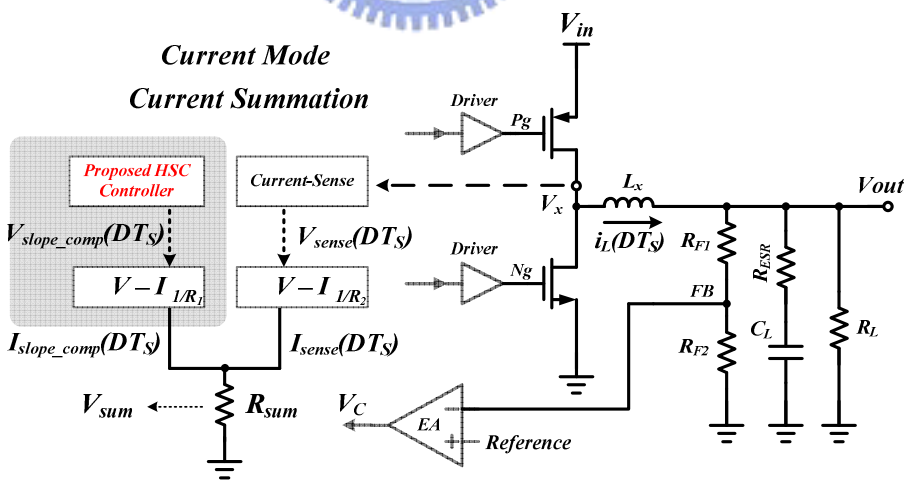


Fig. 26. The slope compensation diagram of current mode buck converter

$$V_{sum} = \left(I_{slope\_comp}(DT_S) + I_{sense}(DT_S)\right) \cdot R_{sum} \tag{37}$$

The V_{sum} signal consists of the I_{ramp} current adding the I_{sense} current and both are

multiplied by R_{sum} resistor. Therefore, we will analysis the V_{sum} signal to separate into the I_{ramp} current and the I_{sense} current individually. To identify what factors affected the quantities of the I_{ramp} and I_{sense} current.

As depicted in the Fig. 27 below, the waveform is the inductor current with ramp up and ramp down slopes in switching period called as m_1 and m_2. The equations of m_1 and m_2 expressed as (38), (39).

$$m_1 = \frac{V_{in} - V_{out}}{L} \tag{38}$$

$$m_2 = \frac{V_{out}}{L} \tag{39}$$

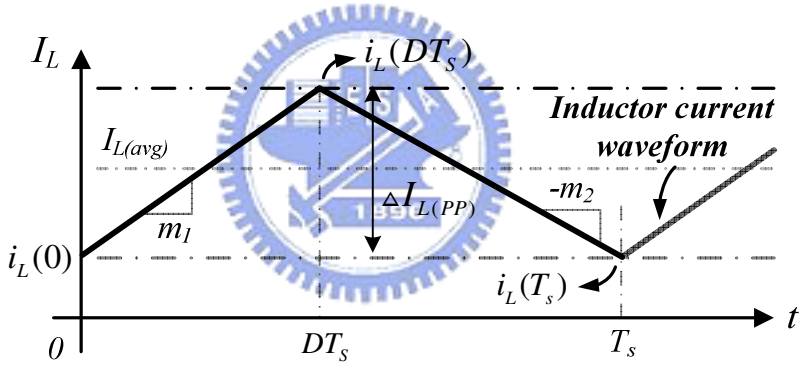


Fig. 27. Inductor current in DC and AC analysis

The slope m_1 ramps up in DTs period and slope m_2 ramps down in Ts-DTs period. Hence, we can derive the $i_L(DTs)$ that consists of the $I_{L(avg)}$ and half of $\Delta I_{L(PP)}$ to express the relationships between $I_{L(avg)}$ and $\Delta I_{L(PP)}$ in equation (40). The signal $i_L(DTs)$ means the waveform function of inductor current.

$$i_L(DT_S) = I_{L(avg)} + \tfrac{1}{2}\Delta I_{L(pp)} \tag{40}$$

The $I_{L(avg)}$ means the average value of inductor current. We can realize that the average value of inductor current is reverse proportional to the output resistor R_L, shown in equation

(41).

$$I_{L(avg)} = \frac{V_{out}}{R_L} \tag{41}$$

And the $\Delta I_{L(PP)}$ can express as slope m_1 to multiply the first interval of switching period DTs or the slope m_2 to multiply the second interval of switching period $(1\text{-}D)Ts$, shown in equation (42) and (43).

$$\triangle I_{L(PP)} = m_1 \cdot DT_s = \frac{V_{in} - V_{out}}{L} \cdot DT_s \tag{42}$$

$$\triangle I_{L(PP)} = -m_2 \cdot (1-D)T_s = \frac{V_{out}}{L} \cdot (1-D)T_s \tag{43}$$

Therefore, the $i_L(DTs)$ is the summation of Eqs (41) and (42) leading to:

$$i_L(DT_S) = \frac{V_{out}}{R_L} + \frac{1-D}{2L \cdot f_S} V_{out} \quad [\, V_{out}, L, f_S \ \textit{are} \text{ constant }] \tag{44}$$

We can recognize that the $i_L(DTs)$ signal with constant parameters of V_{out}, L, fs is dependent on the variables of duty cycle (D) and output resistor (R_L). In other words, the $i_L(DTs)$ signal is reverse proportional to the duty cycle and output resistor R_L as input voltage variation and output load current changes, respectively. Because the resistor R_L is reverse proportional to the load current, the $i_L(DTs)$ signal is proportional to the load current changes. Hence, there are two parameters of output resistor (R_L) and duty cycle (D) to change the $i_L(DTs)$ signal of inductor current.

The Fig. 28 shows the current sensing circuit that almost used to current programmable controller. The circuit sensed the inductor current in the first interval of switching period. The sensed current of inductor is scaled down by a factor K to generate the signal I_{sense}. The I_{sense} signal flows into the resistor R_{sense} to introduce the voltage V_{sense} that is the output signal of current sensing circuit.

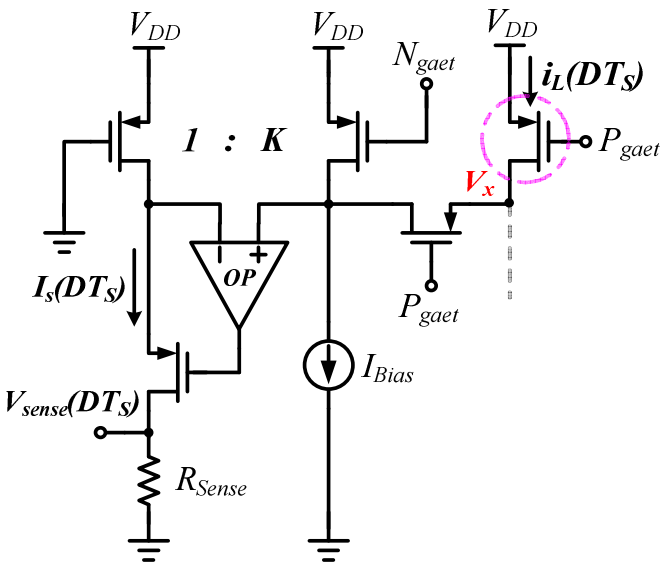


Fig. 28. Current sensing circuit

In Eqs (45), the signal $I_S(DT_S)$ is the $i_L(DTs)$ divided by a K factor to scale down the quantities of inductor current.

$$I_S(DT_S) = \frac{i_L(DT_S)}{K} \tag{45}$$

The sensed current flowed into the resistor to generate the voltage $V_{sense}(DT_S)$ in Eqs (46). Arranging the equation, the $V_{sense}(DT_S)$ equals the R_{sense} to divide by a factor K and multiplied by $i_L(DTs)$.

$$V_{sense}(DT_S) = I_S(DT_S) \cdot R_{sense} = \frac{R_{sense}}{K} \cdot i_L(DT_S) \tag{46}$$

In equation (47), we use the symbol R_s to express the R_{sense} over factor K called as current sensing equivalent resistor or sensing gain.

$$V_{sense}(DT_S) = R_S \cdot i_L(DT_S) = i_L(DT_S) \cdot 1\Omega \quad , \quad [\ let \ \ R_S = 1\Omega\ ] \tag{47}$$

Recommendation of current sensing equivalent resistor R_s is in the range 0.5 ~ 1 ohm. This paper assumed the equivalent resistor to equal one ohm for simplification the circuit design. Hence, the $V_{sense}(DT_S)$ voltage equals the $i_L(DT_S)$ function.

So far, we had derived the inductor current varied with duty cycle and output loadings. Therefore, the continued conceptions will derive the sawtooth ramp information dependent on duty cycle variations.

The sawtooth ramp (V_{ramp}) with clock pulse (V_{CLK}) is depicted as below in Fig. 29. The clock signal changes to high level when the sawtooth signal ramps down from V_H to V_L. On the other hand, the, the clock signal changes to low level when the sawtooth signal ramps up from V_L to V_H.

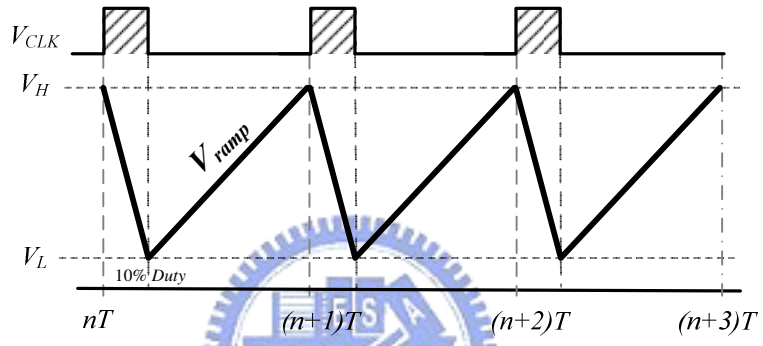


Fig. 29. Sawtooth waveform with clock pulse

In the analysis of sawtooth ramp, the microcosmic waveform is illustrated in Fig. 30. The sawtooth signal ramps up and down between the V_H and V_L voltages. The upper and lower boundary (V_H, V_L) define the sawtooth ramp region from zero percent duty to one hundred percent duty of switching period. As the duty beginning, the sawtooth ramps up from 0% to

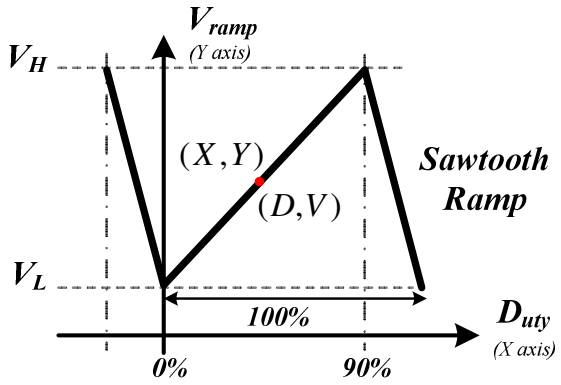


Fig. 30. The microcosmic waveform of sawtooth ramp

90% duty. When the ramp signal touched the upper boundary V_H, it ramps down from 90% duty to 100% duty to accomplish complete switching cycle. However, the afterward 10% ramp is useless for system stability, we will derive the relationships of the sawtooth signal and duty cycle in the first interval of switching cycle. Then, the linear algebra is a useful manner to prove the relations.

In the figure shows, the x-axis means duty cycle and the y-axis means voltage. We can use the equation to derive the following in Eqs (48).

$$\frac{Y - V_L}{X} = \frac{V_H - V_L}{90\% - 0\%} \tag{48}$$

To arrange the above equation, Y signal expressed as below that is dependent on X variable.

$$Y = \frac{V_H - V_L}{0.9} \cdot X + V_L \tag{49}$$

Replacement the X variable with duty cycle (D) and Y variable with ramp signal (V_{ramp}) showed in equation (50).

$$V_{ramp} = \frac{V_H - V_L}{0.9} \cdot D + V_L \quad [\ V_H, V_L \ are \ \text{constant}\ ] \tag{50}$$

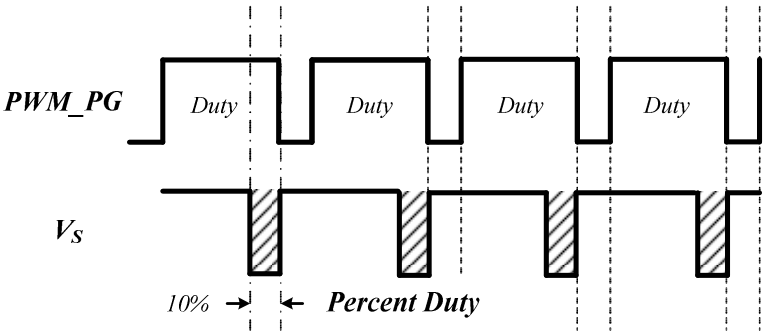


Fig. 31. Duty cycle with percent duty control

Moreover, this paper proposed a significant ten percent control pulse that is produced before the ending of duty width [21][22][23]. In other words, the pulse signal occurred before ending the system duty is 10%. For example, when the system operates at 70% duty cycle, the pulse signal operates at logic low from 60% to 70% duty width of switching cycle. The concept is illustrated in Fig. 31. The *PWM_PG* is the signal that controlled the high-side MOSFET and the width of logic high is the system duty cycle. The shaped region of V_S signal is ten percent width of switching cycles. Thus, we use the produced signal V_S to the next stage circuit called as slope controller to generator the quadratic ramp ($V_{quadratic\_ramp}$) in 10% region. The simple diagram with I_{ramp} current source, two MOS switches and a charged capacitor is showed in Fig. 32. The ramp current is controlled by the 10% signal of V_S pulses. When the V_S signal is low, the I_{ramp} current flowed into the capacitor as the MP_1 is turned on. Oppositely, the V_S signal is high, the charge drained out of the capacitor as the MN_1 is turned on. During the charging and discharging switches, the circuit generates the output signal of $V_{quadratic\_ramp}$ voltage periodically. The $V_{quadratic\_ramp}$ voltage will be used to replace the original sawtooth signal of conventional slope compensation circuit. The proposed $V_{quadratic\_ramp}$ voltage is effective to maintain the V_C voltage regardless of power supply variations. Therefore, the following descriptions will derive the proposed theorem in procedures.

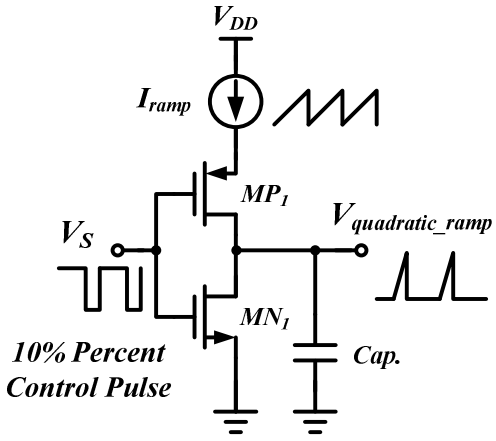


Fig. 32. The simple diagram of the slope controller

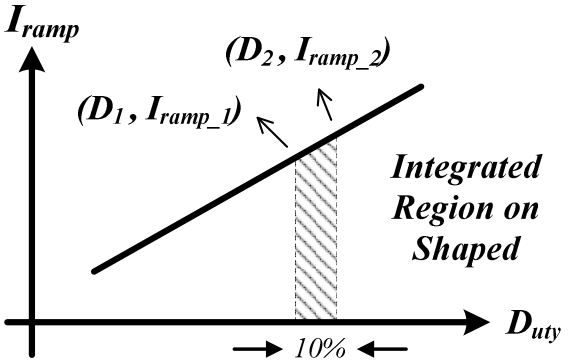


Fig. 33. The I_{ramp} current is charging only with 10% pulse

The Fig. 33 shows the I_{ramp} current to charge the capacitor with 10% charging time of switching period. Because of the I_{ramp} current is proportional to the duty cycle, the different time is corresponding to different quantities of I_{ramp} signal. We can recognize that the I_{ramp_1} current corresponds to D_1 at the beginning of charging, and he I_{ramp_2} current corresponds to D_2 at the end of 10% pulse. Then, we use the formula that derived in equation (49) to represent the different ramp voltage on different duty in equation (51) and (52).

$$V_{ramp\_1} = \frac{V_H - V_L}{0.9} D_1 + V_L \tag{51}$$

$$V_{ramp\_2} = \frac{V_H - V_L}{0.9} D_2 + V_L \tag{52}$$

The different ramp voltages (V_{ramp_1} & V_{ramp_2}) on different duty were transformed into current signals (I_{ramp_1} & I_{ramp_2}) with assumed resistor R_x in equation (53).

$$I_{ramp\_1} = \frac{V_{ramp\_1}}{R_X}, I_{ramp\_2} = \frac{V_{ramp\_2}}{R_X} \tag{53}$$

According to the formula of the capacitor charging in equation (54), the charged voltage

$$\because C \cdot V = I \cdot T \quad \therefore V = \frac{I \cdot T}{C} \tag{54}$$

is the current multiplying by the time period and dividing by capacitor value.

We got the result of V_{slope_comp} signal that is the integration of the shaped area in Fig. 33 and in equation (55).

$$\begin{aligned} V_{slope\_comp} &= \frac{I_{ramp\_2} \cdot D_2 T_S}{2 \cdot C} - \frac{I_{ramp\_1} \cdot D_1 T_S}{2 \cdot C} \\ &= \frac{(I_{ramp\_2} \cdot D_2 - I_{ramp\_1} \cdot D_1)}{2 \cdot C \cdot f_S} \end{aligned} \tag{55}$$

Elimination the variable D_1 and D_2 for simplification, the above equation is replaced into $D_2=D$ and $D_1=D_2-0.1$ in equation (56) as below.

$$\begin{aligned} V_{slope\_comp} &= \frac{(I_{ramp\_2} \cdot D - I_{ramp\_1} \cdot (D-0.1))}{2 \cdot C \cdot f_S} \\ &= \frac{2D \cdot (V_H - V_L) - 0.1 \times V_H + V_L}{18 \cdot C \cdot f_S \cdot R_X} \end{aligned} \tag{56}$$

The V_{slope_comp} signal is a linear equation to the duty cycle D and plots in Fig. 34. In addition, the V_{slope_comp} signal is the link of peak value of each quadratic ramp ($V_{quadratic\_ramp}$).

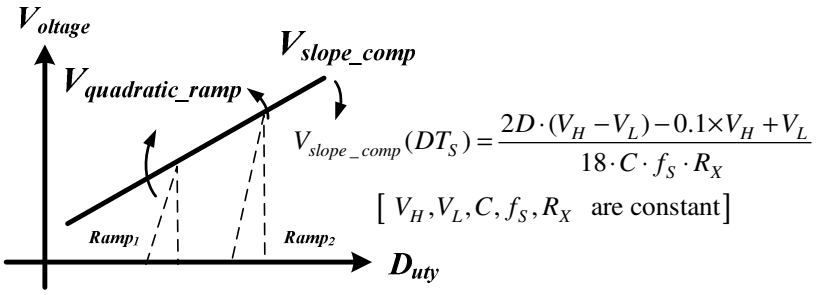


Fig. 34. The V_{slope_comp} function is a linear equation with respect to duty cycle

For example, there are two quadratic ramps ($Ramp_1$, $Ramp_2$) in different duty cycle. The peak values of the different quadratic ramps are the quadratic function (V_{slope_comp}) to substitute into the corresponding duties. The $V_{quadratic\_ramp}$ signal is a quadratic equation to the duty cycle D. But the charging period is 10% of switching cycle, the waveform of

$V_{quadratic\_ramp}$ signal in Fig. 34 is nearly like as linear equation.

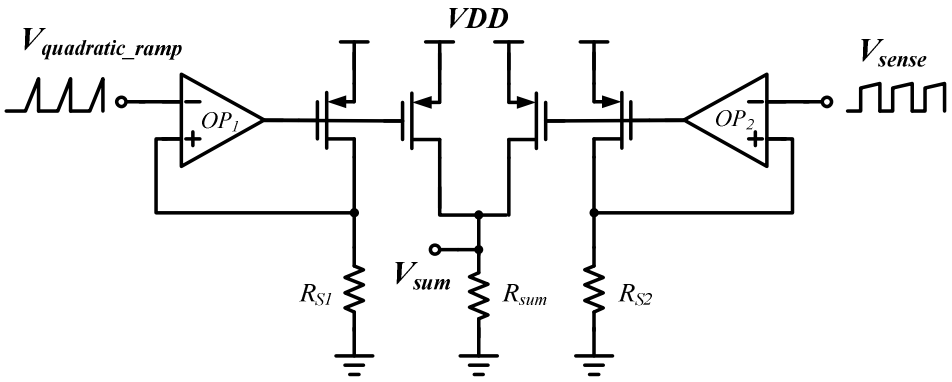


Fig. 35. The schematic of voltage adder

In the current programmable controller, we have to combine the both signal V_{sense} and $V_{quadratic\_ramp}$ together to suppress the sub-harmonic oscillation. As the Fig. 35 shown, the pairs of voltage-to-current circuit are consisted of operational amplifiers to form a voltage adder. Rather than the conventional sawtooth ramp, the proposed signal $V_{quadratic\_ramp}$ is applied to the negative node of OP_1. The combination of both signals is expressed in equation (57) as below.

$$\begin{aligned} V_{sum} &= \left(\frac{V_{slope\_comp}(DT_S)}{R_{S1}} + \frac{V_{sense}(DT_S)}{R_{S2}}\right) \times R_{sum} \\ &= \frac{R_{sum}}{R_{S1}} \cdot V_{slope\_comp}(DT_S) + \frac{R_{sum}}{R_{S2}} \cdot V_{sense}(DT_S) \end{aligned} \tag{57}$$

Substituting equations (44) and (56) into (57), we got the following formula in equation (58) and the parameters of V_H, V_L, capacitor C, inductor L, frequency f_s, output voltage V_{out}, R_x and output resistor R_L are constant values. According to the above analysis, the V_{sense} is reverse proportional to the duty cycle and the $V_{slope\_comp}(DT_S)$ is proportional to the duty cycle.

$$V_{sum} = \frac{R_{sum}}{R_{S1}} \cdot \frac{2D \cdot (V_H - V_L) - 0.1 \times V_H + V_L}{18 \cdot C \cdot f_S \cdot R_X} + \frac{R_{sum}}{R_{S2}} \cdot \left(\frac{V_{out}}{R_L} + \frac{1-D}{2L \cdot f_S} V_{out}\right) \tag{58}$$

$$[V_H, V_L, C, f_S, R_X, V_{out}, R_L, L \text{ are constant}]$$

We can represent the combinations of equation (44) with positive slope and the equation (56) with negative slope to form the equation (59). The voltage-to-current circuit in Fig. 35 provides a function of scaling. The symbol α and β represent the R_{sum} over R_{S1} and the R_{sum} over R_{S2}, respectively in equation (60).

$$V_{sum} = \frac{R_{sum}}{R_{S1}} \cdot (Positive\ Slope) + \frac{R_{sum}}{R_{S2}} \cdot (Negative\ Slope) \tag{59}$$

$$\alpha = \frac{R_{sum}}{R_{S1}} \ , \ \beta = \frac{R_{sum}}{R_{S2}} \tag{60}$$

The equation (61) shows the V_{sum} signal is the combination of the positive slope adding the negative slope multiplying the scaling α and β, respectively. Therefore, the use of changing the scaling quantities is an effective method to eliminate the slopes of positive and negative voltage each other.

$$V_{sum} = \alpha \cdot (Positive\ Slope) + \beta \cdot (Negative\ Slope) \tag{61}$$

So far, we made analyses and derived the equations of the high-efficiency slope compensation technique. The technique is a useful way to control the V_{sum} signal independent of supply voltage variation. As the result, the V_c signal is only dependent on the output loading variations of switching converters.

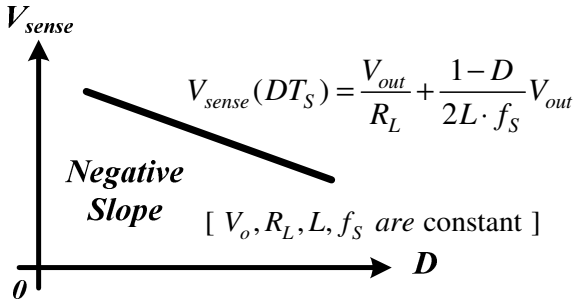


Fig. 36. The V_{sense} function is reverse proportional to the duty cycle

Finally, we synthesize the concepts to make the function plots of each equations derived before. In Fig. 36 shown, the V_{sense} waveform is reverse proportional to the duty cycle as the same as the equation derived in equation (44).

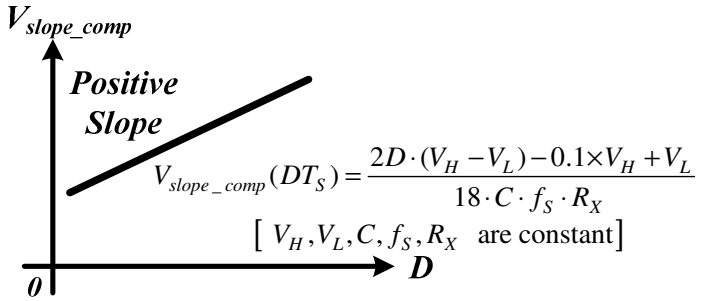


Fig. 37. The V_{slope_comp} function is proportional to the duty cycle

In Fig. 37 shown, the V_{slope_comp} waveform is proportional to the duty cycle as the same as the equation derived in equation (56).

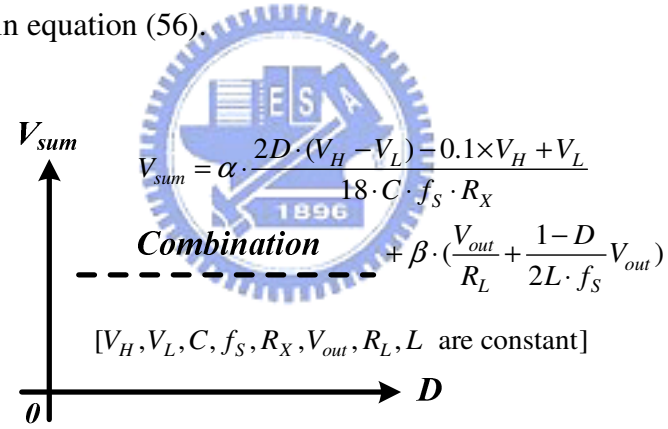


Fig. 38. The combination voltage of both signal V_{sense} and V_{slope_comp}

The combination signal V_{sum} is horizontal to imply that we could vary the symbol α and β to balance the difference of slope showed Fig. 38. In order to verify the analysis is correct and useful for the current programmable controller, this paper simulates these equations with MATLAB computer program. As illustrated in Fig. 39, the blue line indicates the V_{slope_comp} signal proportional to the duty cycle and the green line indicates the V_{sense} signal reverse proportional to the duty cycle.

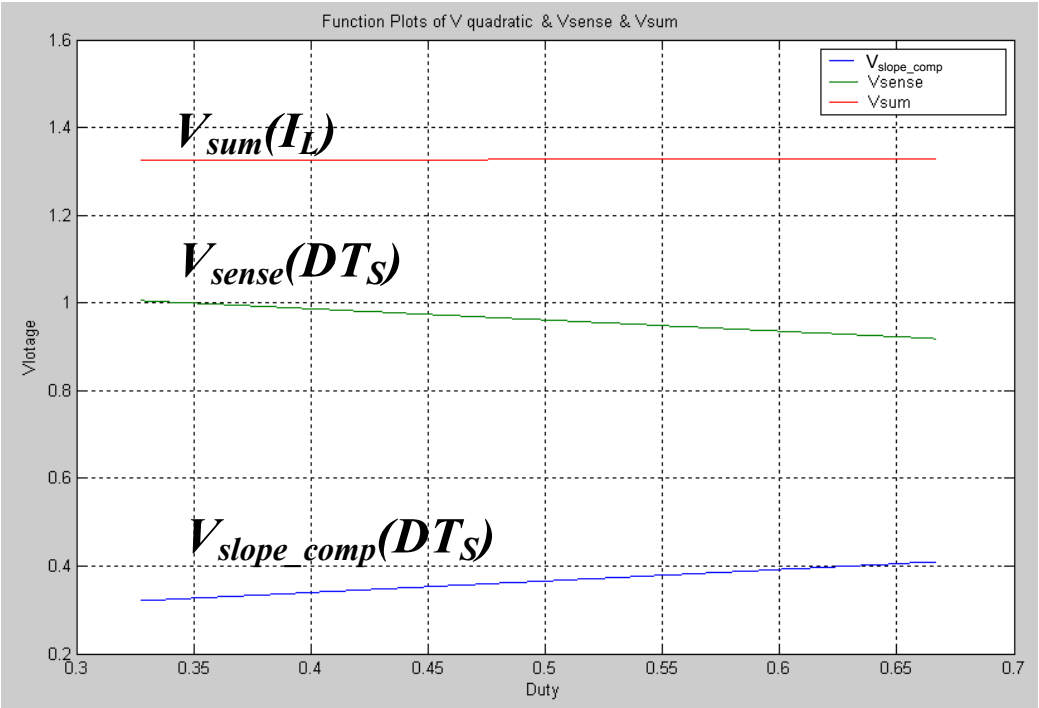


Fig. 39. Matlab diagram of V_{sense}, V_{slope_comp} and V_{sum} signals

As a result, the V_{sum} signal of the red line is horizontally independent of the duty cycle. Therefore, the method that eliminates the positive and negative slope is effective to suppress the duty variation. As long as the V_{sum} signal is controlled on our way, we could use the V_c signal to identify the situation of output loading. In other words, the voltage level of V_c signal reflect the quantities of load current information. Hence, we could use the V_c signal comparing with the pre-defined voltage to switch the operation modes.

Moreover, a significant issue should be concerned is the choice of parameters α and β. In current mode controllers, the compensation slope is used to suppress the unstable state of oscillation. If the compensation slope exceeds the suitable quantities, the current mode controller will be operated like a voltage mode converter that called as deadbeat control mentioned in chapter two. On the other hand, if the compensation slope is insufficient, it's still occurred unstable oscillation. The concept is illustrated in Fig. 40. The slope of sensed inductor current in second period and the proposed quadratic ramp is represented as $S(I_2)$ and the $S(V_{quadratic\_ramp})$, respectively.

In the figure shows, we can use the parameters α and β to modify the slope of compensation ramp $S(V_{quadratic\_ramp})$ and sensed current $S(I_2)\cdot R_s$. Owing to the stability issue, the slope of compensation ramp must be grater than half times of $S(I_2)\cdot R_s$ and be smaller than one times of $S(I_2)\cdot R_s$.

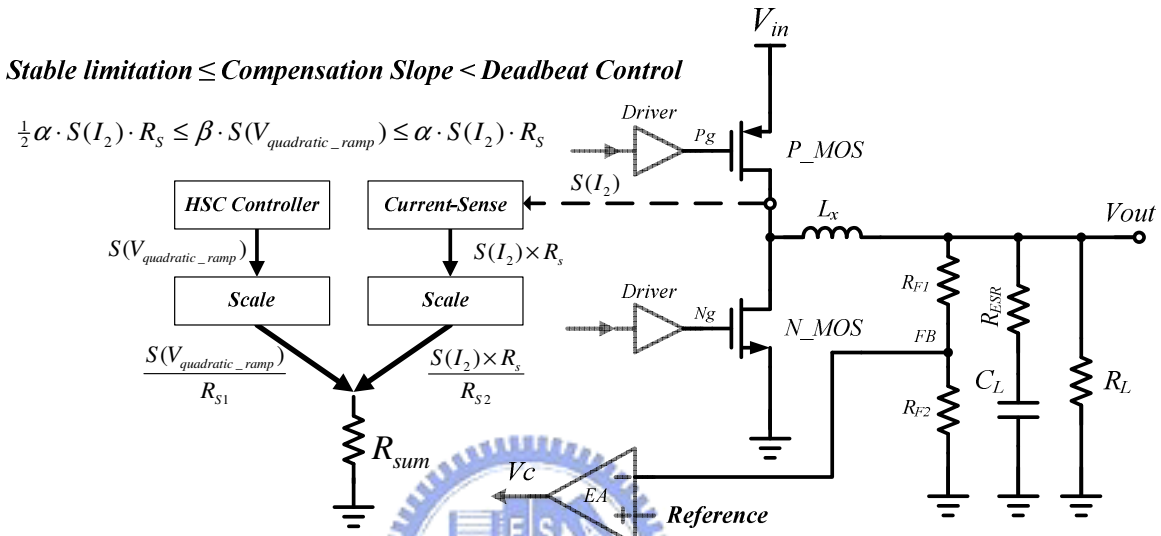


Fig. 40. Slope compensation values in reasonable range

As mentioned before, the symbol α and β is presented as:

$$\alpha = \frac{R_{sum}}{R_{S1}} \quad , \quad \beta = \frac{R_{sum}}{R_{S2}} \tag{62}$$

The stability issue is expressed below in equation (63). The parameters α and β is an effective way to control the system for stable. Hence, in this paper, we choice α is twice as β.

$$\frac{1}{2}\alpha \cdot S(I_2)\cdot R_S \le \beta \cdot S(V_{quadratic\_ramp}) \le \alpha \cdot S(I_2)\cdot R_S \tag{63}$$

3.3 Circuit Implementation of Proposed Slope Compensation

3.3.1 Pulse-Signal Generator

As mentioned before, the high-efficiency slope compensation technique requires the 10% pulse of switching period to control the system stability. The pulse signal occurred before the system duty ending and the pulse width is 10%. As illustrated in Fig. 41, this is the percent duty generator circuit not only for 10%. The use of the charging current ($10 \cdot I_{in}$) is ten times of discharging current (I_{in}) introduces the 10% duty of switching period, expressed in equation (64). The *VA* voltage is controlled by the V_S pulse that controls the charging time of current ($10 \cdot I_{in}$). In the *SR-latch*, the *S* node connects to the *CLK* signal to force the frequency of V_S signal as the same the system and the *R* node connects to the output of the comparator (*COMP*) to reset the circuit. The timing diagram is showed in Fig. 42.

$$\frac{T_1}{T} = \frac{I_{down}}{I_{up}} = 10\% \tag{64}$$

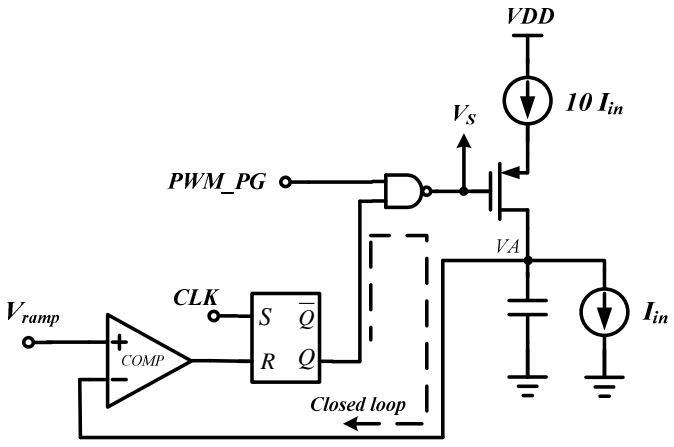


Fig. 41. Percent duty pulse generator

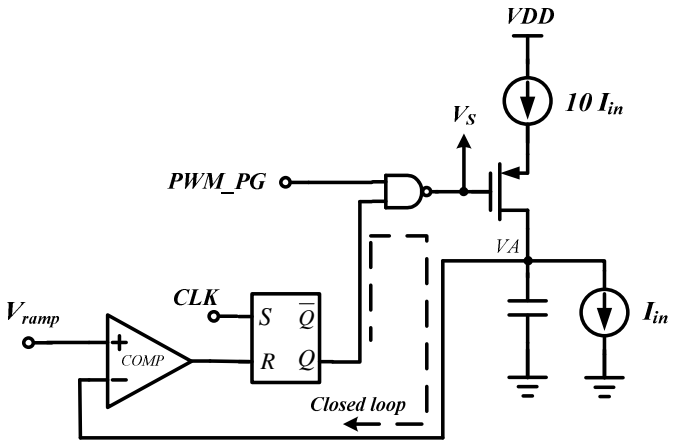


Fig. 42. Timing diagram of percent duty generator

The *PWM_PG* is the signal that controlled the high-side MOS and the high width is the system duty cycles. As the *SET* (*CLK*) signal occurred, the Q signal is from high to low. Oppositely, the *RESET* signal occurred, the Q signal is from low to high. Besides, the *RESET* signal is generated by the comparator (*COMP*) that connects with V_{ramp} and *VA* signals. Finally, the both signals *PWM_PG* and *Q* feed through the *NAND Gate* to generate the V_S signal. The V_S signal is 10% of switching period. If the user wants to modulate the percent duty of V_S, we can change the charging current in Fig. 41 as derived in equation (64).

3.3.2 Pulse-Ramp Generator

As illustrated in Fig. 43, it's the quadratic ramp generator controlled by the V_S pulse. The negative feedback loop consists of R_x, MN_1 and the operation amplifier formed a *V-to-I* circuit to transform the voltage signal V_{ramp} to the current signal I_{ramp}. The current signal I_{ramp} is mirrored by the current mirror pair MP_1 and MP_2 to charge the capacitor C_x. The switches MS_1 and MS_2 that controlled by the V_S signal used to charging or discharging the capacitor.

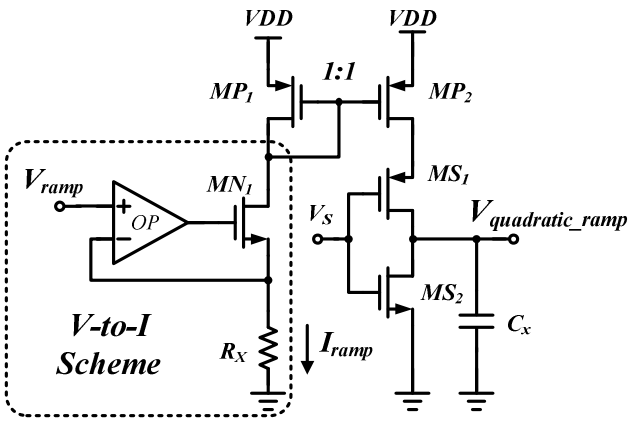


Fig. 43. Quadratic ramp generator controlled by V_S pulse

However, the V_S signal is a 10% pulse of switching period, the generated ramp signal $V_{quadratic\_ramp}$ ramps up with 10% duty, too. The integrated region of the charging current I_{ramp} showed in Fig. 44 generates the $V_{slope\_comp}(DT_S)$ signal in equation (65).

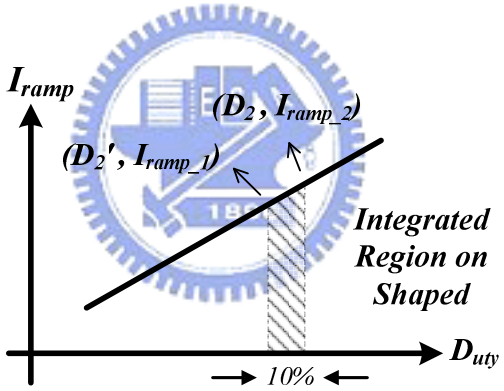


Fig. 44. The I_{ramp} current is charging into the capacitor with 10% duty

$$V_{slope\_comp}(DT_S) = \frac{2D \cdot (V_H - V_L) - 0.1 \times V_H + V_L}{18 \cdot C \cdot f_S \cdot R_X} \tag{65}$$

The $V_{slope\_comp}(DT_S)$ signal is a linear equation with the duty cycle D.

Chapter 4

Circuit Implementations and Simulations

4.1 DC/DC Buck Converter with PWM/PFM Mode

There are two modes operated in this paper. One is Pulse-Width Modulation (PWM) mode and the other is Pulse-Frequency Modulation (PFM) mode. The different operation modes provide distinct properties and performances. In heavy loading, the converter operates in PWM mode to provide large current (energy) to output node. The PWM mode has high efficiency in heavy loadings but suffers from in light condition. In order to maintain a high efficiency and extend the battery lifetime, the second mode is presented to operate in low current requirement system. As a result, this paper operates in either PWM mode or PFM mode.

The PWM/PFM selection circuit detected the load current information to change modes appropriately. The operation of selection circuit is presented and its simulation results plotted below.

4.2 Current Mode Buck Converter with PWM Mode

The architecture of DC/DC current mode buck converter in PWM mode is illustrated in Fig. 45. The operation is descried as follows. In the first interval of switching period called as duty cycle, the inductor current is sensed by the current sensing circuit that is expressed an equivalent resistor R_S. The output voltage of system is scaled down with a divider and subtracted from a reference voltage. The error signal is amplified by the error amplifier. The sensed current is adding to the compensation ramp ($V_{quadratic\_ramp}$) with voltage adder and compared with the signal (V_C). As the sum of those two signals exceeds the V_C voltage, the duty ratio is defined in each switching period. The duty cycle is separated into two signals in non-overlapping circuit to drive the power PMOS and NMOS, respectively. In addition, when the reverse inductor current (light loading) appears, the zero current detector turns off the power NMOS immediately to eliminate the reverse inductor current and improve the power conversion efficiency.

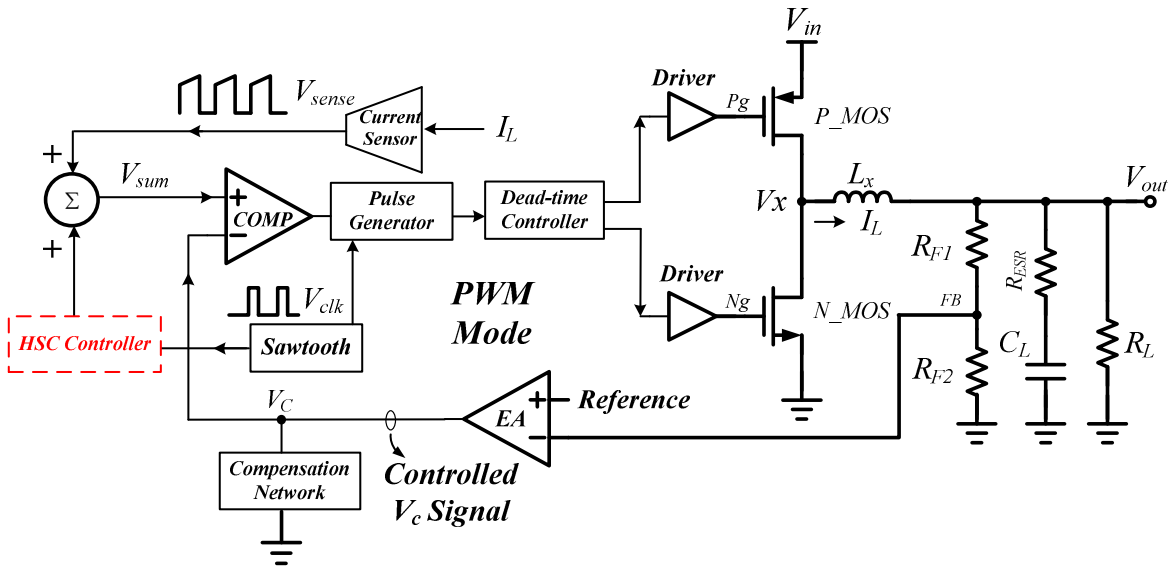


Fig. 45. The architecture of current mode buck converter with PWM controller

The electrical characteristics are listed in Table 4. The following sub-sections are the implementation and the simulation results of the circuits.

Table 4. The electrical characteristics.

Supply Range (V_{in})	2.7V-5.5V
Output voltage (V_{out})	1.8V
Output current (I_{LOAD})	100mA-1000mA
Switching frequency (F_S)	1MHz
Output inductor (L_X)	2.7uH
Output capacitor (C_L)	10uF
Output capacitor series resistance (R_{ESR})	200mΩ

4.2.1 Bandgap Reference

The power management system requires a fixed reference voltage regardless of process, input voltage and temperature variations. Hence, the bandgap reference is a significant circuit in the switching regulators. As illustrated in Fig. 46, the principle of the bandgap reference is the summation of positive temperature coefficient (*PTC*) and negative temperature coefficient (*NTC*) to eliminate the slope difference of each other. The detailed operation of bandgap reference is the voltage difference of base-emitter on BJT that is negative temperature coefficient adding to the voltage that is proportional to absolute temperature (PTAT). Therefore, we can modify the parameter *K* suitably to make sure the voltage reference is irrespective of temperature variation [24][25][26].

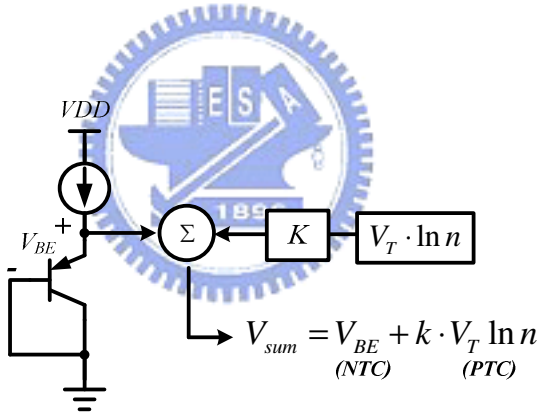


Fig. 46. The principle of bandgap reference

The architecture of bandgap reference is illustrated in Fig. 47 that consists of *Start-up Circuit*, I_{PTAT} *Bias Circuit* and, the *Operational Amplifier*. The I_{PTAT} *bias circuit* provides the biasing current to M_1 which is proportional to the absolute temperature. The structure of M_{B7}-M_{B10} makes the source voltage of M_{B9} and M_{B10} are equivalent. The voltage difference of Q_2 and Q_3 is across the resistor R_d and the current is showed in equation (66).

$$I_{M_{B7}} = \frac{V_{EB3} - V_{EB2}}{R_d} \tag{66}$$

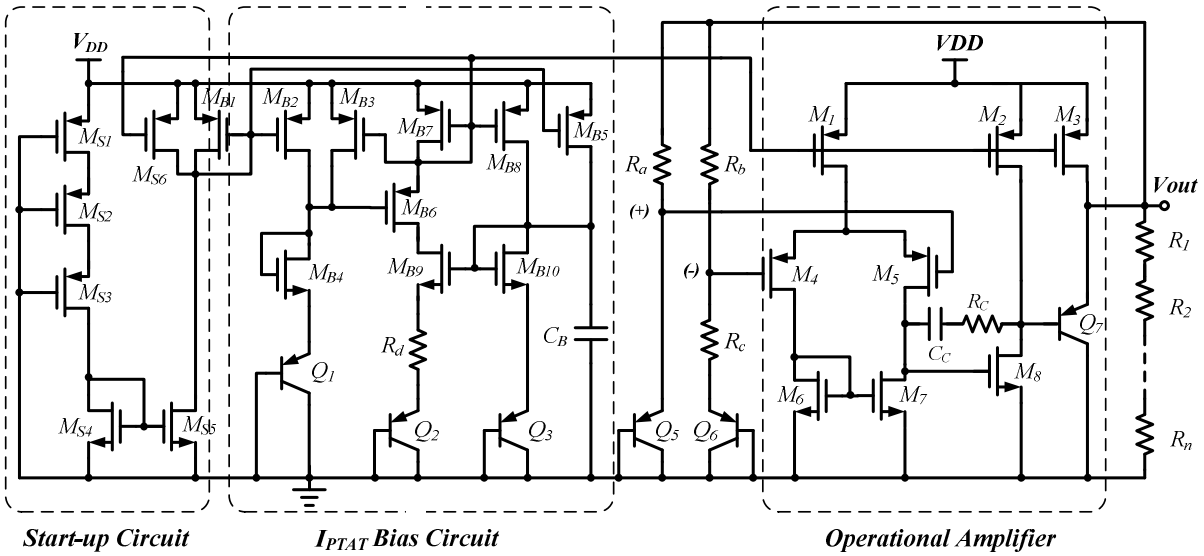


Fig. 47. The conceptual block diagram of bandgap voltage reference

The *start-up circuit* provides the initial condition for the bias circuit because of the I_{PATA} *bias circuit* had two stable operation regions: one is normal state and the other is zero state. The operational amplifier makes the gate voltage of M_4 and M_5 are equivalent. The current on the resistor R_c is showed in equation (67). As a result, the reference voltage of the bandgap circuit expressed in equation (68).

$$I_{R_C} = \frac{V_{EB5} - V_{EB6}}{R_c} = \frac{V_T \ln n}{R_c} \tag{67}$$

$$V_{out} = V_{REF} = V_{EB6} + \frac{R_b + R_c}{R_c} \cdot V_T \ln n = V_{EB6} + k \cdot V_T \ln n \tag{68}$$

The reference voltage is the summation of *PTC* and *NTC*. We can change the parameter *K* to eliminate the slope of temperature coefficient. Finally, the output voltage of bandgap reference is independent of temperature variation. The simulation results with different supply voltages, temperatures, and process variations are illustrated in Fig. 48. The summary of performance is given in Table 5.

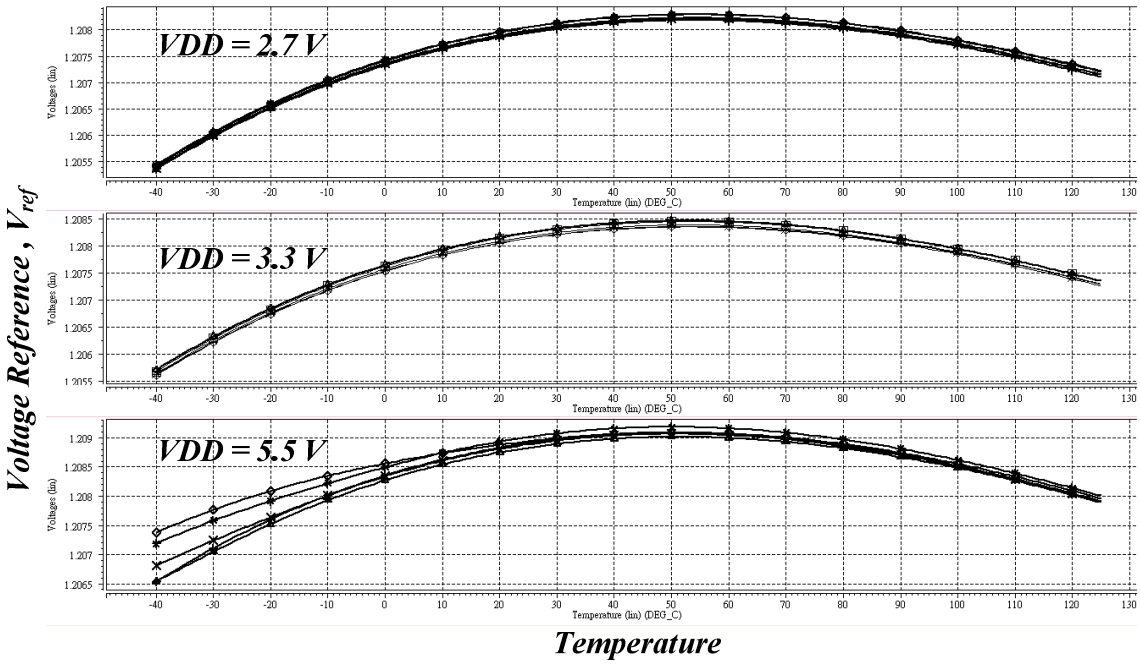


Fig. 48. The simulation waveforms of the bandgap reference with temperature variation

The typical reference voltage is 1.2V and the TC is 13ppm/^{0}C.

Table 5. The simulation results of the bandgap voltage reference circuit.

Specifications	Values
Supply Voltage (V_{IN})	2.7V~5.5V
Temperature	-40℃~125℃
Variation (V_{REF1})	13ppm/℃

4.2.2 Comparator

The schematic of comparator with hysteresis window is shown in Fig. 49 that consists of *Bias Stage*, *Hysteretic Comparator* and the *Buffer*. The transistors M_{B1}-M_{B3} made the biasing current to bias the comparator.

The input differential pair, transistor M_1 and M_2, establish the positive feedback loop with transistors M_4-M_7. This positive feedback loop provides a high gain and hysteresis window. The transistors M_{X1}-M_{X2} are used to a buffer stage providing a rail-to-rail swing [27].

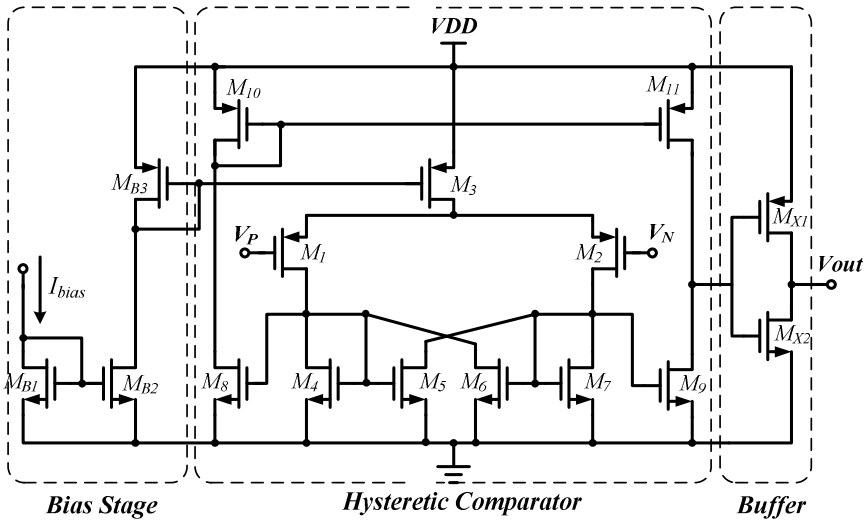


Fig. 49. The schematic of comparator without hysteresis window

4.2.3 Operational Amplifier

The operational amplifier is illustrated in Fig. 49 that constructs by *Biasing Circuit* and *Folded-Cascode OP*. The differential pair of folded-cascode amplifier used P channel for operating at low dc bias requirements.

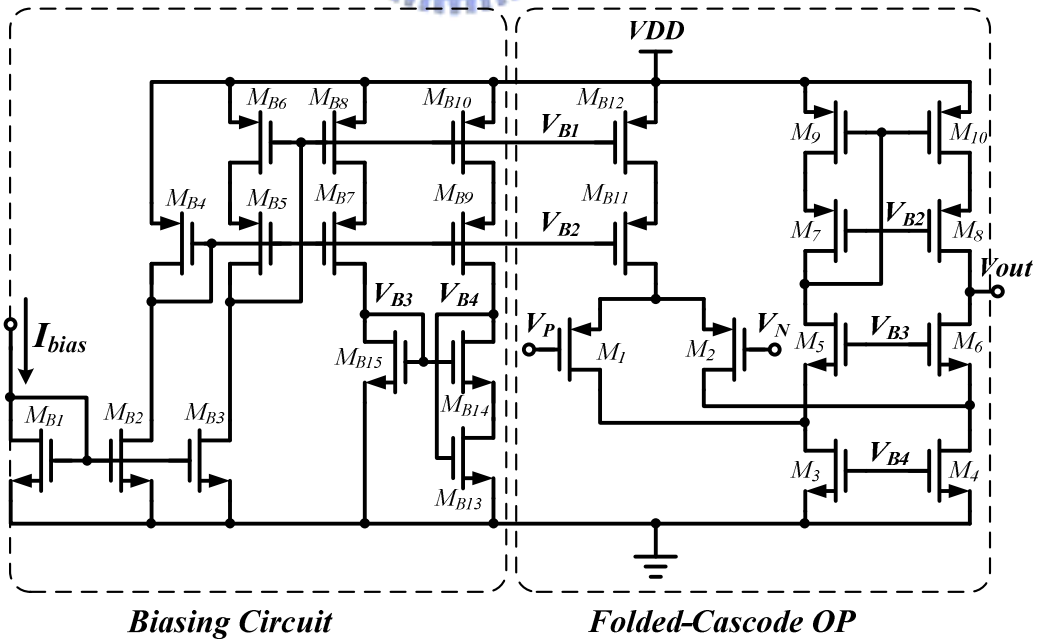


Fig. 50. The schematic of folded-cascode operational amplifier with PMOS input

The transistors M_{B1}-M_{B15} introduce the biasing current to bias the folded-cascode amplifier and the transistors M_1-M_{10} of amplifier provide a high dc gain to enhance system performance. As illustrated in Fig. 51, the structure of two-stage amplifies with miller capacitor used to many circuits such as *V-to-I circuit* that introduced below. We use the components L_Z, C_Z and V_Z to construct a close loop to analysis the system stability. The simulation waveforms of frequency domain are showed in Fig. 52. The magnitude of dc gain and the phase margin equals 80db and 65°, respectively. As shown, the system is stable.

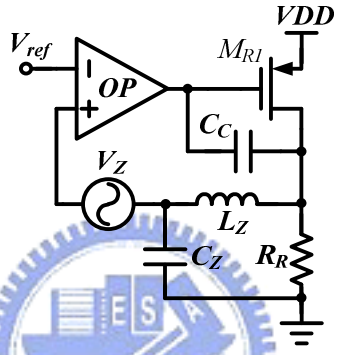


Fig. 51. The architecture of the loop gain analysis

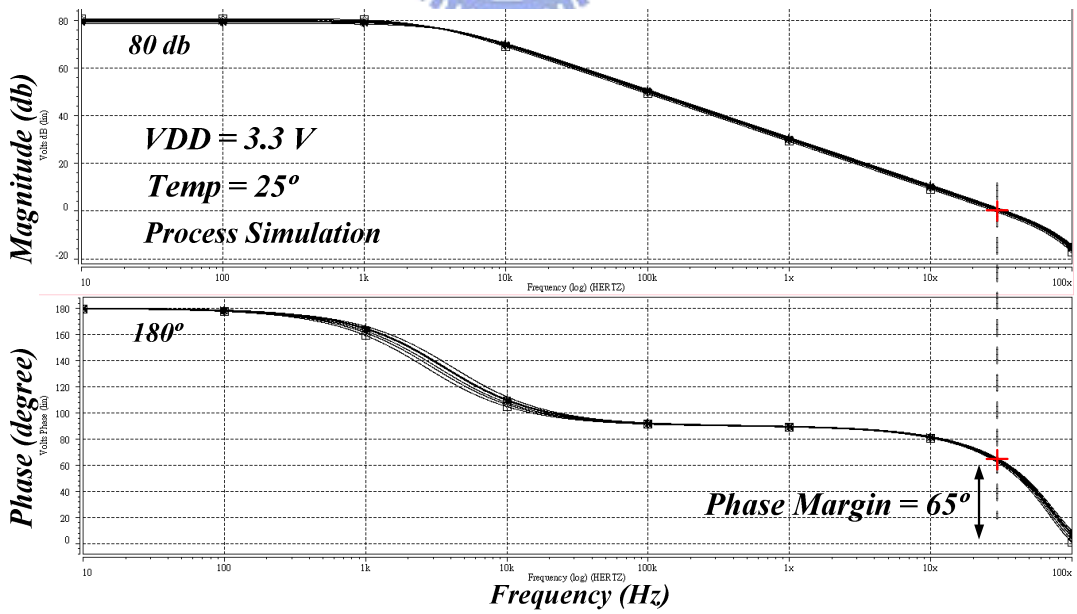


Fig. 52. Stability simulation result of the close loop analysis

4.2.4 Error Amplifier

In current mode buck converters, we usually required a high gain amplifier applied to compensation network to provide a sufficient phase margin for system stability. The folded-cascode transconductance operational amplifier showed in Fig. 53 that used to amplify the error signal between feedback voltage and the reference voltage. The transistors M_{B1}-M_{B15} produce the biasing current to bias the amplifier.

The transistors M_1 and M_2 form the input differential pair with P channel device. The simulation waveforms with capacitor loading in frequency domain are illustrated in Fig. 54. The magnitude of dc gain equals to 76db and the phase margin equals to 65°.

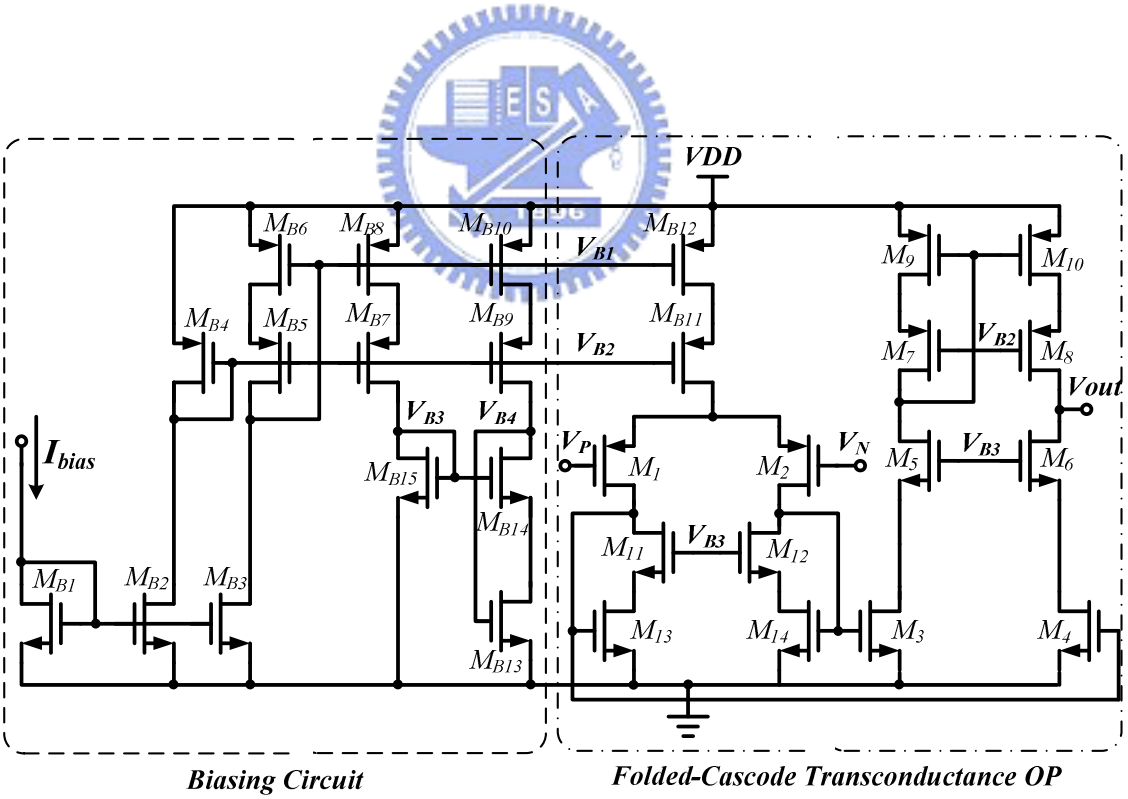


Fig. 53. The schematic of the folded-cascode transconductance operational amplifier

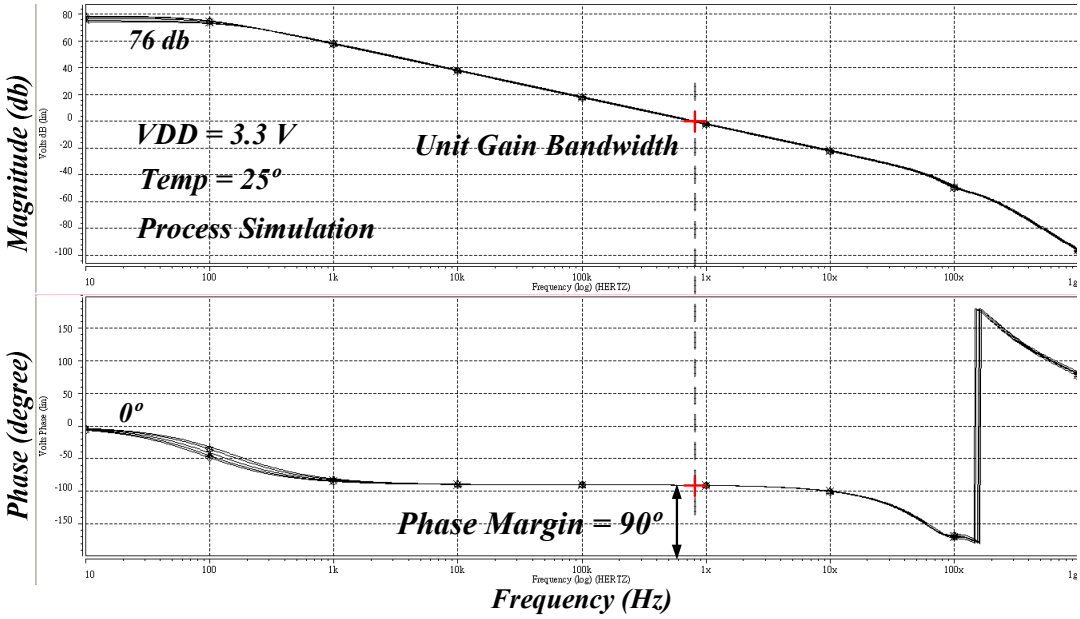


Fig. 54. Frequency analysis of the error amplifier

4.2.5 Frequency Compensation Network

The frequency domain analysis is illustrated in Fig. 55. The red, blue, green and purple lines represent the system, compensator, modulator and the feedback divider, respectively.

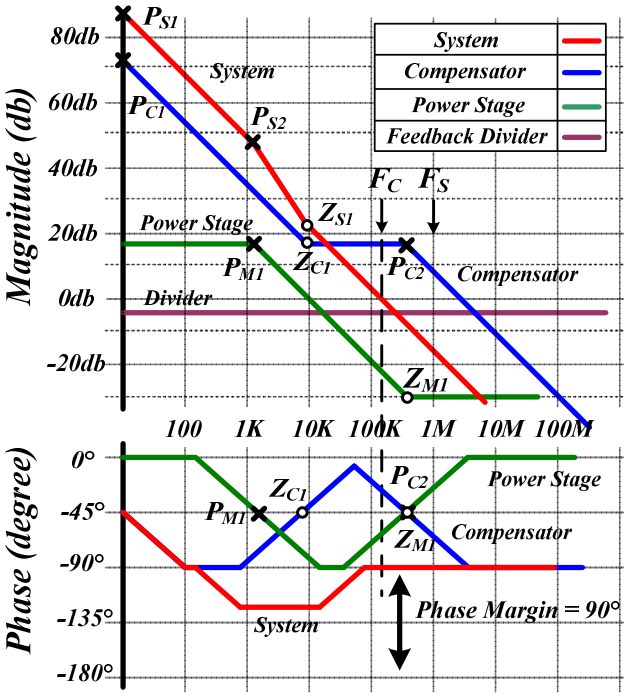


Fig. 55. Frequency response of the current mode buck converter

As the figure shown, the modulator had a dominate pole P_{M1} and an ESR zero Z_{M1} that were generated by the output capacitor and its equivalent resistor. In order to provide a sufficient phase margin and keep the system stable, the compensator had to eliminate the dominate pole P_{M1} of modulator. Therefore, the proposed compensation network had two poles and one zero expressed as P_{C1}, P_{C2} and Z_{C1}. The use of pole-zero cancellation technique is the compensation method. We eliminate the pole P_{M1} and zero Z_{M1} of modulator in compensation zero Z_{C1} and pole P_{C2}, respectively. Mostly, we design the unit gain frequency (UGF) of the system is ten times smaller than the switching frequency (F_S). The compensated system formed a signal pole structure before the unit gain frequency [28]. Hence, the system had sufficiency phase margin and an excellent performance. The compensation network is showed in Fig. 56 that consists of operational transconductance amplifier (*OTA*), resistor R_{C1} and the capacitor C_{C1}, C_{C2}. The parameters are listed in Table 6.

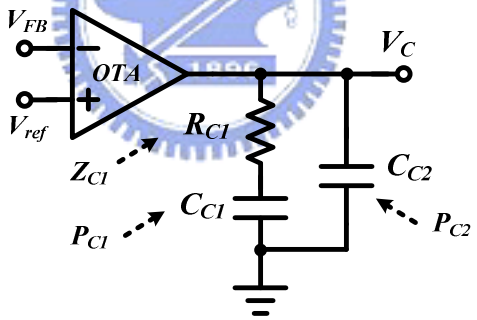


Fig. 56. The scheme of the compensation network

Table 6. The compensation parameters of the compensated network.

Parameter	Value
Switching Frequency (F_S)	1Mhz
Equivalent Current Sensing Resistor (R_S)	1Ω
Output Capacitor (C_O)	10uF
Output Capacitor Series Resistance (R_E)	200mΩ
First Compensation Capacitor (C_{C1})	120pf
Second Compensation Capacitor (C_{C2})	1.5pf
Compensation Resistor (R_{C1})	100kΩ

According to the above discussion, the frequency response of the compensator is shown in Fig. 57 that provides a dc gain 75db and phase margin larger than 90°.

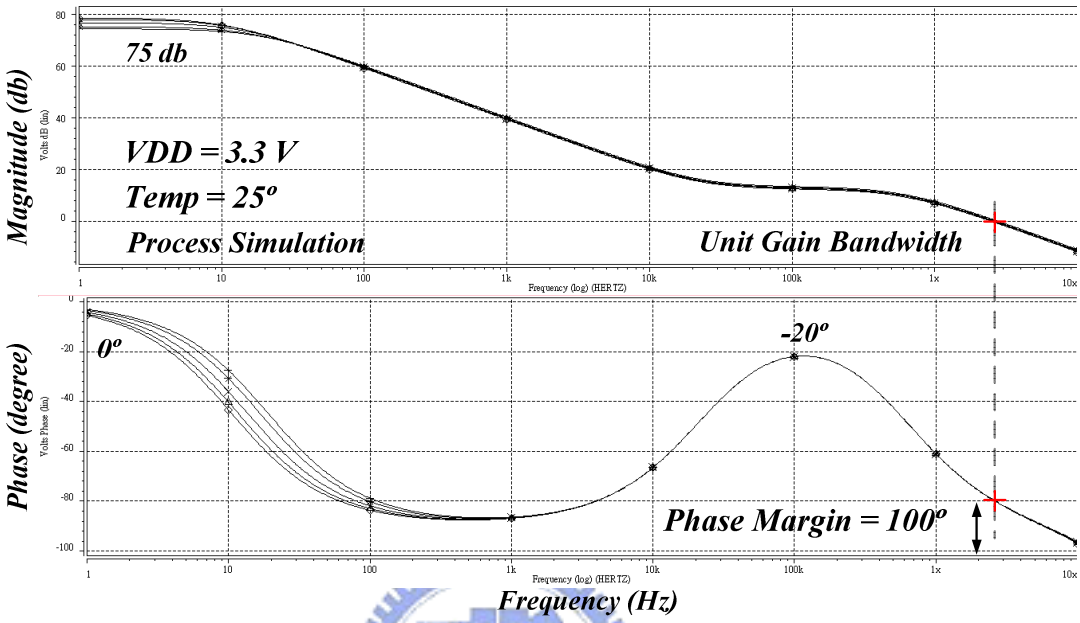


Fig. 57. Frequency domain analysis of compensation network

4.2.6 Current Sensing Circuit

In current mode converters, the use of current sensing circuit is necessary. There are many current sensing techniques such as using a sensing resistor in series with power device or an integrated sensing circuit. This paper proposed an integrated sensing circuit used to sense the inductor current to transform a voltage signal. A high efficiency, high accurate and small size circuit of current sensing is the engineers concerned. The current sensing circuit is illustrated in Fig. 58.

As the system operates in the first interval of switching period, the power PMOS is turned on and the power NMOS is turned off. The *PG* signal is logic low that turns on the transistor M_{SW}. Hence, the node V_B can be approximately equal to the node V_X. An operational amplifier with NMOS differential input forces the voltage V_A and V_B to be equivalent through

the negative feedback loop. The source-gate and source-drain voltage of both transistors of *Power PMOS* and M_{P1} are the same [29]-[33]. Therefore, the sensed current I_S is reverse proportional to the aspect ratio of *Power PMOS* and M_{P1} and expressed in equation (69).

$$I_S = \frac{(W/L)_{M_{P1}}}{(W/L)_{Power\_PMOS}} \cdot I_L = \frac{1}{K} \cdot I_L \tag{69}$$

Finally, the sensed current I_S flows into the resistor R_{sense} to produce the voltage signal V_{sense}.

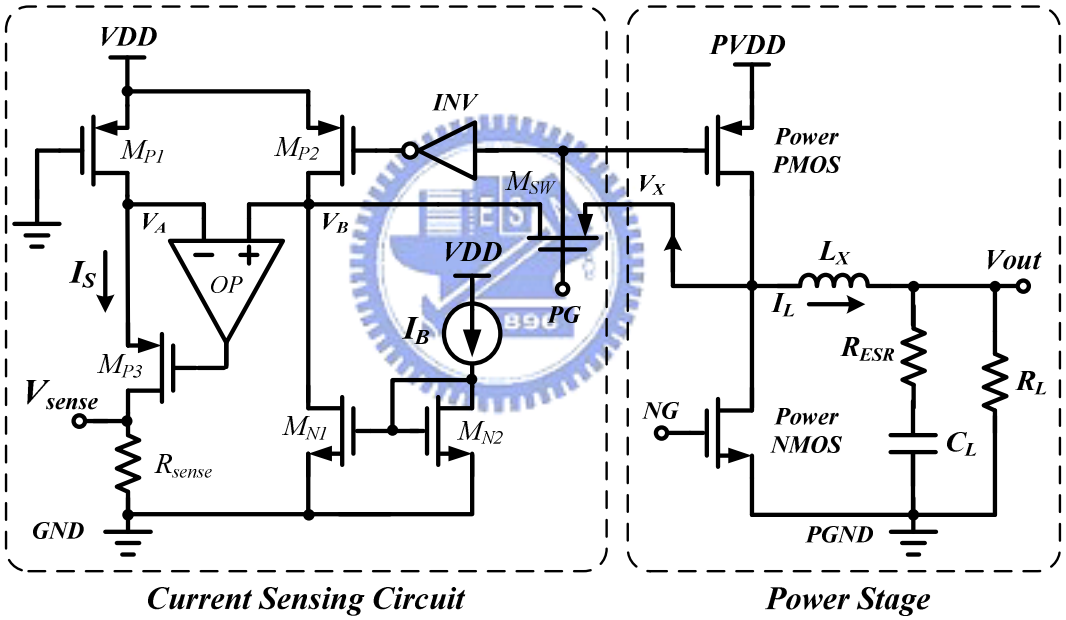


Fig. 58. The schematic of the integrated sensing circuit with power stage

Oppositely, the system operates in the second interval of switching period, the power PMOS is turned off and the power NMOS is turned on. The current sensing circuit stops to sense inductor current and the operational amplifier forces I_S as the same as the biasing current I_B. The simulation waveform is showed in Fig. 59. The current sensing circuit could be presented as an equivalent resistor that mentioned before. In this paper, we assume the equivalent resistor of current sensing circuit to equal 1Ω for simplification.

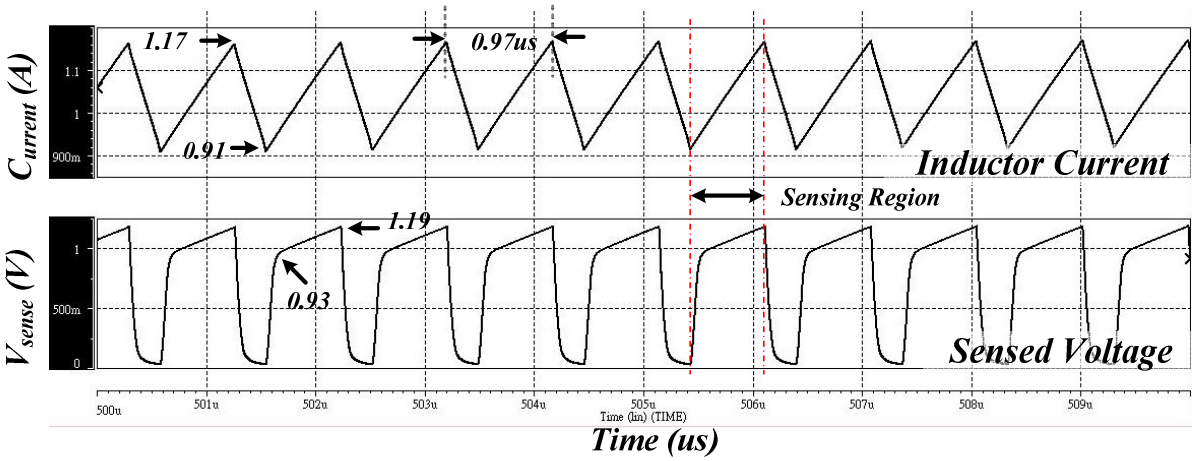


Fig. 59. Simulation for the current sensing circuit

In the figure shown, the sensed voltage is from 0.93V to 1.19V corresponding to the inductor current ripple from 0.91A to 1.17A. According to the waveforms, the circuit has high accuracy and the ratio between sensed voltage and inductor current equals to one.

4.2.7 Clock and Sawtooth Generator

The clock and sawtooth generator is the core circuit of the current mode converters. The operation principle of the clock and sawtooth generator is a constant current charging and discharging the capacitor periodically. The schematic of clock and sawtooth generator is showed in Fig. 60. At the beginning of the period, a constant current I_C is introduced by the transistor M_{R2} and flows into the capacitor C_R. The capacitor voltage is called as V_{ramp} and the constant current I_C is given by:

$$I_C = \frac{V_{ref}}{R_R} \tag{70}$$

Continuously, the capacitor voltage V_{ramp} reaches the V_L signal ($V_H > V_L$ produced by the bandgap reference), the current I_C is charging yet because of the clock signal is logic low. The V_{ramp} voltage is increasing with constant slope in this state. Oppositely, the V_{ramp} signal

reaches the V_H voltage, the *SR-Latch* goes from low to high that results the transistor M_{R4} to turn on. The energy stored in the capacitor is discharged at the second period, the V_{ramp} signal descended immediately. As the V_{ramp} signal decreased to the V_L voltage, the *SR-Latch* goes from high to low and closes the transistor M_{R4} again. The V_{ramp} signal goes up and down between the both voltage V_H and V_L.

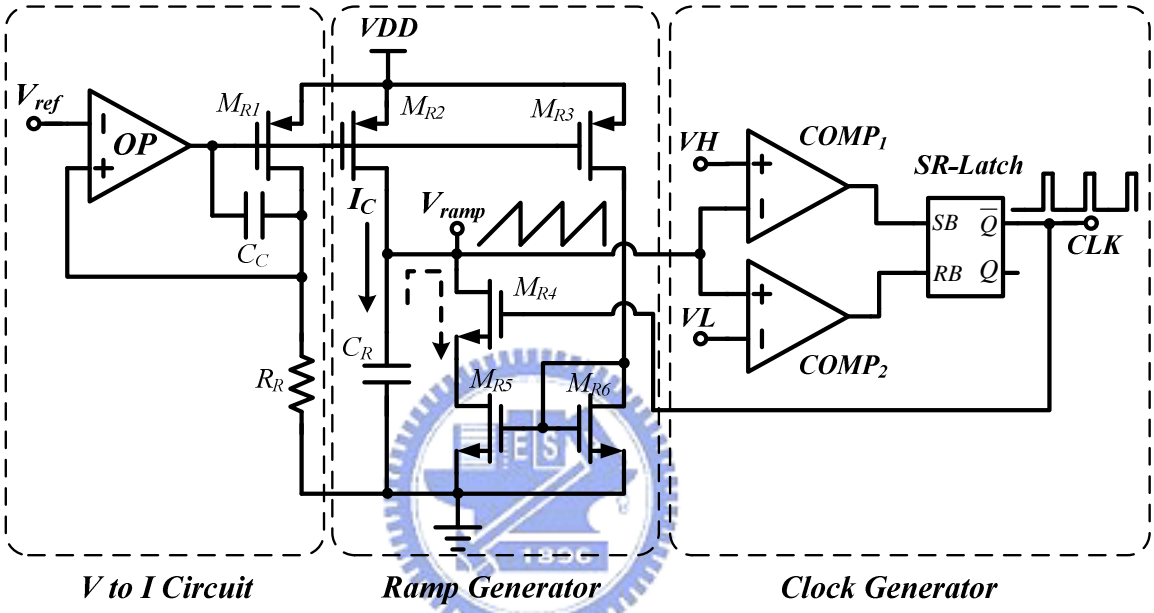


Fig. 60. Clock and sawtooth generator

We let the V_H and V_L voltage to equal 1.0V and 0.8V, respectively. The slope m_1 of the V_{ramp} voltage in the first period is expressed in equation (71). Generally, the design issue of the V_{ramp} signal is 90% to ramp up and 10% to ramp down. According to the equation, we can vary the parameters of the charging current I_C and the capacitor value C_R to meet the required voltage slope.

$$m_1 = \frac{V_H - V_L}{90\% \cdot T_S} = \frac{I_C}{C_R} \tag{71}$$

The simulation results are illustrated in Fig. 61, the peak value of the V_{ramp} voltage is 0.73V and 1.07V.

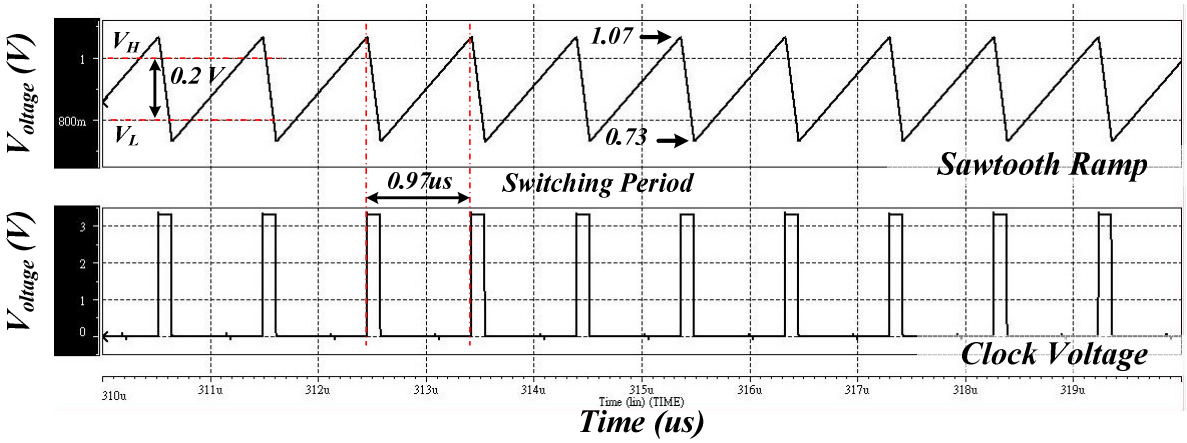


Fig. 61. The simulation result of the clock and sawtooth generator

4.2.8 Percent Duty and Quadratic Ramp Generator

This paper proposed a 10% control pulse that generates a quadratic ramp signal as described before. The percent duty and quadratic ramp generator is illustrated in Fig. 62. This circuit consists of *Percent Duty Circuit* and *Quadratic Ramp Generator*. The percent duty circuit generates the pulse signal V_S to the next stage of quadratic ramp generator. The pulse ratio is determined by the current ratio of $I_1$and I_2. The V_S pulse is introduced before the end of *PWM_PG* signal that is the control voltage of the power PMOS.

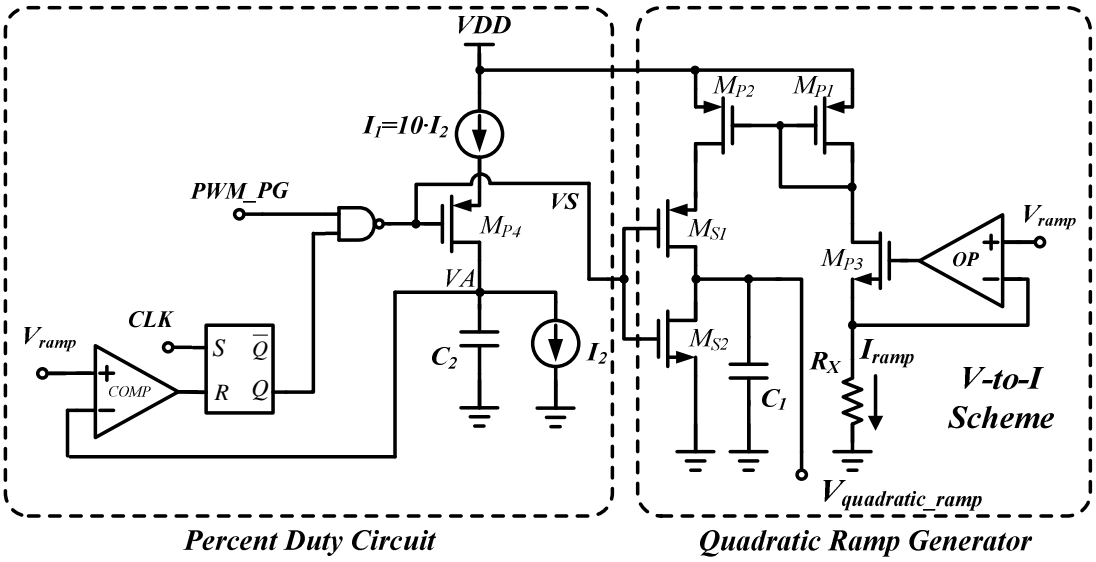


Fig. 62. The schematic of percent duty and quadratic ramp generator

The I_{ramp} current is generated by the *V-to-I* circuit connecting to the V_{ramp} voltage. The I_{ramp} current is mirrored by the transistors M_{P1} and M_{P2} and flows into the capacitor C_1 to produce the voltage signal $V_{quadratic\_ramp}$. Thus, the $V_{quadratic\_ramp}$ signal is used to the compensation ramp in slope compensation techniques. As the Fig. 63 shown, the $V_{quadratic\_ramp}$ signal is generated by the 10% control pulse and the sawtooth ramp. In different duty cycle, the quadratic ramp has different peak value. At this situation, the peak value is 0.83V.

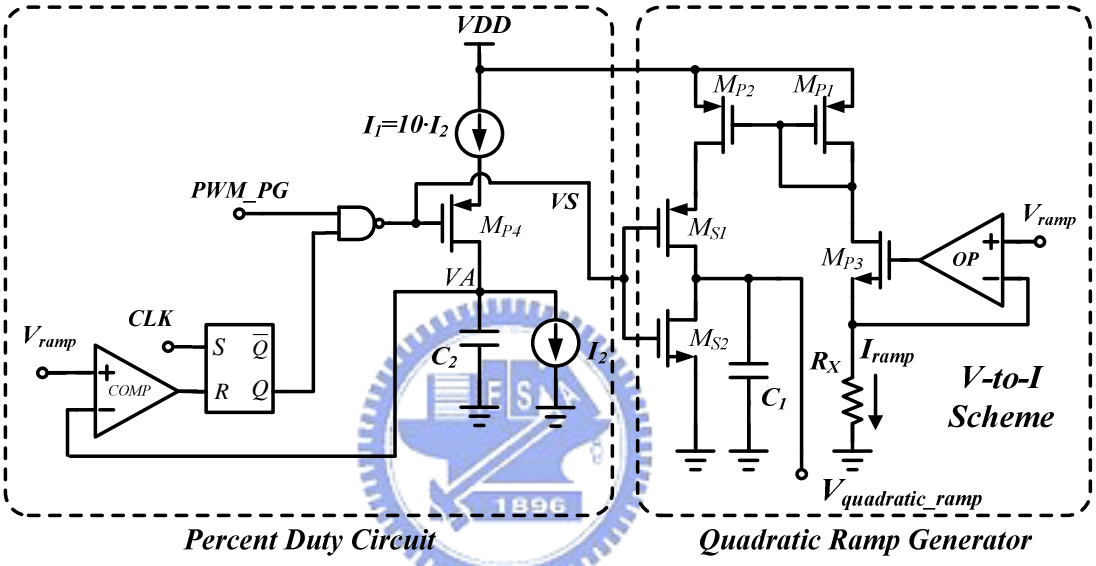


Fig. 63. The simulation waveforms of quadratic ramp and 10% control pulse

4.2.9 Voltage Adder

The function of the voltage adder is the combination of compensation ramp and current sensing voltage to suppress the sub-harmonic oscillations. The voltage adder is composed of two *V-to-I circuits* showed in Fig. 64. The voltage-to-current circuits transform their input voltage V_1 and V_2 into current information and mirrored into resistor R_{sum} to produce the V_{sum} voltage simultaneously [34]. The design issue of the V_{sum} signal is setting the voltage level in the range of output swing of the operational transconductance amplifier. The simulation results and performances are shown in Fig. 65.

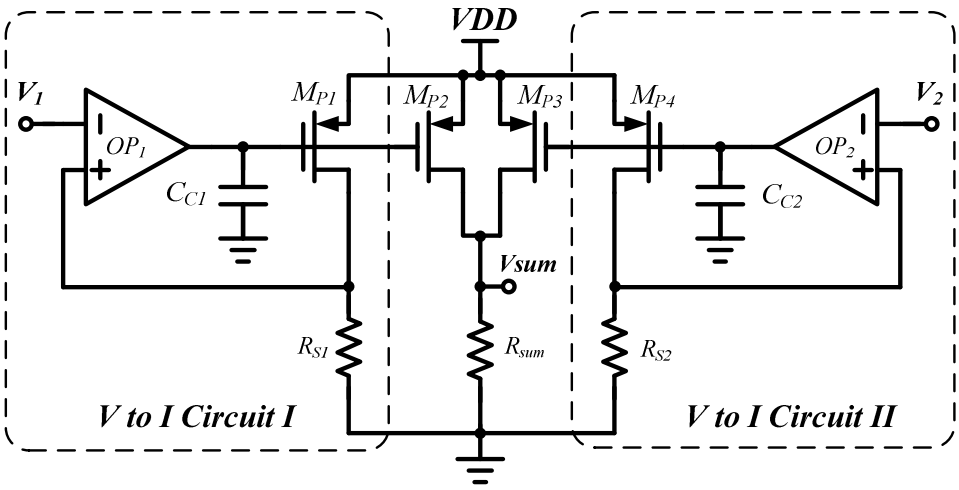


Fig. 64. The schematic of the voltage adder

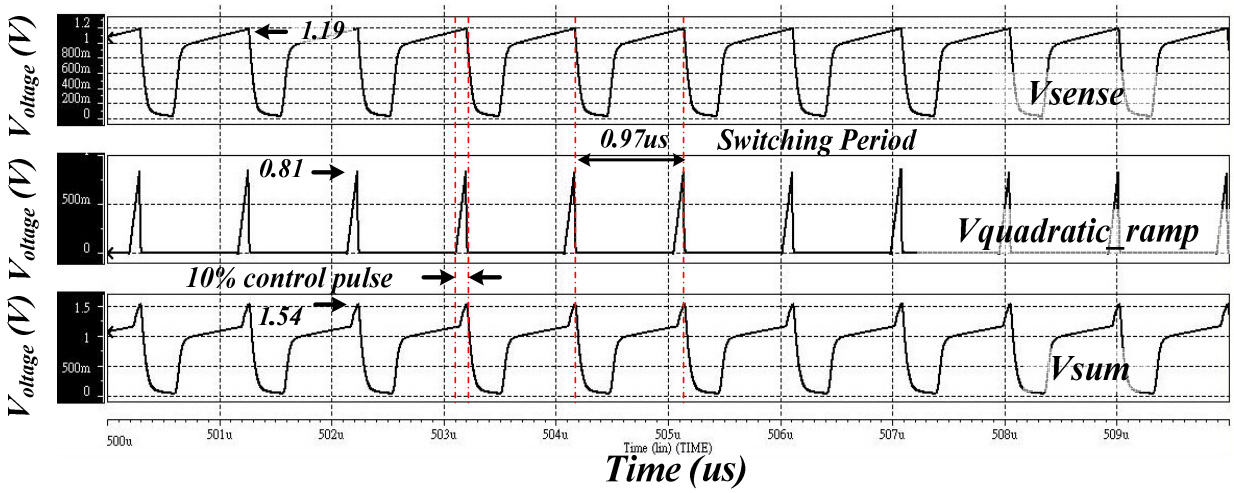


Fig. 65. The simulation waveforms of the voltage adder

4.2.10 Zero Current Detector

In synchronous converters, the zero-current detector is used to prevent the occurrence of reversed current when the average current is less than the ripple current. The reversed inductor current contributes extra conduction losses; however it does not contribute the energy to the output node. Hence, the efficiency will be reduced seriously in this state. The zero-current detector could improve the efficiency in light loadings.

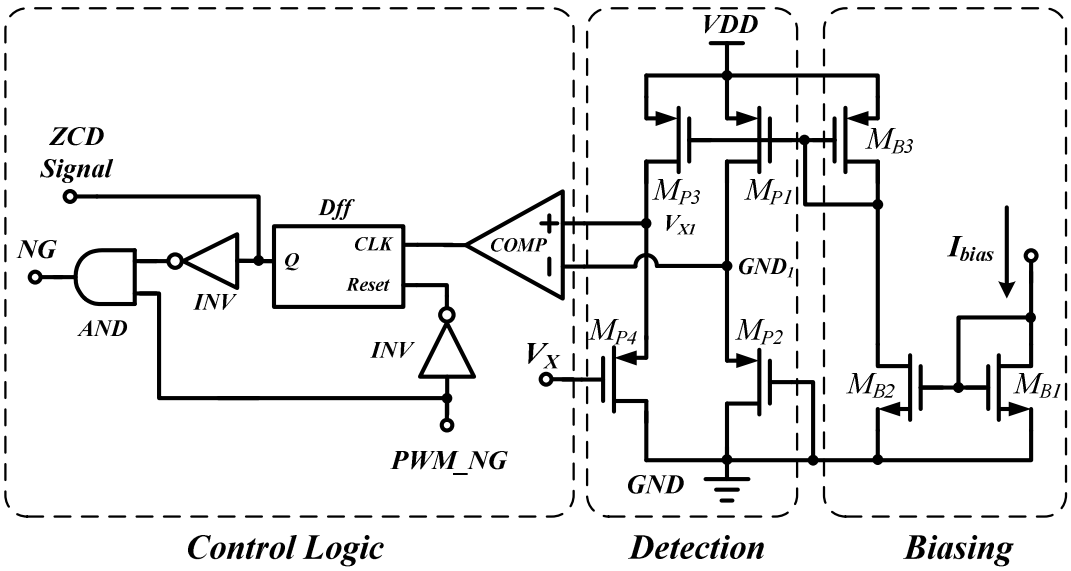


Fig. 66. The schematic of the zero-current detector

The schematic of the zero-current detector is illustrated in Fig. 66. The transistors M_{B1}-M_{B3} produce the biasing current to bias the zero-current detection circuit. The transistors M_{P1}-M_{P2} and M_{P3}-M_{P4} construct the level shifters to shift the signals V_X and ground (*GND*) to the V_{X1} and GND_1 for locating in the input range of the comparator, respectively. In the first interval of switching period, the *PWM_NG* is logic low that maintains the *NG* signal is logic low and resets the D-flip-flop (*Dff*) to make the voltage *ZCD Signal* is low, too. In the second interval of switching period, the *PWM_NG* is logic high to turn on the power NMOS owing to the output voltage of D-flip-flop is still low. However, as the reserve current is occurred, the node V_X is grater than the ground voltage corresponding to the voltage V_{X1} is grater than GND_1. At the same time, the output of the comparator (*COMP*) is from low to high to trigger the D-flip-flop that results the voltage of *ZCD Signal* in high logic level [35]. Simultaneously, the signal *NG* is from high to low to tune off the power NMOS early that prevents from the occurrence of the reverse current. The simulation waveforms are illustrated in Fig. 67.

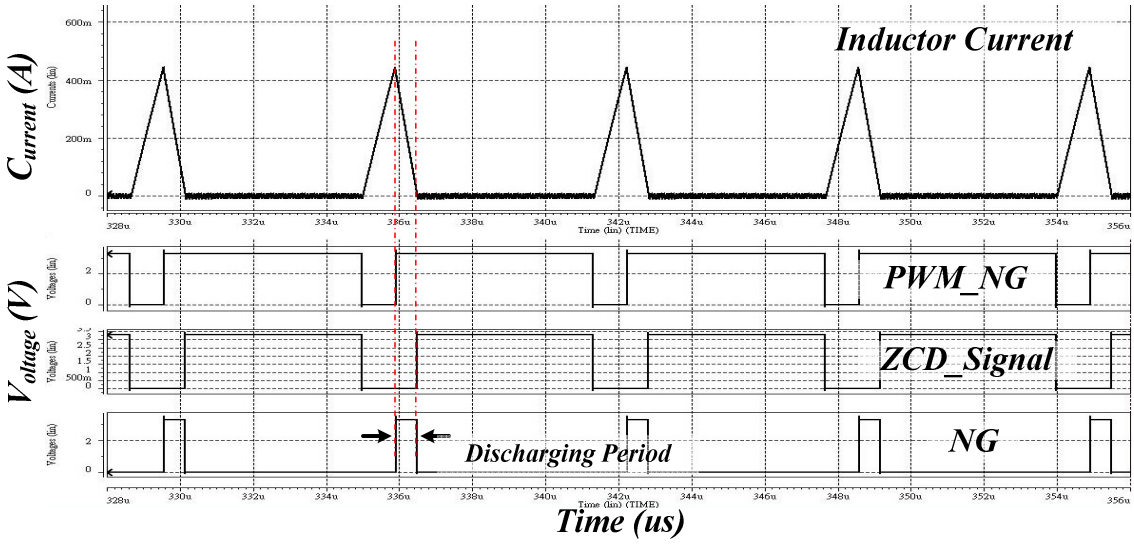


Fig. 67. Simulation waveforms of the zero current detector

4.2.11 Pulse-Width Generator

The pulse-width generator is shown in Fig. 68. The logic inverters and *NOR* gate ensure that both inputs of *SR-Latch* are not low level at the same time. In the beginning of switching period, the *CLK* signal is high to set the output voltage (*PWM Signal*) of *SR-Latch* low level and turns on the power PMOS. Oppositely, as the *Reset* signal is occurred from low to high, the *PWM Signal* of *SR-Latch* is turned to high to turn off the power PMOS immediately.

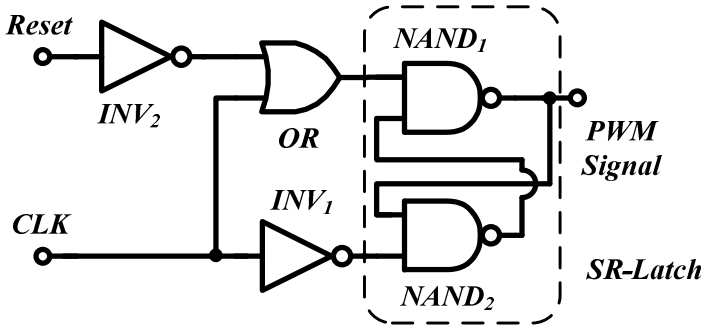


Fig. 68. The schematic of the pulse-width generator

4.2.12 Non-overlapping Circuit

Non-overlapping circuit also called as dead-time control circuit is illustrated in Fig. 69. The function of this circuit is preventing from the power PMOS and NMOS to turn on simultaneously. If both power MOS turned on simultaneously, the large shoot-through current will be generated that caused the power devices to be destroyed [36][37]. Hence, the non-overlapping circuit is used to separate the both signal with a small clearance called as dead-time. The operation principle is that; as the *PWM Signal* is high, the *PG* signal is low to turn on the *Power PMOS* simultaneously. Oppositely, as the *PWM Signal* is low, the *PG* signal is high to turn off the *Power PMOS* simultaneously. But the *NG* signal with a delay second is high to turn on the *Power NMOS*. The simulation waveforms are showed in Fig. 70.

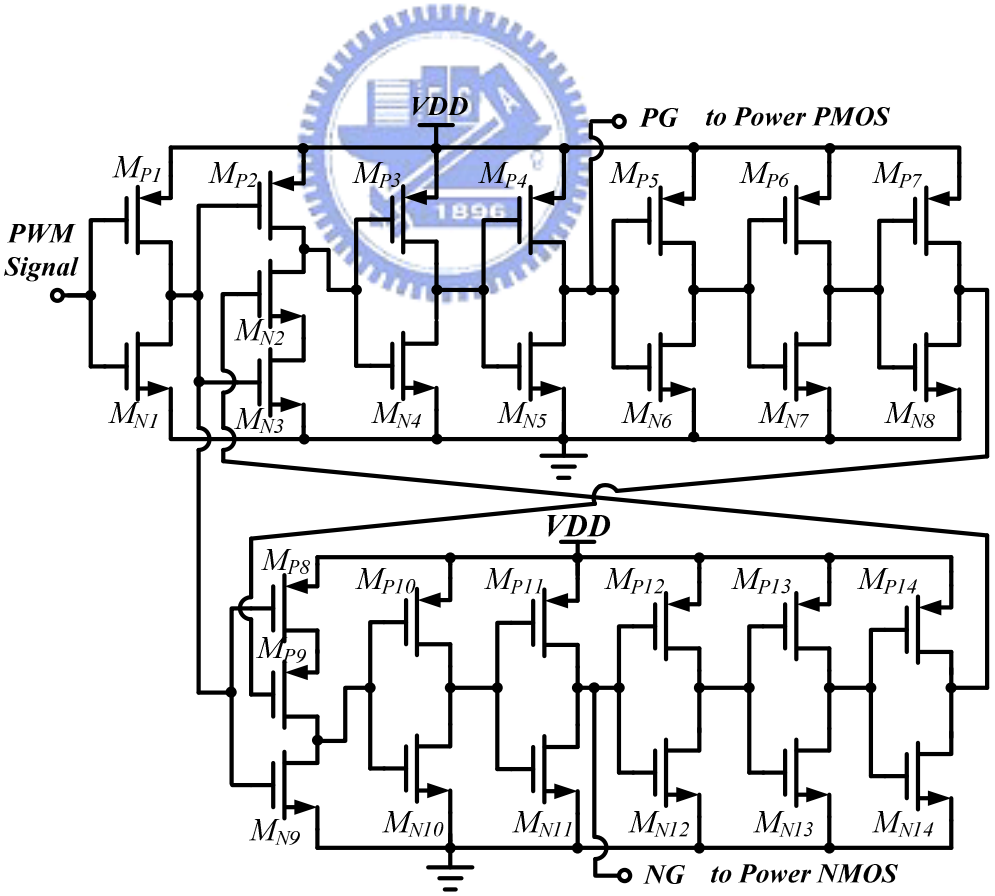


Fig. 69. The schematic of the non-overlapping circuit

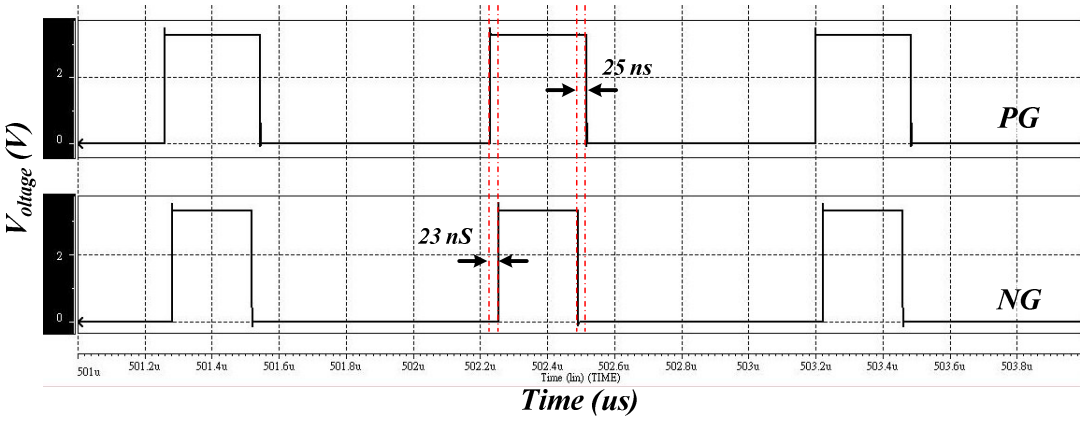


Fig. 70. Simulation waveform of the non-overlapping circuit

4.3 Current Mode Buck Converter with PFM Mode

4.3.1 Architecture of PFM Mode Controller

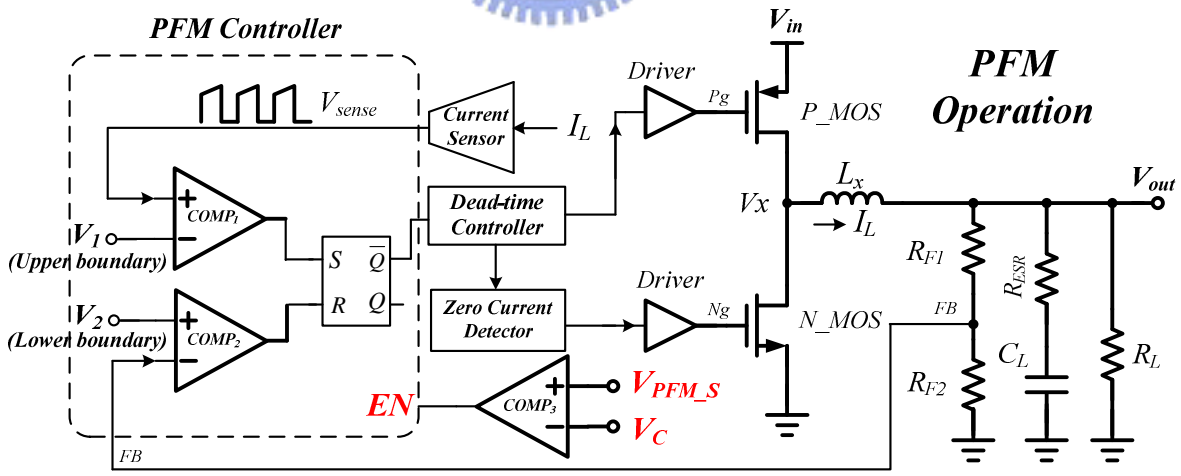


Fig. 71. The architecture of current mode buck converter with PFM controller

The PFM controller is illustrated in Fig. 71 that consists of two comparators ($COMP_1$, $COMP_2$) and a *SR-Latch*. The architecture is also called as peak-current control that limits the peak current of inductor. The function is that: as the feedback voltage (*FB*) is lower than V_2,

the *SR-Latch* turns on the power PMOS to charging the output node until the V_{sense} signal exceeds the V_1 voltage. As the V_{sense} signal exceeds the V_1 voltage, the *SR-Latch* turns off the power PMOS and turns on the power NMOS to discharging the output node. The system operates between voltage V_1 and V_2 periodically. Hence, the switching frequency of the system is proportional and dependent on the output loading requirements.

The system also contains an enable circuit that turns on/off the PFM controller. As the V_C signal is lower than the V_{PFM_S} voltage, the comparator $COMP_3$ turns on to enable the PFM controller. As a result, the mode-transition opportunity between PWM and PFM modes is adaptively dependent on the V_{PFM_S} voltage that we can change the V_{PFM_S} voltage as a rule. As the mode-transition is appropriately, the system has the best efficiency from PWM mode to PFM mode.

4.3.2 Current Fitting Curve Generator

According to the above descriptions that: if the mode-transition is appropriately, the system has the best efficiency from PWM mode to PFM mode. Hence, we propose the circuit – *Current Fitting Curve Generator* that is used to change the V_{PFM_S} voltage reverse proportional to the supply voltage. The relationships between V_{PFM_S} voltage and system efficiency will be explained in next chapter. The results will accompany the efficiency plots of PWM/PFM modes.

This circuit is illustrated in Fig. 72. The output voltage is scaled down by a voltage divider to the negative node of the *V-to-I Scheme*. The current on resistor R_a is mirrored to I_1 and is proportional to the supply voltage. We set the biasing current I_{B1} to subtract the mirrored current I_1 and got the current I_2 that is reverse proportional to the supply voltage. The equation (72) shows that the current I_2 flows into the resistor R_b, the generated voltage V_{PFM_S} is reverse proportional to the supply voltage, too.

$$I_2 = I_{B1} - I_1 = I_{B1} - \frac{V_{DD}}{3 \cdot R_a} \tag{72}$$

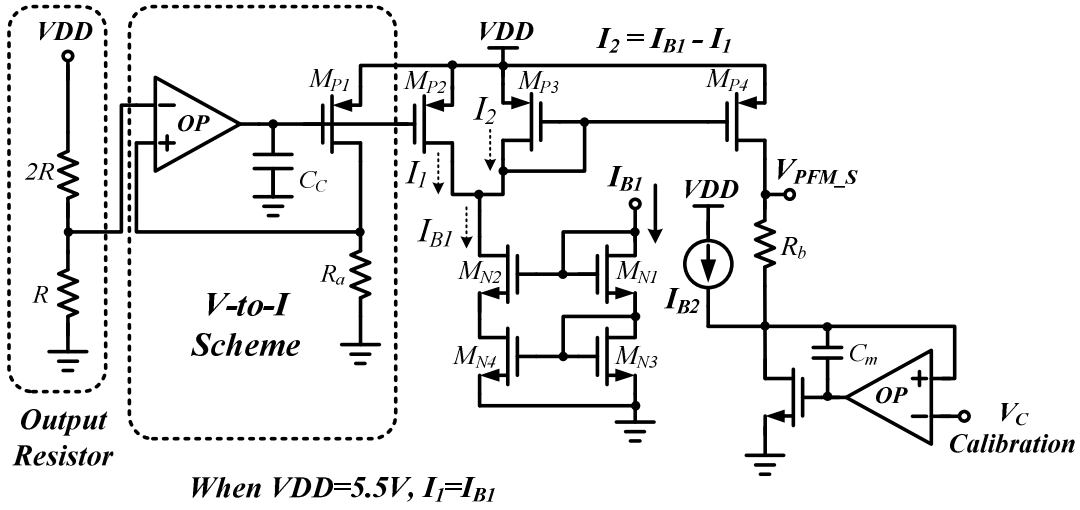


Fig. 72. The schematic of the current fitting curve generator

The waveforms are showed in Fig. 73 and indicated that the voltage V_{PFM_S} is reverse proportional to the supply voltage from 0.51V to 0.70V.

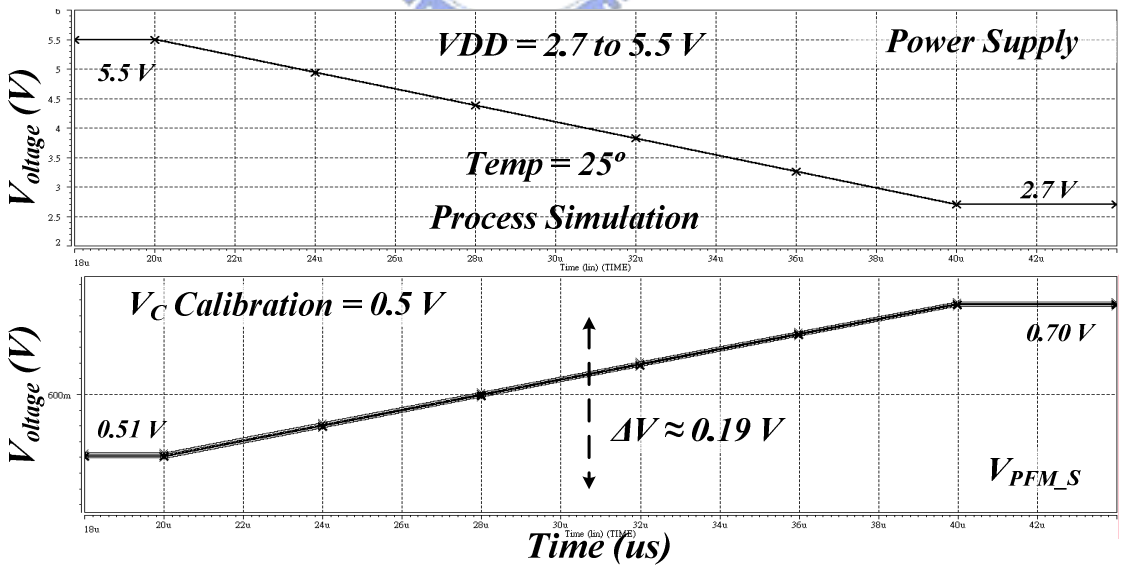


Fig. 73. The simulation waveform of adaptive voltage selection generator

Chapter 5

Simulation Results and Conclusions

5.1 Simulations of Monolithic Buck Converter in PWM Mode

So far, we had derived the expressions and formulas of the proposed compensation technique – high-efficiency slope compensator. The use of $V_{quadratic\_ramp}$ signal replaces the conventional ramp signal (V_{ramp}) which increases from 0% to 90%. The proposed theory is only 10% compensation region of the switching period. Particularly, the 10% compensation region is occurred before the duty cycle (*PWM_PG*) ends. In chapter three, the theorem explains that the V_C signal is affected by supply voltage variation and load current changes. Hence, the proposed theorem used to overcome the problem especially in supply voltage variation. The target is constructing the V_C signal is load dependent only and proportional to the load current requirements. The proposed schematic and sub-circuit simulation results are constructed in chapter four.

In this chapter, whole system simulations are presented. We will simulate the operation of PWM and PFM modes respectively. The simulation results of mode-transition from PWM to PFM mode verifies the proposed theorem is an effective method for replacing the conventional detection circuit.

5.1.1 Simulation Results of Input Voltage Variations

The simulation waveforms of supply voltage changing from 5.5V to 2.7V are illustrated in Fig. 74. In the figure, as the supply voltage decreases from 5.5V to 2.7V, the duty cycle is reverse proportional to the supply voltage to increase larger. The output voltage of system and the inductor current are maintaining at 1.8V and 1A regardless of supply voltage variation, respectively. Particularly, the V_C signal of error amplifier is maintained at a specific voltage level with small difference variation. The voltage difference could be neglected because of the difference is 38mV that is smaller than the V_C voltage variations in load current changes. In other words, the V_C signal is controlled on our way that uses the high-efficiency slope compensation technique to be independent of supply voltage. Hence, the V_C signal is useful and effective to be the detection signal that reflects the information of output loadings.

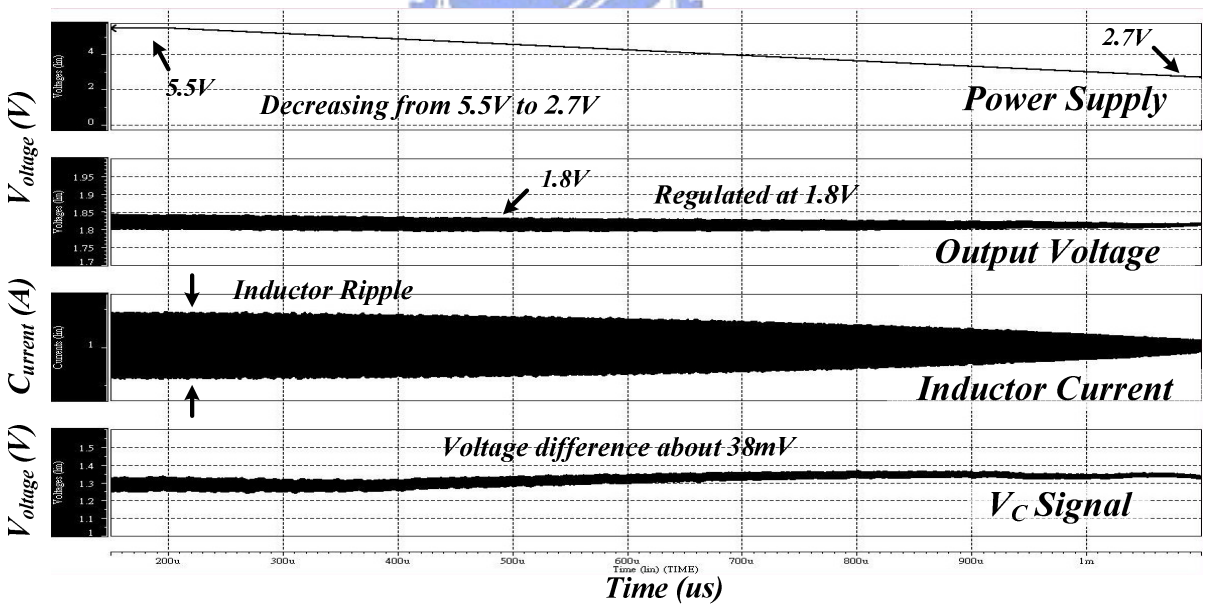


Fig. 74. Simulation waveform of inductor current and Vc signal in supply voltage variation

As the Fig. 75 shown, the V_{sense} is decreasing and reverse proportional to the supply voltage. Oppositely, the V_{slope_comp} is increasing and proportional to the supply voltage. The result of V_{sum} is the combination of both signals and is independent of supply voltage. As the

same described before, the V_{sum} voltage is the positive slope adding to a negative slope establishing a load dependent signal only.

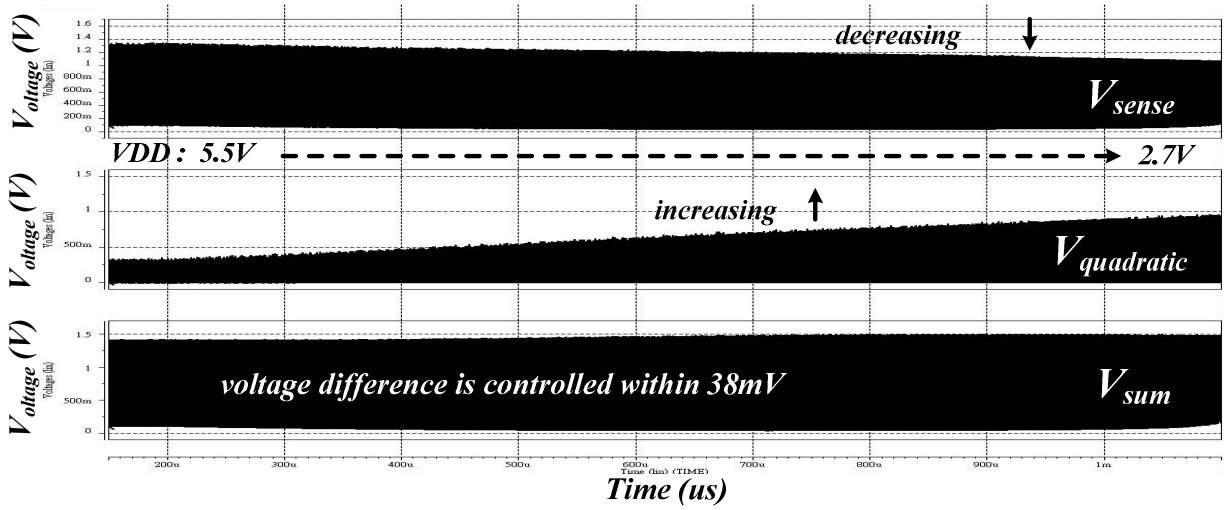


Fig. 75. Simulation waveforms of V_{sense}, V_{slope_comp} and V_{sum} in supply voltage variation

The Fig. 76 is the microcosmic of Fig. 75. The figure shows V_{sense}, $V_{quadratic\_ramp}$ and the V_{sum} signals, respectively.

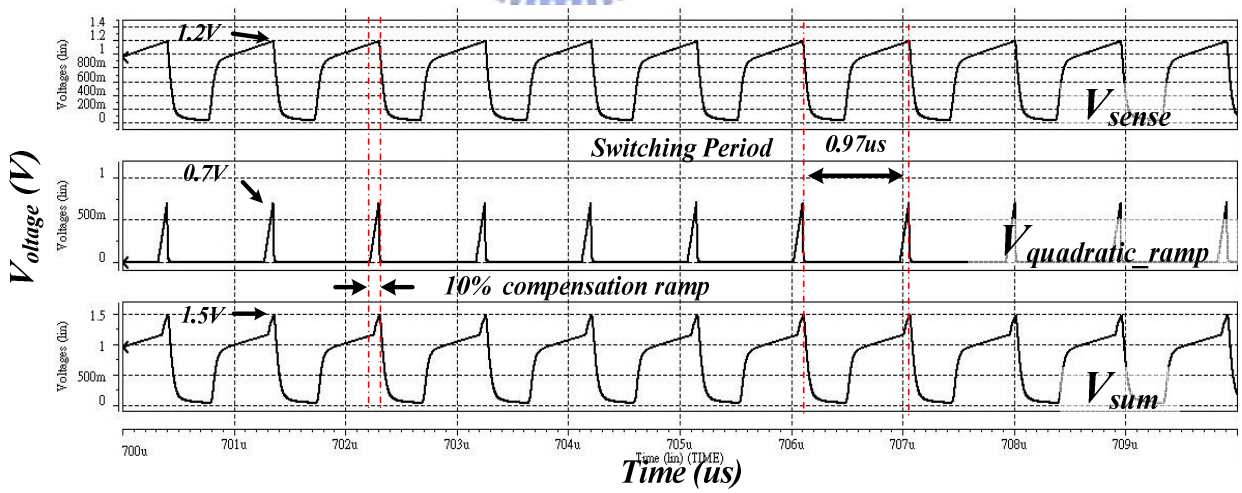


Fig. 76. Simulation waveforms of V_{sense}, $V_{quadratic\_ramp}$ and V_{sum}

The Fig. 77 shows the steady-state waveform of buck converters. The output voltage is regulated in 1.8V and its ripple is 14mV. The inductor current is maintaining at 1A with current ripple 166mA.

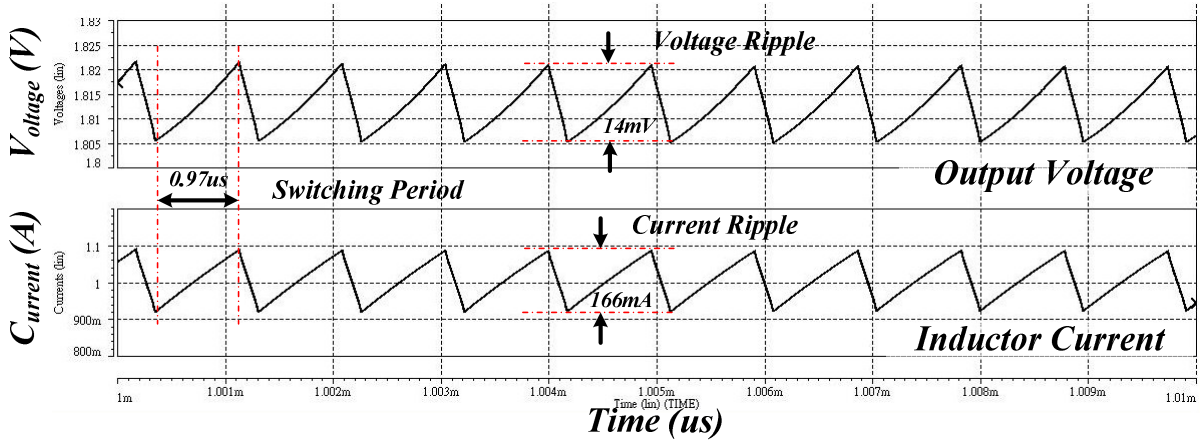


Fig. 77. Simulation waveforms of output voltage and inductor current ripple

5.1.2 Simulation Results of Load Transient Response

The load transient response with load current variation from 1A to 500mA is illustrated in Fig. 78. The output voltage is regulated in 1.8V with supply voltage 3.3V. The Fig. 79 and Fig. 80 is the microcosmic of Fig. 78 that shows the parts of rising and falling time,

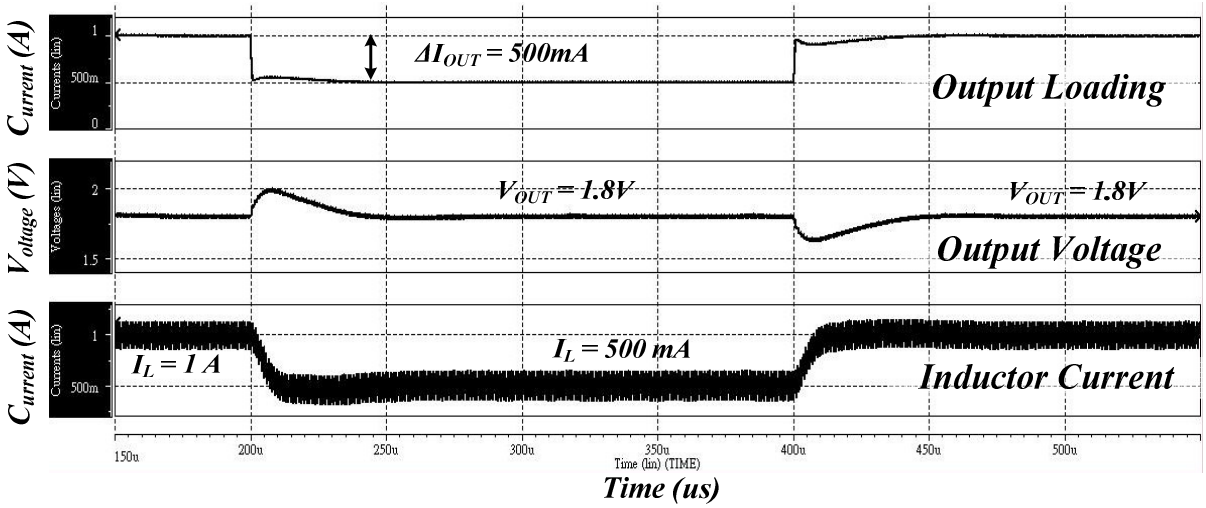


Fig. 78. Whole chip PWM mode simulation: Load transient response (V_{IN}=3.3V)

respectively. In Fig. 79 shows, the load current steps down from 1A to 500mA that results the overshoot of output voltage in 180mV and the settling time equals to 35us. The V_C signal is load dependently changing from 1.35V to 0.85V. Oppositely, as the load current steps up from 500mA to 1A, the undershoot voltage is 150mV and the settling time equals to 40us. The V_C signal is load dependently changing from 0.85V to 1.35V. The parameters of simulation result are listed in Table 7.

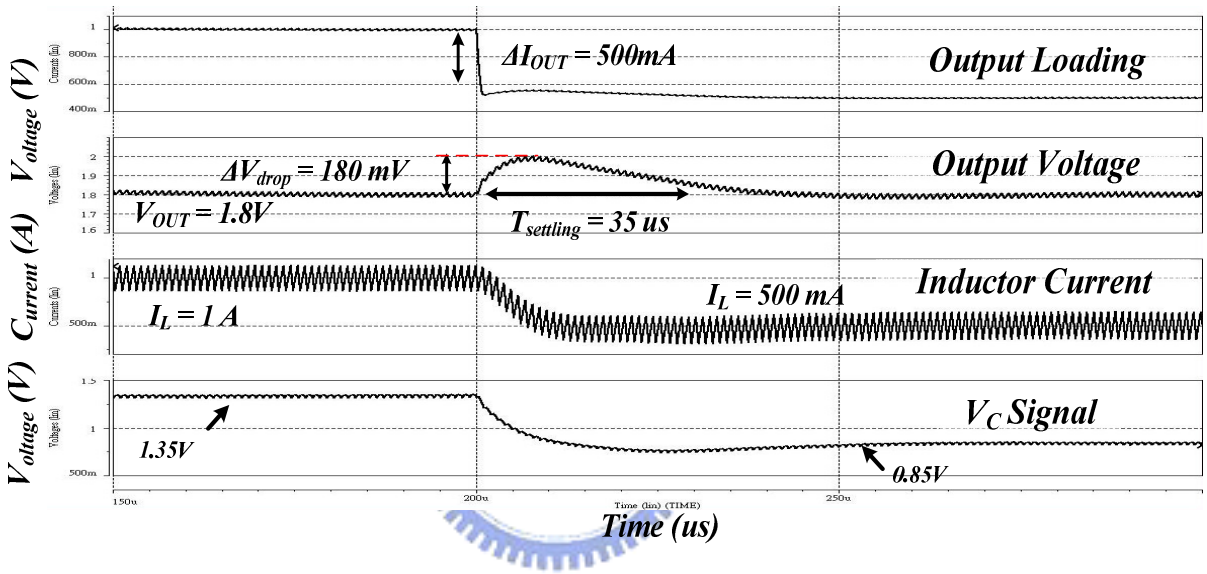


Fig. 79. Load transient response in PWM mode (falling step)

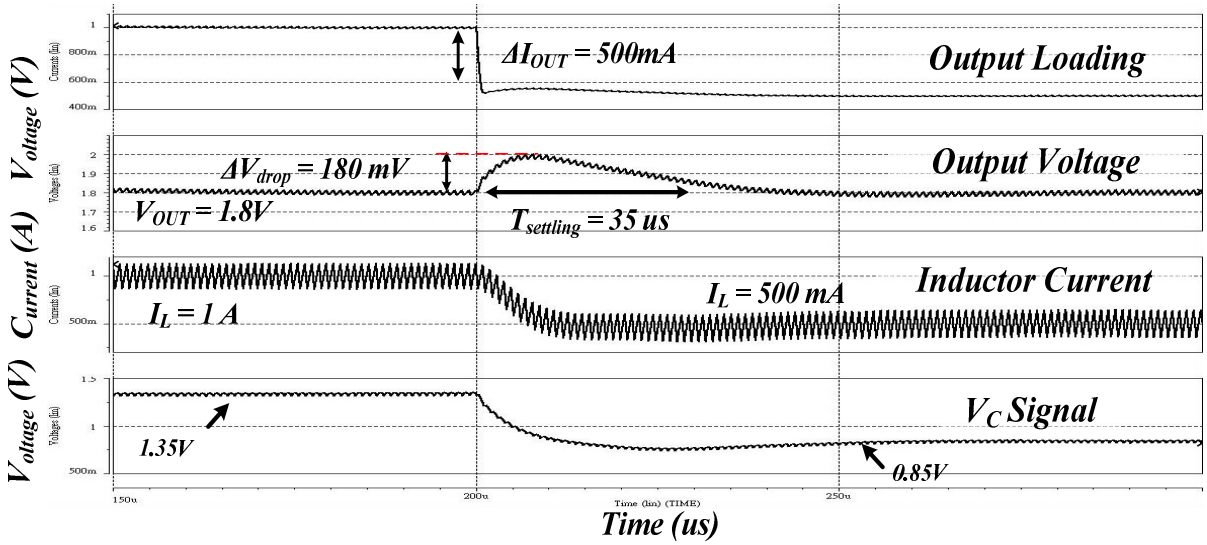


Fig. 80. Load transient response in PWM mode (rising step)

Table 7. The parameters of load transient response in PWM mode

PARAMTER	VALUE	UNIT
Supply voltage (V_{IN})	3.3	V
Output voltage (V_{OUT})	1.8	V
Output current variation (ΔI_{OUT})	500	mA
Overshot voltage at I_{OUT} from 1000mA to 500mA with falling time = 1us	180	mV
Undershot voltage at I_{OUT} from 500mA to 1000mA with rising time = 1us	150	mV
Overshot voltage settling time within ±5% target output voltage	35	us
Undershot voltage settling time within ±5% target output voltage	40	us
Static output voltage error	4	mV
Load regulation	0.008	mV/mA

5.2 Simulations of Monolithic Buck Converter in PFM Mode

The simulation results of PFM mode is illustrated in Fig. 81. There are two different kinds of loadings in the figure, one is 50mA and the other is 100mA. The waveform shows that: the output ripple 60mV corresponds to the frequency 158 kHz and the other ripple 50mV corresponds to the frequency 315 kHz, in loading 50mA and 100mA, respectively. Owning to the operation of zero-current detector, the system is no reverse current occurred on inductor that improves the efficiency in light loadings. Moreover, as the system changes into PFM mode, the sub-circuits that operated in PWM mode only were turned off immediately. Hence, the efficiency in light loading is increasing substantially. The characteristics of different loading in PFM mode are listed in Table 8.

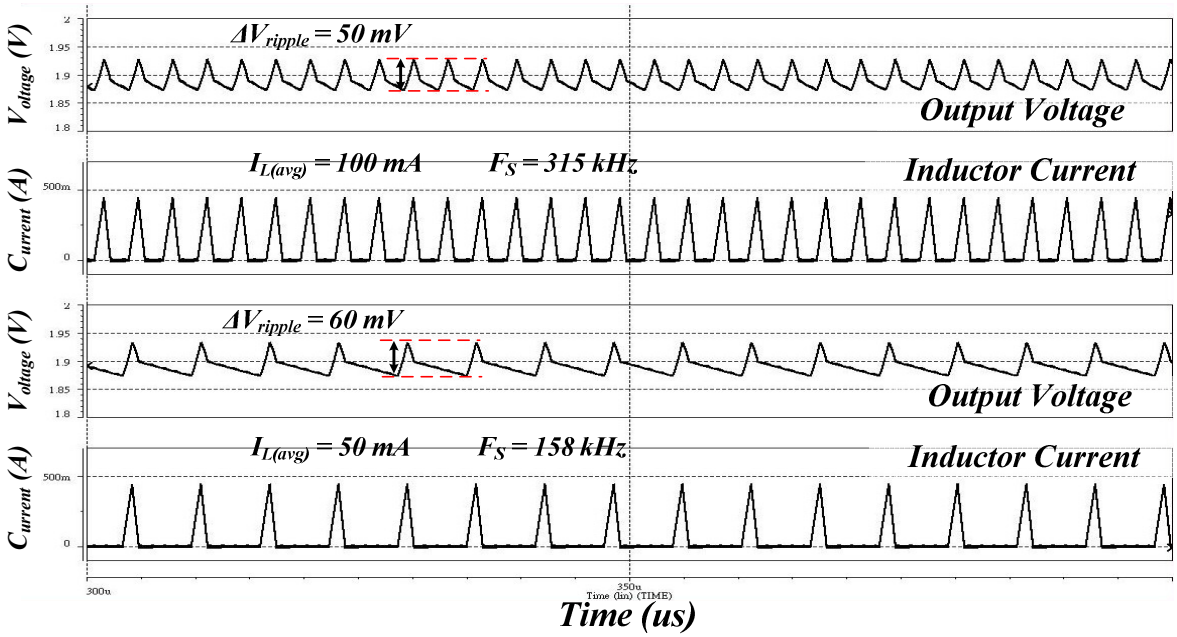


Fig. 81. The simulation waveforms in PFM mode

Table 8. The characteristics of different loading in PFM mode

PARAMTER	Load current	Value
Voltage ripple (V_{ripple})	10mA	70mV
	50mA	60mV
	100mA	50mV
	200mA	35mV
	300mA	18mV
Switching frequency (F_S)	10mA	75KHz
	50mA	158KHz
	100mA	315kHz
	200mA	630kHz
	300mA	1.1MHz

As showed in Table 8, the operation frequency of system in PFM mode is proportional to load requirements. The system efficiency is improved as the switching frequency is reduced because the switching losses are reduced that described in chapter two. Therefore, when the system suffers from the efficiency descending of load current decreasing in PWM, the PFM mode saves the decline tendency to improve the efficiency substantially.

5.3 PMW/PFM Mode Transition

The PWM mode had the best performance and efficiency in heavy loadings. Oppositely, The PFM mode had excellent performance and efficiency in light loadings. Hence, when the system requires load current in wide range, the converter has to operate in either PWM or PFM mode. According to the theorem derived above, the V_C signal is controlled independently of supply voltage variation. Regardless of conventional detection technique, the V_C signal is used to determine the opportunity when to change modes. The Fig. 82 shows the load transient response of mode-transition from PWM to PFM. As the load current decreasing with time, the V_C signal reflects the information of load requirements to descend, too. As the V_C signal is lower than the V_{PFM_S} voltage that mentioned in chapter 4, the V_{PFM_EN} changes from low to high to enable the PFM controller and disable the PWM controller. Thus, the system operates in PFM mode right now. Owning to the duty cycle can't change immediately, the overshoot voltage is generated in 220mV and the settling time is 34us. At the beginning of PFM mode, the inductor current is zero and the requirements of output loading is drawing from the output capacitor only. Hence, the output voltage is decreasing gradually. For a moment, the PFM controller begins to work and regulates the output voltage at 1.8V.

On the other side, as the load current requirements is increasing, the converter had to operate from PFM to PWM mode instantly. The simulation results are illustrated in Fig. 83. Because of the duty cycle can't change immediately, the output capacitor is drawn by loading current that results the output voltage to decrease. As the V_{FB} voltage is lower than 0.59V that is 98% of V_{FB}. The operation mode is changing from PFM to PWM mode and reinstates the switching frequency at 1MHz. The undershoot voltage and settling time is 250mV is 30us, respectively.

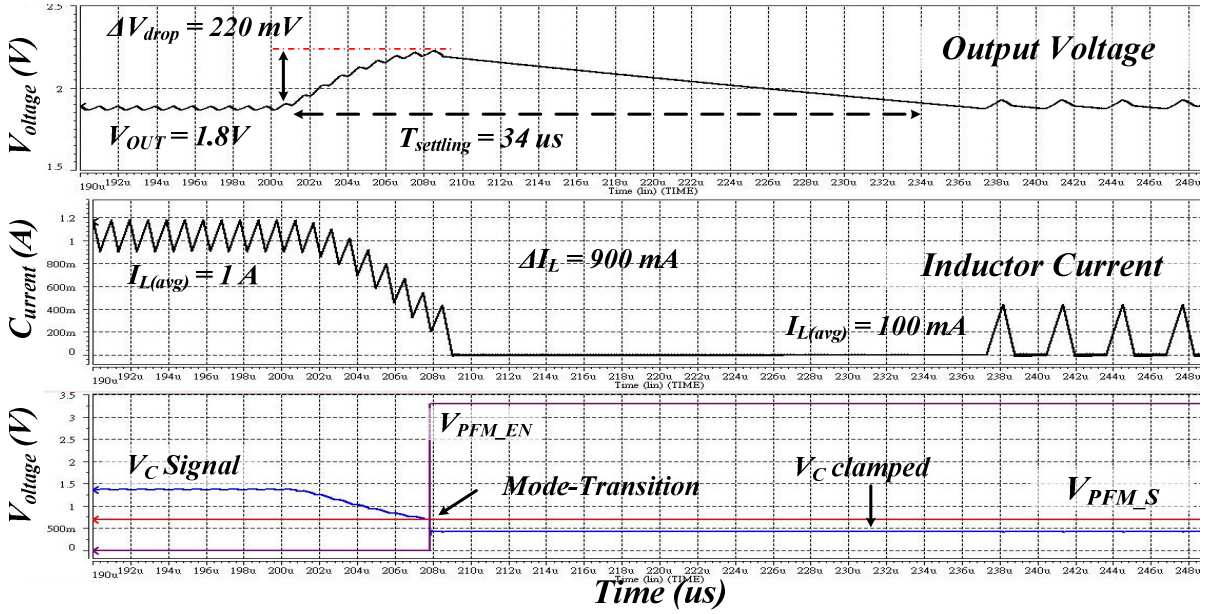


Fig. 82. Full chip simulation: Transition from PWM to PFM mode (falling step load)

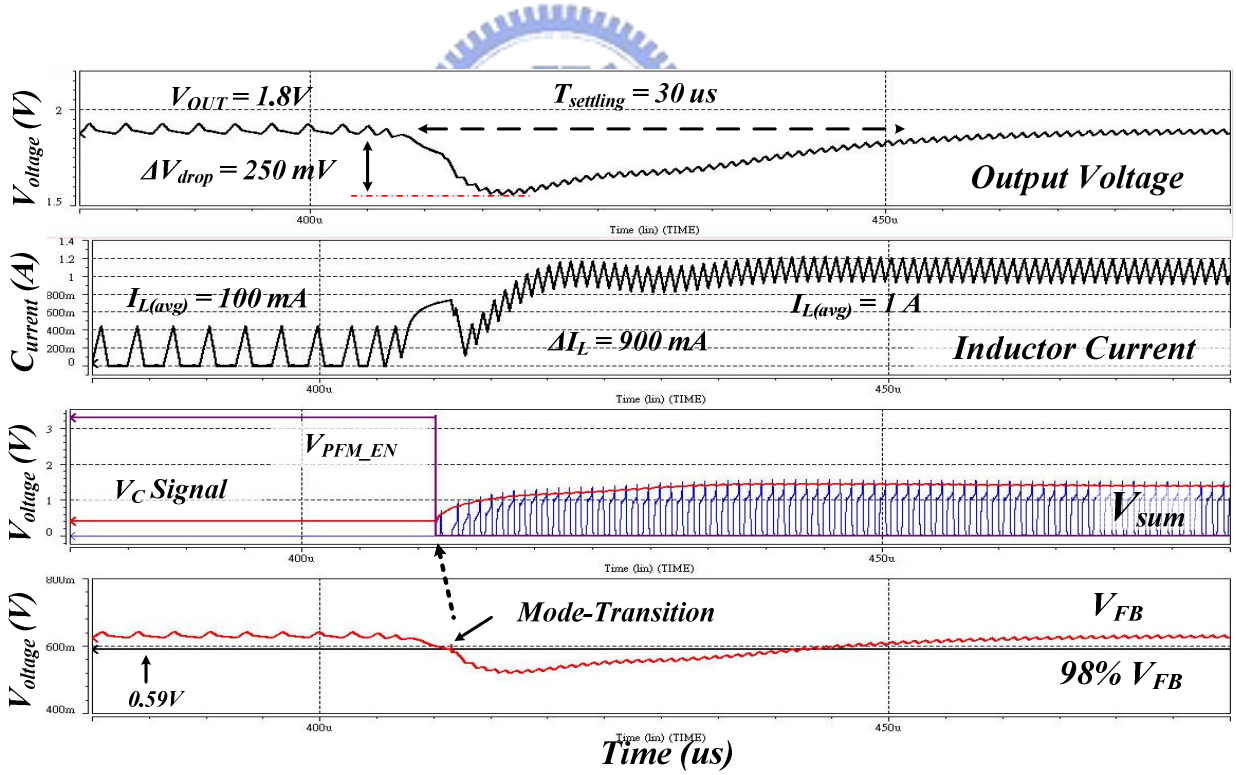


Fig. 83. Full chip simulation: Transition from PFM to PWM mode (rising step load)

5.4 System Efficiency

System efficiency is an important issue to identify the performance of switching converters [38] [39]. The Fig. 84 shows whole system efficiency in distinct supply voltages and operation modes. The PFM mode simulation is in load range from 10mA to 400mA with supply voltage 5.5V, 3.3V and 2.7V. The overall efficiency is generally greater than 80%. The PWM mode simulation is in load range from 100mA to 1000mA with supply voltage 5.5V, 3.3V and 2.7V. The overall efficiency is generally greater than 90%. Particularly, the figure implies that the larger supply voltage has lower system efficiency. Oppositely, the lower supply voltage has larger system efficiency.

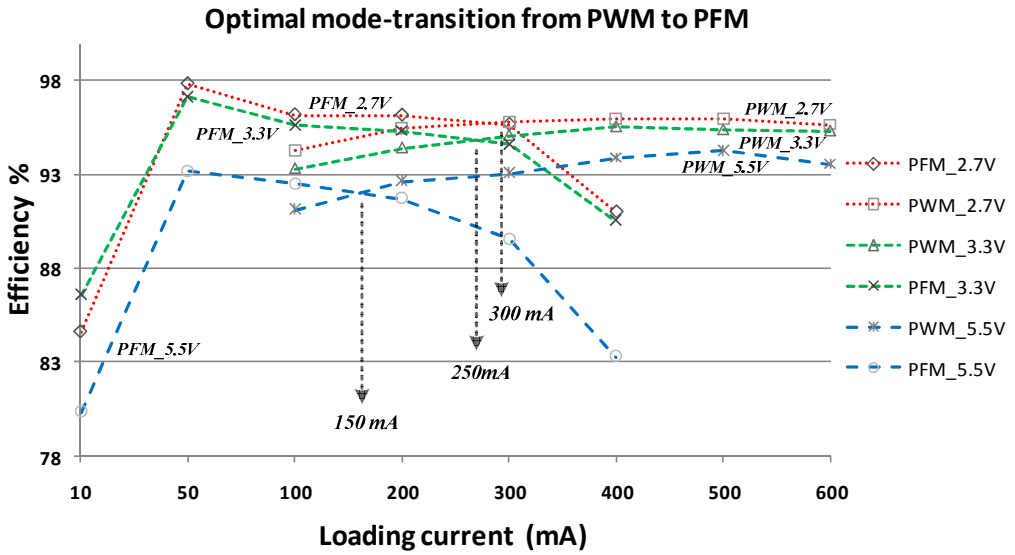


Fig. 84. System efficiency with different supply voltage in PFM mode

We can fine out the optimal transition point from PWM mode to PFM mode are distinct at different supply voltages. The figure shows that the supply voltage 2.7V had higher transition point at load current about 300mA. Oppositely, the supply voltage 5.5V had smaller transition point at load current about 150mA. In supply voltage 3.3V had transition point at load current about 250mA.

5.4.1 Adaptive Mode-Transition Control

According to the figure shows, different supply voltage has different transition points of load current. The optimal transition current are 300mA, 250mA and 150mA corresponding to supply voltage 2.7V, 3.3V and 5.5V, respectively. We could fine out the optimal transition voltage *PFM_S* corresponding to different transition current. The *PFM_S* signal means the boundary voltage between PWM and PFM modes. As the V_C signal larger than the *PFM_S* voltage, the system operates in PWM mode. Oppositely, as the V_C signal lower than the *PFM_S* voltage, the system operates in PFM mode. Hence, we could arrange the values of supply voltage, load current and *PFM_S* voltage to establish the relationships in Fig. 85.

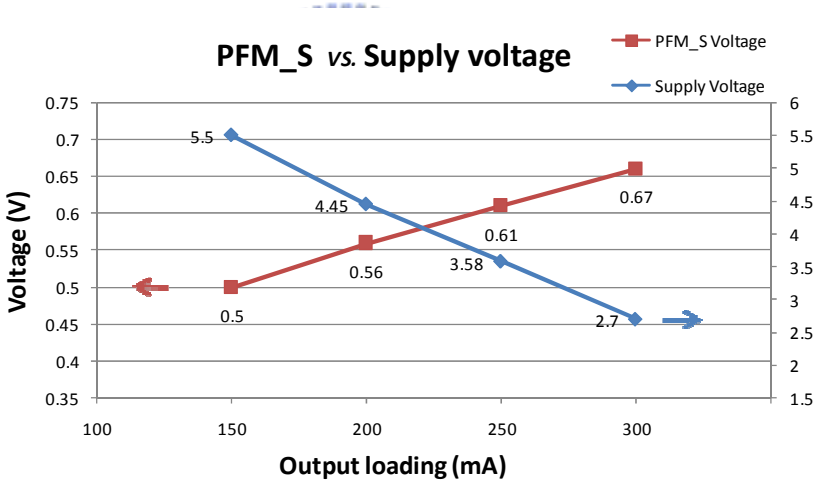


Fig. 85. The relationships of supply voltage, loading current and *PFM_S* voltage

The figure shows that the *PFM_S* voltage increases from 0.5V to 0.67V as the supply voltage decreases from 5.5V to 2.7V and corresponds to the load current increases from 150mA to 300mA. Therefore, we can use current fitting technique plotted in Fig. 86 to achieve adaptive mode-transition control. The original curve of *PFM_S* is the target we want to arrive. And the fitting curve is the artificial curve that we made.

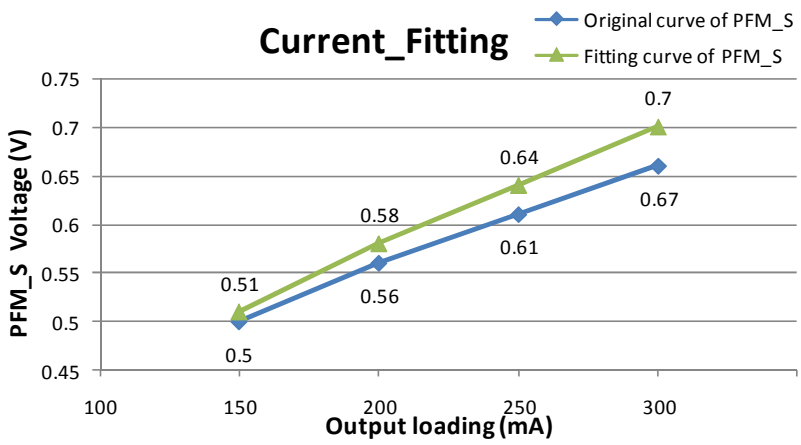


Fig. 86. Current fitting diagram of *PFM_S* voltage and loading current

Circuit implementation in Fig. 87 is an adaptive mode-transition controller. This circuit produces the V_{PFM_S} voltage to be reverse proportional to the supply voltage V_{DD}. Besides, we use the V_C *Calibration* signal to correct the V_{PFM_S} voltage when the V_C voltage was varied in process variation. The formulas of V_{PFM_S} voltage are expressed in (73) and (74).

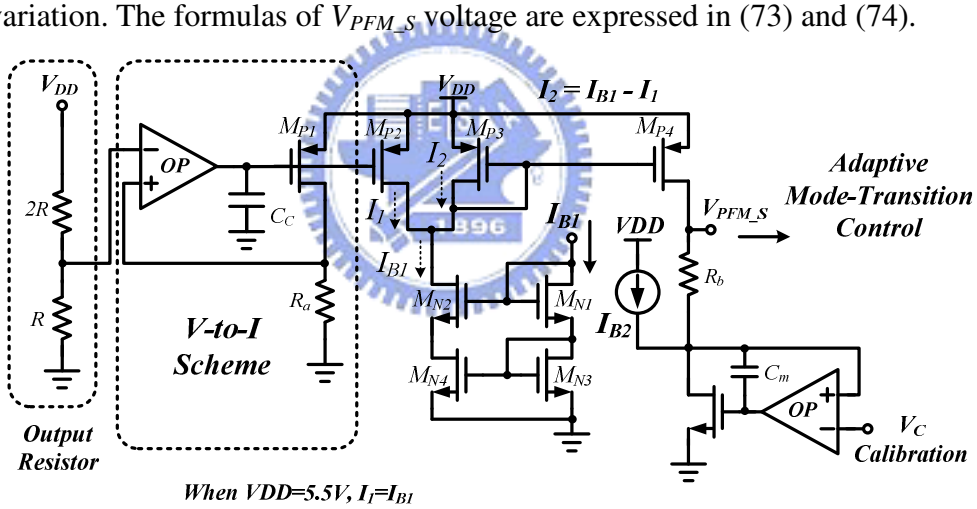


Fig. 87. The schematic of the adaptive mode-transition controller

$$V_{PFM\_S} = V_{C\_cali} + (I_{B1} - \frac{V_{DD}}{3R_a}) \cdot R_b \tag{73}$$

$$V_{PFM\_S} = V_{C\_cali} \text{ , } As\ V_{DD} = 5.5v,\ I_1 = I_{B1}\ \ \&\ \ I_2 = 0 \tag{74}$$

The improvement of whole system efficiency in mode transition region is plotted in Fig. 88. By using the HSC controller and adaptive mode-transition circuit, the efficiency in transition region is improving about 5%.

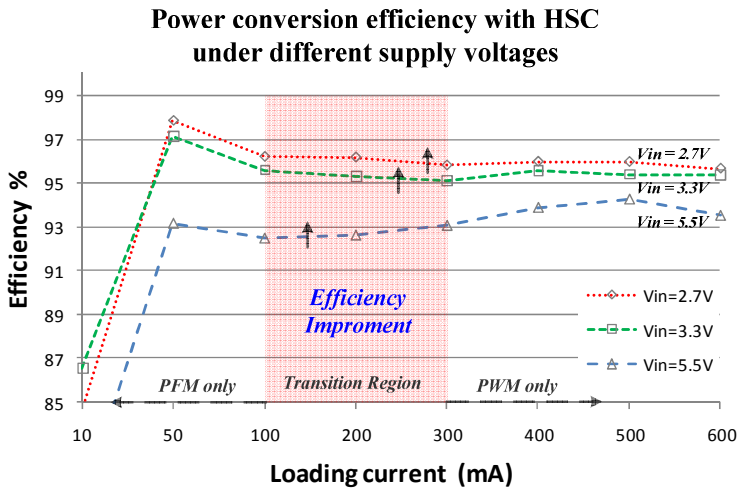


Fig. 88. Efficiency improvement in mode transition region with HSC controller

5.5 Conclusions

So far, the thesis expressed and derived the issues, relationships and formulas of the proposed technique – high-efficiency slope compensation. It doesn't like conventional slope compensator that is using sawtooth ramp only. It uses the pulse-ramp to control the V_C voltage independently of supply voltage variation. Moreover, the system not only had good noise immunity that without using the V_X voltage as a detection signal, but also had excellent efficiency in transition region between PWM to PFM modes. Besides, the advantage of good noise immunity makes the system can operate in high switching frequency more than 20MHz. Thus, the system had wide switching frequency range in power converters.

5.5.1 Whole Chip Layout Diagram

Table 9. The electronic parameters of whole chip system

PARAMTER	VALUE	UNIT
Die Size	1500 x 1200	mm
Technology	0.35	um
Pad Numbers	36	pin
Inductor size (off-chip)	2.7	uH
Capacitor size (off-chip)	10	uF
Switching Frequency	1	MHz

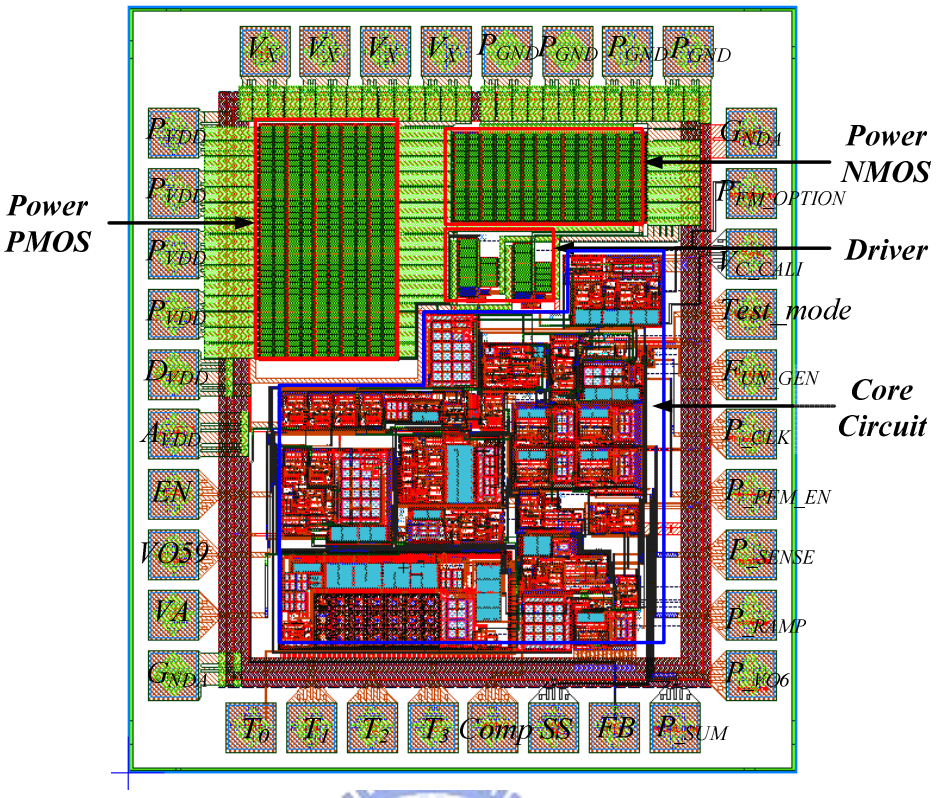


Fig. 89. Whole chip layout diagram of proposed slope compensation circuit

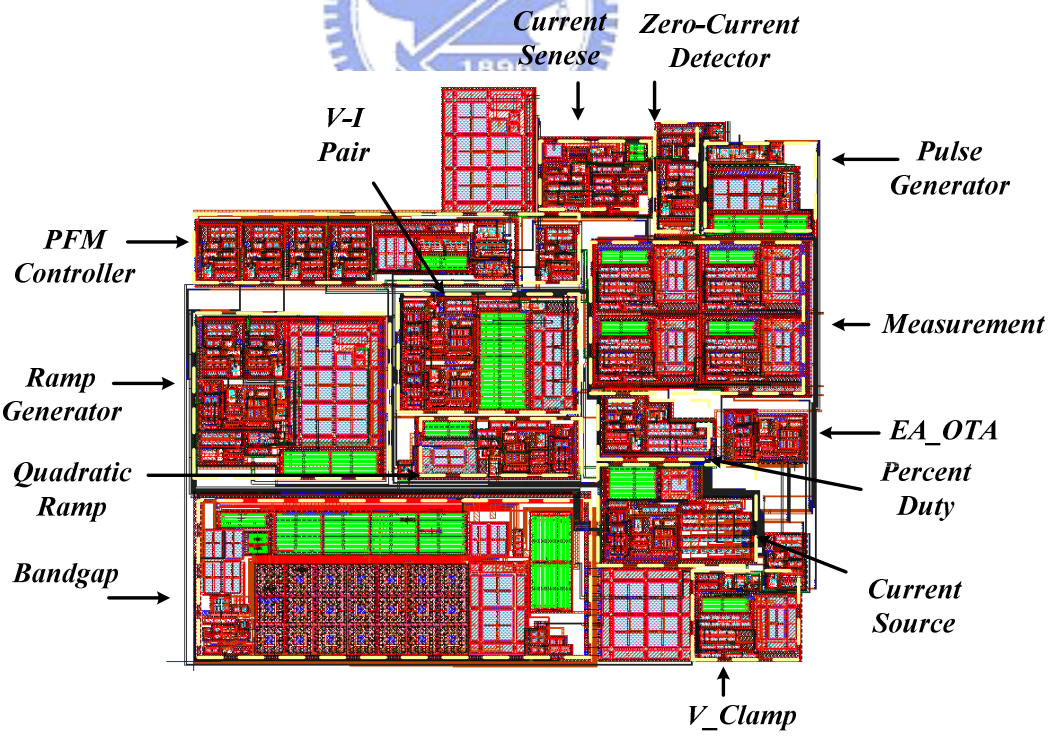
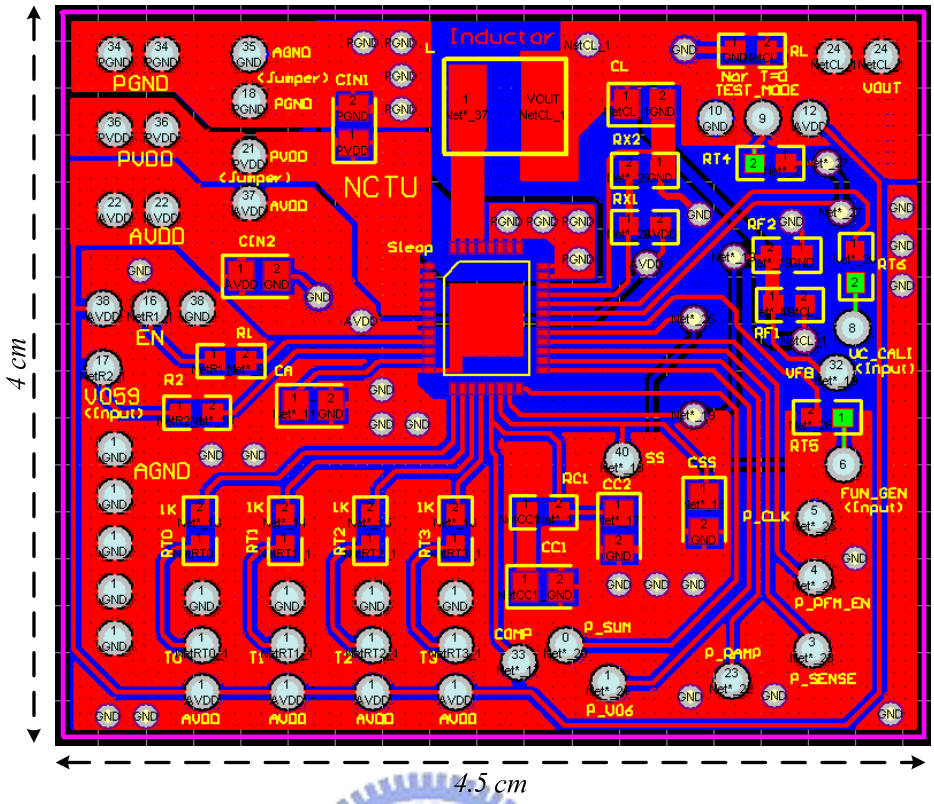


Fig. 90. Core circuit layout diagram of proposed slope compensation circuit



4.5 cm

Fig. 91. PCB layout diagram

5.6 Future Works

Although the proposed system had optimal transition point between PWM and PFM modes, it still had something needs to improve. The V_C *Calibration* signal is used to correct the *PFM_S* voltage to calibrate the variation of process issues. But the V_C *Calibration* is the artificial signal that is forced by function generator. It makes the system inflexible. Therefore, the improvement of the system is removing the artificial signal of V_C *Calibration* to achieve real adaptive mode-transition control in future works. That's the system without extra signal to control the converter. All signals are produced by itself.

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