國立交通大學

電機與控制工程學系

碩士論文

全電流控制高頻切換直流轉直流降壓式電源轉換器

High Switching DC-DC Buck Converters in Current Domain Control

研究生：謝維倫

指導教授：陳科宏　博士

中華民國九十七年十月

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研 究 生：謝維倫　　Student：Wei-Lun Hsieh
指導教授：陳科宏　　Advisor：Ke-Horng Chen

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摘　要

在可攜式電子產品的應用上，高效能和小型的電壓轉換器在提供系統電源上扮演非常重要的角色。為了減少輸出級濾波器的面積，提出高頻切換的直流轉直流降壓轉換器來達到元件整合的功能。然而，對傳統電流控制模式之直流轉直流降壓轉換器來說並不適合在高頻切換的操作，因為使用到運算放大器之子電路其頻寬會被限制住。也就是說，由於電路頻寬的極限造成不正確的操作且無法跟上系統的操作頻率。為了保證電壓轉換器可以操作在高切換頻率下，全電流脈波寬度調變控制器在本論文中被提出了。

由於使用了全電流脈波寬度調變控制器，因為少了外部補償元件使得操作電路將會變的較簡單，且控制訊號全都轉換成電流形式讓訊號相加變得直接。為了能提供高效能電源電壓，也是其中一種電流模式控制技術的全電流脈波寬度調變控制器將可得到較佳的線調節率和負載調節率。

本篇論文實現了 20MHz 的全電流控制高頻切換直流轉直流降壓式電源轉換器，且以台灣積體電路製造股份有限公司點三五微米互補式金氧製程來實現，輸入電壓範圍從 3.0 伏特到 4.0 伏特，其負載調節率及線調節率分別為 0.18356mV/mA 和 48.5V/V。系統特色為可使用較小的外部濾波元件且得到較快的暫態響應，其中電感大小只需 200nH、輸出電容值只需 5μF。非常適合於可攜式電子產品之電源管理。

High Switching DC-DC Buck Converters in Current Domain Control

Student: Wei-Lun Hsieh Advisor: Dr. Ke-Horng Chen

Department of Electrical and Control Engineering
National Chiao-Tung University

Abstract

For portable electronic device applications, high performance and compact size voltage regulator plays an important role to provide system power. To reduce the size of output filter, a high switching dc-dc buck converter is presented to achieve high integration. However, the conventional current mode DC-DC buck converter is not suitable to high switching design because the sub-circuits, which uses operational amplifier, restrict the bandwidth. That is to say, the limitation of circuit bandwidth causes incorrect operation and can not follow the system switching frequency. To ensure the switching regulator can operate at high switching frequency, the current domain PWM controller is presented in this thesis.

Owing the current domain PWM controller, the circuit implementation becomes simple and there are not any external compensation components. The control signals are transformed to current form to process addition of control signal directly. For providing a high performance supply voltage, the current domain PWM control is one of current-mode technique to get good line and load regulations.

In this thesis, a high switching DC-DC buck converter in current domain control with frequency 20MHz is implemented. The test chip was implemented by TSMC 2P4M 0.25-μm CMOS technology. Input operation range varies from 3.0V to 4.0V. The load regulation and line regulation are 0.18356mV/mA and 48.5mV/V respectively. The system features smaller output filter. That is, the inductor and output capacitor values are only 200nH and 5μF respectively. Fast transition response is achieved and demonstrates the design suitable for power management in the portable devices.

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Chapter 1
Introduction

In recent years, power management has become more popular and important subject because the electronic devices need longer usage lifetime, especially for battery-based portable devices such as personal digital assistance (PDA), cell phone and digital camera (DCS). That is to say, effective energy usage and minimum power loss are two major topics to achieve power consumption efficiency enhancement. In this chapter, we will show the background and basic knowledge of power management system in chapter 1.1 firstly. The classification of power management circuits which including switching converters, linear regulators, and charge pump converters will show in chapter 1.2. The motivation will give in chapter 1.3. Finally, the thesis organization will show in chapter 1.4.

1.1 Background of Power Management System

With recent advances in integrated mixed-signal circuits and an increasing demand for low-power multifunction system-on-a-chip (SOC) and extended battery runtime, there is a strong need for the development of efficient on-chip power regulation and distribution. As shown in Fig. 1, the growing of battery energy is not enough to supplying power of chips in the future. That is to say, as increasing chip functionality and complexity will overrun available battery energy budget. To solve this problem, the straightforward method is increasing the quantity of power source. Unfortunately, it is not permitted for portable devices because of convenience. In order to decrease the expenses, the power management systems are utilized to provide the specific regulated voltages without consuming unnecessary batteries.

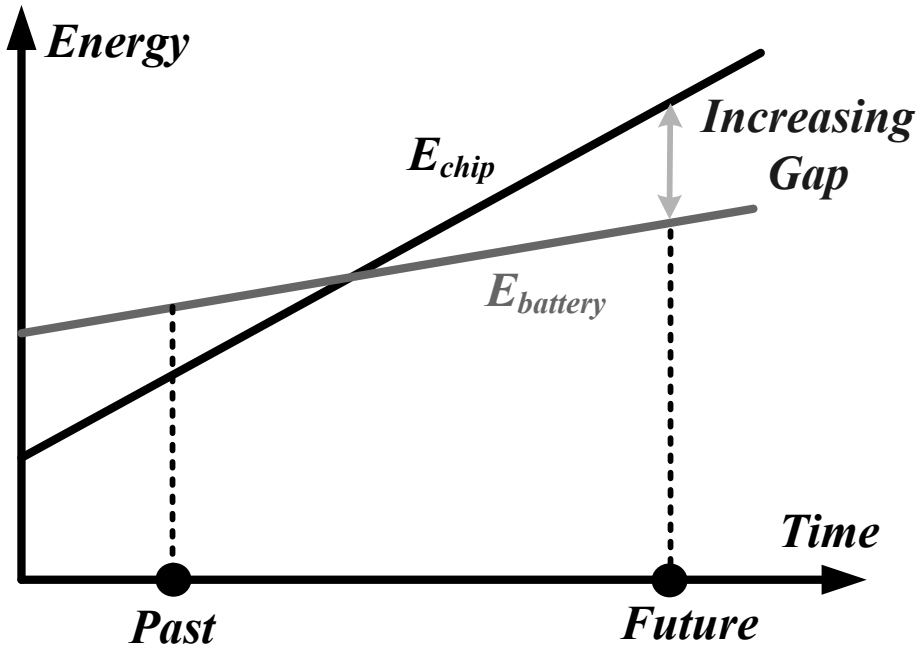


Fig. 1. Energy constrained operation.

As mention before, the best method of power saving and efficiency increasing is constructs power management system. The advantage of power management system not only generate regulated supply voltage for different specific integrate circuits but also suppress the noise which is coupling from battery to electronic devices to extend battery's lifetime. Take cell phone for example, the basic power management system diagram of cell phone is shown in Fig. 2 [1], a mobile phone may need at least five regulated voltages, one buck converter for DSP core CPU, high PSRR LDO regulators for RF power amplifier and low noise amplifier, one boost converter for cooler LCD panel, LDO regulators for analog base-band, audio and interface applications, and one charge pump for white light LED driver. The system of cell phone will operate in different modes, such as sleeping mode, communication mode and so on. The control unit is needed to control the internal power management block enable or disable, respectively. That is to say, by using control unit can enhance system efficiency of power supply circuits, such as linear regulators, switching regulators and charge pumps. The ability

of saving power and efficiency increasing, that is why power management system playing an important roles in the field of electronics, especially for portable devices.

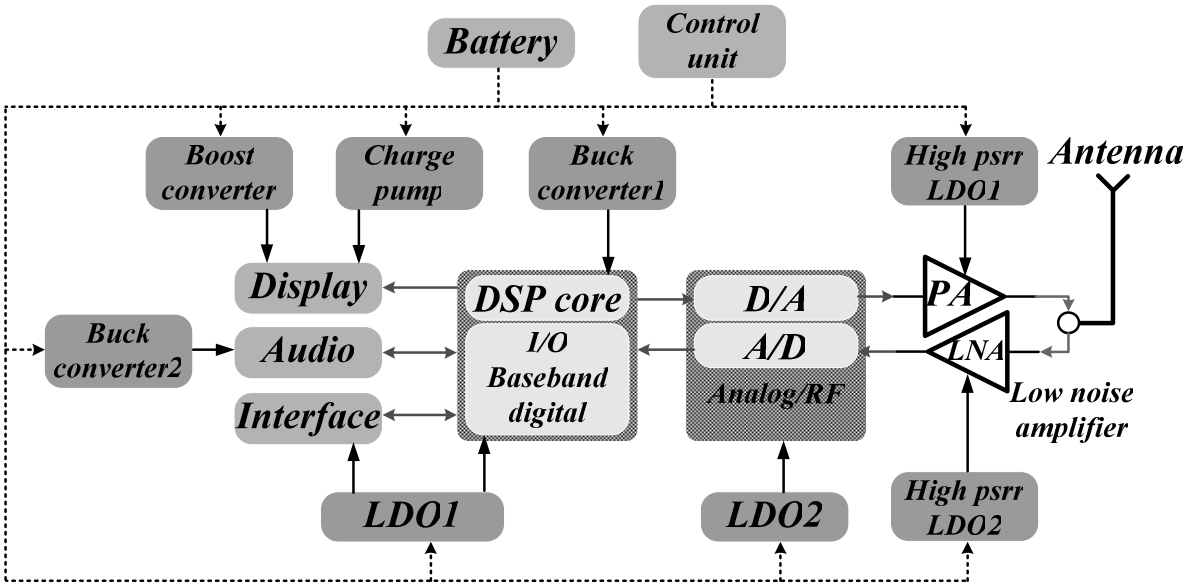


Fig. 2. Power management system diagram of cell phone.[1]

1.2 Classification of Voltage Regulators

In this section, three kinds of voltage regulators will be introduced briefly, including linear regulators, switched capacitor circuits and switching regulators. Finally, a brief comparison will be given about three types of voltage regulators. The comparisons included circuit complexity, cost, efficiency, load ability and so on.

1.2.1 Linear Regulator

The basic structure of linear regulator is shown in Fig. 3[2], it also called low drop-out (LDO) voltage regulator because there is a drop out voltage ($V_{dropout}$) between input and output pin about 100~500mV. The power MOSFET has equivalent resistor (R_{DS}) from input to output, so the power MOSFET size should be well designed to fit the regulated output voltage and load ability. The linear regulator main control circuit was error amplifier, it could adopt output voltage information form resistive feedback network (V_{FB}) then compare to

reference voltage (V_{REF}). After error amplifier operation, it could immediately adjust input and output difference then control the gate of power MOSFET to supply load current.

The features of linear regulator are described as follows. Firstly, the linear regulator whole circuit is simple and compact, so the die size is smaller than other voltage regulators. And secondly, linear regulator is easy to use, instead of using inductor to transfer energy, the linear regulator just adding two capacitors at input and output pin respectively. As a result, it not only can reduces Printed-circuit board (PCB) area but also cost down. Thirdly, linear regulator only uses resistive feedback network and error amplifier output analogy signal to control power MOSFET, it doesn't use any switching base circuits. So this kind of regulator has no Electro Magnetic Interference (EMI) and no output ripple, there are very suit for audio, analog and RF circuit applications. Finally, because of without dual storage components, the linear regulator only can do buck regulation. The efficiency is proportional to output voltage and the highest efficiency occurs that output voltage is near to input voltage.

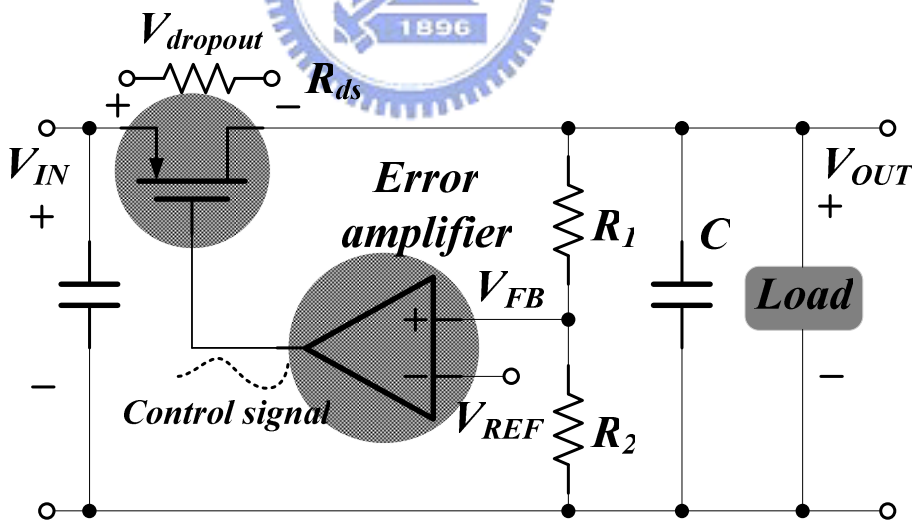


Fig. 3. The basic structure of linear regulator.

1.2.2 Charge Pump

The basic structure of two-phase charge pump regulator is shown in Fig. 4[3] [4]. Power stage consists of capacitors (C_1 C_2) and switches (S_1 S_2 S_3 S_4). Detailed operation is described as follows, during the first phase, switches S_1 and S_2 turn on and switches S_3 and S_4. The input voltage charges capacitor C_1 to the input voltage level (V_{IN}). Than during the second phase, switches S_3 and S_4 turn on and switches S_1 and S_2. Because the capacitor C_1 still maintained the charge from the previous phase, the output voltage equals to input voltage adding voltage across the capacitor C_1, ideally obtains twice input voltage. Adding hysteric feedback control, the output can be regulated at desired voltage level.

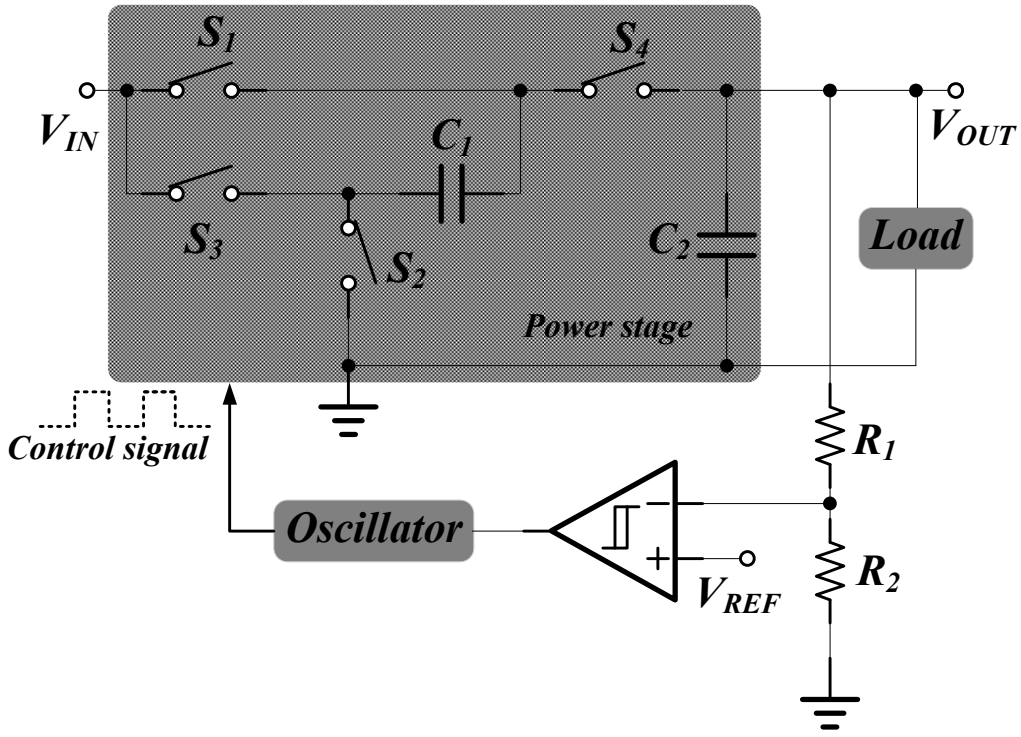


Fig. 4. The basic structure of charge pump.

The features of charge pump are described as follows. Firstly, the charge pump can be operated in both buck and boost types, it depended on the hysteric feedback control and

reference voltage, but it's more efficiently at boost type. Secondly, the circuit complexity of charge pump is between linear regulator and switching regulator, which is more compact than switching regulator but more complicated than switching regulator. Thirdly, due to digital rail-to-rail switching clock control, the charge pump suffers from EMI and output noise problems. But this problem doesn't heavier than switching regulator because of lower operation frequency. Finally, the load ability of charge pump is weak because the ability depends on the output capacitor C_2 and switching frequency. That is to say, the larger output capacitor causes the powerful load ability. Because of light load ability typically, the charge pump is very suit for displaying applications, such as driving the gate of MOSFET to on or off.

1.2.3 Switching Regulator

The basic structure of buck type voltage mode switching regulator is shown in Fig. 5[5]. The power stage of switching regulator consists of a couple of complementary power MOSFET (M_P M_N), passive storage elements inductor (L) and capacitor (C) and resistive feedback network (R_1 R_2). Detailed operation is described as follows; the resistors R_1 and R_2 sensing the variation of output voltage and error amplifier receives the voltage variation information then brings the error signal (V_C). The comparator's inputs receive the error signal from error amplifier and the ramp signal (V_{RAMP}) from ramp generator, then compares the quantity between the error signal and the ramp signal to decide the duty cycle. After generating the control signal, the PWM generator control the detail timing to avoid short through current. At last, the purposes of gate drivers are driving huge complementary power MOSFET. At the first subinterval, upper power MOSFET (M_P) turns on and lower power MOSFET (M_N) turns off then input voltage source charge the inductor and the capacitor. At the second subinterval, lower power MOSFET (M_N) turns on and upper power MOSFET (M_P)

turns off then the inductor will discharge to the capacitor and load. By the above-mentioned, the switching regulator adjusts the output voltage error and regulates to correct voltage.

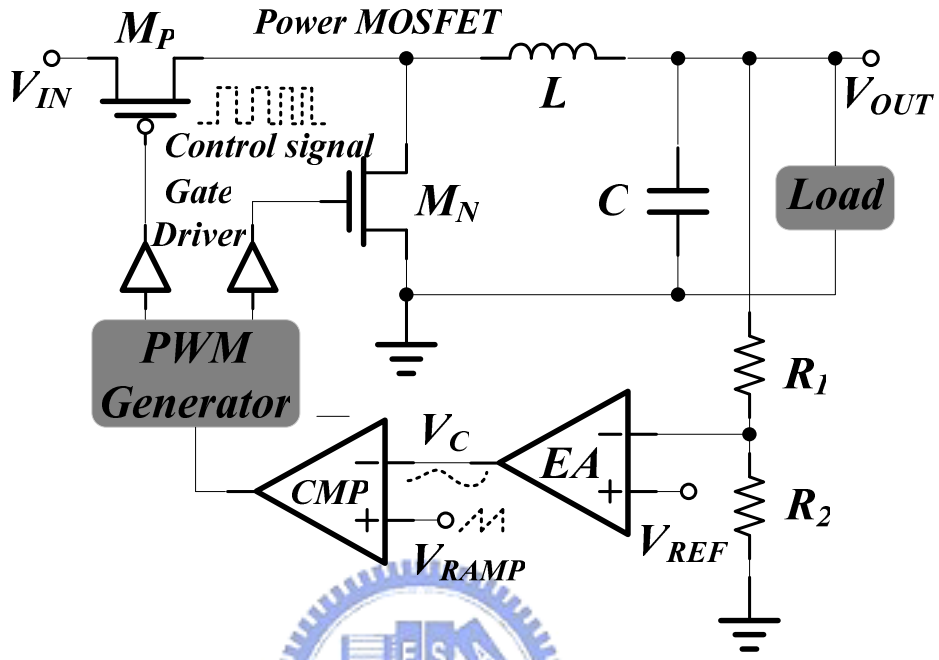


Fig. 5. The basic structure of buck type voltage mode switching regulator.

The features of switching regulator are described as follows. Firstly, due to the storage components such as inductor and capacitor, the switching regulator can operate in three kinds of type including buck, boost and buck-boost mode. But the more external components cause the bigger PCB size and cost. Secondly, because of switching based circuits, it suffers from EMI and noise problems critically, it will take circuit layout into consideration to avoid EMI and noise problems. Finally, the load ability of switching regulator is the largest which is in the range about hundreds of milliamps to several amps, so the efficiency of switching regulator is the highest at heavy loading, up to 90%. But operating at light loading will decline.

1.2.4 Comparison

As the above description, three types of voltage regulator have its own advantages and

disadvantages. How to choose the best voltage regulator as power supply depend on the electronic applications characteristics and specifications. The comparison of different type voltage regulator is listed in TABLE I.

TABLE I. COMPARISONS OF DIFFERENT TYPE REGULATORS.

Characteristics	*Linear Regulator*	*Switching Regulator*	*Charge Pump*
Regulation Type	***Buck***	***Buck/boost/buck-boost***	***Buck/boost***
Chip Area	***Compact***	***Large***	***Moderate***
Efficiency	***Minimum***	***Maximum***	***Medium***
EMI/Noise	***Minimum***	***Maximum***	***Medium***
Load ability	***Medium***	***Maximum***	***Minimum***
Complexity	***Simplest***	***Complicated***	***Medium***
Cost	***Low***	***High***	***Medium***

1.3 Motivation

Conventionally, the switching frequency of current mode DC-DC buck converter operated in the range of hundreds of Kilo-Hertz to several Mega-Hertz. The larger output filter such as inductor and capacitor are placed to off-chip inevitably. To reduce the size of output filter, the straightforward way is increasing the switching frequency. Owing to higher switching frequency, the on-chip output filter in DC-DC switching converter is possible in the future. Meanwhile, with the development of SOC system, a compact solution is needed to reduce the footprint area effectively of the power management module. Besides, the operating voltage of the SOC system is too low to have better signal-to-noise ratio, the high performance voltage regulator needed to generate a regulated and steady supply voltage. In

this part, the current mode technique is used to obtain better line and load regulations. So the implementation of switching frequency 20MHZ current domain DC-DC buck converter is presented base on the above-mentioned motivations.

Although, the higher switching frequency will seriously affect not only current sensing accuracy and response time but also other kind of system circuits. The 20MHz system circuit design is also shown in this thesis.

1.4 Thesis Organization

The thesis introduces the basic knowledge of current mode switching regulator in the Chapter 2. In the Chapter 3, the design and architecture of high switching dc-dc buck converter in current domain control are presented. Base on 20MHz current domain PWM control system, the internal overall circuit implementation and simulation results are shown in Chapter 4. Finally, the whole system chip simulation, system specification, conclusions and future work are presented in Chapter 5.

Chapter 2
Basic Knowledge of Switching Regulator

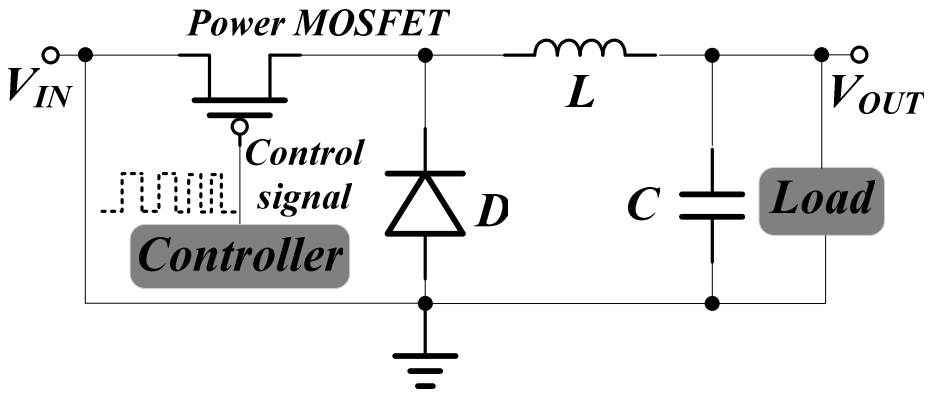
In the chapter 2, the basic knowledge of switching regulator is presented. In section 2.1, the three kinds of DC-DC converter topologies are introduced including conversion ratio and power stage structure. The next section 2.2 will show three kinds of controlling modulator including pulse width modulation (PWM), pulse frequency modulation (PFM) and hysteretic control technique. The control principle of current mode buck converter including CCM (continuous conduction mode) and DCM (discontinuous conduction mode) operation and small signal analysis respectively are shown in the section 2.3. At last, the Characteristics and performance specification of buck converter are presented in the section 2.4.

2.1 Topologies of DC-DC Converter

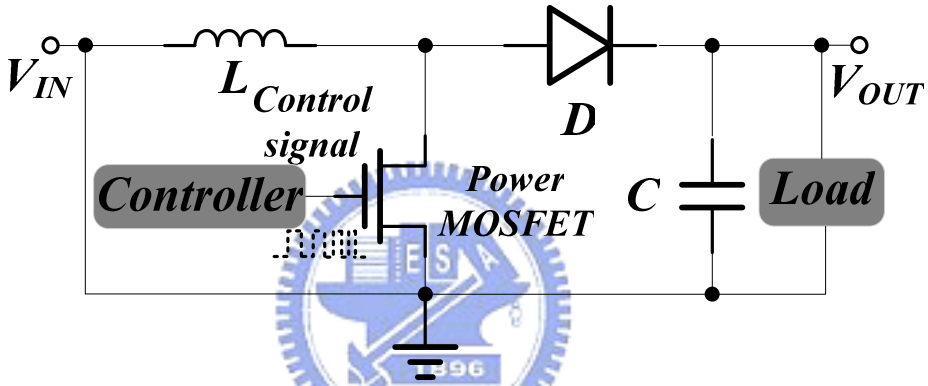
This section introduces three converter topologies of switching regulator, according to the placement of components can combine to buck, boost, and buck–boost types, as shown in Fig. 6[5] [6] [7]. The converter consists of storage element; power MOSFET as the switch to drive large current by control signal and diode as another current passage to charge or discharge output load. The control signal translated the energy from input to output by passing the power MOSFET and regulates output to desire voltage.

The buck converter only can translate high input voltage to low output voltage. Contrarily, the boost converter only can translate low input voltage to high output voltage. The buck-boost can regulate desired output voltage even the input voltage operating at higher or lower than the output. A briefly comparison of the three converter topologies characteristic are listed in the TABLE II. The conversion ratio is defined as the power MOSFET on time

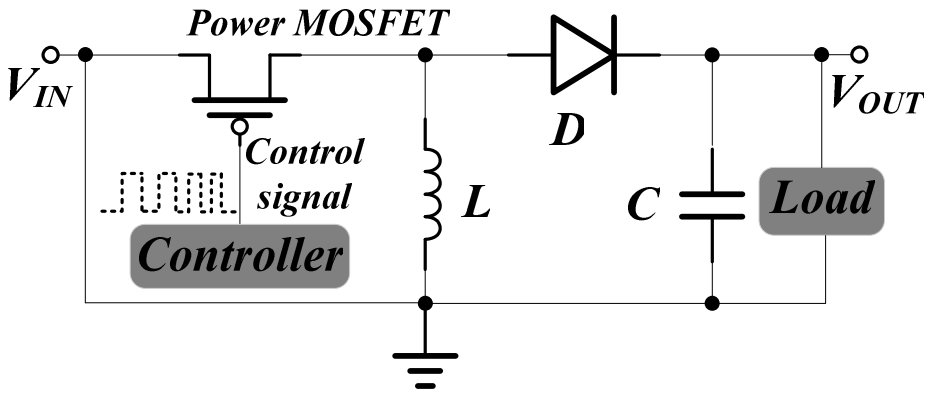
during one switching cycle.



(a) Buck type DC-DC converter



(a) Boost type DC-DC converter



(a) Buck-Boost type DC-DC converter

Fig. 6. Three basic topologies of DC-DC converter.

TABLE II. COMPARISONS OF CONVERTER TOPOLOGIES

Topology	*Buck converter*	*Boost converter*	*Buck-Boost converter*
Conversion Ratio	$\frac{V_{OUT}}{V_{IN}} = D$ ***(CCM)***	$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}$ ***(CCM)***	$\frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D}$ ***(CCM)***
Conversion Type	***Only Step-down***	***Only Step-up***	***D>0.5 doing Step-up*** ***D<0.5 doing Step-down***

2.2 Technologies of Controlling Modulator

Although the switching converter have high conversion efficiency, but at different load conditions the power will be wasted and result in efficiency reduction. The power consumption can be divided into three parts. The first part is the large current pass to power MOSFET, due to the pass of power MOSFET can be equaled to a resistor (R_{ON}), it will result to a power losses. This power consumption is also called conduction loss (P_{CON}) and express as follows:

$$P_{CON} = I_{OUT}^{2} R_{ON} \tag{1}$$

The second part is switching on and off alternately of the power MOSFET, as a results, the gate parasitic large capacitor of power MOSFET alternately charging and discharging. There is a big loss of the converter and this power consumption is also called switching loss (P_{SW}) and express as follows:

$$P_{SW} = (C_{GP} + C_{GN}) V_{IN}^{2} F_{SW} \tag{2}$$

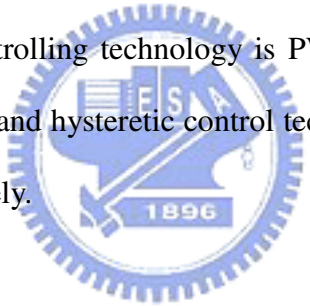
The C_{GP} and C_{GN} are represented as the gate parasitic capacitors of power PMOSFET and power NMOSFET respectively. V_{IN} is represented the input voltage and F_{SW} is represented the switching frequency. The final part is idle mode that is the condition of the converter operating in no loading. Although there is no load at output, but the converter still

can regulate the output voltage, this moment the current consumption of internal controller is called quiescent current. And the system power loss (P_{SYS}) is defined the multiplication of quiescent current and input voltage. The efficiency of DC-DC converter is defined the ratio of the output power and input power including the power loss can be expressed as follows.

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{P_{OUT}}{P_{OUT} + P_{SW} + P_{CON} + P_{SYS}} \times 100\% \quad (3)$$

As above-mentioned, the main power loss of heavy loading condition is P_{CON} because the large current will flow into the pass power MOSFET and generates larger power loss. Contrarily, the main power losses of light loading condition are P_{CON} and P_{SYS}, the solution to reduce power loss at light loading is decreases the frequency of control signal. The best way to increase efficiency is changes the control modulation.

The most three basic controlling technology is PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation) and hysteretic control technique which is introduced in section 2.2.1, 2.2.2 and 2.2.3 respectively.



2.2.1 Pulse Width Modulation (PWM)

Operating with PWM control, the power MOSFET are controlled by a constant clock cycle, the PWM control waveform is shown in Fig. 7 [5] [6]. While the ramp signal is lower than the control signal, the PWM signal at high level; the ramp signal is higher than the control signal, the PWM signal changes to low level. The main modulation is change the width of every clock cycle by the control signal and the output voltage is determined by the duty ratio of the PWM signal.

About the power consumption of Pulse Width Modulation focus on the conduction and switching loss, total power loss is expressed as follows.

$$P_{SW} + P_{CON} = {I_{OUT}}^2 R_{Duty} + (C_{GP} + C_{GN}){V_{IN}}^2 F_{SW} \quad (4)$$

As shown in Eq. 4, operating at PWM control the switching frequency is constant but output current varies with loading. That is to say, the switching loss is invariable with load but conduction loss will increase with the output loading, as shown in Fig. 8.

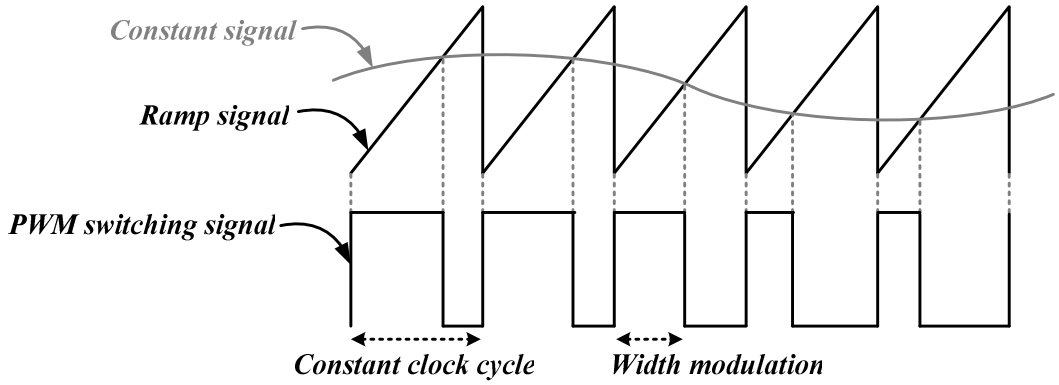


Fig. 7. Pulse-width modulation waveform.

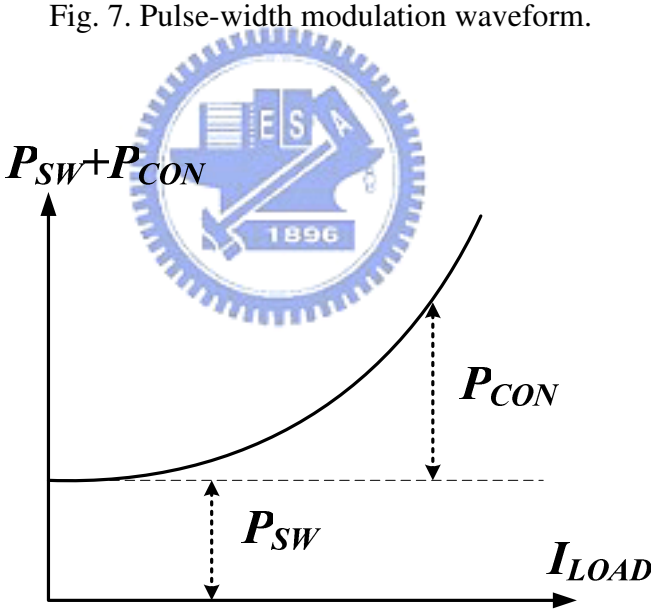


Fig. 8. Analysis of conduction loss and switching loss at Pulse-width modulation

2.2.2 Pulse Frequency Modulation (PFM)

Operating with PWM control, the power MOSFET are controlled by a vary frequency, the PFM control waveform is shown in Fig. 9[8] [9]. The on-time of PFM controller is constant width and off-time is variable with loading. By controlling the off-time of every

switching cycle can obtain different switching signal to achieve desirable output voltage. Therefore, the smaller output loading can reduce the switching frequency.

About the power consumption of Pulse Frequency Modulation also focus on the conduction and switching loss, total power loss is expressed as Eq. (4). Operating at PFM control both the switching frequency and output current varies with loading. That is to say, the switching loss and conduction loss will increase with the output loading, as shown in Fig. 10.

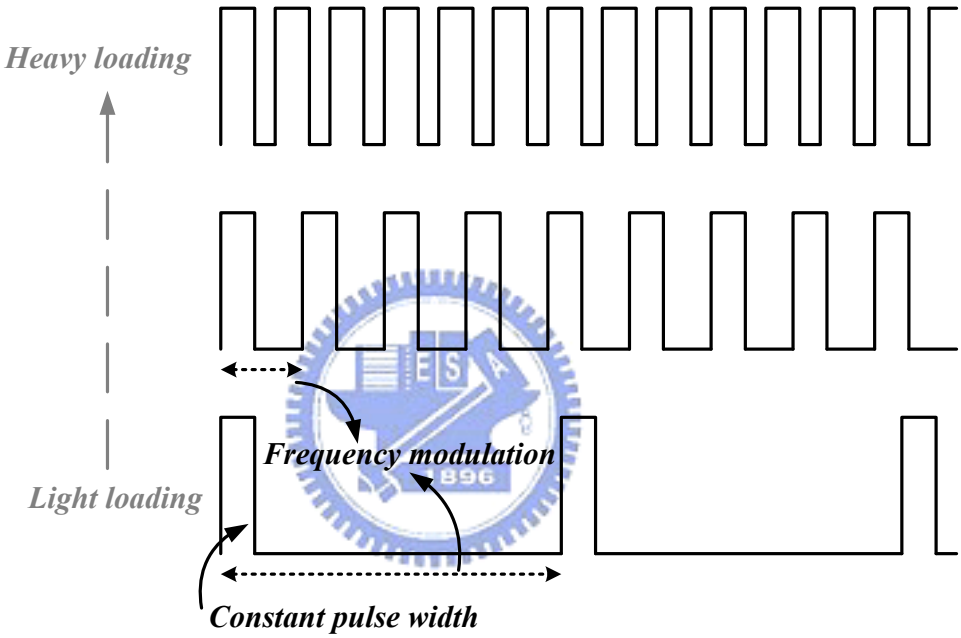


Fig. 9. Pulse-frequency modulation waveform.

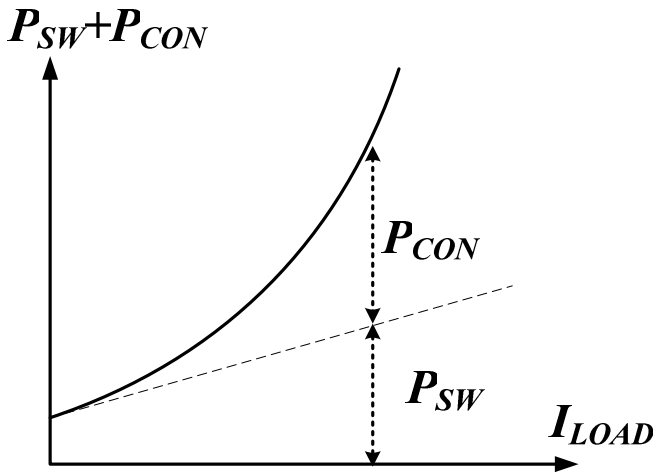


Fig. 10. Analysis of conduction loss and switching loss at Pulse frequency modulation

2.2.3 Hysteretic Control technique

The hysteretic controller is shown in Fig. 11[10], the main control method is generating a hysteresis window. By controlling the upper and lower boundary to regulate the output voltage, when the feedback voltage touch to the hysteretic upper boundary, the power NMOSPET will turn on and PMOSPET will turn off to discharge the inductor current and feedback voltage will decrease. At the same time, the hysteretic window will change to the lower boundary. While the feedback voltage touch to the hysteretic lower boundary, the power PMOSPET will turn on and the power NMOSPET will turn off to charge the inductor current and feedback voltage will increase. The hysteretic window which is calculating by superposition theorem can be expressed as follows.

$$V_H = V_{uppper} - V_{lower} = (V_{REF}\frac{R_2}{R_1+R_2} + V_{IN}\frac{R_1}{R_1+R_2}) - (V_{REF}\frac{R_2}{R_1+R_2}) = V_{IN}\frac{R_1}{R_1+R_2} \quad (5)$$

The features of hysteretic controller are described as follows; firstly, the main control circuit is comparator and the error amplifier does not be used, so it is no problem about system compensation. Secondly, without using any clock generator, the switching frequency of hysteretic controller is generated by system itself. The following is the calculation of

feedback voltage variation, as expressed as follows.

$$I = C\frac{dV}{dt} \Rightarrow \frac{V_{FBAVG} - 0}{R} = C\ \frac{\Delta V_{FB}}{t_{OFF}} \Rightarrow \Delta V_{FB} = \frac{t_{OFF} V_{FBAVG}}{RC} = \frac{DV_{IN}(1-D)T_0}{RC} \quad (6)$$

The voltage V_{FBAVG} is the average voltage of feedback, ideally is DV_{IN}, the parameter D the duty ratio of buck converter. Because the hysteresis window variation (V_H) equals to feedback voltage variation (ΔV_{FB}). Combining the Eq. (5) and Eq. (6), the switching frequency can as expressed as follows.

$$V_H = \Delta V_{FB} \Rightarrow V_{IN}\frac{R_1}{R_1 + R_2} = \frac{DV_{IN}(1-D)T_0}{RC} \Rightarrow f_0 = \frac{1}{T_0} = \frac{1}{RC}D(1-D)(1+\frac{R_2}{R_1}) \quad (7)$$

By controlling the resistor R, capacitor C and the ratio of resistors R_1 and R_2 can defined the switching frequency, its very suit for high switching frequency design. Finally, because the output ripple has been defined, it can't choose the low ESR capacitor to reduce output ripple.

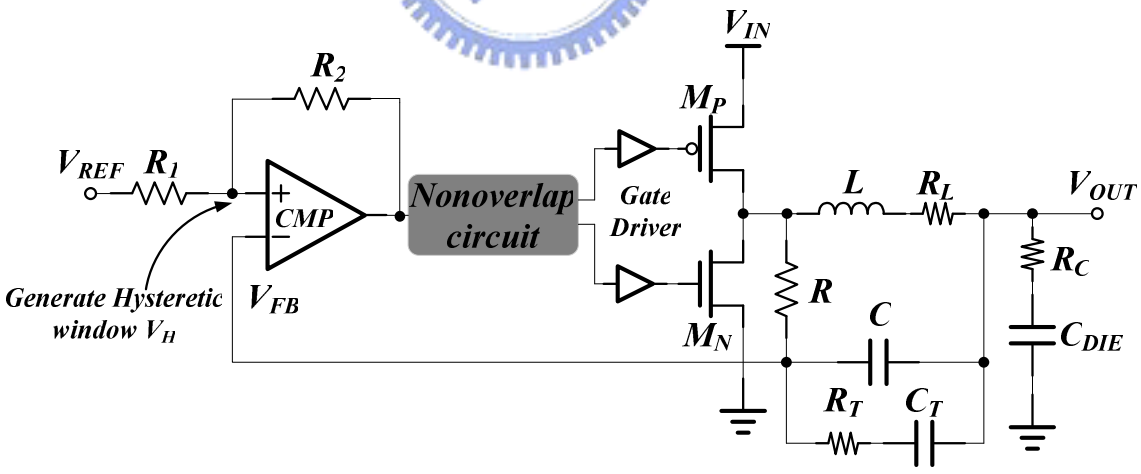


Fig. 11. The block diagram of Hysteretic control technique

2.3 The Theorem of Current Mode Control

The current mode control DC-DC converter has been used for thirty years and the characteristic is added another current loop of whole system to improve the performances of the converter. In other words, there is why the current mode control DC-DC converter hard to be analyzed because of dual-loop controlled. Therefore, the advantage of current-mode control DC-DC converter is providing better line and load regulation than voltage mode control. The complexity of current mode control DC-DC converter is adding the internal inductor current information as shown in Fig. 12 [5] [6].

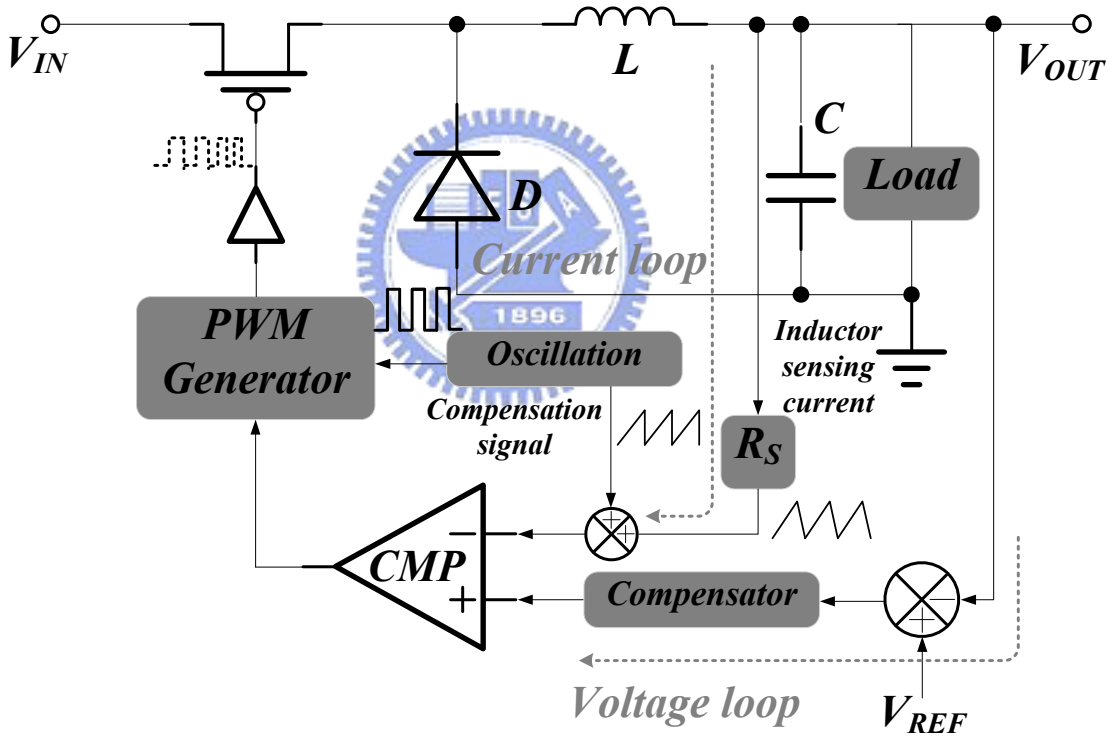


Fig. 12. The conventional current-mode buck converter

As shown in Fig. 12, the current mode control buck converter contains the external output voltage loop and internal current loop. Comparing to the voltage mode control, one of the advantages of current loop is improving the frequency response at AC analysis of the

switching regulator. That is to say, normally the conjugate pole of power stage resulting from the inductor and capacitor will be spilt by adding the current loop and the current mode controller only have one dominate pole at power stage. Not only it can increases the bandwidth of the system but also be compensated easily more than the voltage mode control.

In order to do current mode control, the current sensing and the ramp compensation will be included. The current sensing circuit is sensing the inductor current and size down the current order to compare to the voltage feedback control signal, than deciding the pulse width of every cycle. Because of the current mode control will cause the sub-harmonic oscillation, the ramp compensation is used to prevent this problem.

In this section, the detail current-mode buck converter's operation will be introduced in the Section 2.3.1. The reason why occur to sub-harmonic oscillation is discussed in the Section 2.3.2. To solve this problem, the Section 2.3.3 will describe the condition of ramp compensation. Finally, the CCM and DCM operation mode and small signal analysis for current mode buck switching regulator is shown in the Section 2.3.4 and the Section 2.3.4 respectively.

2.3.1 Operation Principles of Current Mode Buck Switching Regulator

The function blocks of current mode control DC-DC buck converter is shown in Fig. 13[5] [6] [11], the output voltage is dominated by the reference voltage (V_{REF}) which is generated from bandgap voltage reference. The whole system is controlled by the negative feedback loop, so the close loop gain of whole system must larger to result more precise regulation voltage.

The detail system operation is described as follows, at the beginning of the switching period, the power PMOSFET turned on and the power NMOSFET is turned off, this moment

the current from input source will flow through the power PMOSFET and inductor and will be sensed by the current sensing circuit. The current sense signal (V_{SENSE}) will add to the compensation ramp signal (V_{RAMP}) and the summation of two signals (V_{SUM}) will compare to the control signal (V_C) from the output of error amplifier. When the summation voltage signal higher than the control voltage signal, the comparator will change to low level then turn off the power PMOSFET and turn on power NMOSFET. The inductor of output will discharge the current to output capacitor and load. The next period will repeat the steps above mentioned. The operation of current mode controller just like a current source supplies a regulated current to the output. The total gain stage isn't affects the changing of input voltage, but will affect to voltage mode controller. That is why the line regulation of current mode controls better than voltage mode control.

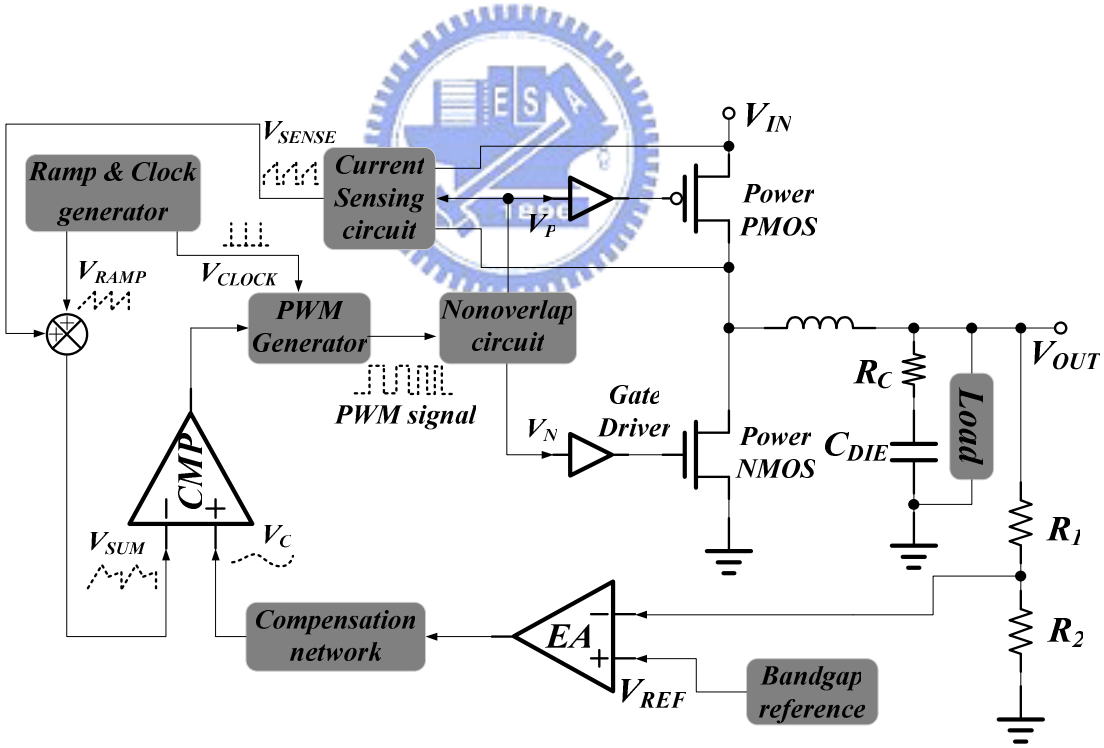


Fig. 13. The function blocks of the current-mode DC-DC buck converter

By the way, the function of the error amplifier not only increases the close loop gain but also generates the control signal to decide the pulse width signal of power switches. The

compensation network will create a pole-zero pair to do frequency compensation.

2.3.2 Sub-harmonic Oscillation at Duty Ratio > 0.5

The steady-state waveform and perturbed waveform are analyzed in Fig.14 [5] [12]. The beginning of perturbed error $i_L(0)$ can be expressed as the multiplication of the slope m_1 and the interval length $-dT_s$ by using the steady-state waveform. As the following express,

$$i_L(0) = -m_1 dT_s \tag{8}$$

In the same way, The end of perturbed error $i_L(Ts)$ can be expressed as the multiplication of the slope $-m_2$ and the interval length $-dT_s$.

$$i_L(T_s) = m_2 dT_s \tag{9}$$

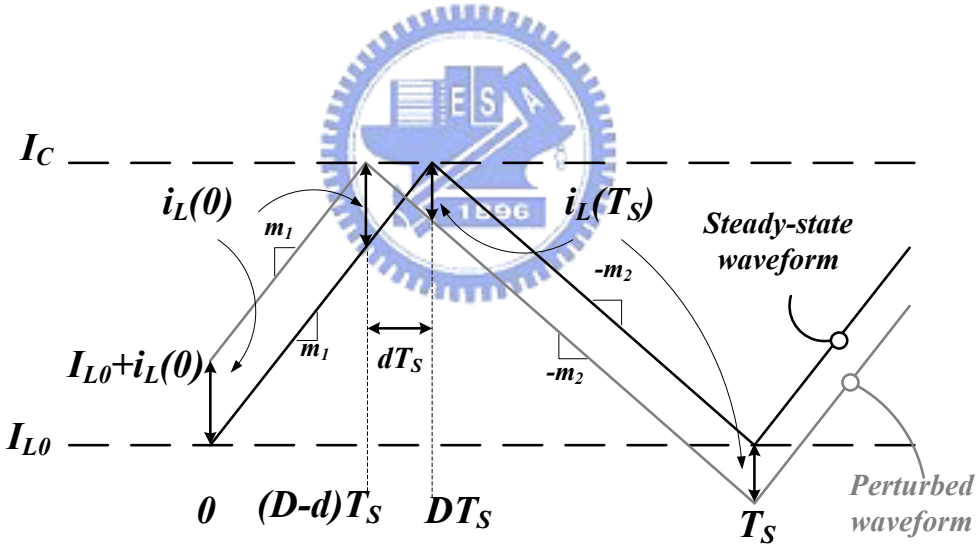


Fig. 14. Steady-state and perturbed Inductor Current Waveform

Elimination of the intermediate parameter dT_S from Eq. (8) and (9) will become

$$i_L(T_s) = i_L(0)\left(-\frac{m_2}{m_1}\right) = i_L(0)\left(-\frac{D}{D'}\right) \tag{10}$$

A similar analysis can be performed during the second switching period, the equation is presented as

$$i_L(2T_s) = i_L(T_s)\left(-\frac{D}{D'}\right) = i_L(0)\left(-\frac{D}{D'}\right)^2 \tag{11}$$

After n^{th} switching periods, the perturbation becomes

$$i_L(nT_s) = i_L((n-1)T_s)\left(-\frac{D}{D'}\right) = i_L(0)\left(-\frac{D}{D'}\right)^n \tag{12}$$

As shown in Eq. (12), when duty cycle smaller than 0.5 (***D<0.5***) over each switching period, the perturbations decrease in magnitude little by little. Therefore the disturbance of the inductor current will disappear after several switching periods. However the sub-harmonic oscillation will occur when the duty ratio is larger than 0.5 (***D>0.5***). The stable situation and unstable oscillation is shown in Fig. 15.

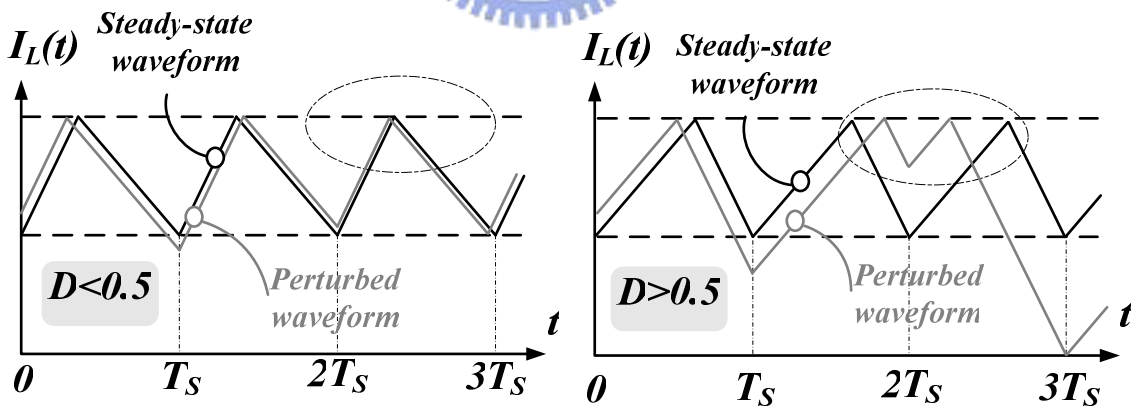


Fig. 15. The stable situation and unstable oscillation of inductor current

2.3.3 Ramp Compensation

The sub-harmonic oscillation of the current mode controlled converter is an inevasible problem, but as mentioned before, the converter of current mode control can be stable for all duty ratios by adding the compensation ramp to the sensed inductor current signal, as shown in Fig. 16 [5] [6]. The function of the compensated ramp can reduce the gain of the inner current sensing feedback loop in AC analysis to solve the unstable oscillation problem in the current mode controller DC-DC converter.

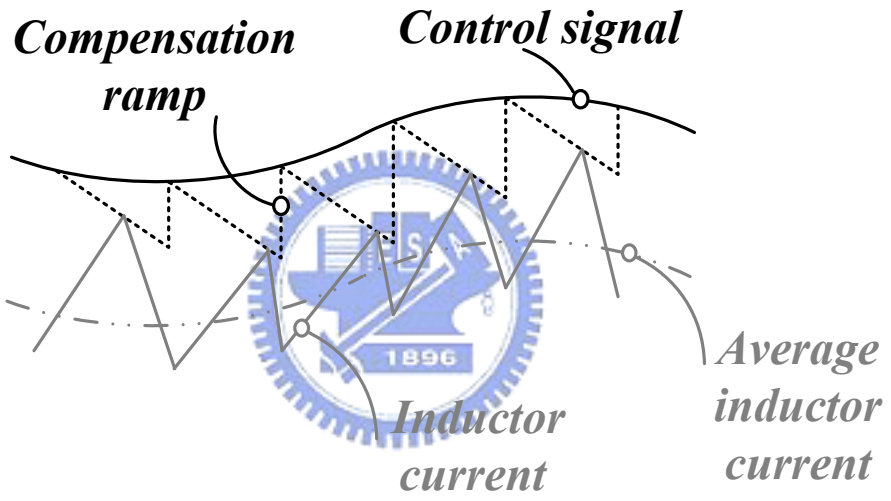


Fig. 16. Current-mode control signal with the compensation ramp and inductor current

The compensation theorem is presented in Fig.17, the beginning of perturbed error $i_L(0)$ and the end of perturbed error $i_L(T_s)$ are expressed in terms of the m_1, m_2, ma, and the $-dT_s$. As the following express,

$$i_L(0) = -dT_s\left(m_1 + m_a\right) \tag{13}$$

$$i_L(T_s) = -dT_s\left(m_a - m_2\right) \tag{14}$$

Elimination of the intermediate parameter dT_S from Eq. (13) and (14) will become

$$i_L(T_s) = i_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) \tag{15}$$

The same analysis can be used after n[th] period and leading to

$$i_L(nT_s) = i_L((n-1)T_s)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right) = i_L(0)\left(-\frac{m_2 - m_a}{m_1 + m_a}\right)^n = i_L(0)\alpha^n \tag{16}$$

For large n period, the perturbation $i_L(nT_s)$ will converge to zero provided that the characteristic value α has magnitude less than one. On the contrary, the perturbation $i_L(nT_s)$ will become large in magnitude when the characteristic value α has magnitude greater than one:

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a} = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}}$$
$$|i_L(nT_s)| \to 0 \ \ when \ |\alpha| < 1 \ ; \ |\alpha| \to \infty \ \ when \ \left|-\frac{D}{D'}\right| > 1 \tag{17}$$

The common choice of the compensation ramp slop is

$$m_a = \frac{1}{2} m_2 \tag{18}$$

This leads to the characteristic value α *equal to* -1 at the maximum duty ratio (***D= 1***), and the characteristic value α in absolute value must be smaller than one (***|α| < 1***) when operating in the normal duty ratio ***(0<D<1)*****.** That is to say, it will leads to stability for all duty ratio ***D*** as the Eq. (18) express,

$$m_a \geq \frac{1}{2} m_2 \tag{19}$$

Another common choice of the compensation ramp slop is

$$m_a = m_2 \tag{20}$$

The compensation ramp results in the characteristic value α to become zero for all duty

circle of the converter. For the reason, $i_L(T_s)$ is always to be zero for any $i_L(0)$ and the converter eliminates any one switching period that is called as deadbeat control.

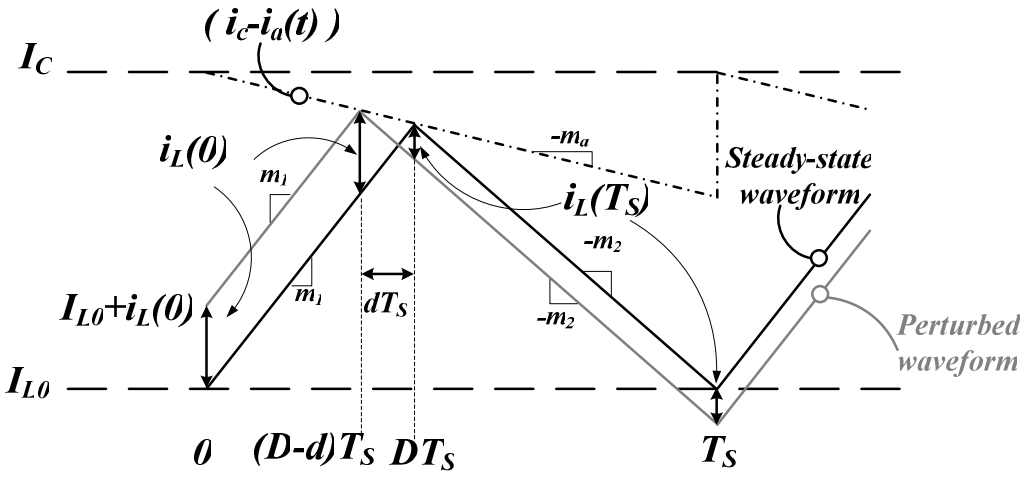


Fig. 17. Steady-state and perturbed inductor current waveforms with ramp compensation.

2.3.4 Continuous Conduction Mode (CCM) and Small Signal Modeling

The characteristic of continuous conduction mode (CCM) discussed in this section including the steady-state signal, the inductor current ripple and the output capacitor voltage then modeling the small signal [5].

When the output average current is larger than the half of inductor peak-to-peak ripple current, the voltage regulator is operated in CCM as shown in Fig. 18 [5]. Because during this mode the inductor current conducts continuously and the minimum current always larger than zero, this situation is usually happening in heavy load condition. For the reason, there are only two subintervals for DC-DC buck converter as shown in Fig. 19(a). Fig. 19(b) and (c) show the first subinterval and second subinterval respectively.

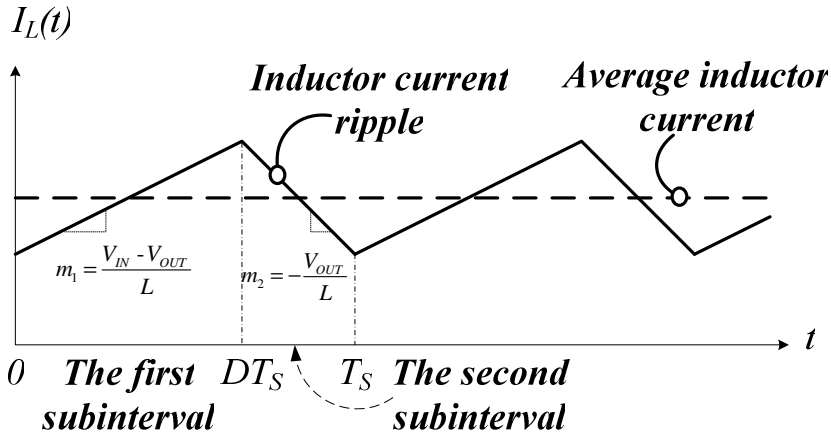


Fig. 18. The inductor and output current operates in continuous conduction mode.

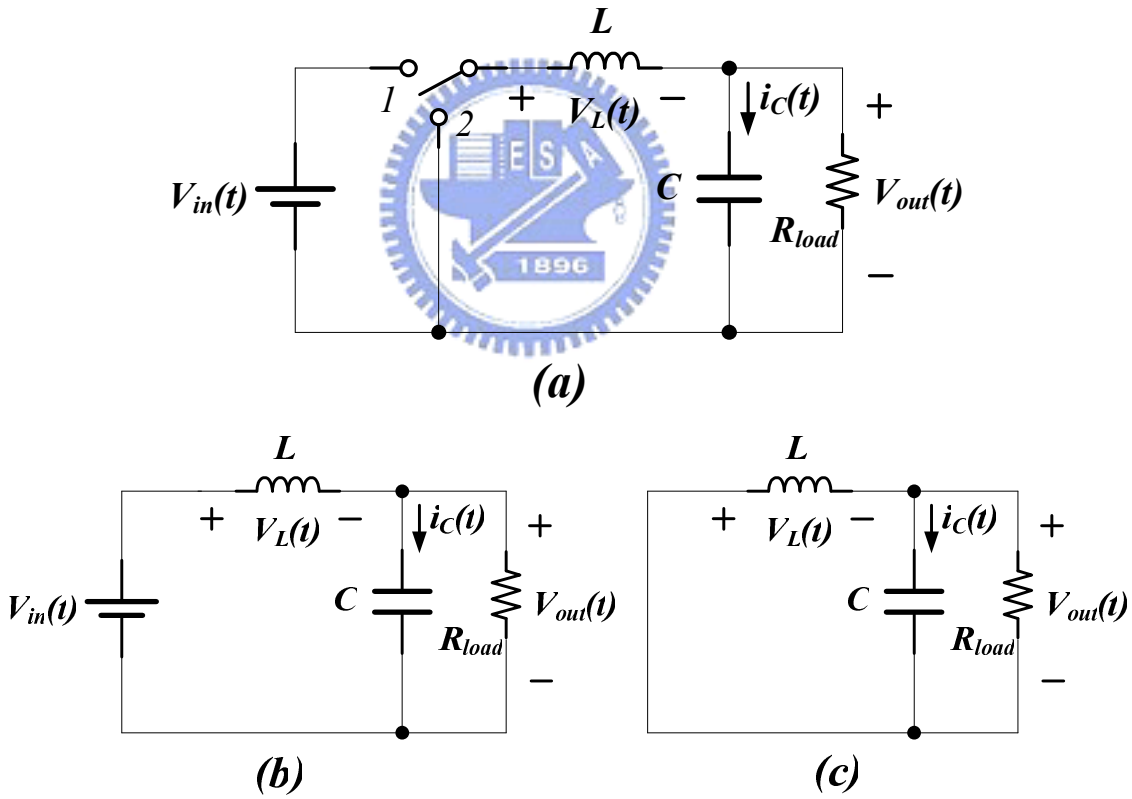


Fig. 19. The operating states in continuous conduction mode.

As shown in Fig. 19(b), the inductor voltage, capacitor current and the inductor current slope can be written as Eq. (21), (22) and (23) during the first subinterval. The resistor R_{load} is

the equivalent loading resistance.

$$V_L(t) = V_{IN}(t) - V_{OUT}(t) = L\frac{di_L}{dt} \tag{21}$$

$$I_C(t) = C\frac{dV}{dt} = I_L(t) - \frac{V_{OUT}(t)}{R_{load}} \tag{22}$$

$$m_1 = \frac{di_L}{dt} = \frac{V_L(t)}{L} = \frac{V_{IN}(t) - V_{OUT}(t)}{L} \tag{23}$$

As shown in Fig. 19(c), the inductor voltage, capacitor current and the inductor current slope can be written as Eq. (24), (25) and (26) during the second subinterval.

$$V_L(t) = -V_{OUT}(t) = L\frac{di_L}{dt} \tag{24}$$

$$I_C(t) = C\frac{dV}{dt} = I_L(t) - \frac{V_{OUT}(t)}{R_{load}} \tag{25}$$

$$m_2 = \frac{di_L}{dt} = \frac{V_L(t)}{L} = -\frac{V_{OUT}(t)}{L} \tag{26}$$

According to inductor voltage second balance, the voltage conversion ratio ***D*** is calculated as Eq. (27). The output voltage increases as conversion ratio ***D*** increasing, and ideal case tends to input voltage as ***D*** tends to one.

$$\left(V_{IN} - V_{OUT}\right)\cdot DT_s + \left(-V_{OUT}\right)\cdot\left(1-D\right)T_s = 0\ ,\ D = \frac{V_{out}}{V_{in}} = \frac{1}{D} \tag{27}$$

Finally, the inductor current ripple and capacitor voltage ripple can be written as Eq. (28) and Eq. (29) respectively.

$$\begin{aligned}&(\text{Changing in } i_L) = (\text{Slope } m_1)\cdot(\text{The first subinterval time } DT_S)\\ &\Rightarrow 2\Delta i_L = \frac{V_{IN} - V_{OUT}}{L}\cdot DT_S \Rightarrow \Delta i_L = \frac{V_{IN} - V_{OUT}}{2L}\cdot DTs\end{aligned} \tag{28}$$

$$\begin{aligned}&(\text{Changing in charge}) = (\text{Changing in voltage})\cdot(\text{Capacitor } C)\\ &\Rightarrow Q = \frac{1}{2}\Delta i_L\frac{Ts}{2} = 2\Delta V_{OUT}\cdot C \Rightarrow \Delta V_{OUT} = \frac{\Delta i_L T_S}{8C}\end{aligned} \tag{29}$$

The small signal modeling of CCM current mode buck converter only needs to model the average value of a length of switching period. Therefore, the switching ripple of inductor and capacitor must be ignored. For example, the average signal ***x(t)*** over an interval of length T_S can be calculated as $\langle X(t) \rangle_{T_S}$ is expressed as follows.

$$\left\langle X\left(t\right)\right\rangle_{T_S} = \frac{1}{T_S}\int_{t}^{t+T_S} x(\tau)d\tau \tag{30}$$

Hence the low frequency underlying ac variations of the inductor and capacitor waveforms can be model by equations of the form:

$$\left\langle V_L \right\rangle_{T_S} = \left[\left\langle V_{in} \right\rangle_{T_S} - \left\langle V_{out} \right\rangle_{T_S}\right] d(t) + \left[-\left\langle V_{out} \right\rangle_{T_S}\right] d'(t) \tag{31}$$

$$\left\langle i_C \right\rangle_{T_S} = \left[\left\langle i_L \right\rangle_{T_S} - \frac{\left\langle V_{out} \right\rangle_{T_S}}{R_{load}}\right] d(t) + \left[\left\langle i_L \right\rangle_{T_S} - \frac{\left\langle V_{out} \right\rangle_{T_S}}{R_{load}}\right] d'(t) \tag{32}$$

$$\left\langle i_{in} \right\rangle_{T_S} = \left\langle i_L \right\rangle_{T_S} d(t) \tag{33}$$

When the system operates at any transient, the average waveforms can be divided into corresponding quiescent values and the equivalent small ac variations which are shown in Eq. (34).

$$\begin{aligned}
\left\langle V_{in} \right\rangle_{T_S} &= V_{in} + \hat{v}_{in}(t) \\
\left\langle V_{out} \right\rangle_{T_S} &= V_{out} + \hat{v}_{out}(t) \\
\left\langle i_L \right\rangle_{T_S} &= I_L + \hat{i}_L(t) \\
\left\langle i_{in} \right\rangle_{T_S} &= I_{in} + \hat{i}_{in}(t) \\
d(t) &= D + \hat{d}(t)
\end{aligned} \tag{34}$$

The Eq. (31) ~ Eq. (33) cab be rewritten as Eq. (35), (36) and (37).

$$L\frac{d\left(I_L + \hat{i}_L\right)}{dt} = \left[V_{in} + \hat{v}_{in} - V_{out} - \hat{v}_{out}\right]\left(D + \hat{d}\right) + \left[-V_{out} - \hat{v}_{out}\right]\left(D' - \hat{d}\right) \tag{35}$$

$$C\frac{d\left(V_{out}+\hat{v}_{out}\right)}{dt}=\left[I_L+\hat{i}_L-\frac{V_{out}+\hat{v}_{out}}{R_{load}}\right]\left(D+\hat{d}\right)+\left[I_L+\hat{i}_L-\frac{V_{out}+\hat{v}_{out}}{R_{load}}\right]\left(D'-\hat{d}\right) \quad (36)$$

$$I_{in}+\hat{i}_{in}=\left(I_L+\hat{i}_L\right)\left(D+\hat{d}\right) \quad (37)$$

In order to get the linear system, the nonlinear ac terms must be neglected. That is to say, the second order nonlinear terms in magnitude of the equations above-mentioned are much smaller than the first order terms, so it can be ignored. And linear equation is given by

$$\begin{aligned}\hat{v}_L&=\hat{d}V_{in}+D\hat{v}_{in}-\hat{v}_{out}\\ \hat{i}_C&=\hat{i}_L-\frac{\hat{v}_{out}}{R_{load}}\\ \hat{i}_{in}&=I_L\hat{d}+D\hat{i}_L\end{aligned} \quad (38)$$

And the small signal ac equivalent circuit model can be built as Fig. 20.

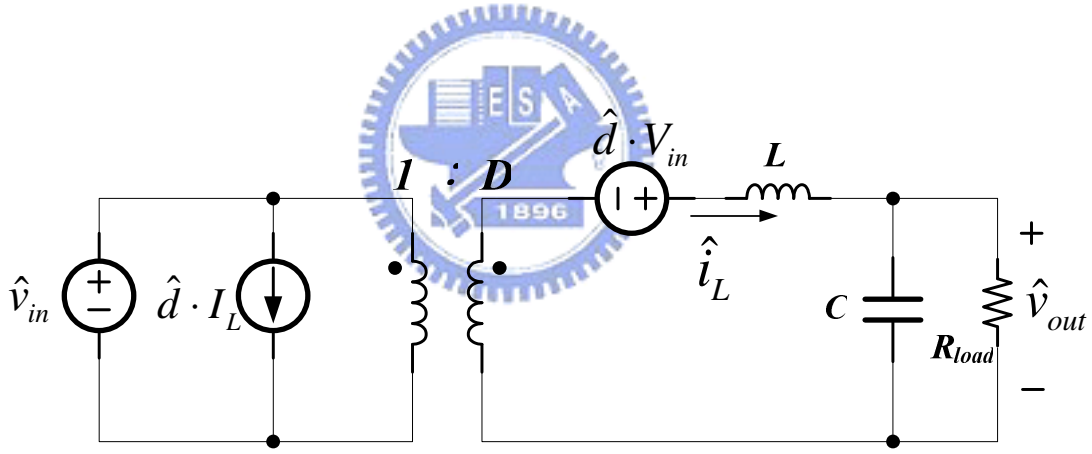


Fig. 20. The small signal ac equivalent circuit model of CCM condition.

According to Fig. 20, control-to-output transfer function could be obtained by

$$G_{vd}(s)=\left.\frac{\hat{v}_{out}(t)}{\hat{d}(t)}\right|_{\hat{v}_{in}(t)=0}=\frac{V_{out}}{D}\cdot\frac{1}{1+\frac{S}{Q\cdot\omega_0}+\left(\frac{S}{\omega_0}\right)^2},\quad Q=R_{load}\sqrt{\frac{C}{L}},\quad \omega_0=\frac{1}{\sqrt{LC}} \quad (39)$$

Line-to-output transfer function could be obtained by

$$G_{vg}(s)=\left.\frac{\hat{v}_{out}(t)}{\hat{v}_{in}(t)}\right|_{\hat{d}(t)=0}=D\cdot\frac{1}{1+\frac{S}{Q\cdot\omega_0}+\left(\frac{S}{\omega_0}\right)^2},\quad Q=R_{load}\sqrt{\frac{C}{L}},\quad \omega_0=\frac{1}{\sqrt{LC}} \tag{40}$$

2.3.5 Discontinuous Conduction Mode (DCM) and Small Signal Modeling

The characteristic of discontinuous conduction mode (DCM) discussed in this section including the steady-state signal, the inductor current ripple and the output capacitor voltage then modeling the small signal [5]. When the output average current is smaller than the half of inductor peak-to-peak ripple current, the voltage regulator is operated in DCM as shown in Fig. 21[5]. Because during this mode the inductor current conducts discontinuously and the minimum current is equal to zero, this situation is usually happening in light load condition. For the reason, there are three subintervals for DC-DC buck converter, the first and the second subinterval structures are the same as in Fig. 19(b) and the Fig. 19(c) respectively. The additional third subinterval for DC-DC converter is shown in Fig. 22.

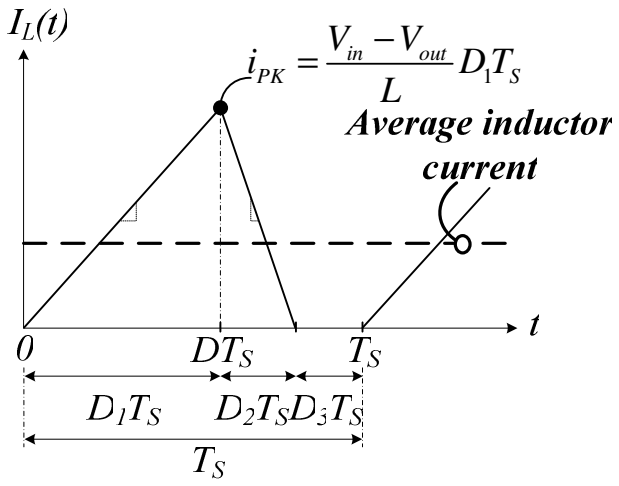


Fig. 21. The inductor and output current operates in discontinuous conduction mode.

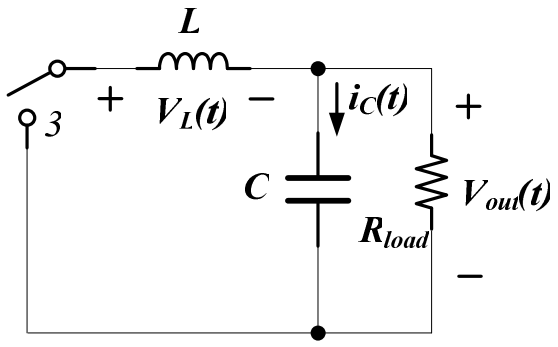


Fig. 22. The third subinterval of discontinuous conduction mode.

As shown in Fig. 21, the DCM operation can divided into three subintervals, the three symbols D_1, D_2, and D_3 is defined during one switching cycle. The inductor voltage, capacitor current and the inductor current slope equations of the first and the two subintervals are shown in Eq. (21) ~ (26). The third subinterval is happening while the power PMOSFET and he power NMOSFET are both turn off, the energy stored in output capacitor discharges to output load and the descriptions are written in Eq. (41)

$$V_L = 0,\ i_C = -\frac{V_{out}}{R_{load}},\ m_3 = 0 \tag{41}$$

According to inductor voltage second balance, the voltage conversion ratio D is calculated as Eq. (42).

$$\left(V_{in} - V_{out}\right)\cdot D_1 T_s \ + \ \left(-V_{out}\right)\cdot D_2 T_s \ + \ 0\cdot D_3 T_S = 0\ ,\ D = \frac{V_{out}}{V_{in}} = \frac{D_1}{D_1 + D_2} \tag{42}$$

D_1 is conversion ratio and D_2 need to obtain by inductor current as calculate in Eq. (43) and Eq. (44).

$$i_L(D_1 T_S) = i_{PK} = \frac{V_{in} - V_{out}}{L} D_1 T_S \tag{43}$$

$$\langle i_L \rangle = \frac{1}{T_S}\int_0^{T_S} i_L(t)dt = \frac{1}{2}(D_1 + D_2)T_S \cdot i_{PK} \tag{44}$$

Combination the Eq. (43) and Eq. (44) can obtain Eq. (45).

$$\langle i_L \rangle = \frac{V_{out}}{R_{load}} = (V_{in} - V_{out}) \cdot \left(\frac{D_1 T_S}{2L}\right)(D_1 + D_2) \tag{45}$$

And the Eq. (42) can be translated as follows.

$$D_1 + D_2 = \frac{V_{in}}{V_{out}} D_1 \tag{46}$$

Combination the Eq. (45) and Eq. (46) can obtain Eq. (47).

$$\frac{V_{out}}{R_{load}} = (V_{in} - V_{out}) \cdot \left(\frac{D_1 T_S}{2L}\right) \cdot \left(\frac{V_{in}}{V_{out}} D_1\right) \tag{47}$$

After calculation the relation between input voltage and output voltage can be expressed as follows.

$$\frac{V_{out}}{V_{in}} = \frac{2D_1}{D_1 + \sqrt{D_1^2 + \left(\frac{8L}{R_{load} T_S}\right)}} \tag{48}$$

As shown in Eq. (48), when the DC-DC converter operated in discontinuous Conduction Mode, input voltage and output voltage are not only relating to duty ratio but also in relationship with inductor value, switching frequency and output equivalent loading resistance.

The small signal model of DCM operation for buck converter can use the similar method as CCM operation. Symbols v_1, v_2, i_1 and i_2 are assumed to be the terminal voltages and currents of switching network as illustrated in Fig. 23.

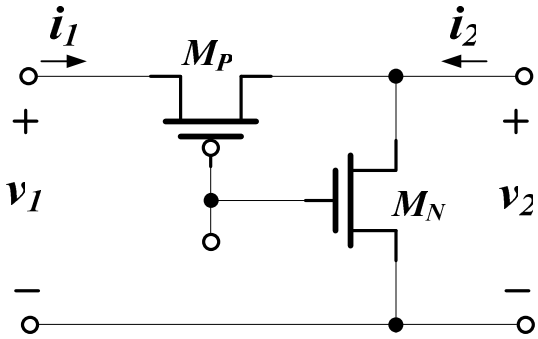


Fig. 23. Definition of terminal quantities of the buck switch network.

The symbols v_1, v_2, i_1 and i_2 can be obtained by using the average signal switching model as expressed as follows.

$$\langle i_1 \rangle_{T_S} = \frac{\frac{1}{2} i_{PK} d_1 T_s}{Ts} = d_1^2 T \frac{\langle V_{IN} \rangle_{T_S} - \langle V_{OUT} \rangle_{T_S}}{2L} \tag{49}$$

$$\langle i_2 \rangle_{T_S} = \frac{\frac{1}{2} i_{PK} (d_1 + d_2) T_s}{Ts} = d_1 (d_1 + d_2) \frac{\langle V_{IN} \rangle_{T_S} - \langle V_{OUT} \rangle_{T_S}}{2L} \tag{50}$$

$$\langle v_1 \rangle_{T_S} = \langle V_{IN} \rangle_{T_S} \tag{51}$$

$$\langle v_2 \rangle_{T_S} = d_1 \langle V_{IN} \rangle_{T_S} + d_3 \langle V_{OUT} \rangle_{T_S} \tag{52}$$

The average waveforms can be divided into corresponding quiescent values and the equivalent small ac variations, the small signal including the first order linear part and the second order nonlinear part. In order to obtain better linearity part, the Eq. (49) ~ (52) must be done partial differentiations and get the small signal model parameters, as calculated in Eq. (53) ~ (58). And the small signal ac equivalent circuit model of DCM condition is shown in Fig. 24.

$$\frac{1}{r_1} = \left. \frac{\partial f(v_1, V_2, D)}{\partial v_1} \right|_{v_1 = V_1} = D^2 T_S \frac{1}{2L} \tag{53}$$

$$g_1 = \left.\frac{\partial f(V_1, v_2, D)}{\partial v_2}\right|_{v_2=V_2} = -D^2 T_S \frac{1}{2L} \tag{54}$$

$$j_1 = \left.\frac{\partial f(V_1, V_2, d)}{\partial d}\right|_{d=D} = 2DT_S \frac{V_1 - V_2}{2L} \tag{55}$$

$$\frac{1}{r_2} = -\left.\frac{\partial f(V_1, v_2, D)}{\partial v_2}\right|_{v_2=V_2} = \frac{D^2 T_S}{2L} \frac{V_1^2}{V_2^2} \tag{56}$$

$$g_2 = \left.\frac{\partial f(v_1, V_2, D)}{\partial v_1}\right|_{v_1=V_1} = \frac{D^2 T_S}{2L} \frac{2V_1 - V_2}{V_2^2} \tag{57}$$

$$j_2 = \left.\frac{\partial f(V_1, V_2, d)}{\partial d}\right|_{d=D} = \frac{DT_S}{L}\left(\frac{V_1^2}{V_2} - V_1\right) \tag{58}$$

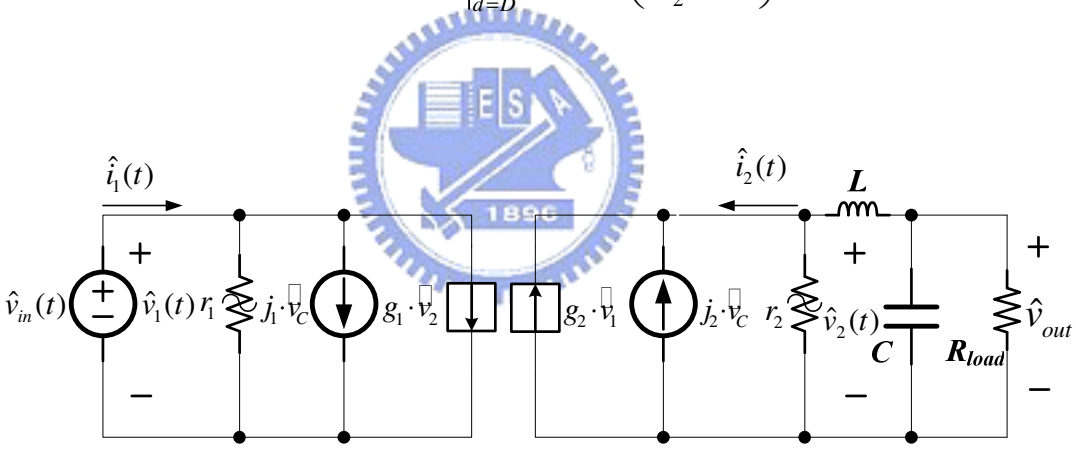


Fig. 24. The small signal ac equivalent circuit model of DCM condition.

According to Fig. 24, control-to-output transfer function in DCM could be obtained by

$$G_{vc\_DCM}(t) = \left.\frac{\hat{v}_{out}(t)}{\hat{v}_c(t)}\right|_{\hat{v}_{in}(t)=0} = \frac{j_2(R_{load} // r_2)}{1 + C(R_{load} // r_2)S} \tag{59}$$

Line-to-output transfer function in DCM could be obtained by

$$G_{vg\_DCM}(t) = \left.\frac{\hat{v}_{out}(t)}{\hat{v}_{in}(t)}\right|_{\hat{v}_c(t)=0} = \frac{g_2(R_{load} // r_2)}{1 + C(R_{load} // r_2)S} \tag{60}$$

2.4 Important Specifications of Switching Converter

Due to more and more electronics application need to be supplied by switching converter, the performances of switching converter have to consideration. The most specifications must be care about can be listed in the parts. Firstly, the conversion efficiency of switching converter is an important topic, how to keep high efficiency over wide loading range will discuss in the section 2.4.1. The second part is excellent load and line regulation, the lower steady-state error of switching regulator will discuss in the section 2.4.2. The final part is transient response, how to immediately response when the sudden large current changing will shown in the section 2.4.3.

2.4.1 Efficiency

The definition of switching converter is the ratio of input power and output power and can be wrote as

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \times 100\% \quad (61)$$

The detail power losses and the operation range of control modulator have been shown in the section 2.2. Overall saying, the pulse width modulation (PWM) mode is suit for operating in heavy load condition, and the pulse frequency modulation (PFM) is suit for operating in light load condition. If the switching converter operating only one module mode, take cell phone for example, the cell phone system operates in standby mode and many blocks of system doesn't work, at light load condition but the converter only have PWM controller, as a result, the battery lifetime will reduce quickly. Hence, the best way to improve the efficiency is including the pulse frequency modulation (PFM) to control at light load condition. By dual mode control can keep high efficiency over wide load range. The comparison of PWM and PFM control technique will be listed in TABLE III.

TABLE III. COMPARISONS BETWEEN PWM AND PFM CONTROL

Features	*Pulse Width Modulation*	*Pulse Frequency Modulation*
Well Efficiency Range	***Moderate to heavy load***	***Light load***
Frequency	***Constant***	***Variable***
Switching Loss of whole loading	***Constant***	***The larger loading, the heavier loss***
Output Ripple	***Smaller***	***Larger***
Transient Response	***Faster***	***Slower***
Circuit Complexity	***Complicated***	***Simple***
Quiescent Current	***Larger***	***lower***

2.4.2 Load and Line Regulation

Switching converters are powerful system of stepping up or down the desires voltage. Therefore, to keep the regulated voltage and decrease the steady state error when increasing the supply voltage and load condition of DC-DC converter is most important.

The load regulation is defined as the percentage of steady state error of output voltage when the load condition changes and can be calculated as follows.

$$\text{Load Regulation} = \frac{\Delta V_{out}}{V_{out\_norm}} . \frac{100}{\Delta I_{load}} \left(\frac{\%}{mA} \right) \tag{62}$$

The line regulation is defined as the percentage of steady state error of output voltage when the input voltage changes and can be calculated as follows.

$$\text{Line Regulation} = \frac{\Delta V_{out}}{V_{out\_norm}} . \frac{100}{\Delta V_{IN}} \left(\frac{\%}{mV} \right) \tag{63}$$

2.4.3 Transient Response

The transient response is an important specification of DC-DC converter for the system applications. The large load current changes suddenly will cause a voltage fluctuation at output of DC-DC converter. The voltage fluctuation may trigger the logic circuit or affect the analog circuit. Therefore, it's important to reduce the large voltage changing and the time during voltage variation. The transient response of output voltage relates to load current is shown in Fig. 25. During the first period Δt_1, the large current flow into the output load from DC-DC converter, due to the DC-DC converter cannot provide enough energy to maintain the output voltage, the output voltage will drop in this period because the output capacitor discharges the energy to support the load current. The drop voltage is shown in Eq. (64). According to the parameters of Eq. (64), selecting the output capacitor well can reduce the drop in this period.

$$V_{drop1} = V_{drop2} = \Delta I_{out} \times \left(\frac{\Delta t_1}{C_{out}} + R_{ESR} \right) \tag{64}$$

During the second period Δt_2, the system senses the output variation by feedback loop then turn on the power PMOSFET to recover the regulated output voltage. The sum of Δt_1 and Δt_2 is called the recovery time and the second period Δt_2 depends on the system bandwidth of the DC-DC converter

The static error ΔV_{OUT} between light load and heavy load is relates to the voltage regulator DC gain, the higher DC gain bringing the better load regulation [13]. Comparing to the Fig. 25(b) and Fig. 25(c), the performance of Fig. 25(b) due to the large DC gain and causes the better load regulation, but the second period Δt_2 extend the recovery time. However, it reduces the time of transient response. The performances of Fig. 25(c) due to the poor DC gain and cause huge static error but reduce the time of second period Δt_2 and improve the dynamic performance.

When the load current is decreasing to light load suddenly, the output voltage will jump until the DC-DC converter start to recovery the regulated voltage. The redundant current charges the output capacitor resulting to a peak voltage as shown in shown in Eq. (65) before the feedback loop of DC-DC converter react.

$$V_{peak1} = V_{peak2} = \Delta I_{out} \times \left(\frac{\Delta t_3}{C_{out}} + R_{ESR} \right) \tag{65}$$

During the final period Δt_4 the output capacitor discharged the redundant current to feedback resistors. As mention described, the transient response is relates to the bandwidth of DC-DC converter, output capacitor, equivalent series resistance (R_{ESR}) of output voltage and the load current.

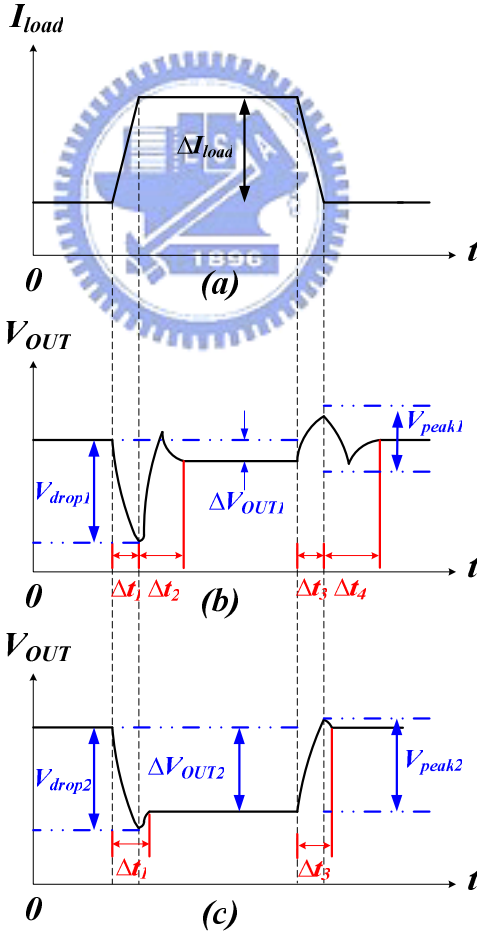


Fig. 25. The transient response of output voltage relates to load current.

Chapter 3

Structure of 20MHz Current Domain DC-DC Buck Converter

In this Chapter, the system architecture of current domain DC-DC buck converter will be introduced. The drawbacks of prior conventional current mode buck converter operating at switching frequency 20MHz and the modifications of proposed current domain buck converter are discussed in the section 3.1. The small signal analysis of current domain 20MHz buck converter and the compensation scheme are shown in the section 3.2. Then, the soft start technique at start up duration is shown in the section 3.3. Finally, the output stage inductor and capacitor selection are discussed in the section 3.4.

3.1 Proposed Current Domain 20MHz Buck Converter

3.1.1 Prior Art Conventional Current Mode Buck Converter

Fig. 26 illustrates the conventional current mode DC-DC buck converter. The detail system operation has been explained in the section 2.3.1. The conventional structure is very suit for normal operation frequency such as the range from 0.1MHz to 1MHz. The sub-circuits operation delay can be neglected due to longer switching period. But the output passive components including inductor and capacitor must be chosen larger value and be placed off-chip. In order to integrate the inductor into chip, increasing switching frequency is the most straightforward method because current ripple decreases with increasing frequency,

which means, in keeping the same ripple variation; a smaller inductor may be used at higher frequency.

When operating at switching frequency 20MHz, the disadvantages of conventional current mode buck converter will be emerged. Firstly, the output transformative time of voltage comparator form high to low or verse vice must be response as quick as possible. Or the delay may cause system output voltage oscillation or unstable. To achieve high speed voltage comparison, the quiescent current of voltage comparator has to increase at least five times larger than normal operation frequency. Secondly, the PWM control signal is generated by the summation of current sensing voltage V_{SENSE} and artificial ramp voltage V_{RAMP} compare to error voltage V_C. To obtain voltage V_{SUM}, the voltage V_{RAMP} and V_{SENSE} has to pass through the block of voltage to current converter (*V to I converter*) respectively, then the current flow into the resistor R_{SUM}. This procedure not only may cause unnecessary operative delay but also the voltage to current converter cannot get the correct current due to high switching frequency. To avoid the unnecessary delay affecting system stability and operation speed, the current domain 20MHz buck converter is shown in next section.

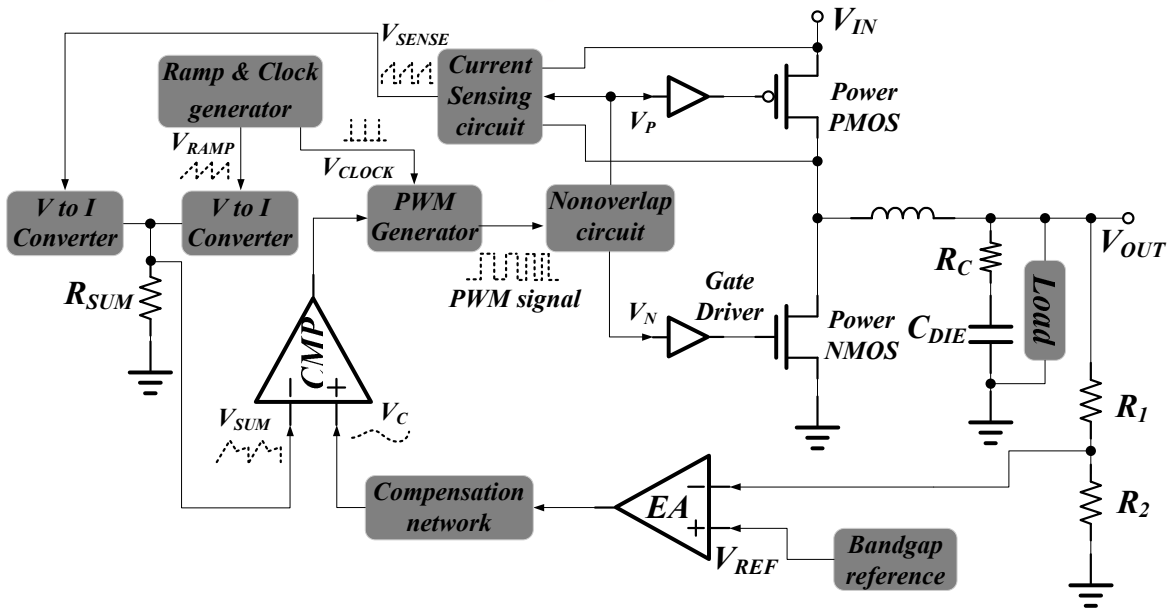


Fig. 26. The structure of conventional current mode DC-DC buck converter.

3.1.2 Current Domain 20MHz Buck Converter

The modified current domain 20MHz buck converter is shown in Fig. 27 [14]. The power stage is containing complementary power MOSFET pair, integration inductor and output capacitor. The external sensing resistor R_{SENSE} is needed to sense the current variance during power PMOSFET turns on. A resistive divider R1 and R2 are the purpose of detecting and scaling down the output variation and DC level. Different from the conventional current mode buck converter, the error GM amplifier compares the error voltage between reference voltage V_{REF} and feedback voltage V_{FB} then transforms into error current I_{ERROR}. The error current I_{ERROR}, the artificial ramp current I_{RAMP} and current sensing current I_{SENSE} are summed in the same node in current domain. Then the current comparator modulates the analog current signal to digital control signal, that is to say, when the input current of current comparator is smaller than zero, the output voltage of current comparator is logic low. On the contrary, as current above the zero, the output voltage of current comparator is logic high. The current domain PWM modulator determines the duty ratio to control the on-time and off-time duration of complementary power MOSFET pair. Finally, the negative feedback will achieve to regulated output voltage.

The advantages of current domain buck converter operating at switching frequency 20MHz are described as follows [15]. Firstly, the operation delay time of current comparator is shorter than voltage comparator in the same quiescent current condition. It's benefit to be used in 20MHz switching frequency. Secondly, the complexity of control circuits can be reduced because the summation of ramp and current sensing signals can be mixed directly. To sum up, comparing with current signal not only simplify the design but also increasing the operation frequency. Finally, the structure of current domain buck converter doesn't need extra compensation passive components; it can reduce external pin of whole chip. That's why choosing current domain PWM control mode to increase switching frequency upon to

20MHz.

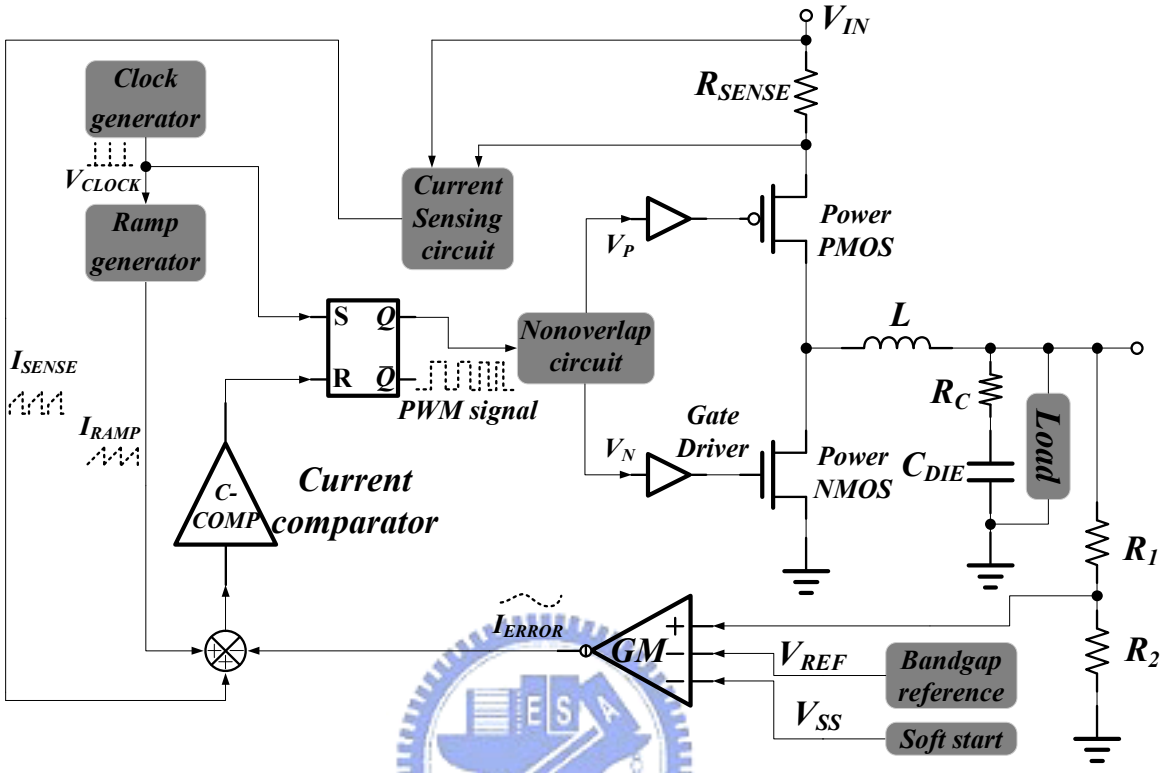


Fig. 27. The structure of modified current domain 20MHz buck converter.

3.2 Small Signal Analysis and Compensation Scheme of Current Domain DC-DC Buck Converter

In this part, the small signal analysis of current domain DC-DC buck converter is shown in the section 3.2.1, then the compensation scheme is described in the Section 3.2.2 and section 3.2.3, which shows the prior art and proposed architecture respectively.

3.2.1 Small Signal Analysis [5]

The small signal analysis of buck switching converter has been mentioned in the section 2.3.4, the control method only consider the duty variation. In order to model the dual control loop current domain DC-DC buck converter, the relationship between the control signal $i_c(t)$

and duty cycle ***d(t)*** must be found and combined to the buck mode small signal model.

Also take CCM operation for example, the relationship between control signal $i_c(t)$ and sensing current signal $i_{cs}(t)$ are illustrated in Fig. 28, where the m_1 and m_2 is the slope of inductor current, α is the current sensing gain and m_a is the slope of compensation ramp.

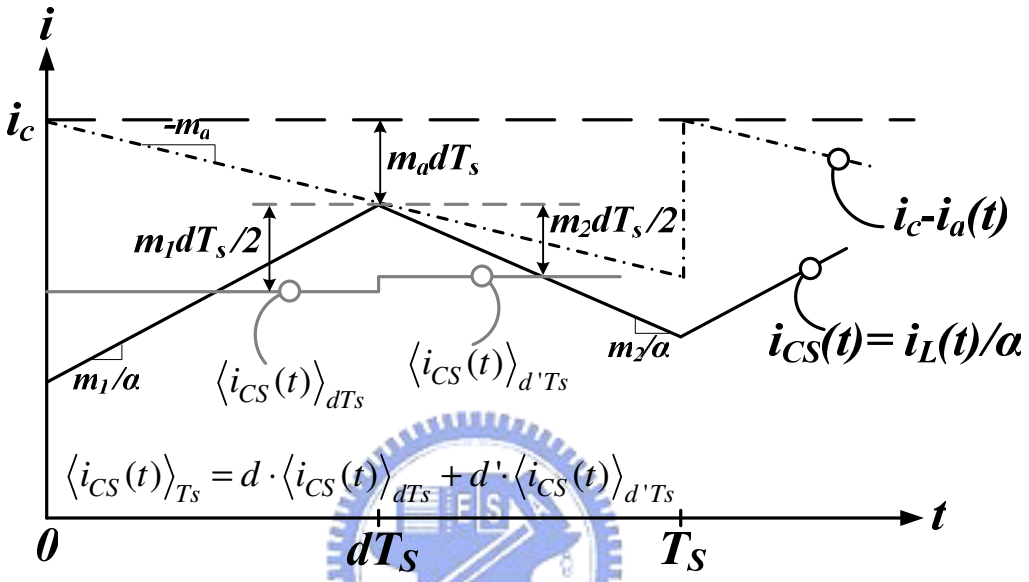


Fig. 28.The relationship between sensing inductor current $i_{cs}(t)$ and control current $i_c(t)$.

According to the Fig. 28, the average value of current sensing is expressed as follows.

$$\begin{aligned}\langle i_{CS}(t)\rangle_{Ts} &= d\cdot\langle i_{CS}(t)\rangle_{dTs} + d'\cdot\langle i_{CS}(t)\rangle_{d'Ts} \\ &= \langle i_c(t)\rangle_{T_s} - m_a dT_s - d\frac{m_1 dT_s}{2\alpha} - d'\frac{m_2 d'T_s}{2\alpha}\end{aligned} \tag{66}$$

Ac variations are added in i_{cs}, i_c, d, m_1, and m_2. Let

$$\begin{aligned}\langle i_{cs}(t)\rangle_{T_s} &= i_{cs} + \hat{i}_{cs}(t) \\ \langle i_c(t)\rangle_{T_s} &= i_c + \hat{i}_c(t) \\ d(t) &= D + \hat{d}(t) \\ m_1(t) &= M_1 + \hat{m}_1(t) \\ m_2(t) &= M_2 + \hat{m}_2(t)\end{aligned} \tag{67}$$

And for buck converter, the slope variations can be given by

$$\hat{m}_1 = \frac{\hat{v}_{in} - \hat{v}_{out}}{L}$$
$$\hat{m}_2 = \frac{\hat{v}_{out}}{L} \tag{68}$$

Assumed that $\boldsymbol{m_a}$ is constant value. Substitution of Eq. (67) into Eq. (66) and approximating the first order ac terms leads to

$$\hat{i}_{cs}(t) = \hat{i}_c(t) - \left(m_a T_s + M_1 D T_s/\alpha - M_2 D' T_s/\alpha\right)\hat{d}(t) - \frac{D^2 T_s}{2\alpha}\hat{m}_1(t) - \frac{D'^2 T_s}{2\alpha}\hat{m}_2(t) \tag{69}$$

With use of the equilibrium relationship $\boldsymbol{DM_1=D'M_2}$, finally the relationship between the control signal and duty cycle is shown as below

$$\begin{aligned}
&\hat{i}_L(t) = \alpha\hat{i}_{cs}(t) \cong \alpha\hat{i}_c(t) - \alpha m_a T_s \hat{d}(t) - \frac{D^2 T_S}{2}\hat{m}_1(t) - \frac{D'^2 T_S}{2}\hat{m}_2(t) \\
&\Rightarrow \hat{d}(t) = \frac{1}{\alpha M_a T_s}\left[\alpha\hat{i}_c(t) - \hat{i}_L(t) - \frac{D^2 T_S}{2}\hat{m}_1(t) - \frac{D'^2 T_S}{2}\hat{m}_2(t)\right] \\
&\quad = \frac{1}{\alpha m_a T_s}\left[\alpha\hat{i}_c(t) - \hat{i}_L(t) - \frac{D^2 T_s}{2L}\hat{v}_{in}(t) - \frac{(1-2D)T_s}{2L}\hat{v}_{out}(t)\right]
\end{aligned} \tag{70}$$

In order to simplicity, the Eq. (70) is shown on the above can be rewritten as Eq. (71).

$$\hat{d}(t) = F_m\left[F_c\hat{i}_c(t) - \hat{i}_L(t) - F_i\hat{v}_{in}(t) - F_o\hat{v}_{out}(t)\right]$$
$$F_m = \frac{1}{\alpha M_a T_s}$$
$$F_c = \alpha \tag{71}$$
$$F_i = \frac{D^2}{2L}T_S$$
$$F_o = \frac{(1-2D)T_S}{2L}$$

The current domain dc-dc buck converter model can be obtained, by combine the

controller block with power stage small signal model, as shown in Fig. 29.

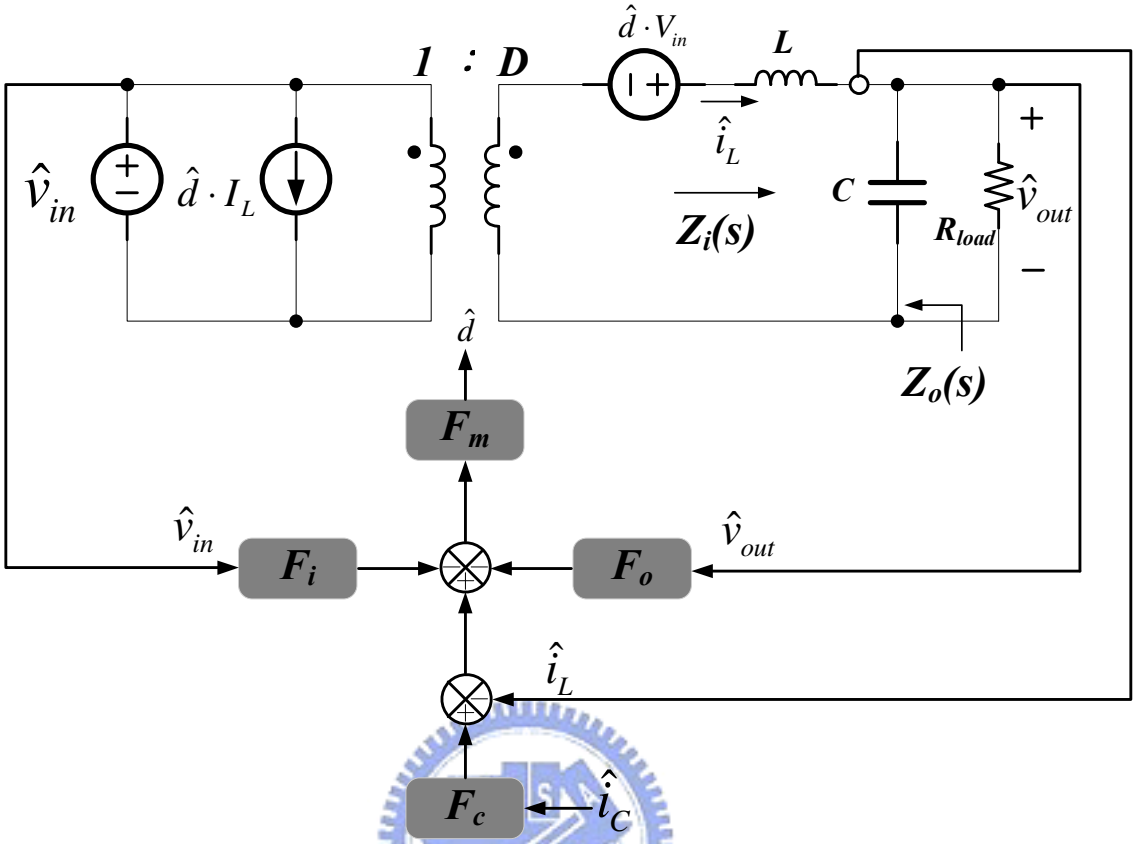


Fig. 29. Small signal model of current domain dc-dc buck converter

Let $\boldsymbol{Z_o(s)}$ is the power stage open-loop output impedance. $\mathbf{Z_i(s)}$ is the input impedance of energy-storage elements.

$$Z_o(s) = \frac{\hat{v}_{out}}{\hat{i}_{load}} = R // \frac{1}{sC}$$
$$Z_i(s) = sL + \left(R // \frac{1}{sC} \right) \tag{72}$$

As shown in Fig. (29), it's very clear that the current domain control is a dual-loop feedback system. The first loop is current feedback loop, which senses the inductor current and the second loop is voltage feedback loop, which senses the output voltage then transforms to control current signal. Fig. 30 shows the small signal block diagram of current domain buck converter which based on the dual loop analysis method. It also points out the current

sensing loop T_i and the output voltage loop T_v.

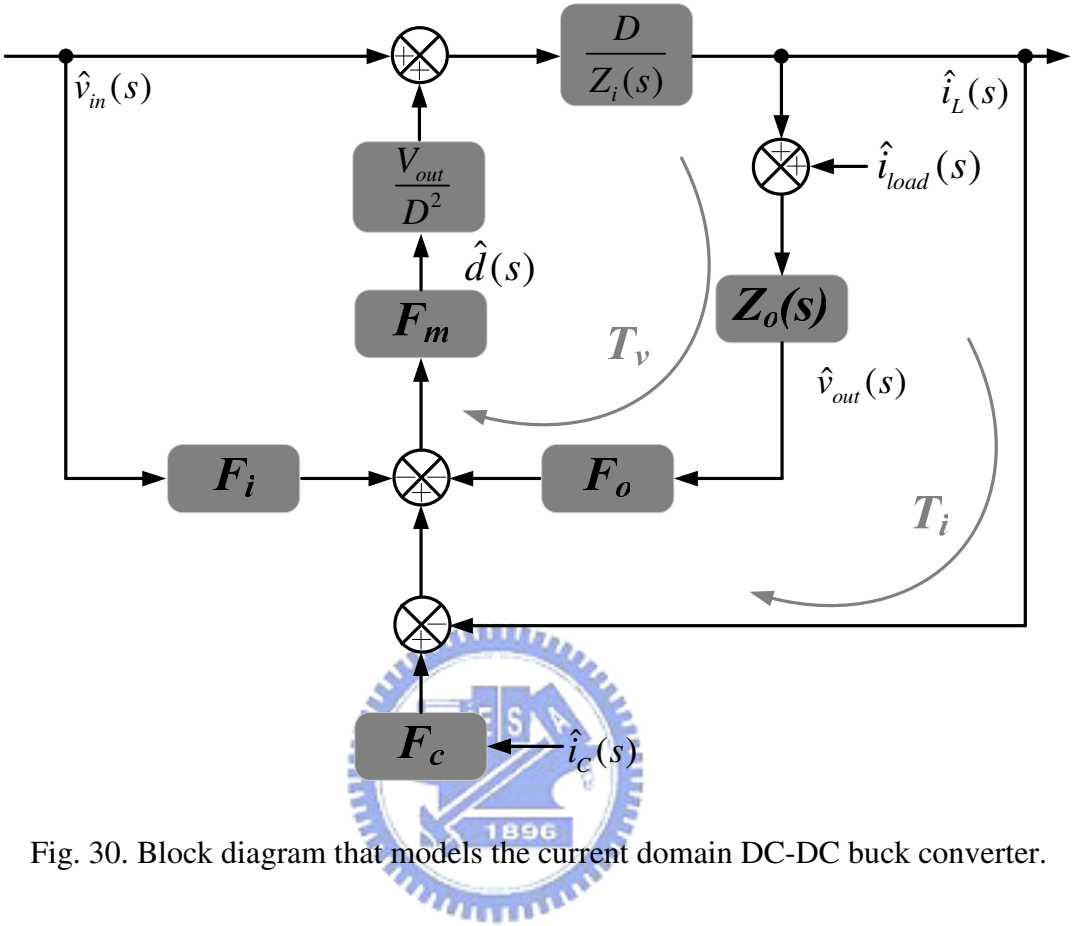


Fig. 30. Block diagram that models the current domain DC-DC buck converter.

As shown in Fig. 30, the ac variation of inductor current could be expressed as

$$\hat{i}_L(s) = \frac{D}{Z_i(s)}\left(\hat{v}_{in}(s) + \frac{V_{out}}{D^2}\hat{d}(s)\right) \tag{73}$$

Therefore, the output voltage variation that produced by inductor current perturbation can be derived as

$$\hat{v}_{out}(s) = \hat{i}_L(s) \cdot Z_O(s) \tag{74}$$

The voltage loop T_v and current loop T_i are defined as:

$$T_v(s) = F_m \frac{V_{out}}{D^2} \frac{D}{Z_i(s)} Z_O(s) F_O$$

$$T_i(s) = \frac{1}{Z_O(s)F_O} \cdot \frac{T_v(s)}{1+T_v(s)} = \frac{F_m \frac{V_{out}}{D^2} \frac{D}{Z_i(s)}}{1 + F_m \frac{V_{out}}{D^2} \frac{D}{Z_i(s)} Z_O(s) F_O} \tag{75}$$

Finally according to the above-mentioned analysis, the control to output transfer function and line to output transfer function are shown in Eq. (76).

$$G_{vc} = \frac{\hat{v}_{out}}{\hat{i}_c} = G_{c0} \frac{1}{1 + \frac{s}{Q_C \omega_C} + \left(\frac{s}{\omega_C}\right)^2}$$

$$G_{vg} = \frac{\hat{v}_{out}}{\hat{v}_{in}} = G_{g0} \frac{1}{1 + \frac{s}{Q_C \omega_C} + \left(\frac{s}{\omega_C}\right)^2}$$

where

$$G_{c0} = \frac{V_{out}}{D} \frac{F_m}{\left(1 + \frac{F_m V_{out}}{DR} + \frac{F_m F_o V_{out}}{D}\right)}$$

$$G_{g0} = D \frac{\left(1 - \frac{F_m F_i V_{out}}{D^2}\right)}{\left(1 + \frac{F_m V_{out}}{DR} + \frac{F_m F_o V_{out}}{D}\right)} \tag{76}$$

$$\omega_C = \frac{1}{\sqrt{LC}} \sqrt{1 + \frac{F_m V_{out}}{DR} + \frac{F_m F_o V_{out}}{D}}$$

$$Q_C = R\sqrt{\frac{C}{L}} \frac{\sqrt{1 + \frac{F_m V_{out}}{DR} + \frac{F_m F_o V_{out}}{D}}}{\left(1 + \frac{RCF_m V_{out}}{DL}\right)}$$

Based on the above analysis, the complete block diagram of current domain dc-dc converter can be shown as Fig. 31.

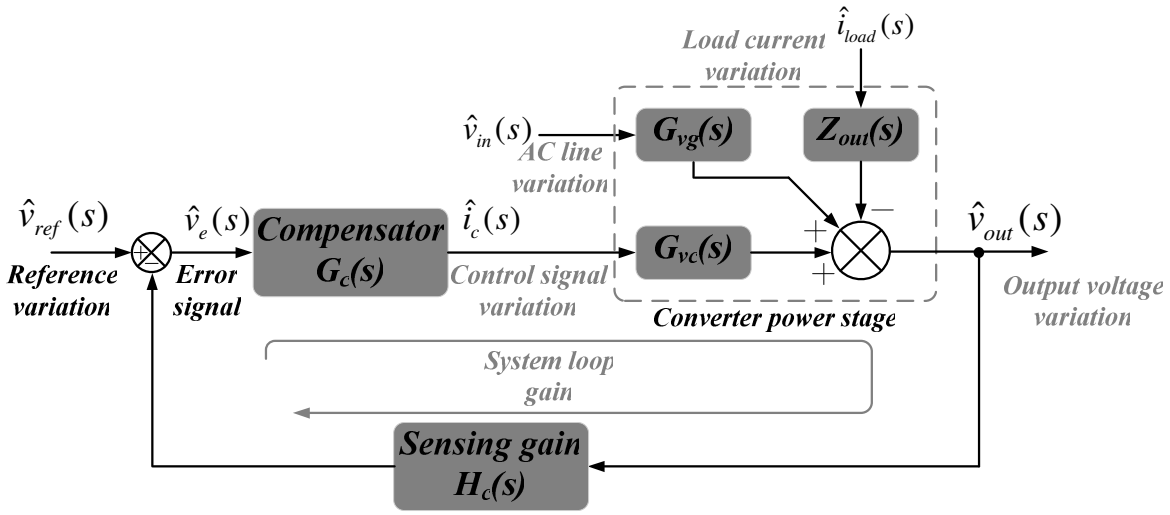


Fig. 31. The block diagram of the feedback system with current mode control.

3.2.2 Structure of PI-Compensator

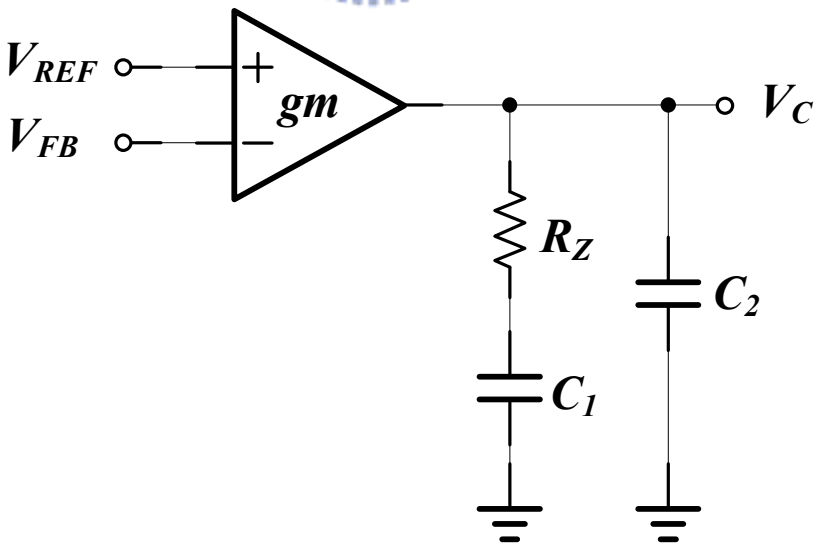


Fig. 32. Schematic of PI-compensator.

According to Eq. (76), the control to output transfer function of current domain buck converter (G_{vc}) has two issues to consideration. Firstly, the original gain of control system (G_{vo}) is too small to result large static regulation error; secondly, the complex double poles may exist if quality factor (Q_c) is too large. Therefore, the compensator is needed in the feedback loop to overcome the problems. As shown in Fig. 32, the PI-compensator contains an operational transconductance amplifier (OTA) and some external passive components (R_Z、C_1、C_2) which connected to the output (V_c) of error amplifier, where g_m is the transconductance and R_o is the output impedance of the error amplifier. Pole-zero cancellation is used in compensation for PI-compensator, the compensator generates a pole-zero pair to replace the originally control to output dominate pole then reset a new stable system dominate pole for new unity gain frequency design. By the way, the value of new unity gain frequency cannot near to switching frequency of DC-DC converter. It will affect the output ripple in magnitude of switching regulator. The safe unity gain frequency must lower than twenty percent switching frequency and it is also called crossover frequency. After compensating, the gain of system loop and phase margin is large enough for small static error and stability of system respectively [5] [6].

The transfer function of PI-compensator is derived as follows and the Bode plot is shown in Fig. 33.

$$T(s)_{PI-comp} = g_m R_O \frac{1 + s \cdot C_1 \cdot R_Z}{(1 + s \cdot C_1 \cdot R_O)(1 + s \cdot C_2 \cdot R_z)} \tag{77}$$

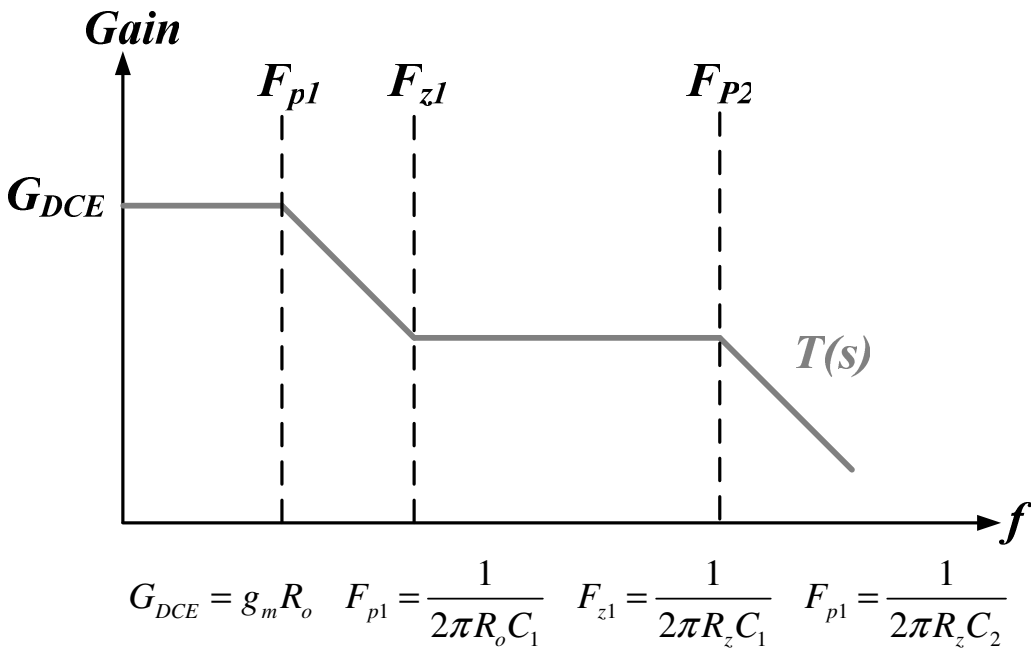


Fig. 33. The Bode plot of PI-compensator.

3.2.3 P-Compensator

As section 3.2.2 mentioned, the small control to output gain will cause big static regulation error, the PI-compensator is needed to provide for high system gain and the zero is used to cancel the original system pole for stability. The drawback of PI-compensator is requires external passive components such as resistor and capacitor to do compensation. Therefore not only one more pin is needed to connect external components but increasing the PCB area [6] [7]. The P-compensator [14] is proposed to increase the dc gain of system controller and doesn't need external compensation. But the additional dc gain of P-compensator is not large enough; it will cause the static regulation error.

On the other hand, the smaller dc gain of P-compensator may cause faster transition. When in the PI-compensation method, as load current changes, huge dc gain maintains the output voltage dc level and just a little bit static error. But the recovery time of output voltage backing to the regulated level will extend.

For fully current domain controller, the control signal must be transformed to current

signal. If using PI-compensator, the output of operational transconductance amplifier generates a voltage signal and it's not suit for current domain design. On the contrary, the P-compensator can see as a voltage to current converter, the current control signal is generated by P-compensator directly.

The feature of P-compensator method is smaller dc gain. It will make the static error of output voltage but reduce the transition time. It's very similar to the design of droop method where the output voltage and load current have linear relationship.

$$T(s)_{P-comp} = G_m \tag{78}$$

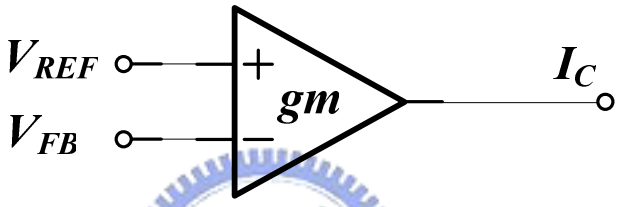


Fig. 34.Schematic of P-compensator.

3.3 Soft Start Technique

For any switching converters, there will be a large inrush current at the moment of power on. During the time of power up, the current rising rate depends on the rising rate of power supply. When taking chip layout into consideration, the inrush current may affect power MOSFET if without any circuit protection. In order to protect the power MOSFET, the soft start technique is needed during the interval of power on [16] [17].

At the beginning of system power on, the output voltage DC level gets close to zero, the inductor current rising slope can be written as V_{IN}/L and the falling slope approximately equals to zero, the close loop system will arise the inductor current and feedback voltage will approach to reference voltage as soon as possible. As a result, the inrush current exists until output voltage comes to the regulated magnitude, then the inductor current goes back to

steady state level. The above description is shown in Fig. 35.

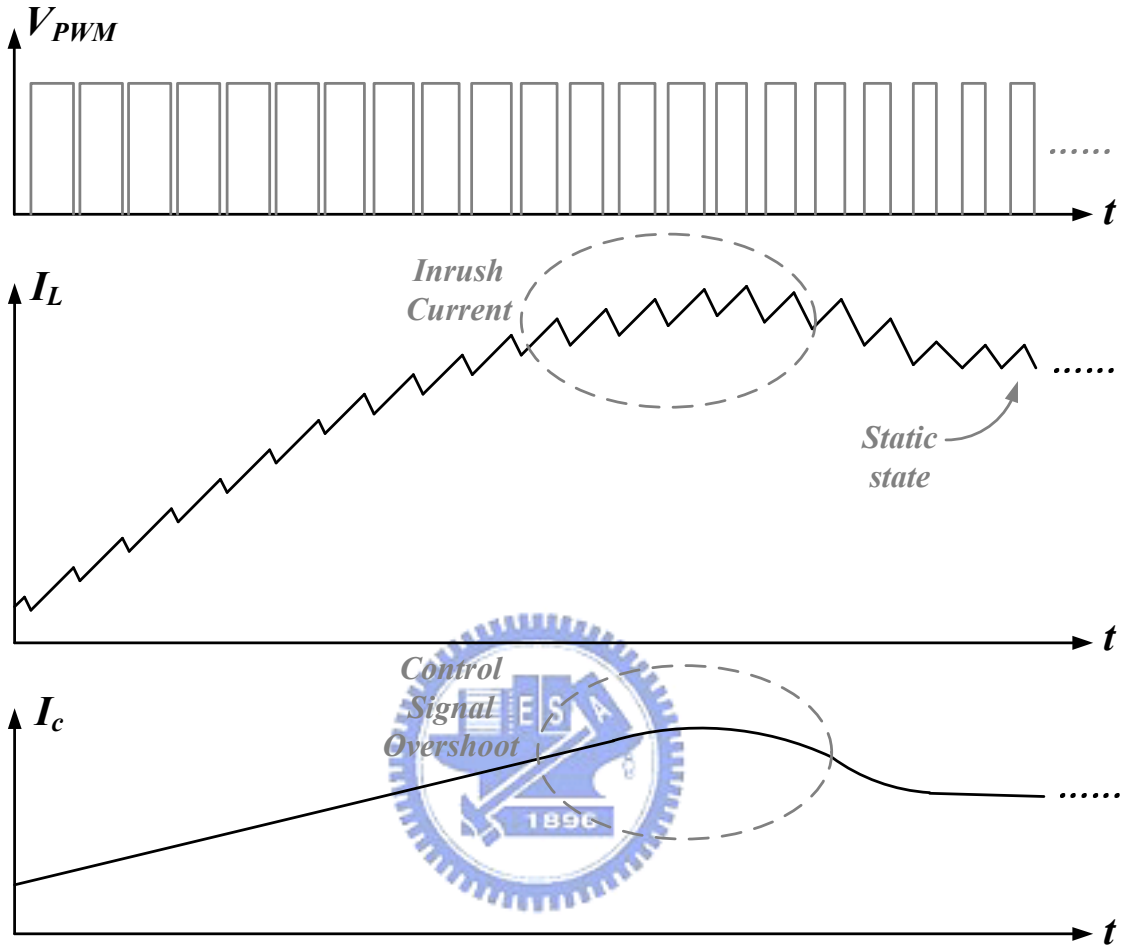


Fig. 35. The inrush current without soft start technique

To avoid the inductor current changing too fast, the soft start technique is implemented to solve this problem. The main function is letting the reference voltage increases slowly and following the output voltage grows up [18]. The simply diagram is shown in Fig. 36. As show in Fig. 36, the off-chip soft-start capacitor C_{SS} and the small bias current I_{SS} make sure the voltage V_{SS} ramps up the output voltage smoothly and slowly. To achieve soft start function, the transistor M_S is added to the input differential stage of P-compensator to substitute for the role of reference voltage V_{REF} during the power on time. At first, the voltage V_{SS} is smaller than V_{REF}, the transistor M_1 is off and the transistors M_S and M_2 comprise the differential

input pair, therefore the P-compensator transforms the error voltage between V_{FB} and V_{SS} to error current signal to regulate output voltage. When V_{SS} approaches to V_{REF}, the transistor M_1 starts to conduct and the transistor M_S turns off gradually. At last, once V_{SS} is high enough, the transistor M_S is completely turned off and transistors M_1 and M_2 comprise the differential input pair, therefore the P-compensator transforms the error voltage between V_{REF} and V_{FB} to error current signal to regulate output voltage. The system backs to the normal operation mode. It is very importance to get a large time constant for implementing the function of soft start. The simulation results and circuit implementation will be shown in the next chapter.

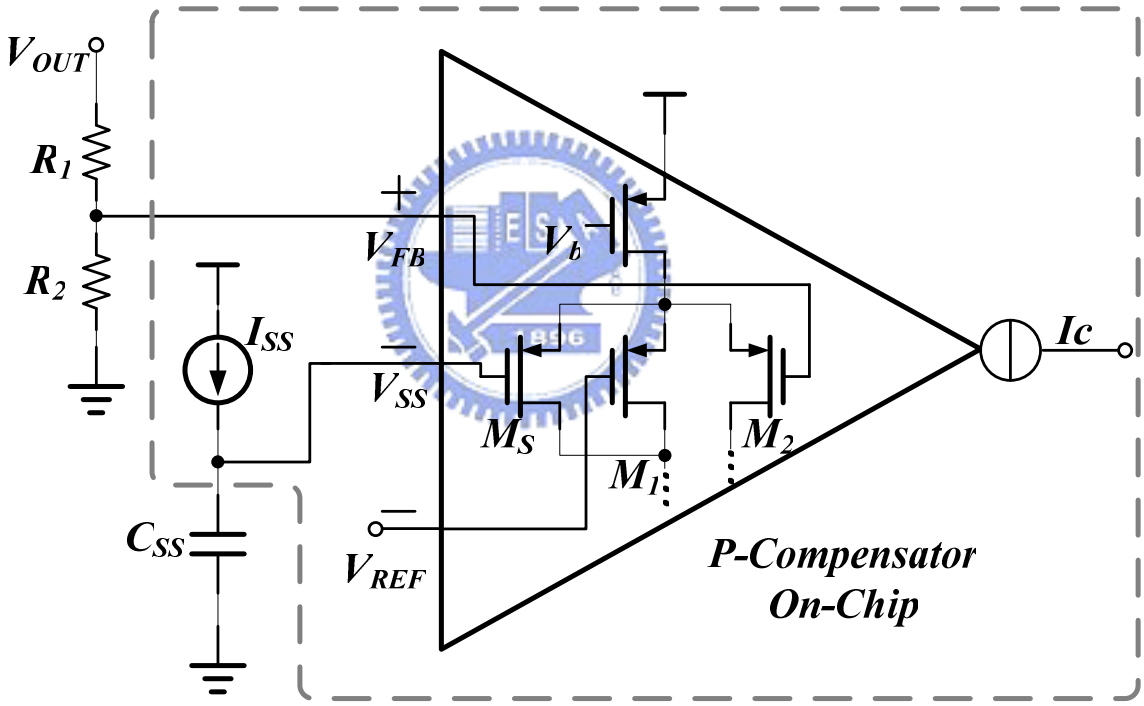


Fig. 36. The simply soft start diagram

3.4 Output Inductor and Capacitor Selection

The inductor value is related to several parameters and it must be examined to choose the best inductor to be used. The inductor value is shown in Eq. (79) [5].

$$L = \frac{V_{IN} - V_{OUT}}{2 \cdot \Delta i_L \cdot fs} D \tag{79}$$

As shown in Eq. (79), there is relating to input voltage, output voltage, switching frequency and inductor current ripple. A higher inductor current ripple can reduce the inductor value, but the drawbacks are high power losses and higher output ripple. The good compromise between inductor size and efficiency is designed for inductor current ripple about the range from fifteen to twenty percent of maximum load current. Increasing the switching frequency also can reduce the inductor value, that's why choosing the current domain method to achieve 20MHZ switching control.

The selection parameters for output capacitor are the actual capacitance value and the equivalent series resistance (ESR). These parameters affect the system stability, output voltage ripple and transient response. The output voltage ripple is composed of two components effect. One is the charge variation of the output capacitor; another is the voltage drop across the capacitor's ESR which is caused by the current flow into and flow out of the output capacitor. The output voltage ripple is derived as follows

$$V_{RIPPLE} \cong V_{RIPPLE}(C) + V_{RIPPLE}(\mathrm{ESR}) \tag{80}$$

The consequence affects the output voltage ripple is capacitor's ESR, and the output capacitance can be defined as

$$V_{RIPPLE}(\mathrm{ESR}) = \Delta I_{L\_P\text{-}P} \cdot \mathrm{ESR}$$

$$V_{RIPPLE}(C) = \frac{I_{L\_P\text{-}P}}{8 \cdot C_O \cdot f_S} \tag{81}$$

The parameter $\boldsymbol{I_{L\_P\text{-}P}}$ is inductor current ripple. The above equations are suitable for output capacitor selection. The capacitor value that calculated by Eq. (80) is the minimum value. If taking the transient drop voltage into consideration, the selected value must be greater than original.

Chapter 4

Circuit Implementation and Simulation Results

In the chapter 4, the detail description of system sub-circuits in chapter3.1 is presented. The simulation results and circuit analysis of system sub-circuit is also discussed. The high switching dc-dc buck converter in current domain control is implemented in TSMC 2P4M 0.25-μm CMOS technology. And the simulation conditions are listed in TABLE IV.

TABLE IV. THE SIMULATION CONDITIONS

	Minimum	*Typical*	*Maximum*
Power supply voltage $V_{DD}(V)$	***3.0***	***3.3***	***4.0***
Temperature (^oC)	***-20***	***25***	***120***
Process corner	***TT, FF, SS, SF, FS***		
Implementation process	***TSMC 2P4M 0.25-μm CMOS technology***		

4.1 P-Compensator

The P-compensator circuit can be seen as one of transconductance amplifier structure, the main function is transferring the input error voltage to the output current. The circuit structure is shown in Fig. 37 [19].

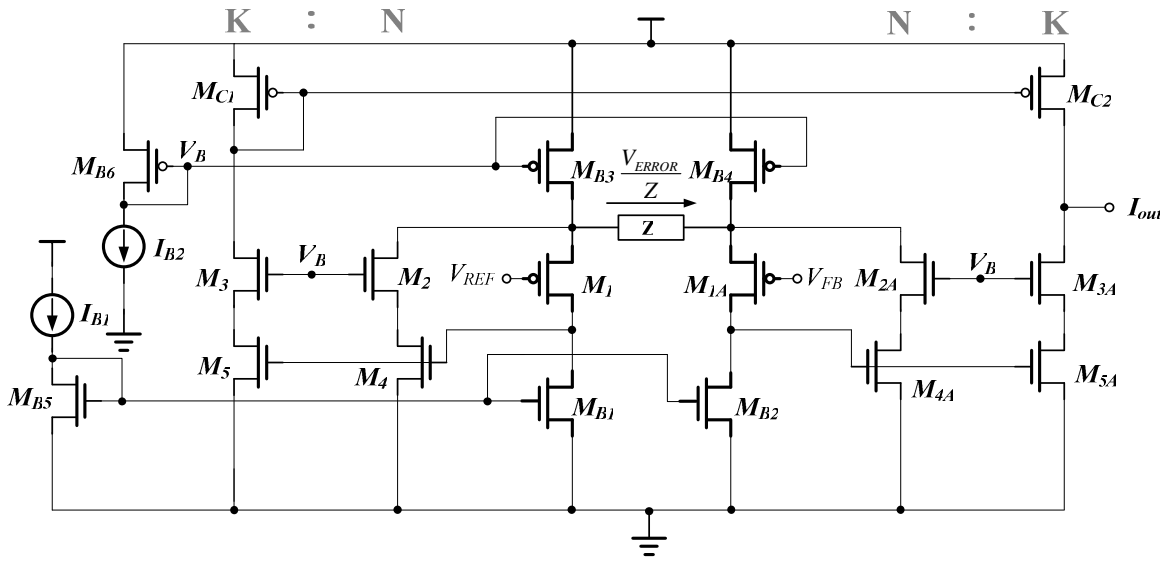


Fig. 37. Schematic of the P-Compensator.

When the input voltage V_{FB} is equal to V_{REF}, the node N_1 is equal to the node N_2. Thus, there is no current pass through the resistor Z. The current on the transistor M_{B3} and M_{B4} equal to the summation of the current on the transistor M_1, M_{1A} and M_2, M_{2A} respectively, the current on the transistor M_{C2} equals to the current on the transistor M_{3A} and M_{5A}. As a result, the output current I_{OUT} equals to zero.

When the input voltage V_{FB} is smaller than V_{REF}, the node N_1 is larger than the node N_2. There is an error current I_{ERROR} flows from the node N_1 to node N_2 across the resistor Z. Thus the current difference between M_{B3} and M_{B4} is equal to I_{ERROR}, and the output stage current I_{OUT} can sink the current. On the contrary, when the input voltage V_{FB} is larger than V_{REF}, the output stage current I_{OUT} can source the current.

The transconductance amplifier can transform the voltage difference to error current. The transconductance of P-Compensator can be written as Eq. (82). The trnasconductance has to consider the output impedance Z_o of node N_1 and the node N_2.

$$G_m \approx \frac{2}{Z + 2Z_O} \times \frac{K}{N} \tag{82}$$

As shown in Eq. (82), the factor $2(K/N)$ is generated by current mirror circuits including

the transistor M_2, M_3, M_{2A}, M_{3A}, M_{C1} and M_{C2}.

The input stage of P-Compensator is voltage follower, as shown in Fig. 38. In Fig. 38(a), the output impedance of original voltage follower is shown as Eq. (83). To reduce the output impedance and improves the P-Compensator linearity, the folded voltage follower is implemented, as illustrated in Fig. 38(b). This structure can reduce output impedance effectively and the output impedance is shown in Eq. (84). But the main disadvantage is input swing depends on the threshold voltage, it becomes very small in modern CMOS technology. The input swing can be written as Eq. (85). For a wider input swing range, the folded flipped voltage follower is implemented, as illustrated in Fig. 38(c). This structure not only reduces output impedance but also improves the input swing range. The output impedance of the folded flipped voltage follower and the input swing range is shown in Eq. (86) and Eq. (87) respectively. By using the folded flipped voltage follower as P-Compensator input stage, the output impedance on the node N_1 and node N_2 in Fig. 37 is greatly reduced, and the linearity of P-Compensator approaches to ideal value.

$$Z_O \approx \frac{1}{gm_1} \tag{83}$$

$$Z_O \approx \frac{1}{gm_2}\frac{1}{gm_1 r_{o1}} \tag{84}$$

$$V_{in}^{swing} = V_{GSM1} - V_{DSM2} - V_{DSM1} = V_T - V_{DSM2} \tag{85}$$

$$Z_O \approx \frac{1}{gm_2}\frac{1}{gm_1 r_{o1}} \tag{86}$$

$$V_{in}^{swing} = V_{DD} - V_{GSM1} - V_{DS2Ib} \tag{87}$$

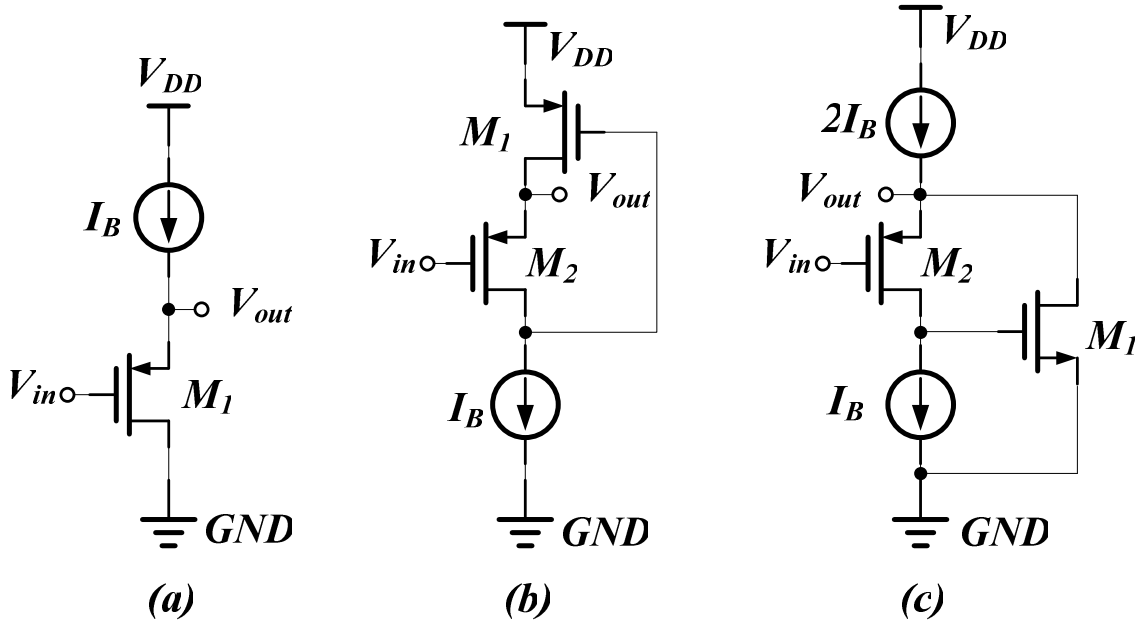


Fig. 38. Schematic of different P-Compensator input stages. (a) Voltage follower. (b) Folded voltage follower. (c) Folded flipped voltage follower.

The simulation result is shown on Fig. 39, where the upper wave is feedback and reference voltage respectively; the lower wave is an output current I_{OUT}.

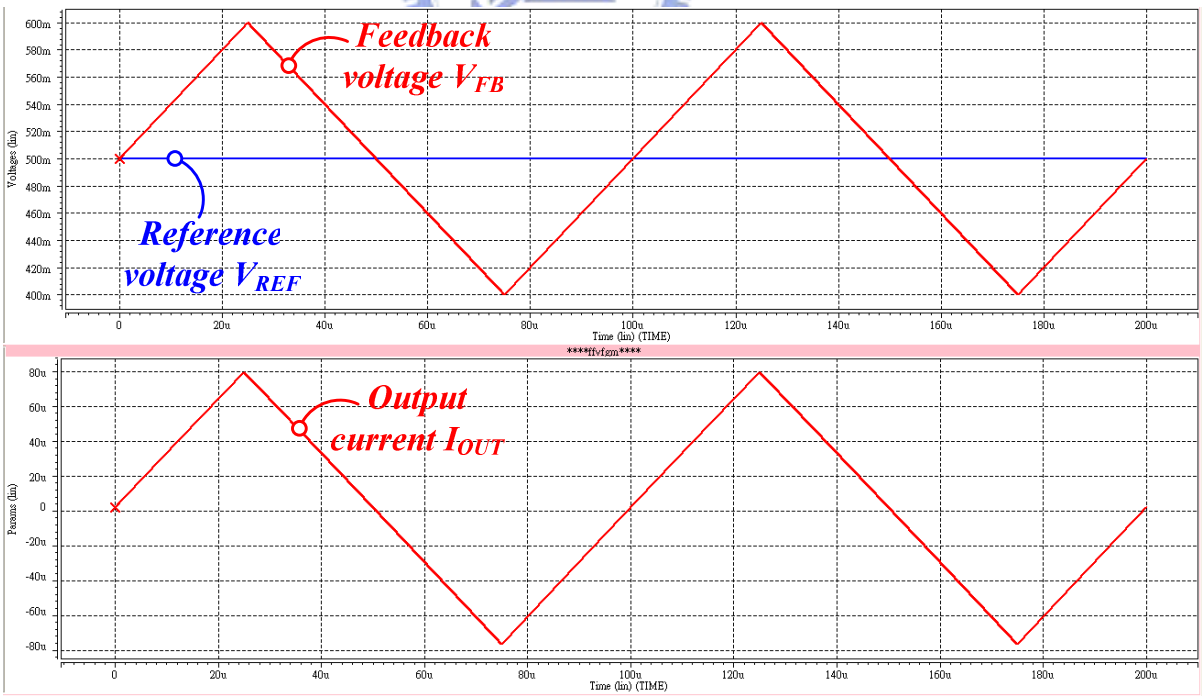


Fig. 39. The simulation result of P-Compensator

The comparison result of linearity between ideal and actual transconductance is shown on TABLEV, the accuracy is about 95%.

TABLE V. THE LINEARITY BETWEEN IDEAL AND ACTUAL TRANSCONDUCTANCE

Ideal transconductance	***800 μA/V***
Actual transconductance	***761.2 μA/V***
Accuracy	***95.15%***
Test waveform	***Triangular form with 0.2V amplitude***

4.2 Current Sensing Circuit

Current sensing [20] [21] circuit is necessary for current mode PWM control. For step-down regulator, it only has to sense the power PMOSFET turn on state. The conventional method is using on-chip current-sensing technique [6] which is depending on the size ratio between power MOSFET and sensing MOSFET. Letting both of MOSFET with the same Gate, Drain and Source dc voltage level, and sensing MOSFET can sensing the ratio of inductor current. Then control the current mode PWM system. But it's not suit for high switching dc-dc buck converter in current domain control because the bandwidth of on-chip current sensing circuit is lower than the switching frequency. The on-chip current sensing circuit doesn't work at high switching frequency. Besides, the current domain control needs actual current signal, but the on-chip current sensing circuit cannot scale down the ratio too much. It has to substitute the conventional design for current domain control.

Fig. 40 shows the schematic of current sensing circuit which scales down the inductor current to the sensing current. This structure consists of external sensing resistor R_{SENSE}, bias circuit M_{B1}~ M_{B3} and bias current I_B. The main sensing loop is including the transistors M_1~M_3, the resistors R_1 and R_2. The purpose of the sensing loop is adjusting the output current I_{OUT} during the power PMOSFET turn on interval, there is a voltage drop across to the

resistor R_{SENSE} and current sensing circuit can get inductor current information to generate output current I_{OUT}.

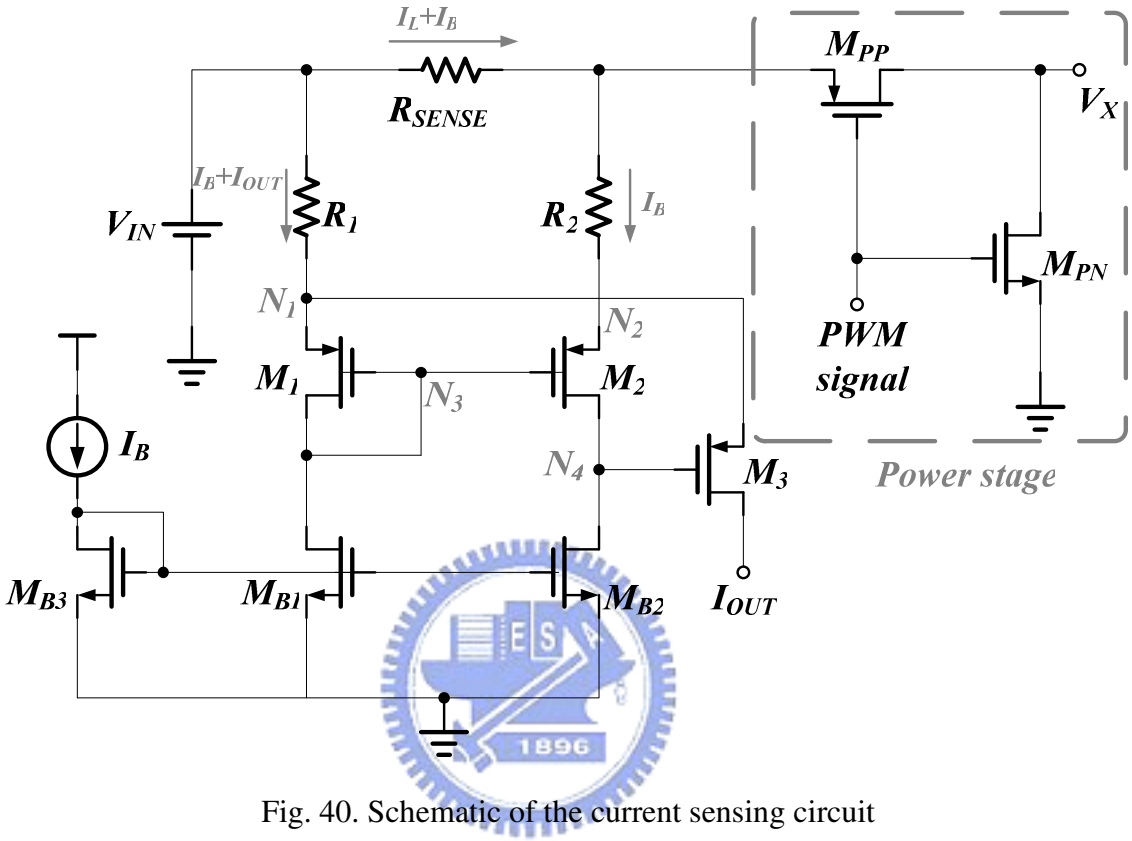


Fig. 40. Schematic of the current sensing circuit

The operation step is described as follows. As the power PMOSFET turn on, the inductor current pass through the resistor R_{SENSE}. Then the voltage at node ***N2*** decreases, but the voltage of the node ***N3*** has been clamped and the bias current from M_{B1} and M_{B2} is fixed. As a result, the voltage level of node N_4 decreases and the current on the transistor M_2 increases. And the voltage of node N_1 is pulled down and equal to the voltage of node N_2. Since the bias current I_B is much smaller than the inductor current, the bias current can be neglected. The formula of current sensing circuit is presented in Eq. (88). As a result, the conversion ratio I_L/I_{OUT} is equal to R/R_{SNESE}.

$$
\begin{aligned}
&(I_L + I_B)\times R_{SENSE} + I_B \times R_2 = (I_B + I_{OUT})\times R_1 \\
&\text{If } I_L >> I_B \text{ and } R_1 = R_2 = R \\
&I_L \times R_{SENSE} + I_B \times R_2 = (I_B + I_{OUT})\times R_1 \\
&\therefore \frac{I_L}{I_{OUT}} = \frac{R}{R_{SENSE}} \Rightarrow I_{OUT} = \frac{R_{SENSE}}{R} I_L
\end{aligned}
\tag{88}
$$

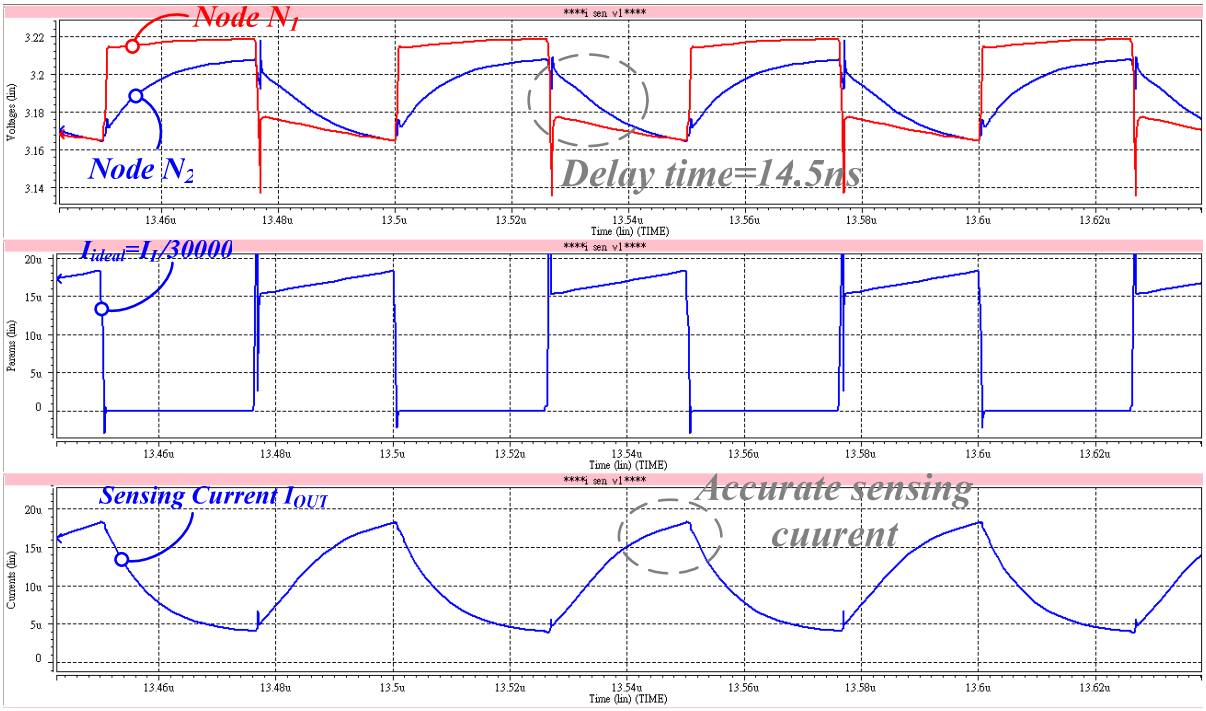


Fig. 41. The simulation results of current sensing circuit with Heavy load condition.

The simulation results of current sensing circuit at switching frequency 20MHz for heavy load and light load condition is shown in the Fig. 41 and Fig. 42 respectively. Due to the response delay time at 20MHZ switching frequency plays an important role because a period cycle only has 50ns. It affects the system minimum duty ratio critically. And it also restricts input and output voltage range. At heavy load condition, the sensing delay is about 14.5ns and the accuracy is about 90% if only considering the correct current sensing interval. And at light load condition, a dc current error happens because the node N_1 and node N_2 have voltage gap. Due to the I_L is close to the I_B at light load condition, the accuracy of light load

condition is only about 85 %.

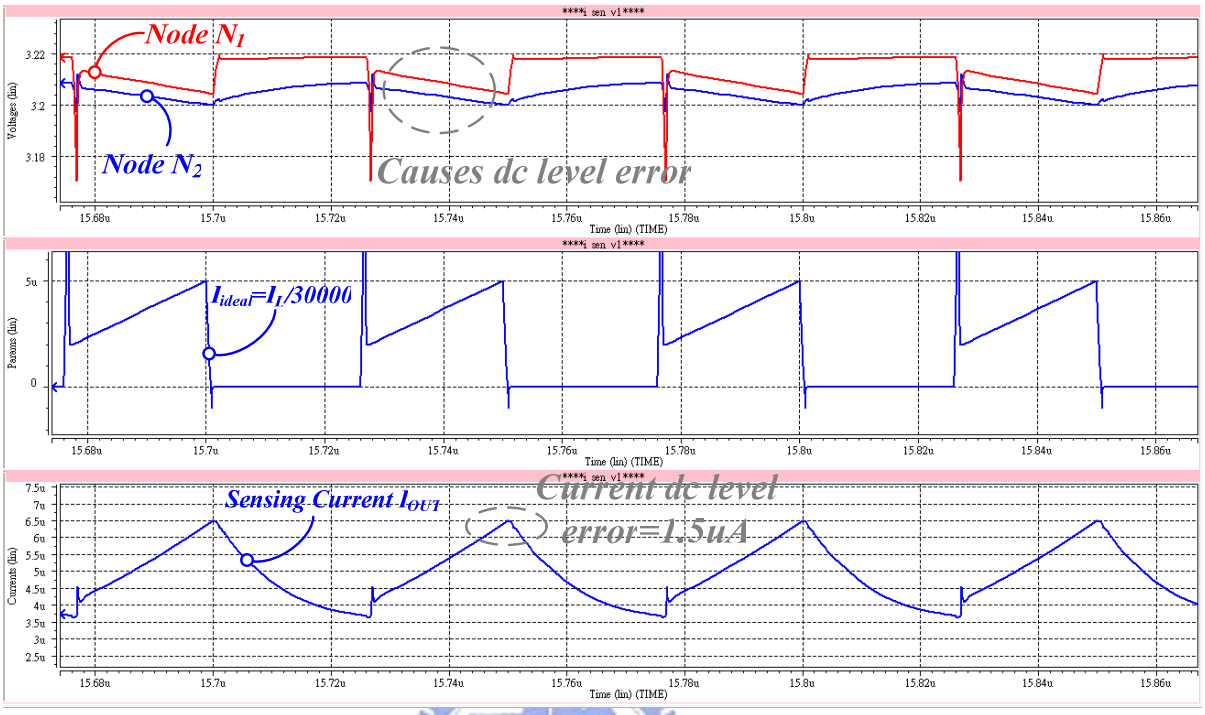


Fig. 42. The simulation results of current sensing circuit with Light load condition

The typical conditions of heavy load and light load sensing accuracy are listed in TABLE VI.

TABLE VI. SENSING ACCURACY IN DIFFERENT LOAD CONDITIONS

Heavy Load (I_L=500mA)	***Light Load (I_L=100mA)***
Temp: 25^{0}C, TT, *Switching Frequency: 20MHz*	*Temp: 25^{0}C, TT,* *Switching Frequency: 20MHz*
VDD=3.3V	*VDD=3.3V*
Sensing current value=18.23uA	*Sensing current value=6.5uA*
ACCURACY=90.3%	*ACCURACY=85.63%*

4.3 Ramp Generator

As mentioned in section 2.3.3, when duty cycle of current mode DC-DC buck converter greater than 50% will cause sub-harmonic oscillation. The slope compensation is needed to prevent this problem. The artificial ramp slope must bigger than the half inductor current down slope. The ramp generator is shown in Fig. 43 [14]. The output current of ramp generator creates an artificial ramp current to add to inductor sensing current.

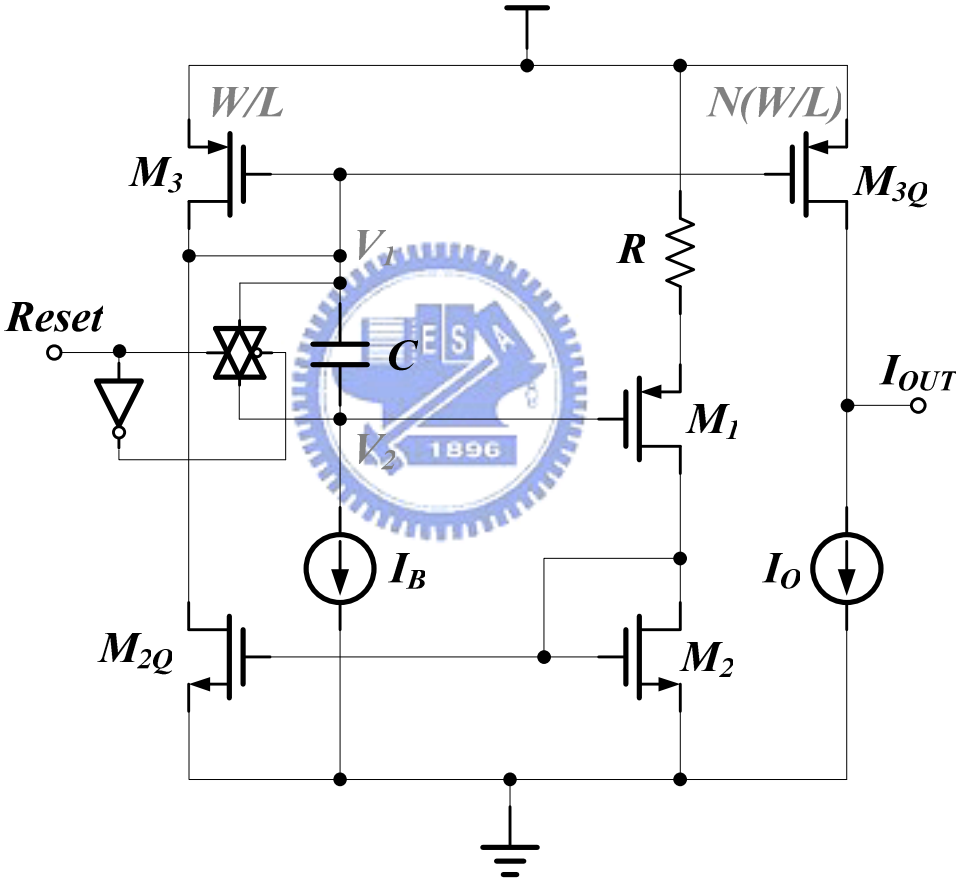


Fig. 43.Schematic of the ramp generator circuit [14].

The function description is shown as follows. At first, the reset signal is logic low; the transmission gate is turned off. Then the current source I_B starts to charge the capacitor C. And the voltage difference on capacitor is equal to the voltage difference across on the resistor R. As the voltage level of the node V_2 becomes lower, the increasing current on the

transistor M_2 is mirrored form M_2 to M_{2Q}. Then the ramp current magnifies form M_3 to M_{3Q}. Once the reset signal is logic high; the transmission gate is turned on, and the original charge on the capacitor is discharged by the transmission gate. Then the output stage M_{3Q} stops to provide current to output node I_{OUT}. The reset signal is generated by clock generator, to make sure that the ramp current signal synchronizes to system clock.

The formula of ramp generator and the compensation slope determination is shown in Eq. (89) and Eq. (90) respectively, where ma where m_a is the slope of ramp current, m_2 is the slope of inductor current during the second subinterval and m_{2S} is the down-slope of inductor sensing current.

$$
\begin{aligned}
& I \times R + V_{gs1} = V_{gs3} + (V_1 - V_2) \\
& Let \;\; V_{gs3} = V_{gs1} \\
& \therefore I \times R = (V_1 - V_2) \\
& \because V_1 - V_2 = \frac{I_B}{C} \times \Delta t \\
& \therefore \frac{I}{\Delta t} = \frac{I_B}{C \times R} \\
& \Rightarrow m_a = \frac{I \times N}{\Delta t} = \frac{I_{OUT}}{\Delta t} = N \times \frac{I_B}{C \times R}
\end{aligned}
\tag{89}
$$

$$
\begin{aligned}
& m_a \geq \frac{1}{2} \cdot \left| m_{2S} \right| \\
& \left| m_2 \right| = \left| \left(\frac{-V_{OUT,MAX}}{L} \right) \right| = \left| \frac{-4}{200n} \right| = 2 \cdot 10^7 \\
& \left| m_{2S} \right| = \left| \frac{\left(\frac{-V_{OUT,MAX}}{L} \right)}{\alpha} \right| , \text{where } \alpha = \frac{I_L}{I_{SNESE}} = 30000 \cong 66.67 \\
& \therefore m_a \geq \frac{1}{2} \cdot 66.67 = 33.335
\end{aligned}
\tag{90}
$$

The simulation result of artificial ramp current is shown in Fig. 44. There is a peak current during reset signal from logic low to logic high. It is because when transmission gate turns on, the node V_2 couples the voltage level from node V_1 and results to a large current is transformed by current mirror circuit to output. But the peak current doesn't affect the system loop because reset signal changes to logic high, the buck converter system will follow to the clock signal.

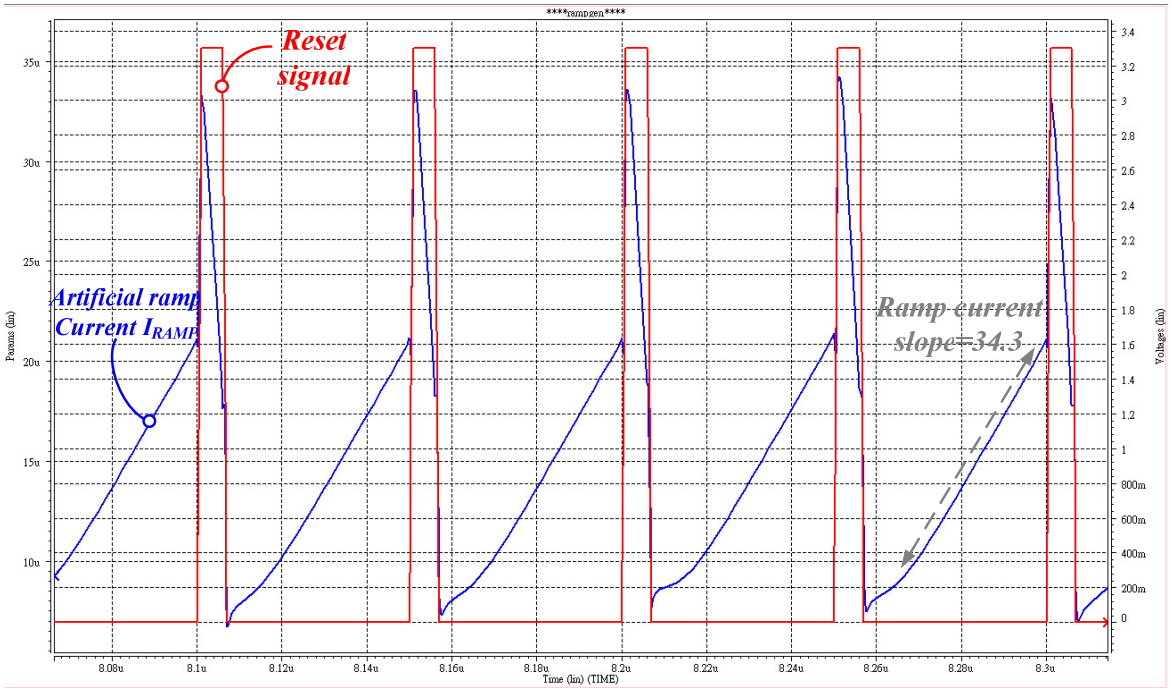


Fig. 44. The simulation result of ramp generator circuit

4.4 Clock Generator

The accurate and integrated clock generator is needed to the switching regulator. Although the structure can be designed easily such as ring oscillator, but the huge frequency variance while supply voltage changes may affect system stability. The clock generator for the high switching DC-DC buck converter in current domain control is shown in Fig. 45 [22].

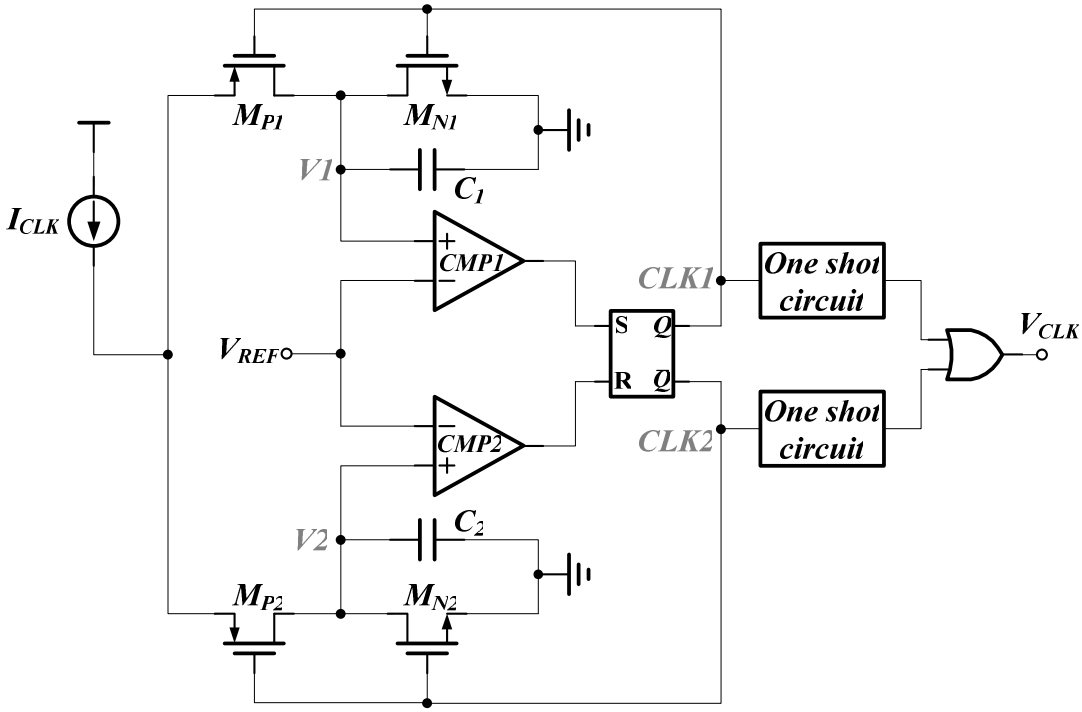


Fig. 45. Schematic of the clock generator circuit.

The operational steps of clock generator are described as follows. At first, assumed that the prior state of the node ***CLK1***=0 and ***CLK2***=1, the transistors M_{P1}, M_{N2} turn on and the transistors M_{P2}, M_{N1} turn off. Then the constant current I_{CLK} charges to the capacitor C_1 and the capacitor C_2 discharges to ground by flow into the M_{N2} path. Before the comparator ***CMP1*** changes the state, both of the comparators output is zero. And it doesn't affect the output of S-R latch because both of input voltage is zero meaning the output of S-R latch keeps the prior state. Once the voltage ***V1*** is bigger than reference voltage V_{REF}, the comparator ***CMP1*** changes state, and the input set ***S*** of S-R latch is logic high. Finally, the node ***CLK1*** changes to logic high and the node ***CLK2*** changes to logic low. Secondly, as the node ***CLK1***=1, ***CLK2***=0, contrary the capacitor C_1 is discharged by M_{N1} and charges the capacitor C_2, and finally the result backs to the first step that the node ***CLK1*** changes to logic low and the node ***CLK2*** changes to logic high. The actions between the first and the second step will operate repeatedly. Consequently, the clock generator with fixed frequency is provided and can be designed by the following formula.

$$f_{sw} = \frac{I_{CLK}}{V_{REF} \cdot C} \text{ ,where } C = C_1 = C_2 \tag{91}$$

As the capacitor C_1 equal to the capacitor C_2, the 50% duty out of phase clock signals are generated on the ***CLK1*** and ***CLK2*** respectively. Then the ***CLK1*** and ***CLK2*** sent the 50% duty out of phase clock signals to the one shot circuit which is sown in Fig. 46 respectively. The main function of one shot circuit is generating a pulse signal when the clock signal is changing from low to high. And the pulse signal determines the minimum duty ratio of system, generally speaking, the delay time of pulse signal is ten percent of system switching period. Finally, using the logic OR gate to combine the output of one shot circuits. The doubled switching clock can be obtained. For 20MHz switching frequency design, just generating 10MHz 50% duty out of phase clock signals can provides a 20MHz clock signal. Eventually, the one shot signal with fixed and doubled clock is provided and the one shot signal can set the converter to turn on the power PMOSFET in the beginning of every switching cycle.

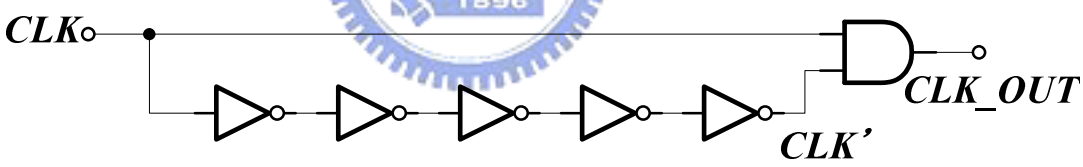


Fig. 46. Schematic of the one shot circuit.

When designing the clock generator, it must be take care of two things. At first, the current I_{CLK} must be a constant current, or it will affect the accuracy of clock signal. The current I_{CLK} can be generated by a voltage to current converter and mirrored into the transistors M_{P1} or M_{P2}. The advantage of this structure is immunizing the current variation cause by supply voltage or process. Secondly, to prevent the error logic control of clock generator, the S-R latch with additional logic is needed. For example, if both the ***CLK1*** and ***CLK2*** are equal to zero in the initial condition, both of capacitors C_1 and C_2 start to charge

current. Then the output of comparator is both logic high and affects the normal operation if only use the S-R latch. The additional logic added on the S-R latch is shown in Fig. 47. The purpose of additional logic is preventing the non-defined case caused by S-R latch and making the clock generator in the incorrect function. Therefore, the non-defined function is defined as "SET" state, that is the ***CLK1***=1, ***CLK2***=0, after adding the additional logic of S-R latch. And the clock generator gets in normal operation. By the way, the pulse generator circuit of current domain buck converter is also using this kind of structure [6]. The truth table of S-R latch with additional logic is also listed in TABLE VII.

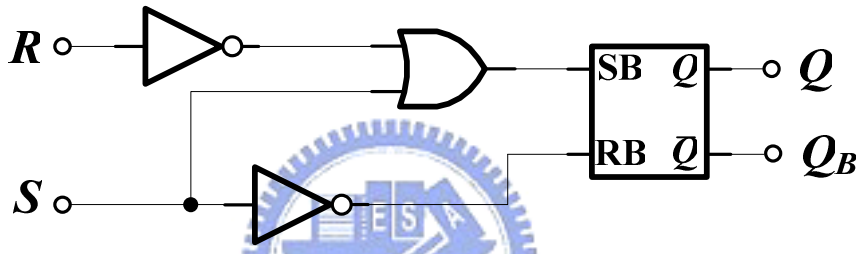


Fig. 47. The additional logic with S-R latch.

TABLE VII. THE TRUTH TABLE OF THE S-R LATCH WITH ADDITIONAL LOGIC

State	***S***	***R***	***Q(n+1)***	***Q_B(n+1)***
Set	*1*	*0*	*1*	*0*
Hold	*0*	*0*	*Q(n)*	*Q_B(n)*
Reset	*0*	*1*	*0*	*1*
Priority set	*1*	*1*	*1*	*0*

Another important component of clock generator is voltage comparator. Because operating at 20MHz switching frequency. The comparison speed of voltage comparator must be as fast as possible. For high switching frequency design, the voltage comparator is shown in Fig. 48 [23] and the structure is described as follows.

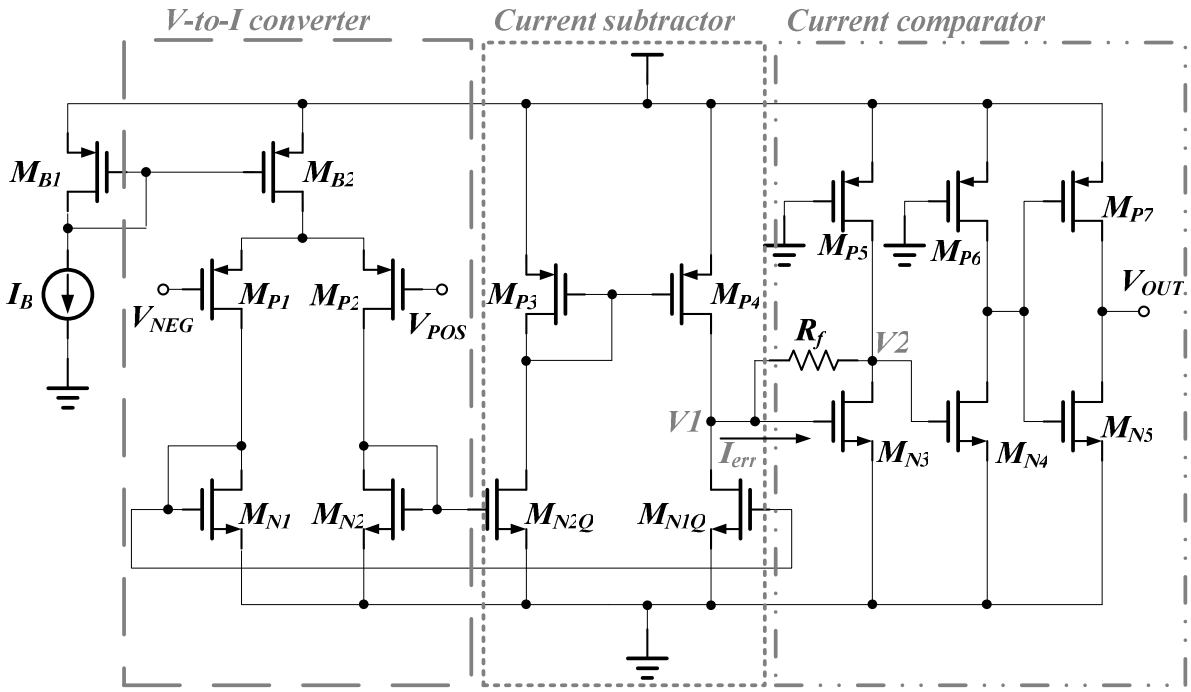


Fig. 48. Schematic of the voltage comparator.

Because of Current-mode comparators have higher speed, larger bandwidth, and lower supply voltage requirements compared to their conventional voltage-mode counterparts [25]. The Fig. 48 shows the circuit schematic of the designed current comparator block. The circuit consists of a V-to-I converter, a current subtractor and a current comparator at the last stage [24]. The difference between V_{POS} and V_{NEG} inputs of the comparator is converted into error current I_{err} at the output of the subtractor stage. The error current I_{err} is then applied to the first current source inverting amplifier, which uses a resistive feedback to reduce its input and output resistance [25]. These small resistances reduce the voltage swing at nodes ***V1*** and ***V2***, which causes faster transient response time in the following inverting amplifiers. The simulation result of voltage comparator is shown in Fig. 49. Operating at switching frequency 20MHz, the rise time and fall time delay is lower than 4n second when there is a 0.1V voltage difference between the positive and negative input stage.

The simulation result of clock generator shows in Fig. 50, where the frequency of 50% duty out of phase cycle signals are about 10MHz, and the one shot time of set signal is about 5n second. Therefore the combinational clock signal is doubled to 20MHz and the one shot is

about 10% of the clock cycle. Finally, the detail clock information between different kinds of process corner and supply voltage is listed at TABLE VIII.

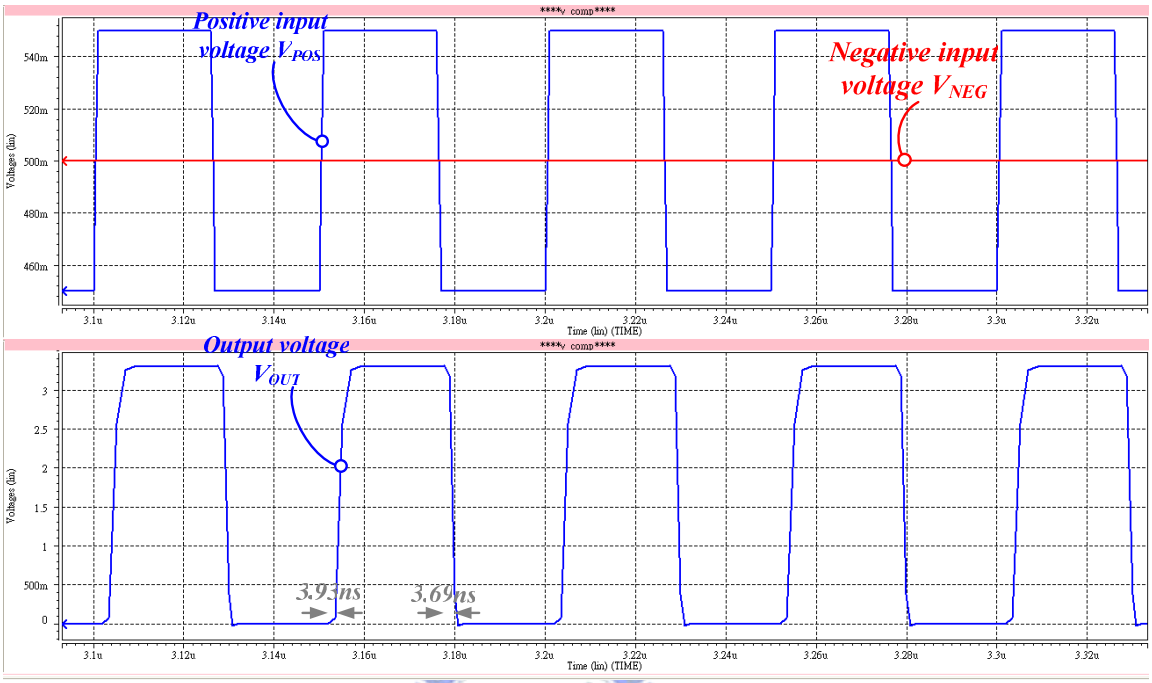


Fig. 49. The simulation results of voltage comparator.

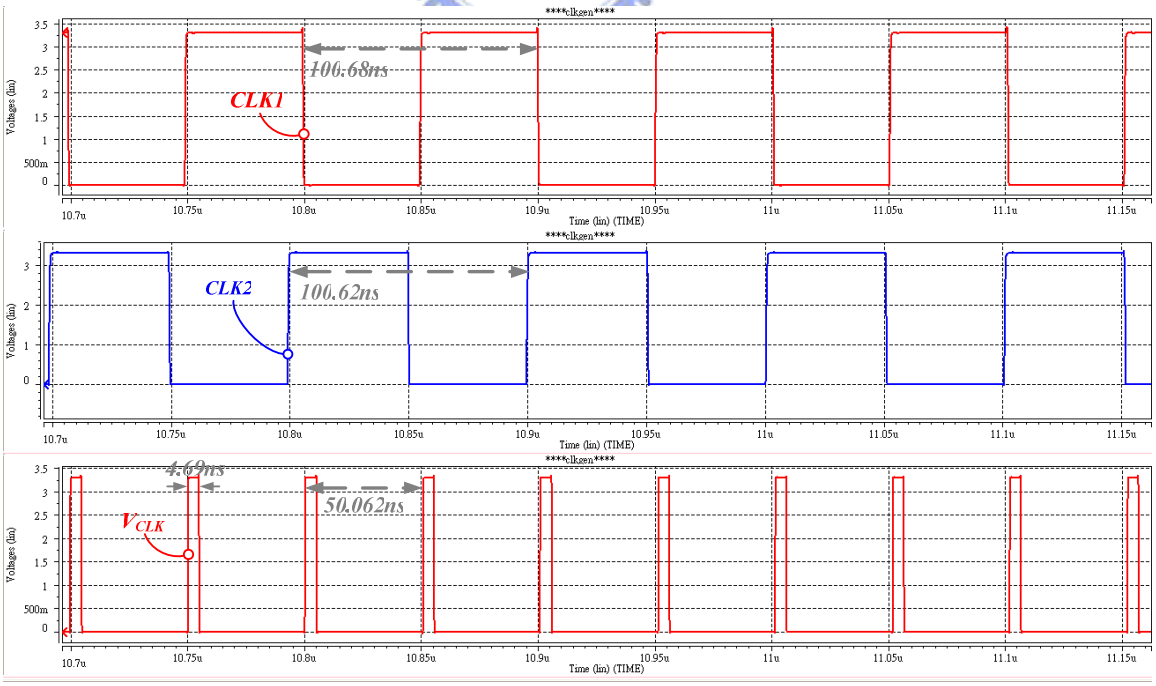


Fig. 50. The simulation results of clock generator.

TABLE VIII. THE CLOCK GENERATOR OPERATING FREQUENCY IN DIFFERENT CONDITIONS

Ideal switching frequency (Hz)	***20M***
Actual switching frequency (Hz)	***16.67M~19.76M***
Error percentage (%)	***-16.65~-1.2***
Ideal one shot delay time (ns)	***5***
Actual one shot delay time (ns)	***4~8***
One shot percentage of a cycle (%)	***8~16***

4.5 Current Comparator

The purpose of current comparator is determining the direction of input current, then transforming to output rail-to-rail digital voltage signal [24]. Simply speaking, when the input current flows into the current comparator, the node ***V1*** is increased then causes the node ***V2*** decreases. After several stages of inverting amplifier, the output voltage becomes logic high. On the contrary, when the input current flows out of the current comparator, finally the output voltage becomes logic low.

The detail operational principle of current comparator is shown in Fig. 51 [25] and described as follows. The current comparator comprises one CMOS complementary amplifier (M_{P1}, M_{N1}), two resistive-load amplifiers (M_{P5}, M_{P6}, M_{N3}, M_{N4}), and a CMOS inverter (M_{P7}, M_{N5}). Because the transistors M_{P1} and M_{N1} both work in saturation region, to prevent too large working current the size of the transistors M_{P1} and M_{N1} has to be considered. The transistor M_{N2} working in linear region acts as the negative feedback resistor of the CMOS complementary amplifier. According to small-signal analysis, the input and output resistances of the CMOS complementary amplifier with a feedback resistor can be expressed as

$$R_{in} \approx R_{out} \approx \frac{1}{gm_{N1} + gm_{P1}} \tag{92}$$

These small input and output resistances can reduce the voltage swings at node ***V1*** and ***V2***, so the response time of the comparator will be greatly decreased. To amplify the small voltage swing at node ***V2***, two resistive-load amplifiers are used to provide additional gains. The last one CMOS inverter can output a rail-to-rail compared result signal. The current comparator has no external bias currents and bias voltages, so the process deviation immunity is enhanced.

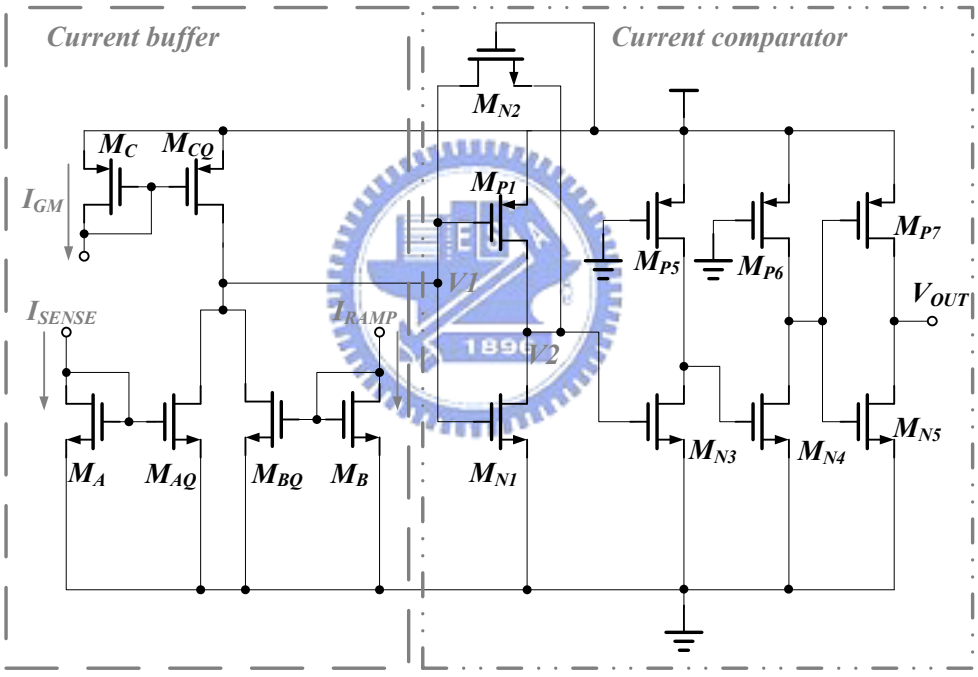


Fig. 51. Schematic of the current comparator circuit

The current comparator is most important component of current domain PWM controller, which converts the direction of current signal into pulse width signal to control the power MOSFET of power stage. To prevent the voltage deviation at the node ***V1*** resulting to the incorrect comparison. The current buffer is needed to keep correct dc voltage level of the node ***V1***, ideally to be designed at half of supply voltage ($V_{DD}/2$). And the comparative current signal can be compared through the mirror transistors (M_{AQ}, M_{BQ}, M_{CQ}). The current

comparator simulation result is shown in Fig. 52, where the rise time delay is 5.75n second and the fall time delay is 6.06n second at the switching frequency 20MHz.

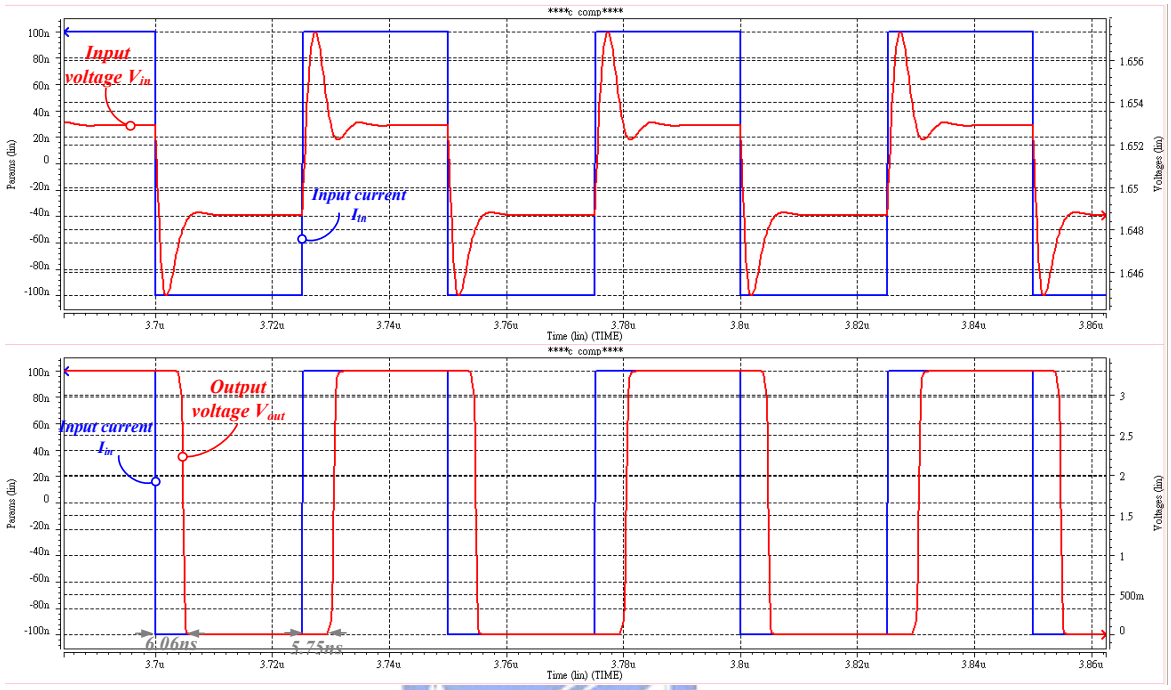


Fig. 52. Simulation results of the current comparator circuit

4.6 Soft Start

The soft start circuit is illustrated in Fig.53. The transistor ***Ms*** is added on the negative side of P-compensator input differential pair, as shown in Fig. 36. The gate of transistor ***Ms*** is connected to the soft start voltage V_{SS}, which connected with the external capacitor C_{SS}. And a small bias current I_{SS} makes V_{SS} rising slowly. Two switch transistors Ms1 and Ms2 are controlled by digital signal END_{SS}, during the soft start time, the END_{SS} signal is logic low and M_{s1} turns on and M_{s2} turns off to keep in soft start state. When the soft start time is ending, the END_{SS} signal becomes logic high and M_{s1} turns off and M_{s2} turns on to release the charge from soft start capacitor C_{SS} and reset the soft start voltage V_{SS} to prepare system power on at next time. The resistor R_C is clamping the release current from C_{SS}, to prevent the large

current destroys the switch MOSFET M_{S2}.

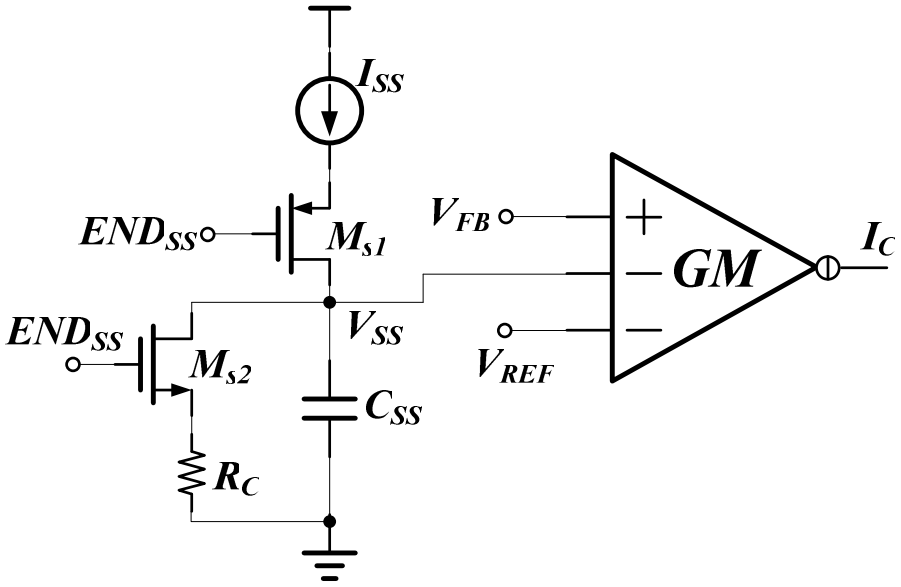


Fig. 53. Schematic of the soft start circuit

The purpose and detail circuit description has been discussed in the section 3.3. The result of the soft start is shown in Fig. 55 in the next chapter. The start up time can be calculated as Eq. (93), as a result, the larger capacitor value provides the longer start up time for switching regulator and smaller inrush current.

$$\begin{aligned} &\because I = C\frac{\Delta V}{\Delta t} \Rightarrow \text{Start up time } \Delta t = \frac{C_{SS}\cdot V_{REF}}{I_{SS}} \\ &set \quad C_{ss} = 0.4nF \quad \Delta V = 0.5V \quad I_{SS} = 2\mu A \\ &\therefore \text{Start up time } \Delta t = \frac{0.4n\cdot 0.5}{2\mu} = 100\mu S \end{aligned} \tag{93}$$

Chapter5

System of High Switching DC-DC Buck Converter in Current Domain Control Simulation Results, Conclusions and Future Work

5.1 System Simulation Results

The high switching dc-dc buck converter in current domain control simulation results is shown in this section. And the summary of whole system is shown in the last section.

5.1.1 Start Up

The system start up response is shown in Fig. 54 and Fig. 55. As shown in Fig. 54, the output voltage V_{out1} and inductor current I_{L1} increase rapidly to steady state but result to the inrush inductor current. It's because the input voltage V_{IN} rises too fast and without the soft start circuit. As shown in Fig. 55, the output voltage V_{out2} and inductor current I_{L2} arise slowly to the steady state. Compare to the Fig. 54, the inductor current I_{L2} and output voltage V_{out2} with soft start circuit grows up slowly and takes longer time to steady state. As a result, with soft start circuit can prevent the inrush current and let output voltage growing up slowly.

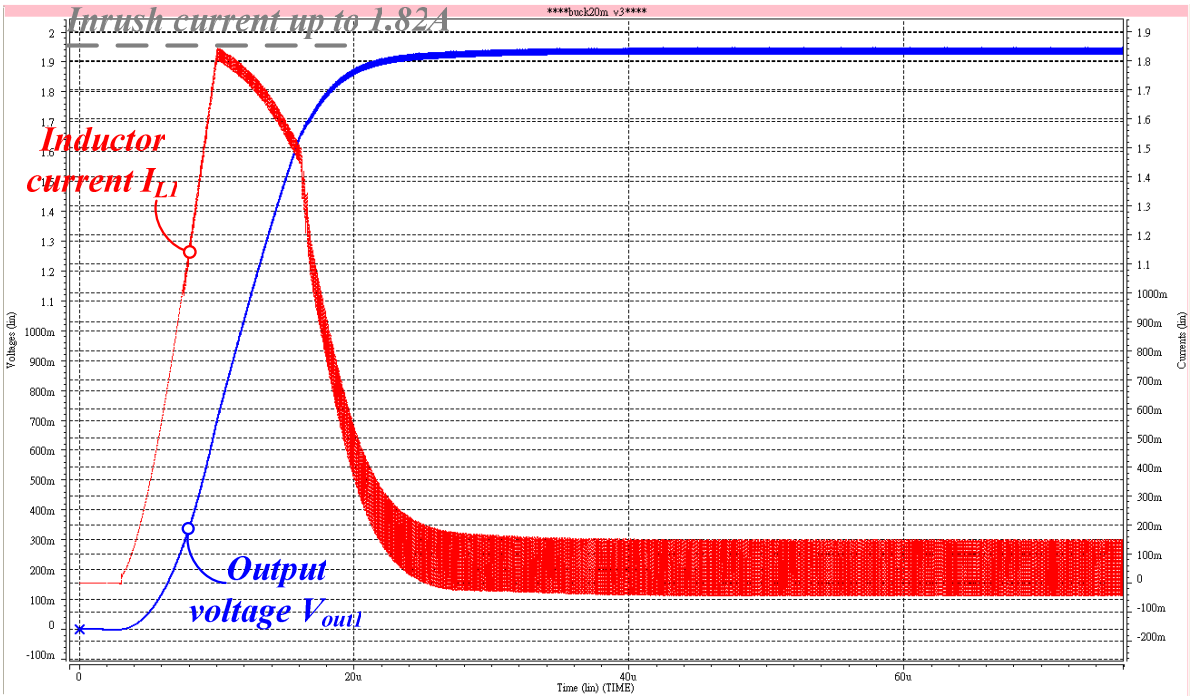


Fig. 54. The start up response waveform without soft start circuit.(@ V_{IN}=3.3V, I_{load}=50mA)

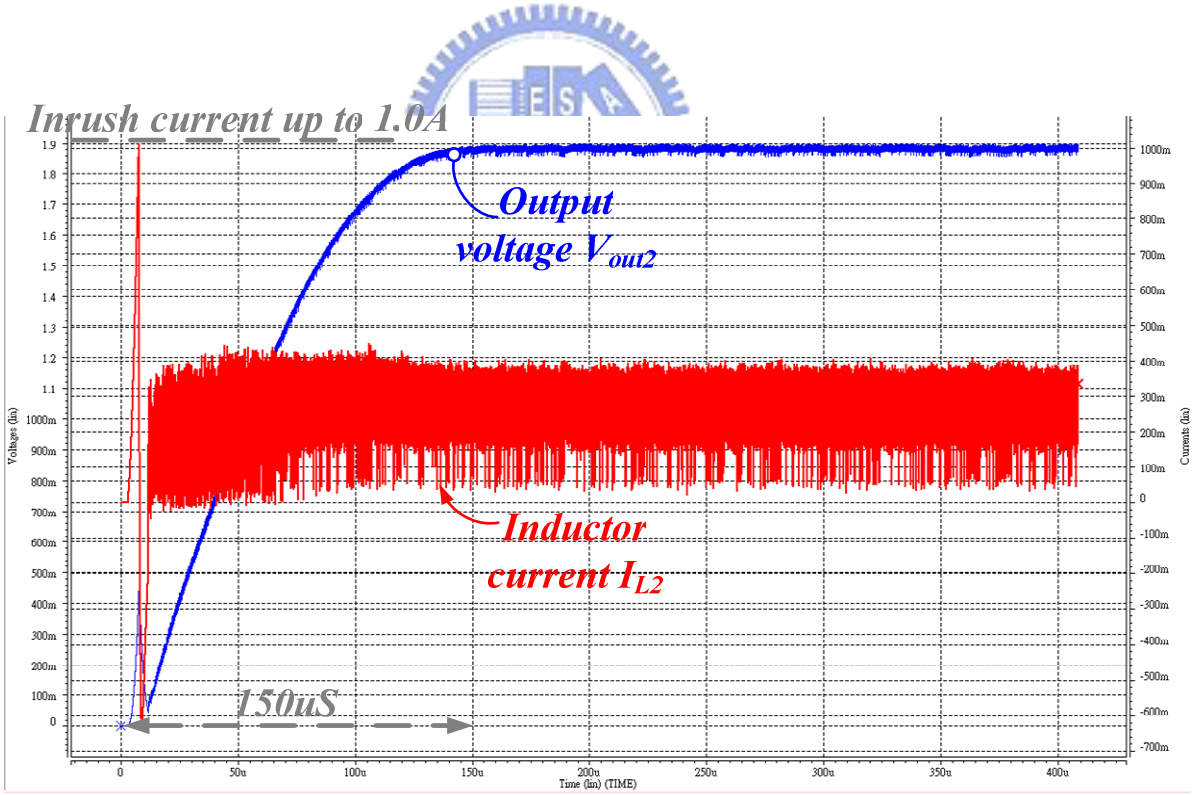


Fig. 55. The start up response waveform with soft start circuit.(@ V_{IN}=3.3V, I_{load}=250mA)

5.1.2 Steady State of Output Voltage

The simulation results of output voltage at steady state region are shown in the Fig. 56. The ideal output voltage is regulated at 2.0V, but the actual output voltage is regulated to 1.936V at the load current 50mA condition. It is because the control-to-voltage gain is not enough to regulate the reference voltage to feedback voltage; the gain of P-Compensator is much smaller than error amplifier with voltage output. The output voltage peak-to-peak ripple is 18.9mV. The output voltage ripple depends on the output capacitor ESR, the value of output capacitor ESR larger, the output voltage ripple increases synchronously. For this design, the output capacitor ESR is setting to 0.1Ω. The inductor current peak-to-peak ripple is 189mA. The inductor current peak-to-peak ripple depends on the inductor value and switching frequency. For this design, the inductor value is setting to 200nH and the inductor ESR is 0.15 Ω. Finally, the switching frequency of output voltage is up to 20MHz that is a period cycle only spends on about 50ns.

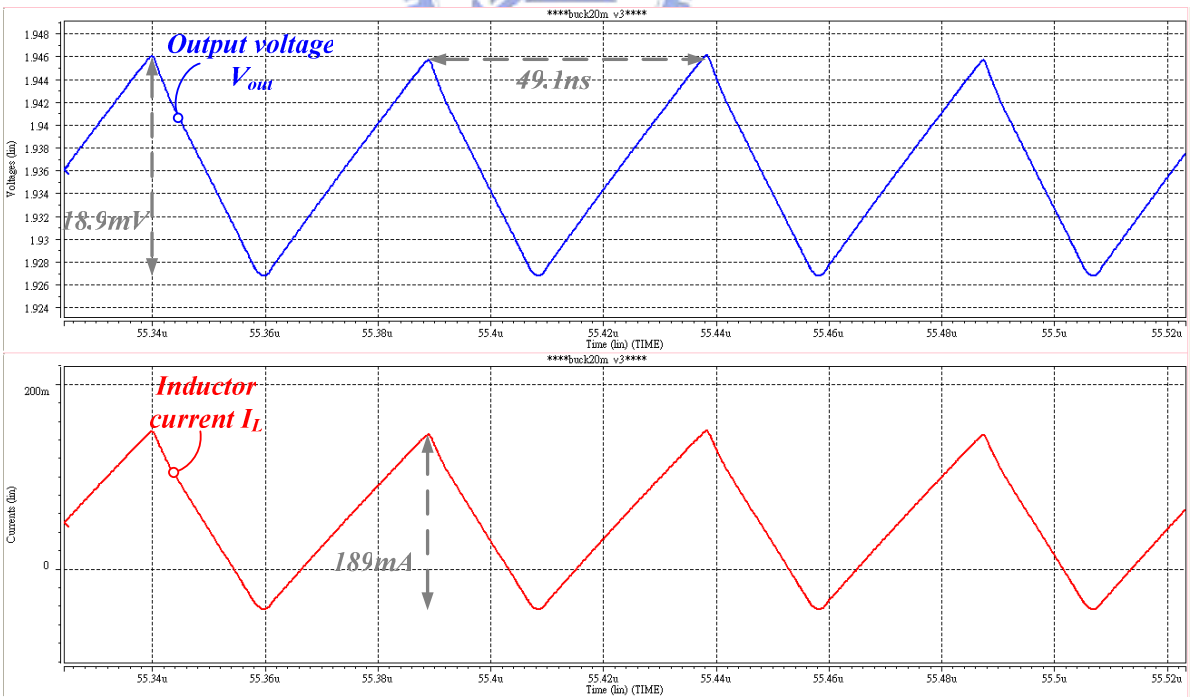


Fig. 56. The steady state output voltage and inductor current waveform. (@ V_{IN}=3.3V, I_{load}=50mA)

5.1.3 Load Regulation

Fig. 57 shows simulation results of load regulation. When load current changes form 50mA to 500mA and V_{IN}=3.3V, the output voltage varied from 1.936V to 1.853V and drops 82.6mV. The load regulation can be calculated as 0.18356mV/mA.

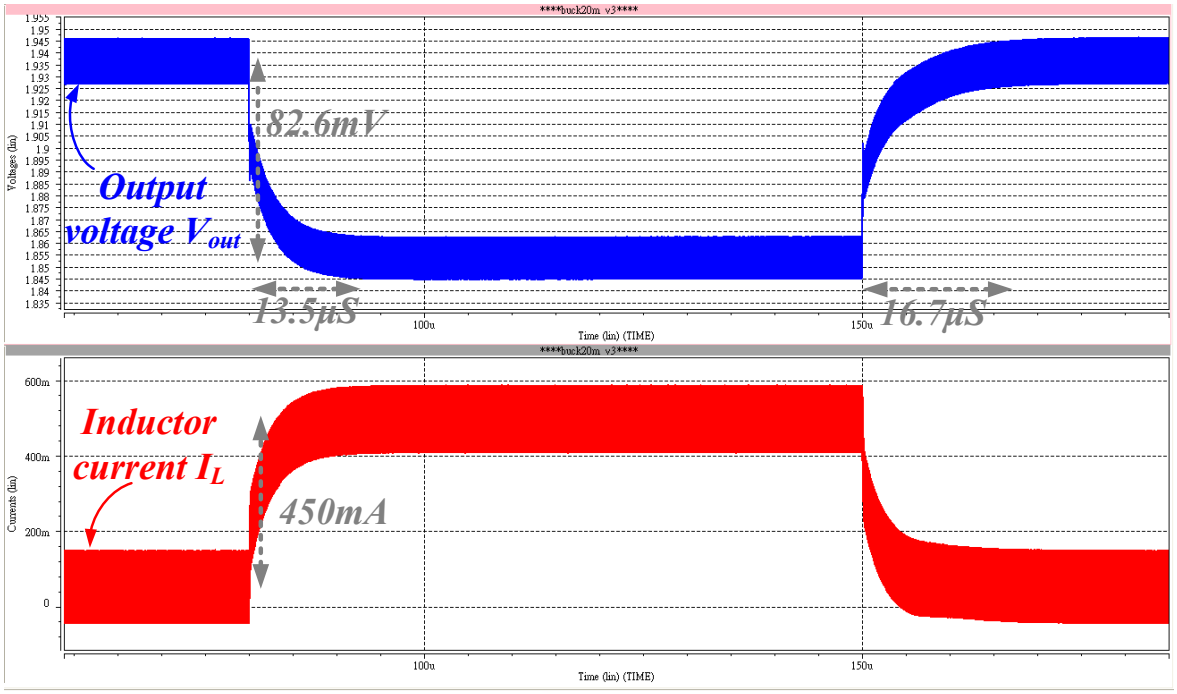


Fig. 57. The load regulation waveform (@ V_{IN}=3.3V).

5.1.4 Line Regulation

The simulation result of line regulation is shown in the Fig. 58. As the input voltage varies from 3V to 4V at load current equal to 250mA, output voltage drops 48.5mV. The line regulation can be calculated as 48.5mV/V.

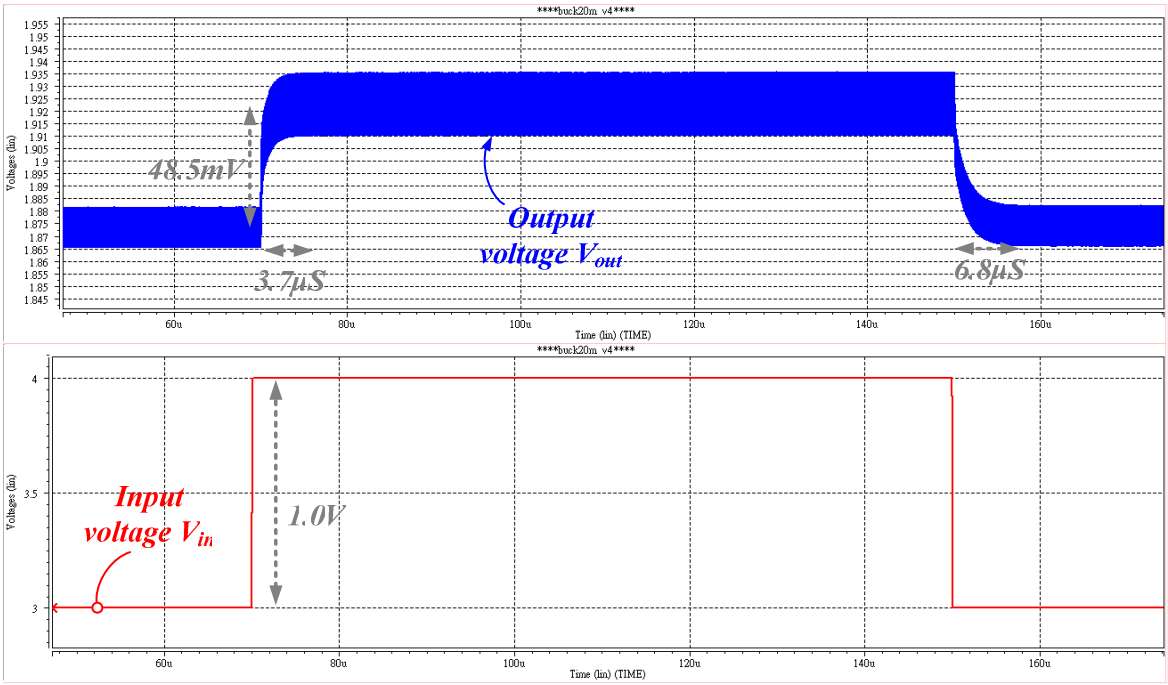


Fig. 58. The line regulation waveform (@ I_{load}=250mA).

5.1.5 Efficiency

As shown in the Eq. (94), the input power not just converts into the output power. The input power consists of the internal circuit power $\boldsymbol{P_{SYS}}$, conduction loss power $\boldsymbol{P_{con}}$, and switching loss power $\boldsymbol{P_{sw}}$ and the output power $\boldsymbol{P_{OUT}}$. When operating with PWM control, the switching loss is the main power loss in the light load condition. Because the switching power loss is fixed power loss, the efficiency is poor in the light load condition. And the main power loss is the conduction loss in the heavy load condition. Because the large current flows through the power MOSFET provides large power loss.

$$\begin{aligned} Efficiency &= \frac{P_{out}}{P_{in}} = \frac{V_{out} \times I_{out}}{V_{in} \times I_{in}} \times 100\% \\ &\approx \frac{Pout}{P_{out} + P_{sw} + P_{con} + P_{SYS}} \times 100\% \end{aligned} \tag{94}$$

The power conversion efficiency is shown in Fig. 59 at $\boldsymbol{V_{IN}}$=3.3V and the range of load current is from 50mA to 500mA.The best efficiency of high switching dc-dc buck

converter in current domain control is 82% at the load current is 200mA. The worst efficiency of the system is about 40% at load current equal to 50mA.

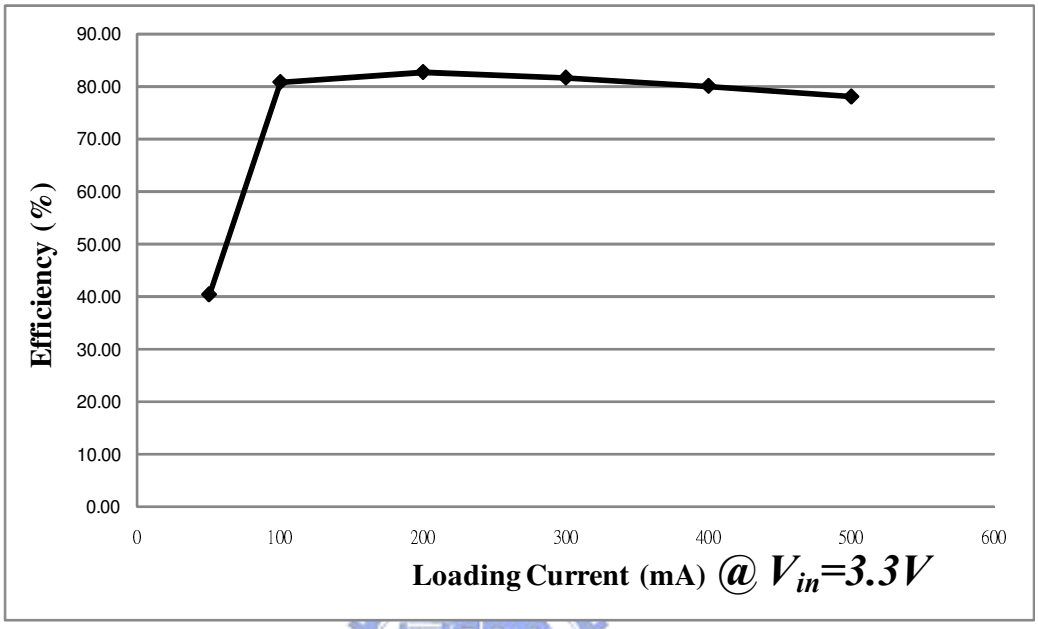


Fig. 59. The efficiency measurement in different load current condition.(@Vin=3.3V)

5.1.6 Performance and Specification

The specification and performance of the whole system simulation are listed in the TABLE IX. The feature of high switching dc-dc buck converter in current domain control is the operational frequency up to 20MHz. The design provides fast transition response however the load and line regulation error is larger than conventional current mode PWM buck converter. And it is suit for adaptive voltage position applications.

TABLE IX. SUMMARY OF SPECIFICATION AND PERFORMANCE

Specification	***Results***
Process technology	***TSMC 2P4M 0.25-μm CMOS technology***
Inductor value	***200nH***
Inductor ESR value	***0.15Ω***
Output capacitor value	***5μF***
Output capacitor ESR value	***0.1 Ω***
External sensing resistor value	***100m Ω***
Switching frequency	***20MHz***
Maximum efficiency	***82%***
Input voltage range	***3.0~4.0V***
Maximum load current	***500mA***
Load regulation	***0.18356mV/mA @ V_{IN}=3.3V***
Line regulation	***48.5mV/V @I_{load}=250mA***

5.2 Conclusions

The high switching dc-dc buck converter in current domain control is designed and presented in this thesis. When increasing the switching frequency, the inductor value can be decreased and integrated in the chip. But the conventional current mode dc-dc buck converter can not operate at such high frequency due to the bandwidth limit of operational amplifier. Under this situation, the current domain controller is presented to solve this problem. Without any operational amplifier structure to construct PWM control loop. The regulator can work in soft start mode and PWM mode. The soft start technique is important for switching regulator

to prevent the inrush current during the interval of power on state. The simple circuit structure and without any external compensation components are the features of current domain PWM controller. And operating at PWM mode ensures the high efficiency in heavy load and switching frequency achieves to 20MHz. Due to increasing the switching frequency, the transient response of system is also increased. The system is simulated by TSMC 2P4M 0.25-μm CMOS technology.

5.3 Future Work

In this thesis, the main control circuits of high switching dc-dc buck converter in current domain control are only designed in PWM mode. The efficiency of converter can achieve to 90% in heavy load condition, but poor efficiency in light load condition. Therefore, by adding the PFM control mode can improve the light load efficiency effectively. Besides, operating at high switching frequency may cause current sensing circuit responding time too short. As a result, the minimum duty ratio is limited and input voltage range is condensed narrowly. The proposed current sensing circuit for high switching frequency current mode converter must be designed. Finally, the chip layout and experimental result should be presented to prove simulation result of whole system is matching.

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