國立交通大學

電機與控制工程學系

碩士論文

切換損失計算及改良式動態斜率技術
應用於高效率多輸入單輸出系統

Switching Loss Calculation (SLC) and Improved Dynamic Droop Scaling (IDDS) Techniques for High-Efficiency Multiple-Input Single-Output Systems

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摘 要

在講求綠色能源的今天，因應多樣化的能源輸入而使得多輸入單輸出系統越來越受到重視，也因此並聯系統因為同時具備高輸出驅動能力而被廣泛的應用，在運用並聯輸入系統的時候，最主要會面臨的兩個問題就是因為每組直流轉換器的初始電壓不同而產生的並聯電流誤差，以及輕載時龐大的切換損耗所帶來的效率低落問題。

面對電流不均的問題，最簡單的方法就是運用斜率控制法，但是同時會帶來輸出電壓變動的問題，也因此，本篇論文提出了一正/負斜率補償系統，配合上動態斜率補償的機制，使得在進行均流的同時，輸出電壓可以維持在超過最小額定輸出電壓的準位，並增進輸出電壓的穩定性。

接著，為了增進輕載時的效率，本篇論文提出了一個切換功率損失計算電路，可以根據輸出電流的狀況最佳化並聯輸出的組數，此則為在輕載的時候，由於單組直流電壓轉換器即可供應輸出的電流，此切換功率損失計算電路將調整各組直流電壓轉換器的控制開關，將多餘的直流電壓轉換器關閉，以增進輕載時候的效率，而一旦進入了重載的輸出電流狀況，此電路則會再次調整控制開關，讓系統回復至並聯輸出的模式下，以減少傳導功率損失。換句話說，此正/負斜率補償輸出系統同時可以減少在進行均流時的輸出電壓下降，以及有良好的效率。

實驗結果證明了此電路在輕載的狀況下可以利用控制開關的調整，對於一個供應電壓為 5V、操作頻率為 5MHz 的系統，在輕載的狀況下提升 12%的功率，可以等效為每日降低 105g 的二氧化碳逸散。

Switching Loss Calculation (SLC) and Improved Dynamic Droop Scaling (IDDS) Techniques for High-Efficiency Multiple-Input Single-Output Systems

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Abstract

The increasing demand of green energy in today's electronic devices needs multiple input sources to deliver high driving capability to single output. Thus, parallel DC-DC converters are widely used to achieve large driving capability. When using parallel system, the major concern are the uniform current distribution caused by the initial output voltage difference and low efficiency at light loads caused by the large switching loss of each DC-DC converter. Considering the current-sharing issue, the simplest method is the droop technique, which has the drawback of increasing output voltage variation. Thus, the proposed Positive/Negative compensated (PNC) dynamic droop scaling (DDS) technique can effectively reduce the output voltage variation, thereby meeting the requirement of allowable minimum output voltage. Besides, the PNC method enhances the performance of output voltage stability.

Furthermore, the light-load efficiency can be improved by a switching loss calculation (SLC) circuit. Actually, by means of the design of SLC circuit in the PNC-DDS system, it can decide the optimum driving solution according to the loading condition. That is, more than one input source is disabled to reduce the switching loss at light loads. Contrarily, multiple input sources are preferred to reduce the conduction loss at heavy loads. In other words, PNC-DDS system with power management can achieve low drop output voltage for current sharing issue and high efficiency over a wide load range.

Experimental results show the efficiency can be improved approximately 12% at light loads when two input source are regulated at the switching frequency equal to 5MHz and 5V supply voltage while doing the good current sharing. This efficiency improvement is equal to decrease about 105g CO_2 wasting per day.

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謹以此篇論文獻給所有周遭關心我的人。

Contents

Figure Captions

Table Captions

Chapter 1

Introduction

The increasing demand of green energy in today's electronic devices needs multiple input sources to deliver high driving capability to single output. Thus, parallel DC-DC converters are widely used to achieve large driving capability. That is, the paralleling of DC-DC converter modules offers a number of advantages over a single centralized power supply. This thesis introduces the benefit of using multiple-input source single-output (MISO) system in Chapter 1.1 first. Second, when several DC-DC converters are connected in parallel, the major concern is the uniform current distribution of each converter. Two kinds of current sharing methods with different complexity and current-sharing performance are introduced in Chapter 1.2. In Chapter 1.3, the discussion of the conduction and switching losses at different loading condition is described to find out a better way for the power management control for parallel DC-DC converters.

1.1 The benefit about multiple input source single output (MISO) system

With the explosion development of integrated circuit, the consumer specification of the power system is hard to meet only by means of single power system. Therefore, the MISO system is utilized to satisfy the requirement in Fig 1.

The advantages of the MISO systems are as follows [1]. The first advantage is modeled power system. Using single power system, the designer needs to redesign the whole system when the consumer requirement is changed. However, the MISO system has the parallel modeled power system and the output power requirement can be met by just choosing the number of parallel power system modules. The second advantage is high current driving capabilities. That is, the load current of the MISO system is separated into multiple power system, thus lowers the requirement of the current driving capability for single module. The third advantage is high conversion efficiency. The power efficiency for the MISO system is better than that of the single power system since the conduction loss is greatly reduced by means of parallel connected power system [2].

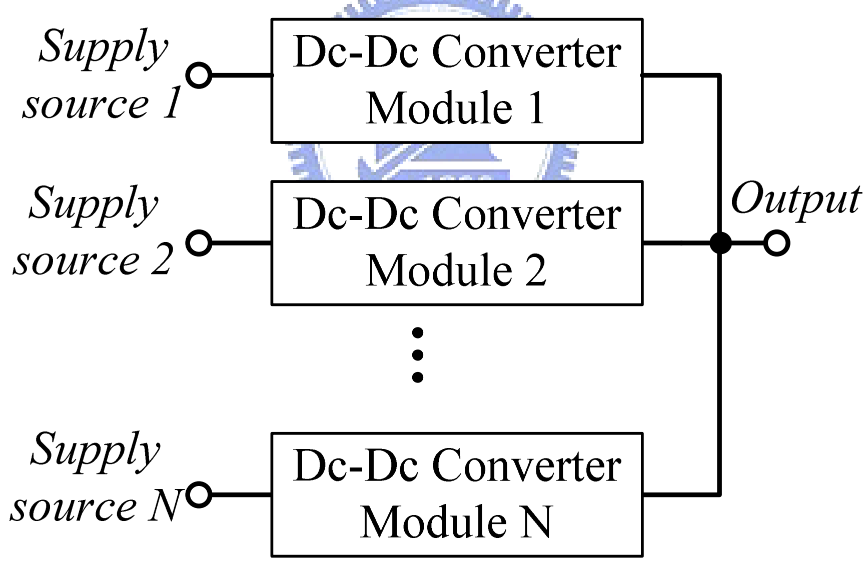


Fig. 1. MISO system.

1.2 The introduction for two majorly current sharing methods

When the MISO system is used, if the current-sharing mechanism of the converter system is not well-designed, one or more modules may bear higher load current. As a result, the reliability of the system is deteriorated and the merit of paralleled power supplies is as significant as expected. In this section, a brief introduction for two types of most common current sharing methods, which are the droop and active current-sharing methods, is presented in this section.

1.2.1 Droop Method

The principle of the droop method is to use the output resistance to form the function of current sharing [3]. In Fig 2, when the resistor R_S is connected to the output of the DC-DC converter, the current difference ΔI_O can be drive as (1).

$$\Delta I_O = \left| I_{O1} - I_{O2} \right| = \frac{\left| V_{O2} - V_{O1} \right|}{R_S} \tag{1}$$

The voltages V_{O1} and V_{O2} are the no-load output voltages of DC-DC converters and the currents I_{O1} and I_{O2} are the corresponding output currents. The voltage V_O is the output voltage of the MISO system with load resistance R_L.

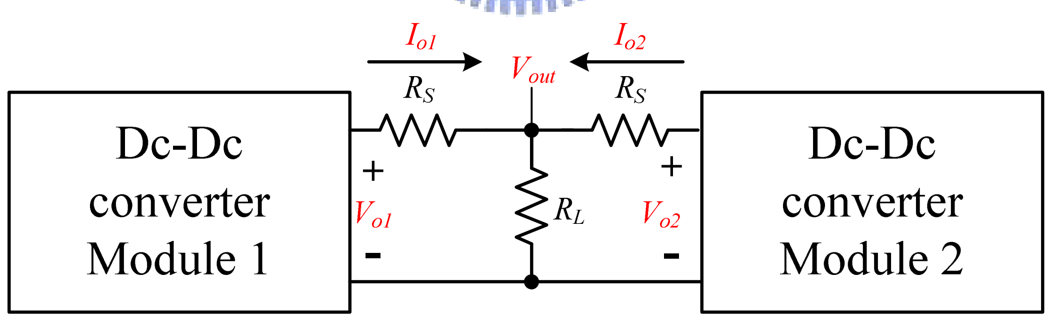


Fig. 2. The droop method by means of external resistance method.

The current sharing performance affected by no-load output voltage of DC-DC converters is shown in Fig 3(a). If the difference between V_{O1} and V_{O2} becomes smaller, the current difference is decreased too. In Fig. 3(b), a larger resistor R_S results in a better current sharing performance, but the output voltage will drop to a lower level if the same rated current is required, even that the value may be below the minimum allowable output voltage. Since the no-load output voltage of DC-DC converters can not be decided by user and will be easily affected by the process variation of the components. Thus, the droop slope is the reasonable way and the trade-off between the current sharing performance and output voltage variation becomes the major concern using the droop method.

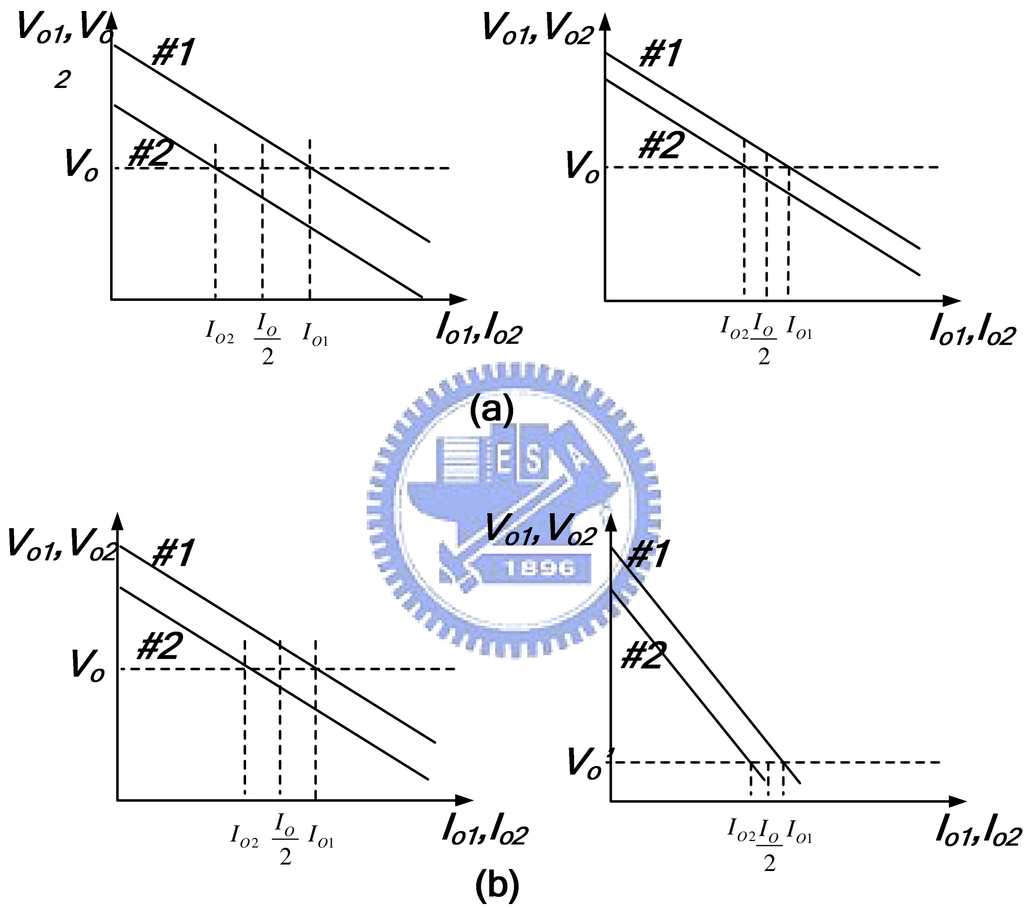


Fig. 3. The current sharing performance of droop method at (a) different output voltage for converters with no-load current and (b) different output voltage droop slope.

1.2.2 Active Current-Sharing Method

The major difference between the active current-sharing method and the droop method is the demand of an external pin to connect the current sharing bus as shown in Fig. 4. The current sharing bus conveys the output current information and provides the signal for the internal current sharing controller to adjust the output current among all the power modules [4].

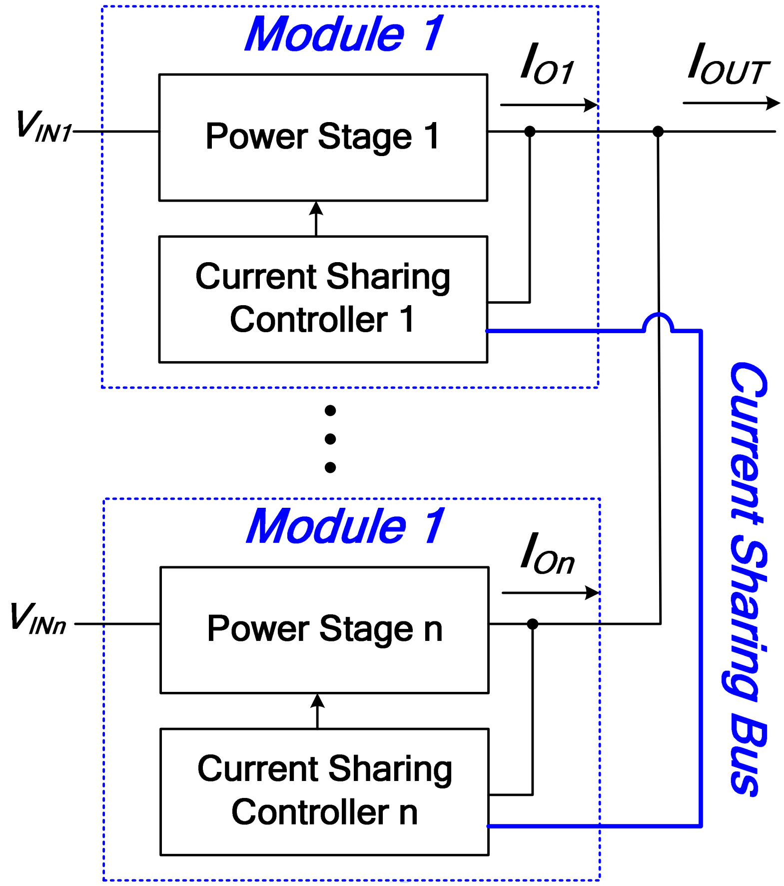


Fig. 4. Active Current-Sharing Method with current sharing bus.

The automatic master method is the common technique using the internal controller for active current-sharing method [5]. The output current information of each power module is connected to the current sharing bus by a buffer amplifier with cascading a diode for rectifying the direction of current. Thus, it forces the current signal at current sharing bus is the highest output current and all the power modules can refer to this signal to adjust itself output current. The controller used automatic master method is shown in Fig 5.

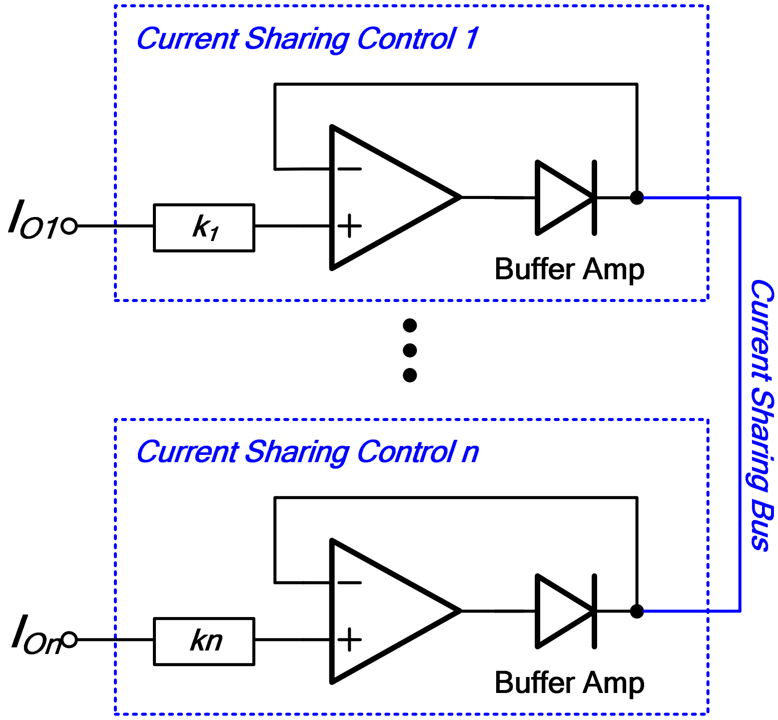


Fig. 5. The controller in Automatic Master Method

The advantages about using the Droop Method compared with Active Current Sharing Method [6] are: The circuit is simple and easy to extend. It doesn't need additional pin to connect with each power modules. The power system is easy to be modeled. The drawbacks are: The output voltage variation is increasing when larger droop slope is used. The current sharing performance will be limited by the minimum output voltage.

The advantages are superior to those of the active current sharing method. But the trade-off between the output voltage variations and current sharing performance by means of conventional method limits the popularity of droop method. It causes the designers to find a method to break through the limitation.

1.2.3 Paralleling control of power system

As we know, the conduction loss is larger than the switching loss at heavy loads [7]. It means that the parallel modules are suitable for improving conversion efficiency owing to the small conduction loss. On other hand, at light loads, the parallel modules will consumes much power than single supply module due to the large switching loss. Especially, for the power system with large-size power MOSFET, the switching loss is huge at very light loads. Thus, for a well-designed parallel system, it must contain the ability to decide how many power modules are needed to supply the output load based on the current load condition. Therefore, the parallel control system needs a switching loss calculation circuit to decide when the parallel modules have the best conversion efficiency in case of load variations. The switching loss calculation (SLC) circuit is used to implement the mechanism of power management system as illustrated in Fig. 6.

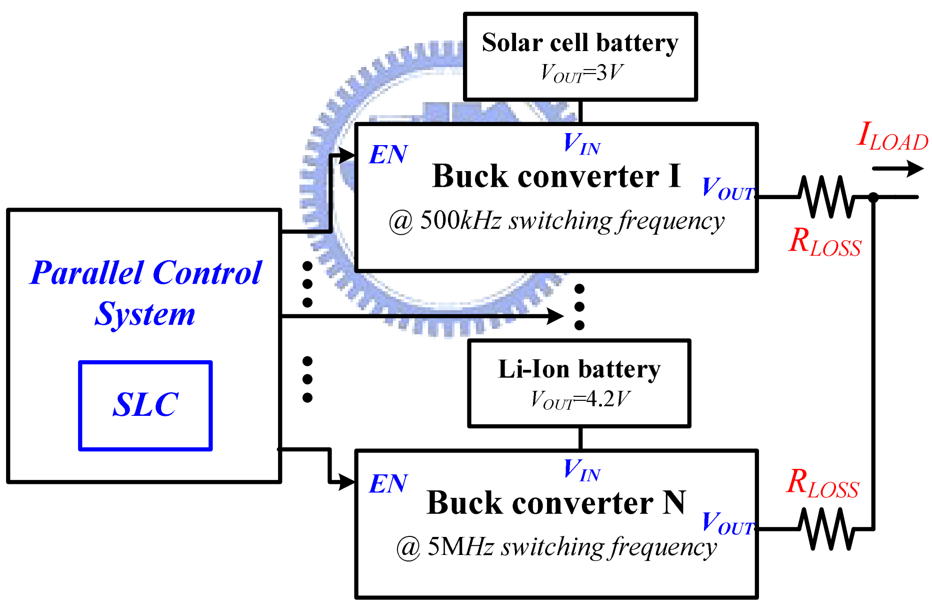


Fig. 6. Parallel control system.

These power modules can be supplied from different sources like NiH, NiCd, and Li-ion batteries or solar cells. Besides, the switching frequencies of the DC-DC converters can be different to each other. Due to the SLC circuit, the parallel control system can decide how many paralleling power modules are needed to drive the output load. Certainly, the input sources can have different voltage values and switching frequencies. In other words, the flexibility is effectively enhanced

Chapter 2

The Dynamic Droop Scaling Method

According to the previous discussion, the prior art of dynamic droop scaling (DDS) method is presented to break through the limitation of conventional droop method. The limitation of conventional droop method is described in section 2.1 and the DDS method is proposed in section 2.2. In section 2.3, the implementation of the DDS technique is presented. The voltage variation problem when using the DDS technique is discussed in 2.4.

2.1 Limitation of Conventional Droop Method

Two major parameters are the value of difference voltage ($\Delta V_{o(set)}$) of DC-DC converters at no load and the value of droop slope K when we adapt conventional droop method in parallel systems. The former is the variations between different power supply modules. The tolerance of $\Delta V_{o(set)}$ is usually controlled within ±1% value of output set-voltage $V_{o(set)}$ in specification. Fig. 7 shows the relationship for output current and voltage of the droop method. In Fig. 7(a), the design margin for droop method is limited to $\Delta V_{o(drp)}$, which is written as equation (2).

$$\Delta V_{o(drp)} = I_{o(rate)} \cdot K = \Delta V_{o(\max)} - \Delta V_{o(set)} \tag{2}$$

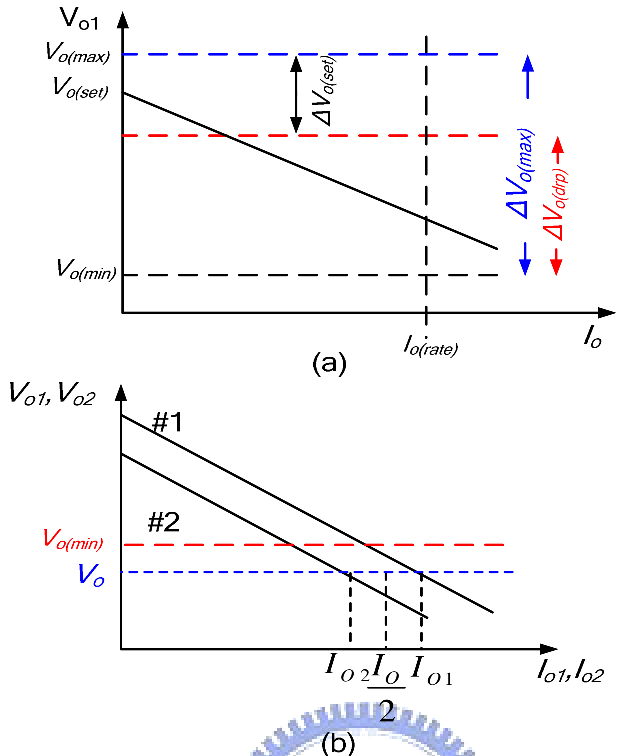


Fig. 7. Definition of dropout voltage.

$I_{o(rate)}$ is rated current load, $\Delta V_{o(max)}$ is maximum allowable output voltage variation of the DC-DC converter systems. From Fig. 7(b), the maximum current deviation between two power supply modules is inversely proportional to the value of K and can be driving as equation (3).

$$\Delta I_o = I_{o1} - I_{o2} = \frac{\Delta V_{o(set)}}{K} \tag{3}$$

It means that the larger value of K is, the smaller deviation between two power supply modules is. However, owing to the steeper slope of droop method, the voltage variation will exceed the minimum allowable output value $V_{o(min)}$ at rated current load. In other words, there is trade-off between error percentage of current sharing and output voltage variation.

2.2 Dynamic Droop Scaling Technique

The major problem of conventional droop method is the limitation of the value of droop slope. Thus, dynamic droop scaling (DDS) circuit shown in Fig. 8 is added to the output of converters to exceed the limitation of conventional droop method [8]. The external resistor is composed of the on-resistance of ORing MOSFET [9], which is used to prevent the individual power supply module from burning out because of short circuit. The increment of load current increases the value of ΔV_C by flowing through the $R_{ds(on)}$ of ORing MOSFET, and therefore the output current of transconductor Gm also increases. Thus, the load current condition of the DC-DC converter can be obtained and will be used to improve the current sharing performance..

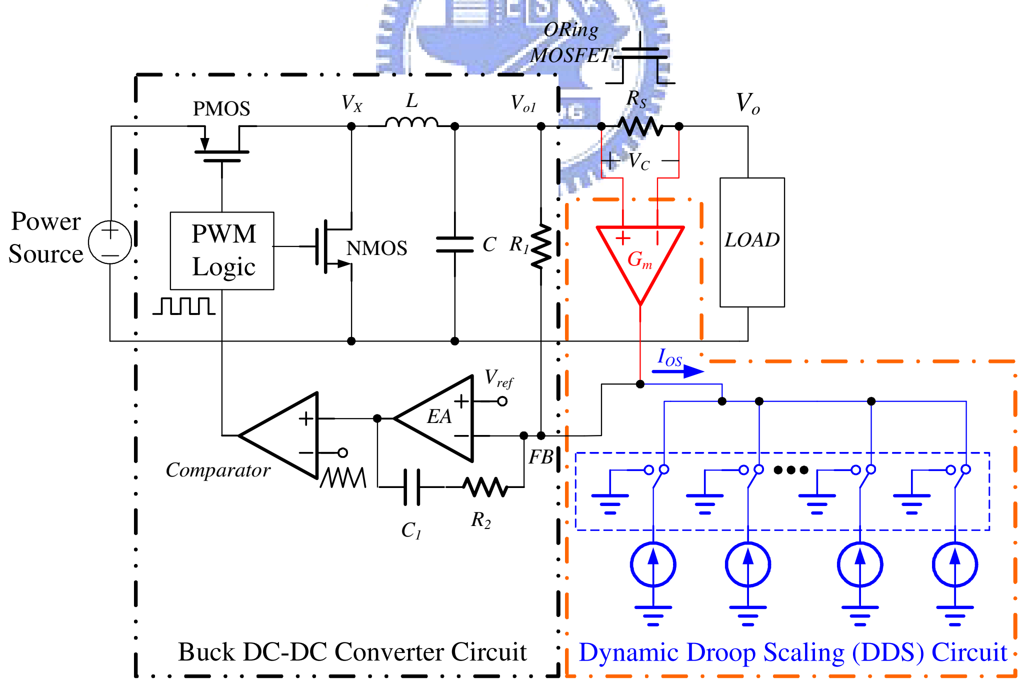


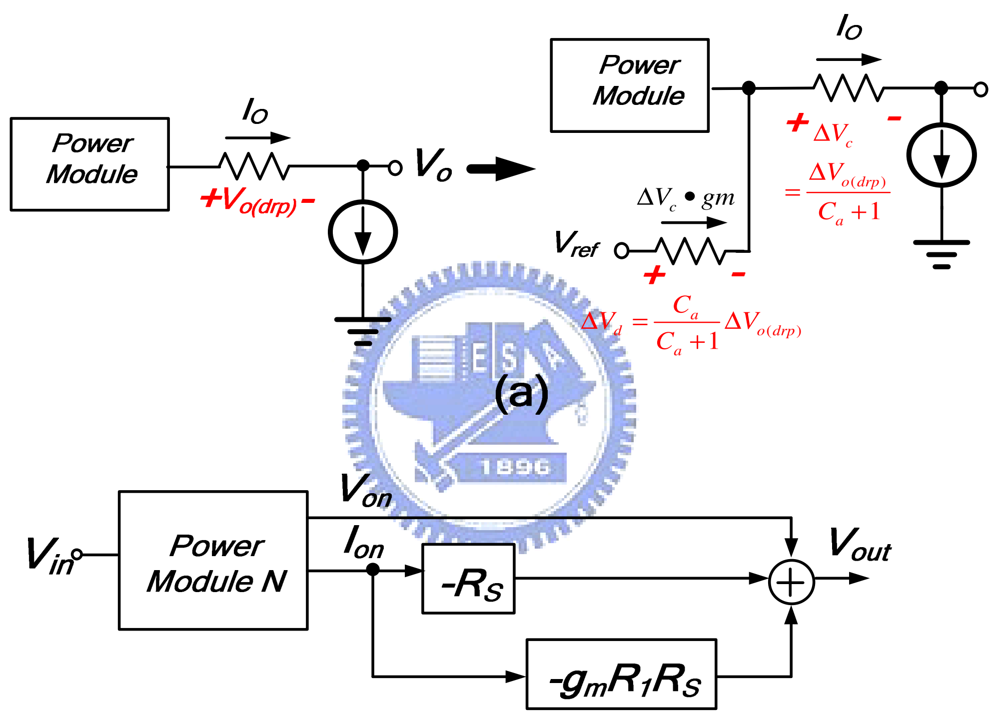
Fig. 8. Current sharing controller with DDS technique in single power module.

2.2.1 Principle of Dual Current Sensing Loop

Because of the negative feedback effect, the negative terminal of the error amplifier is close to the value of $V_{ref,}$ and the current generated by transconductor will only flows through resistor R_1 to generate a voltage drop, which is equal to ΔV_d. The total voltage drop due to the increment of load current is the sum of ΔV_C and ΔV_d. In Fig. 9(a), we can write the new droop slope K_a as equation (4):

$$K_a = \frac{\Delta V_c + \Delta V_d}{I_{o(rate)}} = \frac{I_o R_s + I_o R_s g_m R_1}{I_{o(rate)}} = R_s(1 + g_m R_1) = R_s \cdot (1 + C_a) \ (3) \qquad (4)$$

where C_a is equal to $g_m R_1$



(b)

Fig. 9. Modified droop technique to reduce the power dissipation on sensing resistor R_s (a) Insertion of another sensing loop to conventional droop technique. (b) Flow diagram of new dual sensing loop of DDS technique

Fig. 9(b) shows the flow chart of dual sensing loop. It means that the value of new droop slope is $(1+C_a)$ times of conventional droop slope and the variations of $R_{ds(on)}$ values for different ORing MOSFETs can be compensated by the term of $g_m R_1$ in equation (4). We don't need to put much effort on selecting the perfect matching external components for whole multiple-supplies system. Furthermore, owing to the larger value of droop slope K_a, the error percentage of current-sharing performance is reduced by a factor $(1+C_a)$.

$$\Delta I_{o(\max)} = \frac{\Delta V_{o(set)}}{K_a} = \frac{\Delta V_{o(set)}}{K \cdot (1 + C_a)} \tag{5}$$

Compared with conventional droop method, the DDS technique consumes less power because only $\Delta V_{o(drp)}/(C_a+1)$ is dissipated by ORing MOSFET. The rest voltage drop $[\Delta V_{o(drp)}C_a/(C_a+1)]$ is dissipated by resistor R_1. Fortunately, the current flowing through resistor R_1 is only $I_oR_sg_m$, which is far smaller than I_o.

2.2.2 Incremental Output Voltage Loop

Generally speaking, the enhanced droop slope K_a deteriorates the minimum allowable output voltage at rated load current as shown in Fig. 10(a). Therefore, in order to keep output voltage of DC-DC converters within the range of minimum allowable output voltage and maximum allowable rated current, it is needed to raise the output voltage about $\Delta V_{o(drp)}$ for every $I_{o(rate)}/(C_a+1)$ current increment of output current. In Fig. 10(b), when the load current transits from region I to II, we raise the output voltage about $\Delta V_{o(drp)}$ to meet the specification. Equation (6) and (7) describe the operation between two regions.

$$V_o = V_{ref} - I_o \cdot K_a \text{ where } I_o < \frac{1}{(C_a+1)} \cdot I_{o(rate)} \tag{6}$$

$$V_o = V_{ref} + \Delta V_{o(drp)} - I_o K_a \text{ where } \frac{1}{(C_a+1)} \cdot I_{o(rate)} < I_o < \frac{2}{(C_a+1)} \cdot I_{o(rate)} \tag{7}$$

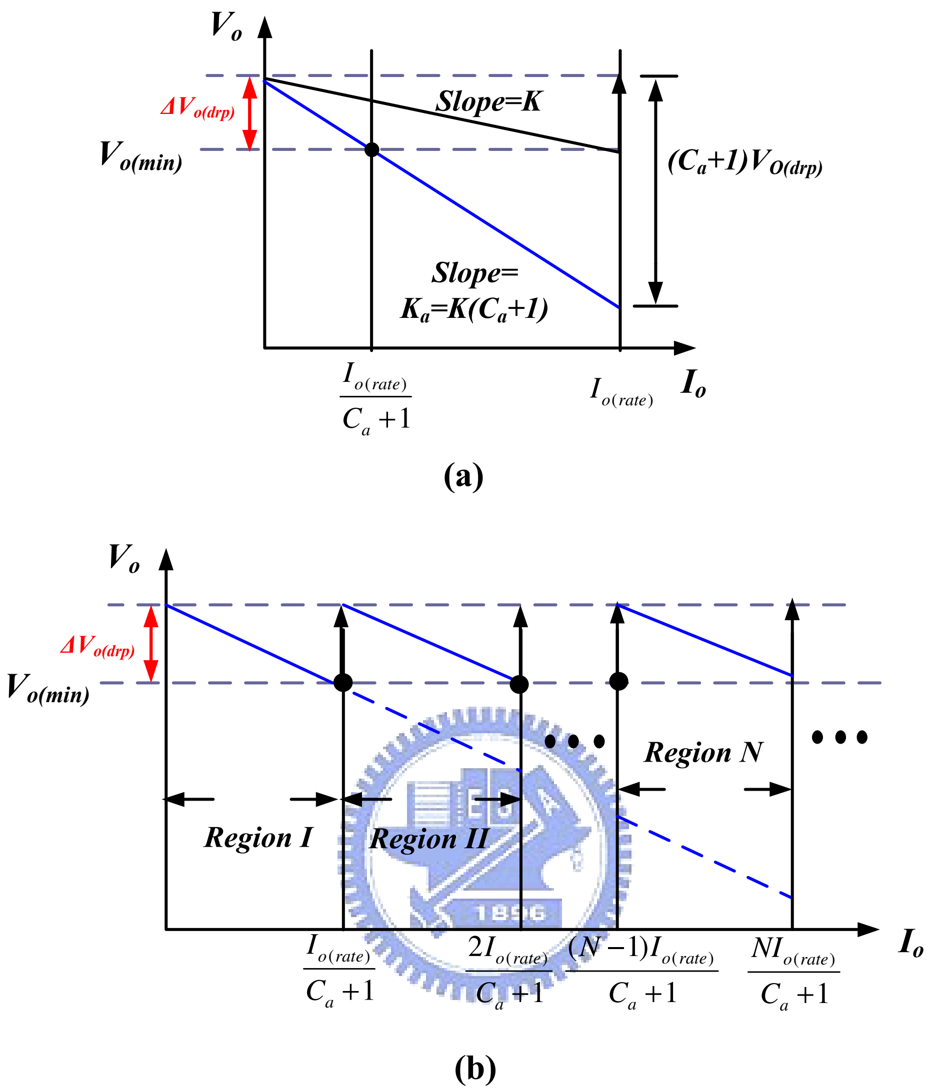


Fig. 10. Operation of DDS technique.

By extending two raising regions to C_a+1 raising regions according to the new drop slope, the load current and output voltage V-I waveform is shown in Fig. 11. Owing to the compensation for extra voltage drop of C_a+1 raising region, the droop scale can be increasing to (C_a+1) times of original and the error percentage of current-sharing performance can be shrunk to only 1/(C_a+1) times that of the conventional droop method.

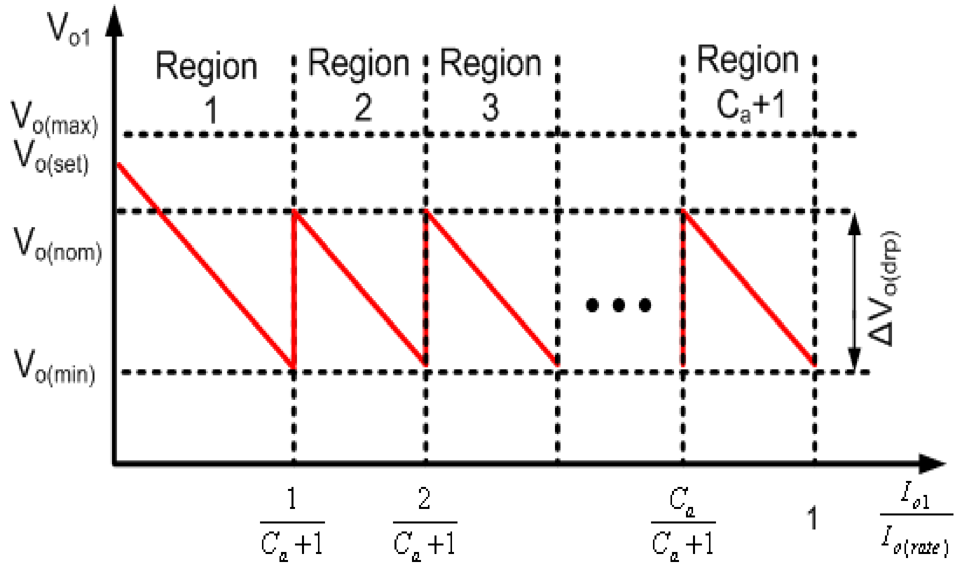


Fig. 11. C_a+1 raising voltage region for breaking through the limitation of conventional droop technique.

2.3 The Implementation of DDS Technique

The implementation of dynamic droop scaling technique is composed of the high linearity transconductor and the incremental output voltage circuit. High linearity transconductor defines low power dissipation performance of droop technique and the circuit of incremental output voltage will break through the limitation of conventional droop technique.

2.3.1 High Linearity Transconductor

The linearity of transconductor is important in dynamic droop scaling technique. In Fig. 12, the output current of transconductor decides the droop slope of every power supply module. Thus, for the system with the i^{th} power module shown in Fig. 12, the linearity of transconductor decides the error current among these supply modules. In order to improve the linearity of the transconductor, the flipped voltage follower (FVF)

[10] technique is used to reduce the output impedance. In Fig. 13, input differential pairs are composed of flipped voltage follower pairs, which are (M_1, M_3) and (M_2, M_4). It means that the linearity of the transconductor can be improved by the characteristic of low output impedance of FVF. Furthermore, after the conversion of transconductor G_m, S/H circuit samples the load current every switching period and hold this value as $I_{ogm,avg}$, which is written as equation (7) and shown in Fig.12.

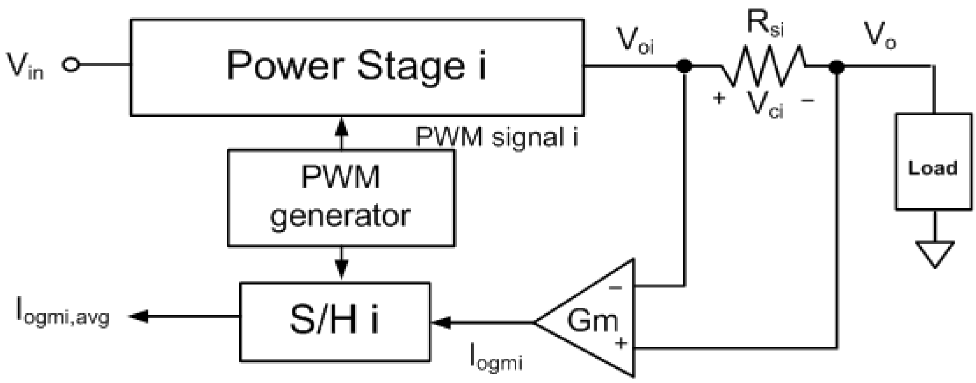


Fig. 12. Dynamic droop scaling technique in the i^{th} power module.

$$I_{ogm,avg} = I_o R_s g_m \tag{8}$$

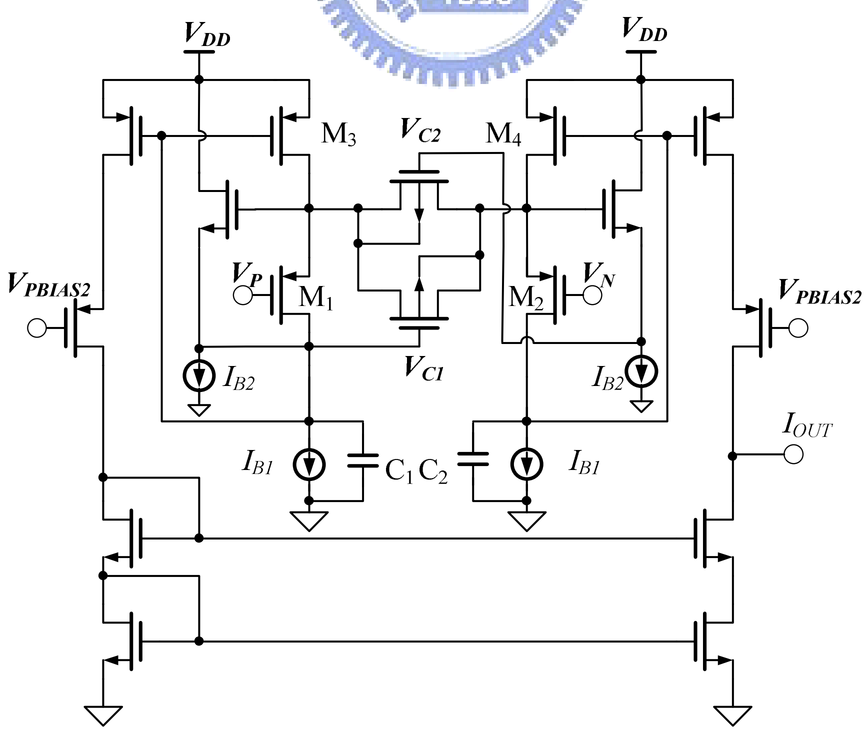


Fig. 13. Modified FVF technique in transconductor G_m.

The average current $I_{ogm,avg}$ is mirrored to two current branches. One is sent to error amplifier for the operation of droop method in Fig. 8. The other one is sent to incremental output circuit to decide the operating region.

2.3.2 Circuit of Incremental Output Voltage

Fig. 14 shows the circuit of incremental output voltage, which contains a current mirror, a smite trigger to be the current comparator array, and an adder of raising current. The average current $I_{ogm,avg}$ sampled from output current of DC-DC converter is sent to compare with reference current sources from $1/(C_a+1)I_{REF}$ to $C_a/(C_a+1)I_{REF}$ to determine the increment current I_{os}. The raising current I_{os} flows through resistor R_1 in Fig. 8 to generate constant voltage drop $\Delta V_{o(drp)}$, and therefore provides the extra compensation voltage ΔV_{os} at the transition point of C_a+1 raising regions. The value of ΔV_{os} relies on the new drop slope as equation (9):

$$\Delta V_{OS} = \Delta V_{o(drp)} \cdot (C_a + 1) \tag{9}$$

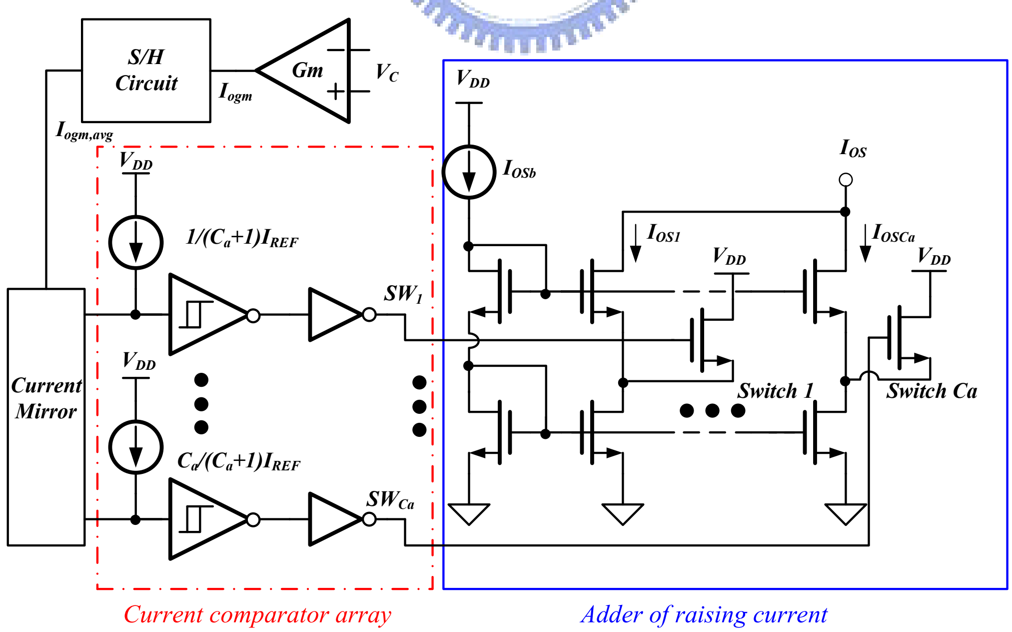


Fig. 14. Schematic of circuit of incremental output voltage is composed of a current r
current comparator array, and a adder of raising current.

For example, the new droop scale is set to *Ca* times the value resulted form the conventional method, offset current source is composed of *Ca* identical current sources from I_{os1} to I_{osCa}. As the result, the decision codes (SW_1~SW_{Ca}) will be sent to current mirror array with a sequence. The switches from switch 1 to switch *Ca* are turned on according to the operating region decided by $I_{ogm,avg}$ which is proportional to the output current of DC-DC converters. In other words, the larger the load current is, the more switches are turned on and the output voltage will be compensate with more ΔV_{os}. Owing to the implementation of incremental output voltage circuit, the output voltage will not exceed the allowable minimum output voltage at rated load current.

2.4 The voltage variation problem when using the DDS technique

Because of the reference voltage of error amplifier internal of the DC-DC converter can not be obtained while using DDS technique, using the feedback loop of the converters to adjust the output voltage for doing current sharing work is the better way. Taking the buck converter to be example, Fig. 15 shows the implementation of using the DDS technique to do the current sharing. For R_{FB1} and R_{FB2} is the feedback resistance of the buck converter, the feedback voltage will be regulated by internal error amplifier to V_{ref} [11] which is generated by the bandgap circuit in buck converters when the system is in steady state. Where V_{ref} can be calculated as:

$$V_{ref} = V_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} V_{o(set)} \tag{10}$$

The droop enhancement current I_{ogm} will source to the feedback pin of buck converter making the current that flow through the R_{FB1} decrease and provide the additional voltage drop to output voltage of buck converter.

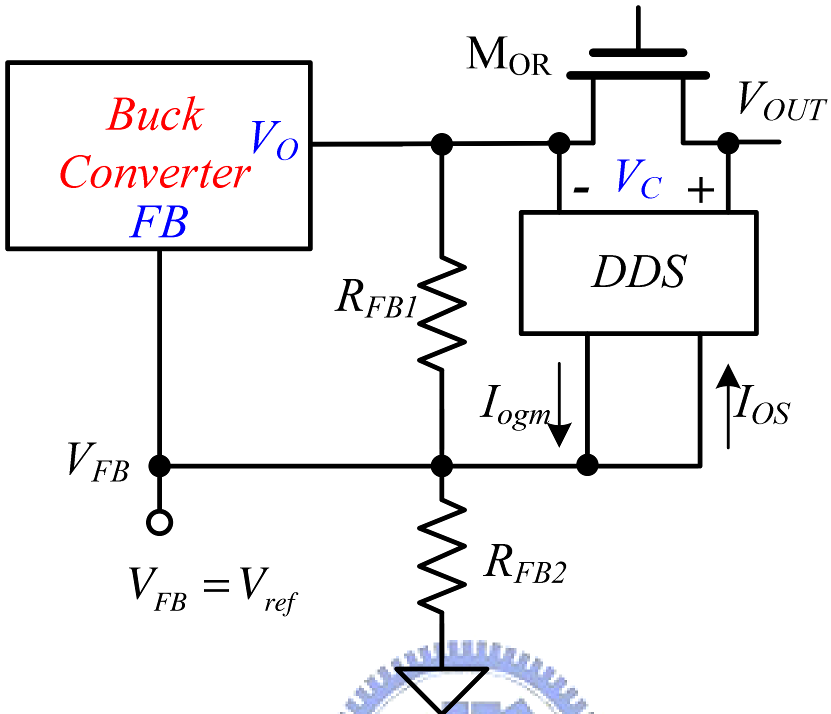


Fig. 15. Using DDS technique in buck converter

And the compensate current I_{OS} will sink from the feedback pin providing the ΔV_{os} voltage raise to output voltage. In other words, the V_{FB} and the R_{FB1} will be the V_{ref} and R_1 in Fig. 8. A stability problem is needed to be mentioned when the DDS technique is used to a DC-DC converter. Because of any small distribution at feedback pin makes the converter having transition response, the sharp dc current change cause by the incremental output voltage circuit in Fig. 11 will produce a DC voltage drop at feedback pin and make the system into transition state [12]. If the output current of the DC-DC converters change rapidly and widely, the system will keep taking transition response and make the output voltage to have variation problem. The variation of the output voltage can be huge according to the transition performance of DC-DC converters and the current change of incremental output voltage circuit, that will effect the current sharing performance and need to be improved by finding a better way to compensate the output voltage drop by the DDS technique.

Chapter 3

The theory of PNC method and SLC circuit

From the discussion in Chapter above, there is two problem need to be concern about. In Chapter 1, the switching loss problem at light load condition for parallel converters has been point out that need to find a dynamic control method to improve light load efficiency. And in Chapter 2, the output voltage variation problem needs to be deal with when the DDS method is using to enhance the droop slope for better current sharing performance. The positive/negative compensate (PNC) method will be introduced in Chapter 3.1 to make the compensate current of incremental output voltage transit smoothly, reduce the output voltage variation. And the analysis about using PNC method on buck converters will be presented in Chapter 3.2. In Chapter 3.3, the loss analysis on a modeled buck converter will be introduced. Finally, the theory about switching loss calculation (SLC) circuit will be presented to provide a really good method improving the efficiency of the parallel buck converters at light load condition in Chapter 3.4.

3.1 The theory about positive/negative compensate (PNC) method for voltage compensate circuit

In the DDS, the steeper droop slope has a better current sharing performance due to the large droop resistor. However, the voltage variation may exceed the allowable minimum output value $V_{o(min)}$ at rated current load $I_{o(rate)}$ as depicted since the large voltage drop across the large droop resistor. In other words, there is a trade-off between the error percentage of current sharing and the output voltage variation. Thus, the voltage incremental circuit is involved in the DDS technique to break through this limit. As shown in Fig. 16(a), the conventional method in DDS has two major drawbacks. The output voltage at the transition currents will be undefined causing the stability problem and the sharp waveform deterioration the output voltage variation problem decreasing the current sharing performance.

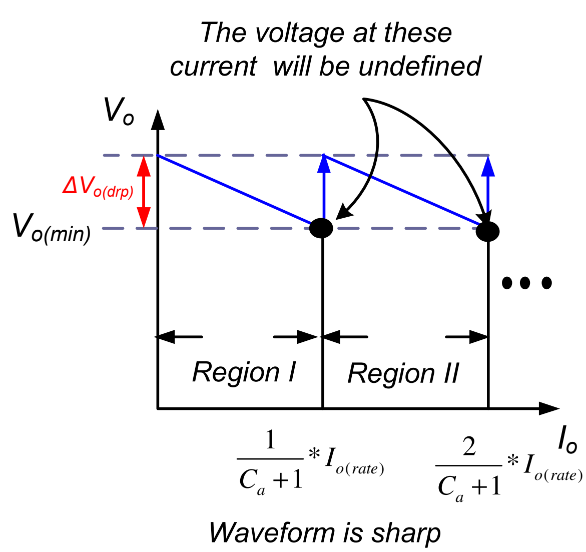


Fig. 16. The sharp output voltage to load current waveform.

To solve this problem, the compensation method should not only add a DC voltage raise to the output voltage when it drop to $V_{o(min)}$ during the output current increasing. In order to smooth waveform, the compensation voltage can not be raised instantly and a compensation region should be created. The variation of the output voltage near the transition current need to decrease as much as possible, it means the condition of output current must be considered for being a element of the compensate voltage. Since the $V_{o(min)}$ is reached, using the positive droop slope for compensation region of output waveform is the only way. While designing the compensation region, we still need to mention that the slope of waveform effect the current sharing performance directly. Fig. 17 show the waveform of different design of output voltage, the even region is compensation region. In Fig. 17(a), smaller compensation slope of the output voltage smooth the waveform but the current sharing performance be worse than original. With bigger slope in Fig. 17(b), the number of transition current is increased due to more regions are created and the circuit design difficultly is increased. At the same time, the current sharing performance will not be same in different region causing the stability problem.

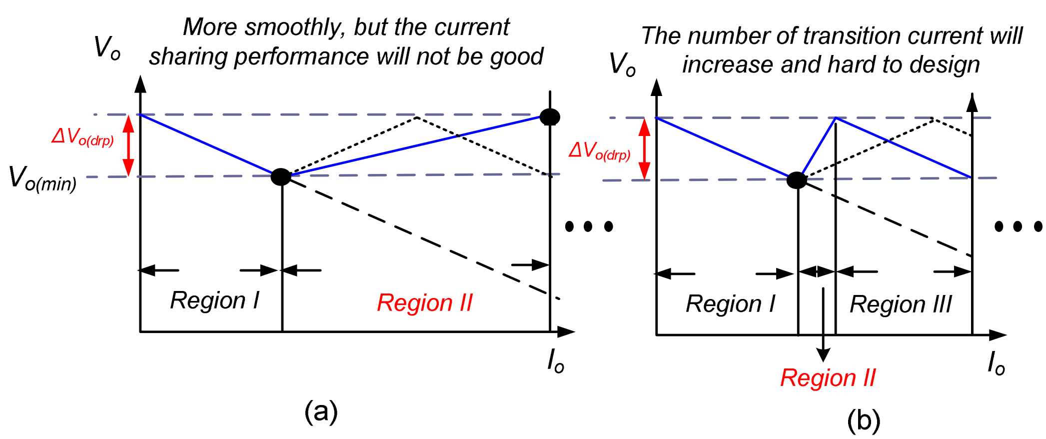


Fig. 17. The waveform of output voltage for different design in compensation region (a) smaller slope (b) bigger slope

Thus, the improved DDS (IDDS) technique with the new positive-negative compensation (PNC) method is presented in Fig. 18. According to the PNC method, the rated current is divided into C_a+1 regions within the allowable output voltage variations and the transition current keep the same with original DDS technique by just turning the even region in Fig. 10.(b) to be the compensation region. The slope K_a of each odd region is $-\Delta V_{o(drp)}(C_a+1)/I_{o(rate)}$. On other hand, each even region has a slope of $\Delta V_{o(drp)}(C_a+1)/I_{o(rate)}$ where C_a is the magnification factor for increasing the droop slope in the DDS technique.

$$K_a = -\Delta V_{o(drp)}(C_a+1)/I_{o(rate)} \quad \text{for Reigon I, III, V.....} \tag{11}$$

$$K_a = \Delta V_{o(drp)}(C_a+1)/I_{o(rate)} \quad \text{for Reigon II, IV, VI.....} \tag{12}$$

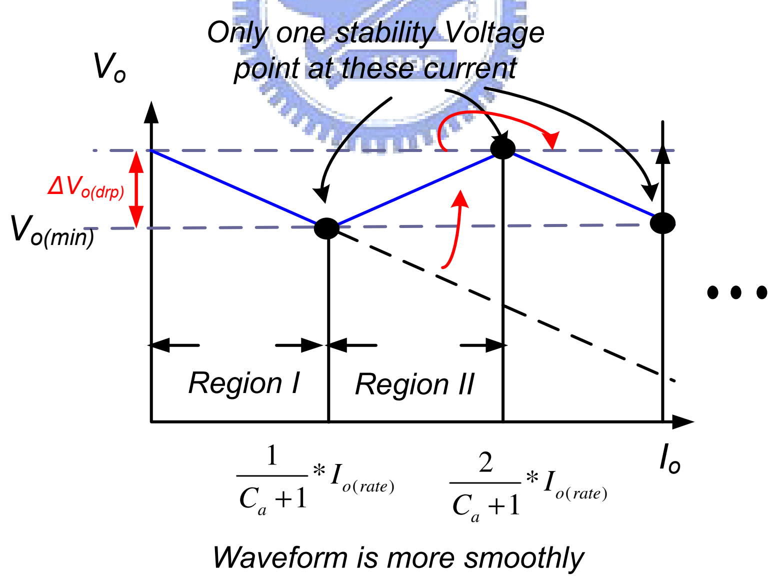


Fig. 18. The theorist PNC waveform for voltage compensation.

The transition from two different regions causes the droop slope has different signs in order not to exceed the allowable output voltage variations. And the slope in compensation region is same with the original droop enhanced by DDS to keep the current sharing performance. Certainly, the IDDS technique has a more stable operation than the previous DDS technique due to the smooth transition between two different regions. It can extend the rated current load within the allowable output voltage variations and will not cause the output voltage variation problem.

3.2 Analysis for using PNC method for buck converters

Take buck converters to be example, the discussion can be divided into two parts as analysis for single buck converter and analysis for parallel buck converters.

3.2.1 Analysis of single buck converter

Continued from the previous discuss in Chapter 2.4, let us consider the saturation for single buck converter first. Using the PNC method for buck converter can be analyzed in Fig. 19

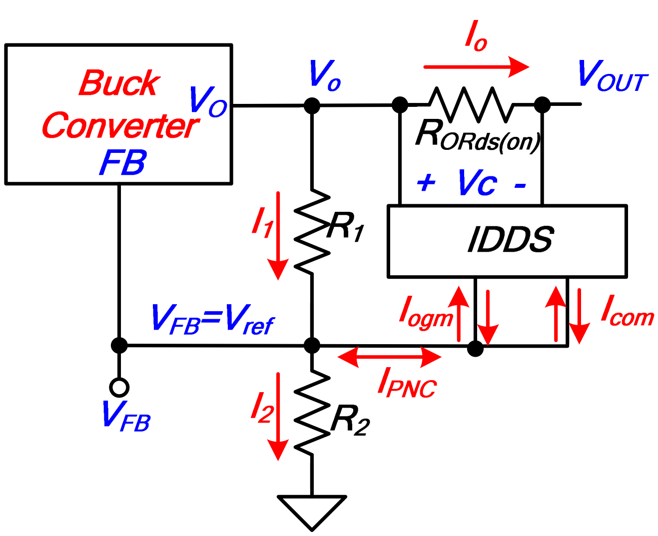


Fig. 19. The analysis for using PNC method for single buck converter.

R_1 and R_2 are the feedback resistors of the buck converter. Because the V_{FB} is regulated to V_{ref} by the internal circuit in the buck converter, the current I_1 and the original output voltage $V_{o(set)}$ can be calculated by let I_2=I_1 as follow [13]:

$$I_2 = \frac{V_{ref}}{R_2}, V_{o(set)} = V_{ref} + I_2 R_1 \quad (13)$$

For R_s is the $R_{ds(on)}$ of the ORing MOSFET providing the original droop slope, I_o is the output current of the converter, the current I_{ogm} is the current shown in equation (8) which is generated by the transconductor in DDS circuit and the current I_{PNC} is the droop enhancement current from IDDS circuit mixed with the compensation current I_{com} and I_{ogm}. The new output voltage V_o of buck converter can be derived as follow:

$$V_o = V_{ref} + I_1 R_1 \quad (14)$$

Since the FB pin of buck converters will not sinking or sourcing current from V_{FB} and the current I_2 is regulated at stately state as equation (13), I_1 can be calculated from equation(15):

$$I_2 = I_1 + I_{PNC} \quad (15)$$

If the I_{PNC} is positive meaning the current is sourcing to the V_{FB} pin, the current I_1 will be lesser than I_2 resulting in the V_o<$V_{o(set)}$ from the comparison with equation (13) and (14), and if it is negative meaning the current is sinking from the V_{FB} pin, the V_o>$V_{o(set)}$ will be the result. Consider saturation that the current I_{PNC} is increasing, the output voltage waveform will get a negative slope because of the decreasing current of I_1. On the other hand if the I_{PNC} is decreasing, the output voltage waveform will have a positive slope due to the increasing value of I_1.

It seems that the current I_{PNC} is the key elemental of the PNC method and the design of I_{PNC} is most important part overall. The analysis of I_{PNC} is shown in Fig. 20.

Consider a buck converter "Buck L" with the lowest original output voltage

$V_{oL(set)}$, the maximum voltage drop range is $\Delta V_{oL(drp)}$ and the rate current is $I_{oL(rate)}$ with the output current of I_{ogmL} from the transconductor in IDDS. For *(Ca+1)* times enhancement from original droop slope, the rate current is separated into *(Ca+1)* Region and need to be compensated due to additional voltage drop. The waveform of V_{+IgmL} is produced by sinking the current I_{+gmL} which is proportional to I_{ogmL} from V_{FB} pin. Otherwise sourcing the current I_{-gmL} being proportional to I_{ogmL} to the V_{FB} pin will generate the waveform of V_{-IgmL}. The triangle waveform that is the final result in PNC method can be composed with taking part of waveform in V_{-IgmL} and V_{+IgmL}. But there are still two major concern need to be deal with, the voltage drop at the on-resistance of ORing MOSFET R_s and the DC voltage difference.

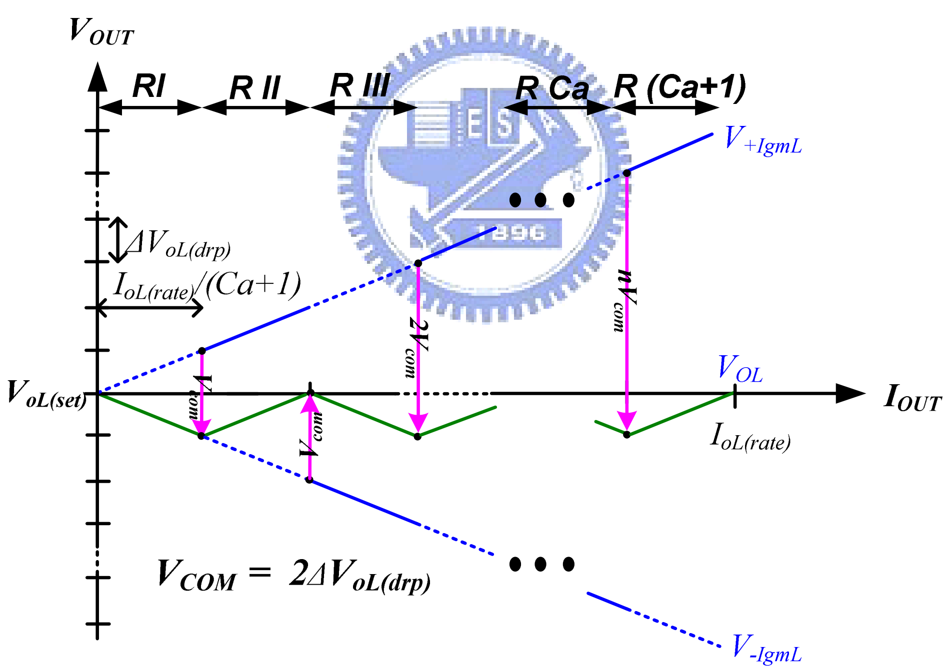


Fig. 20. the composed triangle waveform in PNC method

Let us consider the (C_a+1) times enhancement droop slope in DDS, the C_a times voltage drop is provided by controlling the current I_1 and the original one times slope is provided by the R_s. If the positive (C_a+1) times slope is need, the current I_1 must produce (C_a+2) times slope by flowing through the R_1 to overcome the original slope.

From the discussion above, the current I_{-gmL} and I_{+gmL} will have the relationship as follow:

$$I_{+gmL} = kI_{ogmL}\text{, where k is a constant} \tag{16}$$

$$I_{+gmL} = \frac{C_a + 2}{C_a} I_{-gmL} \tag{17}$$

The other problem comes from the DC voltage difference from the waveform of V_{-IgmL} and V_{+IgmL}. Although the positive and negative slope can be composed by the waveform of V_{-IgmL} and V_{+IgmL} but a compensation voltage V_{com} is required to shift the DC voltage level at transition currents to make the continued triangle waveform. Since the voltage drop in every region is $\Delta V_{oL(drp)}$, the compensation voltage V_{com} can be calculated at different transition currents in Fig. 20 as follow:

$$V_{com} = 2nV_{oL(drp)}\text{, where } n = \left[\frac{N}{2}\right] \text{ for region N} \tag{18}$$

This compensation voltage can be generated by adding a current I_{comL} to flow through the R_1 additional to I_{+gmL} or I_{-gmL}. Finally, the compensation current I_{PNCL} that can produce the triangle waveform for a single buck converter can be derived in equation (18), (19).

$$I_{PNCL} = -1^{N-1} I_{gmL} + I_{com} \text{ for region N} \tag{19}$$

$$\begin{cases} I_{comL} = 0 \quad \text{for region 1} \\ I_{comL} = \sigma \bullet \left[\frac{N}{2}\right] \bullet \frac{2\Delta V_{oL(drp)}}{R_1}\text{, where } \sigma = \text{-}1^N \text{ for region N} \end{cases} \tag{20}$$

3.2.2 Analysis for parallel buck converters

For the parallel buck converters system, we need to consider the synchronization problem. If all of the buck converters are not operated in positive region or negative region at the same time, the output voltage difference between each buck converters will increase and deterioration the current sharing performance. Thus the better way to control the whole system is transiting all the parallel buck converters at the same time. Otherwise the compensation current I_{comL} for each buck converters will be different according to the original output voltage at no load condition and the DC voltage level at transition currents. Thus it is arduous to design the fixed particular current I_{comL} by sensing the initial condition for each buck converter. There must be another way to compensate the DC voltage difference for each buck converters additional to the current in equation (19) for parallel buck converters system.

Let us simplify the question by taking 2 buck converters to be example in Fig. 21.

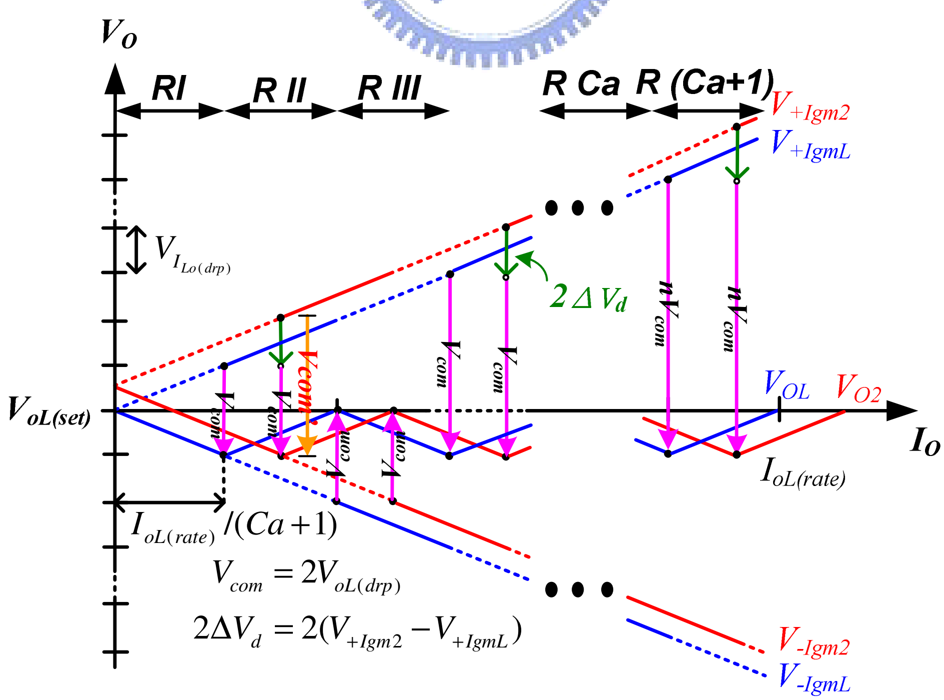


Fig. 21. The analysis for two parallel connected buck converters system

Fig. 21.show the analysis for two buck converters system: Buck 2 and Buck L, where Buck L is the buck converter with lowest original voltage output at no load current condition and Buck 2 is one of the buck converters other than Buck L.

There are many reasons for making the transition current decided by Buck L. Because of the original output voltage of it is lowest at no load condition in each buck converter, the $\Delta V_{o(drp)}$ of it is the smallest one resulting in the R_s value which provide the original slope can not be too large. In other words, it is the worst case from all parallel buck converters. Due to the $V_{oL(set)}$ is the smallest output voltage, the output current of Buck L will be the lowest and since the output current of each buck converter is sampling from the transconductor to I_{ogm}, it is possible to find the lowest one. By setting the $I_{oL(rate)}$ of Buck L to be the condition for transition current, the $I_{oL(rate)}/(C_a+1)$ will be the range between each transition current and the $2V_{oL(set)}$ will be the compensation voltage $V_{com.}$

For the Buck 2, because of the total DC difference voltage will change according to the initial voltage of the buck converter. From the analysis in Fig. 21, in order to generate the continued triangle output voltage waveform, we can find the compensation voltage drop when using V_{+Igm2} to provide positive slope can easily be obtain by adding 2 times of voltage difference between V_{+Igm2} and V_{+IgmL} additional to V_{com}. Thus, an additional voltage drop $2\Delta V_d$ is generated by sourcing a current proportional to the current difference I_d through the R_1, where:

$$I_d = I_{ogm2} - I_{ogmL} \tag{21}$$

$$2\Delta V_d = 2(V_{+Igm2} - V_{+IgmL}) = 2(I_{+gm2} - I_{+gmL})R_1 = 2kI_dR_1 \tag{22}$$

The compensation voltage drop $2\Delta V_d$ only need to be added when transit into even region with positive slope to Buck 2. The stability may be challenged in parallel buck converters system by letting the buck converter with larger output current compensate more voltage than lower output current one in positive slope region, but the solution is obviously. The compensation voltage $2\Delta V_d$ drop also providing the negative feedback loop for stability during positive slope region, if some perturbation occur to increase the current difference between Buck 2 and Buck L, the ΔV_d for will increase providing additional voltage drop at Buck 2, reducing the output voltage difference between Buck 2 and Buck L, force the current difference back to the setting of IDDS.

According to the principle discuss above, the operation when M number of parallel connected buck system can be obtain. Sampling the current output from the transconductor and choose the buck converter with lowest I_{ogm} current to be the Buck L first. Setting the $I_{oL(rate)}$ to decide the transition current and calculate the current difference between I_{ogmN} to I_{ogmL} is the second part. Finally, an index of the I_{PNCM} for Buck M except than Buck L can be drive as follow:

$$I_{PNCM} = -1^{N-1} I_{gmM} + I_{comM} \quad \text{for region N} \tag{23}$$

$$\begin{cases} I_{comM} = 0 & \text{for region 1} \\ I_{comM} = \sigma \bullet \left[\dfrac{N}{2}\right] \bullet \dfrac{2\Delta V_{oL(drp)}}{R_1} + k(\sigma+1) I_d, \text{where } \sigma = \text{-}1^N & \text{for region N} \end{cases} \tag{24}$$

The mathematic formula of I_{PNCM} and I_{PNCL} may be complex, but the circuit for PNC method is quite simple making it is easy to implement.

The analysis above proving the PNC method with lesser output voltage variation by output the continued triangle voltage waveform, and the stability in positive slope region can be maintained from the current difference element I_d in total output current I_{PNC} of IDDS circuit. The PNC method using by IDDS is really better than the original compensation circuit in DDS.

3.3 The loss analysis on a modeled buck converter

From the discussion in Chapter 1.2.3, a power management system is needed to improving the light load efficiency of parallel buck converters due to the switching loss. To design the whole power management method, we need to analysis the loss when a buck converter is supplying the energy.

Start from modeling the buck converter in Fig. 22 first. Because of the output current for the buck converter is several ampere in our case, the power MOSFET is always external the buck converter due to the huge size. An external high current specification power MOSFET result in huge input capacitor and make the high side MOSFET using NMOS rather than PMOS because of the current driving density of NMOS is better than PMOS [14].

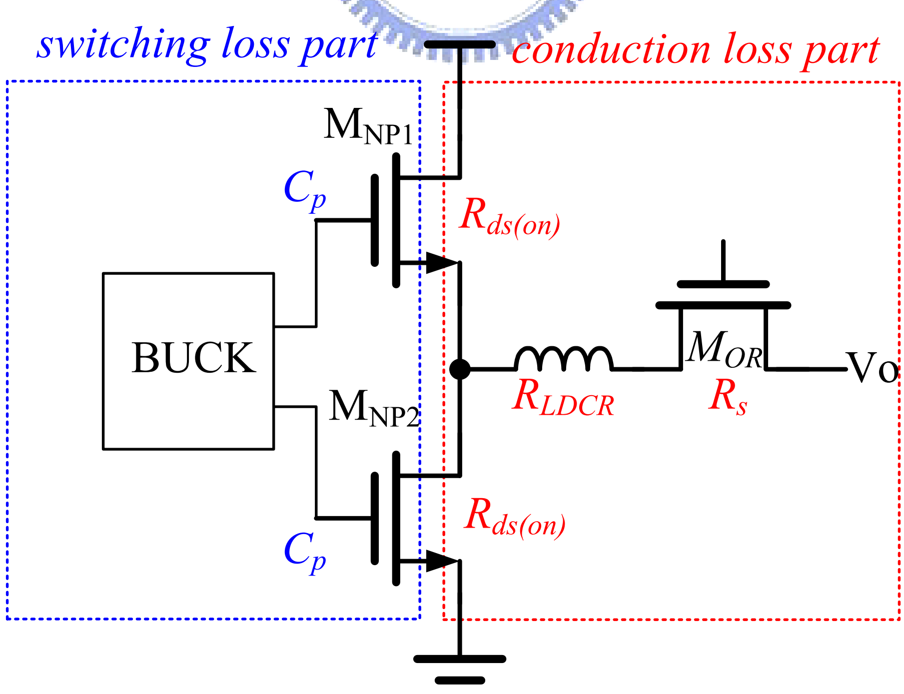


Fig. 22. The analysis for two parallel connected buck converters system

Let the discussion focused on the external conduction loss and switching loss and for the value of the output current I_{out} is several ampere, thereby ignoring the internal loss of each buck converter. Since the conduction loss occurs on the current path mainly [15] and the switching loss occurs on the power MOSFET [16], the model of buck converter in Fig. 22 can be separated into conduction loss part and switching loss part. The resistance on current path is shown in figure, V_{DIN} is the supply voltage and the on-resistance of ORing MOS using to provide the slope in IDDS is R_s, the R_{LDCR} is the DC equivalent resistance of inductor and the on-resistance of power MOSFET is $R_{ds(on)}$. For the output current I_{out}, the loss on the power MOSFET is $DI_{out}^2R_{ds(on)}$ and $(1\text{-}D)I_{out}^2R_{ds(on)}$ due to the switching operation of buck converter [17]. The power loss on conduction loss part is shown in Fig. 23.

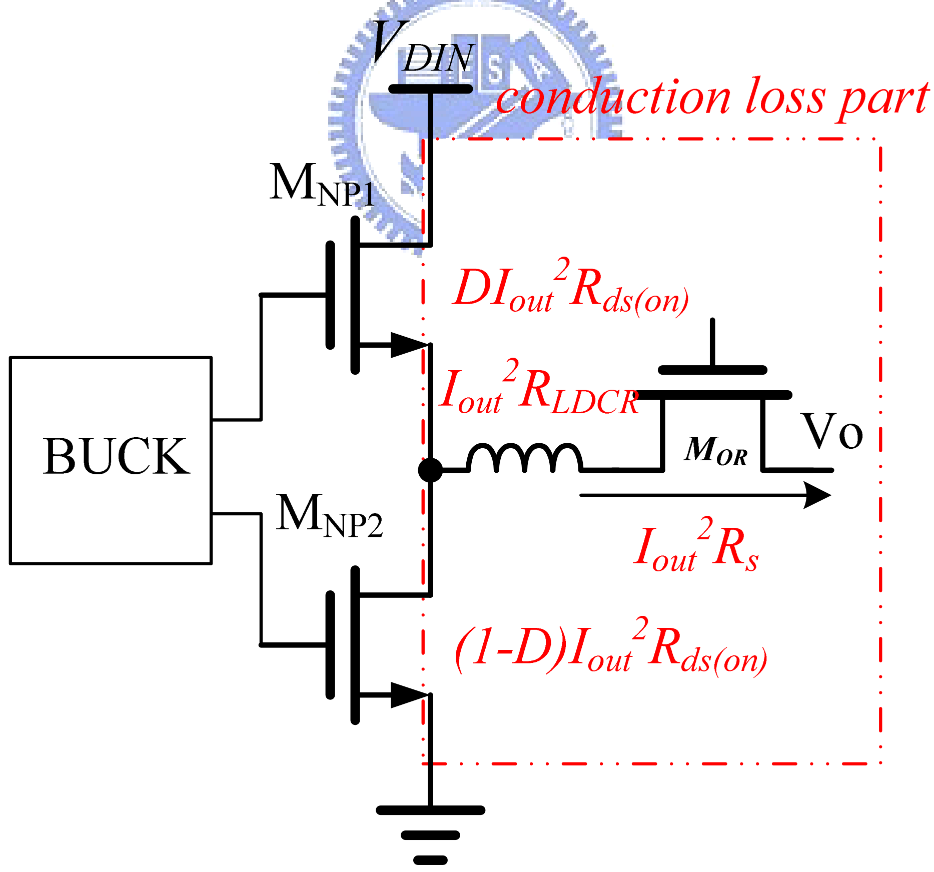


Fig. 23. The analysis for two parallel connected buck converters system

After summing the power loss on each device, the total conduction loss P_{CN} can be calculated as follow:

$$P_{PN} = I_{out}{}^2 (R_{ds(on)} + R_{LDCR} + R_s) \tag{25}$$

For the switching loss part, the switching frequency of buck converter and the input capacitor C_p of power MOSFET is considered. The switching loss can be discuss from the power MOSFET transition switching loss and the gate driving loss of power MOSFET which is shown in Fig. 24.

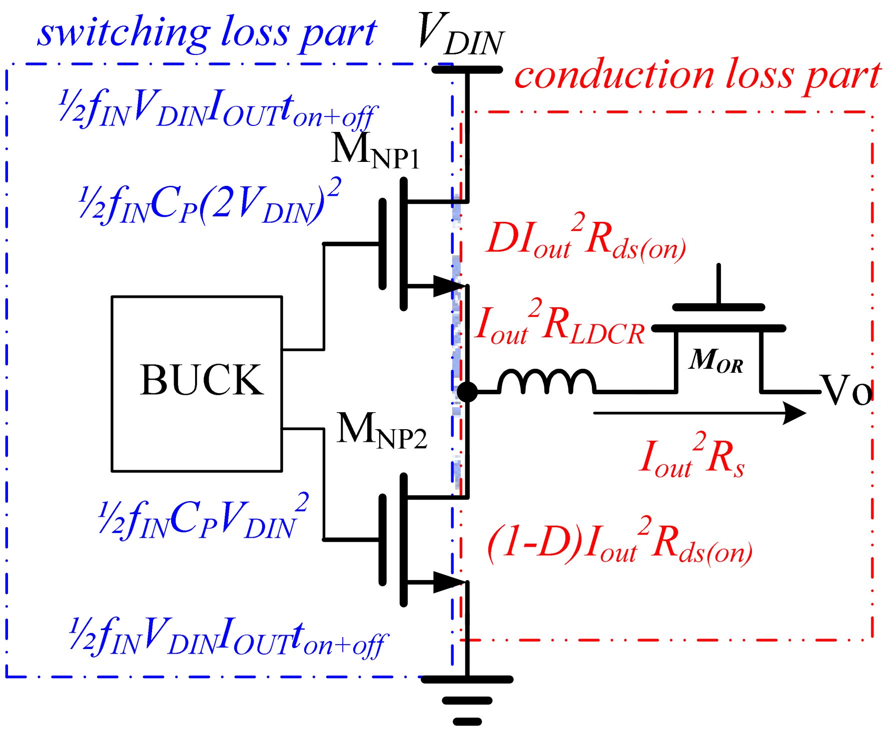


Fig. 24. The analysis for two parallel connected buck converters system

The power MOSFET transition switching loss is $0.5*(f_{IN}V_{DIN}I_{out}t_{on+off})$, where t_{on+off} is the summation time of the power MOSFET from off-to-on and on-to-off [18], it is proportion to current driving ability of the buffer stage internal the buck converter and the value of C_p. The gate driving loss can be calculated by the equation (26):

$$P = fCV^2 \tag{26}$$

Due to the NMOS type high side power MOSFET, the bootstrap technique is needed for the source terminal of it being V_o but ground to get a good "1" when turn on it [19]. The bootstrap technique pump up the gate voltage to about $2V_{DIN}$ when turn on the high side power MOSFET, thus the gate driving loss on it is $0.5*f_{IN}C_p(2V_{DIN})^2$.

The total switching loss PSW can be calculation as follow:

$$P_{SW} = f_{IN}V_{DIN}I_{out}t_{on+off} + \frac{5}{2}f_{IN}C_pV_{DIN}^2 \tag{27}$$

Due to the high output current specification and the huge input resistance of the external power MOSFER, the other loss can be ignored for the domination of these two types of power loss. The total power loss P_{t1} can be simply to equation (28):

$$P_{t1} = P_{SW1} + P_{PN1} = I_{out}{}^2(R_{ds(on)} + R_{LDCR} + R_s) + f_{IN}V_{DIN}I_{out}t_{on+off} + \frac{5}{2}f_{IN}C_pV_{DIN}^2 \tag{28}$$

3.4 The theory about switching loss calculation (SLC) circuit

The discussion on previous section shows the power loss on an operated buck converter. Within the help of these equations, the power management control method can be obtained by analyzing the power loss relationship between single and parallel connected buck converters. For the output current I_{out}, let us define using single buck converter to supply the energy to be the "single module" and using parallel connected buck converters to be the "parallel modules". Fig. 25 shows the analysis of power loss on the N parallel modules. The only difference compare to the single modules is the output current for each buck converter is divided into 1/N times of I_{out}, thus the total power loss P_{tN} is:

$$P_{tN}=\frac{I_{out}{}^{2}(R_{ds(on)}+R_{LDCR}+R_{s})}{N}+f_{IN}V_{DIN}I_{out}t_{on+off}+\frac{5N}{2}f_{IN}C_{p}V_{DIN}^{2} \tag{29}$$

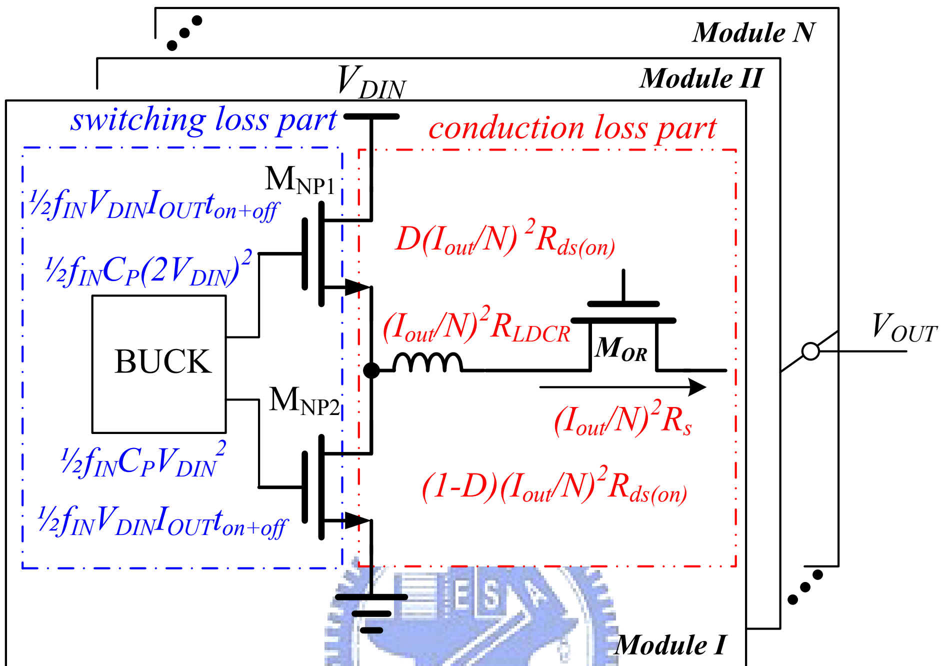


Fig. 25. The analysis for two parallel connected buck converters system

Comparing with the power loss in the single module, the value of P_{SWN}, which is the total switching loss of the N power modules, is n times that of gate driving loss part in P_{SW1} for a single power module. But the value of P_{CN1} in a single power module is n times that of P_{CNN}, which is the total conduction loss of the N power modules. Since the switching loss depends on the switching frequency f_{IN} not on I_{OUT}. Thus, an incremental power module may increases more switching loss but decreases the conduction. The suitable addition of a power module can be derived by (30).

$$\Delta P_{SW}=\Delta P_{CN}\Rightarrow\frac{5(N-1)f_{IN}C_{p}V_{DIN}{}^{2}}{2}=\frac{N-1}{N}I_{outp}{}^{2}\left[R_{ds(on)}+R_{s}+R_{LDCR}\right] \tag{30}$$

It means if the parallel current output is *Ioutp*, the total power loss P_{t1} for supplying from single modules keep the same with the P_{tN} in N parallel modules. In other words, if the output current $I_{out} < I_{outp}$, the P_{t1} will be lesser than P_{tN} and using the single module to supply the output will be more efficiency. For the situation that $I_{out} > I_{outp}$, using the N parallel modules will be more efficiency. There is another improvement in single module. Because that the current sharing issue is not considered in single module, therefore the R_s can be scaled down to reduce the conduction loss of ORing MOSFET which is impossible for keeping the current sharing performance in parallel modules. Assuming that the paralleling system uses N paralleling ORing MOSFETs, the on-resistance of the ORing MOSFETs in single module will become R_s/n and equations (31)-(32) can be derived.

$$\frac{5 f_{IN} C_p V_{DIN}{}^2}{2} > \frac{1}{N} I_{outp}{}^2 [R_{ds(on)} + R_{LDCR}] \tag{31}$$

$$I_{outp} = \sqrt{\frac{5NC_P}{R_{ds(on)} + R_{LDCR}}} \bullet \sqrt{f_{IN}} \bullet V_{DIN} = K_C \sqrt{f_{IN}} \bullet V_{DIN} \tag{32}$$

The current I_{outp} will be the transition current between single module and paralleling modules. Because of the capacitance C_p, $R_{ds(ON)}$ and R_{LDCR} only depend on the output current specification. Thus, in (32) a constant K_c is used to simplify the equation. Thus, I_{outp} is proportional to the root of the f_{IN} and V_{DIN}, which are the parameters of the buck converters. It means that the transition current I_{outp} must take some important parameters of buck converters condition into consideration and these parameters are also the major element for calculating the gate driving loss in switching loss part. Thus, a circuit with the ability to calculate the equation (32) named as switching loss calculation (SLC) circuit is proposed in this paper to be the core of the power management method for parallel connected power system.

Chapter 4

Circuit Implementations and simulation result

In this chapter, we will give a design procedure of our improved DDS with PNC method and the power management method with SLC circuit. At first, Chapter 4.1 shows the whole circuit block diagram and describes the operation method for all function block. In Chapter 4.2, the transconductor part will be introduced, it contains the FFVF transconductor, the bias current generator and the sample and hold circuit. The PNC part will be shown in Chapter 4.3, the current comparator and the winner take all circuit used in it will be introduced too. The SLC circuit and the logic control part will be presented in Chapter 4.4. Finally, the whole circuit simulation is shown in Chapter 4.5. The design environment is TSMC .35 2P4M.

4.1 The whole circuit block diagram

The system can be divided into three major blocks, the transconductor part, the PNC method part and the SLC circuit. The whole circuit block diagram for using IDDS with SLC circuit at the buck converter is shown in Fig. 26, the output current information will be gathered first in the transconductor part first. A voltage drop *Vc* will be generated when the output current I_{out} flow through the ORing MOSFET and the function of the GM part transmutes V_c to a current I_{gm}hich is proportion to I_{out}. The PNC part will output a current I_{PNC} to do the current sharing and voltage compensation work. The current I_{PNC} is generated by mixing the transcundoctor current I_{gm} and the compensation current I_{com}, and output it to the feedback pin of the buck converter. The SLC circuit will provide the power management control to the buck converter. It gathers the operation frequency and the supply voltage information of the buck converter to control the enable signal of buck converter and ORing MOSFET according to the transconductor current I_{gm}. In this secession, the block diagram for all three function parts will be presented.

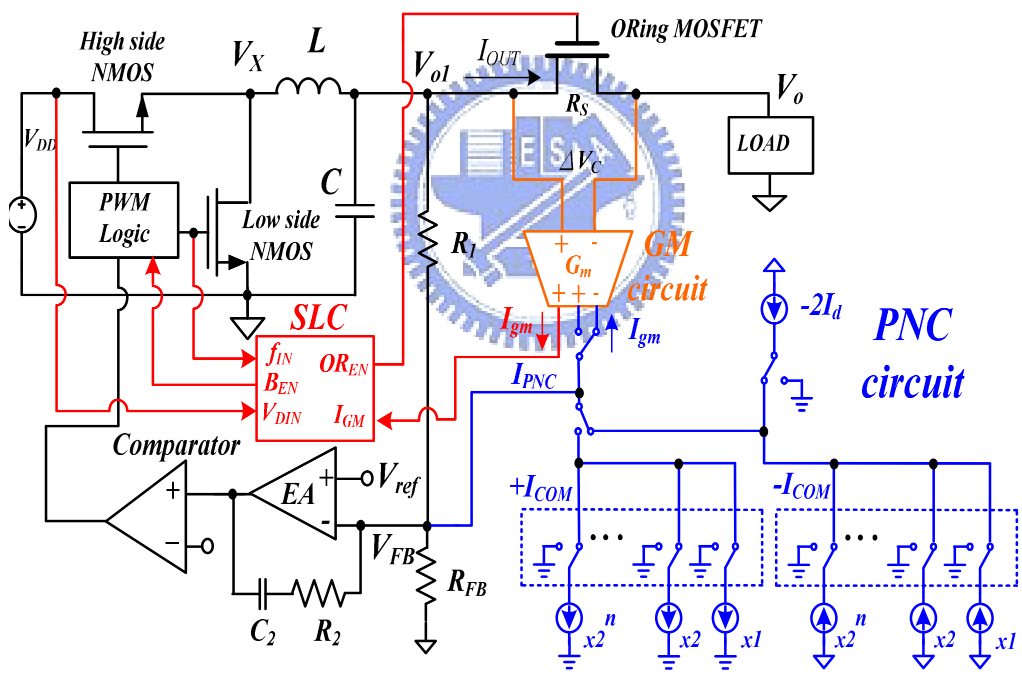


Fig. 26. The Whole circuit block diagram.

4.2 The circuit implementation of the transconductor

Fig. 27 shows the block diagram of the transconductor part of the IDDS circuit.

The bias circuit supply the bias current to all the function block, the FFVF transconductor transmute the V_c signal into a current I_{ogm} which can be the output current information of the buck converter, and the sample & hold circuit is using to removed the effect form the noise and the phase difference between each buck converter making sure the current sharing performance not being effect by them.

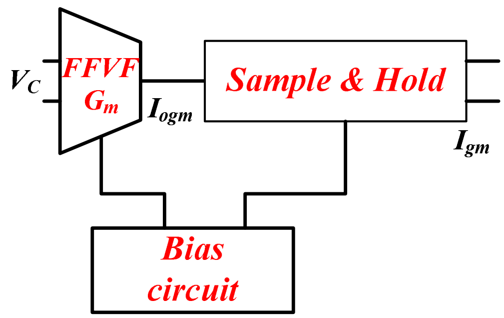


Fig. 27.the block diagram of the transconductor part.

4.2.1 The bias current generation circuit

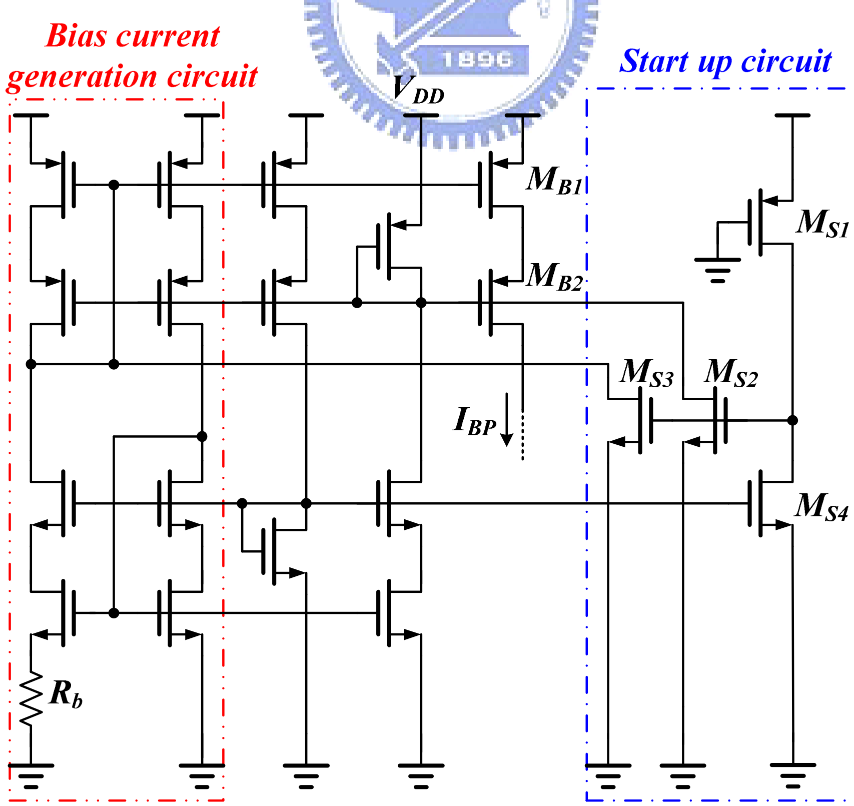


Fig. 28. The bias current generation circuit.

The bias current generation circuit is shown in Fig. 28 [20] [21], after the supply source V_{DD} rising up, the MOSFET M_{S1} turn on pulling up the gate voltage of MOSFET M_{S2} and M_{S3}. It creates an initial current through the bias current generation part and establishes the biasing point according to the R_b and the process parameters of MOSFET. The MOSFET M_{B1} and M_{B2} mirror out the biasing current to the other circuit. In Fig. 29, the simulation result of the bias current generation circuit show the output biasing current I_{BP} in different temperature conditions, the current has positive coefficient to temperature. This biasing current will be the current supply of almost all circuit in IDDS circuit.

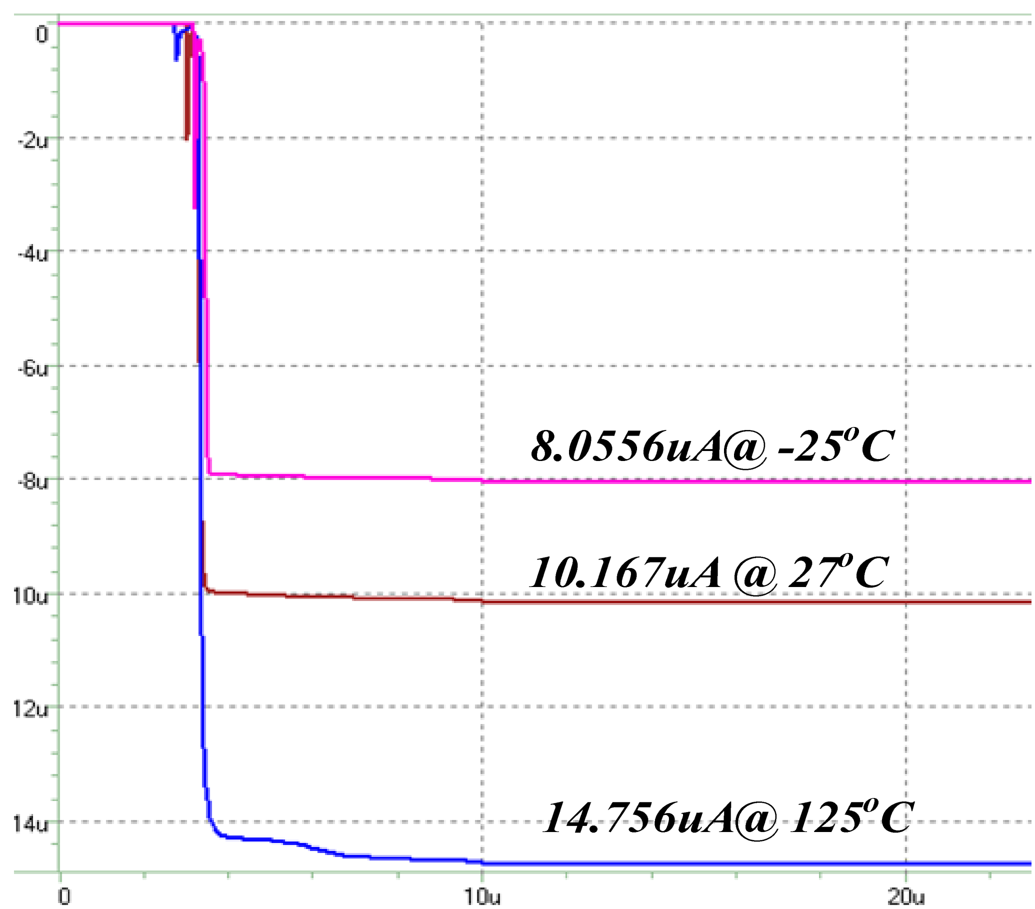


Fig. 29. The simulation result of the bias current generation circuit

4.2.2 The FFVF transconductor

Fig. 30 shows the transconductor using the fold flipped voltage follower (FFVF) [22] technique. The FFVF circuit uses a 2:1 bias current and the folded connected MOSFET M_{N2} and M_{N1} to increase the input voltage swing range extending the operation region and reduce the input resistance of the voltage follower to increase the accuracy and linearity of the transconductor. The input resistance of the FFVF circuit and the input swing range is:

$$V_{in}^{swing} = V_{DD} - V_{DSMBP1} - V_{GS\,MN1} \tag{33}$$

$$R_{IN} \approx \frac{1}{gm_{p1}} \frac{1}{gm_{n1} r_{op1}} \tag{34}$$

Where the V_{DSMBP1} is the drain-source voltage of the MOSFET M_{BP1}, the V_{GSMN1} is the gate-source voltage of the M_{N1}, the gm_{p1} and gm_{n1} is the transconductance of M_{P1} and M_{N1}, the ro_{p1} is the early resistance of the M_{P1}.

The operation principle can be described as follow. At first the gate of the MOSFET M_{P1} and M_{P2} is connected to the both terminal of ORing MOSFET, thus the load depend voltage ΔV_c which is generated by the load current of the buck converters flowing through the on-resistance R_s of the ORing MOSFET is sampled into the FFVF circuit. The output of the FFVF circuit is connected to the MOSFET M_{R1} and M_{R2} to be the voltage control resistance where the control voltage V_{c1} and V_{c2} can be trim to adjust value of the resistance. Finally, the difference voltage ΔV_c linearly transmute into a current signal and mirror through M_{P3}, M_{P4} to become the output current I_{out}.

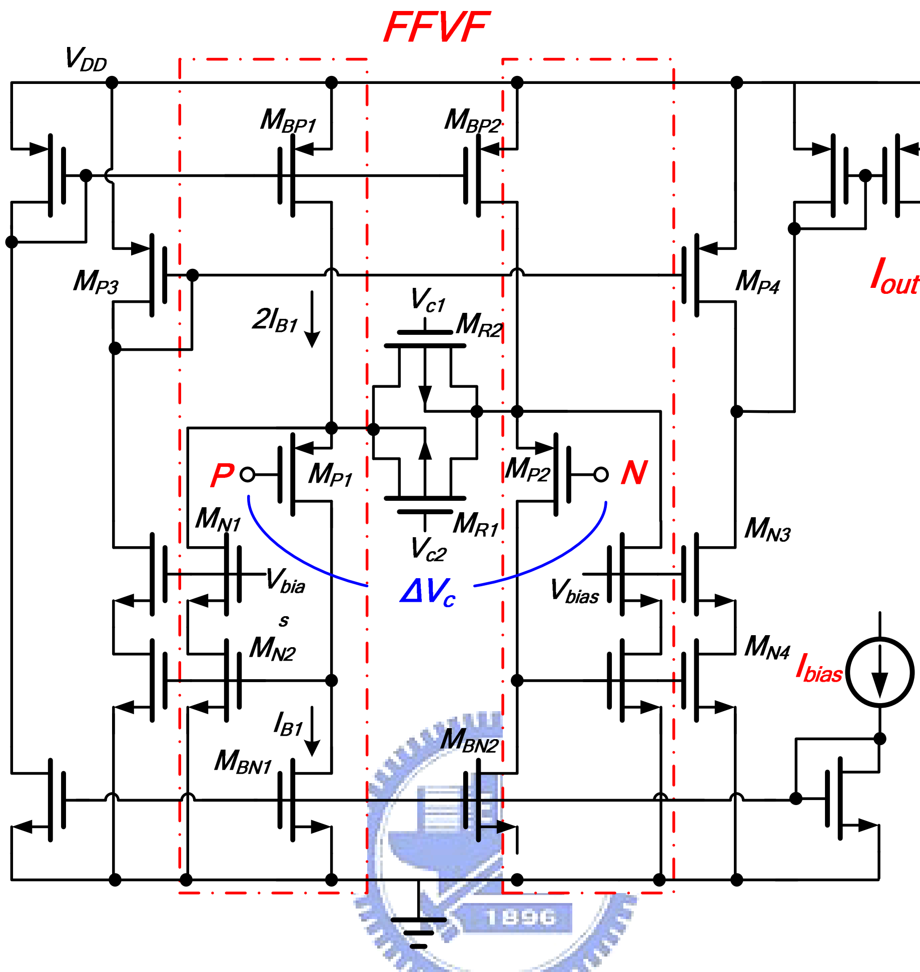


Fig. 30. The FFVF transconductor.

Fig. 31 is the simulation result of the FFVF transconductor, it shows the relationship of the load current I_{LOAD} of the buck converter and the output current I_{OUT} of the FFVF transconductor. The sensing current is set from 0A to 20A and the R_s is set to 5mΩ making the ΔV_c raise from 0V to 100mV, the on resistance of the MOSFET M_{R1} an M_{R2} is set to 2.5kΩ and resulting that the output current range of the transconductor is on 0uA to 80uA. The result shows the maximum error percentage is 1.5% and the FFVF circuit can really provide a high linearity and accuracy transconductor.

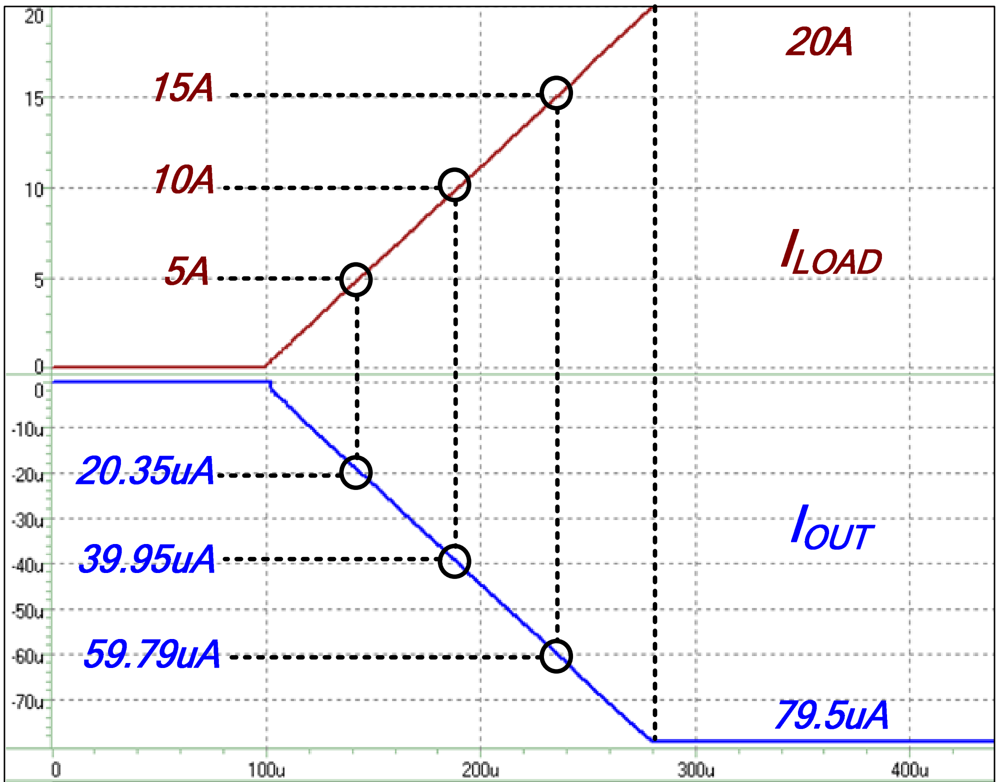


Fig. 31. The simulation result of the FFVF transconductor.

4.3 The circuit implementation of PNC circuit

As depicted in Fig. 28, the block diagram of the PNC circuit contains a winner take all (WTA) circuit [23], a current comparator array, a difference current I_d generator, the encoder, and the I_{PNC} generator. Start from the current input I_{gm1} to I_{gmm}, the winner take all circuit will choose the smallest one to be the I_{gmL} and it will input the current comparator array to confirm the output current information and the output of current comparator array will be send into the encoder to define the operation region. At the same time, the I_d generator output the difference current I_{dk} between I_{gmk} and I_{gmL} by cascading the PMOS type current mirror and NMOS type one to substrate the current. And the compensation current I_{com} corresponding to the worst case can be generated by a simple bias current generator. Finally, the I_{PNC} generator using the current input I_{gmk}, I_{com} and I_{dk} to output the droop enhancement current I_{PNC} by the operation region information given by the encoder.

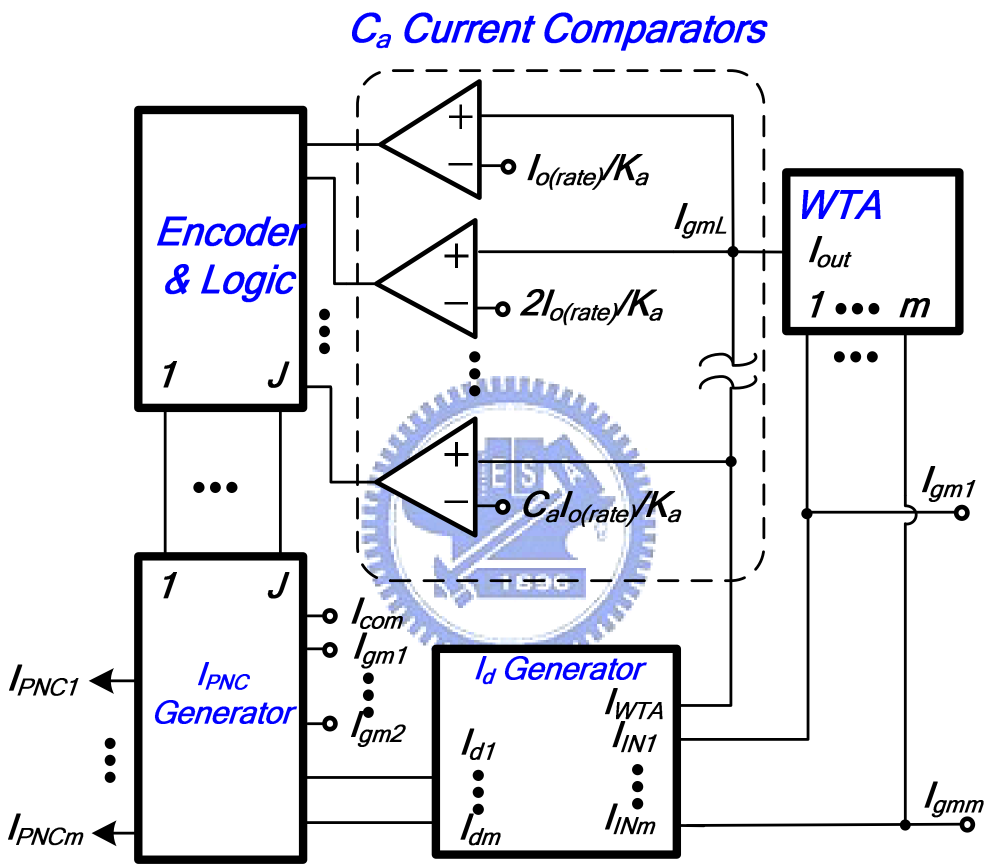


Fig. 32. The PNC circuit block diagram

4.3.1 The winner take all circuit

Fig. 33 shows the circuit implementation of the winner take all circuit, the design is base on the minimum voltage selector [24]. The operation starts from input the current (I_1, I_2, …. I_n) input to the drain of diode connected MOSFET M_{D1} to M_{Dn} and transmute the current input into the gate voltage signal V_{G1} to V_{Gn}. Suppose that the I_1 is the smallest current, the V_{G1} will be the lowest voltage too. The drain voltage V_D will be effected by the gate-source voltage V_{gsA1} of the MOSFET M_{A1} because of the bias current I_B. Thus for the same biasing current of the MOSFET M_{A1} to M_{An}, the drain voltage V_D will be decided by the lowest voltage V_{G1} dominantly.

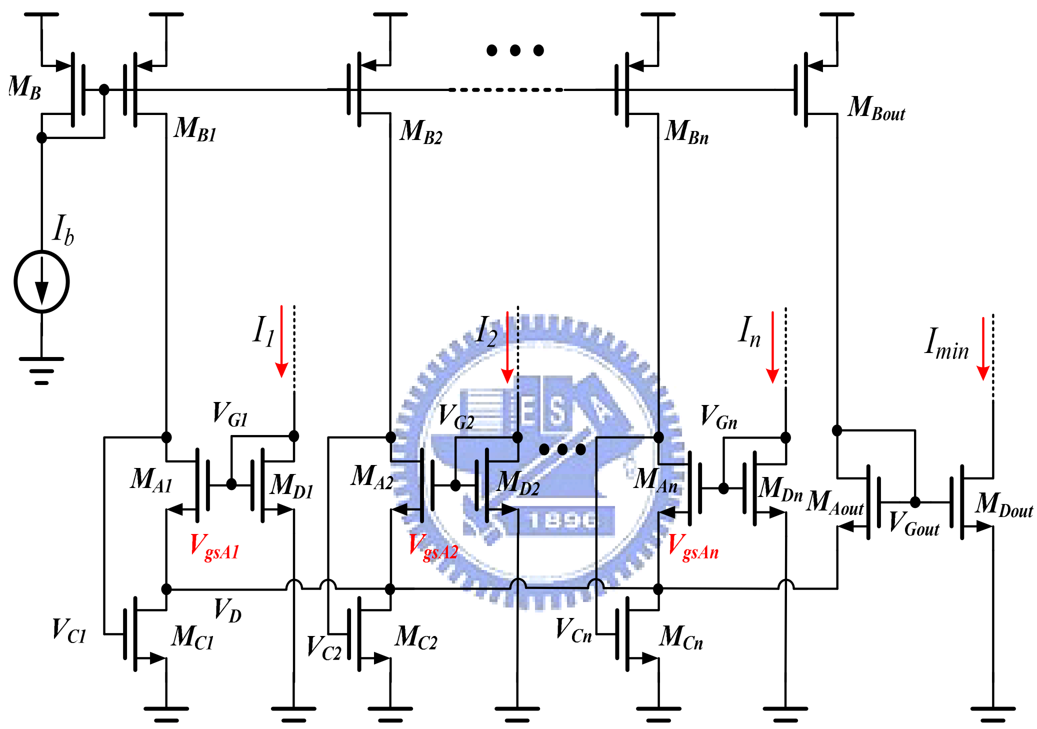


Fig. 33. The winner take all circuit

Because of the VgsAk > VgsA1 where k=2,3….n, the drain voltage V_{C2} to V_{Cn} of the MOSFET M_{A2} to M_{An} will be greatly decreased to keep the same biasing current I_B flowing through and turn off the MOSFET M_{C2} to M_{Cn}. Thus the gate voltage V_{Gout} of the MOSFET M_{Aout} equal to the V_{G1}, the MOSFET M_{Dout} acts like the output part of a current mirror and make the output current $I_{min}=I_1$. The mathematic form can be derived as follow:

$$V_{Gout} = \min(V_{G1}, V_{G2}, ...V_{Gn}) \tag{35}$$

$$I_{\min} = \min(I_{1,} I_2, ...I_n) \tag{36}$$

An issue need to be concern about for that the biasing current of MOSFET M_{A2} to M_{An} flow into the M_{C1} after the M_{C2} to M_{Cn} has been turning off. The length of the MOSFET MC1 to MCn will be designed large enough to ignore the channel length modulation effect for increasing the accuracy of the current I_{min}.

Fig 34 shows the simulation result of the WTA circuit, the input are two ramping current I_1 an I_2, the output current I_{WTA} can always follow the lowest current for a maximum error percentage of 2.21% in the conditional that lowest current is 100uA. The minimum current output of WTA circuit is 4.92uA, the input current can be well designed to avoid this region and make sure the WTA circuit operation in the current range with higher accuracy.

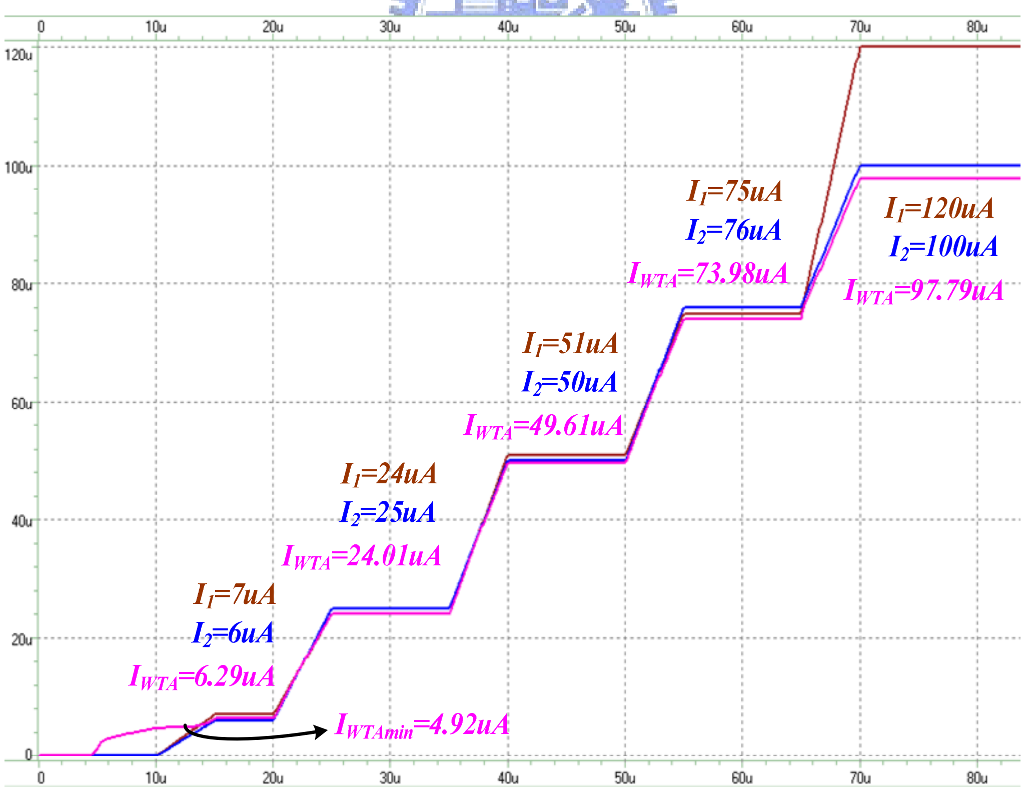


Fig. 34. The simulation result for WTA circuit

4.3.2 The current comparator circuit

The circuit of the current comparator has been shown in Fig. 35, the whole circuit can be divided into the input pair part, hysteresis control part, the comparator part and the inverter chain. The operation starts from the input current I_{IN} and the reference current I_{REF} being substrate by the cascading PMOS and NMOS type current mirror and output to the node N_1. The hysteresis control part provides the hysteresis window by using a constant current I_H and the switch PMOSFET M_{SW2}, M_{SW3} and the NMOSFET M_{SW1}, M_{SW4} which are controlled by the output voltage V_{OUTB} of the current comparator.

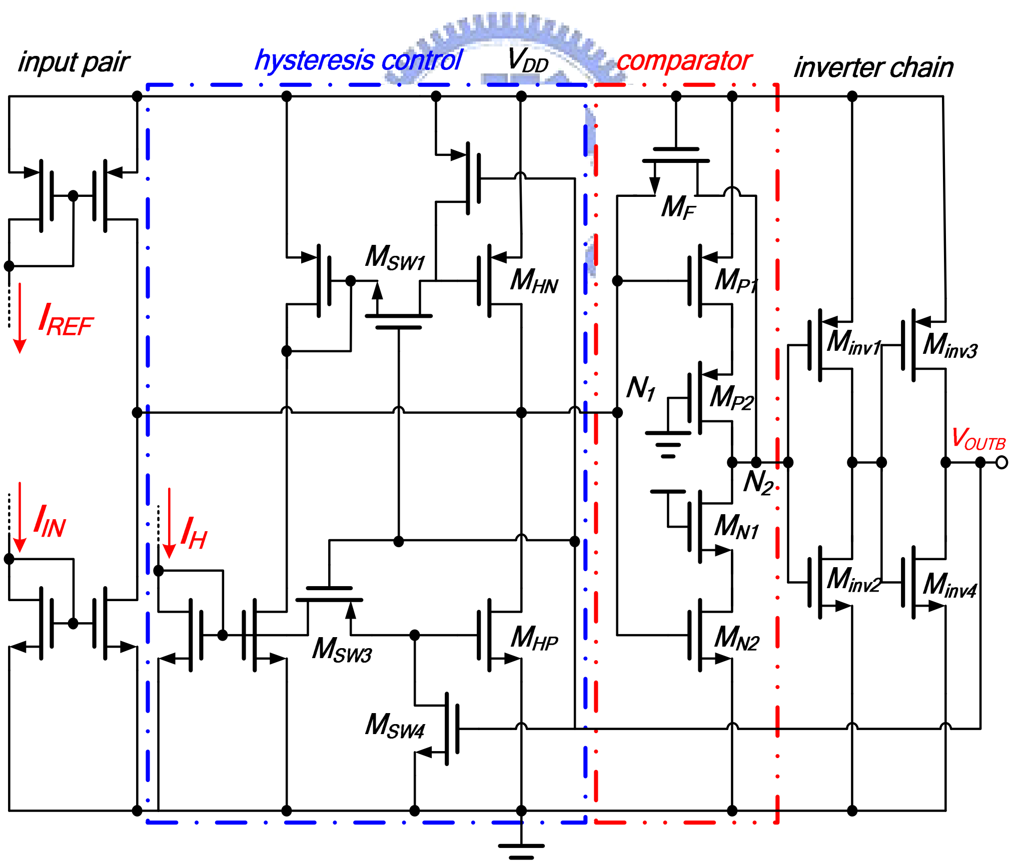
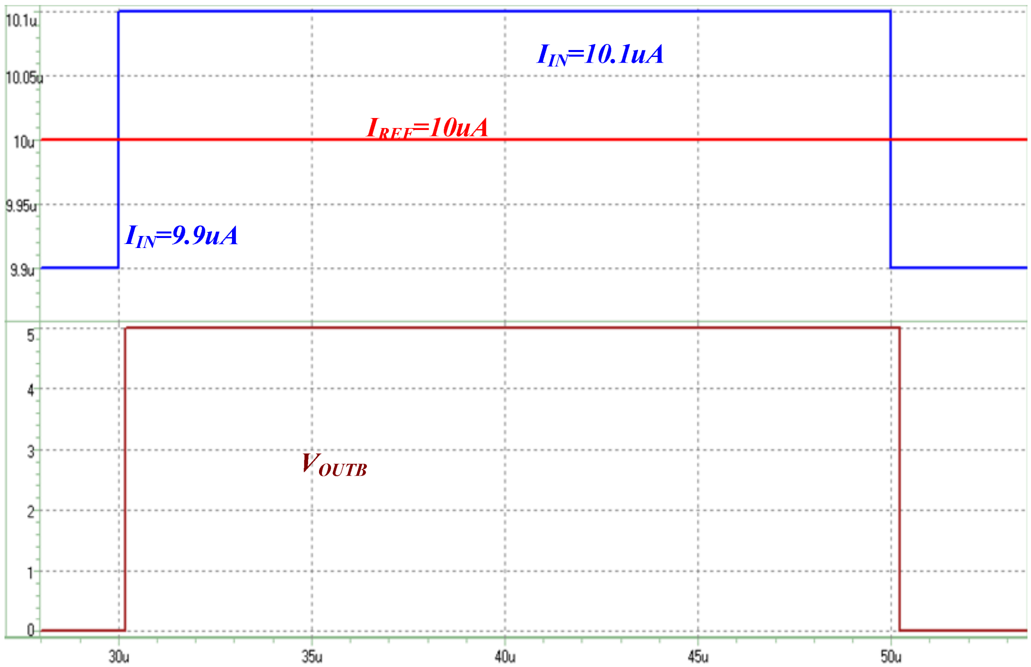


Fig. 35. The current comparator circuit

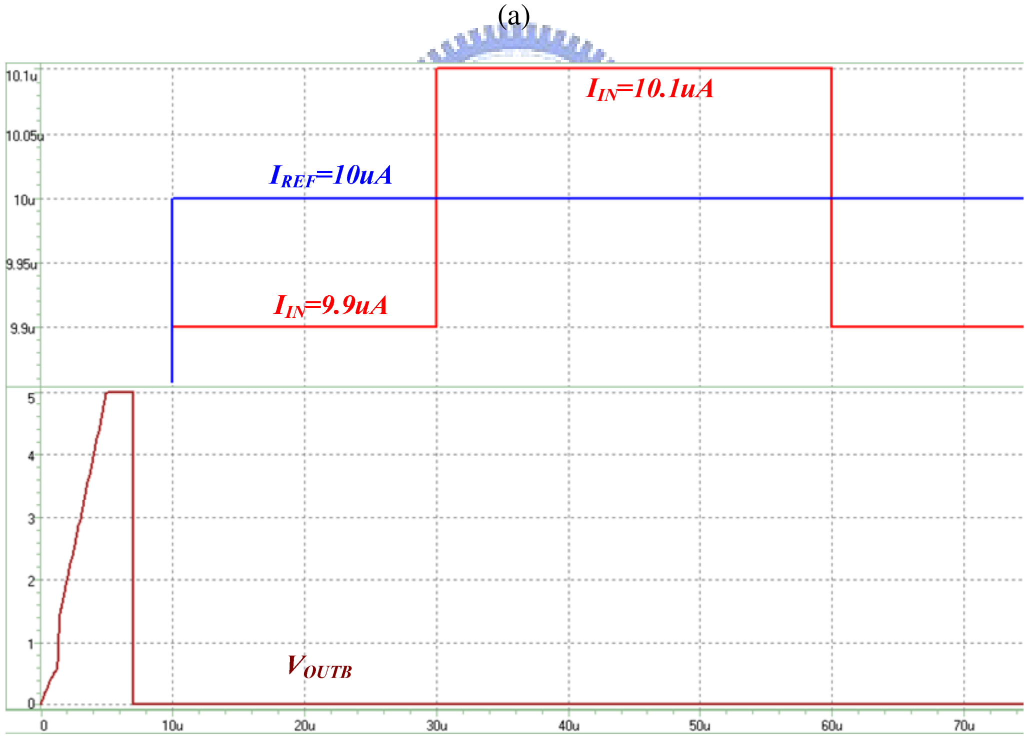
If the V_{OUTB} is low, MOSFET M_{SW3}, M_{SW2} turn on and the M_{SW1}, M_{SW4} turn off, the M_{HP} mirror out the current I_H and provide the positive hysteresis. On the other hand if the V_{OUTB} is high, the M_{HN} mirror out the current I_H and provide the negative hysteresis. The hysteresis window can be adjusted by controlling the magnitude of the MOSFET M_{HN} and M_{HP}.

The comparator part uses the MOSFET M_F to provide a negative feedback loop to reduce the input resistance of node N_1 and N_2 [25]. The small input resistance results in the small voltage swing on the node N_1 increasing the resolution of the comparator and the reducing the transition time of the comparator. The small output resistance shirks the output voltage swing of the comparator and also reduces the transition time. But because of the small input voltage swing the voltage of node N_1 will nearly equal to $V_{DD}/2$ and keep the MOSFET M_{P1} and M_{N2} operating in saturation region, the MOSFET M_{P2} and M_{N1} which is operating in the triode region is added to clamp the quiescent current of the comparator part. For the small voltage swing on the node N_2, the inverter chain composed by the MOSFET Minv1, M_{inv2}, M_{inv3} and M_{inv4} are added to provide the gain and make the voltage V_{OUTB} being a perfect high or low signal.

The simulation result for the current comparator without hysteresis window is shown in Fig. 36 (a), suppose that the reference current I_{REF} is 10uA and the input current I_{IN} step up and down between 9.9uA to 10.1uA, the output voltage waveform of the V_{OUTB} can be obtain. For the condition of resolution of the current comparator is 0.1uA, the delay time from low to high is 0.18us and will be 0.22us from high to low. The DC voltage level of the node N_1 not actually equals to the $V_{DD}/2$ but 3mV lower to it resulting in the difference on the delay time. The total quiescent current is 33.48uA. Fig. 36(b) shows the waveform of the output voltage V_{OUTB} after 0.1uA positive and negative hysteresis is added to the current comparator, the current difference doesn't exceed the hysteresis window thus nothing change on the output voltage waveform.



(a)



(b)

Fig. 36. The simulation result for current comparator in (a) without hysteresis current (b) with 0.1uA hysteresis current

4.3.3 The PNC current generation circuit

Fig. 37 shows the circuit implementation of the PNC current generator by taking the current sharing enhancement coefficient C_a=4 as an example. This circuit controls the MOSFET switches from M_{SW1} to M_{SW15} to mix the currents I_d, I_{COM}, and I_{gm}. The I_d generator is depicted in Fig. 38 and I_{COM} is generated by a constant current source. Besides, I_{gm} is generated by the transconductor. The control signals V_{C1} to V_{C4} is generated by the encoder and control logic. The corresponding logic signals for different regions are shown in TABLE I. Thus, the output current I_{PNC} connected to the feedback pin of the buck converters can cause the triangle V-I waveform as shown in Fig.21. It improves the current sharing performance and keep the output voltage above the minimum value.

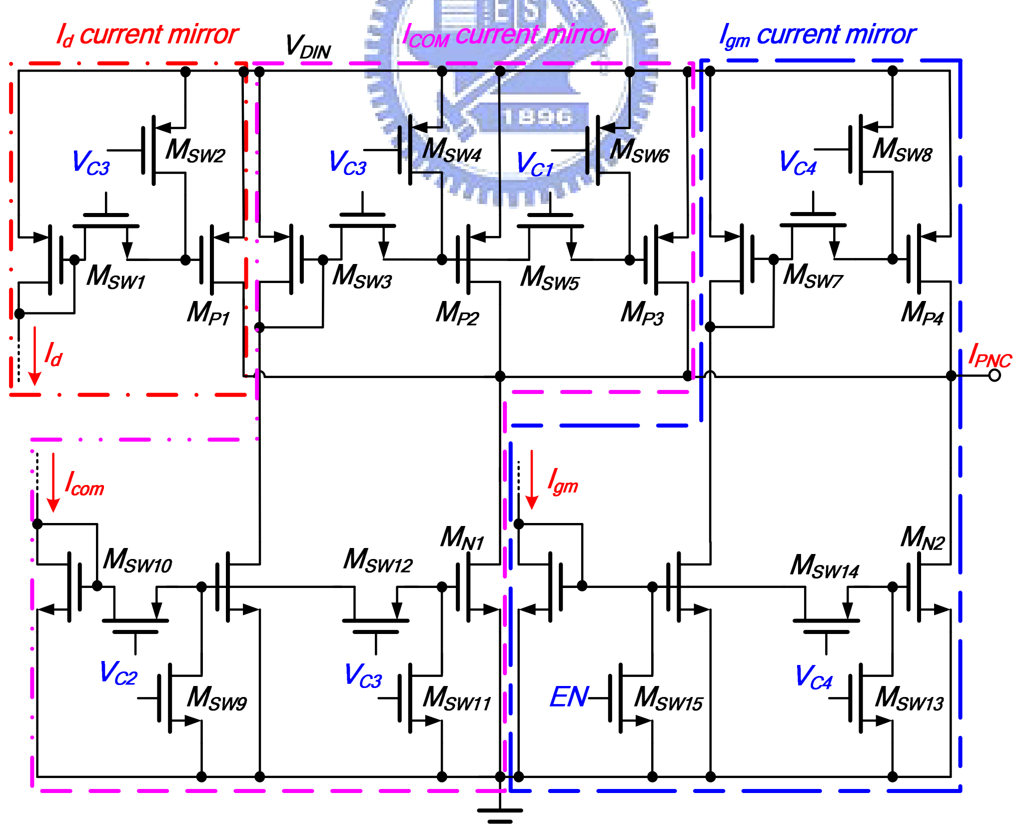


Fig. 37. The implementation of the PNC current generator.

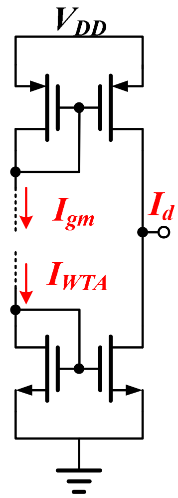


Fig. 38. The I_d current generator.

TABLE I: The Boolean values of the control signals

	V_{C1}	V_{C2}	V_{C3}	V_{C4}
Region I	0	1	0	1
Region II	0	0	1	0
Region III	0	0	0	1
Region IV	1	0	1	0

Because of the original voltage drop ΔV_c produced by the output current flowing through the on-resistance R_S of the ORing MOSFET, the size of the MOSFET M_{P4} and M_{N2} need to be well design to provide the same droop value in positive and negative region. The relationship of the size for these MOSFET can be shown as follow and for the case above, the ratio will be 3:5.

$$(\frac{W}{L})_{MP4} : (\frac{W}{L})_{MN2} = (C_a - 1) : (C_a + 1) \quad (37)$$

Simulation result shows the current transition of the MOSFETs M_{N1}, M_{N2}, M_{P1}, M_{P2}, M_{P3}, and M_{P4}. The current value will be set according to the value of the ratio for the transconductor, the on-resistance R_s for the ORing MOSFET and the feedback resistance for buck converters.

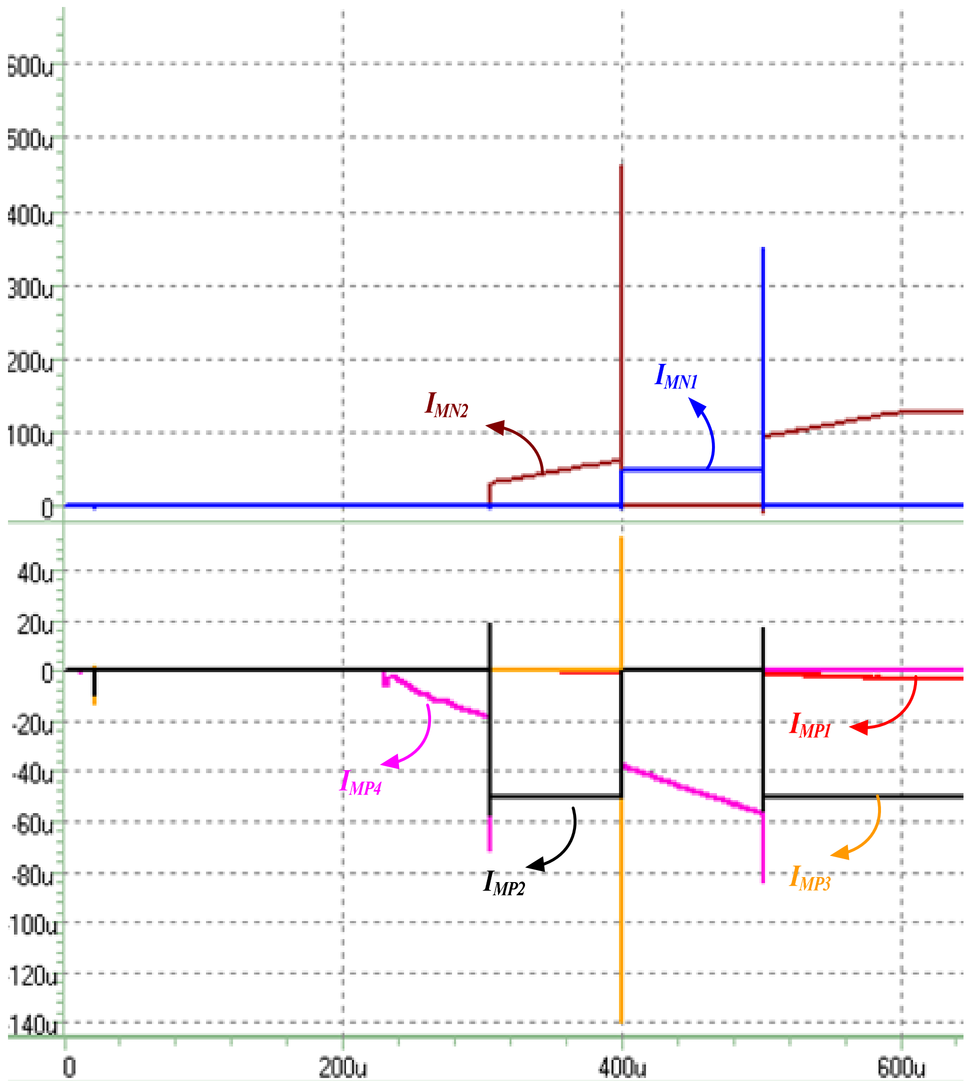


Fig. 39. The I_d current generator

4.4 The circuit implementation of SLC circuit

The block diagram of the SLC circuit is shown in Fig. 40, it contains the frequency divider, the frequency to voltage converter (FIC), the WTA circuit, the current comparators and the control logic.

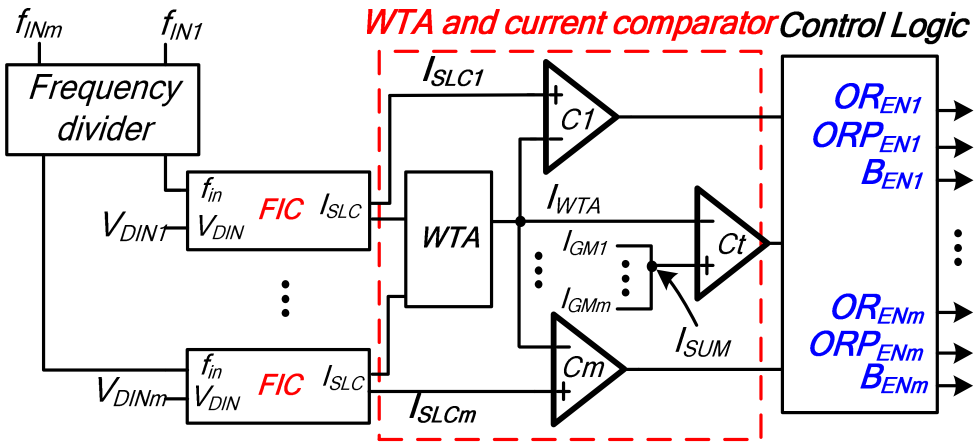


Fig. 40. The SLC part block diagram.

Since the output current of the buck converters is high, the power MOSFET of them will be external for saving chip area. Thus the gate control signals PWM_1 to PWM_m of the parallel buck converters, which are from buck converter 1 to buck converter m, can be used as inputs of operation frequency f_{IN1} to f_{INm} of buck converters. The frequency signal will input to the frequency divider for fixing 50% duty first, the reason will be introduced at section 4.4.2. The supply voltage of the buck converters V_{DIN1} to V_{DINm} is the V_{DIN} of SLC circuit. The output of the SLC circuit corresponds to the currents I_{SLC1} to I_{SLCm}, thereby it will be the current which is proportion to I_{OUTP} for buck converter 1 to buck converter m. The WTA circuit outputs a current I_{WTA}=min(I_{SLC1},… I_{SLCm}), which is proportional to I_{OUTPL}=min(I_{OUTP1},… I_{OUTPm}), the current comparators C1 to Cm compare the I_{WTA} with I_{SLC1} to I_{SLCm}, respectively. Because of the hysteretic in current comparator, the output of comparators shows which the buck converter has the smaller I_{OUTP}. It means this buck converter should keep operation during single module to have less switching loss. On other hand, the other converter with higher I_{OUTP} is turned off. The current comparator Ct compared the current I_{SUM} with I_{WTA} to detect whether I_{OUT} is larger than I_{OUTPL} or not to decide the modules where the paralleling power system operates at.

Control logic circuit needs to control the signal OR_{EN} which connect to the gate of ORing MOSFET, which can decide whether this buck converter needs to supply load current or not. The signal OR_{ENP} connects to the paralleling ORing MOSFET determines the value of $R_{ORds(on)}$ and the signal B_{EN} connecting to the enable pin of buck converter disable the buck converter with higher I_{OUTP} in single-module operation.

4.4.1 The frequency to voltage circuit

The frequency to voltage converter (FVC) [26] circuit is used in frequency-to-current converter (FIC). That is, it transfers the frequency input signal to a voltage signal, which is inversely proportional to it. The operation principle of the circuit is shown in Fig. 41.

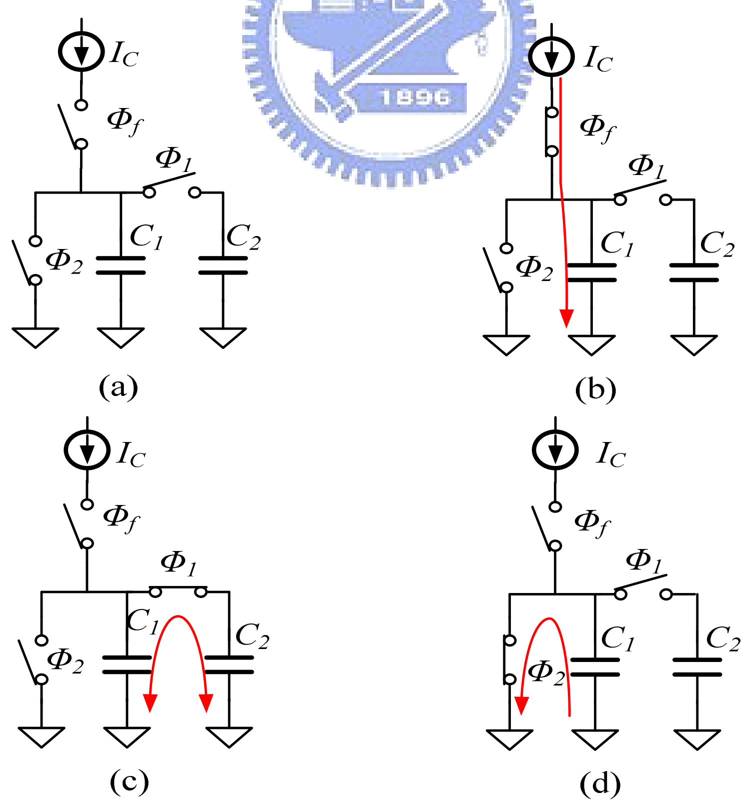


Fig. 41. The operation principle of the FVC circuit.

Fig. 41(a) shows the component used in FVC circuit where I_C is an input current, the f_{IN} is the frequency input and the Φ_1, Φ_2, Φ_f are switches. The operation start from the Fig 41(b) during the off-time of the frequency input signal f_{IN}, the switch Φ_f turn on making the current I_C charge the capacitor C_1, thus the voltage V_1 proportions to the current I_C and the on-time t_{ON} of the frequency input f_{IN}. When the f_{IN} signal raise up, the switch Φ_f turns off and a pulse will be generated to turn on Φ_1, the charge sharing effect occurs between the capacitor C_1 and C_2. Right after the switch Φ_f turning off a pulse signal turn on the Φ_2 clean up the stored charge in C_1. The operation above is shown in Fig 41. (c) and (d). After a few operation cycles, the output voltage V_{FVC} equal to the voltage V_1 and the value can be derived as equation (38) where k is a constant which proportions to the value of the capacitor C_1.

$$V_{FVC} = kt_{off}I_c \tag{38}$$

The circuit of the pulse generator for Φ_1 and Φ_2 is shown in Fig. 42, the delay time of the inverter chain is the on-time of the pulse and will be designed being several nano seconds long, following up the pulse signal Φ_2 will be generated after the Φ_1 falls down. Fig. 43 shows the circuit implementation of the FVC circuit, the MOSFET M_{S1}, M_{S2} act as the switch Φ_1, the M_{N1} acts as Φ_2 and the M_{P1} acts as Φ_f. The MOSFET M_{N2} helps up to clean the charge stored in the node N_1 during the on-time of the f_{IN}.

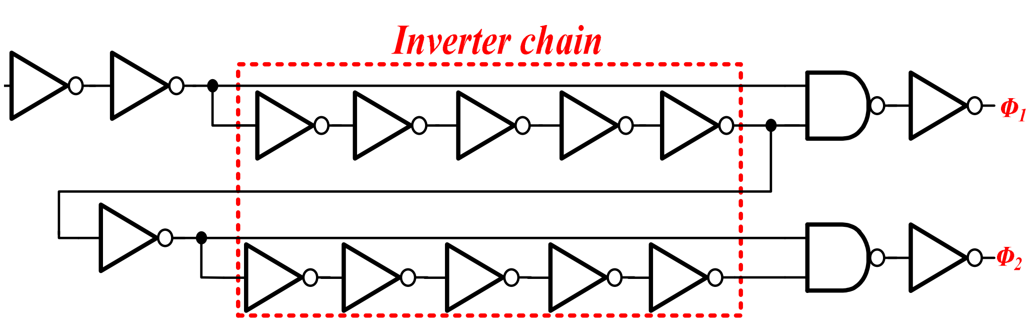


Fig. 42. The pulse generator circuit

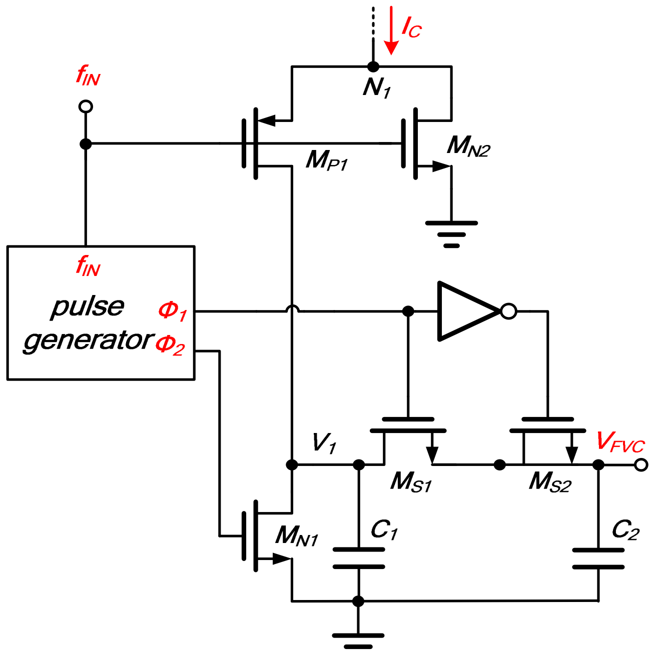


Fig. 43. The circuit implementation of the FVC circuit.

The simulation result of the pulse generator is shown in Fig. 44, the Φ_1 signal starts 0.4 nano seconds after the f_{IN} signal raise up, the on-time of the signal Φ_1 and Φ_2 are 0.8 nano seconds. Fig. 45 shows the simulation result of the whole FV circuit, the output voltage V_{FVC} will be regulated after seven operation cycles.

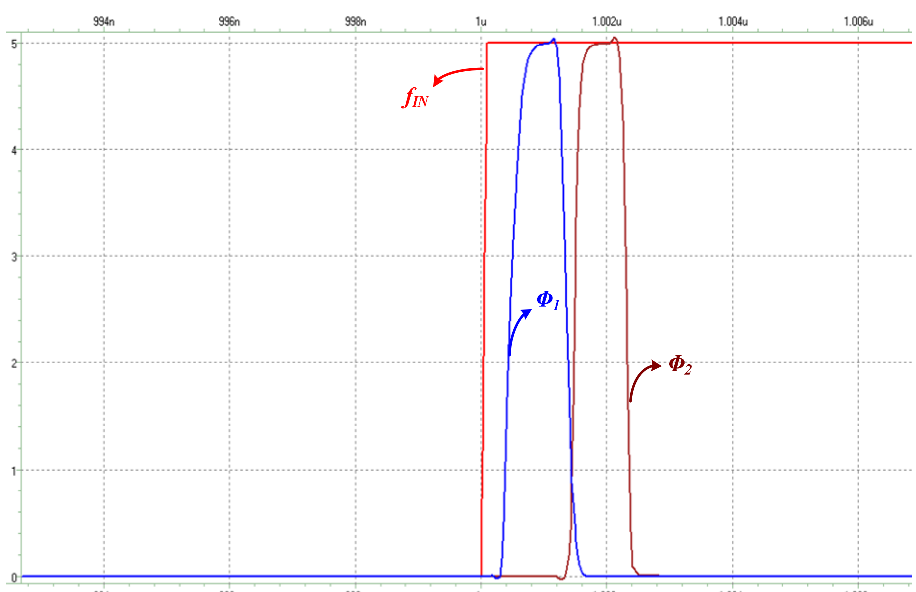


Fig. 44. The simulation result of the pulse generator

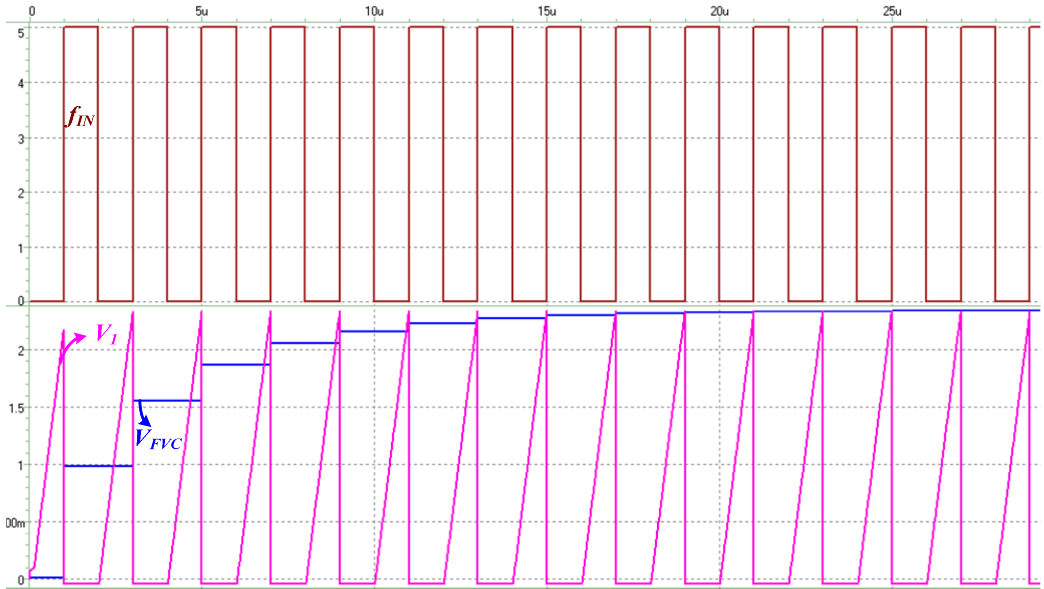


Fig. 45. The simulation result of the FVC circuit

4.4.2 The frequency to current converter

As illustrated in Fig. 44, frequency to current converter (FIC) circuit can output a current I_{SLC} that is proportional to operation frequency $\sqrt{f_{IN}}$ and the supply voltage V_{DIN}. Thus it is also proportional to the current I_{OUTP} in equation (32) and the root of P_{SW} at the same time. This circuit can be divided into third blocks, which are the F-I part, the I-$\sqrt{V}$ part, the voltage control resistance part and the V to I converter. In the F-I part, the FVC circuit is used to output a voltage V_{FVC} in equation (38). Due to the frequency divider in Fig. 40, the input frequency signal f_{IN} will be fixed at 50% duty and the off-time of it can be replaced by $T/2$ where the T is the period time of it. An equation is shown as follow to replace the equation (38) where K_1 is a constant.

$$V_{FVC} = K_1 \frac{I_C}{f_{IN}} \tag{39}$$

Because of the I_{OUTP} in equation (32) is proportion to the frequency $\sqrt{f_{IN}}$, an error amplifier is used to regulate the V_{FVC} to approach to the reference voltage V_{REF} and the transistor M_{N1} converts V_{FVC} into a current signal which is mirrored back to be the current input I_C of the FVC circuit providing a negative feedback path to regulate the current I_C. Finally a current I_f can be expressed as (40) where $K_2 = V_{REF} / K_1$.

$$I_f = I_C = K_2 f_{in} \tag{40}$$

The function of the I-$\sqrt{V}$ converter is to generate the root of the current I_f. After using the level shift transistor M_{PVT1}, the gate voltage V_{RFT} of the transistor M_{ROOT} is equal to ($V_{RF} - V_T$) and due to the characteristic of the relationship between gate voltage and drain current of the transistor operating in the saturation region, the value of V_{RFT} is also proportional to $\sqrt{f_{IN}}$ and expressed as (41) where K_4 is a constant.

$$V_{RFT} = K_4 \sqrt{K_2 f_{IN}} \tag{41}$$

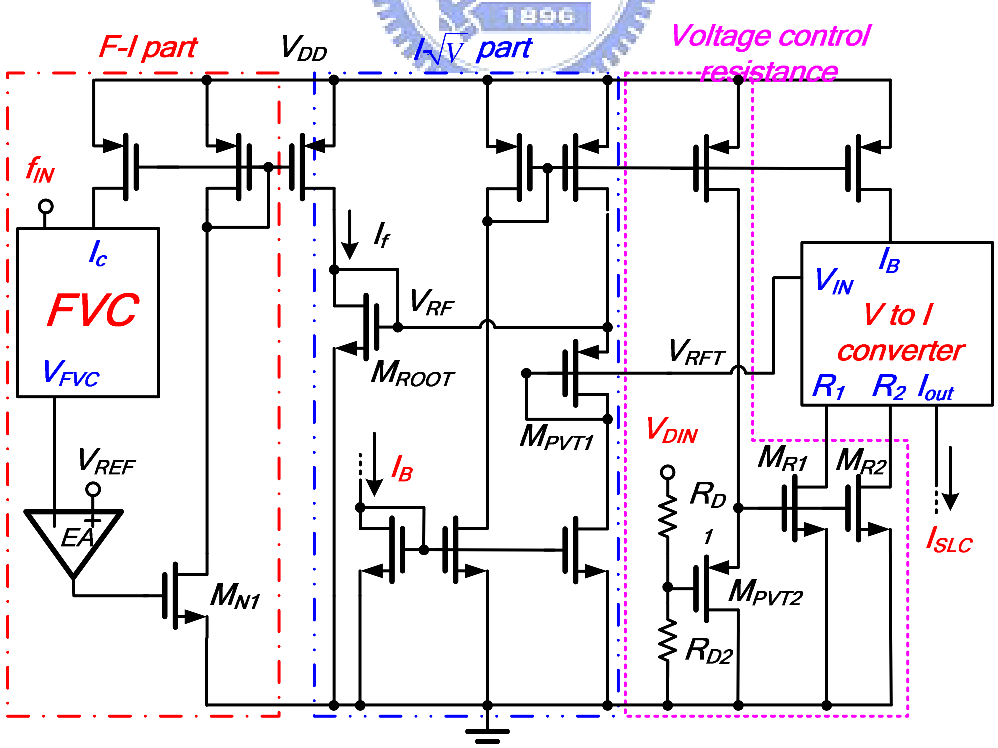


Fig. 46. The circuit implementation of the FIC circuit

In voltage control resistance part, the conversion resistance is implemented by a voltage-control-resistor (VCR). The resistors R_{D1} and R_{D2} ensure the transistors M_{R1} and M_{R2} operated in deep triode region and the transistor M_{PVT2} works as a level shift to compensate the V_T of the transistors M_{R1} and M_{R2}. The VCR resistance of R_{MR1} or R_{MR2}, which is the conversion resistance in the V-I circuit, is equal to $K_3V_{DIN}^{-1}$ with a constant K_3. The voltage-to-current (V to I) converter is shown in Fig. 47. The transistor M_{P1} works as a level shift to compensate a threshold voltage V_T. The M_{N1} transmute the voltage input V_{IN} into a current signal by the value of the resistance at R_1, the transistors M_{P2} and M_{N2} compensate the non ideal effect of the V to I circuit by the resistance R_2. Finally, the current I_{SLC} of the FIC circuit is decided by (42).

$$I_{SLC} = V_{RFT} / R_{MR1} = K_5\sqrt{f_{in}} \cdot V_{DIN}, \text{ where } K_5 = K_4\sqrt{K_2} / K_3 \qquad (42)$$

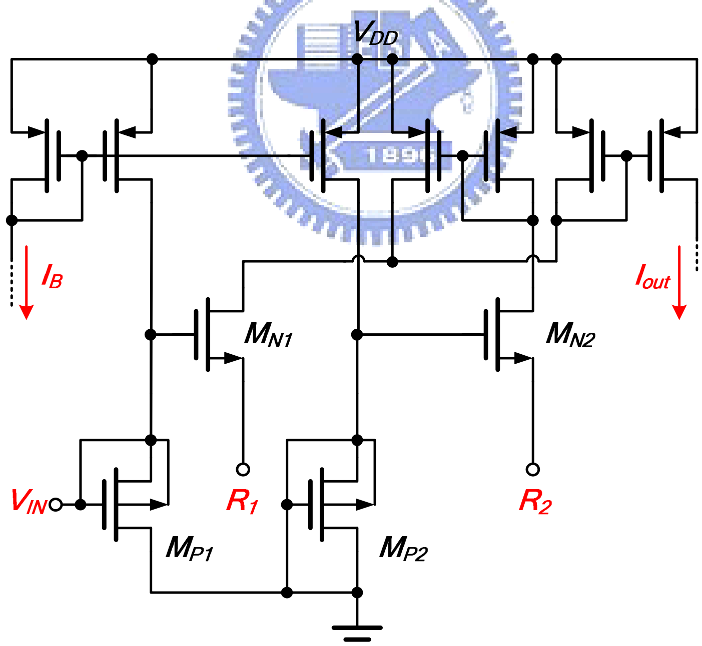


Fig. 47. The circuit implementation of the V to I converter

The simulation result shows the output current I_{SLC} of the FIC circuit under different operation frequency and supply voltage conditions, the current relationship can always fit the equation (42) for a the maximum error percentage 5.2% in a setting time less than 10 us.

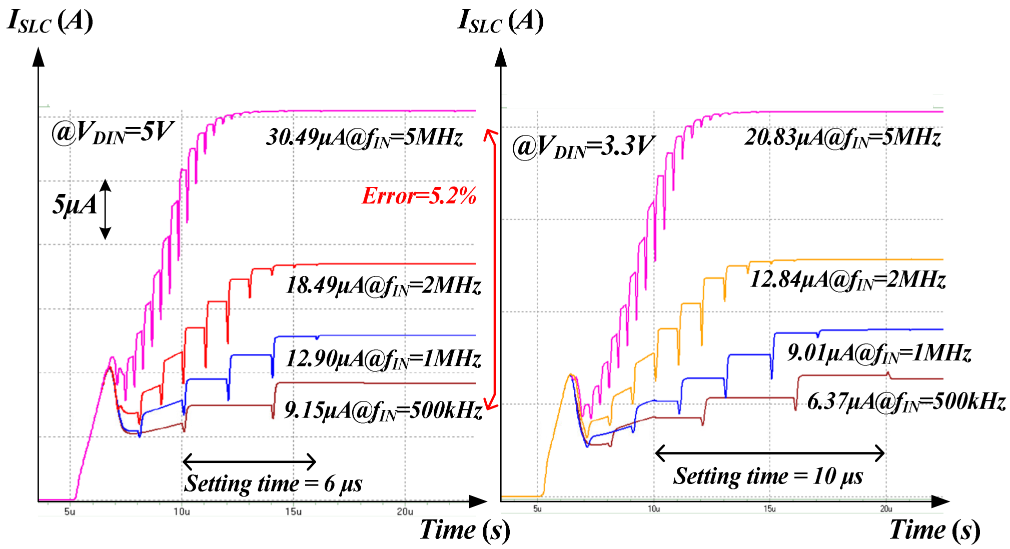


Fig. 48. The simulation result of the output current I_{SLC} of FIC circuit in different operation frequency for (a) 5V supply voltage (b) 3.3V supply voltage

4.4.3 The Logic circuit

The logic circuit outputs the control signal of the ORing MOSFET, the paralleling transistor in single module and the enable signal of the buck converters. The other function is to prevent the error during single-module operation. When operating in single modules, the buck converter with higher switching loss will be disabled and the switching signal *PWM* will be stop resulting in the corresponding current output I_{SLC} of the FIC circuit to be zero. The value of I_{WTA} is wrong in this situation because of the incorrect current input I_{SLC} of the converters which are shut down, the control logic must hold the pervious current result of the WTA circuit after entering the single module to keep the operation of system correctly until the system is transferred into paralleling modules or the enable signal of parallel control circuit is being reset. The logic can be implemented by the SR latch and the other combinational logic. The logic circuit and the flow chart of it can be shown in Fig. 49.

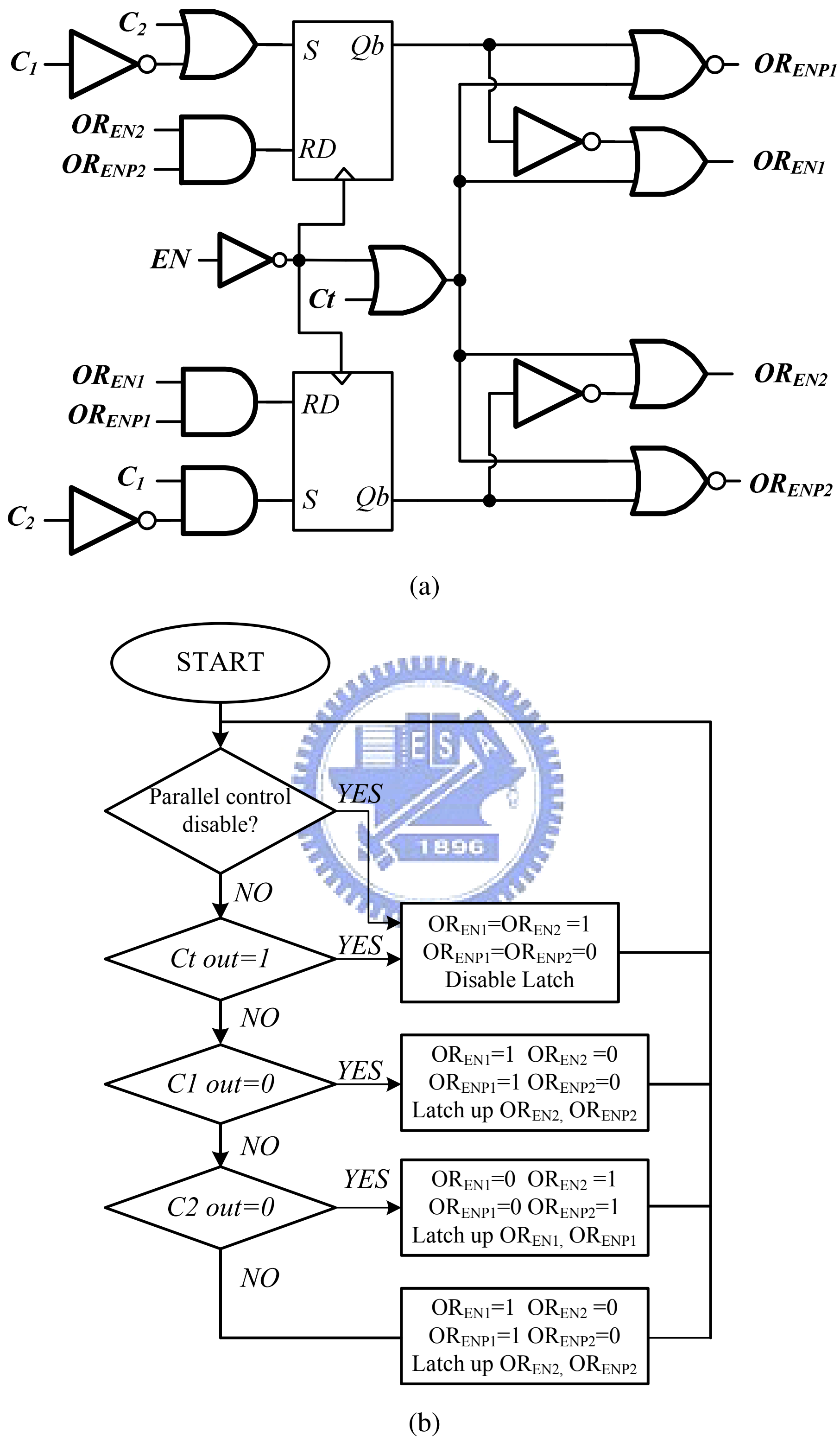


Fig. 49. (a) the logic circuit (b) the flow chart of the logic circuit

4.4 The whole circuit simulation result

The simulation is using TSMC 0.35μm environment, and using two paralleling connected buck converters to simulate the power management for IDDS. The droop resistance is set to be $5m\Omega$ and the initial no load output voltage of the buck converter is 2V and 2.02V, thus the original output current difference will be 4A. By setting the $V_{o(min)}$ to be 1.9V, Fig. 50 shows the output voltage and current waveform of two buck converters with 5V supplying voltage and 300KHz operation frequency, the current difference is sinking to $1A$ form $4A$, and the output voltage V_{OUT} is higher than $V_{O(min)}$ for all the output load current condition form 0A to 40A. In other word, the triangle waveform produced by the PNC method can really provide the current sharing enhancement and reducing the output voltage variations.

Fig. 51 is the output current waveform for I_{LOAD} , I_1 and I_2, where the V_{DIN}=3.3V and f_{IN}=1MHz for a buck converter and V_{DIN}=5V and f_{IN}=2MHz for another buck converter, the on-resistance of the power MOSFET is set to be $5m\Omega$ and using the ideal inductor and the $10000\mu F$ output capacitor with $1.5m\Omega$ ESR resistance. The transition point is 5.31A and the current I_{SLC} is 9.01μA, the corresponding I_{OUTP} will be 5.41A, the simulation shows the result is correct even the input conditions of buck converters are different and the output current difference is shirk into 1.03A. The output current waveform of the I_1 and I_2 are having some variation after into the paralleling modules from the single modules, it is because of the current I_{PNC} can't not perfectly keep the same between modules and resulting in a small transition responds occur at this time.

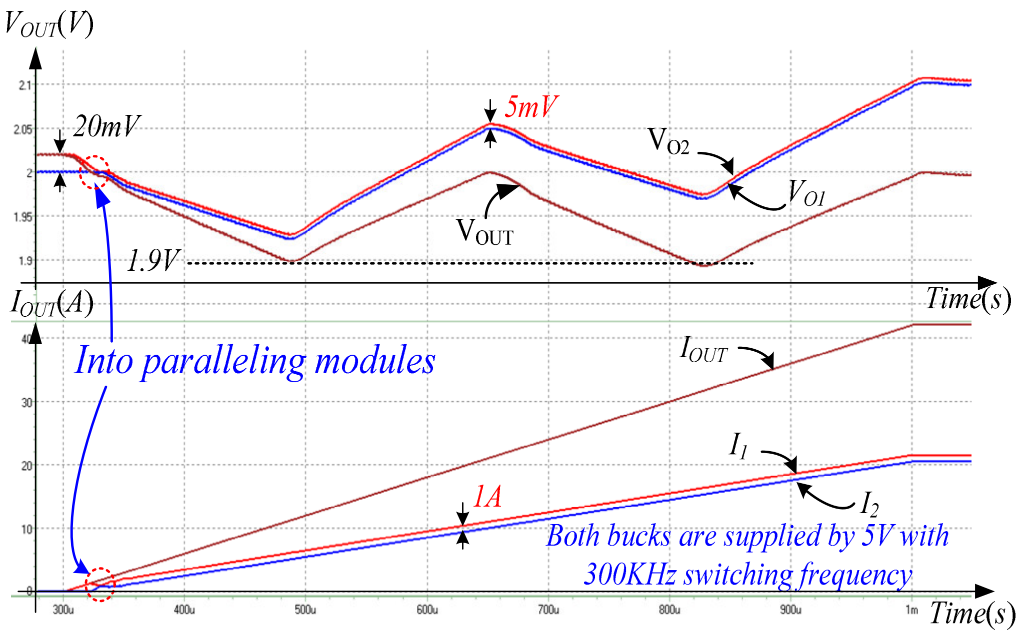


Fig. 50. The simulation result of the voltage and current waveform for paralleling system with IDDS technique

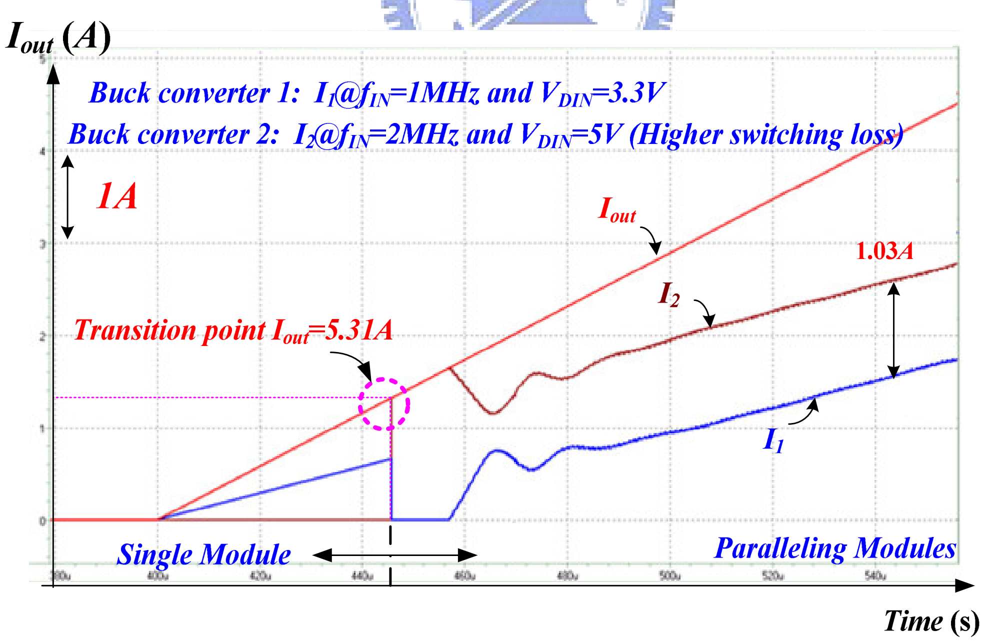


Fig. 51. The simulation result of the current waveform during the transition between two modules.

Chapter 5

Measurement Results and Conclusions

In this Chapter, experimental results with the set-up of the experiment environment are shown in Chapter 5.1. Finally, conclusions are made in Chapter 5.2 and the future work is described in Chapter 5.3.

5.1 Measurement Results

The IDDS circuit with power management was fabricated in TSMC 0.35μm 2P4M process. Fig. 50 shows the model of the system by means of the proposed IDDS circuit with SLC. Two buck converters BUCK 1 and BUCK 2 are used to emulate the paralleling system and estimate the performance of current sharing control. Two buck converters use external power n-type MOSFETs M_{NP1}, M_{NP2}, M_{NP3}, and M_{NP4} for high output current operation. Besides, the high-side power MOSFET uses the bootstrap technique. The on-resistances of power MOSFET and ORing MOSFET M_{OR} are $R_{ds(ON)}$ and $R_{ORds(ON)}$, respectively. The value of M_{ORP} is approximated to $5m\Omega$. The value of the input capacitor C_P of each power MOSFET is approximated to $4000pF$. The value of inductors L_1 and L_2 is $4.7\mu H$ and the DC resistance $R_{LDCR}=1m\Omega$. The IDDS circuit takes the low side MOSFET gate control signals PWM_1 and PWM_2 to be the operation frequency inputs of the buck converters. The value of the output capacitors C_{L1} and C_{L2}

is 12000μF with an ESR resistance (R_{CESR}) of 4 $m\Omega$. The test load current I_{LOAD} varies from 0A to 40A when the BUCK 1 operates under the supply voltage V_{DIN1} of 5V, the operation frequency of 2MHz, and the output voltage $Vo1$ of 2.02V. The BUCK 2 contains the supply voltage V_{DIN2} of 4.2V, the operation frequency of 1MHz and at the output voltage V_{O2} of 2V. After setting the $V_{o(min)}$ 1.9V and utilizing the conventional method, the current difference without IDDS technique is larger than 4A.

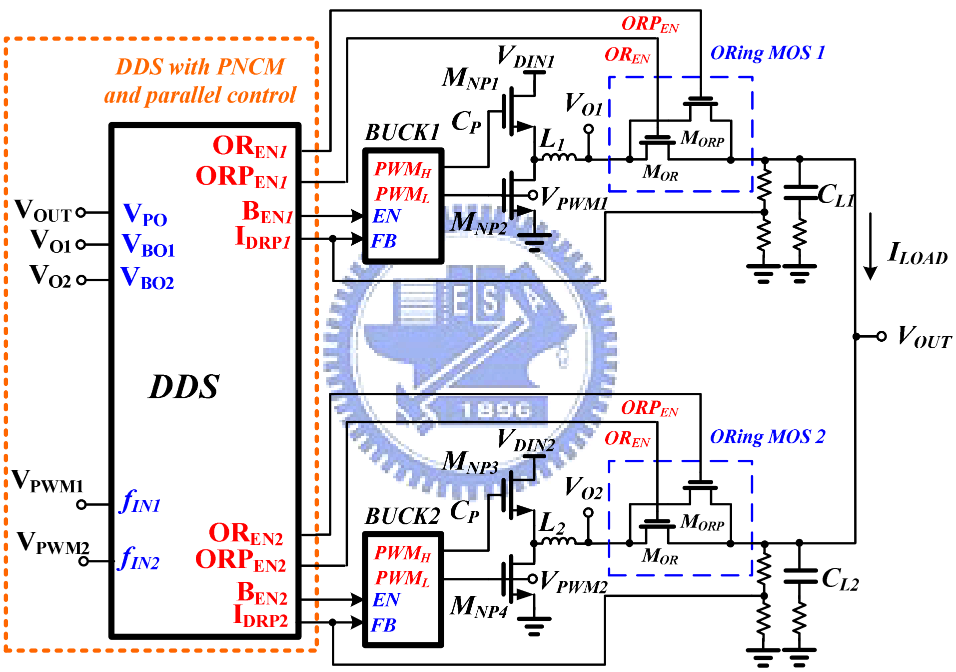
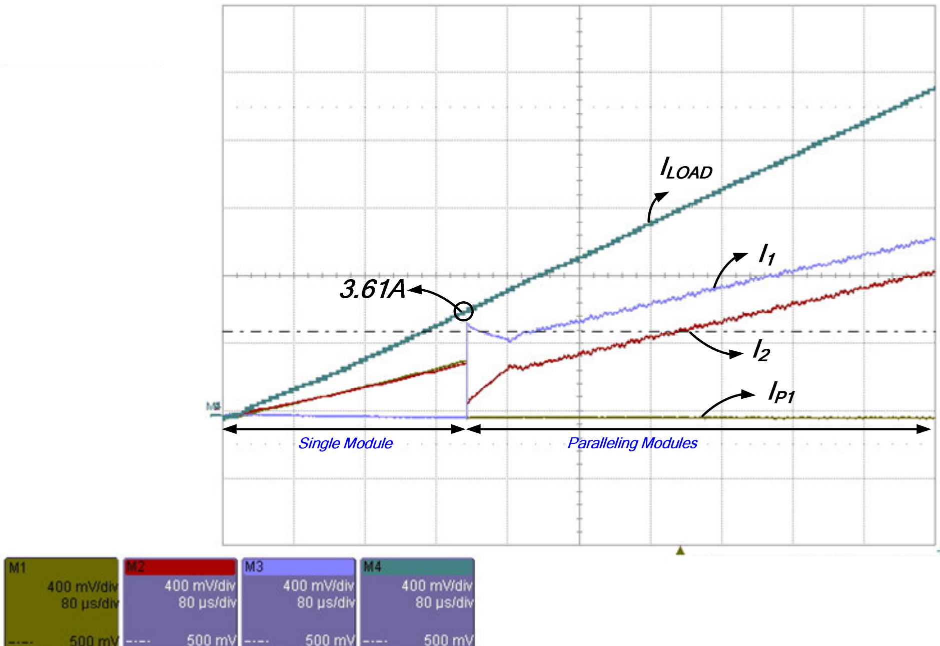
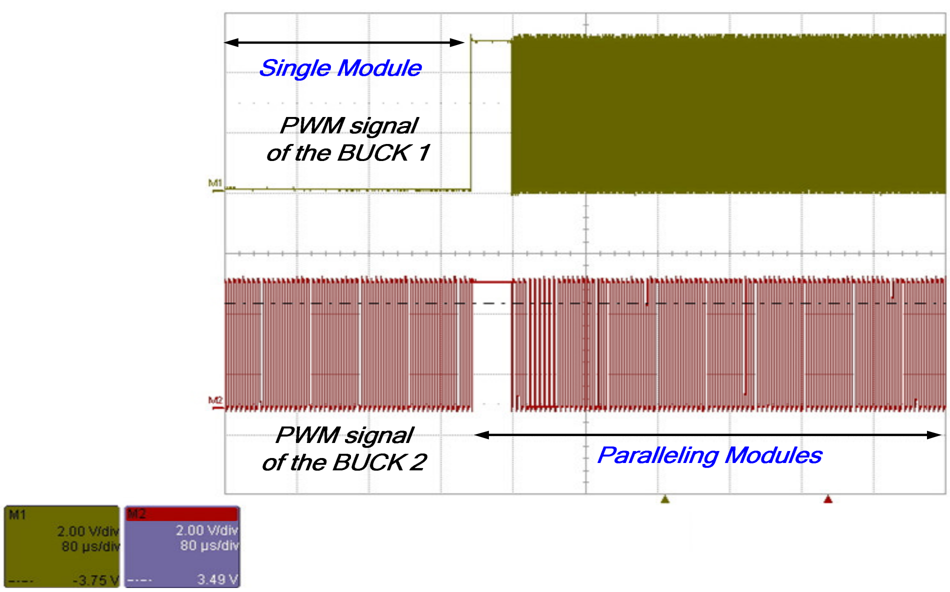


Fig. 52. The setup of the measurement environment.

The current waveforms of the BUCK 1 and BUCK 2 are shown in Fig. 53(a) by means of a 5X current probe. I_1 and I_2 are the currents flowing through the ORing MOSFETs M_{OR} of the corresponding buck converters. The current I_{P1} is the current flowing through the paralleling MOSFET M_{ORP} in single module. The transition current from single module to paralleling modules is 3.62A and the current difference is shrunk to 1.01A from a large current difference of 4A. The corresponding PWM signal waveforms are shown in Fig. 53(b). The output voltage waveforms of the measurement result for the paralleling connected system are shown in Fig. 54. The output voltage difference of the buck converters is shrunk to 5mV from 20mV and thus the output voltage can be kept above the $V_{o(min)}$.



(a)



(b)

Fig. 53. (a)the measured current waveform (b) corresponding PWM signal

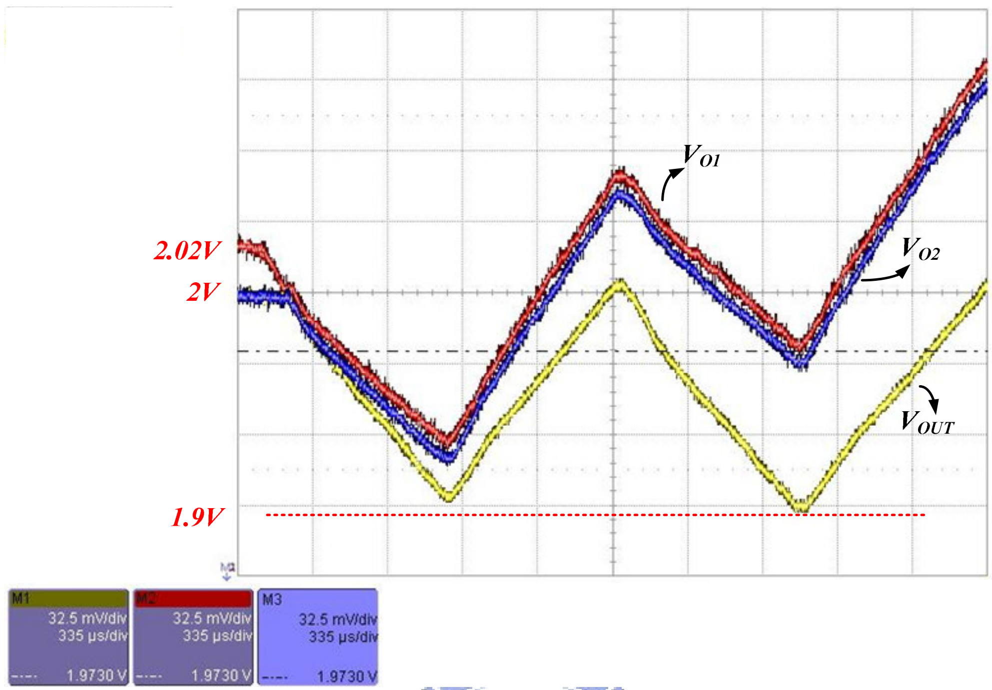


Fig. 54. The measured output voltage waveforms.

Table II shows the corresponding values of I_{OUTP} at different values of I_{SLC} when different values of the supply voltage V_{DIN} and the operation frequency f_{IN} are applied to the system.

TABLE II. The output current of the I_{SLC} corresponds to different experiment test conditions.

Switching Frequency (f_{IN})	I_{SLC} @V_{DIN}=3.3V / 5V	I_{OUTP}
500k	*6.17uA / 9.19uA*	*3.62A / 5.57A*
1M	*9.13uA / 13.2uA*	*5.52A / 7.81A*
2M	*12.93uA / 18.47uA*	*7.79A / 11.09A*
5M	*21.03uA / 32.04uA*	*12.44A / 19.13A*

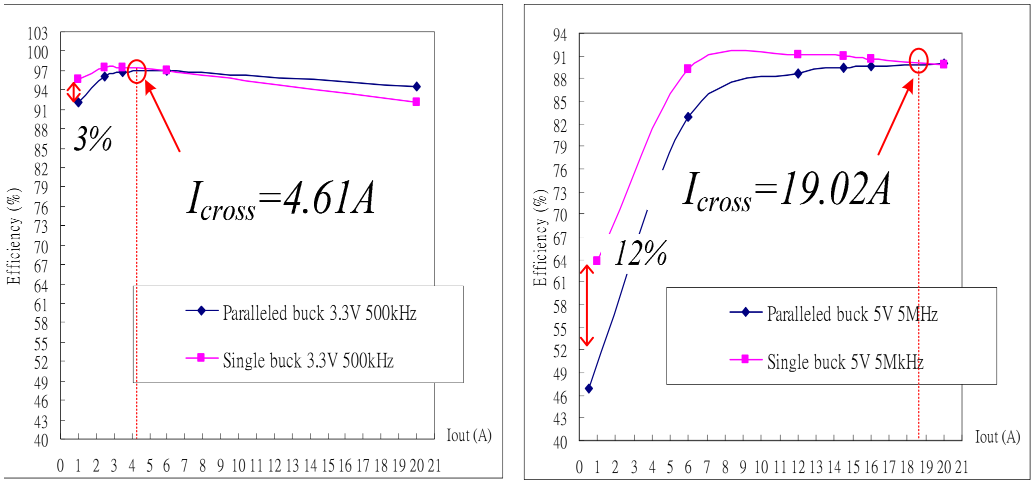
Fig. 55(a) shows the efficiency of single module and paralleling modules with V_{DIN}=3.3V and the switching frequency f_{IN}=500K Hz. The efficiency is calculation by (43).

$$Efficiency = \frac{V_{OUTn} I_{OUTn}}{V_{DINn} I_{OAVGn}} \tag{43}$$

I_{On} is the output current, V_{OUTn} is the output voltage, and the V_{INn} is the supply voltage of the buck converter n. After averaging the data of 100 duty cycles, I_{OAVGn} is the mean of the output current from V_{INn}.

The crossover current I_{CROSS} of the efficiency graph is 4.5A and the I_{OUTP} is 3.62A. The error is about 18%, which is caused by three major reasons. The first reason is the value mismatch of the parameters. The second reason is the bootstrap technique can not ideally boot the gate control signal of the high side power MOSFET to 2V_{DIN}. The last one reason is the current output of each buck converter is not actually equal to each other.

Fig. 55(b) is the efficiency graph of single module and paralleling modules for the buck converters with V_{DIN}=5V and the switching frequency f_{IN}=5MHz. The crossover current I_{CROSS} of the efficiency graph is 19.02A and the I_{OUTP} is 19.13A. The error is less than 1%, which is small than the previous experimental data since the power loss can be ignored at heavy loads. The efficiency improvements in these two conditions are 3% and 12%. When the load current is equal to 1A, the efficiency improvement of the condition in Fig. 55(b) is better than that of Fig. 55(a) owing to larger switching loss.



(a) (b)

Fig. 55. The comparison of the efficiency between single and paralleled buck converters in (a) V_{DIN}=3.3V and f_{IN} =500kHz (b) V_{DIN}=5V and f_{IN} =5MHz.

5.2 Conclusions

The power management is implemented in the multiple-input and single-output system in this paper. Owing to the design of switching loss calculation circuit and the positive-negative compensation method, the performance of current sharing and light-load efficiency can effectively improved. For the multiple kinds of the supply source of the buck converters such as NiH, NiCd, Li-ion batteries or the solar cells, the switching frequency of the buck converter can be different to each other. Experiment results show the efficiency can be improved approximately 12% at light loads. Besides, the IDDS circuit can control the paralleling buck converters to achieve high efficiency over a wide load range. Certainly, the proposed V-I triangle waveform by the PNC method really reduces the output voltage variations while doing current sharing enhancement.

5.3 Future work

Although the SLC circuit can detect the supply source and the operation frequency condition of the buck converters, the input capacitor of the external power MOSFET may affect the transition current between single module and paralleling modules. The SLC circuit can be more accurate if the input capacitor condition can be considered. On the other hand, there are many techniques proposed to reduce switching loss for single buck converter at the light loads. The SLC needs to combine with these techniques to achieve much improvement in power conversion efficiency not only implementing in the IDDS power management.

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