國　立　交　通　大　學

電機與控制工程學系

碩士論文

# 生醫應用之解析度可調變ΣΔ類比數位轉換器

# Sigma-Delta ADC with Configurable Resolution and Bandwidth for Biomedical Applications

研究生：張孟修

指導教授：林進燈 博士

中華民國 九十七 年 七 月

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碩士論文

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## 中文摘要

本論文的研究提出一個可依選擇的模式而改變解析度的三角積分類比數位轉換器，總共分為二種模式可供選擇，此二種模式依不同的輸入訊號而有不同需求的解析度，一為生理電訊號，一為生理影像訊號。則在生理電訊號和生理影像訊號的擷取系統中，透過後端的控制來轉換不同解析度的模式，達到不同通道共用一顆 ADC 的設計以結省整體系統面積和功耗。ADC 的架構選用 Sigma-Delta 的架構，主要分為二個部分：三角積分模組和後端的降頻數位濾波器。

此 ADC 電路操作在 1.28MHz 的操作頻率，訊號取樣頻率為 640kHz，對生理電訊號而言，超取樣率為 256；對生理影像訊號而言，超取樣率為 32。整個 ADC 電路的輸出為 SPI bus 標準介面輸出，使此電路可直接和後端的運算電路(DSP)作溝通。且使用低電壓源 1.5V 的電壓供應，最後結果為在生理電訊號的模式時，SNDR 為 60dB，ENOB 為 10-bit；在生理影像訊號模式時，SNR 為 50dB，ENOB 為 8-bit。此電路實現使用 TSMC 0.18-um 1P6M CMOS 製程，整體電路功耗 14.2mW，其中 Sigma-Delta modulator 的功耗為 0.98 mW；數位降頻濾波器和其餘數位控制電路功耗為 13.3 mW，其晶片大小為 3.21mm$^2$。

關鍵字：生理電訊號，生理影像訊號，三角積分調變器，二種模式，低電壓供應，SPI 介面，CIC filter，HB filter。

Sigma-Delta ADC with Configurable Resolution and Bandwidth for Biomedical Applications

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## Abstract

This paper presents a Sigma-Delta ADC which can change resolutions when the type of the input signal is different. This ADC provides two modes. One is designed for bio-electric signals; the other is designed for bio-image signals. This ADC can change its resolution by the control unit of a multi-channel design for bio-electric and bio-image signal through SPI. It includes two parts: Sigma-Delta modulator and decimation filter.

The proposed ADC operates at 1.28 MHz. Sampling rate is 640 kHz. For bio-electric signals, oversampling rate (OSR) is 256; for bio-image signals, OSR is 32. The ADC communicates with DSP or other devices by SPI bus. In the bio-electric signal mode, SNR is 50dB, effective number of bits (ENOB) is 10-bit; in the bio-image signal mode SNR is 50dB, ENOB is 8-bit. It has been fabricated by TSMC 0.18 μm CMOS 1P6M standard process. The total power consumption of the chip is about 14.4 mW under 1.5V supply, and the power consumption of Sigma-Delta modulator is about 0.98 mW; the power consumption of digital part is 13.3 mW. The area of the chip is 3.21 $mm^2$.

Keyword: Bio-electric signal, Bio-image signal, Sigma-Delta ADC, Configurable, low voltage supply, SPI bus, CIC filter, HB filter.

# 誌 謝

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感謝我的父母親張永宗先生和何雲琴女士對我的教育與栽培，並給予我精神及物質上的一切支援，使我能安心地致力於學業。此外也感謝弟弟張孟哲對我不斷的關心與鼓勵。

謹以本論文獻給我的家人及所有關心我的師長與朋友們。

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# Chapter 1

# Introduction

Architecture of a normal signal analyzing system is shown in Figure 1-1. Usually it includes a front end circuit, analog-to-digital converter (ADC) and operational unit, like DSP. The output of signal analyzing system will be the calculation result depending on different applications. Nowadays, system designed for biomedical application is more and more important. And these biomedical signals like Electroencephalogram (EEG) have to be analyzed by multi-channel inputs.

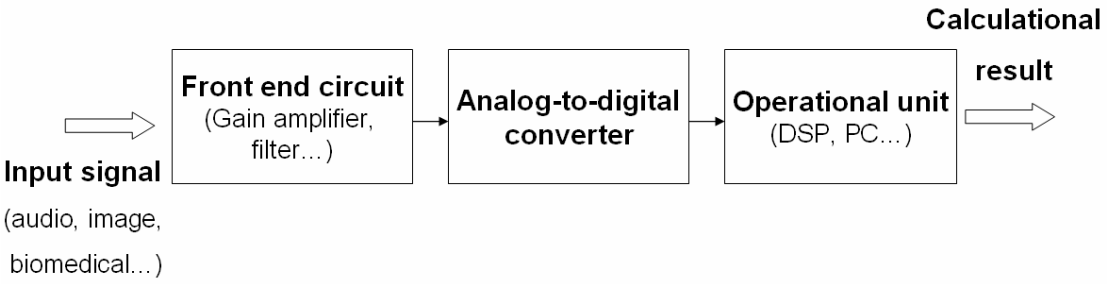



Figure 1 - 1: A signal analyzing system.

A multi-channel system architecture is shown in Figure 1-2. This is a normal and easy way to implement the system. The circuit of each channel is the same as other channels. And the communication interface will be connected between the sensors and operation unit, like digital signal processor (DSP). When the channel number is big, the cost such as power consumption and chip area will increase. So developing a

architecture to decrease the cost of multi-channel system is required. This research presents a ADC architecture with two modes which can be chosen when the input signal is different. The motivation will be introduced as follows.

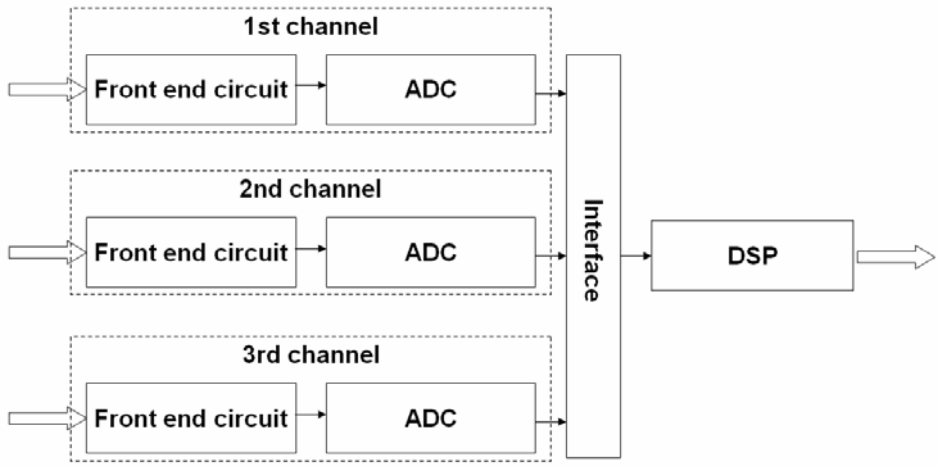



Figure 1 - 2: Multi-channel architecture.

## 1 - 1 Motivation

The block diagram of Electro-encephalogram(EEG) / Electro-cardiogram(ECG) / Electro-oculogram(EOG) / Electro-myogram(EMG) / functional near-infrared imaging (fNIR) multi-sensor platform is shown in Figure 1-3. We use three channels as example. There are three channels in the front of this system. A 3-to-1 multiplexer which can choose channel is beyond them. And Sigma-Delta ADC which will be introduced in this paper is between the multiplexer and DSP which can analyzes the signal. This ADC not only converts the analog signal to digital signal but can change the resolution by different signal applications. And the interface between ADC and DSP is a standard SPI bus. This architecture as Figure 1-3 can decrease the cost of the

system. The mode can be chosen by DSP. The ADC provides two modes can be chosen. One is designed for bio-electric signal which likes EEG, EKG, EOG and EMG; the other one is designed for bio-image signal which likes fNIR. But why do we chose Sigma-Delta ADC to implement? The discuss is describe as follows.

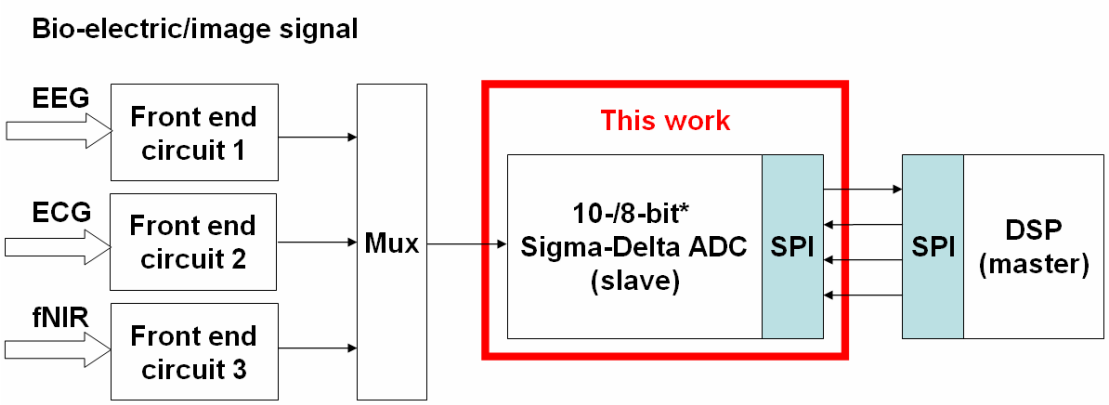



Figure 1 - 3: Block diagram of EEG/EKG/EOG/EMG/fNIRS multi-sensor platform.

## 1 - 2 Oversampling-rate ADC and Nyquist-rate ADC

There are several kinds of analog-digital converters in different applications. Usually, the ADC with high resolution and high speed is desired. But high resolution and high speed is not easy to be satisfied at the same time. The speed and resolution will be considered by different applications. According to the way of sampling, we can divide the ADC into two types of ADC. One is Nyquist-rate ADC, and the other one is Oversampling-rate ADC [18][19]. The different ADCs are divided by speed and accuracy as shown in Table 1 [20].

Table 1: Different architectures of ADC.

| **Low to Medium Speed High Accuracy** | **Medium Speed Medium Accuracy** | **High Speed Low to Medium Accuracy** |
|---|---|---|
| ◦ Integrating<br>◦ **Oversampling* (Sigma-Delta ADC)** | ◦ Successive-Approximation<br>◦ Algorithmic | ◦ Flash<br>◦ Two-Step<br>◦ Interpolating<br>◦ Folding<br>◦ Pipelined<br>◦ Time-Interleaved |

*Oversampling ADC is the only one which is not Nyquist-rate ADC

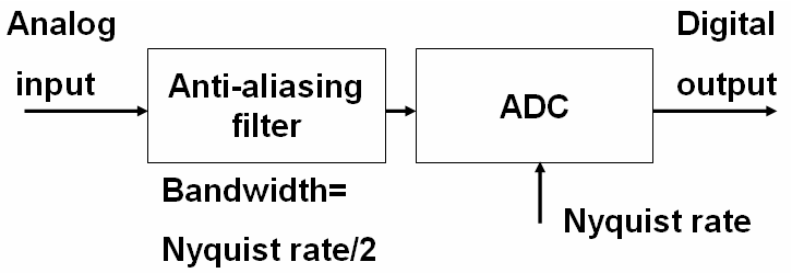
From Table 1, Oversampling-rate ADC is used in low to medium speed and for high accuracy. So the main differences between Oversampling ADC and Nyquist ADC are speed and resolution.

The sampling rate of Nyquist-rate ADC is 3 ~ 20 times of input bandwidth as shown in Figure 1-4 (a) and Figure 1-5 (a). And the sampling rate of Oversampling-rate ADC which is higher than Nyquist-rate ADC is 16 ~ 256 times of input bandwidth as shown in Figure 1-4 (b) and Figure 1-5 (b). It moves the noise in input bandwidth to high frequency to rise the resolution by oversampling and noise shaping. The sampling rate will be decimate to twice of input bandwidth by digital decimation filter. The advantages of oversampling-rate ADC is as follows [18][21].

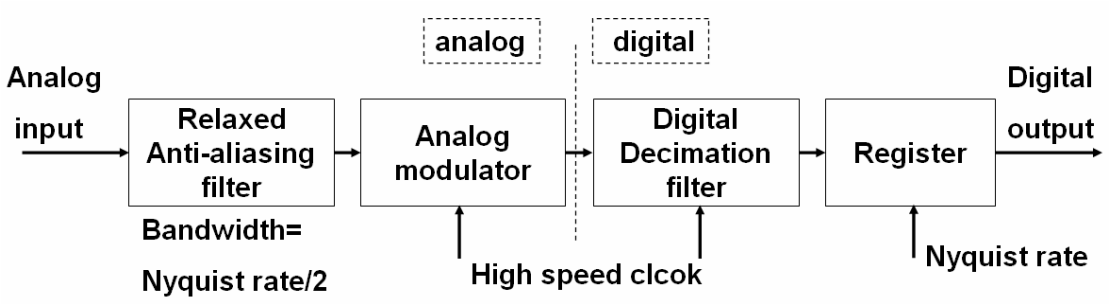
1. Lower the complexity of analog circuit
2. Additional S/H circuit is not needful.
3. Sensitivity of non-match circuit is lower.
4. Anti-aliasing filter is not needful.
5. Higher linearity, high SNR and high dynamic range.

Due to the characteristic of biomedical signal is belong to low speed, we choose

the oversampling-rate ADC to implement our design.




(a)




(b)

Figure 1 - 4: (a) Nyquist-rate and (b) Oversampling-rate ADC architecture.

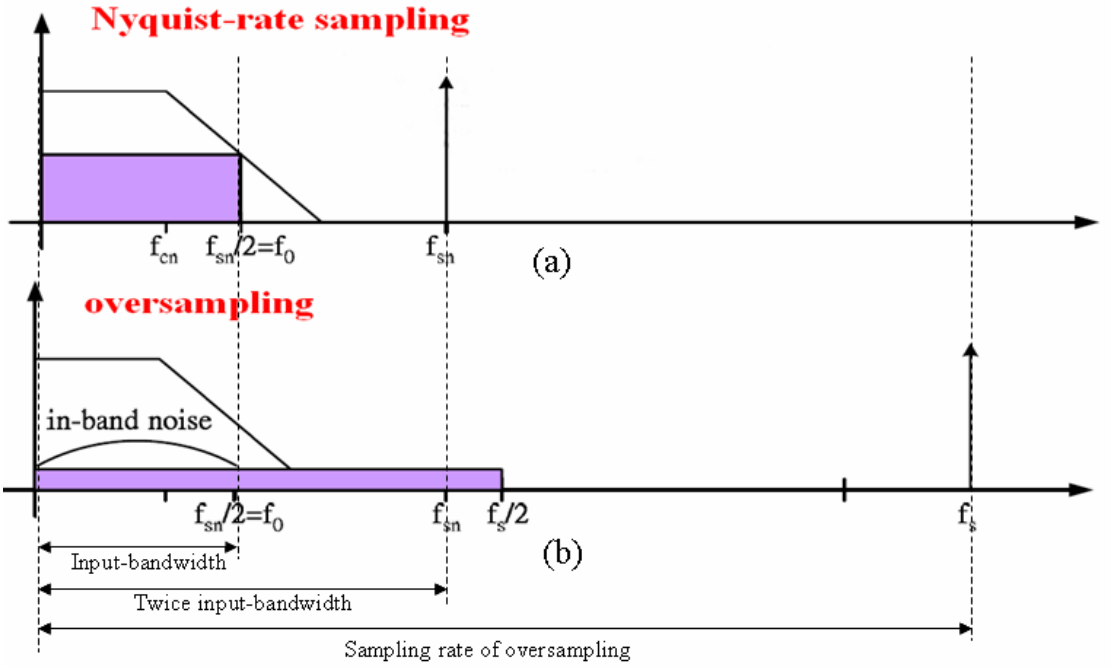



Figure 1 - 5: Spectrum (a) Nyquist-rate ADC (b) Oversampling-rate ADC.

## 1 - 3 Organization of the thesis

The paper is structured as follows. In chapter 2, the principle used in this ADC and related research will be described. The detail architecture of this ADC is discussed in chapter 3. Layout of the whole chip and testing issue are presented in chapter 4. And conclusions and future work are made in the last chapter.

# Chapter 2

# Theorem of Sigma-Delta ADC and Related Research

This chapter introduces the theorem of Sigma-Delta ADC. This introduction includes oversampling and noise shaping skill of Sigma-Delta modulator and theorem of decimation. We also introduce some recent research of Sigma-Delta ADC.

## 2 - 1 Theorem of Sigma-Delta Modulator

The conversion of a continuous-time analog signal into a digital one is done in two operations as shown in Figure 2-1. First there is a sampling of the analog signal (usually with a constant sample period $T_s$), then a quantization of the signal amplitude is done. If the signal band of a sampled signal is less than half the sampling frequency, the sampling in time is a completely invertible process. Looking at the frequency spectrum of a sampled signal in Figure 2-1 this could be understood. When a signal is sampled at uniform time intervals, this results in a periodicity of the signal spectrum at multiples of the sampling frequency, $f_s$, in the frequency domain as seen

in the Figure 2-2. With simple low-pass filtering it is clear that the original baseband spectrum can be reconstructed as long as the spectrums does not overlap. This is achieved when

$$f_s \geq 2 f_b = f_N , \tag{2. 1}$$

where $f_b$ is the bandwidth of the input signal. This equation is known as the Nyquist theorem, and $f_N$ is called the Nyquist frequency. An analog filter preceding the sampling operation is required to assure that the input signal bandwidth is limited to $f_b$. This filter is known as the anti-aliasing filter (AAF). A basic ADC structure is shown in Figure 2-1. An ADC working at a sampling frequency that equals to $f_N$ is called a Nyquist-Rate converter. These converters are hard to design in practice because of the zero transition band required for the AAF. To overcome this problem, this type of converters often use a slight amount of oversampling. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2 f_b}. \tag{2. 2}$$

Nyquist rate converters operates in most cases with an OSR = 1.5 ~ 10. Increasing the OSR greatly relaxes the demands to the AAF, thus simplifies the design and reduces the power and chip area of the filter.

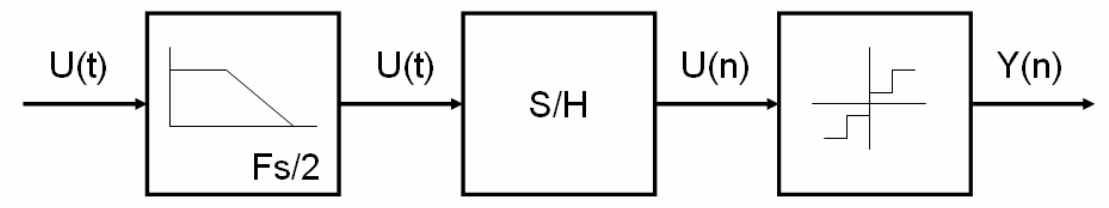



Figure 2 - 1: The operation diagram of ADC.

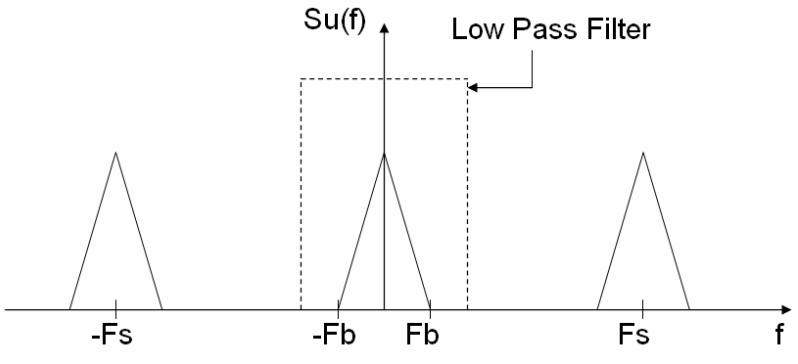



Figure 2 - 2: Spectrum of signal after sampling.

## 2 -1 - 1 Quantization

The quantizer encodes a continuous range of analog values into a set of predefined discrete levels. Quantization is usually uniform and the space between two adjacent output levels of the quantizer is defined as the quantizer step size:

$$\Delta = \frac{FS}{2^N - 1}, \tag{2. 3}$$

where FS is the full-scale input range and $2^N$ is the number of different output levels. Since an infinite number of input values of the sampled input signal is mapped to an finite number of values in the quantizer, the quantization is an noninvertible process. A very useful and important assumption for quantization noise is white. If the input signal x(n) has a rapidly and random varying behavior, the quantization noise e(n) can be approximated as a random number uniformly distributed between $\pm\frac{\Delta}{2}$ and uncorrelated with its previous values. It is also assumed that e(n) has statistical properties independent of x(n). By these properties, e(n) is classified as white noise with a mean square value of $e_{rms}^2 = \frac{\Delta^2}{12}$.

## 2 -1 - 2 Oversampling

When using a one-sided representation of the frequency domain, the power spectral density (PSD) of the quantization noise is :

$$S_e(f) = e_{rms}^2 (\frac{2}{f_s}). \tag{2. 4}$$

Equation (2.4) implies that the quantization noise is uniformly distributed in the frequency range $0 < f < f_s/2$. The signal band, however, might have a range from $0 < f < f_o$. The total in-band noise power is then calculated by using Eqs. (2.2) and (2.4):

$$q_{rms}^2 = \int_0^{f_o} S_e(f)df = \frac{2 f_o e_{rms}^2}{f_s} = \frac{e_{rms}^2}{OSR}. \tag{2.5}$$

Equation (2.5) shows for each doubling of OSR, the in-band noise power decreases by 3dB or 0.5 bits. Data converters employing oversampling to benefit from this property are called oversampled converters. By increasing the OSR they can achieve higher accuracy than Nyquist converters which use the same quantizer.

## 2 -1 - 3 Performance Metrics

This subsection reviews the key metrics, such as signal-to-noise ratio, dynamic range, and Nyquist rate, which are needed by the evaluation of the Sigma-Delta modulator quality.

**1. Total harmonic distortion (THD):**

THD is the ratio between the sum of the power of the higher harmonics, and the power of the fundamental harmonic.

**2. Signal-to-noise ratio (SNR):**

SNR is the ratio in power between the input sine wave $f_{in}$ and the noise of the converter from DC to Nyquist rate. SNR includes all noise sources in the modulator,

both thermal and quantization. It is typically expressed in decibels.

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right). \quad (2.6)$$

**3. Signal-to noise-distortion ratio (SNDR):**

SNDR is similar to SNR, except that it includes the harmonic content.

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right). \quad (2.7)$$

For small signal levels, distortion is not important. As the signal level increased, distortion degrades the modulator performance, and the SNDR will be less than the SNR.

**4. Dynamic range (DR):**

DR is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. Practically, the maximum input signal level is the input level where the SNDR drops 3dB beyond the peak. For an ADC, if the signal is too large, it will over-range the ADC input. If it is too small, the signal will get lost in the quantization noise of the converter.

**5. Spurious-free dynamic range (SFDR):**

SFDR is the ratio of the power value of the input sine wave with a frequency $f_{in}$ for an ADC, to the power value of the peak spur observed in the frequency domain. A large spur in the frequency domain may not significantly affect the SNR, but will significantly affect the SFDR. SFDR is a useful metric in communication applications, where the distortion component can be much larger than the signal of interest due to

the inter modulation of unwanted interferential signals. Consequently, the small input signals are masked into the spurs; the dynamic range of the ADC is attenuated.

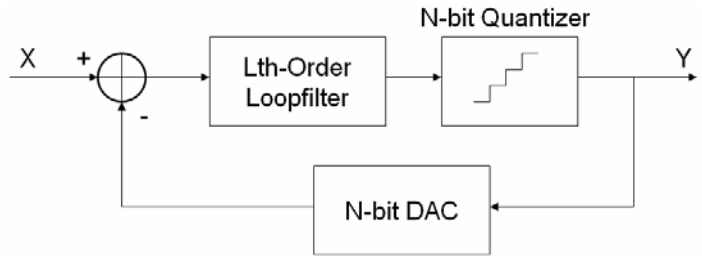
**6. Nyquist rate:**

Nyquist rate $f_N$ is the lowest sampling frequency that can be used for analog-to-digital conversion of a signal without resulting in significant aliasing. This frequency is twice the rate of the highest input frequency $f_b$. Therefore, Nyquist rate specifies the minimum sampling frequency required to avoid aliasing.

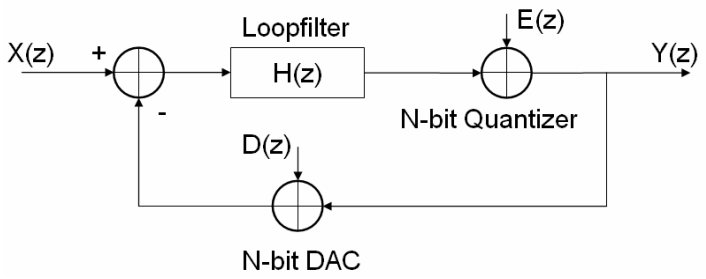
## 2 -1 - 4 The Concept of Sigma-Delta ADC

The basic idea of Sigma-Delta ADC is that it exchanges resolution in amplitude to resolution in time. In such ADC, the analog signal is modulated into a low resolution code at a frequency much higher than the Nyquist rates, and then the excess quantization noise is removed by the following digital filters. Thus, if OSR is high, the oversampling ADCs are very suitable for CMOS VLSI digital technology because it does not require high performance analog buildings.

Figure 2-3 shows the basic block diagram of a Sigma-Delta modulator and its corresponding linear model. The Sigma-Delta modulator consists of a feedforward path formed by a Lth-order loopfilter and a N-bit digital-to-analog converter (DAC). In the linear model as illustrated in Figure 2-3 (b), the DAC is assumed to be ideal, D(z) = 0, and the injected quantization error, E(z), of the quantizer is assumed as an




(a)




(b)

Figure 2 - 3: (a) Basic block diagram of a Sigma-Delta modulator (b) block diagram of Sigma-Delta modulator in Z-domain.

additive white noise approximation. In this way, the modulator can be considered as a two-input, on-output linear system. Therefore, a signal transfer function (STF) and a noise transfer function (NTF) can be derived:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)}. \tag{2. 8}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}. \tag{2. 9}$$

In the frequency domain, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z)X(z) + NTF(z)E(z). \tag{2.10}$$

By properly selecting the loop filter, the STF and the NTF of a theoretical Lth-order modulator yield in the z-domain:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-L}, \tag{2.11}$$

$$NTF(z)=\frac{Y(z)}{E(z)}=\frac{1}{1+H(z)}=(1-z^{-1})^{L}, \tag{2.12}$$

where $H(z)=1/(1-z^{-1})$. Figure 2-4 plots the frequency responses of NTFs with different orders of L. When the loop order is higher than one, the frequency response of NTF presents the characteristic of high-pass filters. The higher the order L is, the more quantization error energy is suppressed at low frequencies.

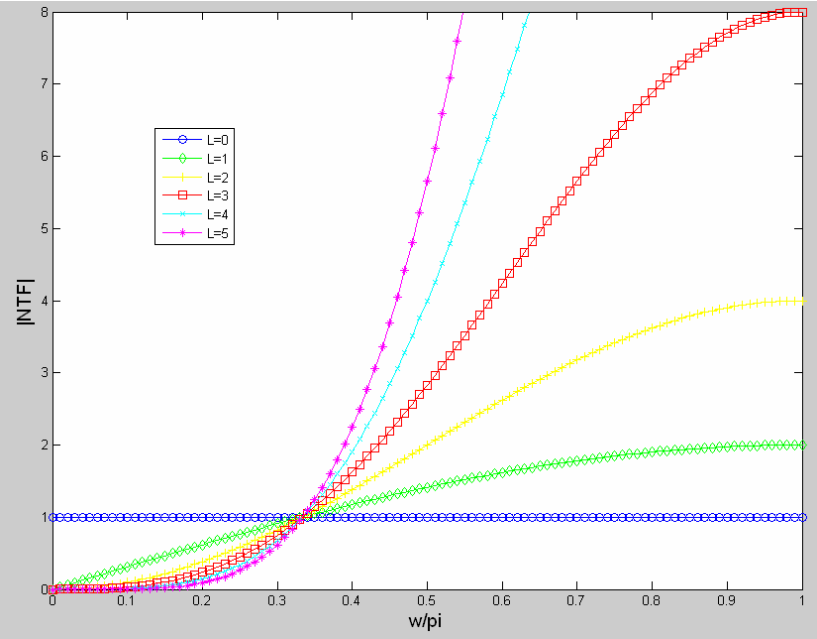



Figure 2 - 4: Spectrum of different L of |NTF|.

## 2 - 2 Digital Decimation FIR Filter

### 2 - 2 - 1 Decimation

The front stage of decimation filter is Sigma-Delta modulator which over-samples many time of input bandwidth. The decimation filter has to lower the sampling frequency to twice of input bandwidth. To lower the sampling rate is to lower the data number for digital signal process. In the frequency domain, the spectrum will be wider when the sampling rate is decimated. As shown in Figure 3-5, the spectrum will

be twice wide, if the sampling rate is decimation twice.

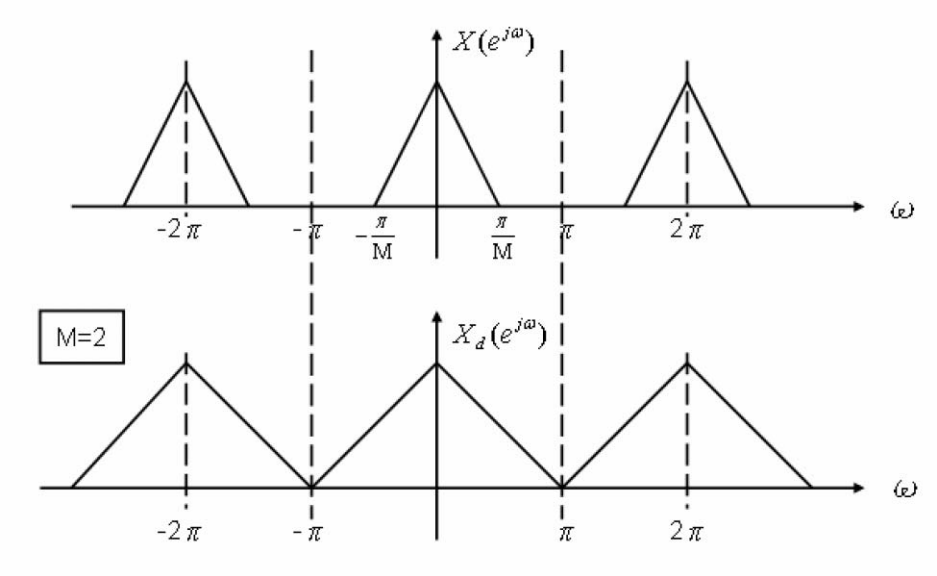



Figure 2 - 5: Spectrum when the sampling date is decimate twice.

The in-band signal will be complete after the sampling rate is decimate twice when the input bandwidth is in $\frac{\pi}{2}$. But the in-band signal will has aliasing situation which is shown in Figure 2-6 after the sampling rate is decimate twice when the input bandwidth is out of $\frac{\pi}{2}$. To avoid the aliasing situation, we have add a low-pass filter which is shown in Figure 2-6 before decimation. The cut off frequency of decimation filter is depend on the decimation rate. If the sampling rate has to be decimated M times, then the cut off frequency has to be $\frac{\pi}{M}$ to avoid the aliasing.

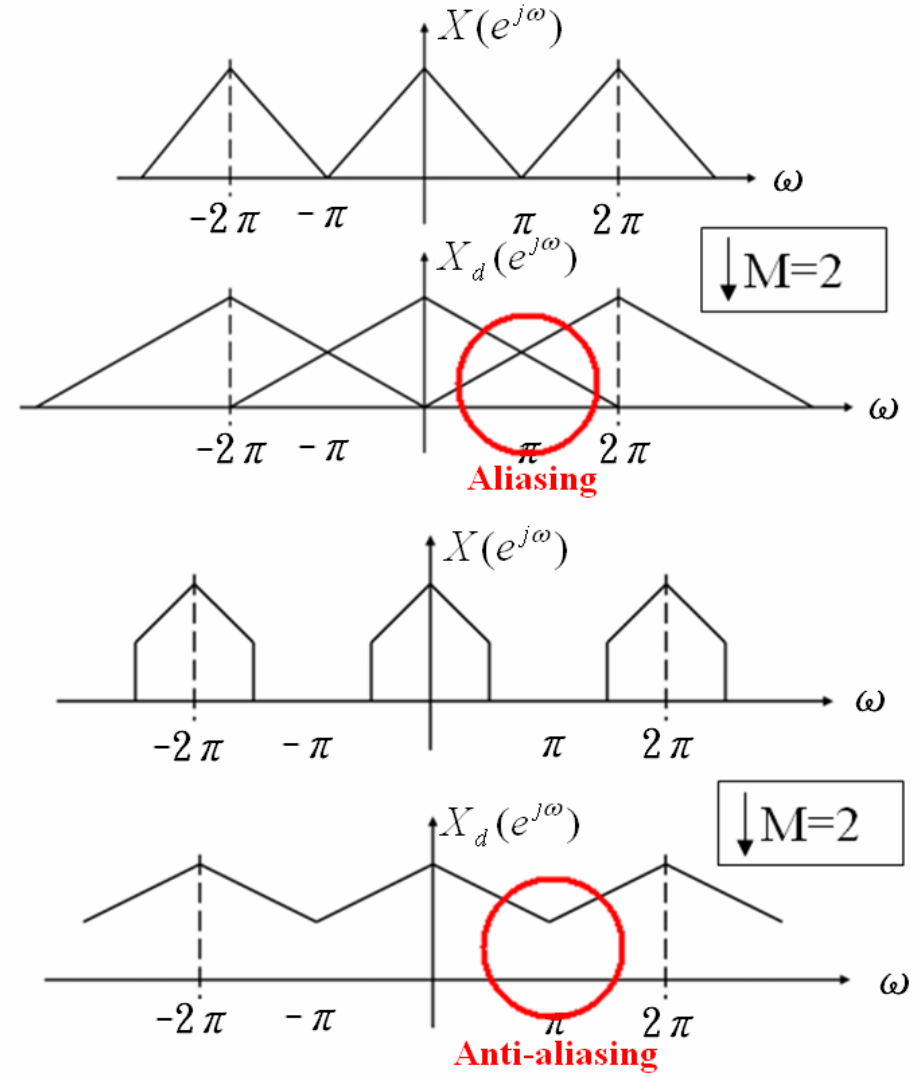



Figure 2 - 6: Spectrum with aliasing versus spectrum of anti-aliasing.

Usually we use multi-stage cascaded to realize the decimation filter. If we use single stage, then it has to decimate much times. Besides, the single stage filter must has a very low cut off frequency, it means the transition band has to be very sharp. The cost of single stage is higher order and bigger area, so we use the multi-stage cascaded to separate the cost and specification of decimation filter.

## 2 - 2 - 2 FIR Filter

Filter is a cell which can choose the frequency band to limit the signal on particular band, so it is a important part of digital signal process. There are two kinds of filter, one is FIR (finite impulse response, FIR) filter and the other one is infinite impulse response (IIR) filter.

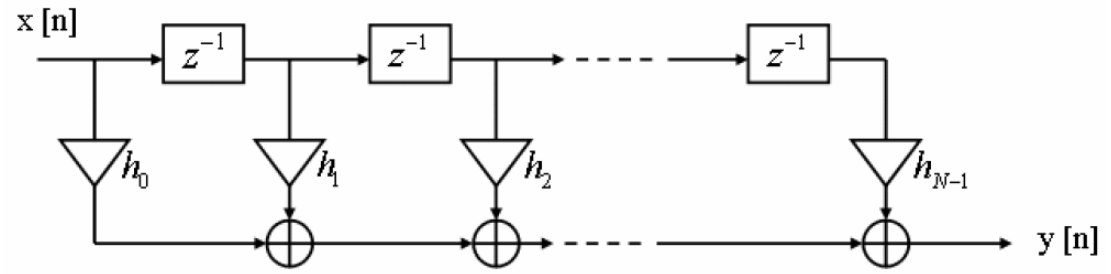
A FIR filter can be expressed to Eq. (2.13). After Z-transfer, we can obtain Eq. (2.14).

$$y[n]=\sum_{k=0}^{N-1}h_k x[n-k]. \tag{2.13}$$

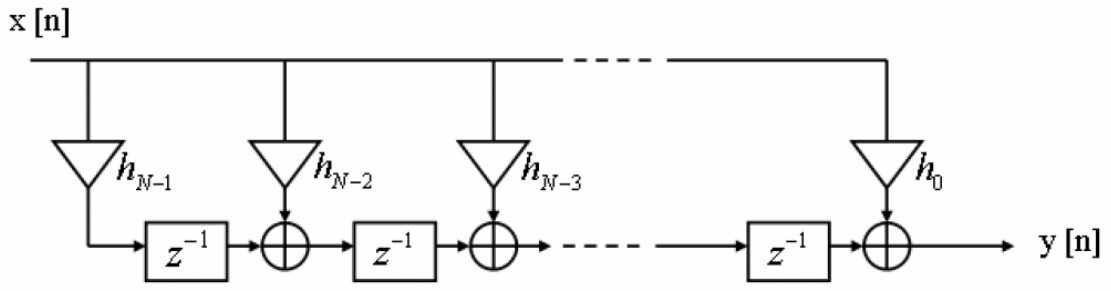
$$H(z)=\frac{Y(z)}{X(z)}=\sum_{k=0}^{N-1}h_k z^{-k}. \tag{2.14}$$

Additionally, $h_k$ means the k-th parameter, and X[z] and Y[z] mean the input and output respectively in time domain.

The basic architecture is shown in Figure 2-7.




(a)



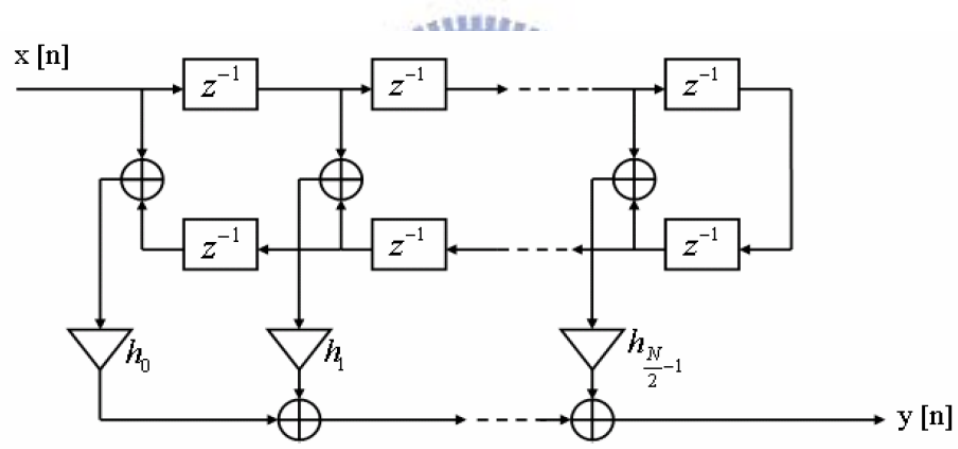

(b)

Figure 2 - 7: (a) direct architecture and (b) transfer-direct architecture of FIR filter.

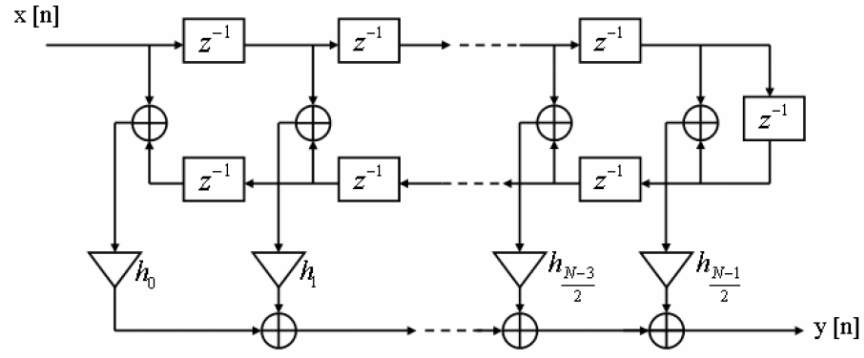
The delay cells "$z^{-1}$" shown in Figure 2-7 are registers. The advantage of the direct architecture is the bit-numbers of register are the same as bit-numbers of input; and the disadvantage is that when the taps of the FIR filter is more, the delay time will be longer to affect the sampling rate because the output is the sum of all multipliers. As compared with direct architecture, the advantage of transfer-direct architecture is the delay time won't be affected by tap number. But the disadvantage of transfer-direct architecture is the bit-number of register will be more. If the tap number of the FIR filter in this design is M + 1, then

$$h[M-n]=h[n], n=0,1,...,M\ . \tag{2.15}$$

Its parameters are symmetric, so it has a advantage which is linear phase.




(a)




(b)

Figure 2 - 8: Linear phase architecture of N-tap FIR filter, (a) when N is even and (b) N is odd.

We can simplify the direct architecture to linear phase architecture. The linear phase architecture of N-taps is shown in Figure 2-8. Due to the advantage of linear phase of FIR filter, the half multipliers can be reduced to lower the complex of this circuit.

## 2 - 3 CIC (Cascaded Integrator-Comb) Filter

As data converters become faster and faster, the application of narrow-band extraction from wideband sources, and narrow-band construction of wideband signals is becoming more important. These functions require two basic signal processing procedures: decimation and interpolation. And while digital hardware is becoming faster, there is still the need for efficient solutions. Techniques found in [8] work very well in practice, but large rate changes require very narrow band filters. Large rate changes require fast multipliers and very long filters. This can end up being the largest bottleneck in a DSP system.

In [10], an efficient way of performing decimation and interpolation was introduced. Hoginauer devised a flexible, multiplier-free filter suitable for hardware implementation, that can also handle arbitrary and large rate changes. These are known as cascaded integrator-comb filter, or CIC filters for short. An overview can also be found in [9]. An extension of CIC filters has been published in [11], and is briefly mentioned here.

### 2 - 3 - 1 Building Blocks

The two basic building blocks of a CIC filter are an integrator and a comb. An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

$$y[n] = y[n-1] + x[n]. \tag{2.16}$$

This system is also known as an accumulator. The transfer function for an integrator on the z-plane is

$$H_I(z) = \frac{1}{1 - z^{-1}}. \tag{2.17}$$

Using the Eq. from [12] for a single pole system, we can determine that

$$|H_I(e^{j\omega})|^2 = \frac{1}{2(1-\cos\omega)}, \tag{2.18}$$

$$ARG[H_I(e^{j\omega})] = -\tan^{-1}[\frac{\sin\omega}{1-\cos\omega}], \tag{2.19}$$

$$grd[H_I(e^{j\omega})] = \begin{cases} undefined, \omega = 0 \\ -\frac{1}{2}, \omega \neq 0 \end{cases}. \tag{2.20}$$

The power response is basically a low-pass filter with a -20dB per decade rolloff, but with infinite gain at DC. This is due to the single pole at z = 1; the output can grow without bound for a founded input. In other words, a single integrator by itself is unstable.

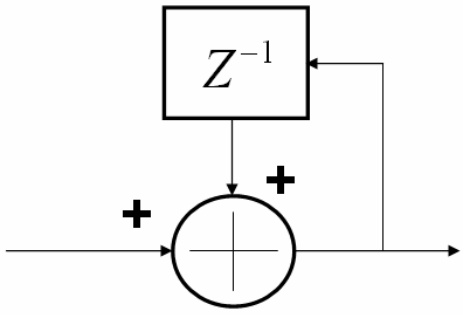



Figure 2 - 9: Basic Integrator.

A comb filter running at the high sampling rate, $f_s$, for a rate change of R is an odd-symmetric FIR filter described by

$$y[n] = x[n] - x[n - RM]. \tag{2.21}$$

In this Eq., M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at $f_s$

$$H_C(z) = 1 - z^{-RM}. \tag{2.22}$$

Again, we can determine that

$$|H_C(e^{j\omega})|^2 = 2(1 - \cos RM\omega), \tag{2.23}$$

$$ARG[H_C(e^{j\omega})] = -\frac{RM\omega}{2}, \tag{2.24}$$

$$grd[H_C(e^{j\omega})] = \frac{RM}{2}. \tag{2.25}$$

When R = 1 and M = 1, the power response is a high-pass function with 20dB per decade gain. When $RM \neq 1$, then the power response takes on the familiar raised cosine form with RM cycles from 0 to $2\pi$.

When we build a CIC filter, we cascade, or chain output to input, N integrator sections together with N comb sections. This filter would be fine, but we can simplify it by combining it with the rate changer. Using a technique for multirate analysis of LTI systems from [8], we can "push" the comb sections through the rate changer, and have them become

$$y[n] = x[n] - x[n - M]. \tag{2.26}$$

At the slower sampling rate $\frac{f_s}{R}$. We accomplish three things here. First, we have slowed down half of the filter and therefore increased efficiency. Second, we have reduced the number of delay elements needed in the comb sections. Third, and most important, the integrator and comb structure are now independent of the rate change. This means we can design a CIC filter with a programmable rate change and keep the same filtering structure.

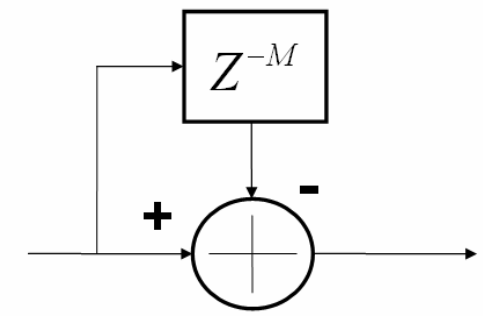



Figure 2 - 10: Basic Comb filter.

To summarize, a CIC decimator would have N cascaded integrator stages clocked at $f_s$, followed by a rate change by a factor R, followed by N cascaded comb stages running at $\frac{f_s}{R}$. A CIC interpolator would be N cascaded comb stages running at $\frac{f_s}{R}$, followed be a zero-stuffer, followed by N cascaded integrator stages running at $f_s$.

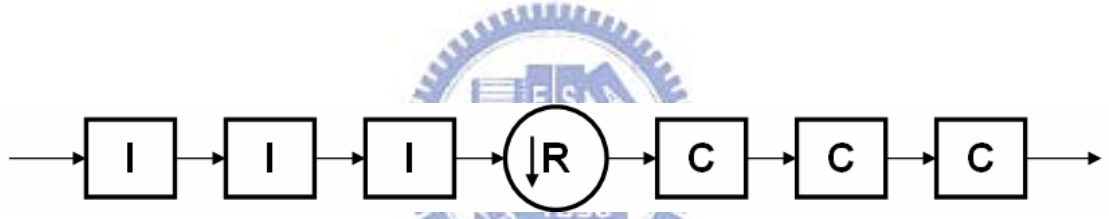



Figure 2 - 11: Three Stage Decimating CIC Filter.


Figure 2 - 12: Three Stage Interpolating CIC Filter.

## 2 - 3 - 2 Frequency Characteristics

The transfer function for a CIC filter at $f_s$ is

$$H(z) = H_I^N(z) H_C^N(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = (\sum_{k=0}^{RM-1} z^{-k})^N . \qquad (2.27)$$

This Eq. shows that even though a CIC has integrators in it, which by themselves have an infinite impulse response, a CIC filter is equivalent to N FIR filters, each

having a rectangular impulse response. Since all of the coefficients of these FIR filters are unity, and therefore symmetric, a CIC filter also has a linear phase response and constant group delay.

The magnitude response at the output of the filter can be shown to be

$$|H(f)| = \left| \frac{\sin \pi M f}{\sin \frac{\pi f}{R}} \right|^N . \tag{2.28}$$

By using the relation $\sin x \approx x$ for small x and some algebra, we can approximate this function for large R as

$$|H(f)| \approx \left| RM \frac{\sin \pi M f}{\pi M f} \right|^N , \text{ for } 0 \le f < \frac{1}{M} . \tag{2.29}$$

We can notice a few things about the response. One is that the output spectrum has nulls at multiples of $f = \frac{1}{M}$. In addition, the region around the null is where aliasing/imaging occurs. If we define $f_c$ to be the cutoff of the usable passband, then the aliasing/imaging regions are at

$$(i - f_c) \le f \le (i + f_c) , \tag{2.30}$$

for $f \le \frac{1}{2}$ and $i = 1, 2, ..., \left\lfloor \frac{R}{2} \right\rfloor$. If $f_c \le \frac{M}{2}$, then the maximum of these will occur at the lower edge of the first band, $1 - f_c$. The system designer must take this into consideration, and adjust R, M, and N as needed.

Another thing we can notice is that the passband attenuation is a function of the number of stages. As a result, while increasing the number of stages improves the imaging/alias rejection, it also increases the passband "droop." We can also see that the DC gain of the filter is a function of the rate change.

### 2 - 3 - 3 Bit Growth

For CIC decimators, the gain G at the output of the comb section is

$$G = (RM)^N . \tag{2.31}$$

Assuming two's complement arithmetic, we can use this result to calculate the number of bits required for the last comb due to bit growth. If $B_{in}$ is the number of input bits, then the number of output bits, $B_{out}$, is

$$B_{out} = \lceil N \log_2 RM + B_{in} \rceil . \tag{2.32}$$

It also turn out that $B_{out}$ bits are needed for each integrator and comb stage. The input needs to be sign extended to $B_{out}$ bits, but LSB's can either be truncated or rounded at later stages. The analysis of this is beyond the scope of this tutorial, but is fully described in [10].

For a CIC interpolator, the gain, G, at the ith stage is

$$G_i = \begin{cases} 2^i, i = 1, 2, ..., N \\ \dfrac{2^{2N-i}(RM)^{i-N}}{R}, i = N+1, ..., 2N \end{cases} . \tag{2.33}$$

As a result the register width, $W_i$, at ith stage is

$$W_i = \lceil B_{in} + \log_2 G_i \rceil , \tag{2.34}$$

and

$$W_N = B_{in} + N - 1 . \tag{2.35}$$

If M = 1. Rounding or truncation cannot be used in CIC interpolators, except for the result, because the small errors introduced by rounding or truncation can grow without bound in the integrator sections.

It is now worth revisiting the unstable aspect of the integrator stages. It turns out that it is not a problem. For decimators, integrator overflow is not a problem as long as two's complement math is used and we don't expect an overall system gain > 1. For interpolators, the comb stages and zero stuffing will prevent integrator overflow.

### 2 - 3 - 4 Implementation Details

Due to the passband droop, and therefore narrow usable passband, many CIC designs utilize an additional FIR filter at the low sampling rate. This filter will equalize the passband droop and perform a low rate change, usually by a factor of two to eight.

In many CIC designs, the rate change R is programmable. Since the bit growth is a function of the rate change, the filter must be designed to handle both the largest and smallest rate changes. The largest rate change will dictate the total bit width of the stages, and the smallest rate change will determine how many bits need to be kept in the final stage. In many designs, the output stage is followed by a shift register that selects the proper bits for transfer to the final output register. A system designer can use the Eq. for $B_{out}$ for a decimator and $W_{2N}$ for an interpolator to calculate proper shift values.

For a CIC decimator, the normalized gain at the output of the last comb is given by

$$g = \frac{(RM)^N}{2^{\lceil N \log_2 RM \rceil}}. \tag{2.36}$$

This lies in the interval $\left(\frac{1}{2}, 1\right]$. Note that when R is a power of two, the gain is unity. This gain can be used to calculate a scale factor, s, to apply to the final shifted output.

$$s = \frac{2^{\lceil N \log_2 RM \rceil}}{(RM)^N}. \tag{2.37}$$

Which lies in the interval $[1, 2)$. By doing this, the CIC decimation filter can have unity DC gain.

### 2 - 3 - 5 Sharpened CIC Filters

Filter sharpening can be used to improve the response of a CIC filter. This technique applies the same filter several times to an input to improve both passband and stopband characteristics. If H(z) is a symmetric FIR filter, then a sharpened version, $H_S(z)$, can be expressed as

$$H_S(z) = H^2(z)[3 - 2H(z)]. \tag{2.38}$$

The magnitude response of a sharpened CIC filter would then be

$$\left|H(f)\right| = \left| 3\left(\frac{\sin \pi Mf}{\sin \frac{\pi f}{R}}\right)^{2N} - \left(2\frac{\sin \pi Mf}{\sin \frac{\pi f}{R}}\right)^{3N} \right|. \tag{2.39}$$

The interested reader is referred to [11] for more details. Please note that it uses different parameters and implements a CIC filter a bit differently than [10].

Since their inception, CIC filters have become an important building block for DSP systems. They have found a particular niche in digital transmitters and receivers. They are currently used in highly integrated chips from Intersil, Graychip, Analog Devices, as well as other manufacturers and custom designs.

## 2 - 4 Relative Architecture Survey

We find three relative papers to our design. The first one is “Very Low-Voltage Digital-Audio ΔΣ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping.”[1] The second one is “A 2.5-V 14-bit, 180-mW Cascaded ΣΔ ADC for ADSL2+ Application.”[3] The third one is “A Reconfigurable A/D Converter for 4G Wireless Systems.”[22]. They will be introduced as follows.

## 2 - 4 - 1 Very Low-Voltage Digital-Audio ΔΣ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping

A 1-V 1-mW 14-bit ΔΣ modulator in a standard CMOS 0.35-um technology is resented in this paper. Special attention has been given to device reliability and power consumption in a switched-capacitor implementation. A locally bootstrapped symmetrical switch that avoids gate dielectric overstress is used in order to allow rail-to-rail signal switching. The switch constant overdrive also enhances considerably circuit linearity. Modulator coefficients of a single-loop third-order topology have been optimized for low power. Further reduction in the power consumption is obtained through a modified two-stage opamp. Measurement results show that for and oversampling ratio of 100, the modulator achieves a dynamic range of 88 dB, a peak signal-to-noise ratio of 87 dB and a peak signal-to-noise-plus-distortion ratio of 85 dB in a signal bandwidth of 25 kHz.

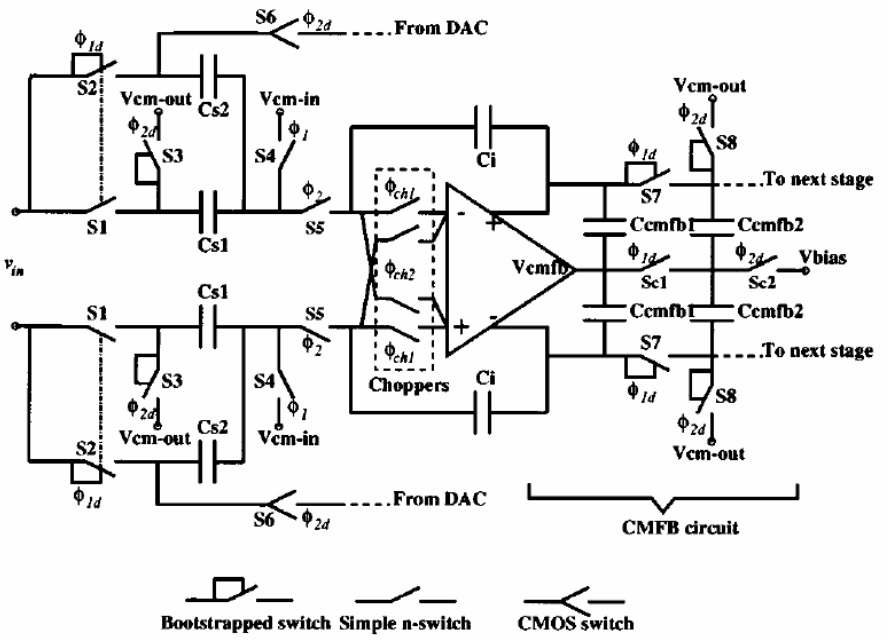



Figure 2 - 13: Fully differential low-voltage integrator.

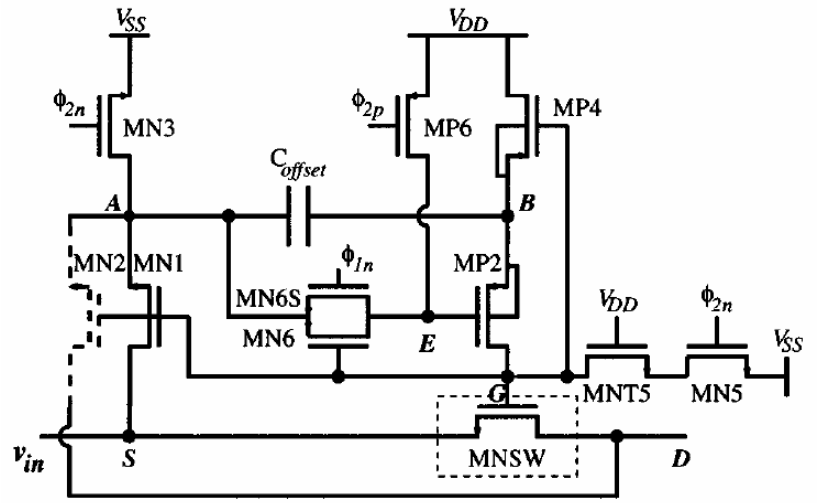



Figure 2 - 14: Transistor-level implementation of the bootstrapped switch.

## 2 - 4 - 2 Cascaded ΣΔ ADC for ADSL2+ Application

This paper presents a sigma-delta analog-to-digital converter for the extended bandwidth asymmetric digital subscriber line application. The core of the ADC is a cascaded 2-1-1 sigma-delta modulator that employs a resonator-based topology in the first stage, three tri-level quantizers, and two different pairs of reference voltages. As shown in the experimental result, for a 2.2-MHz signal bandwidth, the ADC achieves a dynamic range of 86 dB and a peak signal-to-noise and distortion ratio of 78 dB with an oversampling ratio of 16. It is implemented in a 0.25-um CMOS technology, in a 2.8 $mm^2$ active area including decimation filter and reference voltage buffers, and dissipates 180 mW from a 2.5-V power supply.

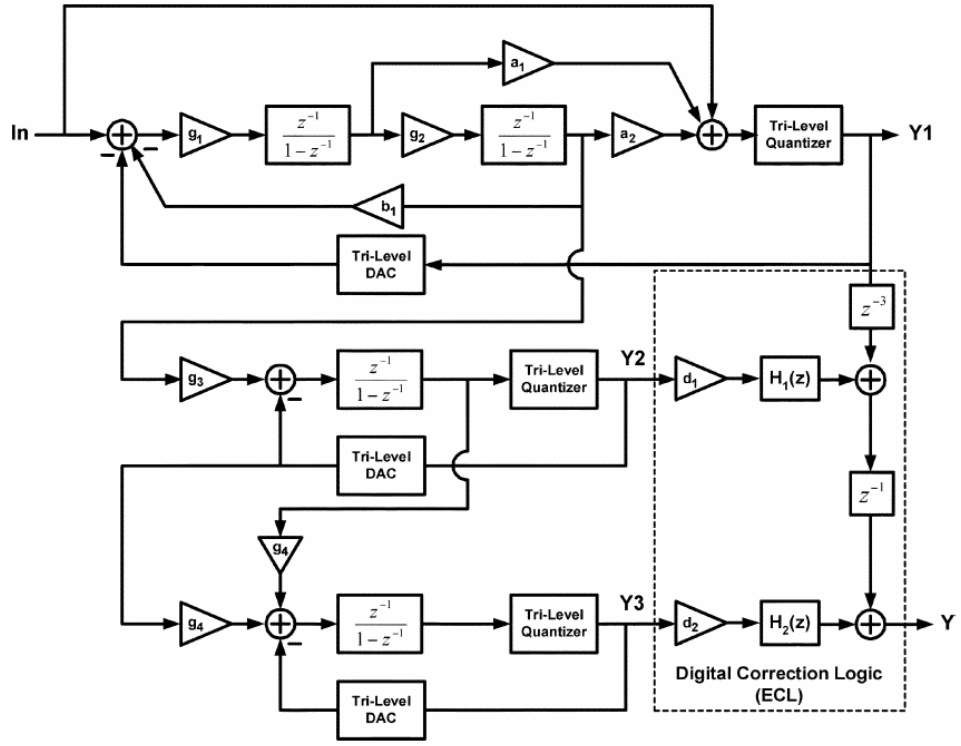



Figure 2 - 15: Block diagram of RMASH 2-1-1$_{1.5b}$.

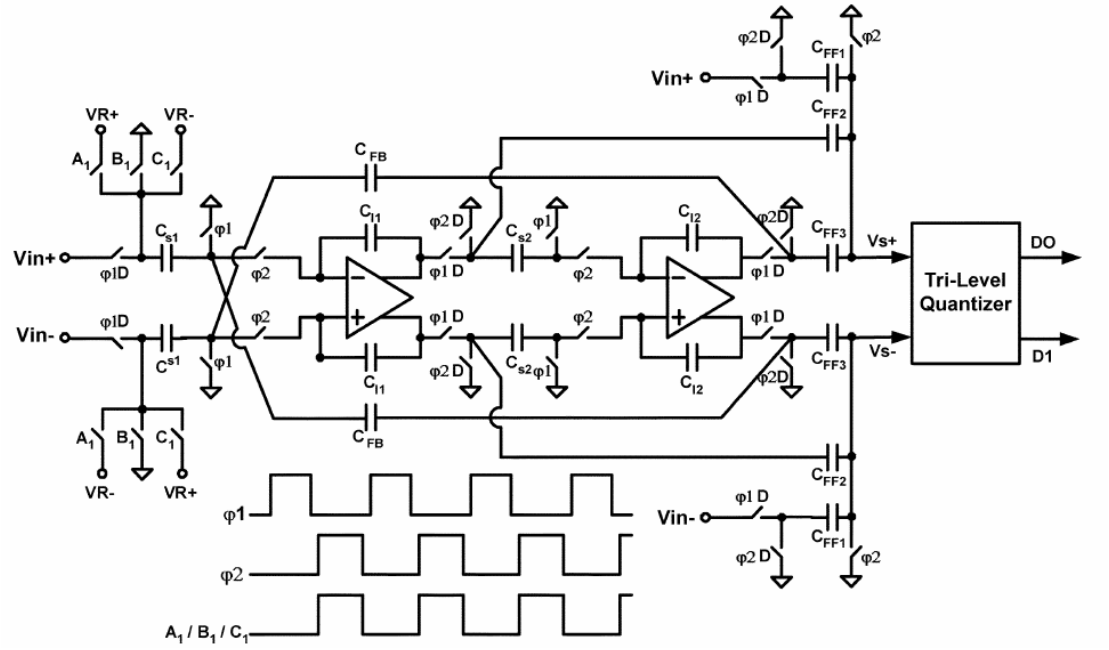



Figure 2 - 16: Circuit implementation of the first-stage modulator.

## 2 - 4 - 3 A Reconfigurable A/D Converter for 4G Wireless System

This paper presents a multi-standard reconfigurable Sigma-Delta modulator, which is able to support the predictable standards of fourth generation of mobile communication systems (4G). Furthermore, the proposed architecture halves the number of required analog-to-digital converters in parallel receivers, by processing concurrently two different signals. The major design issues are outlined and operation modes are detailed. A system-level simulation is performed to demonstrate the feasibility of the presented solution. The modulator is implemented into switched-capacitor circuits and device level simulations demonstrate the performance of the converter.

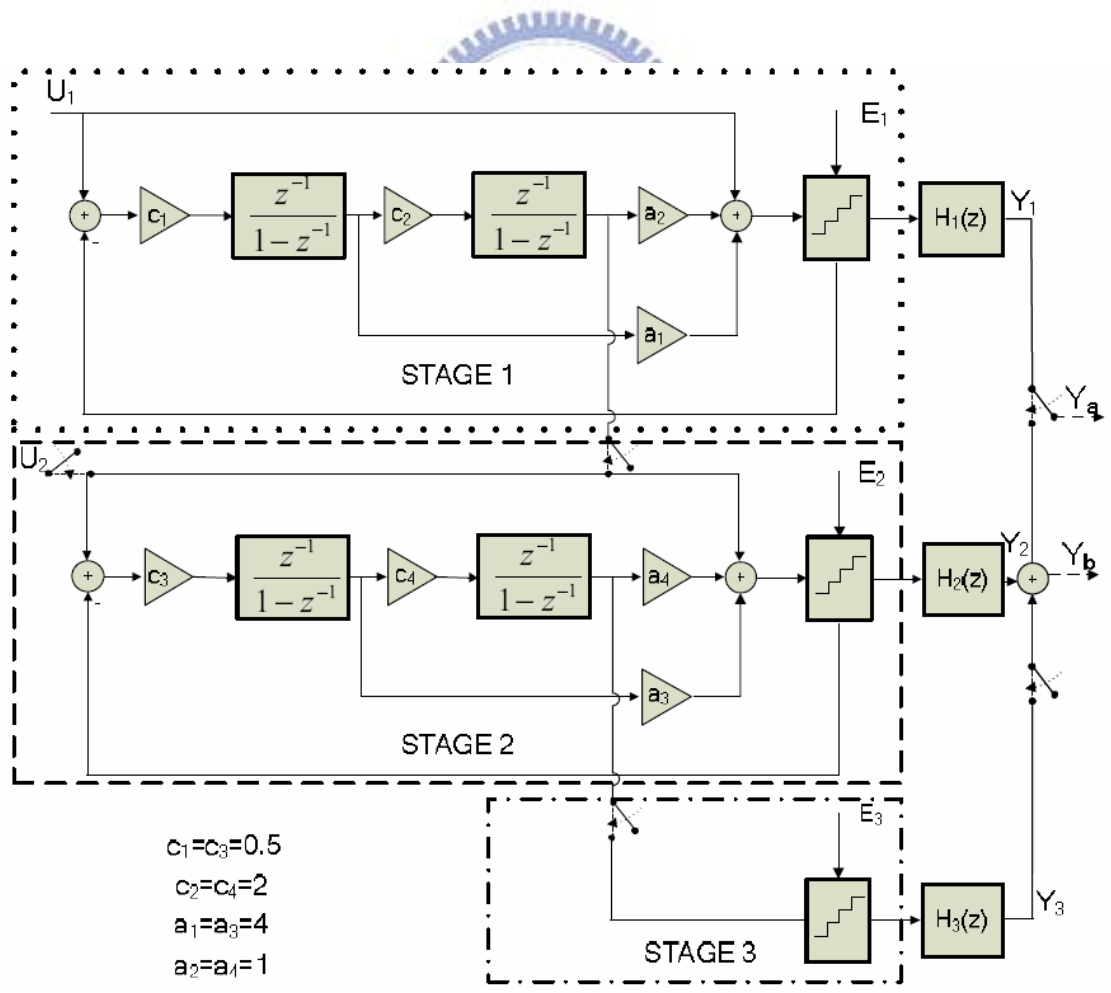



Figure 2 - 17: Block diagram of proposed architecture.

Table 2: Modulator Transfer Functions.

| Standard GSM | Digital filters | | | Modulator Output |
|---|---|---|---|---|
| | H1 | H2 | H3 | Y |
| Mode 1 | - | - | - | $U(z)+E1(z)\ (1-z^{-1})^2$ |
| Mode 2 | $z^{-2}$ | $(1-z^{-1})^2$ | - | $U(z)z^{-2}+E1(z)\ (1-z^{-1})^4$ |
| Mode 3 | $z^{-2}$ | - | $(1-z^{-1})^2$ | $U(z)z^{-2}+E1(z)\ (1-z^{-1})^2$ |
| Mode 4 | $z^{-4}$ | $z^{-2}(1-z^{-1})^2$ | $(1-z^{-1})^4$ | $U(z)z^{-4}+E1(z)\ (1-z^{-1})^4$ |

# Chapter 3

# System Architecture

In this chapter, we introduce the detail architecture of this ADC. The introduction includes which circuit we use, how we make the specification, simulation result of all components and how we simplify the circuit to decrease the cost. Due to the low-voltage architecture, comparing to high-voltage design we have to do some changes.

To confirm the accuracy of the architecture, we do the behavior simulation of the $2^{nd}$-order Sigma-Delta modulator by MATLAB. And we also can make the specification of the real circuit by MATLAB. After this simulation, we can design all the components, then using these components to realize a $2^{nd}$-order Sigma-Delta modulator.

The sampling-rate has to down sample to twice bandwidth of input signal and filter the noise in high frequency because of the oversampling and noise shaping technique of Sigma-Delta modulator. We use the low pass filter to avoid aliasing also. The input of the digital decimation filter is 1-bit input. And the bit number depends on the ENOB of the output of Sigma-Delta modulator. In this design, the ENOB is 10-/8-bit for each mode. Normally, the digital part of a Sigma-Delta ADC will cost more than half power and half area of the ADC. The most important issue for designing the digital decimation filter is how to reduce the power consumption and area.

## 3 - 1 Architecture of Sigma-Delta ADC

This ADC is composed of Sigma-Delta modulator, decimation filter, SPI bus and other control units. The block diagram of this ADC is shown in Figure 3-1 and Figure 3-2. The first block is Sigma-Delta modulator which can lower the in-band noise by skills of oversampling and noise shaping. And the decimation filter can filter the noise in high frequency and decimate the sampling frequency to twice of input bandwidth. In the end, the ADC output the data by SPI to DSP beyond this ADC. Then the DSP can analyze the date (bio-electric signal or bio-image signal). And all components of this ADC will be introduced in the back chapters. In this design, $2^{nd}$-order Sigma-Delta modulator is chosen. Due to the small input bandwidth, we choose high OSR not architecture of high order to reach the same resolution.

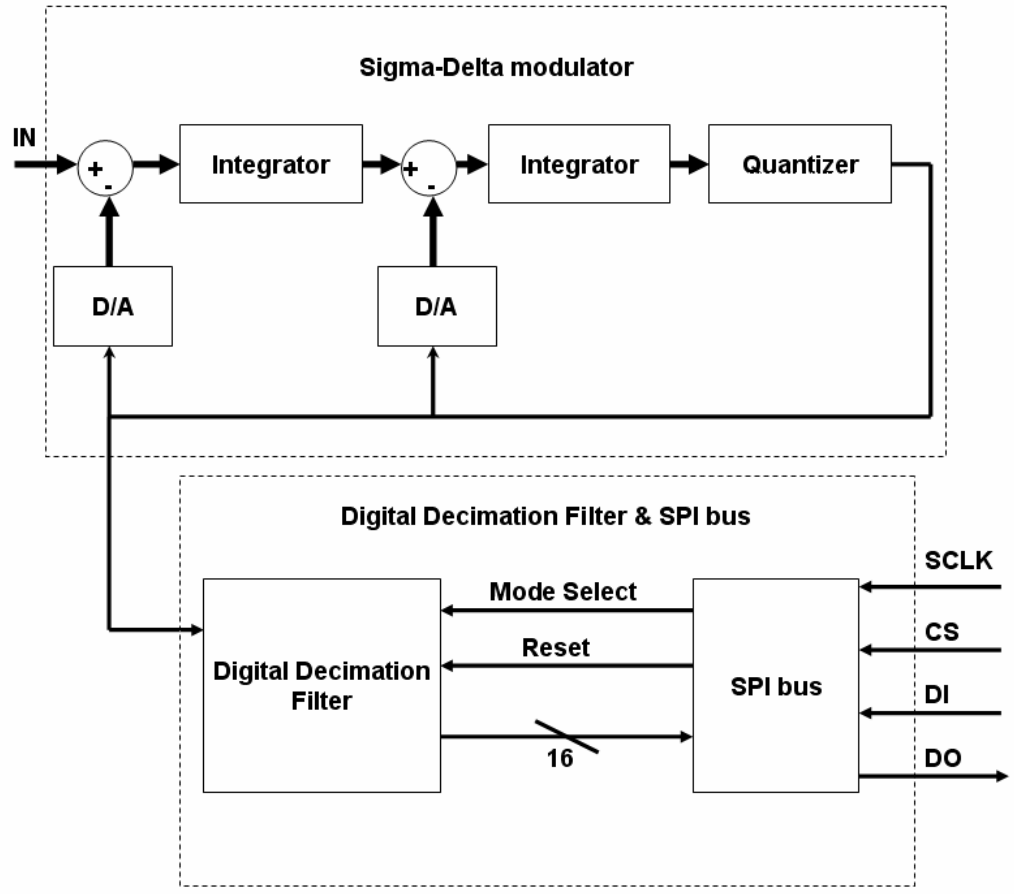



Figure 3 - 1: Block diagram of this Sigma-Delta ADC.

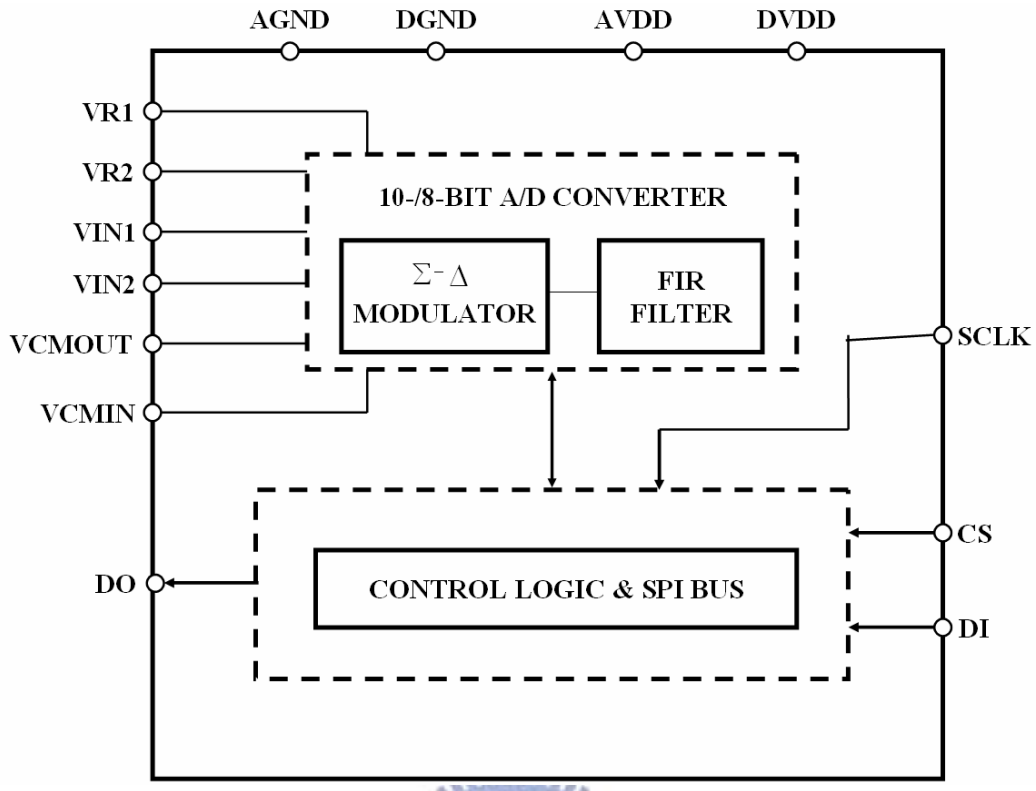



Figure 3 - 2: Block diagram of this Sigma-Delta ADC with all necessary IOs.

## 3 - 2 Behavior Simulation of Sigma-Delta Modulator

Before designing the real circuit, we simulate the function of 2nd-order Sigma-Delta modulator by SIMULINK in MABLAB first.

This ADC is designed for bio-electric signal and bio-image signal both to save the area. So we have to discuss the bandwidth of the two signal to make the sampling frequency. We can see that bandwidth of bio-electric signal is in 1.25 kHz in Figure 3-3. And the bandwidth of bio-image signal is about in 10 kHz.

According to the bandwidth shown up, we make the specification of the ideal 2nd-order Sigma-Delta modulator as Table 3. And we can see that the sampling frequency of the ADC is 640 kHz.

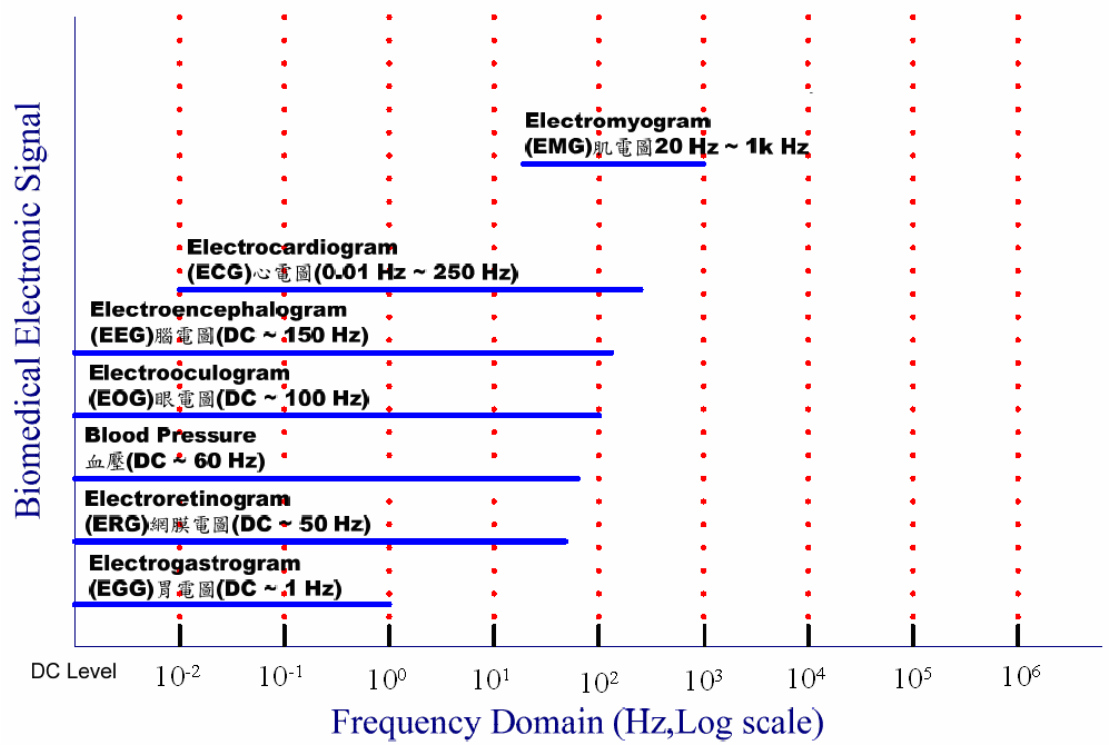



Figure 3 - 3: Bandwidth of bio-electric signals.

Table 3: Specifications of 2nd-order Sigma-Delta modulator

| Signal type | Bandwidth | OSR | Sampling rate |
|---|---|---|---|
| Bio-electric signal | 1.25kHz | 256 | 640kHz |
| Bio-image signal | 10kHz | 32 | |

A block diagram of a 2nd-order Sigma-Delta modulator is shown in Figure 3-4, and we use 1-bit quentizer here. we change the block diagram to signal flow as shown in Figure 3-5, we can calculate the transfer function of X, E and Y (X means the input, Y means the output and E means the quantization error).

The transfer function is shown in below.

$$Y[z] = \frac{a_1 a_2 z^{-2}}{(a_2 b_1 + 1 - b_2) z^{-2} + (b_2 - 2) z^{-1} + 1} X[z] + \frac{(1 - z^{-1})^2}{(a_2 b_1 + 1 - b_2) z^{-2} + (b_2 - 2) z^{-1} + 1} E[z]. \quad (3.1)$$

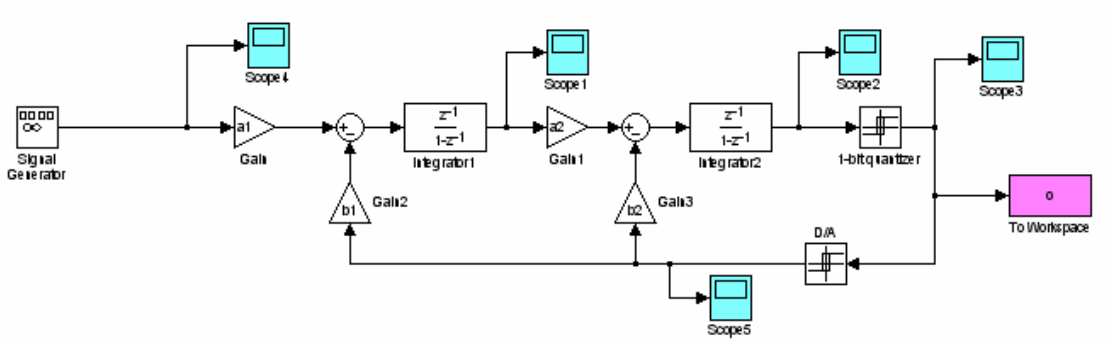



Figure 3 - 4: Block diagram of a 2nd-order Sigma-Delta modulator.

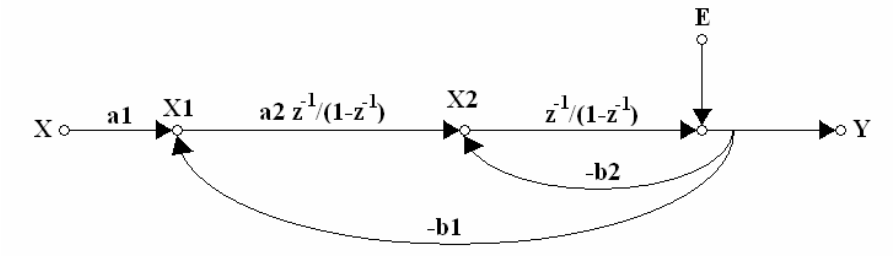



Figure 3 - 5: Flow diagram of 2nd-order Sigma-Delta modulator.

If we let a1 = a2 = b1 = 1 and b2 = 2, then we can simplify Eq. (3.1) as blow:

$$Y[z] = z^{-2}X[x] + (1-z^{-1})^2 E[x] = STF[z]X[z] + NTF[z]E[z]. \qquad (3.2)$$

As upper Eq., we can see that STF is a low-pass filter for input signal, and NTF is a high-pass filter for quantization noise (or white noise). So the operation theorem of Sigma-Delta modulator is keep the signal in input bandwidth, and remove the quantization noise to high frequency from low frequency.

But considering the real situation, the integrator is made by a fully differential opamp, so the output swing will limit to the output swing of fully differential opamp. Especially the first integrator, has the greater effect than the second one. Due to the circuit beyond the second integrator is a 1-bit quantizer which only cares about the output of the second integrator is positive or negative. So the real output of the second

integrator is not so important. We have to adjust the parameter of Eq. (3.2), a1 , a2, b1 and b2 without changing the behavior of the modulator, because of the limit of output swing. We choose a1 = b1 = 0.25, a2=1 and b2=0.5 to make sure that the output swing of the first integrator can be smaller.

As the upper discussing, we make sure the architecture of the 2nd-order Sigma-Delta modulator. Now we discuss the SNDR, ENOB and the output of different stages of the two different modes (bio-electric signal mode and bio-image signal mode).

### 3 - 2 - 1 Simulation in Bio-electric Signal Mode

Bandwidth of bio-electric signal is in 1.25 kHz. To test the function, we input the sine wave of 400 Hz to simulate.

The outputs of four stages is shown in Figure 3-6, when input signal is sine wave of 400 Hz, Vp-p = 0.375 V and 640 kHz sampling frequency.

As shown in Figure 3-6, we can see the output of the Sigma-Delta modulator is a square wave with different width. We change the output to frequency domain by FFT to observe its spectrum which is shown is Figure 3-7. We can get the SNDR is 98.1837 dB, and ENOB is 16-bit in bio-electric signal mode. This spectrum shows that the function of block diagram of modulator is correct. Next we observe the relationship between DR (dynamic range) and SNDR in the same OSR. It's shown in Figure 3-8. It shows the dynamic range is about 100 dB.

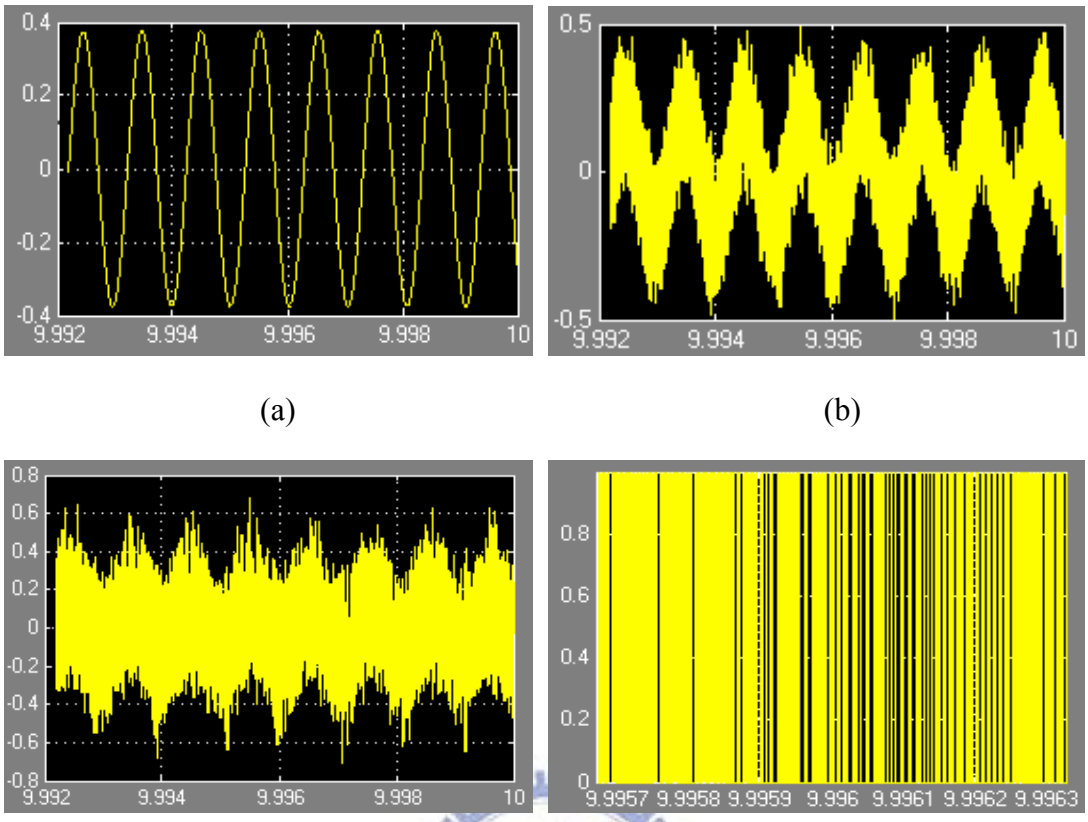



Figure 3 - 6: Waves of four nodes of Sigma-Delta modulator: (a) input (b) output of the first integrator (c) output of the second integrator (d) output of quntizer.

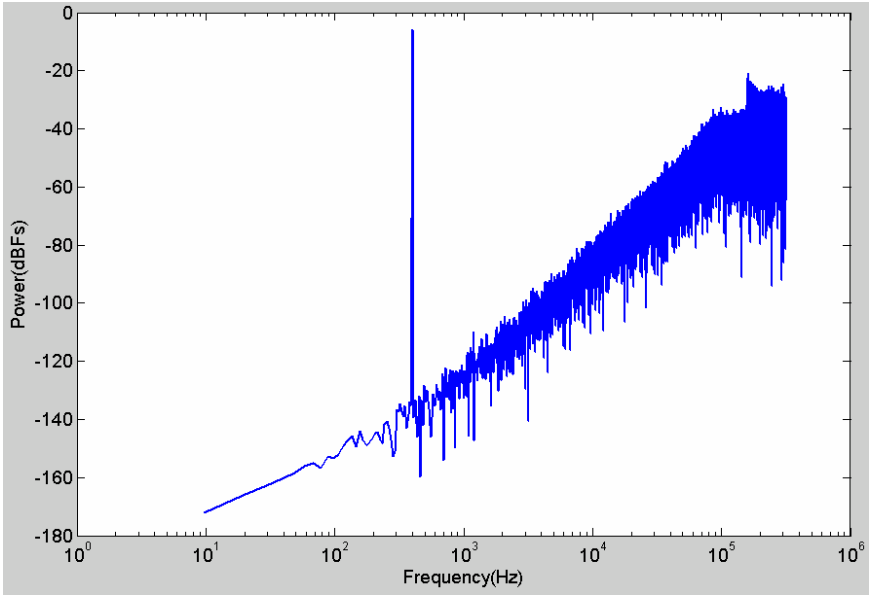



Figure 3 - 7: Spectrum of output in bio-electric signal mode.

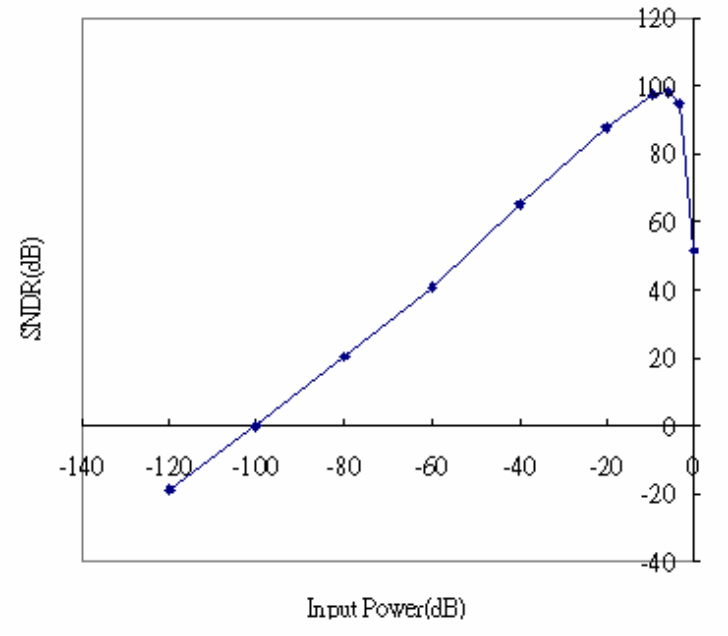



Figure 3 - 8: SNDR versus input lever in bio-electric signal mode.

### 3 - 2 - 2 Simulation in Bio-Image Signal Mode

Bandwidth of bio-image signal is in 10 kHz. To test the resolution of this mode, we input the sine wave of 3.2 kHz to simulate.

The outputs of four stages is shown in Figure 3-9, when input signal is sine wave of 3.2 kHz, Vp-p = 0.375 V and 640 kHz sampling frequency.

As shown in Figure 3-9, we can see the output of the Sigma-Delta modulator is a square wave with different width. We change the output to frequency domain by FFT to observe its spectrum which is shown is Figure 3-10. We can get the SNDR is 54.7919 dB, and ENOB is 9-bit in bio-image signal mode. Next we observe the relationship between DR (dynamic range) and SNDR in the same OSR. It's shown in Figure 3-11. The dynamic range is about 61 dB.

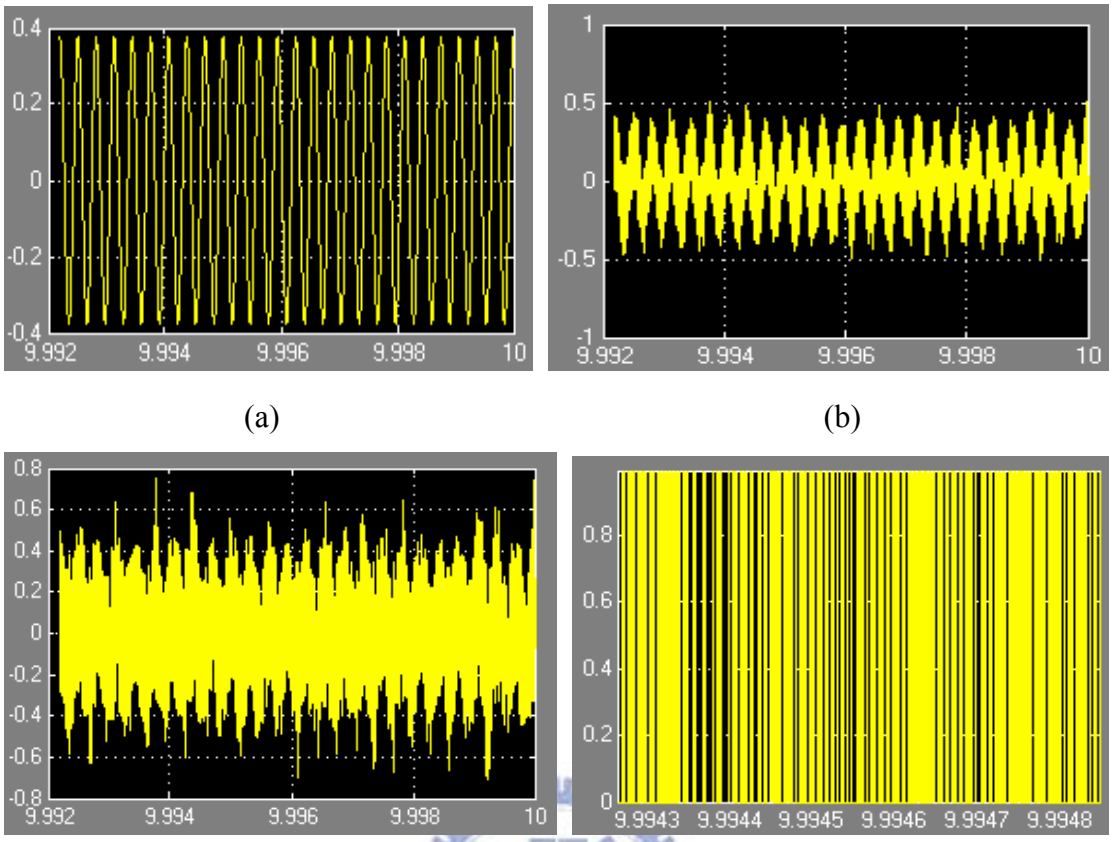



Figure 3 - 9: Waves of four nodes of Sigma-Delta modulator: (a) input (b) output of the first integrator (c) output of the second integrator (d) output of quntizer.

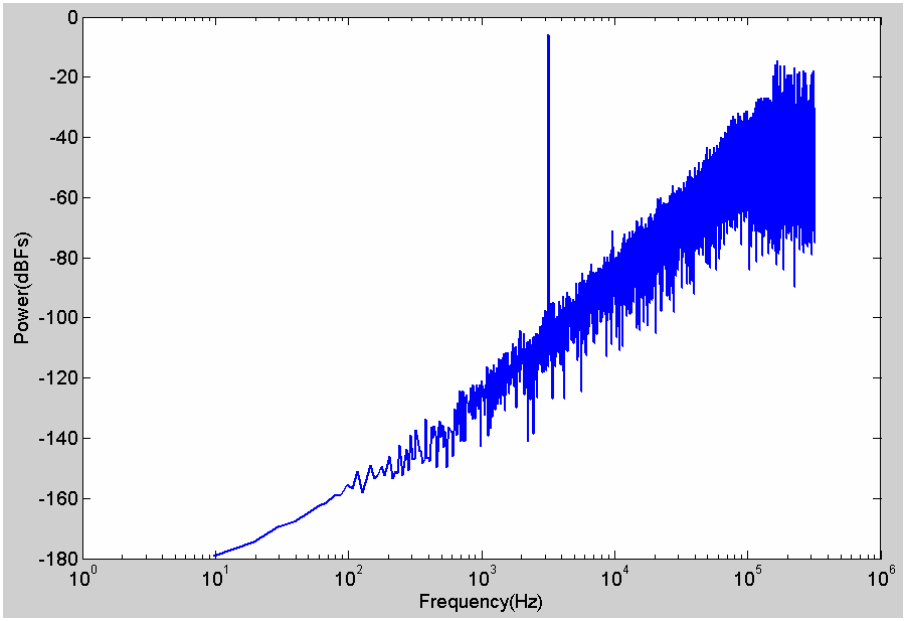



Figure 3 - 10: Spectrum of output in bio-image signal mode.

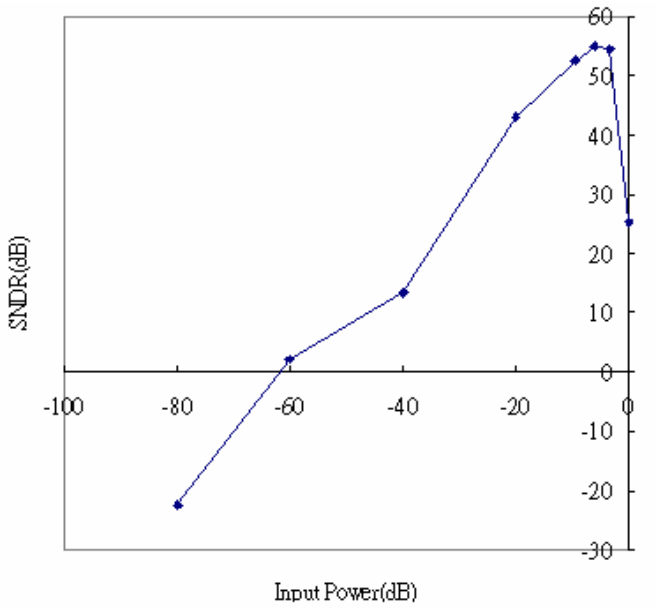



Figure 3 - 11: SNDR versus input level in bio-image signal mode.

As shown above, we can get resolution we need in sampling rate of 640 kHz, no matter the mode we choose is bio-electric signal mode or bio-image signal mode. But that's the ideal situation; in real case, the resolution will be affected under some non-ideal conditions of real circuit. We will introduce the components of the Sigma-Delta modulator, and how we make the specifications of them to let the resolution under acceptable range.

## 3 - 3 Architecture and Design of Sigma-Delta Modulator

The 2nd-order Sigma-Delta modulator desired is composed of clock generator, switch for low voltage supply, comparator and opamp. How we make the specifications of them, and the simulation result are introduced as follows.

### 3 - 3 - 1 Non-overlap Clock Generator

All clock phases of the Sigma-Delta modulator is generated by the clock generator. It's a key point about if the Sigma-Delta can work correctly. It only needs two inverse

phases of clock when we simulate a ideal modulator. But when we design a non-ideal or real modulator, it needs four phases clock which are non-overlapping to control the modulator. As shown in Figure 3-12, it has a time delay between P1 and P1d. It also has a time delay between P2 and P2d. The delay of the non-overlapping phases of clock is to avoid charge injection and clock feedthrough.

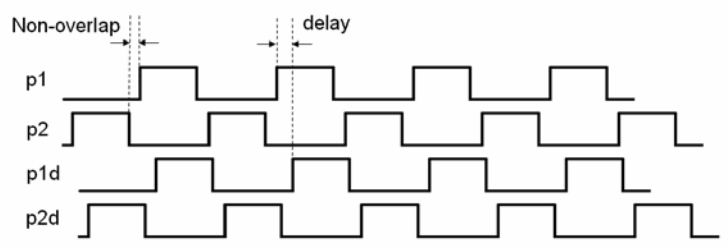



Figure 3 - 12: Four non-overlap clocks.

Clock generator is composed of nor gates, inverters and same delay cells. As shown in Figure 3-13, the delay cells are composed of some inverters to produce different delay times to control the modulator and make sure the modulator can work properly. P1 and P2 are two inverse phases, and P1d and P2d are their delay phases respectively. And the other four phases clock shown in Figure 3-13, are the inverse phases of P1, P2, P1d and P2d.

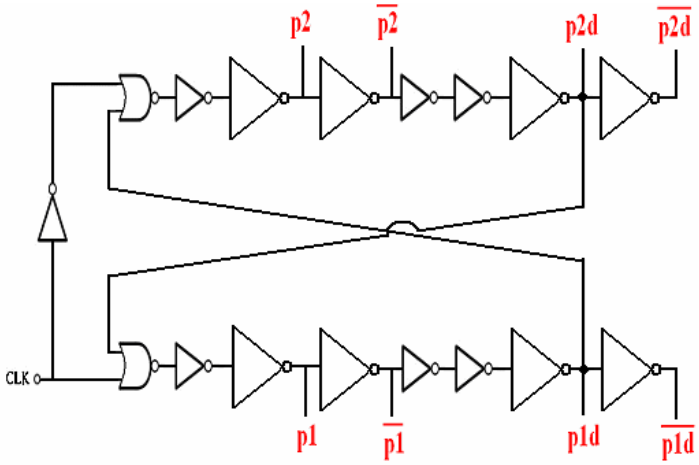



Figure 3 - 13: Circuit of clock generator.

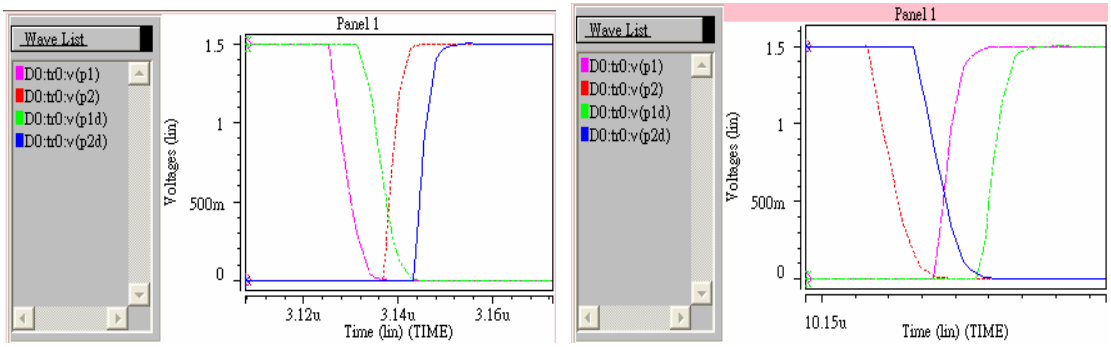
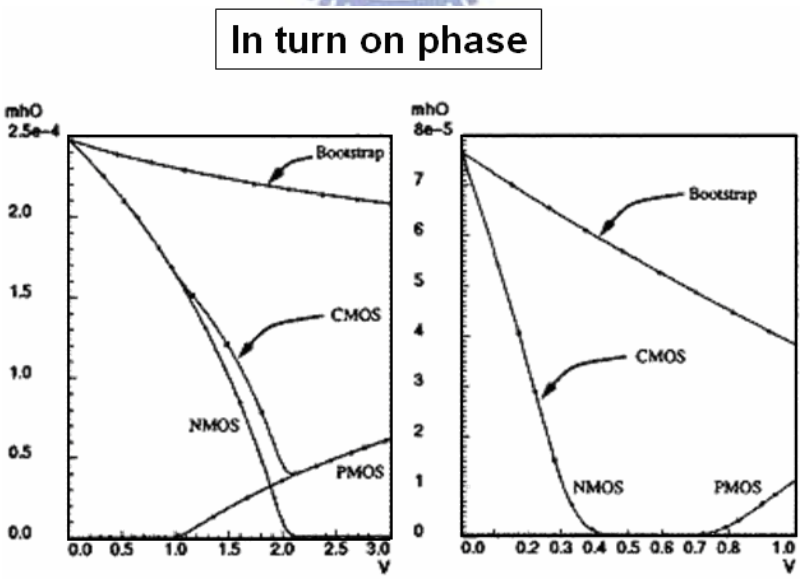



Figure 3 - 14: Simulation result of clock generator.

## 3 - 3 - 2 Bootstrapped Switch

In order to design a low power consumption ADC, we use 1.5 V to be our voltage supply. As shown in Figure 3-15, we can see a problem of that normal mos switch can't be turned on properly in low voltage supply. Differently, bootstrapped switch can work in low voltage supply properly. And the value of Gon of bootstrapped switch is almost the same when different input voltage is supplied. So in this design, some switches are chosen to be bootstrapped switches to carry the right data.




(a) (b)

Figure 3 - 15: Gon of nmos, pmos and bootstrapped switch versus input voltage when (a) VDD=3V (b) VDD=1V.

Illustration of bootstrapped switch as shown in Figure 3-16, additionally, clk and clkb are two inverse clocks. In clkb phase, the capacitor C will be charged to VDD and the switch SW will be turned off; in clk phase, the switch SW will be turned on and the voltage of gate will be about Vin + VDD, because of charging of C in clkb phase. So the switch SW will make sure to be turn on and work well in clk phase.

Some switches in Sigma-Delta modulator will be bootstrapped switches. When the input signal is always low voltage, the switches used will be nmos switches; in other hand, when the input signal is uncertain, the switches used will be bootstrapped switches.

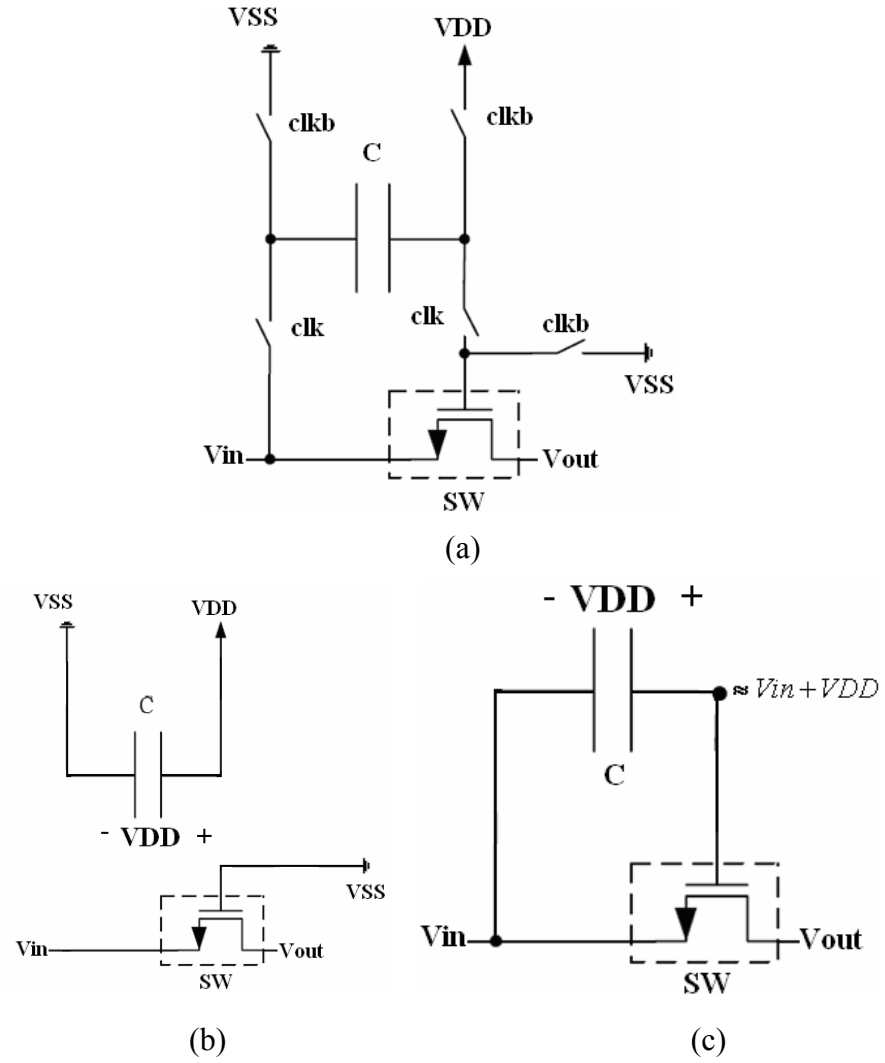



Figure 3 - 16: (a) circuit of bootstrapped switch (b) during clkb phase (c) during clk phase.

In this design, the circuit of bootstrapped switch is shown in Figure 3-17 [1]. MNT5 is added to prevent the gate-drain voltage of MN5 from exceeding VDD while it is off. MP2 and MP4 must be tied to the highest potential, node B. Transistor MN6S triggers MP2 on at the beginning of while transistor MN6 keeps it on as the voltage on node A rises to the input voltage Vin. Gate connections of transistors MN1 and MN6 allow them to be turned on similar to the main switch MNSW.

The simulation result of bootstrapped switch is shown in Figure 3-18. In this case, VDD = 1.5 V and input is sine wave with 0 ~ 1.5 V voltage. No matter what the input voltage is, the output is the same as input voltage in $\Phi_1$ phase.

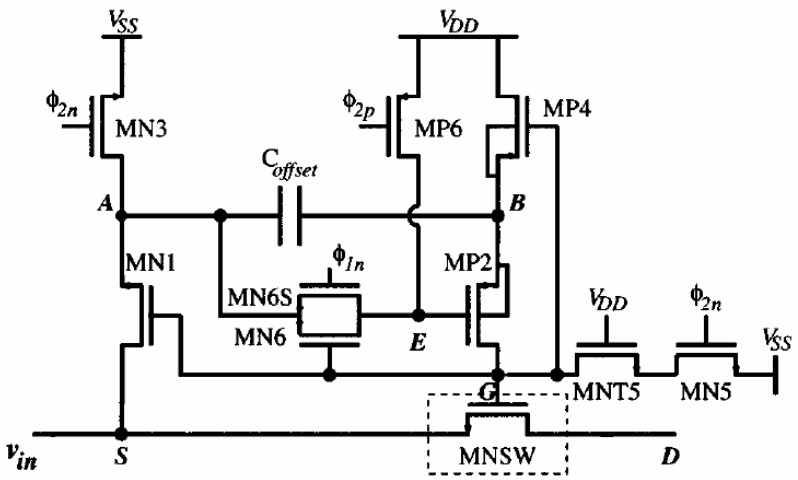



Figure 3 - 17: Transistor level implementation of the bootstrapped switch.

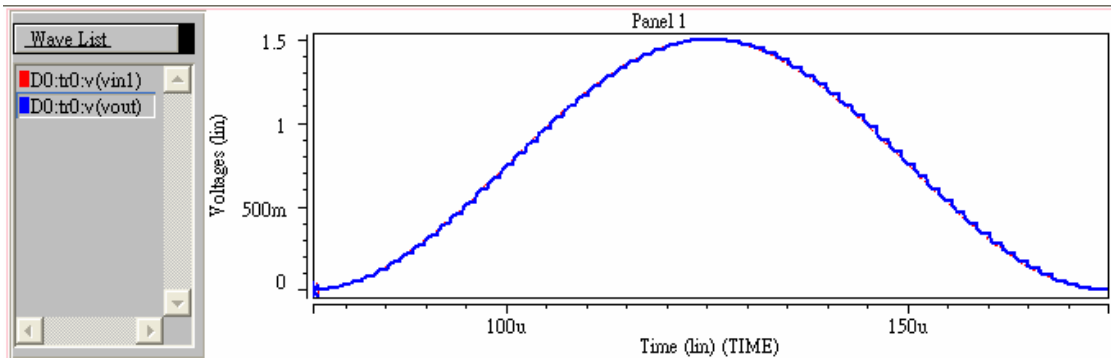
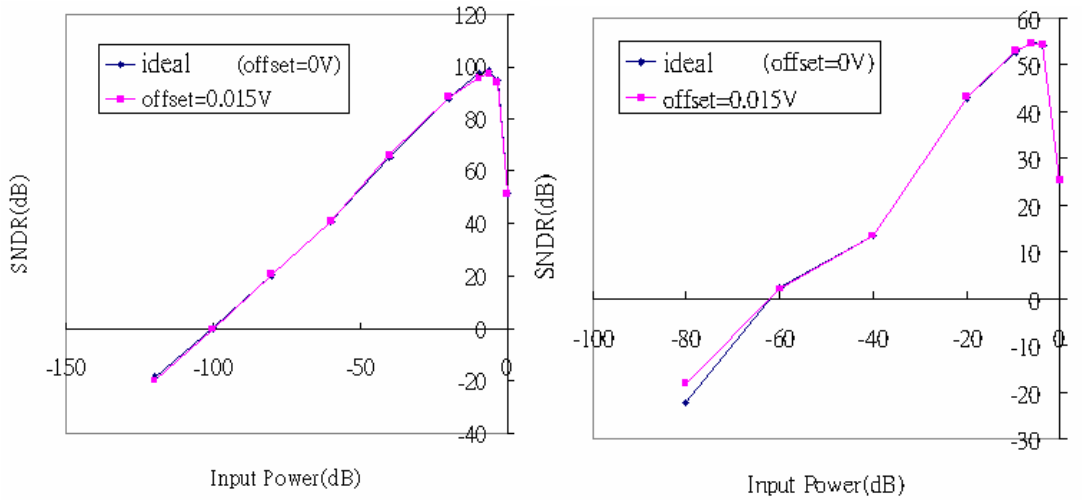



Figure 3 - 18: Simulation result of bootstrapped switch.

### 3 - 3 - 3 Comparator

The SNDR of comparator with offset voltage = 0 V and offset voltage = 15 mV versus input level is shown in Figure 3-19. We can see that when offset voltage is 15mV, the SNDR value is almost the same as the ideal situation. The specification of Sigma-Delta modulator will not be affected by the offset and hysteresis of comparator, because those non-ideal signal will be shaped to high frequency as the quantization noise. Here, we set the offset of comparator to be ± 15mV.




(a) (b)

Figure 3 - 19: The SNDR versus input level (a) in bio-electric mode (b) in bio-image mode when offset voltage is 0V and 15mV.

The circuit of comparator is shown in Figure 3-20. It's a usual comparator circuit. When V(in+) > V(in-), the output Y will be high level (V(Y)=VDD=1.5V); in the other hand, when V(in+) < V(in-), the output Y will be low level (V(Y)=VSS=0V). Additionally, the switch between out+ and out- is bootstrapped switch.

We test the comparator by these three suits of inputs which are V(in+) = (1.5,

0.735, 1.5, 0, 0.765, 0, 0.8, 0.5, 0.765, 0.735, 1.2, 0.3, 0.77, 0.73)V, V(in-) = 0.75V; V(in+) = (1.015, 0.9, 1.03, 0.8, 0.985, 1.2, 0.95, 1.1, 0, 1.015, 0, 1.5, 0.985，1.5)V, V(in-) = 1V; V(in+) = (0.52, 0.4, 0.6, 0.47, 0.6, 0, 0.515, 0, 1.5, 0.485, 1.5, 0.4, 0.52, 0.48)V, V(in-) = 0. 5V. And simulation results of 5 corners are shown in Figure 3-21, additionally, the waves on the top of every figure are the values of (V(in+)-V(in-)) in every simulation. The simulation results tell us that the offset of the comparator is 15mV, and its current consumption is 1.99 uA.

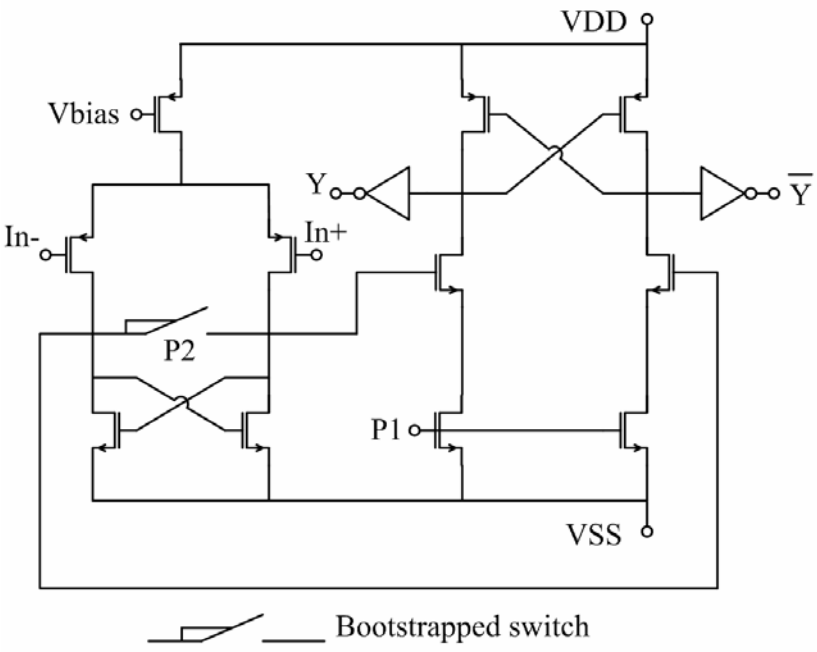
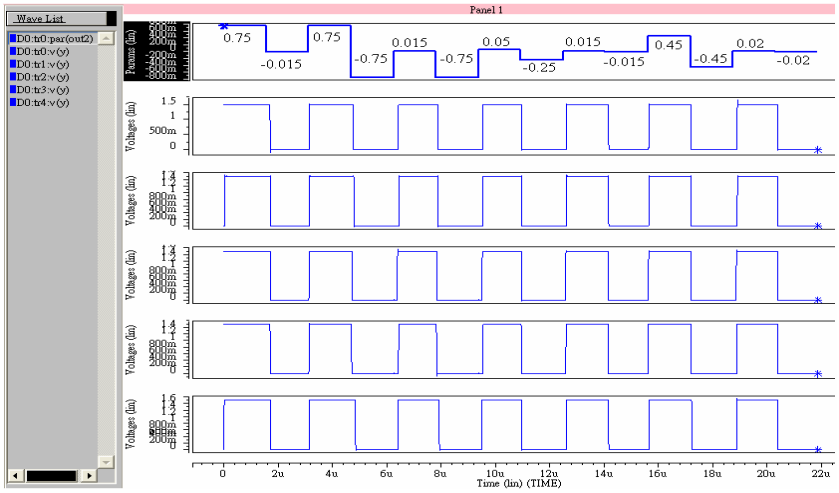
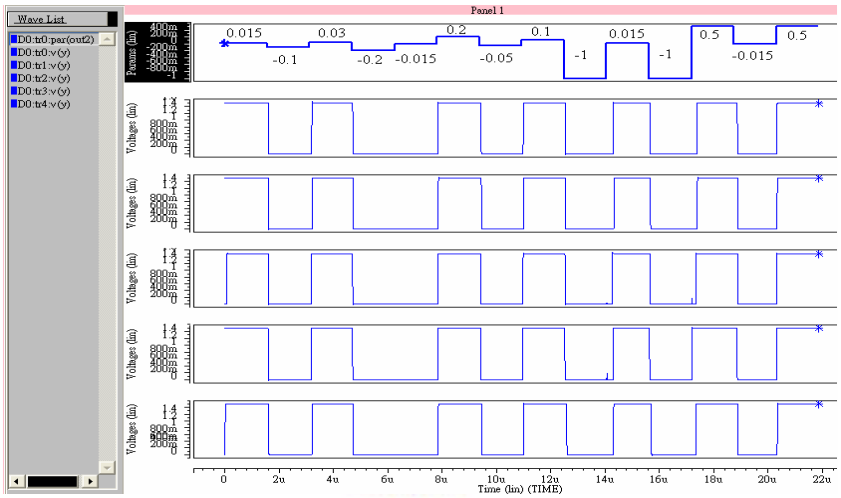


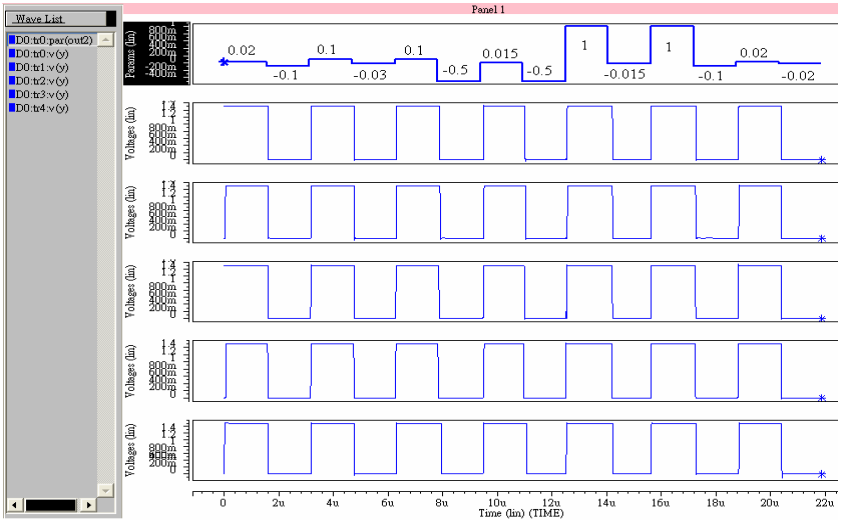

Figure 3 - 20: Circuit of comparator.




(a)




(b)




(c)

Figure 3 - 21: Simulation results of testing of the comparator. (a) first pattern (b) second pattern (c) third pattern.

### 3 - 3 - 4 Operation Amplifier

When we design a operation amplifier (opamp), we have to consider a lot of specifications, as power consumption, output swing, slew rate and DC gain etc.

First, we discuss the issue of output swing by simulink. The biggest output will happen when the input is between 0.75~-0.75 V. In this situation, the output of the first integrator will be between 0.844~-0.844 V. It means that output swing of the opamp is at least 1.688 V (0.844~-0.844 V). The output of the first integrator which is simulated by simulink is shown in Figure 3-22. Due to the circuit beyond the output of the second integrator is a comparator, the output swing of the second integrator is not so important. It only has to consider if the output of the second integrator is bigger or smaller than 0.

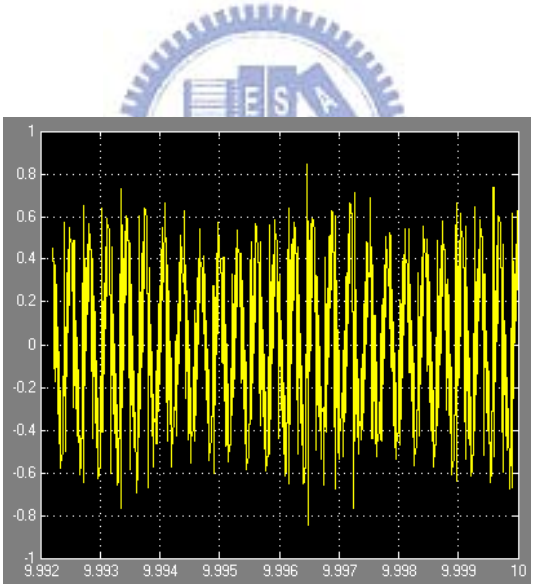



Figure 3 - 22: the output of the first integrator which is simulated by simulink.

Next we consider the issue of slew rate. The variation of the output of opamp in half of clock cycle (1/(640000*2)s) will not be over 1.5 V. And we hope the output can rise to 1.5 V in 1/10 of clock cycle, so we get

$$\frac{1.5}{\frac{1}{640000}*\frac{1}{2}*\frac{1}{5}}=9.6(V/us)\,. \qquad (3.3)$$

In this design, we set the slew rate of the opamp has to be bigger than 9.6 V/us.

Then we talk about the dc gain. A normal integrator is shown in Figure 3-23. In this case, switches S1 and S3 are controlled by the same phase clock1; in the other hand, switches S2 and S4 are controlled by the same phase clock2 which is non-overlapping with clock1.

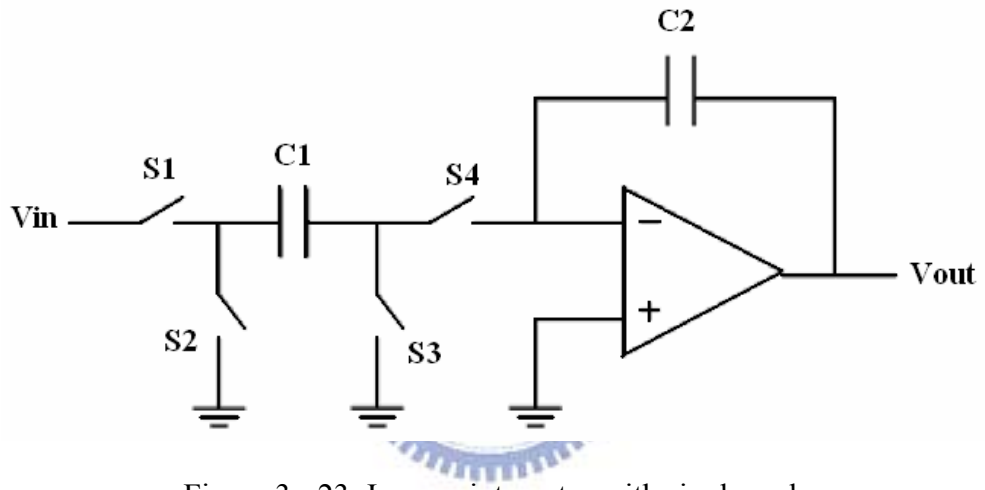
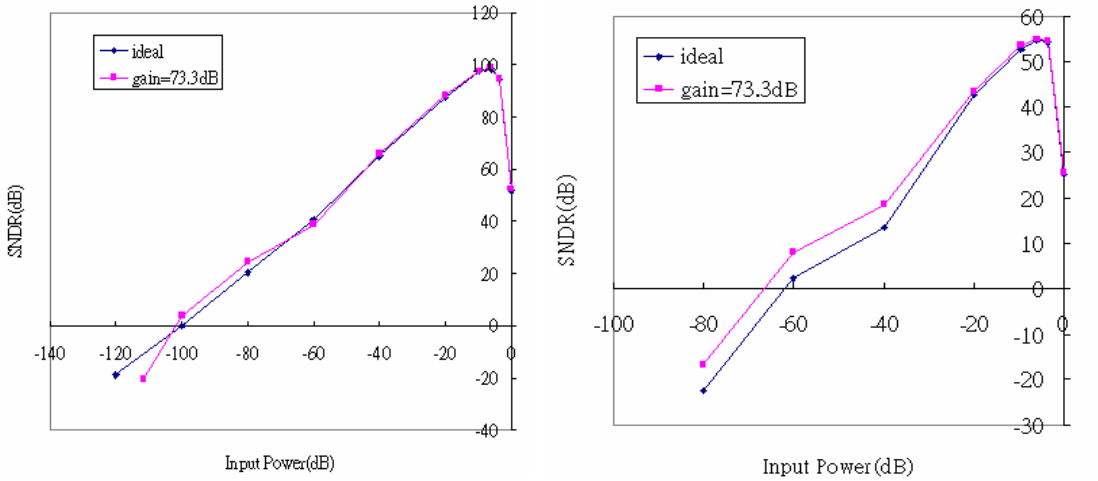



Figure 3 - 23: Inverse integrator with single end.

We can get the function of this integrator shown in Figure 3-23:

$$\frac{Vout[z]}{Vin[z]}=\frac{C_1}{C_2}z^{-1}\frac{\frac{Av}{Av+1+C_1/C_2}}{1-\frac{Av}{Av+1+C_1/C_2}z^{-1}}\cong\frac{C_1}{C_2}\frac{z^{-1}}{1-(1-\frac{C_1/C_2}{Av})z^{-1}}\,. \qquad (3.4)$$

There is error coefficient $e=\frac{C_1/C_2}{Av}$ in Eq. (3.4). a1 and a2 are 0.25 and 1 respective, so the biggest C1/C2 is 1. The SNDR with infinite gain and gain of 73.3dB versus input level is shown in Figure 3-24. When dc gain of opamp is 73.3dB, the error coefficient e will be $2.16\times10^{-4}$. In Figure 3-24, we can see that the SNDR won't be worse when the dc gain of opamp is 73.3dB.




(a) (b)

Figure 3 - 24: The SNDR with infinite dc gain and gain of 73.3 db versus input level. (a) in bio-electric signal mode (b) in bio-image signal mode.

Considering the low voltage supply, we choose a circuit of opamp which applies to low voltage supply. The circuit of the opamp is shown in Figure 3-25. It is a two stage opamp with some variations in the load of differential pair to let the opamp suit for low voltage supply. And we add two compensated capacitors to compensate the bandwidth and phase margin of this opamp.

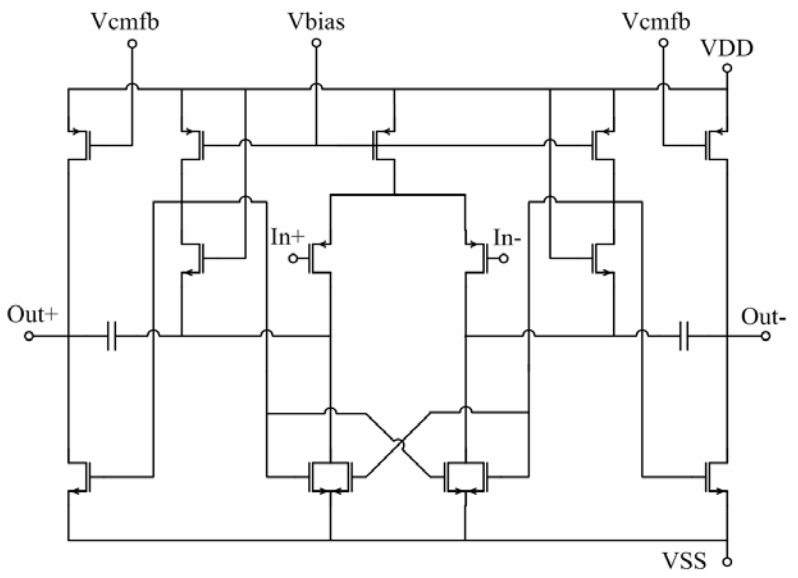



Figure 3 - 25: Circuit of opamp.

The frequency response of the opamp is shown in Figure 3-26. When temperature is $25°C$ and VDD is 1.5 V, the DC gain of the opamp is 81 dB, unit-gain bandwidth is 11.5 MHz, current consumption is 320.5 uA, phase margin is $65^{\circ}$ and the gain is above 60 dB between 0 Hz ~ 10 kHz.

We simulate the opamp in voltage supply of 1.5V±10% (1.35 V ~ 1.65 V) and temperature of $0^{\circ}C \sim 90^{\circ}C$ to make sure that the opamp can work well in different situations. The simulation result is shown in Figure 3-27, it has DC gain 73.3 dB, unit-gain bandwidth 11.5 MHz, phase margin is $65^{\circ}$ and the gain is above 60 dB between 0 Hz ~ 10 kHz.

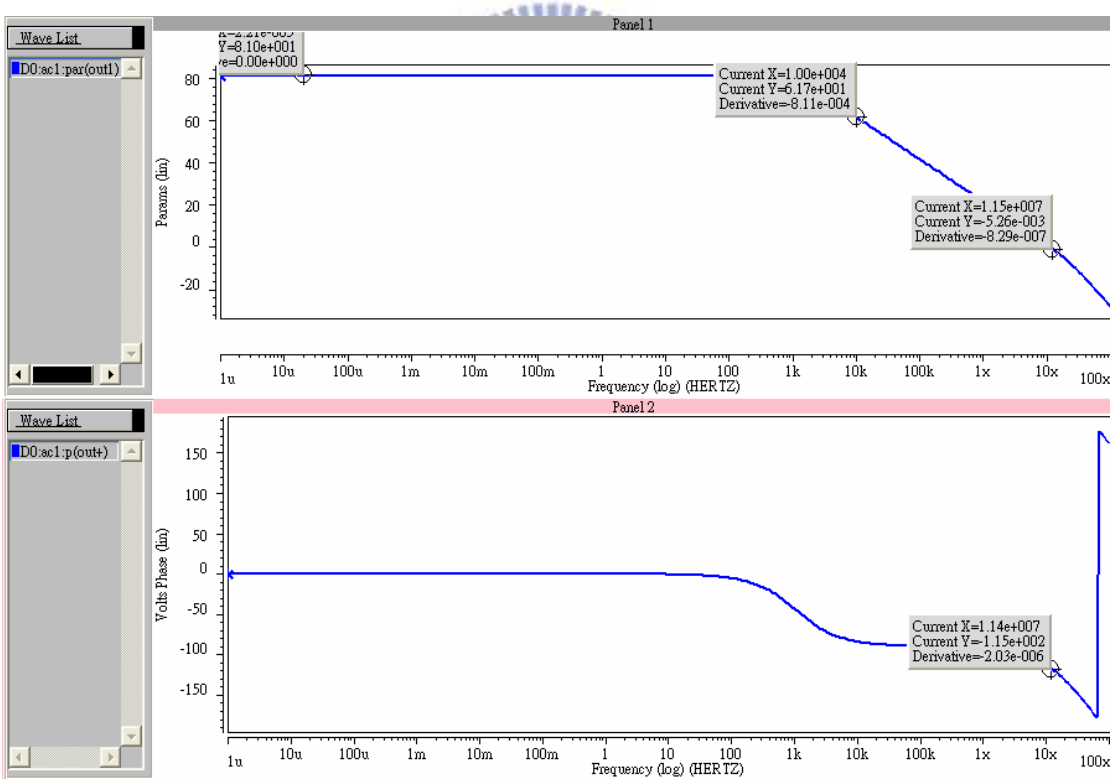



Figure 3 - 26: Frequency response of opamp.

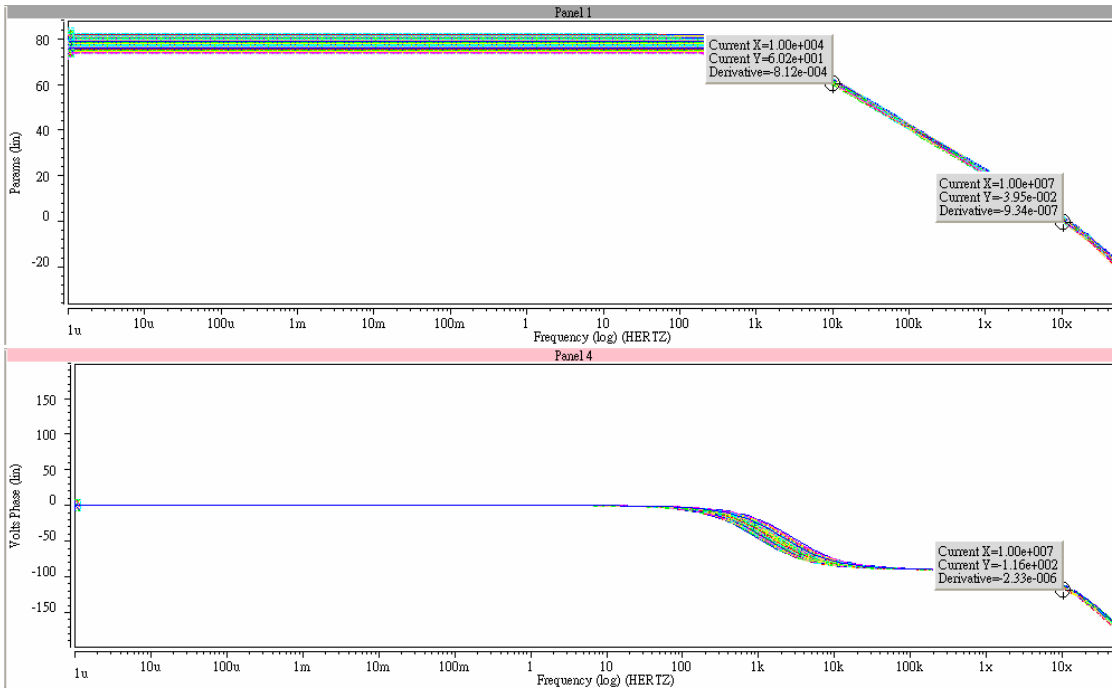



Figure 3 - 27: Frequency responses of opamp when voltage supply is 1.5V ±10% (1.35 V ~ 1.65 V) and temperature is $0^{\circ}C \sim 90^{\circ}C$.

To test the output swing and slew rate of the opamp, we connect the circuit as shown in Figure 3-28. In this case, R1=100kΩ, R2=112.6kΩ, Vid=(Vi+)-(Vi-) and Vout=(Vout+)-(Vout-). Let Vid be a sine wave with 1.5 V and 20 kHz to test if the output swing is sine wave with 1.688 V. Figure 3-29 shown us that output swing of the opamp has at least 1.688 V. And the output wave at the beginning is not stable because the operation of CMFB is still on the unstable state. We change the Vid to a square wave to test the slew rate of the opamp. The result is shown in Figure 3-30. The slew rate is 10.2 V/us. The detailed specifications of opamp and comparator are shown in Table 4.

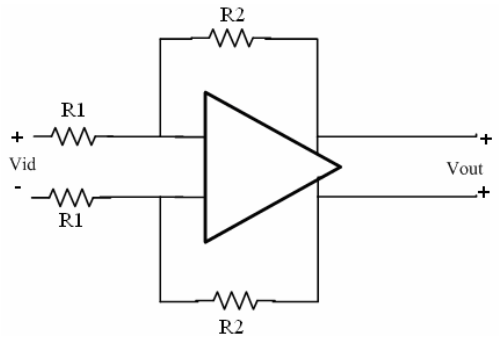



Figure 3 - 28: Testing circuit.

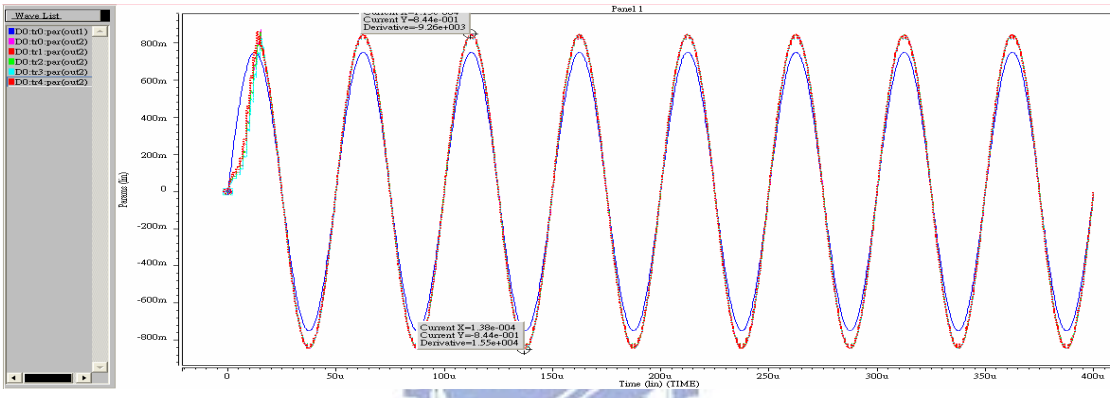



Figure 3 - 29: Output of testing circuit when Vid is a 20 kHz sine wave with 1.5 V Vp-p.

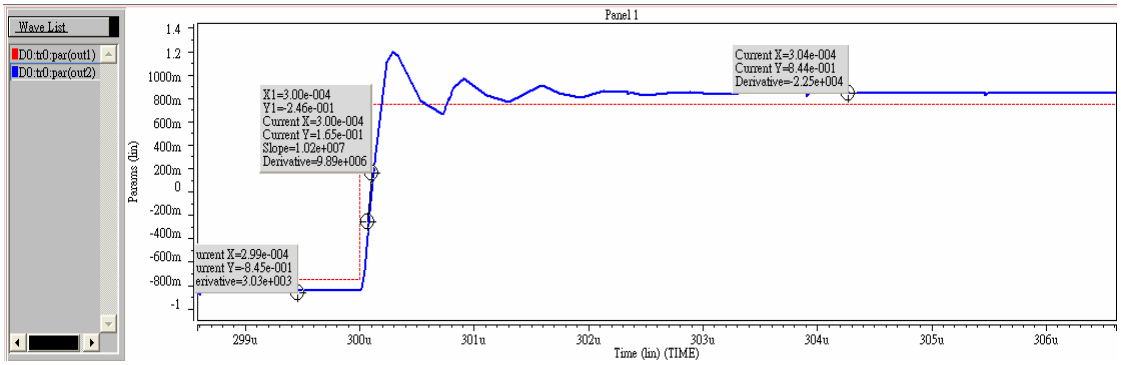



Figure 3 - 30: Output of testing circuit when Vid is a square wave.

Table 4: The specifications of opamp and comparator.

| | | |
|---|---|---|
| **Opamp** | Voltage supply | 1.5V±10% |
| | DC gain | 81dB |
| | Slew Rate | 10.2V/us |
| | Output swing | 1.688V |
| | unity gain bandwidth | 11.5MHz |
| | Temperature | 0°C ~ 90°C |
| | Current Consumption | 320.5uA |
| | Phase Margin | 65° |
| **Comparator** | Offset | ±15mV |
| | Current Consumption | 1.99uA |

## 3 - 4 2nd-Order Sigma-Delta Modulator

We realize the 2nd-order Sigma-Delta modulator by the components introduced above. The simulation result will be discussed as follows.

As the architecture shown in Figure 3-4 by simulink, we can design the Sigma-Delta modulator. The whole circuit of the modulator is shown in Figure 3-31. Due to using the low voltage supply, some switches are bootstrapped switches introduced above. To avoid the area of the chip will become bigger, we use two common-mode voltage in this design, here, one is Vcmout, the other one is Vcmin. In the input of the second integrator we use Vcmout which is equal to VDD/2. And We use Vcmin which is equal to 0 V to implement other ground. So the switches connect with Vcmin can be nmos switch to transit the signal. The use of Vcmout and Vcmin is introduced in [1] particularly.

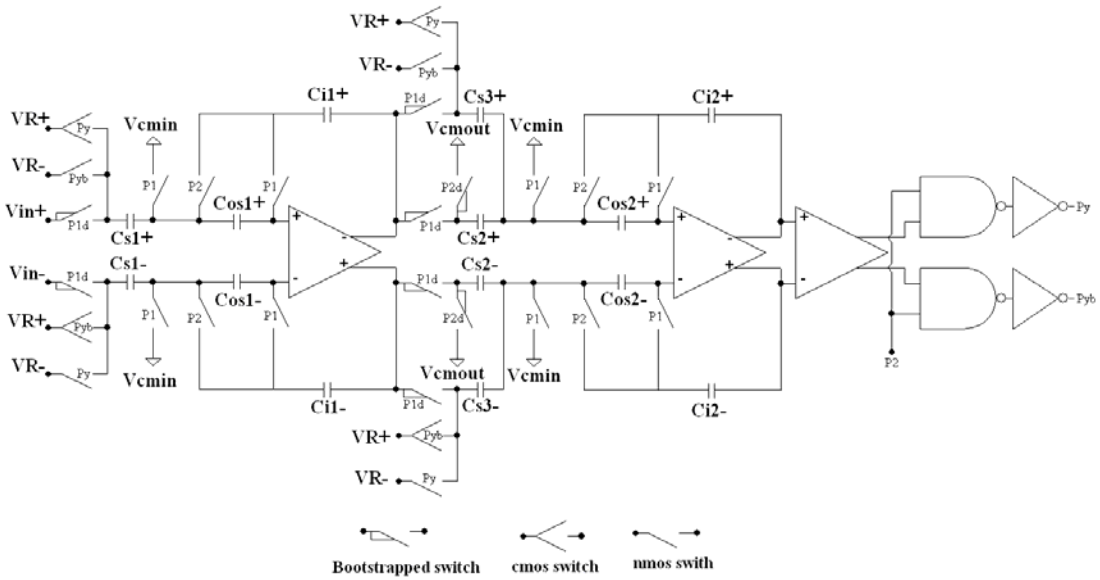


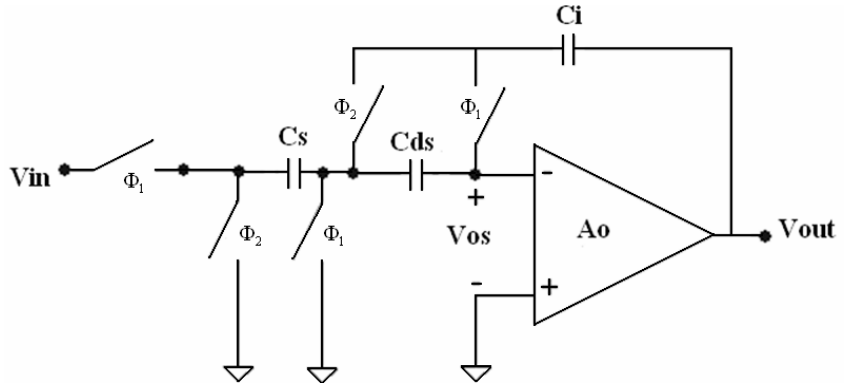

Figure 3 - 31: Circuit of the 2nd-order Sigma-Delta modulator.

Inverse integrator is used in this design. To eliminate the offset, 1/f noise and finite dc gain, the CDS (Correlated Double Sampling) technique [6] as shown in Figure 3-32 is used. The CDS technique is used widely to realize the S/H and integrator of high resolution.

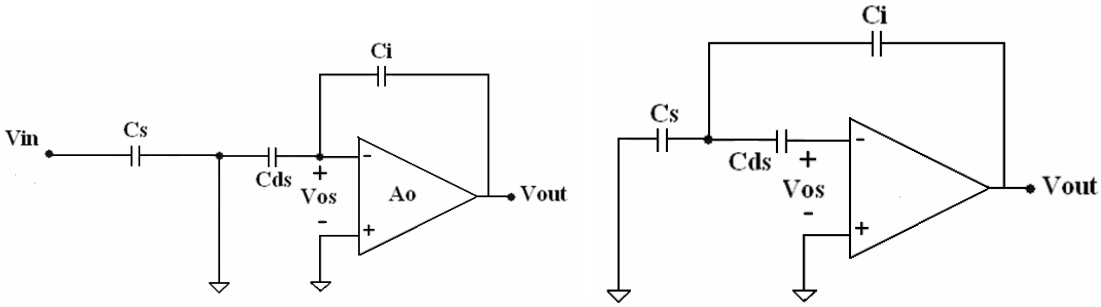
Adding a fitting $C_{ds}$ in the integrator is shown in Figure 3-32. When in $\Phi_1$ phase, the $C_{ds}$ stores the offset voltage of opamp; when in $\Phi_2$ phase the offset voltage of opamp will be eliminated by the charge stored in $C_{ds}$ at last half cycle. We can express that operation as Eq. (3.5).

$$V_o(z) = V_n - z^{-\frac{1}{2}} V_n . \qquad (3.5)$$

Then the resolution of the integrator will be increase by eliminating the low frequency noise of opamp by high pass filter as shown in Eq. (3.5).




(a)




(b) (c)

Figure 3 - 32: (a) CDS (Correlated Double Sampling) integrator (b) in $\Phi_1$ phase (c) in $\Phi_2$ phase.

We realize the 2nd-order Sigma-Delta modulator with differential ended as shown in Figure 3-31, then it has such advantages as follows:

1. To depress the even order distortion to lower whole distortion.
2. To improve the sampling noise to increase the resolution of the modulator.
3. Output swing increase two times.

The simulation result of the 2nd-order Sigma-Delta modulator is shown in Figure 3-33. The result tells us that ENOB is 10.44-bit in bio-electric signal mode and ENOB is 8.18-bit in bio-image signal mode. But we can see the noise in low frequency is increase, the reason will be discussed as follows:

1. The low voltage supply expresses amplitude of the input swing, relatively,

amplitude of the noise isn't change, then the SNR is decrease.

2. Noise in low frequency is affected by thermal noise and flicker noise.

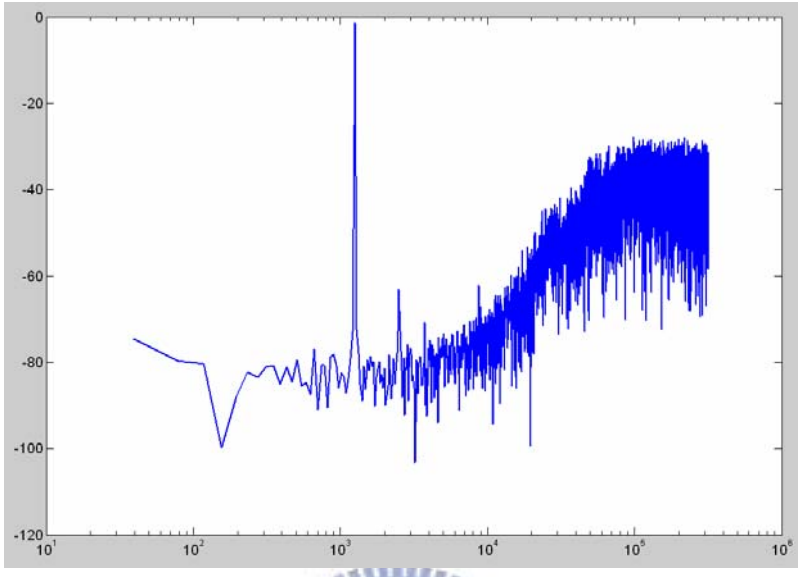



Figure 3 - 33: The simulation result of 2nd-order Sigma-Delta modulator.

## 3 - 5 Design of Digital Decimation Filters

This ADC which has two modes with the same Sigma-Delta modulator is what we desire. The OSR for bio-electric signal mode is 256 and the OSR for bio-image signal mode is 32. To design a Sigma-Delta ADC suits the conditions of OSR, the architecture of the digital decimation filter is shown in Figure 3-34.

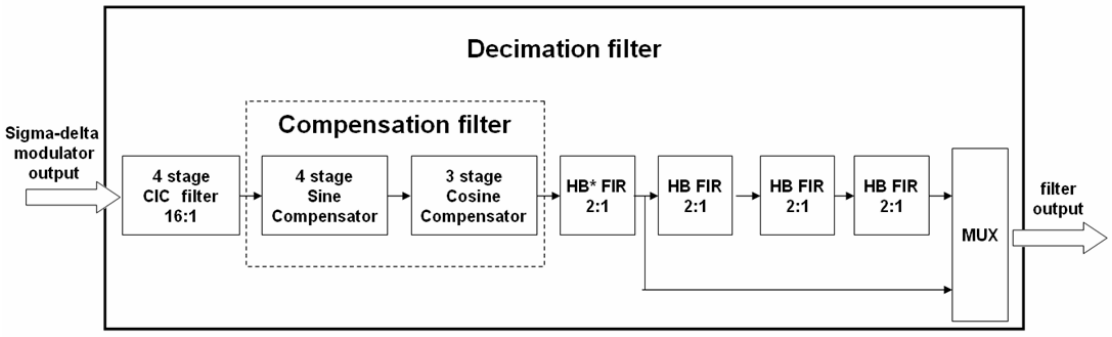



Figure 3 - 34: Architecture of digital decimation filter.

The 2-to-1 multiplexer which is the last stage of decimation filter is controlled by the mode-select. As shown in Figure 3-34, the first filter which is realized by comb filter decimates 16 times. And the compensation filter is used to compensate the narrow pass-band of comb filter. Subsequently, there are four stages half-band filter which decimates 2 times. The specifications and design considerations is introduced as follows.

### 3 - 5 - 1 Low Power Design of CIC Filter

The first stage of decimation filter is a $16^{th}$-order CIC filter. The Z-transform of the CIC filter is shown is Eq. (3.6). Here, we use four stages CIC filters to realize the first stage of decimation filter in this design.

$$H_{CIC}[z] = \frac{1}{16}\frac{1-z^{-16}}{1-z^{-1}}. \quad (3.6)$$

There are some advantages of using CIC filter as follows:

1. The area and power consumption of the ADC will be reduced. We use higher order CIC filter to decimate the sampling rate, so number of FIR filter which needs more multipliers and adders can be reduced effectively. And the operation of multiplier will be reduced to adders and delay cells. Then the area and power consumption will be smaller.
2. No quantization error. The parameters of CIC filter are integer, so we don't have to simplify the parameter. So there is no quantization error when we design CIC filter.

The narrow pass-band of CIC filter will be a problem in this design. It weakens

the in-band signal. So we add a compensation filter beyond the CIC filter to compensate the narrow pass-band. Here, the Sine compensator is chosen to compensate that problem. The Z-transform of Sine compensator is shown in Eq. (3.7). To solve the problem properly, we use four stages Sine compensator to compensate the narrow pass-band of CIC filter.

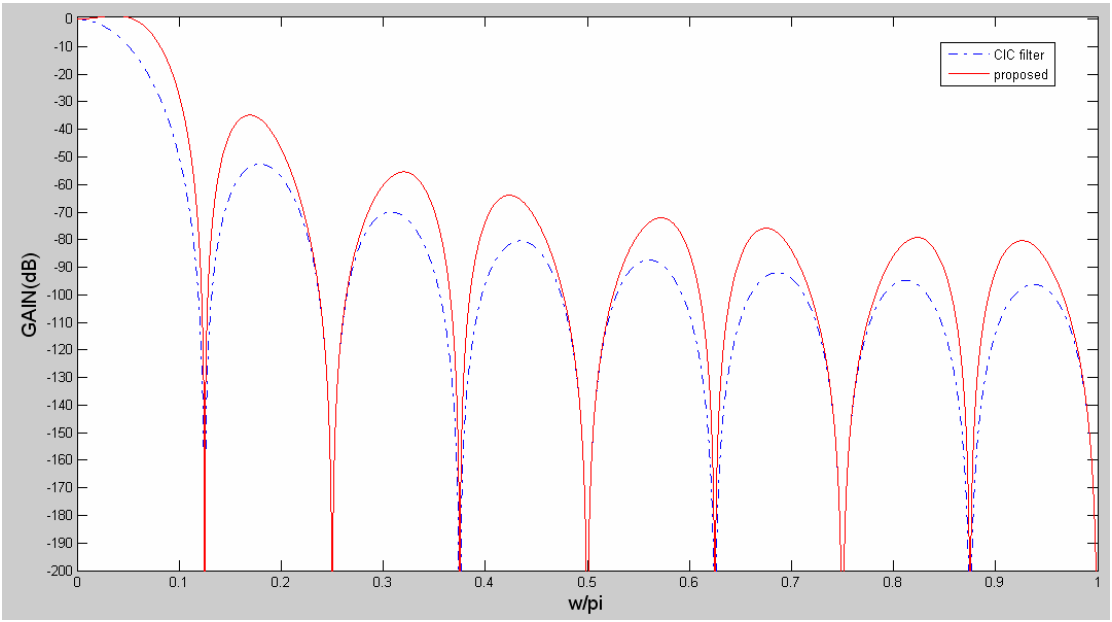
$$H_{SIN}[z] = \frac{1}{4}[-1 + 6z^{-8} - z^{-16}]. \quad (3.7)$$

The spectrum of the original CIC filter versus the spectrum of CIC filter compensated by Sine filter is shown Figure 3-35 (a). It shows the improvement of the narrow pass-band, furthermore, it shows that the attenuation of stop-band becomes smaller. That new problem will make the aliasing become critical. So it needs another compensator to compensate the small attenuation to avoid aliasing.

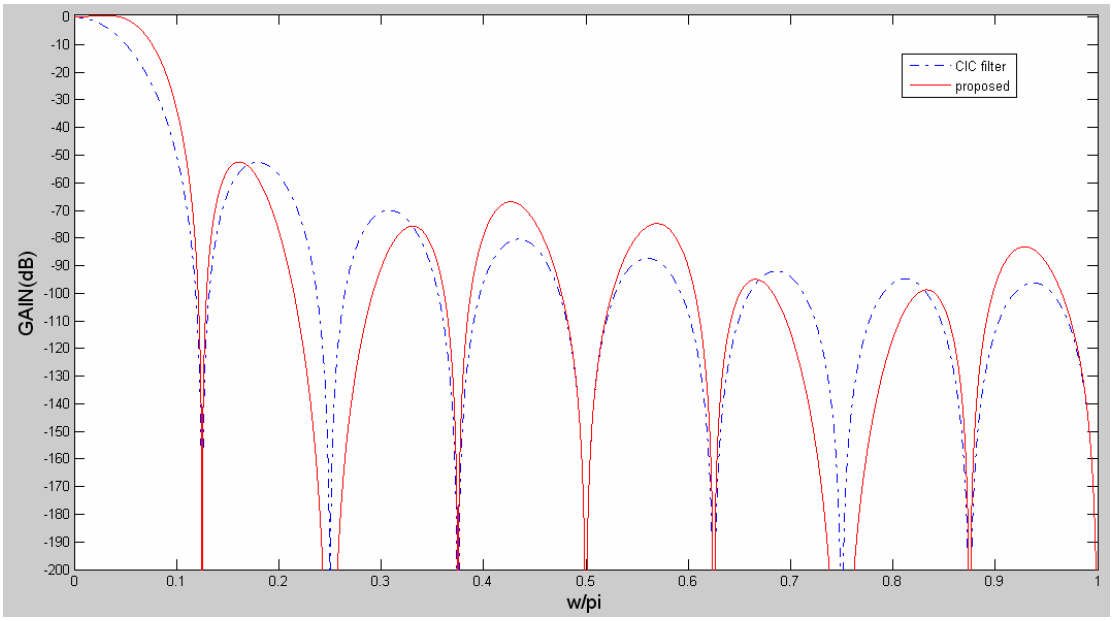
Cosine filter is used to compensate the problem of small attenuation. Z-transform of Cosine filter is shown as Eq. (3.8). Three stages Cosine filters are used to reach the specification of the decimation filter.

$$H_{COS}[z] = \frac{1}{2}(1 + z^{-4}). \quad (3.8)$$

Figure 3-35 (b) shown below is the spectrum of original CIC filter versus the spectrum of CIC filter compensated by Sine filter and Cosine filter. We can see that the pass-band is flat and the attenuation of stop-band doesn't decrease. So we compensate the CIC filter by Sine filter and Cosine filter and solve the problems of pass-band and stop-band successfully.




(a)




(b)

Figure 3 - 35: the spectrum of original CIC filter versus the spectrum of CIC filter compensated by (a) Sine filter (b) Sine filter and Cosine filter.

As above, we can write the Eq. of CIC filter as Eq. (3.9).

$$\left(\frac{1-z^{-16}}{1-z^{-1}}\right)^4 = \left(a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} + a_4 z^{-4} + a_5 z^{-5} + a_6 z^{-6} + \ldots + a_{58} z^{-58} + a_{59} z^{-59} + a_{60} z^{-60}\right) \quad (3.9)$$

The matrix of the parameters of this CIC filter is [a0 a1 a2 a3 a4 a5 a6 … a58 a59 a60]=[1 4 10 20 35 56 84 120 165 220 286 364 455 560 680 816 965 1124 1290 1460 1631 1800 1964 2120 2265 2396 2510 2604 2675 2720 2736 2720 2675 2604 2510 2396 2265 2120 1964 1800 1631 1460 1290 1124 965 816 680 560 455 364 286 220 165 120 84 56 35 20 10 4 1], additionally, $a_n$ means the parameter of $z^{-n}$. Its cost a lot of operations if we design the CIC filter directly. If the parameters can be arranged properly, the power consumption and area can be reduced greatly.

Here, we use two ways to reduce the operations of CIC filter. The first way is that we can distribute some parameters into a group. For example, we can distribute parameters, a0, a1, a2 and a15, and we can get the result as follow.

$$\begin{aligned} &a_0x(n)+a_1x(n-1)+a_2(n-2)+a_{15}x(n-15)= \\ &x(n)+4x(n-1)+10x(n-2)+816x(n-15)= \\ &2^0x(n)+2^2x(n-1)+2^1x(n-2)+2^3x(n-2)+2^4x(n-15)+ \\ &2^5x(n-15)+2^8x(n-15)+2^9x(n-15) \end{aligned} \quad (3.10)$$

As shown in Eq. (3.10), there are 2 to the power of 0, 1, 2, 3, 4, 5, 8 and 9 ($2^0$, $2^2$, $2^1$, $2^3$, $2^4$, $2^5$, $2^8$ and $2^9$). Those binary parameters can be combined into a 10-bit register. Originally, the operation needs three adders of 10-bit and four registers to save the four parameters. Now, it only needs one 10-bit register. The architecture of this example is shown in Figure 3-36.

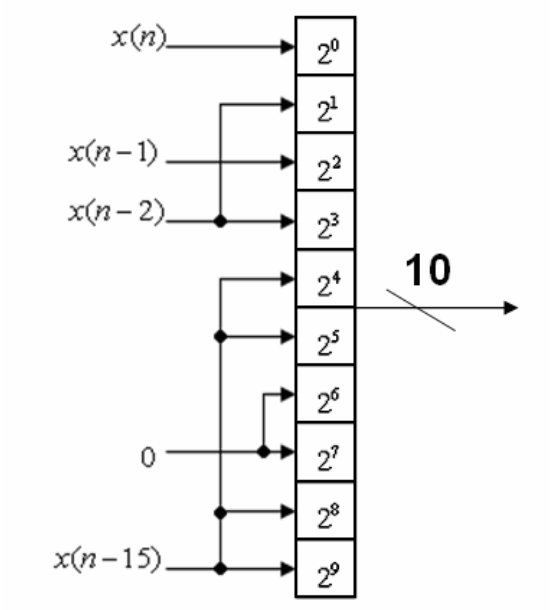



Figure 3 - 36: The simplified architecture:

$$a_0x(n)+a_1x(n-1)+a_2(n-2)+a_{15}x(n-15).$$

We can observe 17 suits of this kind of parameters which can be combined into a register. They are (a0, a1, a2, a15), (a3, a14), (a4, a9), (a12, a5), (a6, a18, a29), (a8, a21), (a13, a26), (a19, a23), (a60, a59, a58, a45), (a57, a46), (a51, a56), (a48, a55), (a31, a42, a54), (a39, a52), (a34, a47), (a41, a37) and (a30). The architectures of them are shown in Figure 3-37.

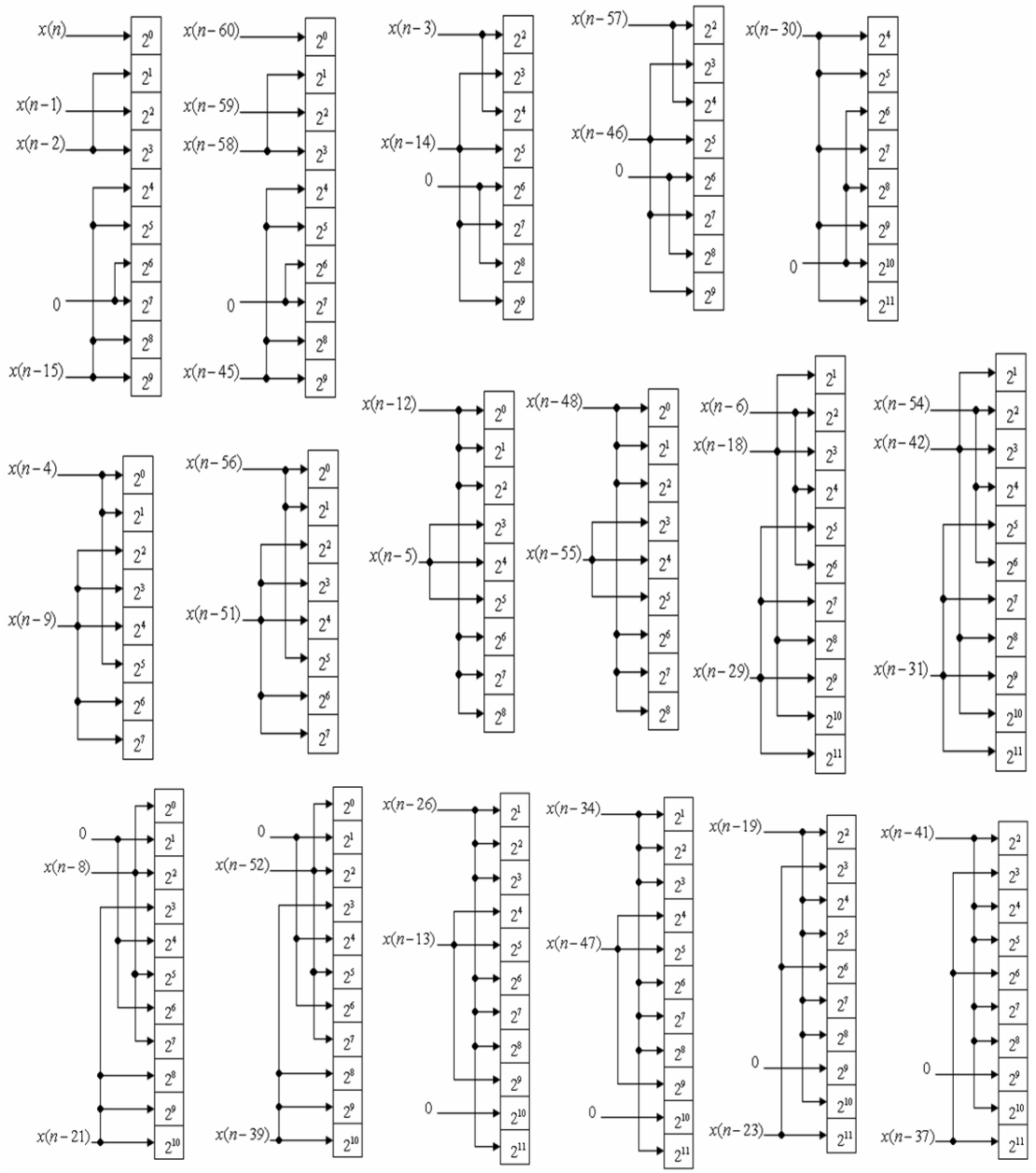



Figure 3 - 37: The 17 registers after simplifying operations.

Except those parameters which can be combined into a register, we have to find a way to simplify other parameters. Here, we introduce the second way to fix those parameters. It must exists a parameter which we can find another parameter is just the same as. For example, a11 and a49, $a11 = a49 = (364)_{10} = (101101100)_2$. We arrange them in the Table 5, additionally, $b_n$ means the n-bit of the sum of $a_{11}x(n-11) + a_{49}x(n-49)$. It can be observed that there is a special relation which is

shown in Eq. (3.11), between a11 and a49. Eq. (3.11) can be realized as the architecture shown in Figure 3-38. There are no components of $2^0$ and $2^1$ in a11 and a49, so we can store the answer of $a_{11}x(n-11)+a_{49}x(n-49)$ by a register of 8-bit. A 10-bit adder is used in this operation originally. Now three simple gate can realize the operation. These two ways reduce power consumption and area of the ADC greatly. And the other parameters which cannot be distributed by the first way are realized by the second way as shown in Figure 3-39.

$$\begin{aligned} b2 = b5 = b8 &= x(n-11) \oplus x(n-49) \\ b4 = b7 = b9 &= x(n-11) \bullet x(n-49) \\ b3 = b6 &= x(n-11) + x(n-49) \end{aligned} \quad . \qquad (3.11)$$

Table 5: Truth table of $a_{11}x(n-11)+a_{49}x(n-49)$.

| x(n-11) | x(n-49) | b12 | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

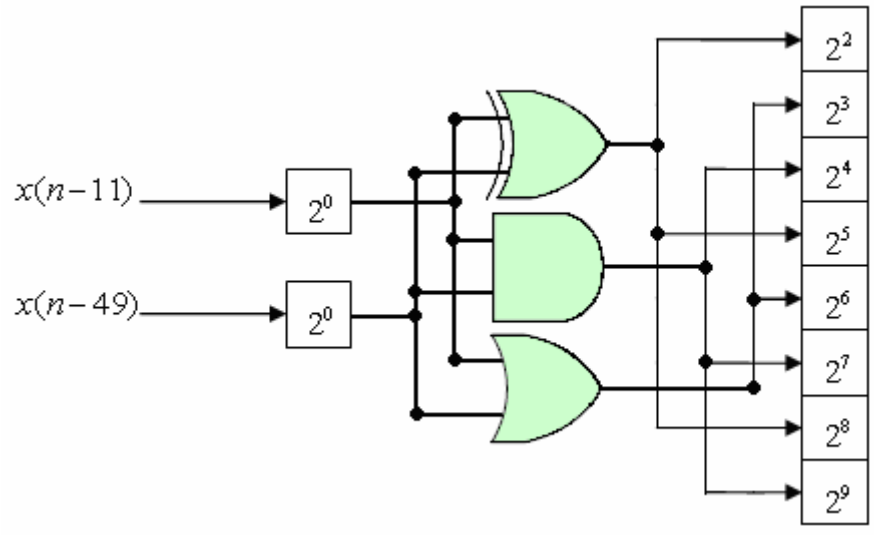



Figure 3 - 38: The architecture of $a_{11}x(n-11)+a_{49}x(n-49)$.

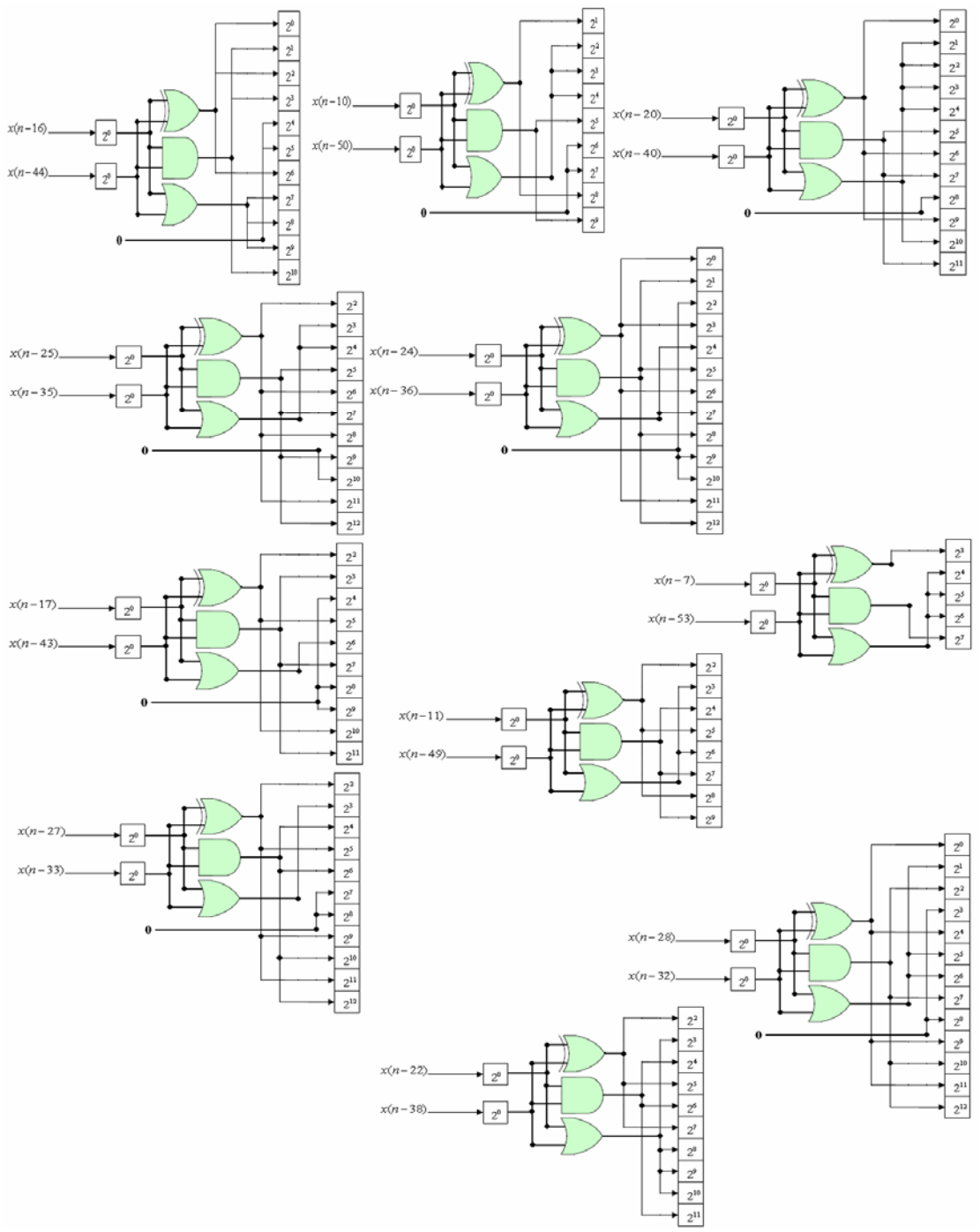



Figure 3 - 39: Architectures of whole operations which use the second way.

By above two ways, the extensive operations of CIC filter which needs a lot of adders are reduced to be realized by few adders, logic gates and registers. In the other hand, because numbers of parameters of Sine compensator and Cosine compensator are not many, there are 9 and 4 parameters in Sine compensator and Cosine

compensator, respectively, multipliers is replaced by moving the bit to left. For example, the forth operation of Sine compensator is $-[x(n-3)*(936)_{10}]=-[x(n-3)*(1110101000)_2]$ . Due to the input of Sine compensator is 17-bit, a multiplier of 17-bit will be used if we use multiplier to realize the operation. Otherwise, we can add these five numbers which move x(n-3) to left 3, 5, 7, 8 and 9 bits. The way can reduce power consumption and area greatly.

### 3 - 5 - 2 Design of HB Filter

HB filter is used for second, third, forth and fifth stages decimation filter. Half parameters of HB filter are 0. So HB filter has the same efficiency as other kind FIR filter with the same order, but its quantization error, area and power consumption will be lower than other kind FIR filter with the same order. There are four stages HB filters which have to be designs. We use FDA tool of MATLAB to simulate them first. Equirippple type of Halfband low pass filter is chosen. The specification is shown in Table 6.

Table 6: Specifications of the four stages decimation filter.

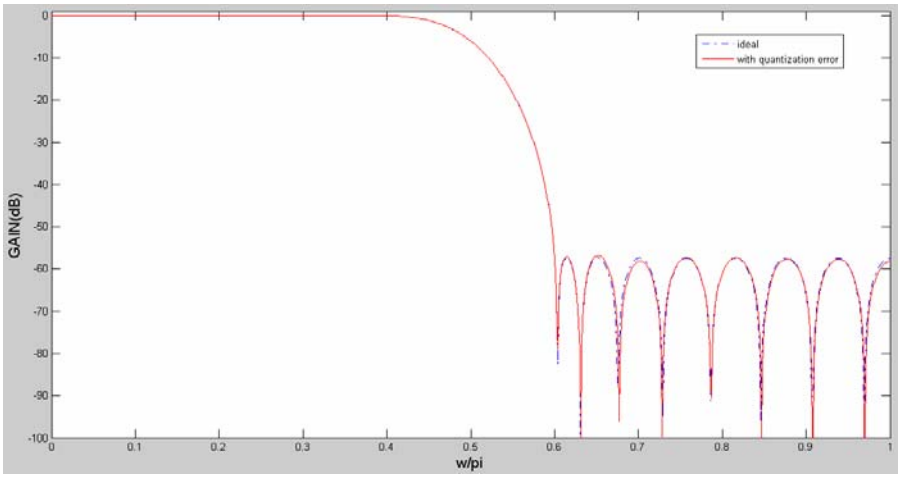
| | Decimation rate | Tap number | order | Cutoff frequency | Ripple in pass-band | Attenuation in stop-band | Sampling frequency |
|---|---|---|---|---|---|---|---|
| **First stage HB filter** | 2 | 16 | 30 | 8kHz | <0.012dB | 57dB | 40kHz |
| **Second stage HB filter** | 2 | 9 | 14 | 3.5kHz | <0.05dB | 45dB | 20kHz |
| **Third stage HB filter** | 2 | 9 | 14 | 1.75kHz | <0.05dB | 45dB | 10kHz |
| **Forth stage HB filter** | 2 | 13 | 22 | 1kHz | <0.05dB | 45dB | 5kHz |

The parameters of HB filters include decimal figure. Due to the limit of finite bit number, we have to approximate these parameters in our design. Table 7 shows the parameters of the four stages HB filters in approximation. Additionally, the parameters of the first stage HB filter approximate value of 13-bit, and then the parameter errors will be limited to the value lower than $\frac{1}{2^{14}}$. The parameters of the second and third stage HB filter approximate value of 10-bit, and then the parameter errors will be limited to the value lower than $\frac{1}{2^{11}}$. The parameters of the forth stage HB filter approximate value of 11-bit, and then the parameter errors will be limited to the value lower than $\frac{1}{2^{12}}$. These parameters of the four stages are shown in Table 7. And their spectrums are shown in Figure 3-40. It's easy to see that the error between the ideal filters and the filters with approximation is small, so those approximations are effective.

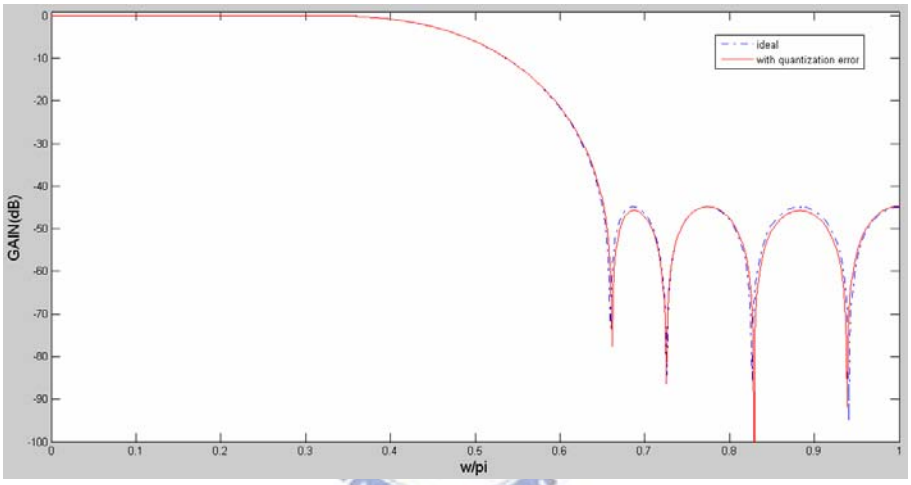
Those four stages HB filters are realized by verilog code without multiplexer, because multiplexer can be replaced by moving the binary value to the left. For example, if there is a operation of multiplying by $(2130)_{10} = (100001010100)_2$, we just have to add these values moved the multiplicand to left by 2-bit, 4-bit, 6-bit and 11-bit. Then there is no need to use multiplexer, so the way can save power and area of the design.

Table 7: Approximated parameters of the four stage HB filters.

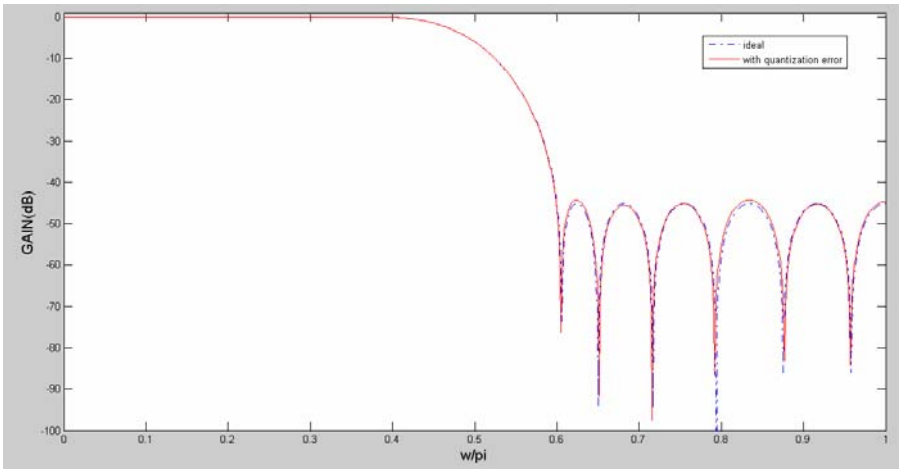
| | 1st HB filter | 2nd & 3rd HB filter | 4th HB filter |
|---|---|---|---|
| 0 | -0.0020751953125 | -0.01171875 | -0.00732421875 |
| 1 | 0 | 0 | 0 |
| 2 | 0.004638671875 | 0.033203125 | 0.013671875 |
| 3 | 0 | 0 | 0 |
| 4 | -0.0093994140625 | -0.0849609375 | -0.0263671875 |
| 5 | 0 | 0 | 0 |
| 6 | 0.0172119140625 | 0.310546875 | 0.048828125 |
| 7 | 0 | 0.5 | 0 |
| 8 | -0.02978515625 | 0.310546875 | -0.0966796875 |
| 9 | 0 | 0 | 0 |
| 10 | 0.051513671875 | -0.0849609375 | 0.31494140625 |
| 11 | 0 | 0 | 0.5 |
| 12 | -0.098388671875 | 0.033203125 | 0.31494140625 |
| 13 | 0 | 0 | 0 |
| 14 | 0.315673828125 | -0.01171875 | -0.0966796875 |
| 15 | 0.5 | | 0 |
| 16 | 0.315673828125 | | 0.048828125 |
| 17 | 0 | | 0 |
| 18 | -0.098388671875 | | -0.0263671875 |
| 19 | 0 | | 0 |
| 20 | 0.051513671875 | | 0.013671875 |
| 21 | 0 | | 0 |
| 22 | -0.02978515625 | | -0.00732421875 |
| 23 | 0 | | |
| 24 | 0.0172119140625 | | |
| 25 | 0 | | |
| 26 | -0.0093994140625 | | |
| 27 | 0 | | |
| 28 | 0.004638671875 | | |
| 29 | 0 | | |
| 30 | -0.0020751953125 | | |




(a)




(b)




(c)

Figure 3 - 40: Spectrum of the ideal filter and filter with approximate parameters (a) the 1st stage HB filter (b) the 2nd and 3rd one (c) the 4th one.

### 3 - 5 - 3 Simulation Result

Those seven stages decimation filter are simulated by simlink as Figure 3-41. And the HB filters are simulated with approximation. We connect the decimation filters with Sigma-Delta modulator to observe the spectrum of the output of decimation filters.

The simulation result is shown in Figure 3-42. From this result, we can get ENOB is 16-bit in bio-electric signal mode; ENOB is 8-bit in bio-image signal mode. The function of decimation filter is correct form this result.

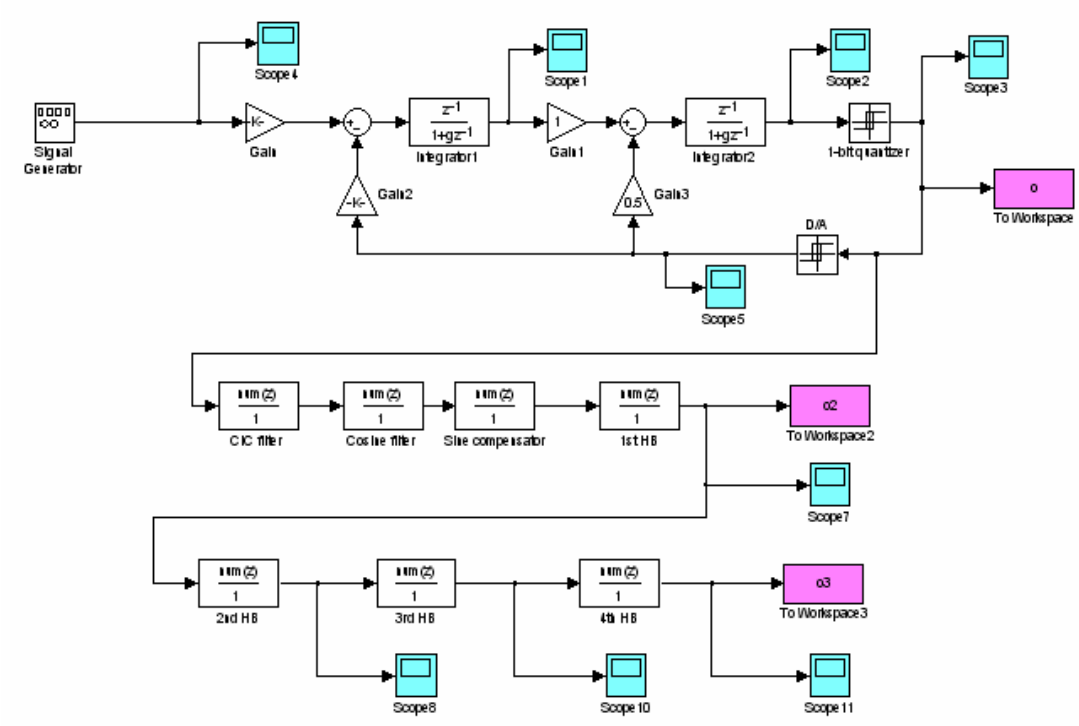



Figure 3 - 41: Block diagram of decimation filter by simulink.

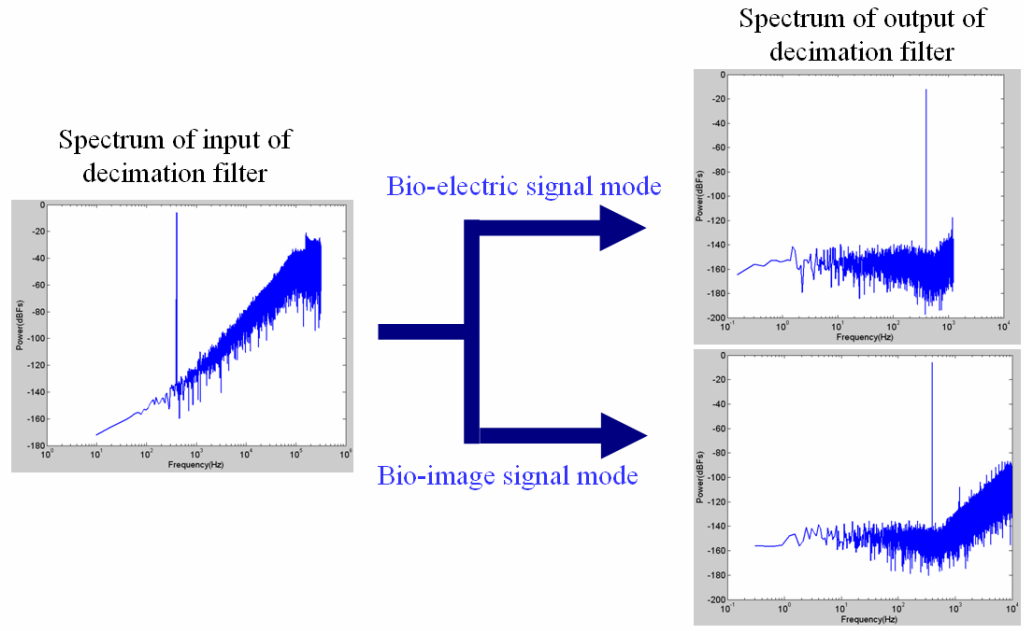



Figure 3 - 42: Simulation result of decimation.

## 3 - 6 Design of SPI Bus

We hope our ADC can communicate with DSP directly in this design, so we choose SPI to be the bridge between ADC and DSP. The mode which is that CPOL = 1 and CPHA = 1 of SPI is chosen. The diagram of this mode is shown in Figure 3-43. The kind of transmission is that input or output of slave (ADC) is delivered to DSP on the negative edge of CLK not on the negative edge of SS. Then DSP can receive or deliver date on positive edge of CLK. It's a more convenient way for DSP to receive or deliver date.

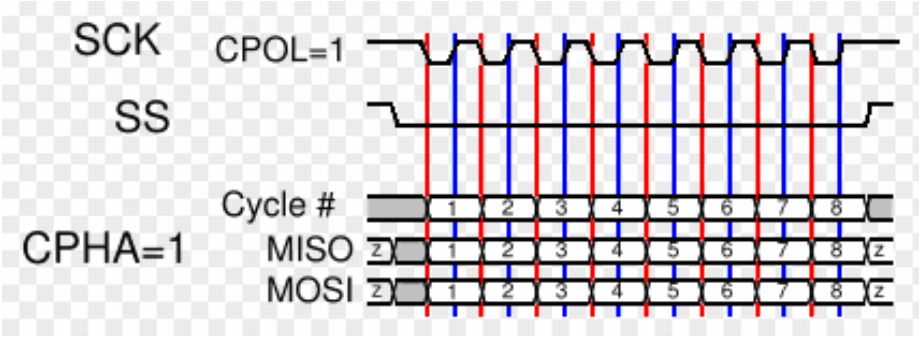



Figure 3 - 43: SPI of CPOL = 1 and CPHA = 1.

# Chapter 4

# Realization and Layout of Whole Chip and Testing Consideration

In this chapter, chip realization including the design flow, layout and post simulation will be described. And the testing plan will be introduced beyond the realization.

## 4 - 1 Design Flow

The design flow of Sigma-Delta modulator is shown in Figure 4-1. The whole modulator specification has to be planned first. Then simulink is used to simulate the modulator with the non-ideal factors, and to let the modulator with non-ideal factors meets the specification. After simulation by simulink, we design the transistor level circuit by HSPICE. Then we draw the layout of modulator by Laker, and do DRC and LVS verification by Calibre tool. Then we do the post simulation of the modulator with parasitical capacitor, parasitical resistor and coupling capacitor.

The design flow of digital part is shown in Figure 4-2. The specifications was planned first. Then system level simulation of the decimation filter was simulated by Matlab. Then RTL simulation and Gate level simulation were be done by modelsim. After the two simulations, we place and route the circuit by Soc Encounter.

In order to design a mix signal chip, the circuit and IO pad of analog part have to be translated into several macros. Then we can place and route the whole ADC by Soc Encounter.

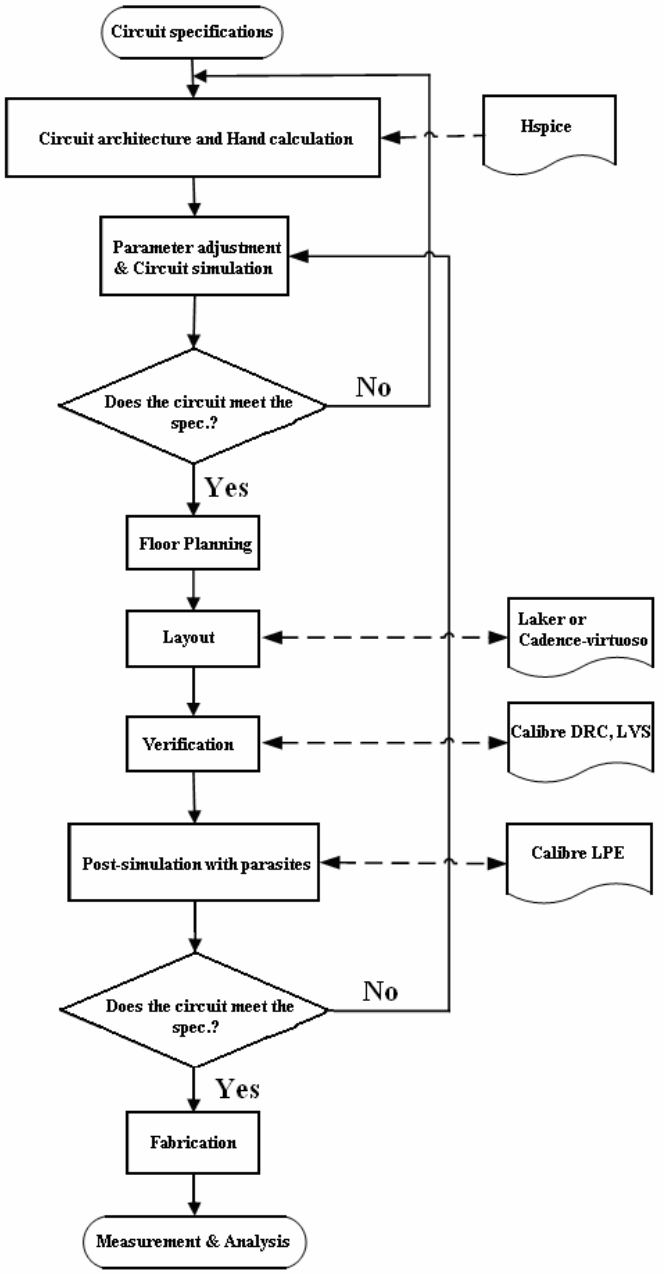



Figure 4 - 1: Design flow of Sigma-Delta modulator.

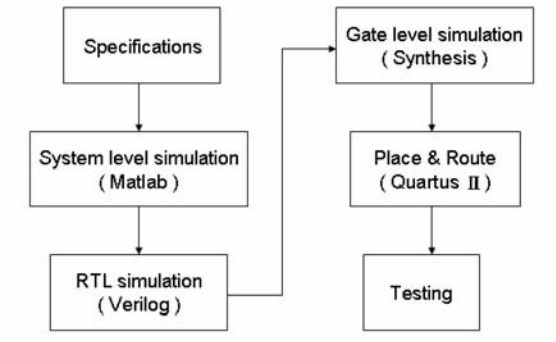



Figure 4 - 2: Design flow of digital part.

## 4 - 2 Layout and Post Simulation of Sigma-Delta Modulator

The layout of Sigma-Delta modulator is shown in Figure 4-3. And its post simulation result is shown in Figure 4-4. we can get SNR is 60db which means ENOB is 10-bit in bio-electric signal mode and SNR is 50db which means ENOB is 8-bit in bio-image signal mode. It's almost the same with pre-simulation.

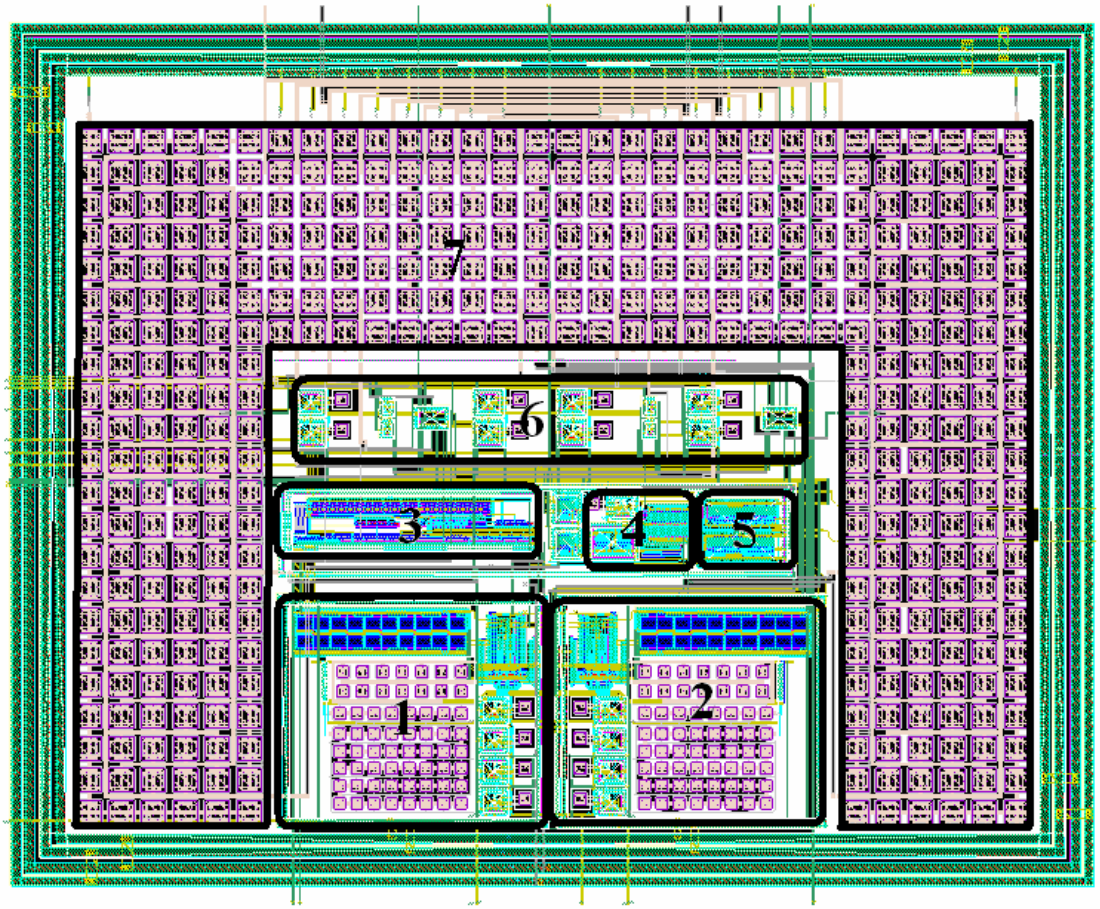



Figure 4 - 3: Layout of Sigma-Delta modulator, additionally, 1, 2 are opamp circuits; 3 is bias circuit; 4 is comparator circuit; 5 is clock generator circuit; 6 is switch circuit; 7 is capacitor array.

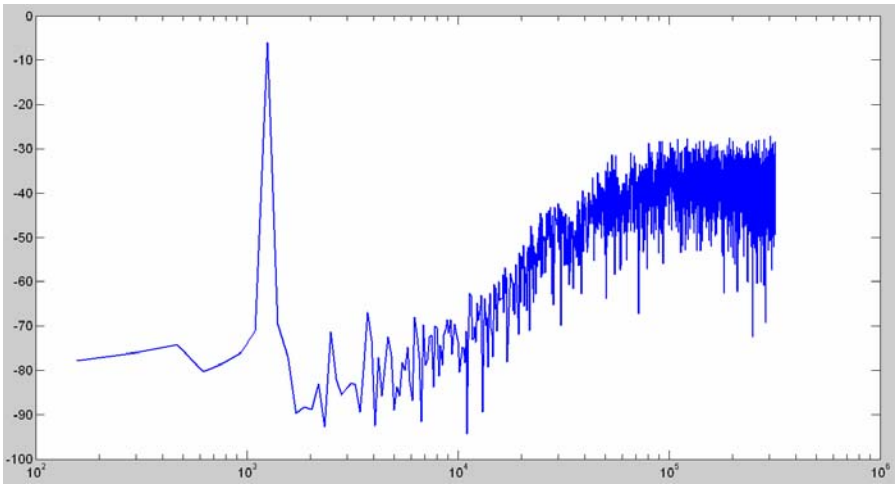



Figure 4 - 4: Post simulation result of Sigma-Delta modulator.

## 4 - 3 Layout and Post Simulation of Sigma-Delta ADC

The layout of whole circuit is shown is Figure 4-5. Additionally, the core size of the whole chip is 2.14mm×1.5 mm, and its power consumption is 14.2mW (analog part: 977.53uW; digital part: 13.235mW).

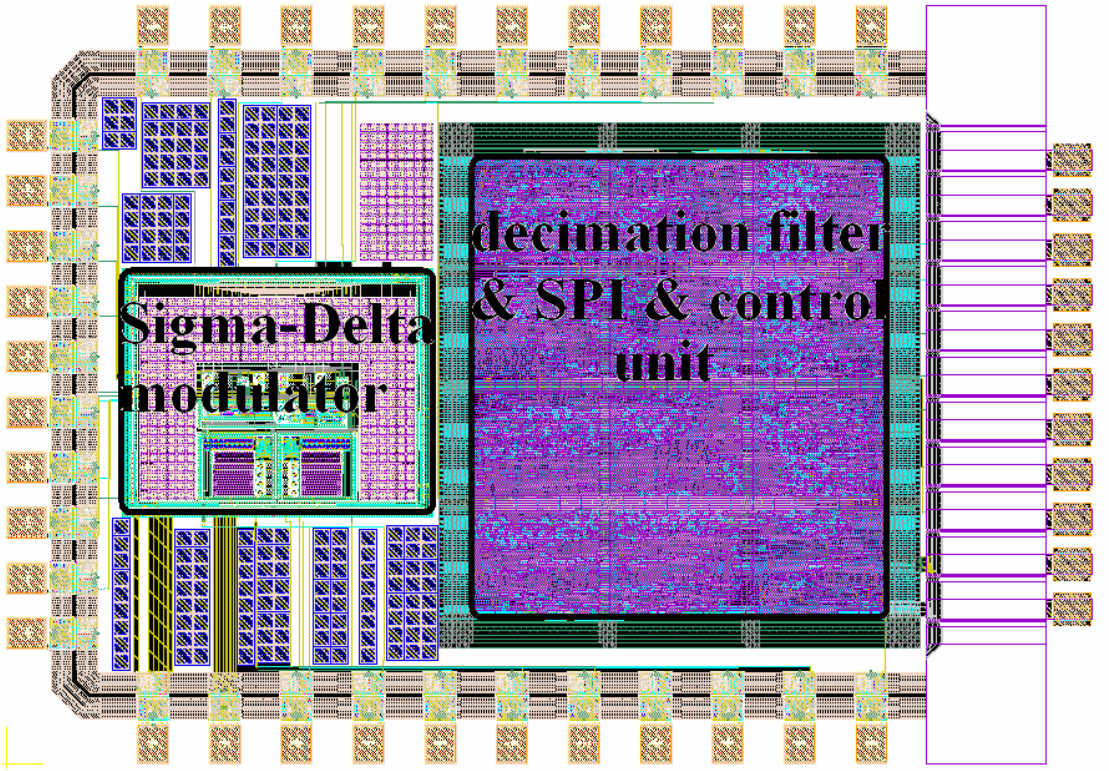



Figure 4 - 5: Layout of whole chip.

To verify the digital circuit of this work, we use two patterns to test it and compare the result with the result simulated by simulink to verify if the circuit is work well. One pattern is for bio-electric signal mode, the other one is for bio-image signal mode.

1. bio-electric signal input:

The input is a 500 Hz sine wave with 0.375 V amplitude. The result is shown in Figure 4-6. The transmission conforms to SPI which is triggered by negative edge of clock.

The output of the design is shown in right of Figrue 4-7. And the left of Figure 4-7 is the ideal wave drawn by simulink. It's easy to see they are almost the same. The spectrum of the output of the design is shown in Figure 4-8. we can get SNR is 80dB and ENOB is 13-bit.

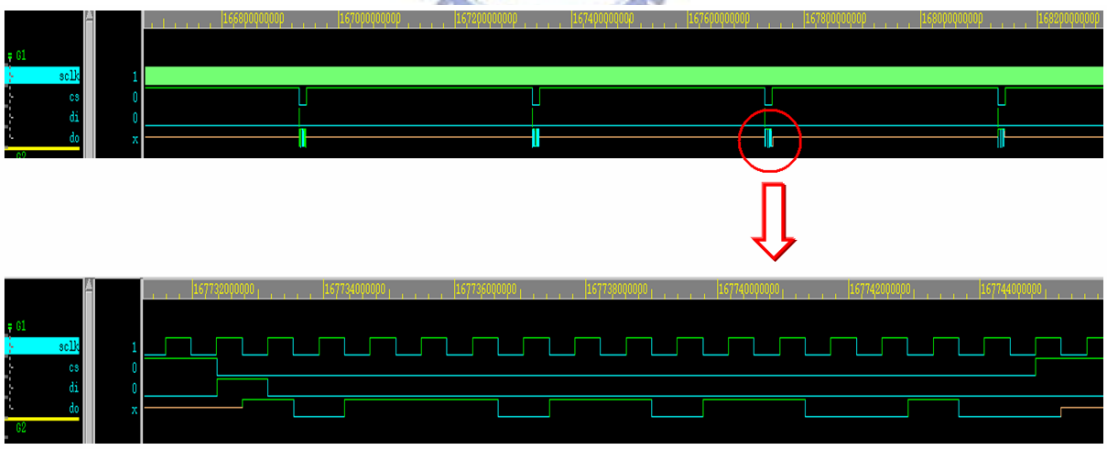



Figure 4 - 6: The ADC output in bio-electric signal mode.

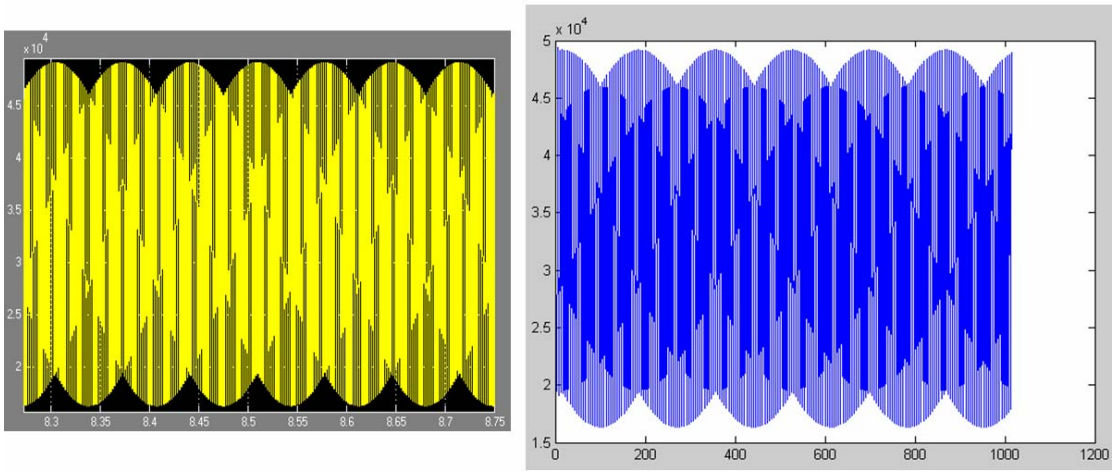



Figure 4 - 7: Ideal output wave versus the output of real design.

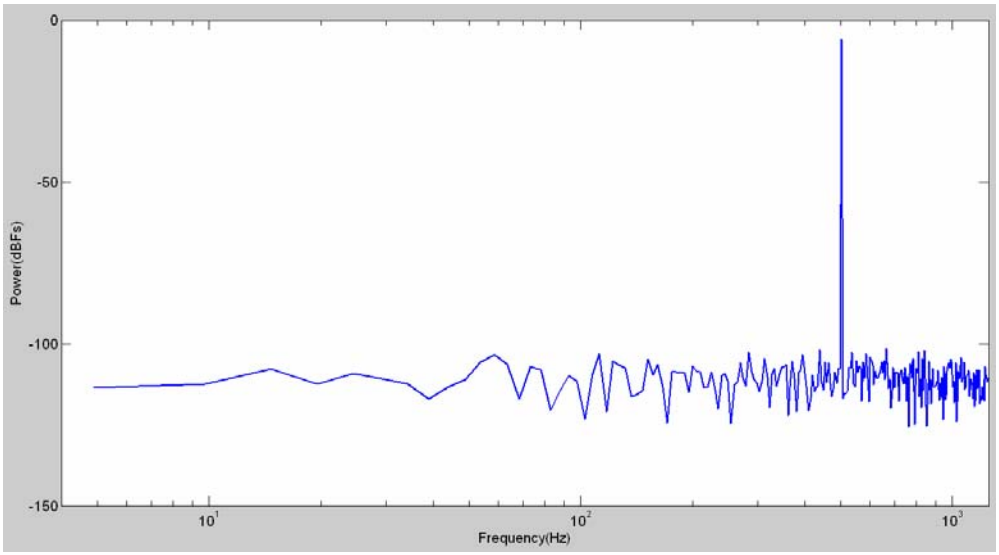



Figure 4 - 8: Spectrum of the output of the first test.

2. bio-image signal input:

The input is a 4 kHz sine wave with 0.375V amplitude. The result is shown in Figure 4-9. The transmission conforms to SPI which is triggered by negative edge of clock.

The output of the design is shown in right of Figrue 4-10. And the left of Figure 4-10 is the ideal wave drawn by simulink. It is easy to see they are almost the same. The spectrum of the output of the design is shown in Figure 4-11. we can get SNR is 45dB and ENOB is 8-bit.

Specifications of this design are shown in Table 8. And Table 9 shows that this work versus other researches.

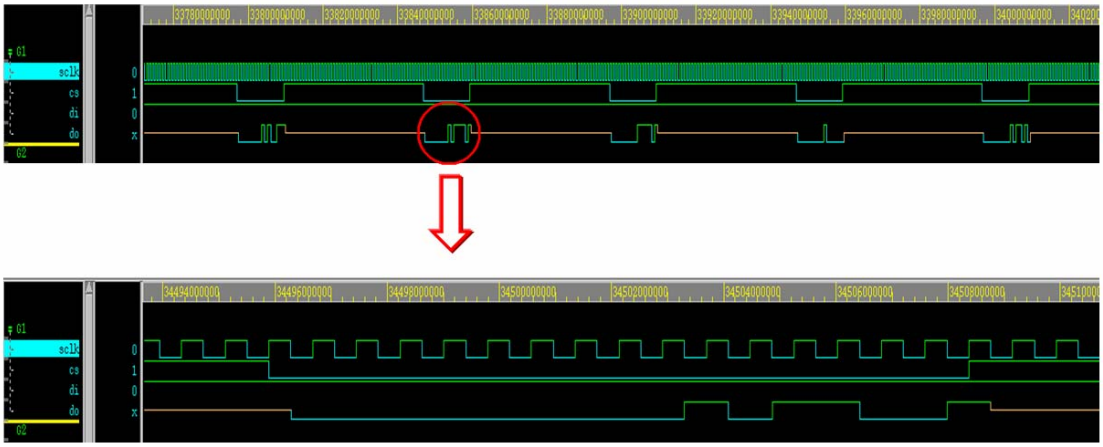



Figure 4 - 9: The ADC Output in bio-image signal mode.

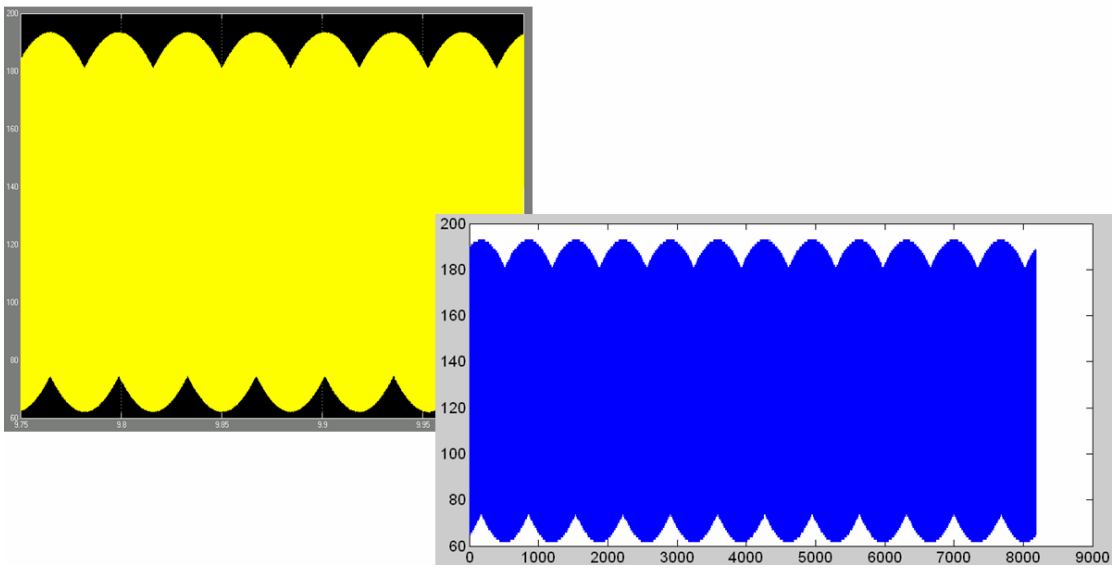



Figure 4 - 10: Ideal output wave versus the output of real design.

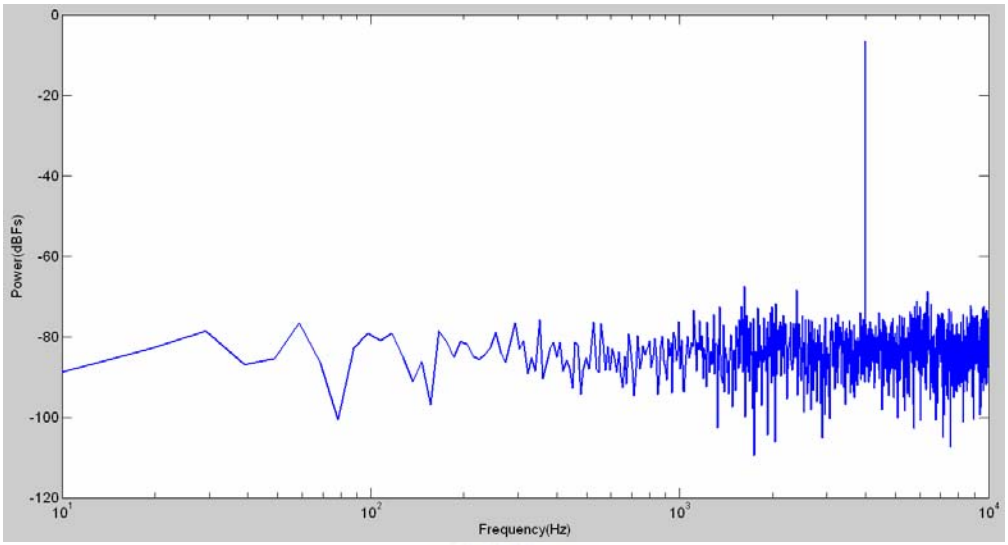



Figure 4 - 11: Spectrum of the output of the second test.

Table 8: Specifications of this ADC.

| | | |
|---|---|---|
| **Process** | TSMC 0.18um 1P6M | |
| **Supply Voltage** | 1.5V | |
| **Temperature range** | 0°C ~ 90°C | |
| **Input Clock** | 1.28MHz | |
| **Mode** | **Bio-electric signal** | **Bio-image signal** |
| **Signal Bandwidth** | 1.25kHz | 10kHz |
| **Sampling Frequency** | 640kHz | |
| **SNR** | 60 dB | 50 dB |
| **Resolution** | 10 bit | 8 bit |
| **Power Dissipation** | 14.2 mW (analog:977.53uW; digital:13.235mW) | |

Table 9: Comparison with other researches.

| Refs | Topo-logy | Mode | Signal type | BW (Hz) | OSR | SNDR (dB) | Tech-nology (um, V) | Die size ($mm^2$) | Power (mW) | FOM (uW/step) |
|---|---|---|---|---|---|---|---|---|---|---|
| **IEEE 2001 [13]** | 2nd | N/A | Audio | 8k | 64 | 49.7 | 0.6, 3.3 | N/A | 6.996 | **27.33** |
| **ESSCIRC 2002 [15]** | 2nd | N/A | ADSL | 300k | 96 | 82 | 0.18, 1.8 | N/A | 9 | **1.1** |
| **ISSCC 2005 [16]** | 2nd | N/A | WCDMA | 1.94M | 20 | 63 | 0.09, 1.2 | 0.2 | 1.2 | **1.17** |
| **ESSCIRC 2006 [17]** | 2nd | N/A | Audio | 312k | 16 | 65 | 0.09, 0.6 | 2.2 | 7.2 | **3.52** |
| **IEEE 2008 [22]** | 2nd | Mode 1 | GSM | 100k | 128 | 85.7 | 0.18, 1.8 | N/A | 4.2 | **0.26** |
| | | | GPS | 1000k | 32 | 61.1 | | | 6.3 | **6.15** |
| | | | Bluetooth | 500k | 64 | 76.3 | | | 6.3 | **1.54** |
| | | | WCDMA | 1.92M | 32 | 59.4 | | | 10.7 | **10.45** |
| | 4th | Mode 2 | GPS | 1000k | 16 | 73.7 | | | 12.7 | **3.1** |
| | | | WCDMA | 1.92M | 16 | 71.2 | | | 17 | **4.12** |
| | 2nd | Mode 3 | WiMAX | 10M | 8 | 59.9 | | | 49 | **47.85** |
| | | | WLAN | 11M | 8 | 60.1 | | | 49 | **47.85** |
| | 4th | Mode 4 | WiMAX | 10M | 8 | 65.9 | | | 74.6 | **36.43** |
| | | | WLAN | 11M | 8 | 63.9 | | | 74.6 | **72.85** |
| **This work** | 2nd | Mode 1 | Bio-electric signal | 1.25k | 256 | 60 | 0.18, 1.5 | 0.3 | 0.98 | **0.96** |
| | | Mode 2 | Bio-image signal | 10k | 32 | 50 | | | 0.98 | **3.83** |

* $FOM = \frac{Power}{2^{ENOB}}$

## 4 - 4 Testing Consideration

We connect the chip with signal generator and power supply, and use signal generator to generate sine waves for the input of this chip. The mode has to be chosen when testing. Then we observe the output wave if it conforms to SPI bus. We can get the data by logic analyzer, and then analyze this data in Matlab to see if the spectrum

of the output is correct. After that, we can analyze the SNR, ENOB, INL and DNL of this ADC.

If the testing result is not correct, then we can test where the problems are. We output some testing IO pin of analog part, so we can test the chip to figure out what stage is wrong. In the digital part, we have added the scan chain to test the whole D filp-flop. After getting the error information, we can improve or resolve those problems in next generation.

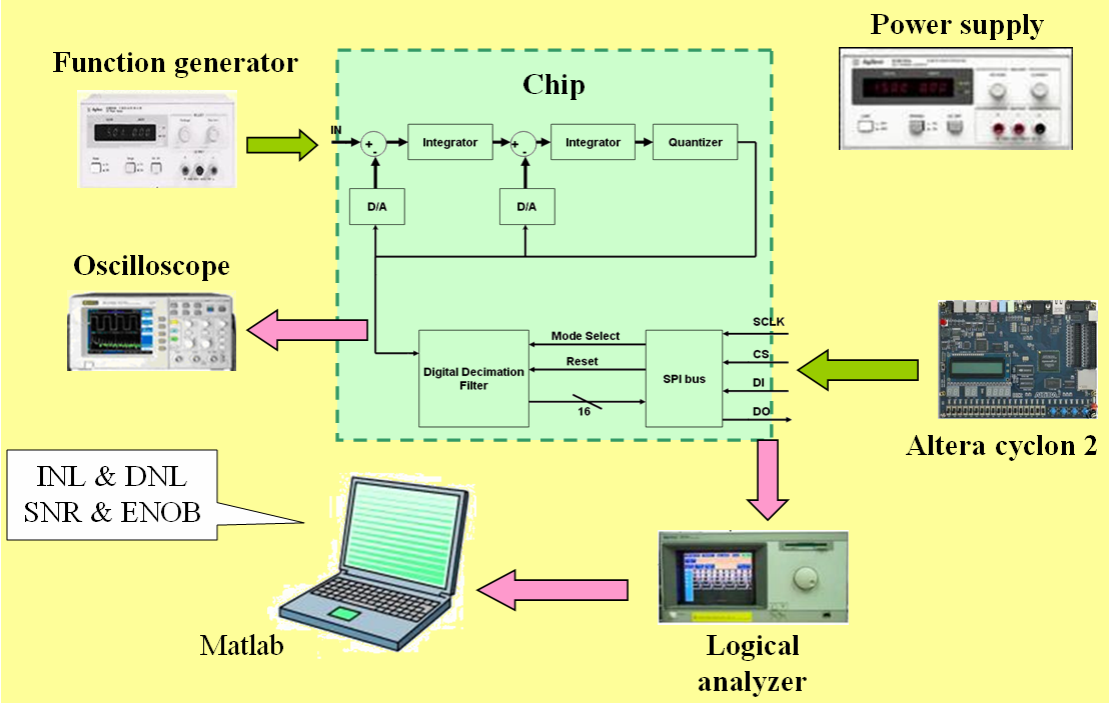



Figure 4 - 12: Testing platform.

# Chapter 5

# Conclusions

This paper presents a Sigma-Delta ADC which can change resolution when the kind of the input signal is different. This ADC provides two modes can be chosen, one is for bio-electric signal, the other one is for bio-image signal. This ADC operates on 1.28 MHz. The sampling rate of the ADC is 640 kHz. For bio-electric signal, OSR is 256; for bio-image signal, OSR is 32. The ADC communicates with DSP or other operator by SPI bus. In the bio-electric signal mode, SNR is 50dB, ENOB is 10-bit; in the bio-image signal mode SNR is 50dB, ENOB is 8-bit. It has been fabricated by TSMC 0.35 μm CMOS 2P4M standard process. The total power consumption of the chip is about 14.4 mW under 1.5V supply, and the power consumption of Sigma-Delta modulator is about 977uW; the power consumption of digital part is 13.3 mW. The area of the chip is 3.21 $mm^2$.

There are two ways to improve the ADC for biomedical application as follows.

1. Increase the resolution of the ADC.

The first one is that SNR of the ADC can be improved. To improve SNR, the problem of noise in low frequency has to be solved. As above, the sources of noise are thermal noise and flicker noise, which are belong noise in low frequency. The solution might be that chapping circuit is added in the input of each integrator, then the noise in low frequency can be move to the high frequency, and the filter can filter the noise in high frequency to increase the SNR.

2. Decrease the cost of whole circuit.

The second way is decrease the cost of the chip, like area and power consumption. Using smaller process or lower the size of passive cells can let the area of the ADC be smaller. And designing op or comparator in subthreshold region can lower power consumption of the ADC. In digital part, optimizing the operation of decimation filter can lower power consumption and area of the ADC also.

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# Appendix

## A DRC Verification

The error information is shown in Figure A. By the way, there are some errors which can be ignored like OD.S.1, OD.C.1, OD.C.5, RPO.C.3 and RPO.C.6 which are the fake errors of IO PAD and PO.R.3, M1.R.1, M2.R.1, M4.R.1, M5.R.1 and _M6T.R.1 errors which occur, when the density of every metals and poly are not enough, in the cause of that the cells in digital part have not put in the layout file.

```
351 RULECHECK OD.S.1 ............ TOTAL Result Count = 0   (0)
352 RULECHECK OD.C.1 ............ TOTAL Result Count = 20  (248)
353 RULECHECK OD.C.5 ............ TOTAL Result Count = 4   (31)
354 RULECHECK RPO.C.3 ........... TOTAL Result Count = 10  (118)
355 RULECHECK RPO.C.6 ........... TOTAL Result Count = 96  (96)
356 RULECHECK PO.R.3 ............ TOTAL Result Count = 1   (1)
357 RULECHECK M1.R.1 ............ TOTAL Result Count = 1   (1)
358 RULECHECK M2.R.1 ............ TOTAL Result Count = 1   (1)
359 RULECHECK M4.R.1 ............ TOTAL Result Count = 1   (1)
360 RULECHECK M5.R.1 ............ TOTAL Result Count = 1   (1)
361 RULECHECK _M6T.R.1 .......... TOTAL Result Count = 1   (1)
362 RULECHECK VTMN.I.3 .......... TOTAL Result Count = 0   (0)
```

Figure A: The information of DRC verification

# B LVS Verification

The ADC is mix-signal chip design, so there are two LVS verifications, one is verification of the analog circuit, the other one is verification of the whole chip. In the second verification, analog circuit and other digital cells are accounted block boxes, the verification checks the connection of every cells only. The information of LVS verification of the analog part is shown in Figure B-1; the information of LVS verification of the whole chip is shown in Figure B-2.

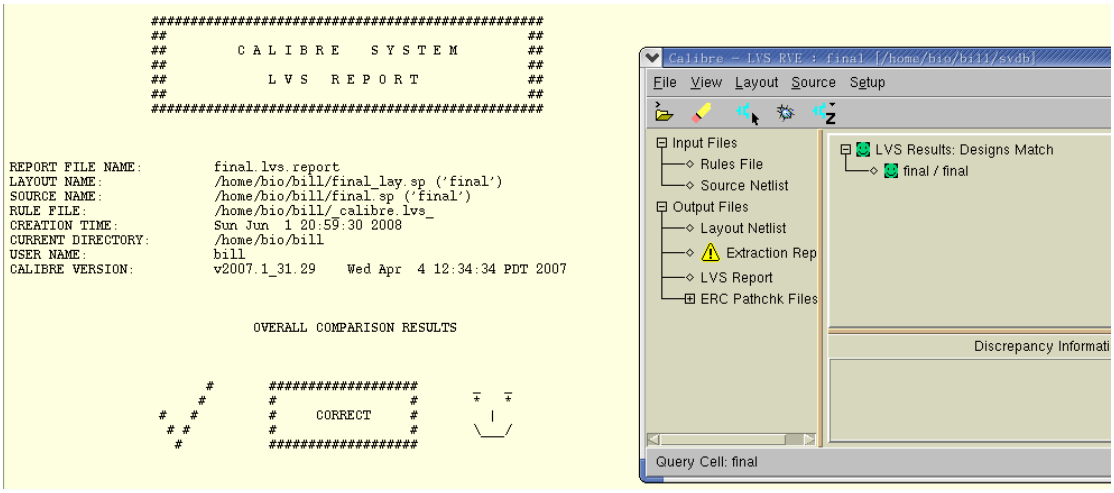
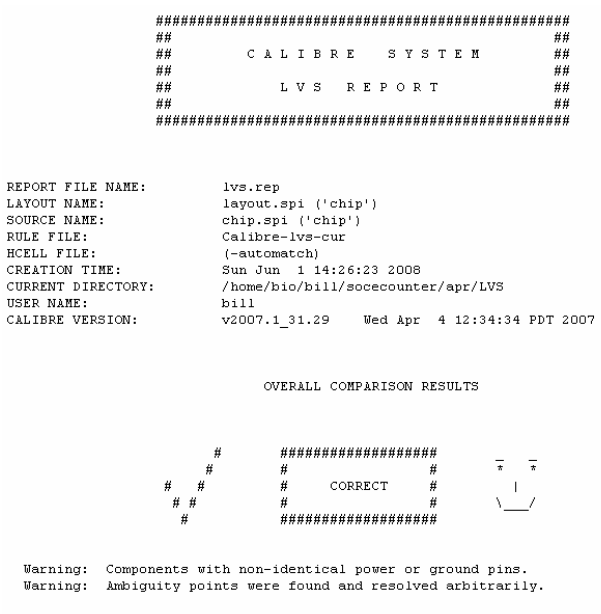



Figure B - 1: The information of LVS verification of the analog part



```
#####################################################
##                                                 ##
##         C A L I B R E    S Y S T E M            ##
##                                                 ##
##             L V S   R E P O R T                 ##
##                                                 ##
#####################################################


REPORT FILE NAME:          lvs.rep
LAYOUT NAME:               layout.spi ('chip')
SOURCE NAME:               chip.spi ('chip')
RULE FILE:                 Calibre-lvs-cur
HCELL FILE:                (-automatch)
CREATION TIME:             Sun Jun  1 14:26:23 2008
CURRENT DIRECTORY:         /home/bio/bill/socecounter/apr/LVS
USER NAME:                 bill
CALIBRE VERSION:           v2007.1_31.29    Wed Apr  4 12:34:34 PDT 2007


                          OVERALL COMPARISON RESULTS


                        #       ####################        _   _
                      #         #                  #        *   *
                    #   #       #     CORRECT      #          |
                     # #        #                  #        \___/
                      #         ####################


  Warning:  Components with non-identical power or ground pins.
  Warning:  Ambiguity points were found and resolved arbitrarily.
```

Figure B - 2: The information of LVS verification of the whole chip

# C Tapeout Review Form

## 1．Tapeout review form (for Full-custom IC)

Tapeout review form 的用意在提醒設計者在設計、模擬、佈局、佈局驗證及 tapeout 時具備設計理念及了解應注意事項,希望能藉此提昇晶片設計的成功率及達到完整的學習效果。因此,請指導教授及設計者確實檢查該晶片設計過程是否已注意本表格之要求,並在填寫確定後簽名,若審查時發現設計內容與 Tapeout Review Form 之填寫不符,很可能遭取消該晶片下線製作資格。可參考本表後所附範例確實填寫。

1 電路概述

專題名稱: 低電壓供應、低功耗、二種模式(適用於生醫訊號和影像訊號)、SPI 介面傳輸之 sigma-delta adc

1-1. Top Cell 名稱: chip

1-2. 製程名稱: TSMC 0.18 UM CMOS Mixed Signal RF General Purpose MiM AI 1P6M 1.8&3V

1-3. 工作電壓: 0V~1.5V

1-4. 工作頻率: 1.28KHz

1-5. 功率消耗: 類比部分：977.53uW；數位電路：13.235mW；共 14.2mW

1-6. 是否使用 CIC 提供之 ARM CPU IP？ 否

使用 CPU 之種類爲何？(ARM7TDMI or ARM926EJ) 未使用

1-7. 此電路架構於貴實驗室是否第一次設計?是(接 2-1) 是 否(接 1-6-1)

1-7-1. 此電路之前不 work 或 performance 不好的原因爲何?

1-7-2. 對之前的錯誤作何種修改?

2 電路模擬考量

2-1 . 已用 SS,SF,TT,FS,FF 中哪些不同狀態之 spice model 模擬? SS SF TT FS FF

2-2 . 已模擬過電壓變動+/-10%中哪些情況對電路工作之影響? 是

2-3 . 如何考量溫度變異之影響? 已測試過溫度變異對整體電路的影響(0 度~90 度)

2-4 . 如何考量電阻、電容製程變異之影響?加入 dummy 及使用對稱佈局法以減少變異影響

2-5 模擬時是否加入 IO PAD、Bonding wire 的效應及考量測試儀器之負載等影響? 是

2-6 是否作 LPE 及 post layout simulation? 是 使用的軟體爲 Laker&Calibre&Hspice

3 Power Line 佈局考量

3-1. Power Line 畫多寬? >5um

3-2. 是否考量 power line current density? 是

3-3. 是否考量 Metal Line 之寄生電阻、電容? 是

4 DRC,LVS

4-1. 是否有作 whole chip 的 DRC 及 LVS?___是_____

4-2. 除了 PAD 上 DRC 的錯誤之外,內部電路及與 PAD 連接的線路是否有錯?_0___錯誤原因爲何?_____

4-3. 在作 LVS 的過程中,PIN 腳及元件是否 match?__是___ 不 match 的原因爲何?_____

4-4. 檢查 PAD 與 PAD 間是否有移位、短路或斷路的現象?____否_____

5 類比-混合訊號電路佈局考量(類比-混合訊號電路設計者填寫)

5-1 佈局對稱性及一致性考量

5-1-1 OP(Comparator) Input Stage 是否對稱?__是_____

5-1-2 OP(Comparator) Input Stage 是否對稱?____是_____

5-1-3 佈局中對稱元件是否使用 dummy cell 技巧?___是_____

5-1-4 對稱電容是否採用同心圓佈局?__是_____

5-1-5 對稱單位電容四周是否切成 45 度斜角?_____是_____

5-1-6 對稱電容的單位面積是否一致?___是_____

單位電容面積多大?___7.399_____um x___7.399____um

單位電容值多大?___0.05_____pF

5-1-7 電阻採用哪一材質製作?P+ poly resistor with RPO

單位電阻值多大?_____1K____ohm_____

5-2 電路雜訊佈局考量

5-2-1 是否將 Analog 及 Digital 的 power line 分開?_____是_____

5-2-2 Analog area 是否用 guard ring 隔絕?_____是_____

5-2-3 Digital area 是否用 guard ring 隔絕?_____是_____

5-2-4 對於 sensitive line 是否使用 shield 的技巧?____是_____

5-2-5 Analog guard ring 及 shield 是否接至乾淨之電位?__是_____

5-2-6 是否將 sensitive line 儘量縮短及避免跨越 noise(clock)line?__是____

5-2-7 電容的上下極板是否接對?_____是_____

6 MEMS 設計考量(MEMS 設計者填寫)

6-1 請簡述所進行之後製程：_____

6-2 後製程操作地點：_____

6-3 下線者目前是否有操作該製程設備之合法授權?_____若目前無操作該製程設備之合法授權，是否可在晶片取回前得到合法授權?_____

6-4 下線者是否有使用該製程設備之經驗?_____

6-5 是否有該後製程之製程參數（壓力、溫度、流量、……）?_____

6-6 之前是否有成功實現過該後製程?_____

6-7 Layout 違反 design rule 的部分是否會影響微結構本身或元件操作？___

6-8 Layout 之蝕刻孔尺寸是否足以讓結構懸浮?_____

6-9 元件驅動電壓範圍?_____

7 RF Circuit 電路佈局考量 ( RF 操作頻段設計者填寫)：

7-1 電路規格適用何種系統? _____

7-2 說明被動元件模型的來源 _____

7-3 模擬軟體 (可不只一種)? _____

7-4 系統整合 chip 裡之各個 block 是否曾下過線且量測符合預期規格 (chip 爲系統整合者回答,並說明製程梯次代號)?_____

7-5 佈局考量：

7-5-1 元件佈局方式是否與模型提供者所提供的佈局一致? _____

7-5-2 接地與電壓源是否均勻? _____

7-5-3 元件與拉線的電流承載能力考量? _____

7-5-4 拉線是否過長過細? _____

7-5-5 PAD 的佈局是否配合量測上之考量? _____

7-5-6 PAD 與 Bond-wire 的效應是否考量? _____

7-6 DRC 驗證過程中, 部分錯誤若爲特殊考量, 請說明_____

_____

_____

7-7 LVS 驗證過程中, 電感電容或其他特殊元件的比對是否做過處理, 請說明_____

_____

_____

7-8 量測方式爲 on wafer, on PCB or in package? 並說明量測時應該注意事項與量測地點

_____

_____

8 PAD Replacement 考量(使用 TSMC I/O PAD 設計者填寫)

8-1 已於申請表勾選申請使用 TSMC I/O PAD

8-2 個人設計的 Cell 名稱(cell-name)未與 TSMC 所提供之任一 Pad Cell 名稱相同__是____

8-3 採用 Create Instance 方式加入 I/O Pad，未用 Copy 或 Flatten 破壞 Instance 的結構_是

8-4 由 IC Core 部份拉線到 Pad 只拉到最邊緣部分，未過於覆蓋 Pad__是____

9. 使用 ARM926EJ or ARM7TDMI CPU IP

9-1. 若有使用 ARM926EJ /ARM7TDMI CPU IP，請提供以下訊息以便向 ARM 原廠申請 Design ID。

使用的 CPU 種類 (ARM926EJ or ARM7TDMI) :_____

使用的 metal layers 的層數:_____

佈局中 ARM926EJ /ARM7TDMI Macro 的 cell name:_____

這個晶片是否爲修訂版本(revision,也就是之前曾下線過相同晶片)？_____

若是修訂版本，前一次下線的晶片編號:_____

修訂版本的原因是？(例如修正 bug) _____

10 其他考量

10-1 是否考量測試時的輸出量測點?____是____

10-2 是否考量電路之可修改性(如用 laser cut 設備)_____是_____

設計者簽名:__張孟修_____ 指導教授簽名:__林進燈_____

# 2．Tapeout Review Form (for Cell-Based IC)

Tapeout review form 的用意在提醒設計者在設計、模擬、佈局、佈局驗證及 tapeout 時具備設計理念及了解應注意事項,希望能藉此提昇晶片設計的成功率及達到完整的學習效果。因此,請指導教授及設計者確實檢查該晶片設計過程是否已注意本表格之要求,並在填寫確定後簽名,若審查時發現設計內容與 Tapeout Review Form 之填寫不符,很可能遭取消該晶片下線製作資格。可參考本表後所附範例確實填寫。

1 晶片概述：

專題名稱：_低電壓供應、低功耗、二種模式(適用於生醫訊號和影像訊號)、SPI 介面傳輸之 sigma-delta adc_____

1-1 Top Cell 名稱：_chip_____

1-2 使用 library 名稱：

___ CIC_CBDK13

v__CIC_CBDK18

___ CIC_CBDK35

CBDK 版本: _CBDK018_TSMC_Artisan_v2.0_____

是否使用 Core Cell: _是__ 若有使用 Core Cell 有無更改 Cellname: _否__ (建議保留勿更改)

是否使用 IO: _是__ 若有使用 IO, 採用形式是 : _v__ Linear ___ Staggered

1-3 是否使用 CIC 提供之 Memory？ _否___ 若使用 Memory, 是否已上傳 spec 檔: __

使用 Memory 之種類爲何？ _____

1-4 是否使用 CIC 提供之 ARM CPU IP？ _否____(若爲 Yes, 請務必填寫第 9 項)

使用 CPU 之種類爲何？(ARM7TDMI or ARM926EJ) _____

1-5 工作頻率：___1.28kHz_____

1-6 功率消耗：類比部分：977.53uW；數位電路：13.235mW；共 14.2mW_

1-7 晶片面積：_2.14mm X 1.5mm

2 設計合成：

2-1. 使用之合成軟體？__Synopsys design compiler_____

2-2. 是否加入 boundary condition：

_v__ input drive strength、_v__ input delay、_v__ output loading、_v__ output delay

2-3. 是否加入 timing constraint：

_v_ specify clock (sequential design)

_v_ max delay、_v_ min delay (combinational design)

2-4. 是否加入 area constraint？ _v_

2-5. 合成後之 report 是否有 timing violation？no

___ 有 setup time violation、___ 有 hold time violation

2-6. 合成後之 verilog 是否含有 assign 描述？ 否

2-7. 合成後之 verilog 是否含有 *cell* 之 instance name？ 否

2-8. 合成後之 verilog 是否含有反斜線 \ 之 instance name 或 net name？ 否

3 可測試性設計(前瞻性晶片必填)：

3-1. 使用之設計軟體？DFT compiler

3-2. 使用之 ATPG 軟體？TetraMAX

3-3. 使用 Embedded memory 數量: SRAM 0 ，ROM 0

Memory 大小:

測試方法: BIST ，or 其他測試方法

若使用 BIST,其 Test Algorithm 爲何?

同時有多個 memory，是否共用 BIST controller ，BIST controller 數量

3-4. Scan Chain Information

Flip-Flop 共有多少個？ 2172

Scan chain 的數量共有多少條？ 1

Scan chain length (Max.) ？ 2172

3-5. Uncollapsed fault coverage 是否超過 90% ？ 是 ，爲多少？ 97.6%

ATPG pattern 的數目爲多少？ 98

註：若使用 Synopsys TetraMAX 來產生 ATPG pattern，請使用 set faults -fault_coverage 指令指定 TetraMAX 產生 fault coverage information

若使用 SynTest TurboScan 之 asicgen 來產生 ATPG pattern，請以 atpg pessimistic fault coverage 的值爲準

4 佈局前模擬

4-1. gate level simulation 是否有 timing violation？否

___ 有 setup time violation、___ 有 hold time violation

5 實體佈局

5-1. 使用之 P&R 軟體？ ___ Apolo、_v_ SOC Encounter

5-2. power ring 寬度？ 8um 是否已考量 current density(1mA/1um)？ 是

5-3. 是否考慮 output loading？ 是

5-4. 是否加上 Clock Tree？ 是

5-5. 是否加上 Corner pad？ 是

5-6. IO Buffer 間是否加上 IO Filler: 是 IO Filler 寬度: 48.37 um (建議至少需 12um 寬)

5-7. 是否加上 Core Filler？ 是

5-8. 是否上加 Bonding Pad？ 是

以下(A-1)爲使用 Apollo 者才須回答

A-1. 是否執行 Fill Notch and Gap 步驟？

以下(S-1 至 S-2)爲使用 SOC Encounter 者才須回答

S-1. power ring 上是否有 overlap vias？ 否

S-2. 是否確定 IO Row 和 Corner Row 互相貼齊？ 是

6 佈局後模擬

6-1. 是否做過 post-layout gate-level simulation？ 是

STA(static timing analysis) 軟體？ Modelsim

6-2. 是否做過 post-layout transistor-level simulation？ 是，sigma-delta modulator 有做

6-3. 已針對以下環境狀態模擬：v SS、v TT、v FF

6-4. 晶片取得時將以何種方式進行測試？將此晶片所需的直流電路接好，使用波形產生器產生不同的弦波輸入此晶片中，觀察其輸出，看其 spi 介面傳輸是否正確，再用邏輯分析儀將其輸出值抓出，再代回 matlab 中分析其輸出的時域值和頻域值是否正確。分析其解析度、有效 bit 數和線性度( INL & DNL )。

6-5. 模擬時是否考量輸出負載影響？ 是 若有輸出負載是: 20 pF (建議至少需 20pF)

7DRC/LVS 驗證

7-1. 是否有 DRC 錯誤？ 是 錯誤原因： OD.C.1 OD.C.5 RPO.C.3 RPO.C.6 以上四個爲 io pad 的假錯； PO.R.3 M1.R.1 M2.R.1 M4.R.1 M5.R.1 M6T.R.1 等的錯誤爲 poly 或 metel 層的 density 問題，因爲在數位電路部分，所有的 cell 還未填入，所以會有此些 density 的問題。

驗證 DRC 軟體？ Calibre

是否有不作 DRC 的區域？ 否

7-2. 是否有 LVS 錯誤？ 否

驗證 LVS 軟體？ Calibre

是否有非 CIC 提供的 BlackBox？ 是，有非 cic 提供的 BlackBox

8MT Form 填寫

8-1. 是否填上 v 系所單位、v 設計者姓名、v 聯絡電話(與手機) 、v 日期

8-2. 是否填上晶片上傳目錄？ v

8-3. 是否填上檔案名稱？ v

8-4. 是否寫上 top cell name？ v

9 使用 ARM926EJ or ARM7TDMI CPU IP

9-2. 若有使用 ARM926EJ /ARM7TDMI CPU IP，請提供以下訊息以便向 ARM 原廠申請 Design ID。

使用的 CPU 種類 (ARM926EJ or ARM7TDMI) :_____

使用的 metal layers 的層數:_____

佈局中 ARM926EJ /ARM7TDMI Macro 的 cell name:_____

這個晶片是否爲修訂版本(revision,也就是之前曾下線過相同晶片)？_____

若是修訂版本，前一次下線的晶片編號:_____

修訂版本的原因是？(例如修正 bug) _____

設計者簽名: 張孟修 指導教授簽名: 林進燈

# D SPI bus

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines. Sometimes SPI is called a “four wire” serial bus, contrasting with three, two, and one wire serial buses.


Figure D - 1: SPI bus with single slave and single master

The SPI bus specifies four logic signals.

1. SCLK (or SCK) --- Serial Clock (output from master).

2. MOSI/SIMO (or SDI or DI or SI) --- Master Output, Slave Input (output from master).

3. MISO/SOMI (or SDO or DO or SO) --- Master Input, Slave Output (output from slave).

4. SS (or CS) --- Slave Select (active low; output from master).

The SPI bus can operate with a single master device and with one or more slave devices. If a single slave device is used, the SS pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge of the slave select to initiate an action. With multiple slave devices, an independent SS signal is required from the master for each slave device. Most devices have tri-state outputs that become high impedance (“disconnected”) when the device is not selected. Devices without tri-state outputs can’t share SPI bus segments with other devices; only one such slave may talk

to the master, and only its chip select may be activated.

To begin a communication, the master first configures the clock, using a frequency less than or equal to the maximum frequency the slave device supports. Such frequencies are commonly in the range of 1-70 MHz.

The master then pulls the slave select low for the desired chip. If a waiting period is required then the master must wait for at least that period of time fefore starting to issue clock cycles.

During each SPI clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line; the slave reads it from that same line. The slave sends a bit on the MISO line; the master reads it from that same line. Not all transmissions require all four of these operations to be meaningful but they do happen.

Transmissions normally involve two shift registers of some giver word size, such as eight bits, one in the master and one in the slave; they are connected in a ring. Data is usually shifted out with the most significant bit first, while shifting a new least significant bit into the same register. After that register has been shifted out, the master and slave have exchanged register values. Then each device takes that value and does something with it, such as writing it to memory. If there is more data to exchange, the shift registers are loaded with new data and the process repeats.

Transmissions may involve any number of clock cycles. When there are no more data to be transmitted, the master stops toggling its clock. Normally, it then deselects the slave. Transmissions often consist of 8-bit words, and a master can initiate multiple such transmissions if it wishes/needs. However, other word sizes are also common, such as 16-bit words for touchscreen controllers or audio codecs; or 12-bit words for many digital-to-analog or analog-to-digital converters. Every slave on the bus that hasn’t been activated using its slave select line must disregard the input clock and MOSI signals, and must not drive MISO. The master selects only one slave at a

time.

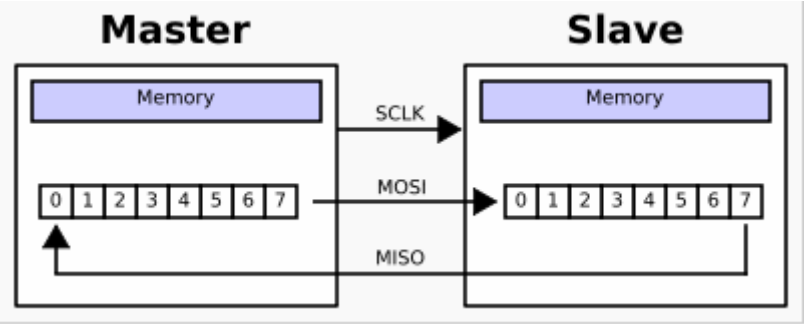



Figure D - 2: A typical hardware setup using two shift registers to form an inter-chip circular buffer

In addition to setting the clock frequency, the master must also configure the clock polarity and phase with respect to the data. Freescale's SPI Block Guide names these two options as CPOL and CPHA respectively, and most vendors have adopted that convention.

The timing diagram is shown to the below. The timing is further described below and applies to both the master and the slave device.

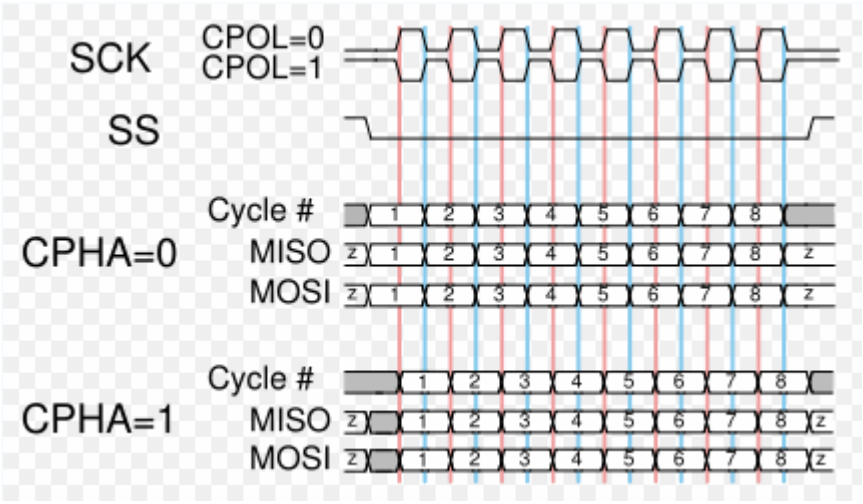



Figure D - 3: A timing diagram showing clock polarity and phase

- At CPOL = 0 the base value of the clock is zero.

(1) For CPHA = 0, data are read on the clock's rising edge and data are changed on a falling edge.

(2) For CPHA = 1, data are read on the clock's falling edge and data are changed on a rising edge.

- At CPOL = 1 the base value of the clock is one (inversion of CPOL = 0).

(1) For CPHA = 0, data are read on clock's falling edge and data are changed on a rising edge.

(2) For CPHA = 1, data are read on clock's rising edge and data are changed on a falling edge.

That is, CPHA = 0 means sample on the leading (first) clock edge, while CPHA = 1 means sample on the trailing (second) clock edge, regardless of whether that clock edge is rising or falling. Note that with CPHA = 0, the data must be stable for a half cycle before the first clock cycle. Also, note that no matter what the CPOL and CPHA modes say, the initial clock value must be stable before the chip select line goes active. This adds more flexibility to the communication channel between the master and slave.

The combinations of polarity and phases are often referred to as modes which are commonly numbered according to the following convention, with CPOL as the high order bit and CPHA as the low order bit:

| Mode | CPOL | CPHA |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

Figure D - 4: CPOL and CPHA of four modes of SPI bus

In the independent slave configuration, there is an independent slave select line for each slave. This is the way SPI is normally used. Since the MISO pins of the slaves are connected together, they are required to be tri-state pins.

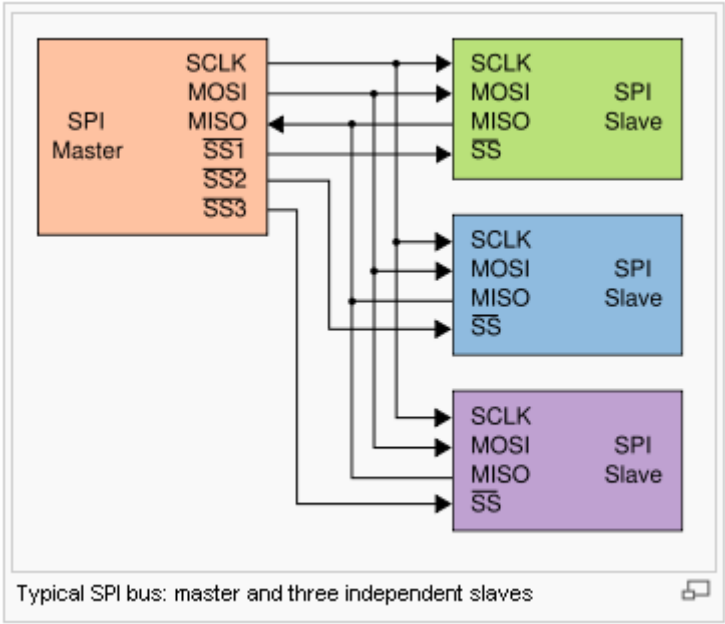



Figure D - 5: Typical SPI bus of a master and three independent slaves

There are the advantages of using spi bus:

1. Full duplex communication
2. Higher throughput than $I^2C$ or SMBus
3. Complete protocol flexibility for the bits transferred
   (1) Not limited to 8-bit words
   (2) Arbitrary choice of message size, content, and prupose
4. Extremely simple hardware interfacing
   (1) Typically lower power requirements than $I^2C$ or SMBus due to less circuitry (including pull-ups)
   (2) No arbitration or associated failure modes

(3) Slaves use the master’s clock, and don’t need precision oscillators

(4) Transceivers are not needed

5. Uses many fewer pins on IC packages, and wires in board layouts or connectors, than parallel interfaces

6. At most one “unique” bus signal per device (chip-select); all others are shared