A New Cryogenic CMOS Readout Structure for Infrared Focal Plane Array

Chih-Cheng Hsieh, Chung-Yu Wu, *Senior Member, IEEE*, and Tai-Ping Sun

***Abstract*— A new current readout structure for the infrared (IR) focal-plane-array (FPA), called the switch-current integration (SCI) structure, is presented in this paper. By applying the share-buffered direct-injection (SBDI) biasing technique and off focal-plane-array (off-FPA) integration capacitor structure, a high-performance readout interface circuit for the IR FPA is realized with a pixel size of 50×50 μm^2. Moreover, the correlated double sampling (CDS) stage and dynamic discharging output stage are utilized to improve noise and speed performance of the readout structure under low power dissipation. An experimental SCI readout chip has been designed and fabricated in 0.8-μm double-poly-double-metal (DPDM) n-well CMOS technology. The measurement results of the fabricated readout chip at 77 K with 4 and 8 V supply voltages have successfully verified both the readout function and the performance improvement. The fabricated chip has a maximum charge capacity of 1.12×10^8 electrons, a maximum transimpedance of 1×10^9 Ω, and ae active power dissipation of 30 mW. The proposed CMOS SCI structure can be applied to various cryogenic IR FPA's.**

***Index Terms*—CMOS integrated circuit, cryogenic electronics, focal plane array, readout circuit.**

I. Introduction

In the design of the infrared (IR) focal-plane array (FPA), high resolution has become a common requirement in many applications. This leads to large array format and small pixel size. Due to the small pixel size, it is difficult in the design of high-resolution large IR FPA's to implement complex high-performance readout input circuits (e.g., buffered direct injection (BDI) [1], [2], capacitive transimpedance amplifier (CTIA) [3], [4], and chopper-stabilized input circuit (CSI) [5]) with a large enough in-pixel integration capacitor. Usually one uses a simple readout circuit to maintain a large enough in-pixel capacitor. Thus, the readout performance (e.g., dynamic range and signal-to-noise ratio) is degraded. Moreover, the strict constraint on the unit-cell power dissipation also increases the difficulty to obtain the good readout performance in a large format IR FPA.

So far, several developed simple current readout schemes such as the direct injection (DI) [1], [6], [7], the source follower per detector (SFD) [8], [9], and the gate-modulation input (GMI) [8], [10], have been developed and have become commonly used structures in the IR FPA readout chip. In these readout schemes, a simple circuit is used to satisfy both pixel size and power dissipation limitations while sacrificing some readout performance such as the poor injection efficiency, the detector bias nonuniformity, and the noise figures. In the applications of long wavelength infrared (LWIR) detection, a large integration capacitor is needed because of the large amount of both background photons and dark currents in the photodiode. Thus, a large common off-focal-plane integration capacitor is used in the readout circuit to meet the requirement while minimizing the chip area [11], [12]. In performing the signal integration, the conventional multiplexed electronically scanned array (MESA) [11] is used to select the detector directly through MOS switches and the direct injection gate (DIG). In the operation, the inevitable switching noise is easily coupled to the detector bias. Moreover, using the DIG as a buffer, it has the constraints on detector bias stability and the same poor readout performance as in the DI readout circuit.

In this paper, a new current readout structure for the IR FPA, called the switch-current integration (SCI) structure, is proposed to solve the above mentioned problems and improve the readout performance. It has been shown from both simulation and experimental results that the proposed SCI readout structure can achieve good readout performance in a small pixel size through the use of the SCI technique, the off-FPA shared integration capacitors, and the previously proposed share-buffered direct injection (SBDI) input circuit [13], [14]. The circuit structure, readout strategy, and circuit performance of the new SCI readout structure are described in Section II. In Section III, both simulation results and experimental results of the fabricated SCI readout chip are presented. Finally, a conclusion is given.

II. Switch-Current Integration (SCI) Readout Structure

Fig. 1 shows the block diagram of the proposed SCI readout structure which is composed of three major parts: the unit-cell input stage, the shared off-FPA integration capacitor stage, and the common output stage. The circuit operation is explained as follows. The photon-generated current in the detector cell is buffered and switched one row at one time by the vertical row shift register to the shared off-FPA integration capacitor and integrated. After an integrating interval, the voltage signal is sampled, one column after the other by the horizontal column shift register to the common output stage serially. In the following, the detailed circuit structure and the operational principle of each block are described.

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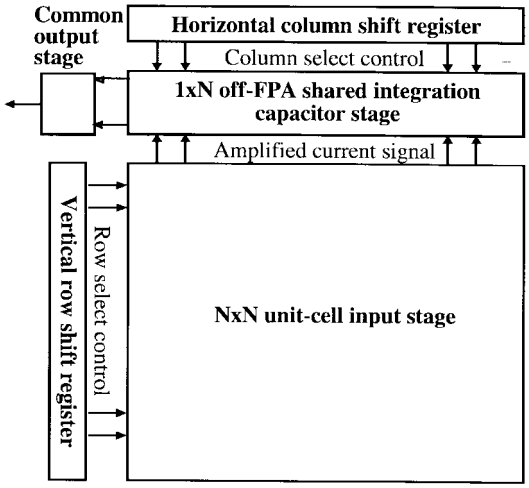

Fig. 1. The block diagram of the SCI readout structure.

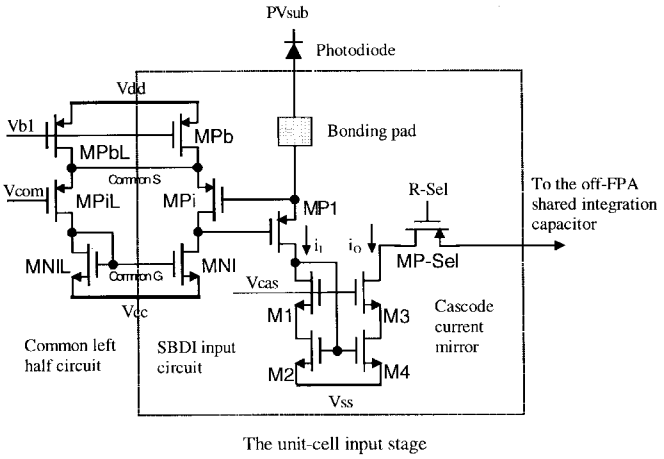

Fig. 2. The unit-cell input stage of the SCI readout structure with SBDI input circuit and cascode current mirror.

A. The Unit-Cell Input Stage

The circuit diagram of the proposed unit-cell input stage is shown in Fig. 2. In the new input stage, the previously proposed SBDI circuit [13], [14] is adopted and a cascode current mirror is used. As shown in Fig. 2, the SBDI circuit consists of the SBDI input circuit formed by the MOS devices MPb, MPi, and MNl in each pixel and the common left-half circuit formed by the MOS devices MPbL, MPiL, and MNlL and shared by all the pixels in one column. In the shared common left-half circuit, three common output bias lines $V_{b1} = 6.5$ V, commonS, and commonG are connected to the SBDI input circuits of all the pixels in the same column. The total power dissipation of the unit-cell input stage can be kept small because the bias current of the SBDI input circuit in each pixel is low. Moreover, the chip area can be kept small because only three MOSFET's are needed to realize the SBDI input circuit for each pixel. Due to the function of the SBDI differential amplifier, the detector bias at the anode of the photodiode can be stabilized to Vcom $= 6$ V through the virtual ground and the input impedance of the input MOS device MP1 can be decreased to obtain high injection efficiency. The high injection efficiency, good detector bias stability, low noise, good threshold uniformity, low power dissipation, and small chip area can be achieved in the unit-cell input stage by applying the SBDI interface design technique.

The photocurrent i_1 signal flowing through MP1 of the SBDI circuit is further mirrored to the row-select switch MP-Sel through the high-swing cascode current mirror M1–M4 as shown in Fig. 2. The current mirror can improve the detection sensitivity and avoid the noise coupling effect to the SBDI input circuit. Moreover, as compared to the conventional cascode current mirror, the high-swing cascode current mirror [15] increases output impedance and ratio accuracy while decreasing the required mirror output voltage to keep the output MOS devices in the saturation region.

The current ratio of i_o to i_1 of the current mirror is determined by the dimension ratio of the MOS devices M2 and M4, which is very stable [16]. The optimal gain of the current mirror can be determined for different input signal levels to achieve a maximum signal-to-noise ratio without integrating saturation on the capacitor. In this design, a current gain of ten is designed to achieve an optimal dynamic range for a maximum input current level of 50 nA.

The amplified pixel current signal at the output of the current mirror is switched to the off-FPA shared integration capacitor stage through the MOS switch MP-Sel controlled by the row select clock *R-Sel*. The current signal is integrated row by row in the integration capacitor stage.

Since only a simple cascode current mirror with four MOS devices and the SBDI input circuit with four MOS devices are used in the SCI unit-cell input stage, they occupy a small chip area. Thus, the pixel size can be small. Using the proposed SCI input stage, the readout performance in the high-resolution large-format IR FPA can also be improved.

B. The Shared Off-FPA Integration Capacitor Stage

As shown in Fig. 3, the shared off-FPA integration capacitor stage is composed of the integration capacitor C_{int}, the reset device Mres, and the isolation device Miso. In the SCI readout structure, the in-pixel integration capacitor is removed off the focal plane array and shared by one column of detector cells. Therefore, the pixel size limitation can be released. The maximum integration time of the SCI structure is $(\textit{frame} - \textit{read} - \textit{time})/N$, where N is the row number. Since the input referred noise is proportional to the square root of the integration time, a lowering factor $\sqrt{N}$ of signal-to-noise ratio might be introduced to this structure due to the limited integration time. However, the integrating operation usually does not occupy the whole frame-read-time in the conventional readout circuit. The integration time is usually shorter than frame-read-time and tunable to avoid the saturation on the limited integration capacitance, especially in the high background flux operation. Thus, the lowering factor of signal-to-noise ratio in this structure is less than $\sqrt{N}$. Moreover, the lowering of signal-to-noise ratio due to the limited integration time can be compensated for by the current gain of the front stage and the increasing integration capacitance.

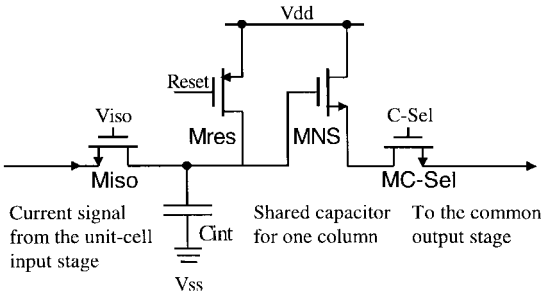

Fig. 3. The shared off-focal-plane integration capacitor stage of the SCI readout structure.

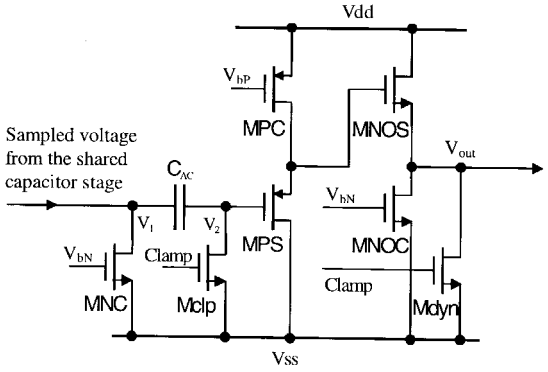

Fig. 4. The common output stage of the SCI readout structure with both clamping and dynamic discharging circuits.

The isolation device Miso and the isolation voltage $V_{\rm iso} = 3.5$ V are used to isolate the clock feedthrough of the row-select clock *R-Sel*, which is coupled to the integration capacitor $C_{\rm int}$. The minimum voltage on the integration capacitor during discharging can also be controlled by the isolation voltage $V_{\rm iso}$ to maintain the proper working region of the current mirror.

The charge storage capacity can be enlarged by designing a large off-focal-plane integration capacitor without increasing the pixel size. The well charge capacity of the readout circuit is

$$\text{Well Capacity} = \frac{V_{\max} \cdot C_{\rm int}}{q} \tag{1}$$

where $V_{\max}$ is the maximum integration voltage of the capacitor $C_{\rm int}$ and q is the unit charge. The dynamic range of the readout circuit is defined as the ratio of well capacity to total noise. It can be expressed as

$$\text{Dynamic Range} = \frac{\text{Well Capacity}}{\text{Noise}} \tag{2}$$

where the noise in the denominator is the total noise electrons of the photon noise, the detector thermal noise, and the readout circuit noise. When operating with large background flux, the noise is dominated by the photon noise which is independent of the integration capacitance. Thus, the dynamic range is proportional to the well capacity, that is, the integration capacitance as may be seen from (1) and (2). When operating with small background flux, the noise contribution of integration capacitor becomes significant. The noise charge contributed by the integration capacitor is the kTC noise which is generated by the trapping of the switch thermal noise in the integration-reset function. The kTC noise can be expressed as [17]

$$\text{kTC Noise} = \left(\frac{\text{kT}C_{\rm int}}{q^2}\right)^{1/2}. \tag{3}$$

From (1)–(3), it can be shown that the dynamic range is proportional to the square root of the integration capacitor under small-background-flux operation.

From the above analysis, it can be seen that the dynamic range can be improved by increasing the integration capacitor. In the proposed technique of a shared integration capacitor, large integration capacitance can be easily designed by extending the capacitor size along the direction vertical to the pixel pitch. Thus, high dynamic range can be obtained without increasing the pixel size. Moreover, under the fixed integration time, the integration speed is tunable by changing the integration capacitance through the switching of several parallel on-chip capacitors. Thus, the SCI structure can be used in a wide range of background currents or dark currents without the saturation problem in the current integration.

The integrated voltage signal of the shared off-FPA capacitor stage is sampled to the common output stage column by column serially after the integration interval through the NMOS switch MC-Sel controlled by the column select control signal *C-Sel*. The N-type source follower constructed by MNS in Fig. 3 and the current source in the common output stage is used as a unit-gain buffer between shared integration capacitor stage and common output stage.

C. The Common Output Stage

In the common output stage, as shown in Fig. 4, the NMOS MNC with the dc gate bias $V_{bN} = 2$ V is the NMOS current source load of the source follower MNS in Fig. 3 when the switch MC-Sel is ON. The correlated double sampling (CDS) function is realized by the MOS switch MC-Sel, the clamp device Mclp, and the ac coupling capacitor $C_{\rm ac}$. The PMOS devices MPS and MPC form a P-type source follower with the dc bias voltage $V_{bP} = 6$ V. The NMOS device MNOS and MNOC form an N-type source follower which serves as the output buffer. The NMOS Mdyn is the dynamic discharging device. The dc biases such as the detector common voltage $V_{\rm com}$, the cascode gate dc voltage $V_{\rm cas}$, and the isolation voltage $V_{\rm iso}$ are given directly from the off-chip regulator. On the other hand, in order to monitor the internal current of the gate, those dc biases of current sources such as the op amp V_{b1} and the N-type (P-type) source follower V_{bN} (V_{bP}) are given through on-chip current mirrors and bias from the drain node of slave MOS. The additional power consumption of the current mirrors is included in the total active power dissipation.

The CDS function of the common output stage is described below. At time T_1, the sample clock *C-Sel* in Fig. 3 and the clamping clock *Clamp* are high and the clamp device Mclp is ON. The first sampled voltage signal is charged on the ac coupling capacitor $C_{\rm ac}$ and the voltages of V_1 and V_2 at time T_1 are

$$V_1(T_1) = V_{dd} - V_{\rm int} - V_{\rm GSN} \tag{4a}$$

$$V_2(T_1) = 0 \tag{4b}$$

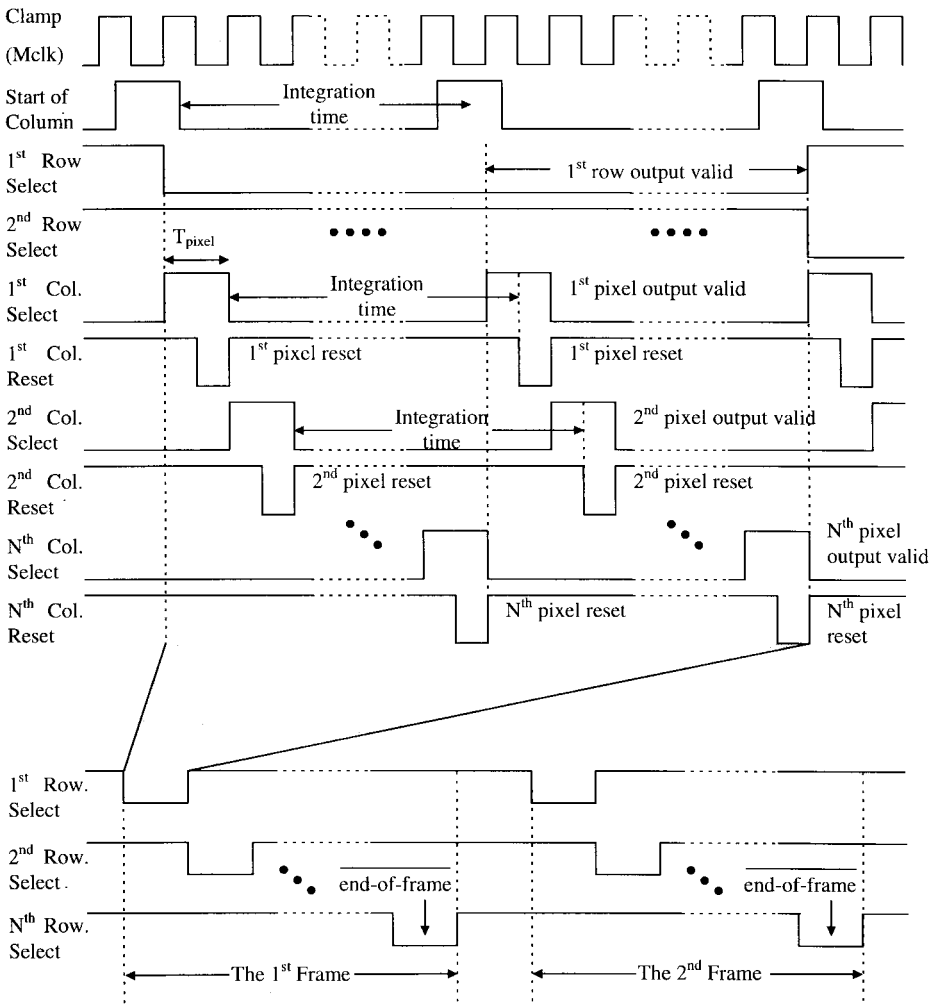

Fig. 5. The clock timing waveforms of master clock (*Mclk*), clamping control (*Clamp*), row select (*R-Sel*), column select (*C-Sel*), and end-of-frame.

where $V_{\rm int}$ is the integrated voltage signal on the capacitor and $V_{\rm GSN}$ is the voltage drop of the N-type source follower composed of the devices MNS and MNC. At time T_2, the clamp device Mclp is turned OFF before the internal integration capacitor is reset. Then the integrated node is reset to V_{dd} and the second sampled voltage $V_1(T_2)$ becomes

$$V_1(T_2) = V_{dd} - V_{\rm GSN} \tag{5}$$

since the charges on the ac coupling capacitor $C_{\rm ac}$ are the same at T_1 and T_2. From (4) and (5), we have

$$C_{\rm ac}[V_1(T_1) - V_2(T_1)] = C_{\rm ac}[V_1(T_2) - V_2(T_2)]. \tag{6}$$

Thus, the output signal $V_2\ (T_2)$ after the CDS is

$$V_2(T_2) = V_{\rm int}. \tag{7}$$

The net voltage $V_2\ (T_2)$ is sent to the P-type source follower. This realizes the CDS function [18]–[20].

The P-type source follower MPS and MPC and the N-type source follower MNS and MNC form a complementary cascaded source-follower stage which can obtain a nearly zero dc offset by properly compensating their gate-source threshold voltages. In the output buffers MNOS and MNOC, the dynamic discharge device Mdyn is used to save the static power dissipation and maintain the proper readout speed [14].

D. The SCI Chip Operation

There are six dc bias voltages in the SCI chip. Array them, the detector common voltage $V_{\rm com}$, the cascode gate dc voltage $V_{\rm cas}$, and the isolation voltage $V_{\rm iso}$ are given directly from the off-chip regulators. On the other hand, in order to monitor the internal current of the gate, the op amp bias voltage V_{b1} and the N-type (P-type) source-follower bias V_{bN} (V_{bP}) are provided through on-chip current mirrors with the external bias voltages applied to the drain node of slave MOS devices. The additional power consumption of the current mirrors is included in the total active power dissipation.

The clock timing waveforms of the master clock *Mclk*, column start signal, row select *R-Sel*, column select *C-Sel*, and clamping control *Clamp* are shown in Fig. 5 where the clock signal has a high level of 8 V and a low level of 0 V. The readout operation of the SCI chip is described below. When the first row select *R-Sel* is low and the first column select *C-Sel* is high, the unit-cell input stage of the first row is switched to the shared integration capacitor and the first column in the first row is selected and reset. After an integration time $T_{\rm int}$ controlled

by the column reset signal, the first column select signal *C-Sel* is high again and the voltage signal of the first column in the first row is sampled to the output stage. The integration time is defined as the high level time interval between two column reset signals as shown in Fig. 5. The integration capacitor is reset immediately after it is sampled. Then the second pixel of the first row is read out serially. After all pixels in the first row have been readout, the second row select *R-Sel* is low and then the second row is switched to the integration capacitor. The minimum integration time is $N \times T_{\text{pixel}}$ where N is the column number and T_{pixel} is the pixel processing time defined by the time when the column select clock is high. When the Nth row is selected, the row select signal is invited to form the end-of-frame signal which indicates the first frame has been read out. Then the second frame is read out.

III. Simulation and Experimental Results

The SPICE simulation results of the waveforms of integration voltage V_{int} during the integration time $T_{\text{int}} = 128\ \mu$s in the SCI readout circuit with the input current signals 5 nA, 15 nA, 25 nA, 35 nA, 45 nA, and 55 nA and the integration capacitor 1 pF are shown in Fig. 6 where the device parameters of 0.8-μm double-poly-double-metal (DPDM) n-well CMOS technology at 77 K are used and the simulations are performed at 77 K. As shown in Fig. 6, the discharging rate is proportional to the input current. The minimum discharging voltage on the integration capacitor C_{int}, which is controlled by the isolation NMOS device M_{iso}, can reach 2 V at the 8 V power supply. The output waveforms of node voltage V_1 and output voltage V_{out} in the common output stage are shown in Fig. 7. As shown in Fig. 7, when *Clamp* is high during $T_{\text{pixel}}, V_{\text{out}}$ is clamped to 0.3 V. When *Reset* is low during T_{pixel}, V_1 is reset to 5.5 V. These two operations realize both clamping and dynamic discharging functions. The simulation readout speed can reach 1 MHz under 30 mW power dissipation at a 45 pF output loading and 8 V supply with 64 $\times$ 64 format. The readout speed is defined as the reciprocal of the pixel processing time $(1/T_{\text{pixel}})$. It is evidently shown in Fig. 7 that the summation of the rising and falling time is less than 200 nS, and thus, the maximum readout speed can be as high as 2 MHz to fit different system requirements.

An experimental 64 $\times$ 64 SCI readout chip has been designed and fabricated to verify the proposed new CMOS SCI readout structure. The block diagram of the 64 $\times$ 64 SCI readout chip is shown in Fig. 8. The 64 common left-half circuits for 64 columns are placed at the bottom of the chip and three vertical bias lines are used in each common circuit to connect the bias voltages to the SBDI input circuit in each pixel in the same column. This layout arrangement makes the buffer of the SBDI input circuit isolated for each column when one row is selected. Thus, the noise coupling can be avoided to improve the readout performance. The 64 shared integration capacitor stages are placed at the top of the chip. The normal integration capacitance is 1 pF. An extra capacitor of 1 pF with a MOS switch conveniently laid along vertical direction and in parallel with the 1 pF normal integration capacitor. Through

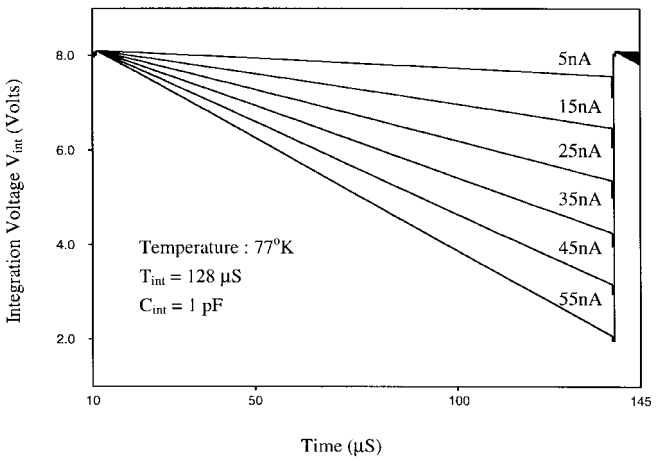

Fig. 6. The simulated discharging waveforms of the SCI integration capacitor C_{int} with the input currents from 5 nA to 55 nA with 10 nA step.

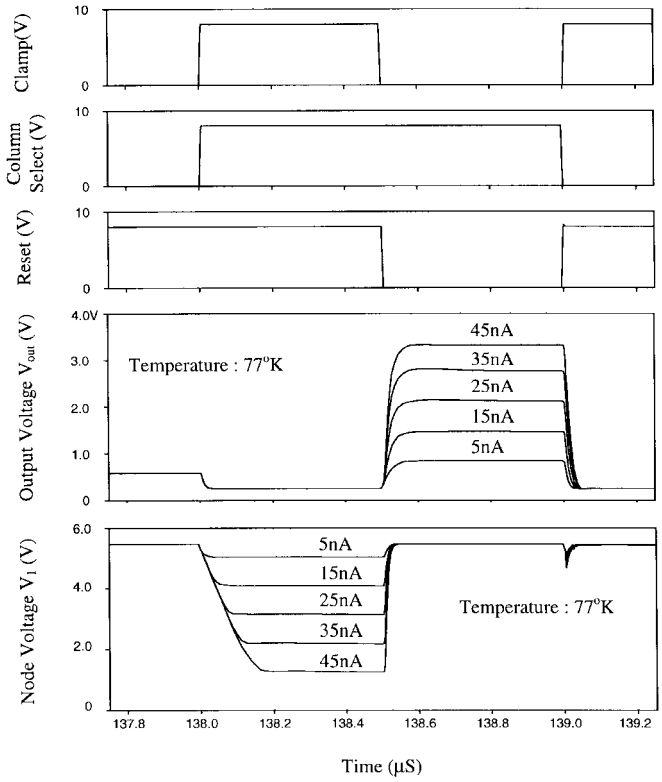

Fig. 7. The simulated waveforms of V_1 and V_{out} in the common output stage with input currents from 5 nA to 45 nA with 10 nA step.

the MOS switch, the integration capacitance is tunable to 2 pF. The total layout area for the two capacitors is 50 $\times$ 80 μm using the interpoly capacitance of the double-poly technology. Some noise shielding techniques for mixed-mode IC's are used in the proposed SCI readout chip, such as the separation of the analog and digital power line, the different analog and digital ground, the independent substrate bias line [14], [21], and the low-pass filters of input pads.

The photographs of the 64 $\times$ 64 SCI readout chip fabricated in 0.8-μm double-ploy-double-metal (DPDM) n-well CMOS technology is shown in Fig. 9. This chip is designed to work under 4 and 8 V power supplies. The chip is packaged properly

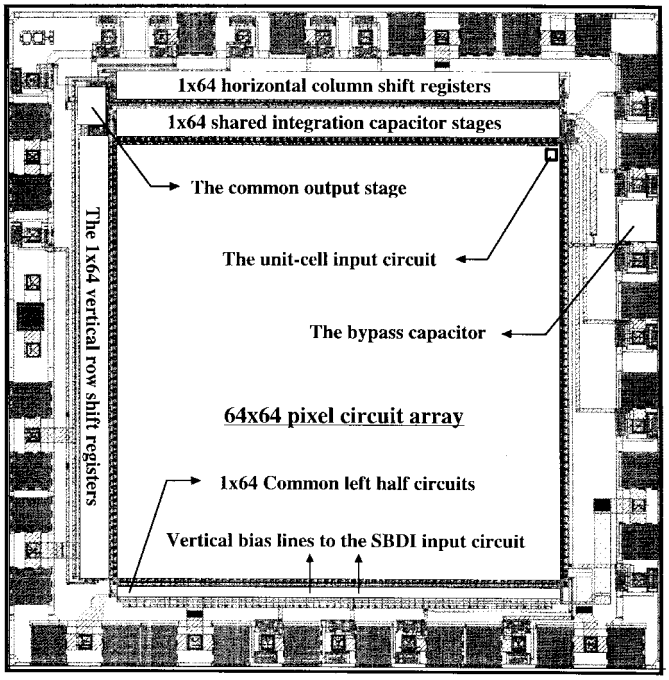

Fig. 8. The block diagram of the layout of the 64 × 64 SCI readout chip.

in a vacuum dewar and tested under a 77 K environment with liquid hydrogen as the cooling source. All power supplies and voltage bias are connected to the chip from an external board. The maximum charge capacity can achieve 1.12 × 10^8 electrons by designing a 2-pF integration capacitor with 1-pF stray capacitance which is caused by the long signal path of the column line. On-chip testing current sources are used to simulate the photocurrents of IR detectors and the experimental results are shown in Figs. 10–12. In Fig. 10, the $V_{\rm out}$ waveforms of two frame cycles are measured with the end-of-frame signal. The measured $V_{\rm out}$ waveforms under different input currents are shown in Fig. 11. The uniformity of the fabricated SCI readout chip as shown in Fig. 11 is expected to be better than 98% limited by the accuracy of on-chip testing current sources. Fig. 12 shows the measured $V_{\rm out}$ waveforms of a single pixel under different integration times from 300 to 900 μs. As shown in Fig. 12, the maximum output swing is 3 V. The measured output voltage $V_{\rm out}$ versus integration time is shown in Fig. 13 where the integration time is changed from 200 to 900 μs. It is shown that the linearity performance of the SCI readout chip is better than 99%. The measured performances of the fabricated SCI readout chip are summarized in Table I. The transimpedance can be as high as 1.3 × 10^9 with a current gain of ten at the unit cell current mirror. The total active chip power consumption is below 30 mW at 77 K.

TABLE I
TEST RESULTS AND OPERATION CONDITIONS FOR THE FABRICATED SWITCH-CURRENT-INTEGRATION (SCI) 64 × 64 READOUT CHIP

Detector Interface Circuit	Share-Buffered Direct-Injection
Power supply	4 V, 8 V
Pixel pitch	50 × 50 μm^2
Maximum Integration capacitance	3 pF
Maximum output swing	3 V
Maximum charge capacity	1.12 × 10^8e$^-$
Maximum readout speed	2 MHz
Linearity	99%
Maximum Transimpedance	1.3 × $10^9\Omega$
Active Power dissipation	30 mW
Operating temperature	77 K
Technology	0.8 μm DPDM n-well CMOS

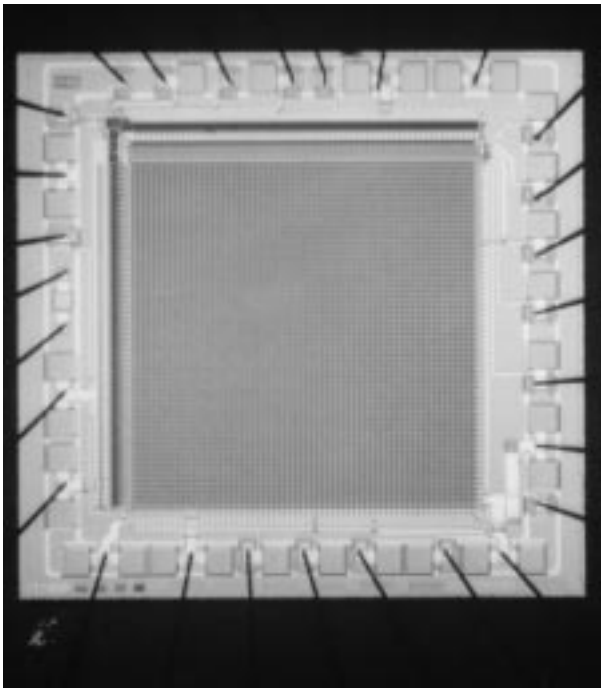

Fig. 9. The photograph of the fabricated 64 × 64 SCI readout chip.

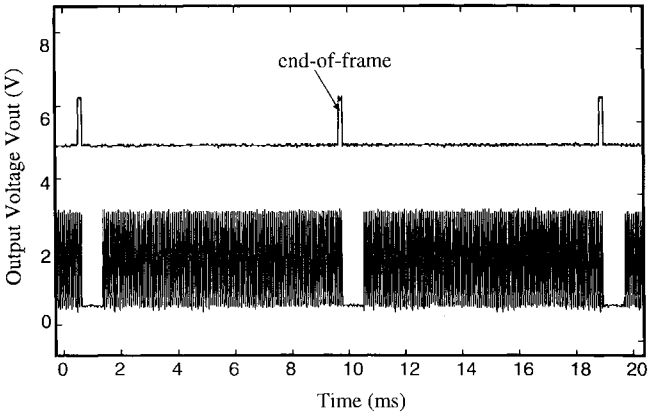

Fig. 10. The measured $V_{\rm out}$ waveforms of the fabricated 64 × 64 SCI readout chip at 77 K during the two-frame period with the end-of-frame control signal.

IV. CONCLUSION

In this paper, a new SCI readout structure for IR FPA is proposed, analyzed, and experimentally verified. In the new CMOS SCI readout structure, the design techniques of the SBDI interface, the cascode current mirror for buffering and current mode gain, the off-FPA integration capacitor, and the dynamic discharging output stage with the CDS are used to release the pixel pitch limitation in the conventional structures and achieve good readout performance. Besides the inherent

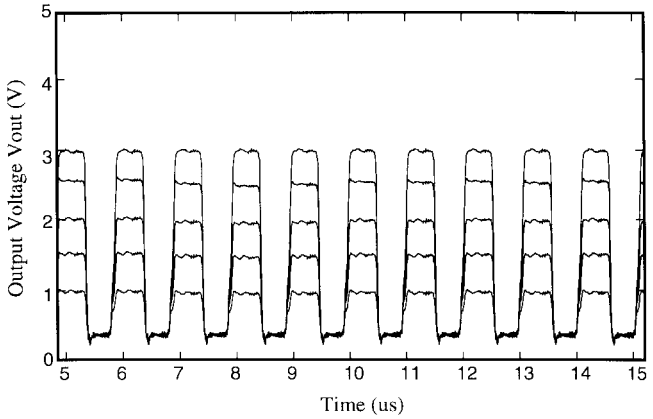

Fig. 11. The measured $V_{\rm out}$ waveforms of the 64 × 64 SCI readout chip at 77 K under different input currents.

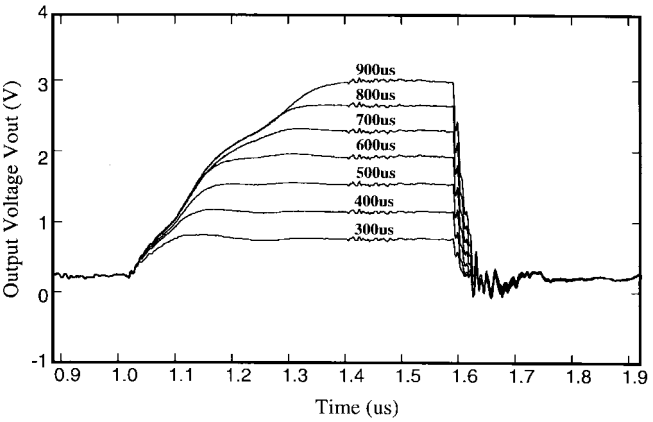

Fig. 12. The measured $V_{\rm out}$ waveforms of a single pixel on the readout chip at 77 K for different integration times from 300 to 900 μs.

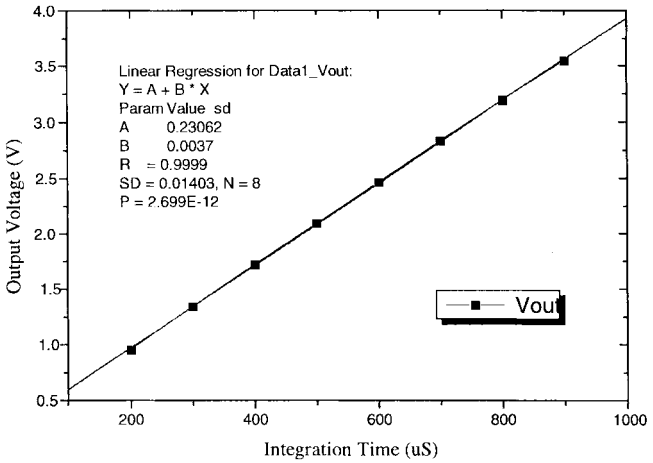

Fig. 13. The measured linearity of the 64 × 64 SCI readout chip at 77 K.

high injection efficiency, low noise, good threshold uniformity, and the stable detector bias performance as in the SBDI interface, the new SCI readout structure also has a large storage capacity, high dynamic range, and good detector sensitivity performance with a small pixel size. The inherent advantages of the low power and small pixel size make it suitable for the application of the high-performance readout input circuit design of the high-density large-format IR FPA. The function and performance of the proposed new SCI readout structure has been verified by HSPICE simulation and the measurement on a 64 × 64 format experimental chip.

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