國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用改良式無負載架構之8位元100百萬赫茲取樣互補式金氧半導管式類比數位轉換器

An 8-bit 100MS/s CMOS Pipelined ADC With Improved Loading-Free Architecture

研究生：夏竹緯

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中 華 民 國 九十七 年 九 月

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國 立 交 通 大 學

電 信 工 程 學 系 碩 士 班

碩 士 論 文

A Thesis

Submitted to Department of Communication Engineering

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master

in

Communication Engineering

September 2008

Hsinchu, Taiwan.

中華民國九十七年九月

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摘要

有著高速、中解析度及低功率的特性，導管式類比數位轉換器被廣泛使用於通訊及影像訊號處理等商業應用。於此篇論文中，一個嶄新的改良式無負載架構被提出。此架構可增加導管式類比數位轉換器中倍乘式數位類比轉換器的頻寬，進而提升轉換速率。此外，藉由在鄰近兩級間使用運算放大器共用技術，功率消耗及晶片面積也可被有效降低。應用上述兩種技術，數位類比轉換器可達到較高轉換速率且消耗較低功率。

在此篇論文中，兩個導管式數位類比轉換器被設計於台積電 0.18 微米互補式金氧半製程。第一個設計是一個應用運算放大器共用技術 10 位元每秒 100 百萬取樣導管式數位類比轉換器，第二個設計是一個應用改良式無負載架構及運算放大器共用技術之 8 位元每秒 100 百萬取樣導管式數位類比轉換器。採用每級 1.5 位元的架構以獲得較高的操作速度，所以此類比數位轉換器主要包含一個前端取樣保持電路、八個(或六個)串接 1.5 位元單級和最後一級的 2 位元快閃式轉換器。所有類比電路皆以全差動架構設計，而在 1.8 伏特供應電壓下擁有峰對峰值 1.6 伏特的輸入擺幅。在每秒 100 百萬取樣及 5 百萬赫茲輸入訊號下，第一個設計可達到 59.95dB 訊號對雜訊及失真比 (SNDR), 71.18dB 無寄生動態範圍(SFDR)及 9.67 有效位元(ENOB)。 最大差動非線性誤差 (DNL)為 0.4LSB 而最大積分非線性誤差 (INL)為 1.07LSB。在每秒 100 百萬的取樣速度下功率消耗為 72.6 毫瓦而晶片面積為 1.95 毫米平方。而在每秒 100 百萬取樣及 10 百萬輸入訊號下，第二個設計可達到 46.98dB 訊號對雜訊及失真比 (SNDR), 57.24dB 無

寄生動態範圍 (SFDR)及 7.51 有效位元(ENOB)。 最大差動非線性誤差 (DNL)為 0.38LSB 而最大積分非線性誤差 (INL)為 0.88LSB。在每秒 100 百萬的取樣速度下功率消耗為 78 毫瓦而晶片面積為 1.89 毫米平方。

An 8-bit 100MS/s CMOS Pipelined ADC With Improved Loading-Free Architecture

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Abstract

With high-speed, medium-resolution, and low-power characteristics, pipelined analog-to-digital converters (ADCs) are very popular for a wide variety of commercial applications, including data communications and image signal processing. In this thesis, a newly improved loading-free architecture is proposed. It much enhances the bandwidth of the multiplying digital-to-analog converter (MDAC) circuit in pipelined ADC, and thus the conversion rate can be speeded up. Besides, the power consumption and chip area can also be reduced efficiently by using the opamp-sharing technique between two successive stages. With above two techniques, the ADC can achieve much higher conversion rate and consume less power.

In this thesis, there are two pipelined ADCs implemented in TSMC 0.18-μm CMOS process. The first design is a 10-bit 100MS/s pipelined ADC with opamp-sharing technique, and the second design is an 8-bit 100-MS/s pipelined ADC with both improved loading-free architecture and opamp-sharing technique. To achieve higher operation speed, the 1.5-bit/stage architecture is adopted, and thus these ADCs mainly consist of one front-end S/H, eight (or six) cascaded 1.5-bit stages, and a 2-bit flash ADC in the last stage. All analog circuits are fully differential with a 1.6Vpp input signal swing at 1.8-V supply voltage. The first design achieves 59.95dB SNDR, 71.18dB SFDR, 9.67bit ENOB for a 5-MHz input signal at 100-MS/s. The maximum DNL is 0.4LSB and the maximum INL is 1.07LSB. The power consumption at 100MS/s sampling rate is 72.6 mW and the chip size is 1.95mm^2. The

second design achieves 46.98dB SNDR, 57.24dB SFDR, 7.51bit ENOB for a 10-MHz input signal at 100-MS/s. The maximum DNL is 0.38LSB and the maximum INL is 0.88LSB. The power consumption at 100MS/s sampling rate is 78 mW and the chip size is 1.89mm^2.

誌謝

隨著這份碩士論文的完成，兩年來在交大的求學生活也即將告一段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，首先，要感謝我的指導教授洪崇智老師在我兩年的研究生活中，對我的指導與照顧，並且在研究主題上給予我寬廣的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授和羅天佑學長撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

另一方面，要感謝所有類比積體電路實驗室的成員兩年來的互相照顧與扶持。首先，感謝博士班的學長羅天佑、薛文弘和黃哲揚以及已畢業的碩士班學長何俊達、邱建豪、林明澤、廖德文、白逸維、高正昇和吳國璽在研究上所給予我的幫助與鼓勵，尤其是俊達學長和建豪學長，由於他平時不吝惜的賜教與量測晶片時給予的幫助，使得我的論文研究得以順利完成。另外我要感謝林永洲、楊文霖、郭智龍、邱楓翔，黃介仁和張維欣等諸位同窗，透過平日與你們的切磋討論，使我不論在課業上，或研究上都得到了不少收穫。尤其是工四718實驗室的同學們，兩年來陪我一塊兒努力奮鬥，一起渡過同甘苦的日子，也因為你們，讓我的碩士班生活更加多采多姿，增添許多快樂與充實的回憶。此外也感謝學弟們簡兆良、許新傑、李尚勳和黃聖文的熱情支持，因為你們的加入，讓實驗室注入一股新的活力與朝氣。

到這邊，特別要致上最深的感謝給我的父母及家人們，謝謝你們從小到大所給予我的栽培、照顧與鼓勵，讓我得以無後顧之憂地完成學業，朝自己的理想邁進，衷心感謝你們對我的付出。

最後，所有關心我、愛護我和曾經幫助過我的人，願我在未來的人生能有一絲的榮耀歸予你們，謝謝你們。

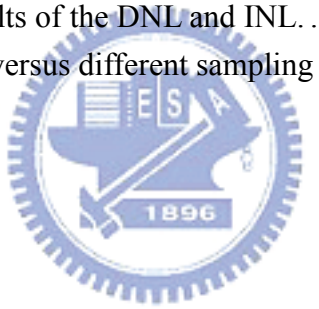
夏竹緯 于 交通大學工程四館 718 實驗室

2008.8.21

Table of Contents

List of Figures

Figure Page



List of Tables

Table Page

Chapter 1

Introduction

1.1 Motivation

For many applications, such as audio, video and communication system, a large number of data have to be processed. However, it would consume much hardware and large power by using analog circuits. In order to acquire low power consumption and cost reduction, digital signal processing (DSP) is becoming more and more popular. Usually, the input and output signals of the system are inherently analog in many applications, but the signal processing in the system is digital. Therefore, analog to digital converters (ADCs) and digital to analog converters (DACs) are the necessary interfaces in the system.

High-speed analog-to-digital converters (ADCs) are important elements in a wide variety of commercial applications including data communications and image signal processing. When applications require integration of multiple on-chip ADCs in the analog front-end with digital signal processors, the reduction of both power consumption and chip area is an important design issue. Among many ADC architectures suitable for baseband data communication or video applications, pipelined ADCs have proven to very efficient for meeting the high speed, medium resolution, and lower power consumption requirements. The reason that the pipelined ADC can be so efficient is due to its concurrency of operation. The sample-and-hold amplifiers (SHAs) are used at the first stage to sample the residue output from the previous circuit block. This feature allows each pipelined stage to process a new sample as soon as its residue is sampled by the following stage, and also allows all

stages to operate concurrently, giving a throughput of one output sample per clock cycle. Thus, pipelined ADCs can operate at high sample rates with high efficiency in terms of power and chip area [1]-[3].

In this research, the improved loading-free architecture is proposed, which has higher feedback factor and less output loading capacitance in the multiplying digital-to-analog converter (MDAC) circuit. With higher close-loop bandwidth, the ADC can operate in higher conversion rate. Even operating in normal speed, the high bandwidth architecture would have less power consumption. Besides, the opamp-sharing technique is also used in the design. By sharing a opamp between two successive stages, the number of required opamp for whole ADC can be reduced almost half, thus the area and power consumption would be more efficient. Finally, a 10-bit 100MS/s pipelined with opamp-sharing technique, and an 8-bit 100MS/s pipelined ADC with improved loading-free architecture and opamp-sharing technique are implemented in TSMC 0.18-μm CMOS process.

1.2 Thesis Organization

This thesis is organized into six chapters.

Chapter 1 briefly describes the motivation of this thesis.

Chapter 2 begins with the fundamental concepts of analog-to-digital conversion and performance metrics used to characterize ADCs. Then, several Nyquist-rate ADC architectures are introduced. The evolutions and properties for different ADCs are described.

Chapter 3 concentrates on the detail operation principle and the calibration techniques of pipelined ADCs. Then, the most popular 1.5-bit/stage structure for pipelined ADC is presented, which is very suitable for high speed and low power design. For even more enhancing the performance, the proposed improved loading-free architecture is developed to speed up the ADC and opamp-sharing technique is used for better area and power efficiency. A summary is placed in the last to describe the whole pipelined ADCs with above two techniques.

Chapter 4 illustrates the designs and implementations of the circuit blocks used in the proposed pipelined ADCs. First, the analog blocks, such as MDAC and Sub-ADC, are described. The core components like opamp and comparator are discussed deeply. Then, the digital blocks like digital error correction logic and clock generator are introduced. The transistor level simulation results of each circuit are also presented. Finally, the layouts of the proposed pipelined ADCs are shown with their floor plans.

Chapter 5 presents the measurement environment, including the required instruments and component circuits on the DUT board. The measured results of the pipelined ADC with opamp-sharing technique described in Chapter 3 and Chapter 4 are shown and summarized.

Finally, Chapter 6 is the conclusions of this work. Some suggestions and improved recommendations are proposed for the future work.

Chapter 2

Overview of Analog-to-Digital Converters

2.1 Introduction

This chapter first introduces the concept of ideal analog-to-digital converters and the performance metrics which are useful to determine the quality of the ADCs. In the following section, some Nyquist-Rate ADC architectures are introduced and their characteristics are described. These architectures are developed for differential requirement such as speed, resolution, power consumption and area. The techniques used to cancel the various error sources for several architectures are also introduced.

2.2 Fundamental Aspects of A/D Converters

A analog-to-digital converter connects the continuous analog signal and the discrete digital word. In the beginning, the ideal behavior of the conversion is introduced. Following, the quantization noise caused by the quantization error is also discussed, since it is the dominate noise source of a analog-to-digital converter. In the final section, the performance metrics, which obviously indicate the quality of ADCs, are described.

2.2.1 Ideal A/D Converter

A ideal analog-to-digital converter tend to quantize the analog input signal into an N-bit digital word is shown in Figure 2.1, where B_{out} is the digital output word while V_{in} and V_{ref} are the analog input and reference signals, respectively. That is, the full range of analog input signal is divided into several uniform levels according to the number of quantization steps,

$$Number\ of\ quantization\ steps\ =\ 2^N \tag{2.1}$$

and each level width is defined as

$$V_{LSB} = \frac{V_{ref}}{2^N} = 1\ LSB \tag{2.2}$$

In the other word, the input full range is divided into 2^N uniform levels, and each level is related to a digital output word, B_{out}. We also define $b_{N\text{-}1}$ as the most significant bit (MSB) and b_0 as the least significant bit (LSB).

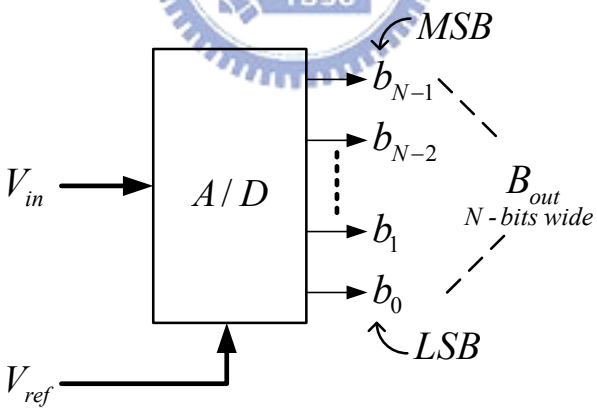


Figure 2.1 Ideal analog-to-digital converter.

For an A/D converter, the following equation relates these signals,

$$V_{ref}\left(b_{N-1}2^{-1} + b_{N-2}2^{-2} + \cdots + b_0 2^{-N}\right) = V_{in} + V_x, \quad \text{where } -\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB} \tag{2.3}$$

Note that V_x also known as *quantization error* is the difference between the analog input signal and the quantized output signal [4][5].

2.2.2 Quantization Noise

As mentioned above, quantization errors occur even in ideal A/D converter. We can make a linear model for the quantized output signal, $V_{staircase}$, which is equal to the analog input signal, V_{in}, subtract the quantization noise signal, V_Q, as shown in Figure 2.2.

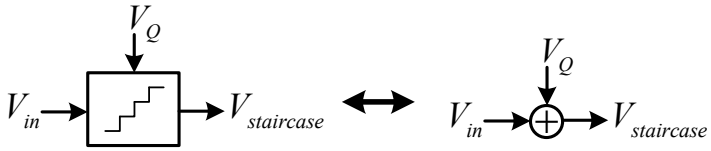


Figure 2.2 Linear model for the quantized output signal.

The quantization noise signal is defined as the difference between the actual analog input and the quantized output signal, and can be represented as

$$V_Q = V_{in} - V_{staircase} \tag{2.4}$$

Figure 2.3 (a) shows the transfer curve for an ideal 3-bit ADC and the corresponding quantization noise is shown in Figure 2.3 (b) [6]. Note that the quantization noise is limited to $\pm V_{LSB}/2$.

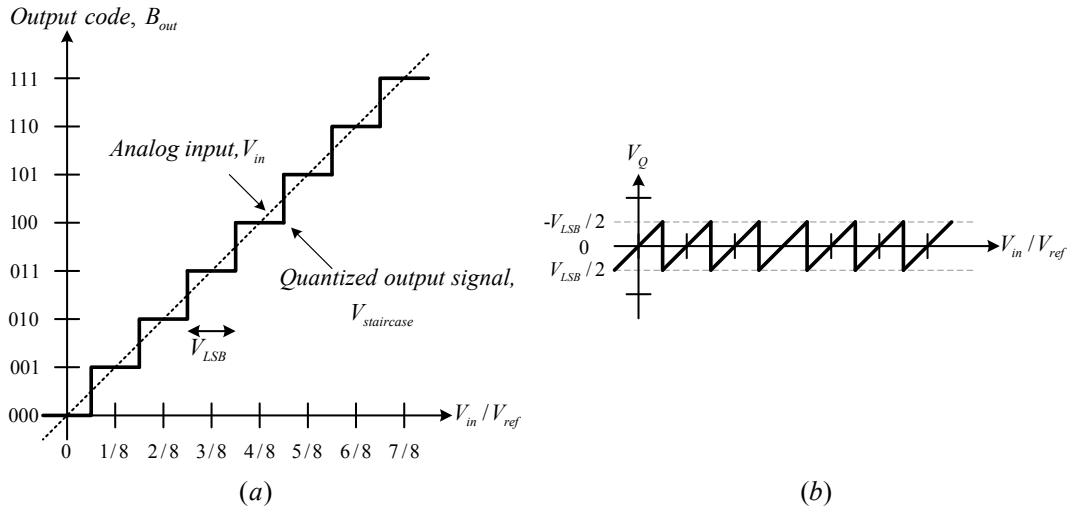


Figure 2.3 (a) Transfer curve for an ideal 3-bit ADC and

(b) its corresponding quantization error.

In a stochastic approach, we assume that the input signal is varying rapidly such that the quantization noise signal, V_Q, is a random variable uniformly distributed between $\pm V_{LSB}/2$. The probability density function for such an noise signal, $f_Q(q)$, will be a constant value, as shown in Figure 2.4. Hence, the quantization noise power, P_Q, is given by

$$P_Q = \int_{-\infty}^{\infty} q^2 f_Q(q)\,dq = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} q^2 dq = \frac{{V_{LSB}}^2}{12} \tag{2.5}$$

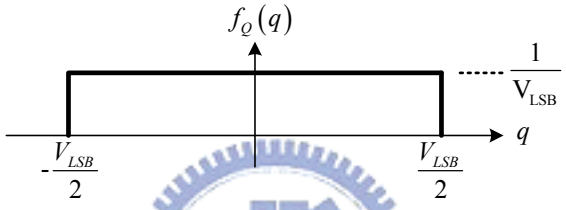


Figure 2.4 Probability density function of quantization noise.

2.2.3 Performance Limitations

Before proceeding, it is required to know the performance metrics for determining the transfer response of the data converters. In this section, some commonly used terms characterizing the performance of data converters are introduced as below.

2.2.3.1 Resolution

The resolution of an ADC is defined to be the number of the distinct input segments corresponding to the different output word. It also indicates the minimal difference of the input signal that can be recognized by the ADC. An N-bit resolution ADC means that the converter can resolve 2^N distinct input segments. We can find that high resolution ADCs can resolve smaller segments of the input signal than low

resolution ADCs. This quantity does not mean actually the accuracy of the converter, but instead it usually refers to the number of output bits.

2.2.3.2 Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio of the signal power to the output noise power. The SNR includes the quantization noise and other circuits noise excluding the harmonic components of the input signal. If it is assumed that the input signal is a sinusoidal waveform between 0 and V_{ref}, then the RMS value of the sinusoidal wave is equal to $V_{ref}/\left(2\sqrt{2}\right)$. If we only consider the quantization noise of the ADCs, the maximum SNR of an N-bit ADC is

$$SNR = 20\log_{10}\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log_{10}\left(\frac{V_{ref}/\left(2\sqrt{2}\right)}{V_{LSB}/\left(\sqrt{12}\right)}\right) = 20\log_{10}\left(\sqrt{\frac{3}{2}}2^{N}\right) \qquad (2.6)$$

$$SNR = 6.02N + 1.76\ dB$$

However, the SNR decreases from the best possible value for reduced the input signal levels [4].

2.2.3.3 Signal-to-Noise plus Distortion Ratio (SNDR)

The signal-to-noise plus distortion ratio (SNDR) is often used to measure the performance of an ADC. When a sinusoidal signal is applied to an ADC, the output spectrum generally contains a single tone at the fundamental frequency. Due to distortion, the output spectrum also contains several tones at the harmonic frequency, known as harmonic distortion. As a result, the SNDR of the ADC is defined as the ratio of the signal power at the fundamental frequency to the total power of non-ideal effects, including the harmonic distortion, quantization noise and other noise sources presented at the output.

2.2.3.4 Spurious Free Dynamic Range (SFDR)

The spurious free dynamic range is defined as the power ratio of the input signal to the largest distortion component. In a fully differential signal system, generally the largest distortion component is the 3rd harmonic term.

For more clearly figuring out the difference among SNR, SNDR and SFDR, a spectrum diagram is shown in Figure 2.5, where S is the fundamental frequency of the input signal, D are the distortion components and N is the noise floor.

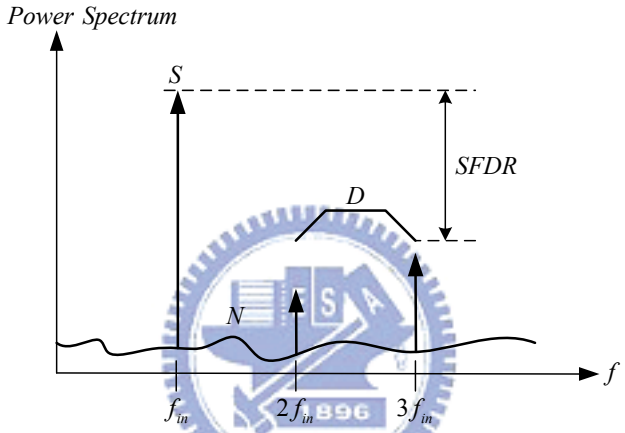


Figure 2.5 The spectrum diagram with signal, distortion and noise.

The SFDR is depicted in Figure 2.5, and the SNR and SNDR are depicted as below respectively.

$$SNR = \frac{S}{N} \qquad SNDR = \frac{S}{N+D} \tag{2.7}$$

2.2.3.5 Effective Number of Bits (ENOB)

Another specification often used to describe the ADC's performance is the effective number of bits (ENOB). Different from resolution, ENOB indicates the ADC's accuracy in a specific input frequency and sampling rate, and it can be expressed from SNDR as follow:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad bits \tag{2.8}$$

2.2.3.6 Offset and Gain Error

The transfer characteristic of an ADC is expected to be a straight line with uniform step width. However, the actual transfer step widths might not be uniform ideally. These non-ideal terms cause errors and non-linearity performance in ADCs. Figure 2.6 (a) shows the offset error, which is defined as the horizontal deviation from the ideal position by a constant amount. The gain error (or scale factor error) describes the difference of slop between the ideal straight line and the actual transfer line, as shown in Figure 2.6 (b).

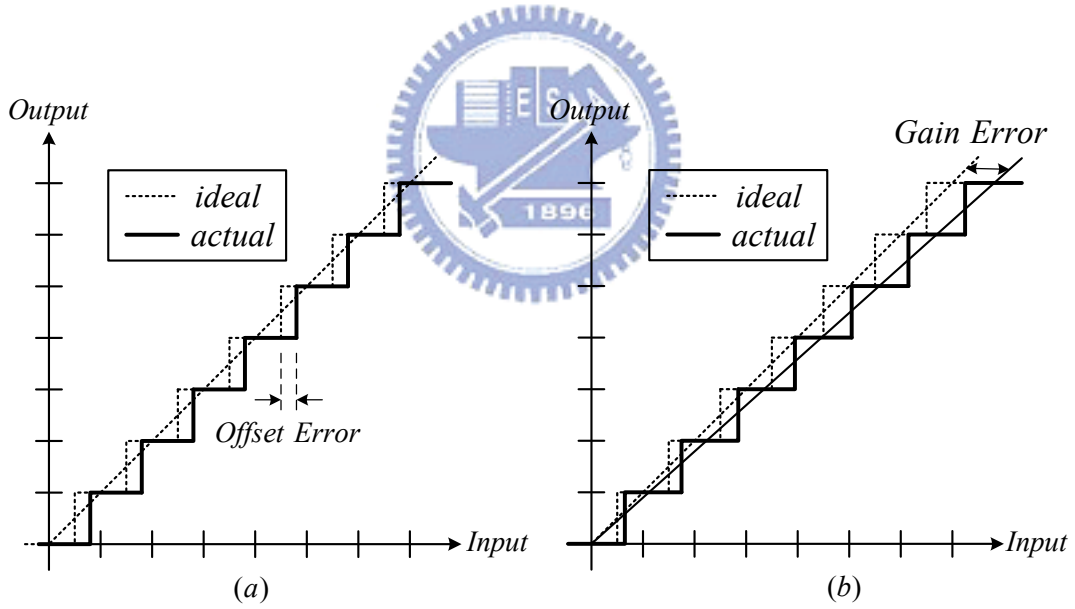


Figure 2.6 Illustrating (a) offset error and (b) gain error for a 3-bit A/D converter.

2.2.3.7 Differential Non-Linearity Error (DNL)

After both the offset and gain errors have been removed, each transfer step level might not be equal to 1 LSB ($=\frac{V_{ref}}{2^N}$) ideally. The *differential non-linearity error* is defined as the variation of each transfer width from 1 LSB, and it can be expressed as

$$DNL(n) = \frac{Width_{step,n} - 1\ LSB}{1\ LSB} \tag{2.9}$$

An ADC is guaranteed not to have any missing codes if the minimum DNL error is larger than -1 LSB.

2.2.3.8 Integral Non-Linearity Error (INL)

The *integral non-linearity error* is defined as the deviation of the middle point of each transfer step form the ideal straight line. There are two ways to define the straight line. A common used definition is known as the endpoint straight line which is drawn through the end points of the first and last code transition. An alternative definition is to find the best-fit straight line such that the maximum INL is minimized [4]. The INL is also specified after both the offset and gain errors have been removed and can be expressed as

$$INL(n) = \frac{V_{t(n),actual} - V_{t(n),ideal}}{1LSB} \tag{2.10}$$

Figure 2.7 shows the illustration of the DNL and INL.

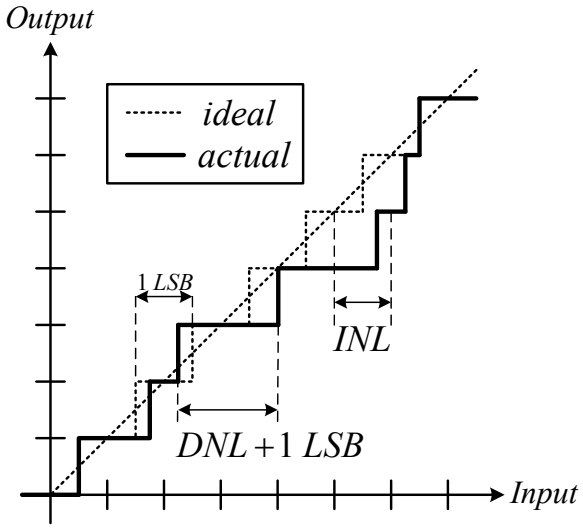


Figure 2.7 Illustrating the DNL and INL.

2.2.3.9 Sampling-Time Uncertainty (Aperture Jitter)

The sampling-time uncertainty is another significant issue that limits the performance of ADCs, which is also known as aperture jitter. Considering a sinusoidal wave input signal, V_{in}, with input frequency f_{in} as below

$$V_{in}(t) = \frac{V_{ref}}{2}\sin(2\pi f_{in} t) \tag{2.11}$$

Since the variance of V_{in} for a sinusoidal waveform is the largest at the zero crossing point, we can find out the maximum slope by differentiating V_{in} with respect to time and setting t=0, as shown below

$$\left.\frac{\Delta V_{in}}{\Delta t}\right|_{\max} = \pi f_{in} V_{ref} \tag{2.12}$$

If Δt represents the sampling-time uncertainty, and if we want to keep ΔV_{in} less than 1 LSB, we can find that

$$\Delta V_{in} = \pi f_{in} V_{ref} \Delta t < V_{LSB} \tag{2.13}$$

In consequentially, we get the limit of the aperture jitter Δt of a N-bit ADC as follows

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}} \tag{2.14}$$

Figure 2.8 shows the concept of the aperture jitter [4].

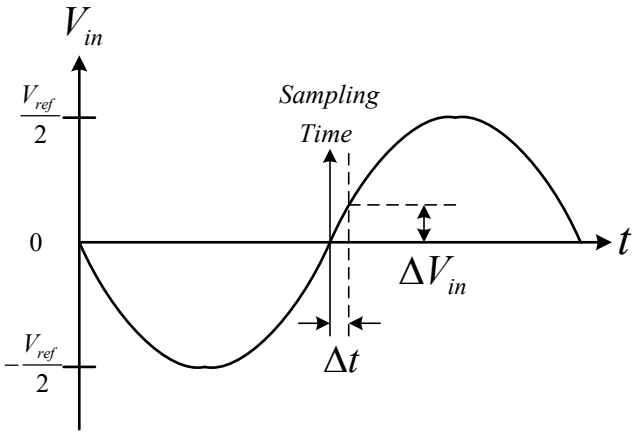


Figure 2.8 Aperture jitter.

2.2.3.10 Dynamic Range (DR)

The dynamic range is defined as the ratio between the maximum signal power for peak SNR and the minimum detectable signal power within a specified bandwidth. With a sinusoidal input signal, we can measure the dynamic range by varying its amplitude to find the 0dB SNR and peak SNR positions, as shown in Figure 2.9. If the noise power is independent on the signal power, the dynamic range is equal to the SNR at full scale. However, generally the noise power increases as the signal power increases. Therefore, the actual peak SNR will be less than the dynamic range [3].

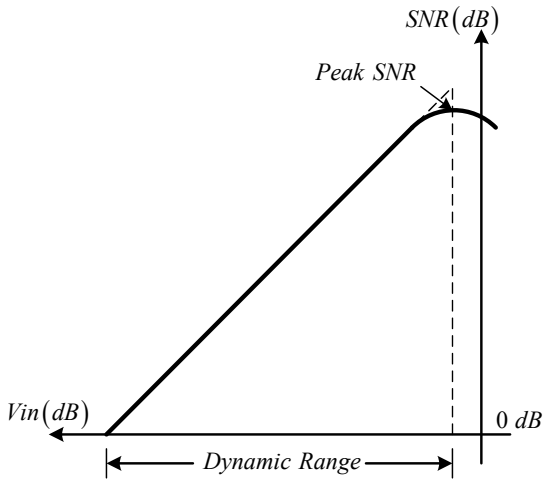


Figure 2.9 Dynamic range.

2.3 Review of Nyquist-Rate A/D Converter Architecture

Architectures for implementing analog-to-digital converters (ADCs) can be roughly divided into three categories (Table 2.1)—low-to-medium speed, medium speed, and high speed. These different architectures of ADCs are developed for different applications. Each of them has different trade-off among speed, resolution, power, and area. In the section, Nyquist-rate A/D converters are introduced. These ADCs generate a series of output codes in which each code has a one-to-one correspondence with a single input value. With high operation speed near the Nyquist rate, these ADCs are good for high speed application. Another kind of ADCs is known as oversampling A/D converters, which are not introduced in this section. These ADCs operate much faster than the input signal's Nyquist rate and increase the signal-to-noise ratio (SNR) by filtering out quantization noise. Generally, the oversampling ADCs are adopted for high resolution design.

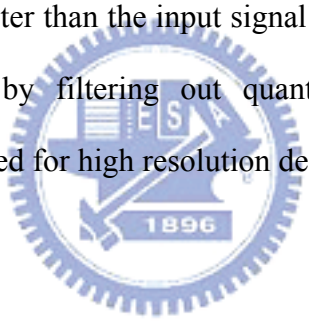


Table 2.1 Different A/D converter architectures [4].

Low-to-Medium Speed, High Accuracy	**Medium Speed, Medium Accuracy**	**High Speed, Low-to-Medium Accuracy**
Integrating	Successive approximation	Flash
Oversampling	Algorithmic	Two-step
		Interpolating
		Folding
		Pipelined
		Time-interleaved

2.3.1 Flash (or Parallel) ADC

Flash ADCs, also known as Parallel ADCs, have the highest speed in overall ADC architectures. As seed in Figure 2.10, a flash ADC is composed with a resistor string、2^N-1 comparators and a (2^N-1)-to-N decoder. The resistor string contains 2^N resistors and divides the reference voltage into 2^N-1 segment values, and each of which is fed to a comparator's negative input. The input voltage is compared with each segment value and results in a thermometer code at the output of the comparators. The thermometer exhibits all ones at the bottom if V_{input} is great then the voltage on the resistor string, and zeros at the top if V_{input} is less then the voltage on the resistor string. Finally, an (2^N-1)-to-N decoder is used to convert the (2^N-1)-bit thermometer code into an N-bit binary output code. It is obvious that all comparators operate in parallel, and then the decoder deals with the output codes of these comparators immediately. Therefore, flash ADCs can generate a digital output word in each clock phase. Besides, the conversion speed of the flash ADC is only dependent on the speed of the comparators and the digital decoder, so it is easy to achieve high speed. With extremely high throughput, the flash ADC is quite suitable for very high speed application. However, for high resolution flash ADCs, a larger number of comparators and small offset for these comparators are required. Design of a comparator with small offsets is difficult and expensive. Furthermore, a large number of comparators induces a large input capacitive loading limiting the conversion rate and consumes large power and area. For above reasons, high resolution ADCs are rarely implemented by flash architectures.

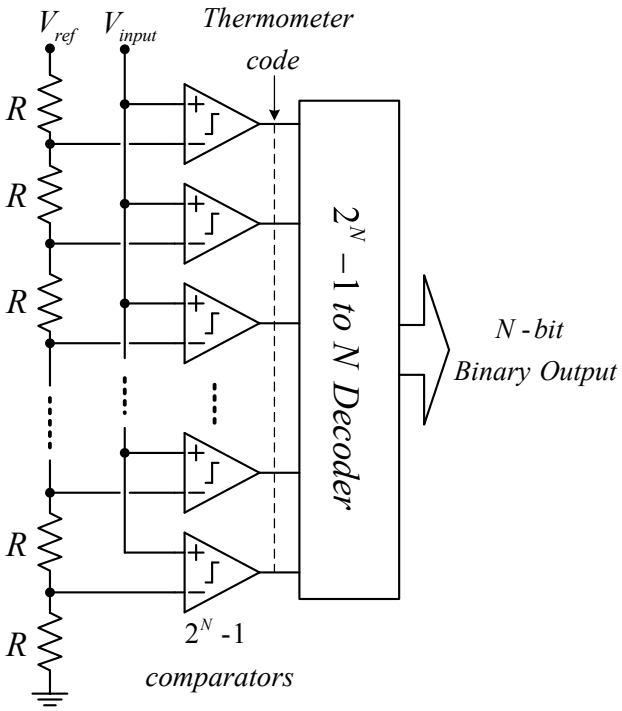


Figure 2.10 An N-bit Flash ADC.

2.3.2 Two-Step ADC

Accompanying the increase of resolution, the flash ADC becomes nearly impossible to be realized for too large power consumption and area. One way to solve this problem is to separate the converter into two complete flash ADCs, which is known as two-step ADC. A two-step ADC mainly consists of a MSB ADC and a LSB ADC, which are used to convert the former bits and the later bits separately. As shown in Figure 2.11, we assume the MSB ADC is an M-bit converter and the LSB ADC is an L-bit converter, so the Sub-DAC must be an M-bit converter and the total output resolution, N, is equal to the sum of M and L. First, the input signal is quantized by the MSB ADC, and then the Sub-DAC would convert the first M-bit output code back to analog signal. This analog signal would be subtracted from the input signal, and then the result would be multiplied by 2^M. The output value of the amplifier is known as residue value. In the next phase, the residue value is fed to the

LSB ADC to determine the last L-bit output code, and then the total N-bit output code is accomplished by combining the first M-bit output and the last L-bit output. By applying the two-step architecture, the number of required comparators can be reduced greatly from original 2^N-1 to 2^M+2^L-2 (if M=L=N/2, it is equal to $2*(2^{(N/2)}-1)$) only. Therefore, it would be possible to realize high resolution ADC by using two-step architecture. However, the two-step ADC requires two clock cycle to generate one digital output word, so the speed of two-step ADC is slower than the flash ADC, which only needs one clock cycle [7].

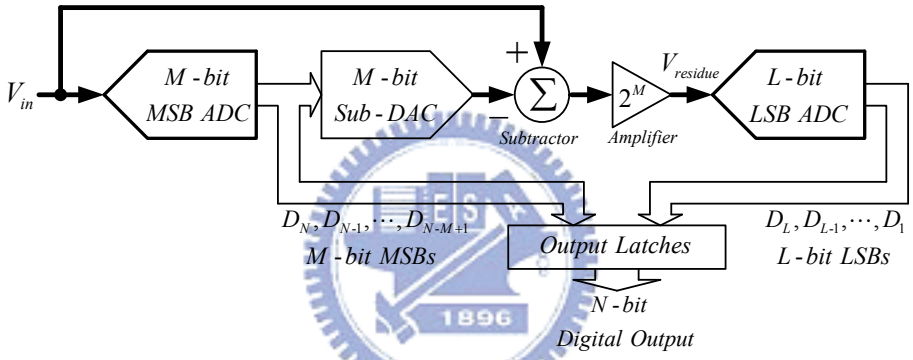


Figure 2.11 An N-bit Two-Step ADC.

2.3.3 Pipelined ADC

In two-step ADC, the ADC is divided into two steps, and it could be possible to separate the ADC into N steps, which is known as a pipelined ADC. As shown in Figure 2.12, a pipelined ADC consists of a S/H, several identical stages and a flash ADC in the final part. Each identical stage includes a Sub-ADC and a multiplying digital-to-analog converter (MDAC), which is composed of the S/H, the Sub-DAC, the subtractor and the gain amplifier.

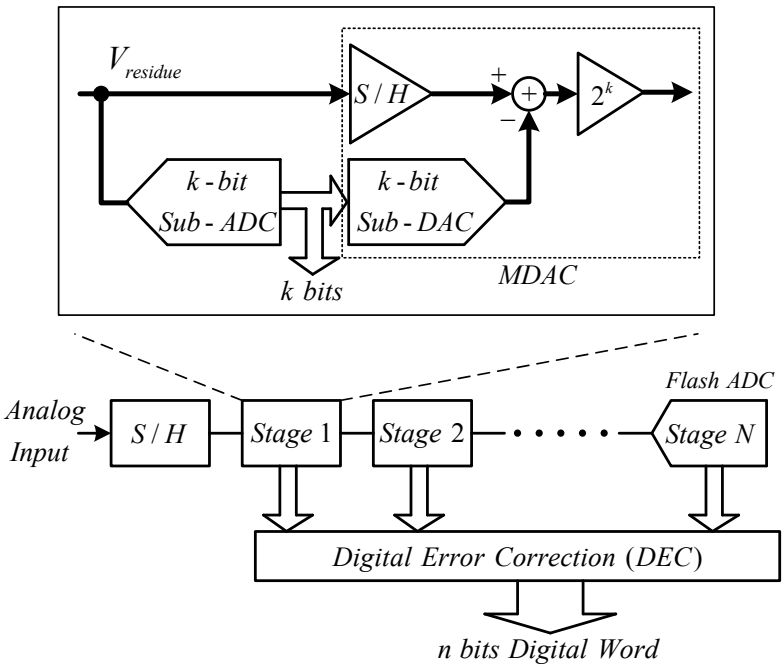


Figure 2.12 An N-bit Pipelined ADC.

First, the input signal is sampled by the S/H and then the held value is fed to stage 1. The following identical stages sample the residue of the previous stage and process the signal likely a two-step ADC. The S/H in each stage allows stages to operate concurrently, so that each stage is free to process a new sample as soon as its residue is sampled by the next stage. Finally, the residue is fed to a flash ADC to determine the last bits. After an initial latency of N clock cycles, one conversion will be completed per clock cycle. Therefore, the pipelined ADC could still keep high throughput rate even though the number of stages increases. Because of the feature, pipelined ADCs can generally operate at much higher sampling rates.

With the inter-stage gain amplifiers, the requirement of the comparators for the following stages could be relaxed. Therefore, we could realize a high resolution pipelined ADC by only increasing the number of stages without raising the complexity of the comparators too much. However, the additional gain amplifiers would become the dominate sources of power dissipation. Therefore, pipelined ADCs might consume larger power than other Flash and Two-Step ADCs. For high

resolution applications, pipelined ADCs need fewer circuits compared to Flash and Two-Step ADCs, since the circuit complexity for pipelined ADCs approximately increase linearity but that is exponential growth in Flash and Two-Step ADCs. Because of the ability of each stage to operate concurrently and the tolerance of the comparator offsets, pipelined ADCs are quite suitable for high speed and medium-to-high resolution application [8].

2.3.4 Cyclic ADC

A cyclic ADC is similar to a single stage of pipelined ADCs with the output fed back to the input, as shown in Figure 2.13. It has only one stage and this stage would be repeatedly used in one cycle. When an input is sampled by the cyclic ADC, it takes N cycles to complete the output word and the delay time is the same as the pipelined ADC. However, the new input would not be sampled for a cyclic ADC before the N-bit output word is completed, so the throughput rate of the cyclic ADC is only 1/N times compared with the pipelined ADC. However, since only one stage is required, the cyclic ADC is extremely suitable for low power and low area designs.

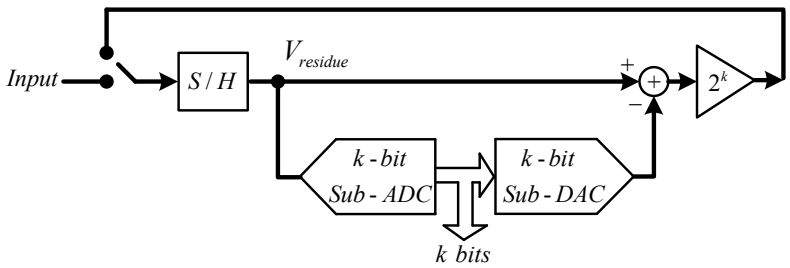


Figure 2.13 A Cyclic ADC.

2.3.5 Successive Approximation ADC

Successive-approximation ADCs apply a binary search algorithm to determine the closest digital word to match the input signal. As shown in Figure 2.14, it is also known as successive-approximation register (SAR) ADC. In the first cycle, the MSB, b_1, is determined and stored in the successive-approximation register (SAR), and then b_1 is fed to the D/A converter to generate a new reference value, $V_{D/A}$. In the second cycle, the original input signal is compared with the new $V_{D/A}$ to determine b_2 and then the same operation is repeated again. After N period cycles, the complete N-bit output word is determined. Successive approximation ADCs are very analogous to Cyclic ADCs, but in each cycle the former varies the reference voltage and the later varies the input signal.

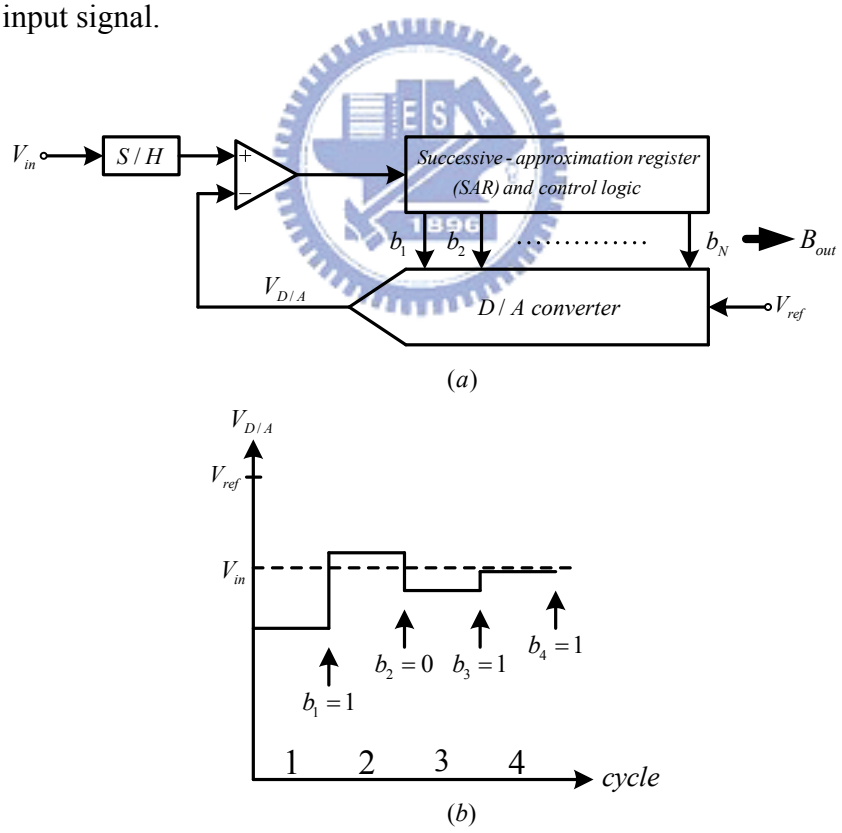


Figure 2.14 (a) Successive-approximation converter and

(b) transfer curve of $V_{D/A}$.

2.3.6 Time-Interleaved ADC

The time-interleaved ADC is realized by operating many identical ADCs in parallel. Figure 2.15 shows a four-channel time-interleaved ADC. Here, Φ_0 is a clock at four times the rate of Φ_1 to Φ_4. The additional Φ_1 to Φ_4 are delayed with respect to each other by the period of Φ_0, such that each converter will get successive samples of the input signal, V_{in}, sampled at the rate of Φ_0. In this way, the throughput rate of the time-interleaved ADC is four times the rate of each ADC in the four channels. By using many ADCs in parallel, time-interleaved ADCs achieve high conversion rate but consume large power and area. It is also essential that the channels are extremely well matched, as mismatches will introduce tones at f_s / m when there are m channels [4] [9].

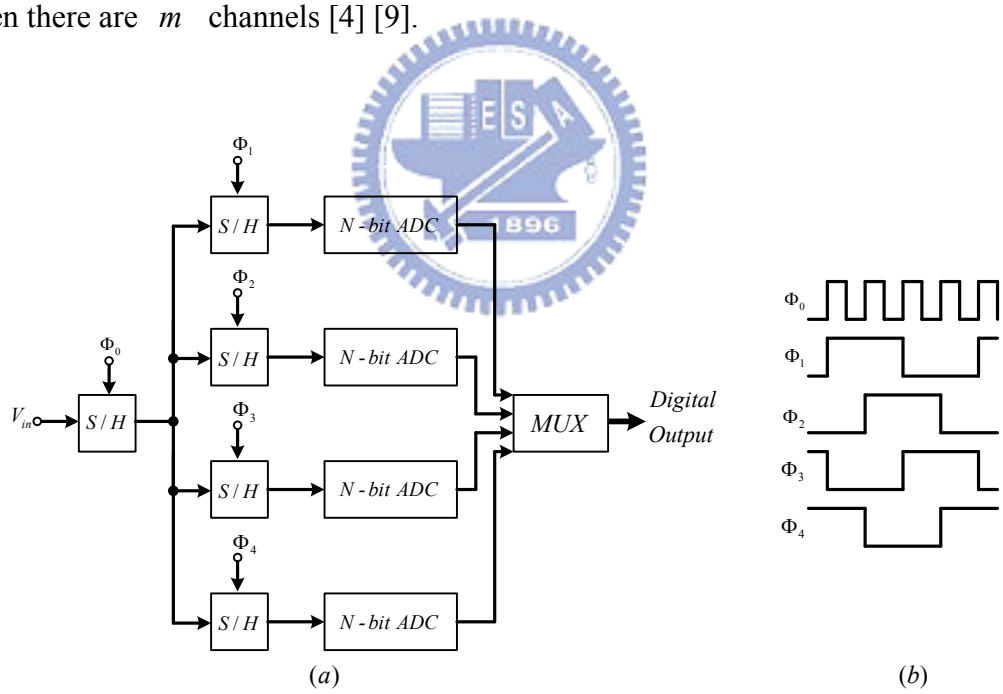


Figure 2.15 (a) A four-channel time-interleaved ADC and (b) its clock phases.

Chapter 3

Pipelined ADC with Opamp-Sharing Technique and Improved Loading-Free Architecture

3.1 Introduction

In this chapter, the proposed pipelined ADCs with opamp-sharing technique and improved loading-free architecture would be discussed in detail. Before these discussions, the basic blocks of pipelined ADCs and the calibration techniques are introduced first. With the calibration techniques, the nonlinearities occurring in pipelined ADCs could be compensated and the requirements of comparator offsets are also relaxed. Then, the most popular 1.5-bit/stage structure in pipelined ADC is presented. In this architecture, the inter stages have large bandwidth and can be realized by simple components. Thus, it is very suitable for high speed and low power design. For higher power- and area- efficiency, opamp-sharing technique is introduced first. This technique could significantly reduce the number of required opamps. Following, the loading-free architecture based on switched-opamp (SO) circuits is presented. SO structure is suitable for low voltage design since no floating switched is needed. By reducing the output capacitive loading, loading-free architecture can achieve higher operation speed than conventional SO circuits. For even more improving the loading-free architecture, the proposed new loading-free MDAC is developed, which has less output capacitive loading and larger feedback factor. A summary is placed in the last to describe the architectures of these two ADCs with opamp-sharing technique and improved loading-free architecture.

3.2 Conventional 1.5-Bit/Stage Pipelined ADC

The detail components of pipelined ADCs are discussed following. Then, the calibration techniques are introduced, which overcome the nonlinearities and relax the requirement of comparators. After that, the most popular architecture, 1.5-bit/stage pipelined ADC, is introduced. It owns large tolerance to the offset of comparators and is easy to be realized with simple components. Besides, the 1.5-bit/stage architecture is good for high speed design. In the final part, we discuss the requirements of gain and speed for pipelined ADCs.

3.2.1 Basic Blocks of Pipelined ADC

The block diagram of a typical pipelined ADC is shown in Figure 3.1, including a S/H, several identical stages, a flash ADC, delay elements and a digital error correction (DEC) logic. The S/H relaxes the timing requirement of the first stage, since the first stage can sample a static signal from the S/H rather than a variant signal from the analog input. Following the S/H, several identical stages are in series. Within each stage, the analog input signal from the previous stage is sampled and fed to the Sub-ADC to resolve k bits. Then, the quantized value from the Sub-DAC is subtracted from the original analog input to yield the output residue. Finally, the residue is multiplied by the amplifier with a gain of 2^k in order to maintain the input signal range equal to the output signal range for each stage. The S/H, Sub-DAC, subtraction and the amplification are combined into one single circuit called multiplying digital-to-analog converter (MDAC). The last signal is fed into a Flash ADC to determine the last bits. Since the former bits are generated early, the delay elements are required for synchronizing the output codes. By passing the digital error correction (DEC) logic, the final output digital word is completed [3] [4].

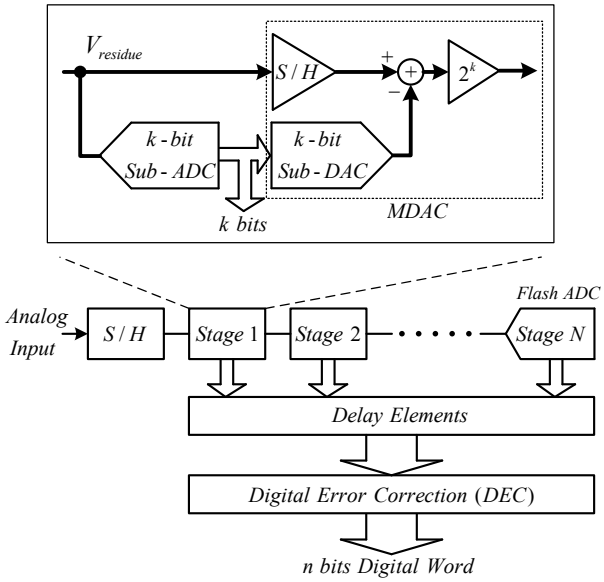


Figure 3.1 The block diagram of a k-bit/stage pipelined ADC.

The timing diagram for a pipelined ADC is shown in Figure 3.2. The pipelined ADC needs two clock phases for each conversion. One clock phase is used for sampling the input signal, and the other is employed for processing and holding the residue voltage. Since the hold residue voltage in current stage has to be sampled by the next stage, the consecutive stages must operate in opposite clock phase. Thus, the latency in clock cycle is a half of the number of stages. Besides, since each stage is free for processing a new sample as soon as its residue is sampled by the next stage, the pipelined ADC is good for operating concurrently and gives a throughput of one output sample per clock cycle [10] [11].

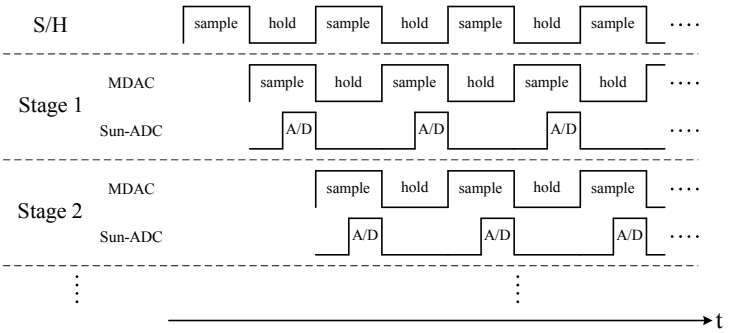


Figure 3.2 Timing diagram of the pipelined ADC.

An example of 2-bit per stage is shown in Figure 3.3(a). The 2-bit ADC divides the full scale input range into four subranges, and each subrange is corresponding to a given 2-bit digital code. According to the digital code, the input signal subtracts the output of the DAC to get the residue value. For restored the original full scale input range, the residue value is multiplied by the amplifier with the gain of 4, so the output value for each stage is

$$V_{out} = 4\left(V_{in} - V_{DAC}\right) \tag{3.1}$$

As shown in Figure 3.3(b)(c), the residue plot is in the shape of sawtooth with the full scale range between V_{ref} and $-V_{ref}$ [12].

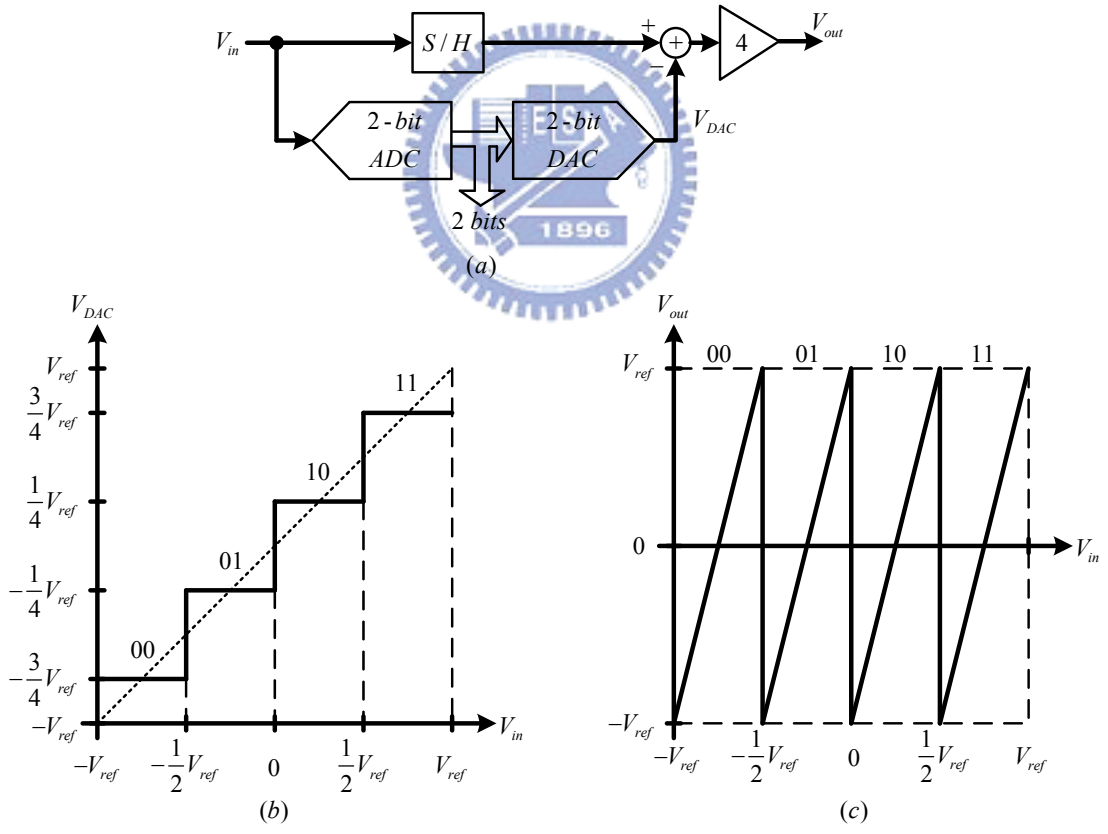


Figure 3.3 (a) Block diagram for 2-bit/stage

(b) V_{in} to V_{DAC} transfer curve (c) V_{in} to V_{out} residue plot.

3.2.2 Nonlinearities and Calibration Techniques

For a general pipelined ADC, the output signal range is equal to the input signal range of each stage. If the output signal range is larger than the input signal range of the next stage, the following stages would solve the wrong codes and the missing codes may also appear. The output signal range is determined by the gain of the residue amplifier which is used to amplify the residue voltage. For an ideal 2-bit per stage pipelined ADC, the gain of the residue amplifier is four. So that, the gain error of the residue amplifier will induce the over range problem, as shown in Figure 3.4(a). Another non-ideal issue also causing the over range problem is the comparator offset of the Sub-ADC, as shown in Figure 3.4(b). The comparator offset would shift the transition level and make the transfer curve exceed the signal range.

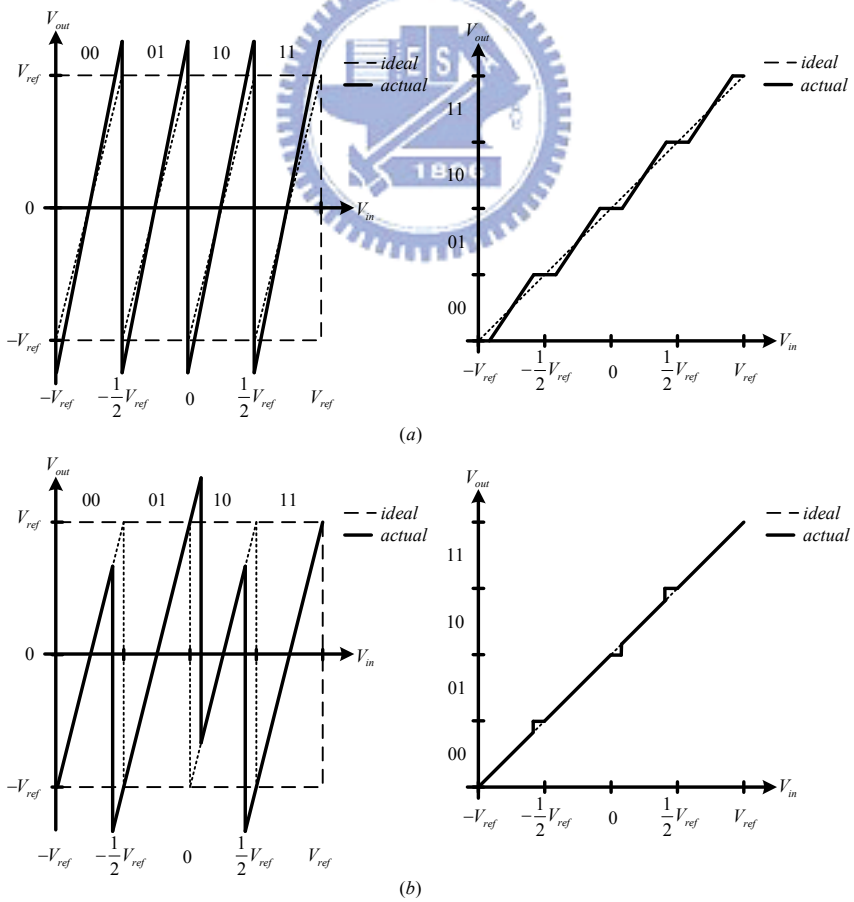


Figure 3.4 Residue plots and conversion characteristics of a 2-bit/stage with (a) Gain error (b) Comparator offset.

In order to prevent the over range problem, the inter stage gain is half reduced so that the amplified residue can remain within the conversion range of the next stage no matter what kind of error exists. To illustrate the calibration technique in more detail, we take a 2-bit per stage pipelined ADC for example. When the inter stage gain is reduced to 2, the residue range is compressed between 1/2 V_{ref} and -1/2 V_{ref}, illustrated in Fig 3.5 (a). If the comparator offset is less than ±1/4Vref, the residue would still be within V_{ref} and $-V_{ref}$. The following stage could correct the output codes by adding or subtracting correction, as shown in Figure 3.5 (b). When one of the transition level of the sub-ADC has an offset, the output of this stage will exceeds ±1/2 V_{ref}. The next stage, sensing the overhanging, will add or subtract the output by 1 LSB, and this is known as digital error correction (DEC) technique. It allows the comparator offset to be as large as ±1/4 V_{ref} and the output is still in the input range of the following stage. Digital error correction simply utilizes the extra bit to correct the overhanging section from the previous stage.

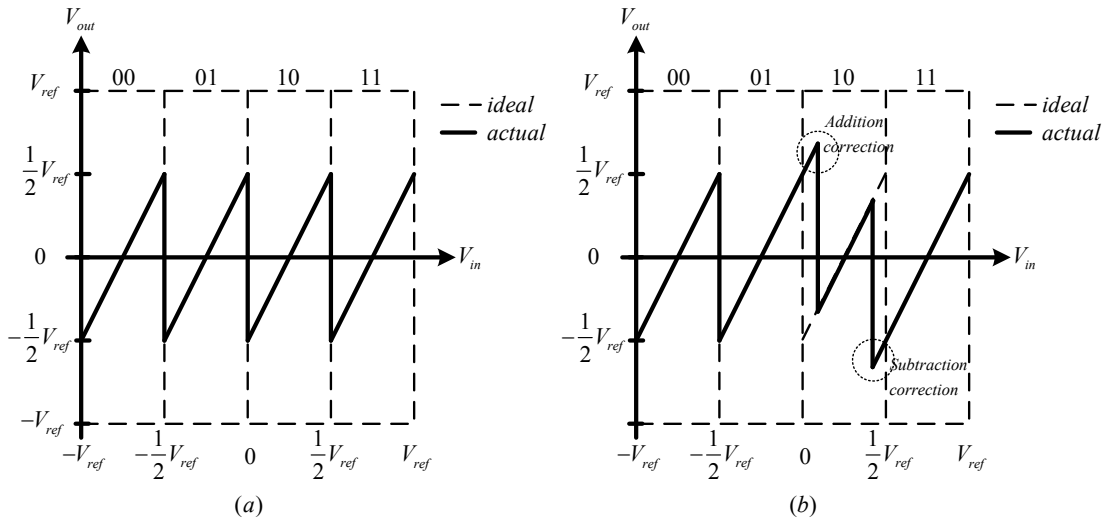


Figure 3.5 (a) the residue plot of 2-bit/stage with inter stage gain of 2

(b) with comparator offset.

Since subtraction is equivalent to addition with offset, we could eliminate subtraction by intentionally adding a 1/2 LSB offset to both sub-ADC and DAC, as shown in Figure 3.6. After shifting 1/2 LSB offset in the transition level, the subranges are separated in different width. The section of "00" is enlarged and that of "11" is reduced. Because the inter stage gain is 2, the amplified residue remains within the conversion range of the next stage when the offset of comparators are between $\pm 1/4V_{ref}$. Under these conditions, errors caused by the sub-ADC nonlinearity can be corrected, and the correction requires no change and addition.

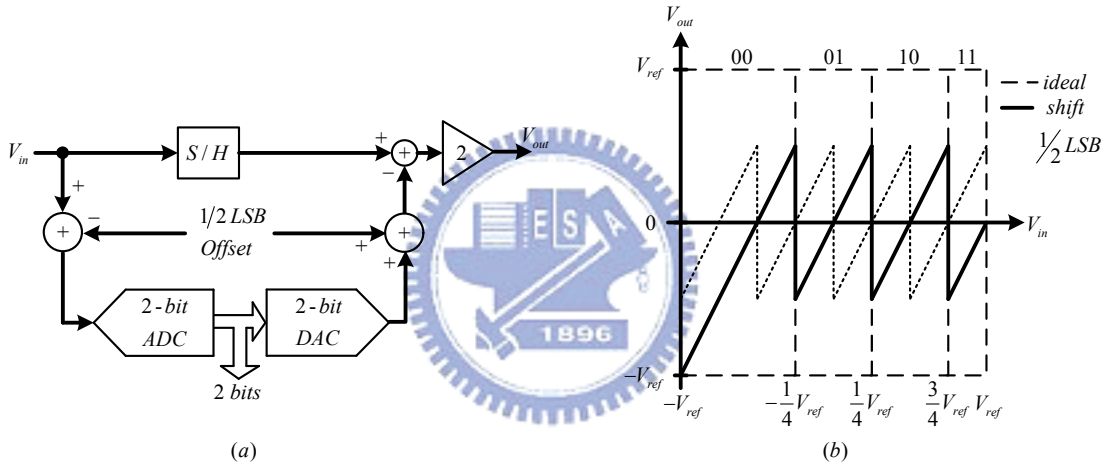


Figure 3.6 (a) Block diagram of one stage with 1/2 LSB offset in ADC and DAC (b) residue plot versus held input with 1/2 LSB offset.

Since the last transition level is only 1/2 LSB below the maximum stage input, we can assume that the decision level of the top comparator has an offset of 1/2 LSB adding and it is shifted to the upper bound of the conversion range, as shown in Figure 3.7(b). The digital output code "11" is eliminated. However, the output code "11" can be recovered by the digital error correction of the next stage and the output residue is still within the conversion range. According to this assumption, removal of the top-most comparator does not change the correction range, since the transition level

can still move by up to ±1/2 LSB before saturating the next stage [12] [13]. This architecture only needs two comparators at 1/4 V_{ref} and -1/4V_{ref} for each Sub-ADC and three reference voltages at at -1/2V_{ref}, 0, 1/2V_{ref} for each Sub-DAC. Since only three codes (00, 01 ,10) are solved per stage, it is known as 1.5-bit/stage pipelined ADC architecture. The digital error correction logic corrects the wrong code by adding the first bit of the next stage to the previous stage, so only 1 bit full adders are used in the correction logic, as shown in Figure 3.8.

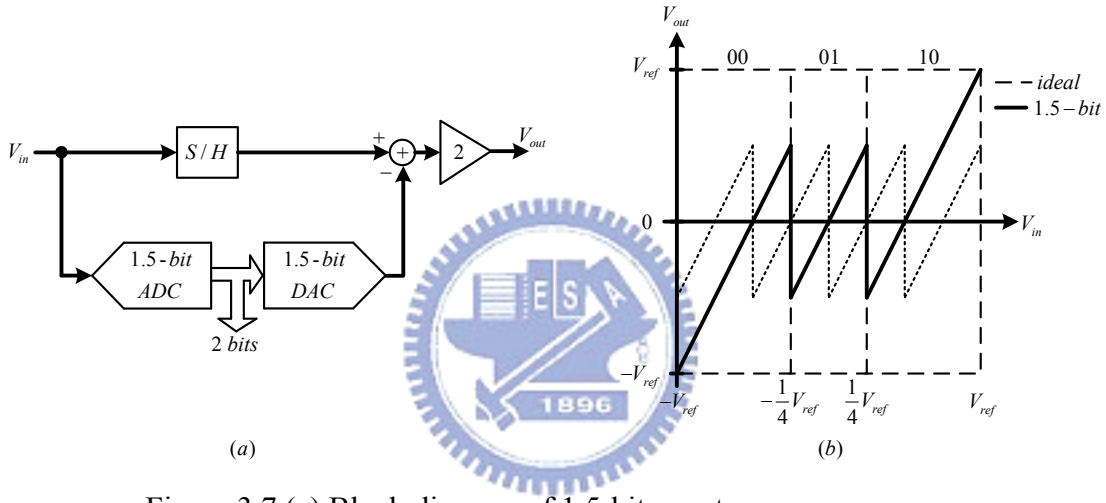


Figure 3.7 (a) Block diagram of 1.5-bit per stage

(b) residue plot versus held input without top comparator.

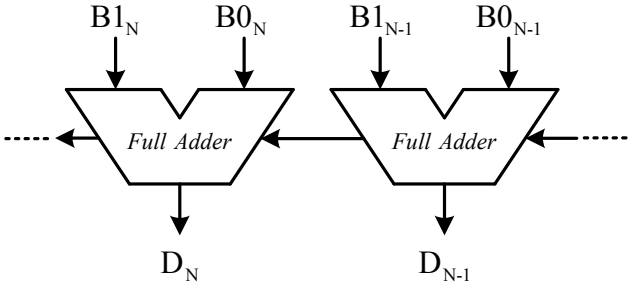


Figure 3.8 Digital error correction logic.

3.2.3 1.5-Bit/Stage Architecture

The number of bits per stage determines the speed, accuracy and power requirements for each stage. Therefore, the best choice of the bit number is dependent on the specification for the overall ADC. With fewer numbers of bits per stage, fewer comparators are required for each Sub-ADC and the comparator requirements are more relaxed. Besides, accuracy requirement is also reduced which allows the stage operating in higher speed due to the fundamental gain bandwidth tradeoff of amplifiers. However, for fewer numbers of bits, more stages are required and the lower accuracy also contributes much noise to the overall conversion. Therefore, lower number of bits is much suitable for high speed, low resolution design.

The 1.5-bit per stage architecture has been shown to be effective in achieving high sampling rate with medium-to-high resolution [12] [14]. An 8-bit pipelined ADC using 1.5-bit per stage architecture is shown in Figure 3.9. The 1.5-bit per stage architecture is employed in the first 6 stage, and the last stage is composed of a 2-bit Flash ADC. By combining the 12 bits from the first six stages and last 2 bits from the Flash ADC, the digital error correction logic produces the final 8-bit output code.

Each stage resolves 2 bits output code with the Sub-ADC, subtracts the output value of the Sub-DAC from its input and amplifies the residue by a gain of 2. The Sub-ADC is characteristic of only 3 digital output codes (00, 01, and 10) and has thresholds at $V_{ref}/4$ and $-V_{ref}/4$. The residue plot has been shown in Figure 3.7 (b) and the residue transfer function can be expressed as

$$V_{out} = \begin{cases} 2V_{in} - V_{ref}, & if \quad 1/4V_{ref} < V_{in} & D = (10)_2 \\ 2V_{in}, & if \quad -1/4V_{ref} < V_{in} < 1/4V_{ref} & D = (01)_2 \\ 2V_{in} + V_{ref}, & if \quad V_{in} < -1/4V_{ref} & D = (00)_2 \end{cases} \tag{3.2}$$

D is the output code for each stage. By using the digital error correction technique with the redundant bits, the comparator offset between $\pm V_{ref}/4$ can be tolerated.

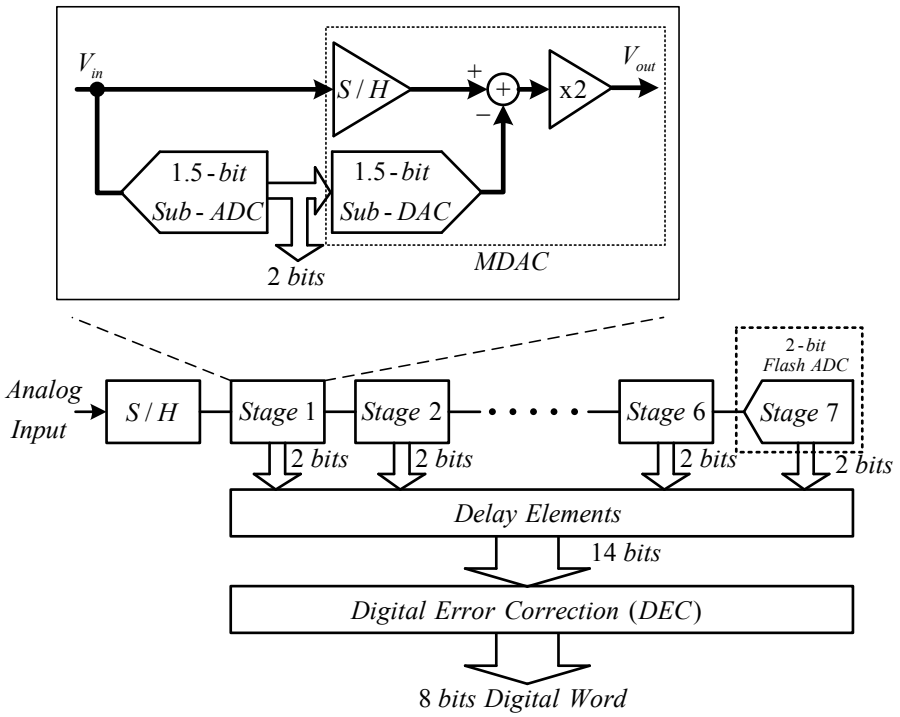


Figure 3.9 Block diagram of 1.5-bit-stage pipelined ADC.

Figure 3.10 illustrates one method to implement the 1.5-bit per stage architecture by using the switched-capacitor circuit. This circuit operates on a two-phase clock. In the first phase, the input signal, V_{in}, is applied to the Sub-ADC, which has two thresholds at $\pm V_{ref}/4$, to solve the 2-bit output code. At the same time, V_{in} is also sampled in the capacitors C_s and C_f. In the next phase, C_f closes a negative feedback loop around the opamp, while the top plate of C_s is switched to the DAC output.

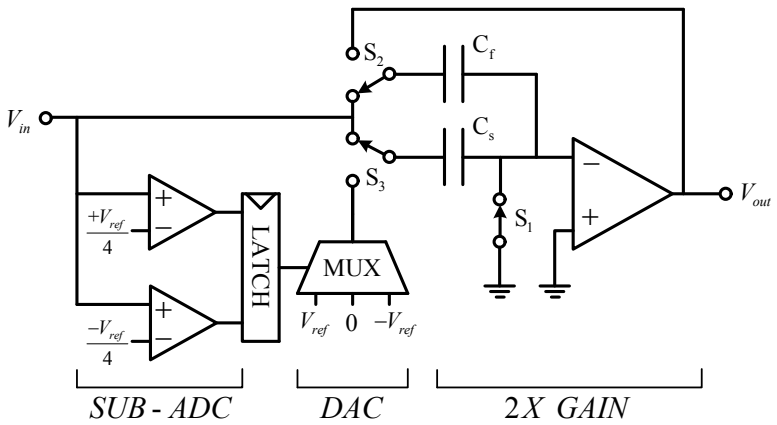


Figure 3.10 Switched-Capacitor circuit for 1.5-bit/stage architecture.

According the 2-bit output code, the reference voltages (V_{ref}, 0, $-V_{ref}$) would be determined by the DAC and the output voltage can be expressed as

$$V_{out} = \begin{cases} \left(1+\frac{C_s}{C_f}\right)V_{in} - \frac{C_s}{C_f}V_{ref}, & if \quad 1/4V_{ref} < V_{in} \\ \left(1+\frac{C_s}{C_f}\right)V_{in}, & if \quad -1/4V_{ref} < V_{in} < 1/4V_{ref} \\ \left(1+\frac{C_s}{C_f}\right)V_{in} + \frac{C_s}{C_f}V_{ref}, & if \quad V_{in} < -1/4V_{ref} \end{cases} \tag{3.3}$$

For 1.5-bit per stage architecture, $C_s = C_f$ is chosen to get a stage gain of two. Since only two comparators are required and the requirements of the comparators are very relax, the amplifier becomes the best part of power consumption.

3.2.4 Accuracy Requirements

The accuracy requirement on each stage of a pipelined ADC is different because the resolution for each stage output is decreased by the number of bit solved per stage. For example, in an N-bit pipelined ADC with B-bit effective resolution per stage, the first stage has to meet N bits resolution requirement and the next stage only need to meet N-B bits resolution requirement. The lower resolution requirement relax the requirements of the inter stage gain amplifier, capacitor mismatch and the thermal noise effect.

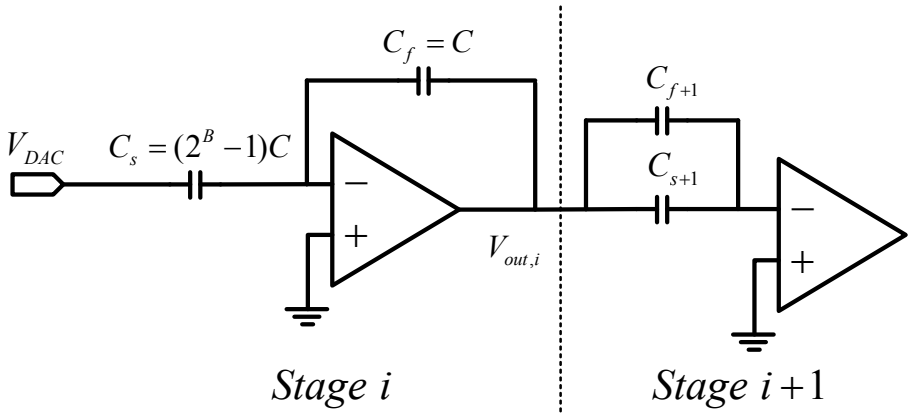


Figure 3.11 B-bit/stage switched-capacitor MDAC.

Figure 3.11 illustrates a switched-capacitor MDAC circuit. Assuming that this is an N-bit resolution pipelined ADC and the stage i is the first stage. Since each stage solves B bits effective resolution, the output of the first stage has only to meet N-B bits resolution requirement. Considering the nonidealities of the inter stage amplifier that introduce the finite opamp gain, the output value can be expressed as

$$V_{out} = G_i \cdot \left(V_{in} - V_{DAC}\right) \tag{3.4}$$

$$G_i = \left(\frac{C_s + C_f}{C_f}\right)\left(\frac{1}{1+\frac{1}{Af}}\right)\left(1 - e^{-\frac{t}{\tau}}\right) \tag{3.5}$$

$$f = \frac{C_f}{C_s + C_f + C_{op-amp}} \tag{3.6}$$

where f is the feedback factor as expressed in Equation (3.6). The exponential term represent the finite settling time t of the single pole opamp, where the τ is the time constant for the SC configuration, and the A is the finite opamp gain. For a infinite opamp DC gain, the ideal inter stage gain G_i can be known as

$$G_i = \frac{C_s + C_f}{C_f} = \frac{\left(2^B - 1\right)C + C}{C} = 2^B \tag{3.7}$$

In order to meet the N-B bits resolution requirement for the next stage, the finite gain error of the inter stage should be theoretically less than 1/2 LSB and it can be described as

$$\varepsilon_{rr} = \left|\frac{G_{actual} - G_{ideal}}{G_{ideal}}\right| = \left|\frac{1}{Af}\right| \tag{3.8}$$

Therefore, we can get

$$\varepsilon_{rr} = \left|\frac{1}{Af}\right| < \frac{1}{2} \cdot \frac{1}{2^{N-B}} \tag{3.9}$$

Combining Equations (3.6) and (3.9), the limit of finite gain for the inter stage amplifier can be expressed as following

$$A > \frac{1}{f} \times 2^{N-B+1} = \frac{C_s + C_f + C_{op-amp}}{C_f} \times 2^{N-B+1} = \frac{2^B C + C_{op-amp}}{C} \times 2^{N-B+1} \qquad (3.10)$$

If $C_{op\text{-}amp}$ is small enough to be neglected, Equation 3.10 is equal to 2^{N+1} and this is the minimum requirement of A for the first stage. Increasing the number of bit per stage solved does not enhance the minimal required gain of the amplifier. In practice, the opamp gain should be much larger than this value since errors caused by other sources such as incomplete settling and capacitor-mismatch are not taken into account.

After considering the gain requirement of the inter stage amplifier, the finite settling time of the switch-capacitor circuit is discussed. The speed constraints influencing the accuracy include the slew time for large signal and the settling time for small signal. The slew time is related to the tail current and the output load capacitance of the inter stage opamp; while the settling time depends on the unity-gain frequency (f_u) and the phase margin of the opamp, and the feedback factor (f) of the close-loop circuit.

Referring to Equation (3.5), the settling error can be expressed as following

$$\varepsilon_{rr,settle} = e^{-t/\tau} \qquad (3.11)$$

where τ is the time constant of the close-loop circuit. For a single pole opamp switched-capacitor circuit, the time constant is equal to

$$\tau = \frac{1}{\omega_{3dB}} = \frac{1}{2\pi \cdot f_u \cdot f} \qquad (3.12)$$

where ω_{3dB} is the close-loop bandwidth, f_u is the unity-gain frequency of the amplifier and f is the feedback factor.

For the same reason to meet the N-B bits resolution requirement, the settling error of output response must less than 1/2 LSB.

$$\varepsilon_{rr,settle} = e^{-T_{settle}/\tau} < \frac{1}{2} \cdot \frac{1}{2^{N-B}} \tag{3.13}$$

According to Equation (3.12) and (3.13), we can obtain the required minimum unity-gain frequency f_u of the amplifier as following

$$f_u > \frac{(N-B+1)\cdot \ln 2}{2\pi \cdot T_{settle} \cdot f} = \frac{(N-B+1)\cdot \ln 2}{2\pi \cdot T_{settle}} \cdot \left(2^B + \frac{C_{op-amp}}{C}\right) \tag{3.14}$$

where T_{settle} is the allowed settling time and it is usually 75%~90% of half conversion period. From above equation, higher unity-gain frequency is required to sustain the accuracy for larger number of bit per stage solved, B.

Another nonideality that also influences the accuracy is the capacitor-mismatch effect due to the process variation. The required matching of the sampling and feedback capacitors in MDAC are determined by the required DAC accuracy. Assuming that the value of the capacitors deviates by ΔC, which makes $C_s = C+\Delta C/2$ and $C_f = C-\Delta C/2$, the output of the MDAC is given by

$$V_{out} = \left(2 + \frac{\Delta C}{C}\right) V_{in} \pm \left(1 + \frac{\Delta C}{C}\right) V_{DAC} \tag{3.15}$$

From Equation (3.15), the error term ΔC/C must be less than $1/2^{N-B}$ to ensure that offset of DAC is less than 1 LSB.

$$\frac{\Delta C}{C} < \frac{1}{2^{N-B}} \tag{3.16}$$

In addition to above deterministic errors, the thermal noise KT/C also causes random errors in the SC circuits. As we known larger capacitors tend to have better matching property and less thermal noise contribution than smaller capacitors. However, smaller capacitors provide less loading and faster settling for enabling high speed. In the other word, the thermal noise can be reduced by increasing the size of the sampling capacitors, but that would increase the power consumption and slow

down the settling behavior. Therefore, there exists a tradeoff to determine the capacitor size. For designing ADCs, the thermal noise power has to be less than the quantization noise power which had been shown to be $V_{LSB}^2/12$. Thus, the lowest limit for the sampling capacitor value is set as following [15]

$$C >> \frac{4kT \cdot 12}{V_{FS}^2} \cdot 2^{2N} \tag{3.17}$$

where N is the total resolution of the ADC which has the full-scale input signal V_{FS} and four sampling capacitors C in the MDAC.

3.3 Opamp-Sharing Technique

The opamp-sharing technique has been presented in previous paper [16]-[18]. Amplifier sharing between two successive stages is motivated by the fact that in SC architecture, the amplifier is active only in half of a clock cycle, which is during the amplification phase. As illustrated in Figure 3.12, when the stage N is in the sampling phase, the opamp is in the idle state. At the same clock phase, the stage N+1 is in amplification phase, and the opamp is active in a closed feedback loop. In the next phase, stage N changes to amplification phase and stage N+1 changes to sampling phase. Thus, for the whole clock cycle only one opamp is needed.

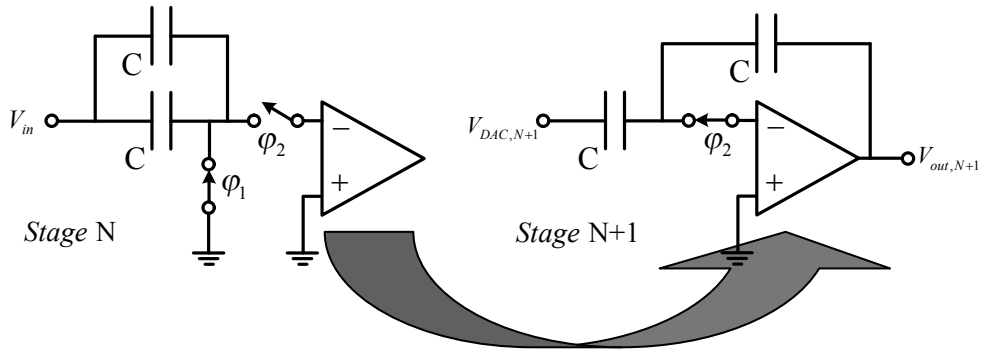


Figure 3.12 Opamp-sharing technique.

Therefore, this opamp can be shared between these two consecutive pipeline stages by adding two more switch sets, which enables the opamp to commutate between these two SC networks. By using the opamp-sharing technique, the power dissipation and chip size for whole pipelined ADC can be reduced about half amount.

However, the amplifier shared between two stages has no time to be reset, so each input sample will be affected by the finite-gain error from the previous sample. The feedback signal polarity inverting (FSPI) technique [16] has been presented in previous paper to reduce the error signal, as shown in Figure 3.13. We assume that the shared opamp would induce an error signal at the output that is added to the residue signal as an output-referred offset voltage of the opamp. For 1.5-bit/stage architecture, the first and second residue signals would be given by

$$V_{res,1} = 2V_{in} - D_1 V_{ref} + V_{err,1} \tag{3.18}$$

$$\begin{aligned} V_{res,2} &= 2V_{res,1} - D_2 V_{ref} + V_{err,2} \\ &= 4V_{in} - 2D_1 V_{ref} - D_2 V_{ref} + 2V_{err,1} + V_{err,2} \end{aligned} \tag{3.19}$$

The output-referred offset voltages are composed of low frequency components compared with the ADC clock frequency, and thus, we can assume that it has similar value between two phases and the second residue signal becomes

$$V_{res,2} = 4V_{in} - 2D_1 V_{ref} - D_2 V_{ref} + 3V_{err,1} \tag{3.20}$$

By swapping two input terminals and two output terminals of the opamp between two sharing stages, as illustrated in Figure 3.13, the polarity of the second error signal is inverted during the next phase. Thus the error voltage of the second residue will be subtracted from that of the first residue, as follows:

$$\begin{aligned} V_{res,2} &= 4V_{in} - 2D_1 V_{ref} - D_2 V_{ref} + 2V_{err,1} - V_{err,1} \\ &= 4V_{in} - 2D_1 V_{ref} - D_2 V_{ref} + 1V_{err,1} \end{aligned} \tag{3.21}$$

Therefore, with the proposed FSPI technique, the error voltage of the shared amplifier can be reduced to 1/3 of the conventional error voltage. However, the additional switches introduce extra series resistance that increases the settling time and also cause extra charge injection resulting in larger input offset voltage. The bottom plate sampling technique is used to reduce the charge injection and clock feedthrough effect.

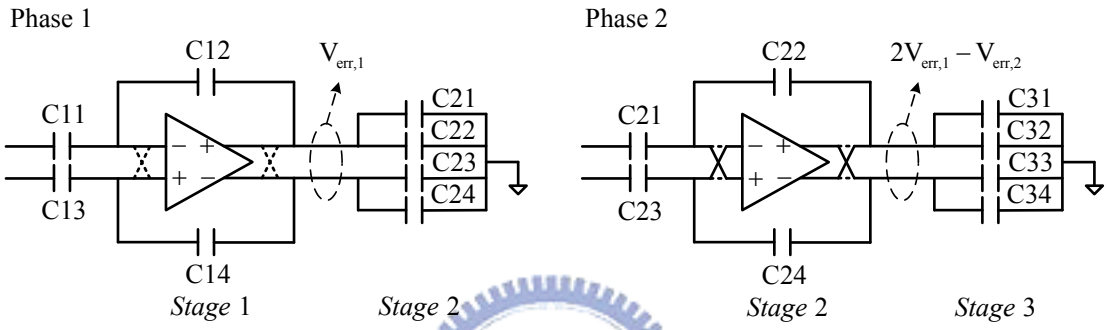


Figure 3.13 Feedback signal polarity inverting (FISP) technique.

3.4 Improved Loading-Free Architecture

In this section, we first introduce the pipelined ADC architecture and the limitation of conventional switched-opamp (SO) MDAC. Then, the loading-free architecture is discussed [19] which address the issue of limited speed in conventional SO pipelined ADC. Finally, the improved loading-free architecture is proposed. With higher feedback factor and less output loading, the proposed architecture is better for higher speed application.

3.4.1 Switched-Opamp Pipelined ADC

Switched-capacitor (SC) pipelined ADCs are the most popular architectures with high speed and low power. However, this architecture is not suitable for low voltage

design because SC MDACs command the use of many floating switches, which may lead to insufficient switch overdrive at low supply voltage. This scenario deteriorates to a floating switch (a switch that passes varying voltage rather than constant voltage) with zero conductance when the supply voltage is lower than the sum of pMOS and nMOS threshold voltages. Switched-opamp (SO) is an analog circuit technique proposed to address this issue.

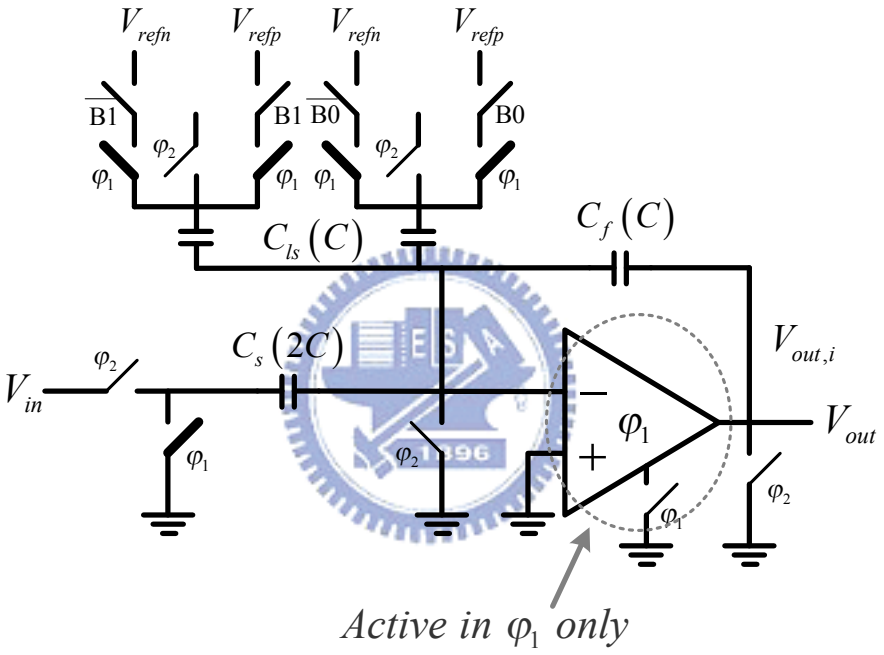


Figure 3.14 Implementation of 1.5-bit/stage MDAC in switched-opamp (SO).

The previously reported SO MDAC is shown in Figure 3.14 [20] [21]. It is noted that floating switches are removed and replaced by a switched-opamp. This opamp only works in half clock cycle for the amplification. In the next phase, the opamp turns off and feedback capacitor, C_f, is reset by shunting to ground. Without floating switches, the sampling capacitor, C_s, and feedback capacitor, C_f, are forced to permanently connect to the previous stage's output and around the opamp, respectively. For setting the stage gain of two, theses two capacitors are sized in the

ratio of 2:1. The additional capacitors, C_{ls}, are required for fed the reference voltages. They have the same size of C_f. With above setting, the feedback factor of SO MDAC is only 1/4, and additional capacitors are added to the opamp's loading. For fair comparison of SC and SO MDACs, we assume the loading from the next stage in both case is equivalent. Since the allowable signal swing at the opamp output of the low-voltage SO circuits is considerably smaller than that of the high-voltage SC circuits, the SO circuits may further need to use larger capacitors to maintain the same dynamic range by reducing the thermal noise. Thus, the SO MDAC is inherently slower than its SC counterpart due to smaller feedback factor and larger capacitive load.

3.4.2 Loading-Free Architecture

A newly reported SO MDAC known as loading-free architecture is shown in Figure 3.15. The loading-free architecture significantly reduces the capacitive loading of the opamp and thus increases the operation speed [19] [20].

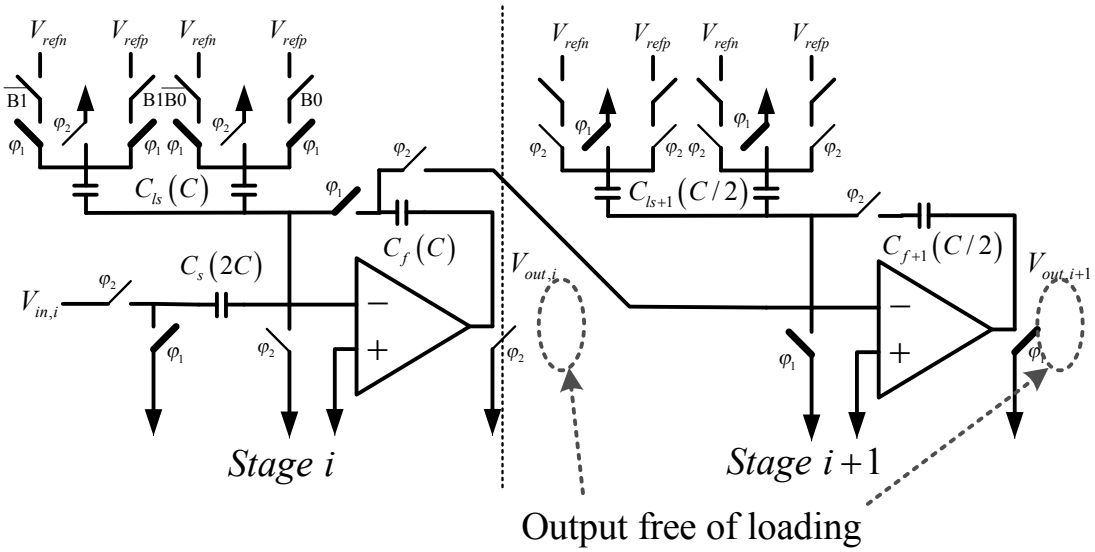


Figure 3.15 Loading-Free architecture.

Its working principle is described as follow: during φ1, the stage i is in amplification phase, and the output signal is stored in the feedback capacitor C_f, while in φ2, the charge stored in C_f is transferred to C_{f+1}. The difference from conventional SO MDAC is that the charge stored in C_f is not reset in φ2, so the feedback capacitor C_f still stores the output voltage information during φ2. Then, we can remove the dedicated sampling capacitor from stage i+1, and make use of C_f to replace the sampling capacitor for stage i+1 in φ2. Hence, the opamp output is free from loading of the next stage's sampling capacitors. The additional capacitor, C_{ls}, is still required for fed the reference voltage. To achieve a stage gain of two, C_f has to be half of C_s and C_{f+1} has to be half of C_f. Hence, the choice of downscaling factor of 1/2 is perfectly suitable for the load-free architecture. The C_{ls} is in the same size of C_f and the C_{ls+1} is in the same size of C_{f+1}.

By using feedback capacitors in both phases for different functions, the dedicated large sampling capacitor from next stage is removed and the capacitive loading of the opamp is reduced. As illustrated in Figure 3.14 with downscaling factor of 1/2 , the capacitive load of conventional SO MDAC stage is given by

$$\begin{aligned} C_L &= \left[(C_s + C_{ls}) \| C_f \right] + C_{s+1} + C_{other} \\ &\approx \left[(2C + C) \| C \right] + C/2 \end{aligned} \tag{3.22}$$

where C_{s+1} is the sampling capacitance of next stage with the value of C/2 and C_{other} is the sum of capacitance from opamp's common-mode feedback (CMFB), sub-ADC, etc, assuming that is small enough to be neglected. Loading-free architecture eliminates the last term, C_{s+1} and reduces C_L to only (3/4)C. Hence, the loading-free architecture is more suitable for high speed operation compared with conventional SO MDAC architecture.

The settling speed of MDACs is determined by the closed-loop bandwidth as discussed above, which can be expressed as following for single pole opamp

$$\mathrm{BW} = gm / C_L \times f \tag{3.23}$$

where the *gm* is the transconductance of the opamp, C_L is the output loading capacitance, and *f* is the feedback factor. For the same opamp design, the *gm* factor can be neglected. As shown in Figure 3.16 with downscaling factor of 1/2, the output loading capacitance of SC MDAC is equal to

$$\begin{aligned} C_L &= \left(C_s \| C_f\right) + \left(C_{s+1} + C_{f+1}\right) \\ &= \left(C \| C\right) + \left(C/2 + C/2\right) = \left(3/2\right)C \end{aligned} \tag{3.24}$$

, and the feedback factor is equal to

$$f = C_f / \left(C_s + C_f\right) = 1/2 \tag{3.25}$$

Compared with loading-free architecture, the C_L of SC architecture is the double of the reduced output capacitive loading, which is (3/4)C. However, the loading-free SO MDAC has smaller feedback factor. Be the same with conventional SO MDAC, the feedback factor of loading-free architecture is only 1/4. From above discussion, we can find that the loading-free architecture is not faster than SC architecture. Even thought its output capacitive loading is reduced, its feedback factor is small.

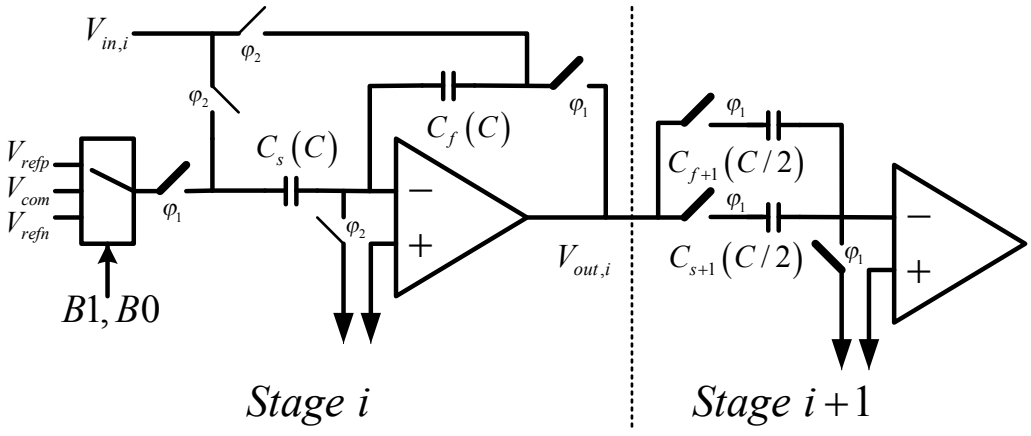


Figure 3.16 SC MDAC with downscaling factor of 1/2.

3.4.3 Improved Loading-Free Architecture

Figure 3.17 shows the newly proposed loading-free architecture. Its working principle is described as follow: in φ_1, the *stage i* is in amplification phase, and the output voltage is stored in the feedback capacitor C_f, while in φ_2, the *stage i+1* changes to amplification phase, and the feedback capacitor C_f in *stage i* becomes the sampling capacitor in *stage i+1*, at the same time. In the other word, the capacitor C_f is also shared between *stage i* as a feedback capacitor and *stage i+1* as a sampling capacitor, so the opamp output can be free from the sampling capacitor of the next stage, and the principle is like the previously reported loading-free architecture. However, the difference is that the C_{ls} capacitor in Figure 3.15 is removed and the voltage V_{DAC} is directly fed by the C_s capacitor. Without the C_{ls}, not noly the feedback factor *f* is enhanced, but also the output capacitive loading CL is decreased.

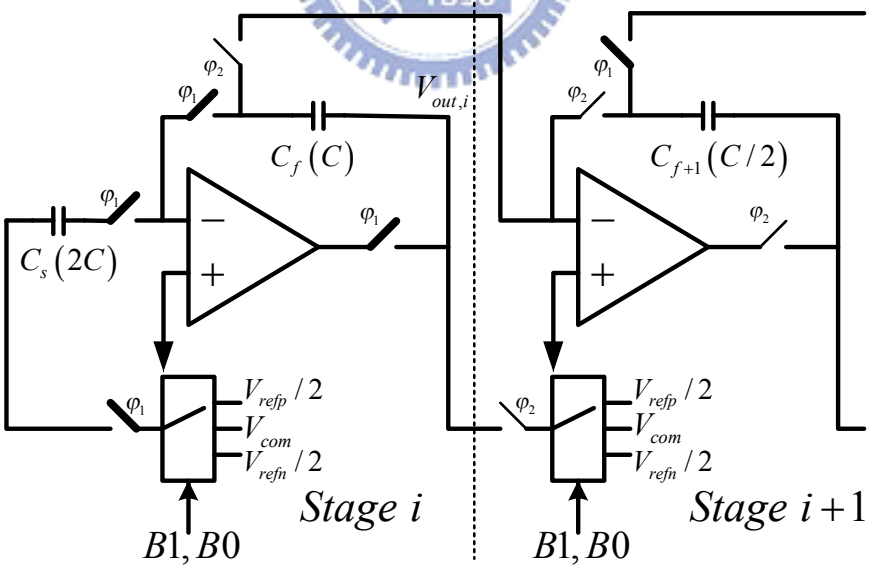


Figure 3.17 Improved Loading-Free architecture.

The feedback factor *f* in Figure 3.17 is equal to

$$f = C_f / \left(C_s + C_f \right) = 1/3 \tag{3.26}$$

and the C_L is equal to

$$C_L = \left(C_s \| C_f \right) = \left(2C \| C \right) = \left(2/3 \right) C \tag{3.27}$$

Because the C_s is two times of the C_f, the reference voltage should be reduced half, as the $V_{rep}/2$ and the $V_{ren}/2$ shown in Figure 3.17. By removing the C_{ls} and using the loading-free architecture, the proposed MDAC can achieve a even high bandwidth. The comparison of SC architecture, previously reported loading-free architecture and the newly improved loading-free architecture is shown in Table 3.1. We can find that the bandwidth of the proposed architecture has 50% improvement compared to the others, if the gm factor is neglected.

Table 3.1 Comparison of different architectures.

Pipelined ADC Architecture	**SC**	**Loading-Free**	**Improved Loading-Free**
Feedback factor *f*	1/2	1/4	1/3
Loading capacitance C_L	(3/2)C	(3/4)C	(2/3)C
Bandwidth BW=$gm/C_L \times f$	*gm**(1/3)C	*gm**(1/3)C	*gm**(1/2)C

3.5 Summary

In this work, two pipelined ADCs are implemented. The first design is a 10-bit pipelined ADC with opamp-sharing technique and the block diagram is shown in Figure 3.18. For a 10-bit pipelined ADC, the eight middle stages are separated into four opamp-sharing stages, each of which resolves four-bit output codes. Input signal is first sampled by the front-end S/H, and then passes through the four opamp-sharing stages and the last flash ADC. Final output codes are completed by the digital error correction logic. The required clock signals for different blocks are driven by single clock generator circuit through clock buffers.

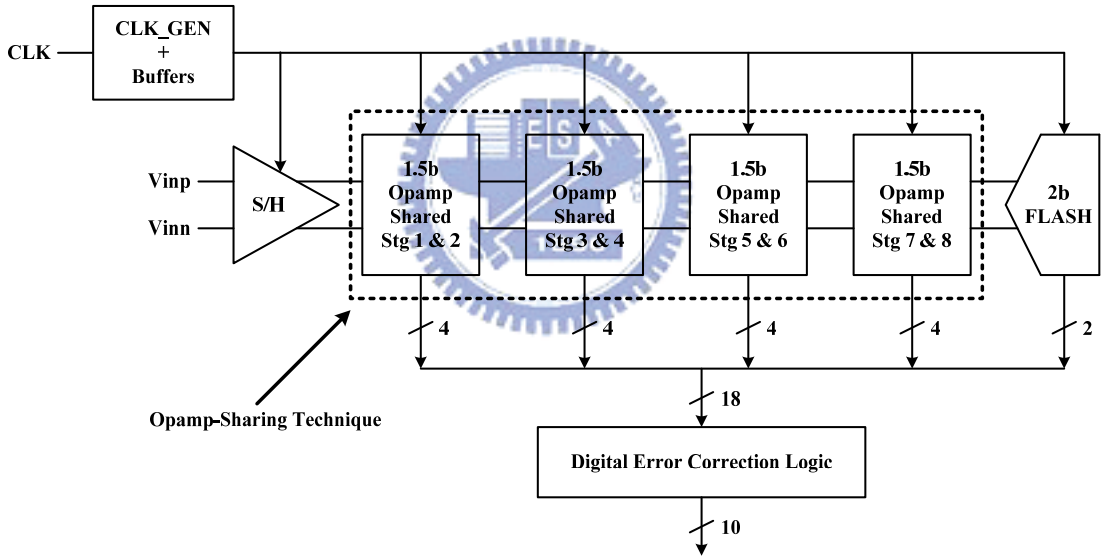


Figure 3.18 Pipelined ADC with opamp-sharing technique.

The second design is a pipelined ADC with both improved loading-free architecture and opamp-sharing technique which is shown in Figure 3.19. The improved loading-free architecture is only used in sample-and-hold and stage 1-2, and the following stage 3 to 6 use opamp-sharing technique. In order to achieve a stage gain of 2, the downscaling factor of 1/2 is chosen, so the capacitor size will be

reduced half per stage. However, considering the thermal noise (kT/C), small capacitor size introduces large thermal noise, so the proposed loading-free architecture will not be implemented in too many stages. Besides, since the operation speed for a pipelined ADC is dominated in the sample-and-hold and the former stages, the improved loading-free architecture is only used in the sample-and-hold and stage 1 and 2. Opamp-sharing technique is also used in stage 3 to 6 for better power and area efficiency.

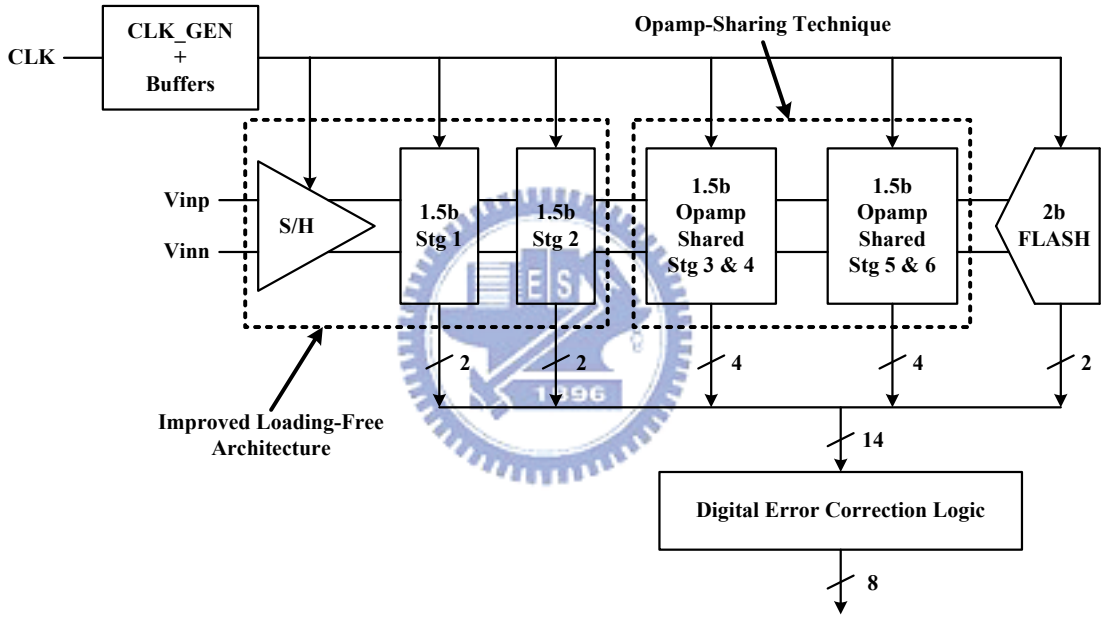


Figure 3.19 Proposed pipelined ADC with improved loading-free architecture and opamp-sharing technique.

Chapter 4

Implementation of Proposed Pipelined ADC

4.1 Introduction

In this section, we discuss the circuits implemented in the proposed pipelined ADCs. First, the MDAC circuits and the opamp are introduced. The main analog signal processing is realized by MDAC circuits, so they dominate the main performance of the pipelined ADC. The opamp is the most important analog component and the non-ideal effects, such as finite dc gain and bandwidth, are discussed in detail. Then, the flash quantizers are introduced following. For low power consumption, dynamic comparator is chosen. After the analog components, the digital circuits, such as register arrays and digital error correction logic, are described. A multi-phase clock generator is implemented to produce the non-overlapping clock phases. Finally, the simulation results and the layouts of the proposed two pipelined ADCs would be presented with their floor plans separately.

4.2 Design of MDAC

The multiplying digital-to-analog converter (MDAC) in each stage of pipelined ADC is the most significant component of the whole converter, since it realizes the main analog signal processing. Opamp with high gain and high bandwidth is required to maintain high accuracy and high operation speed, and switch issue also should be considered carefully. Above two topics will be discussed in the former of this chapter,

and then the circuits implemented with improved loading-free architecture and opamp-sharing technique are introduced. For achieving better performance, some skills, such as bottom-plant sampling technique, and the tradeoff about the circuit would also be described in the last part.

4.2.1 Gain-Boosting Telescopic Opamp

The most important analog element of the pipelined ADC is the operation amplifier, which is not only used in the S/H but also needed for each pipelined stage. The limitations of the opamp such as finite dc gain, finite bandwidth, stability and linearity should be well considered, since the settling behavior of the opamp determines the speed and the accuracy of the pipelined ADC. Fast settling requires a high unity-gain frequency to support, whereas accurate settling needs a high dc gain to accomplish. However, the realization of a operation amplifier that combines high dc gain with high unity-gain frequency is very difficult.

Multi-stage amplifier may have high dc gain and large output swing for different stages functionality. However, it is not suitable for high speed application because there is at least one pole in each stage, which decreases the bandwidth and stability of the feedback system. Besides, the power consumption of multi-stage amplifier is much higher than the single-stage amplifier. Single-stage amplifier, such as telescopic and folded-cascode architectures, is usually designed for high speed requirement and also capable for high gain due to cascode stage with large output impedance. Among the single-stage amplifiers, telescopic amplifier has the highest bandwidth. Besides, the power consumption of telescopic amplifier is also less than folded-cascode architecture. Nevertheless, the output swing of telescopic amplifier is smaller than other amplifiers.

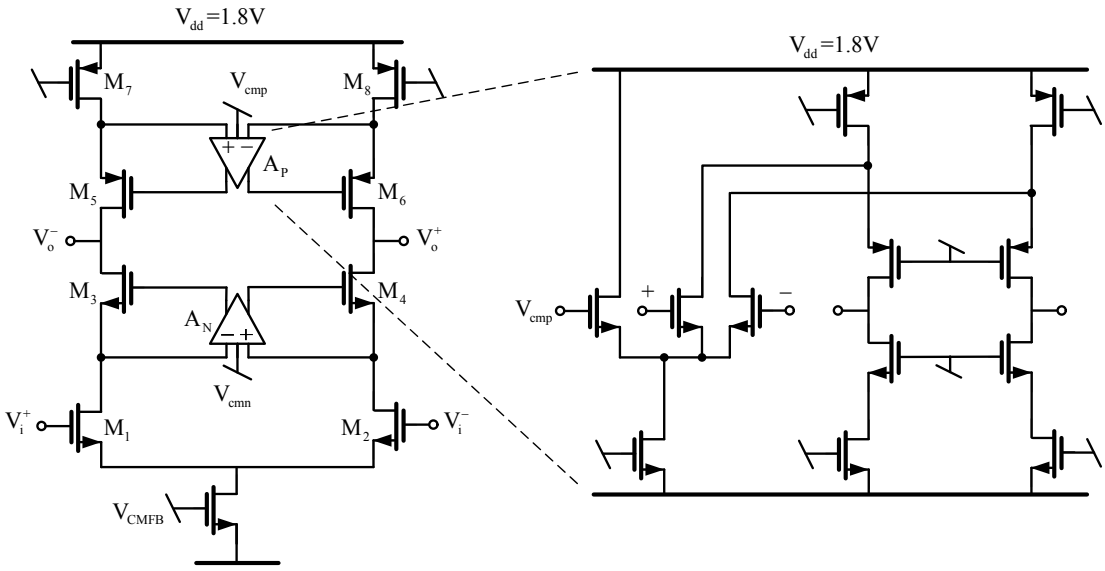


Figure 4.1 Gain-boosting telescopic opamp.

Figure 4.1 illustrates the fully differential telescopic opamp. This opamp is adopted in the S/H stage and as well as the six pipelined stages for considering the high bandwidth and low power consumption. For the requirement of higher resolution accuracy, it is necessary to use the gain enhancement technique to increase the dc gain of the opamp. Gain-boosting technique is employ in the opamp without adding additional stages or stacking more cascade devices, which would consume more power or decrease the signal swing [22] [23].

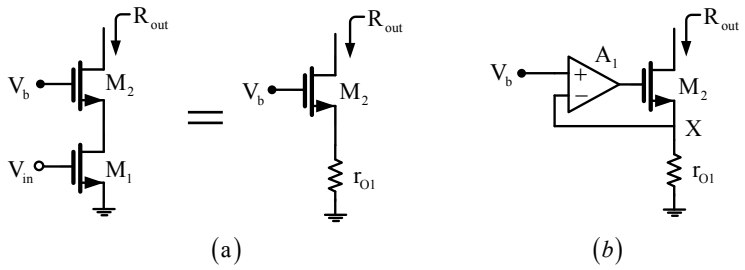


Figure 4.2 Increasing the output impedance by feedback.

Consider the simple cascade in Figure 4.2(a), whose output impedance is given by $R_{out} = g_m r_{O2} r_{O1}$, where M_1 operates as a degeneration resistor, sensing the output current and converting it to a voltage. As illustrated in Figure 4.2(b), the idea is to

drive the gate of M_2 by an amplifier that forces V_X to be equal to V_b. Thus, voltage variations at the drain of M_2 now affect V_X to a lesser extent because A_1 "regulates" this voltage. With small variations at X, the current through r_{O1} and hence the output current remain more constant, yielding a higher output impedance. By using small signal model, the output impedance can be proved that

$$R_{out} \approx A_1 g_{m2} r_{O2} r_{O1} \tag{4.1}$$

Concluding that output impedance can be "boosted" the value of A_1 without stacking more cascade devices on top of M_2 [23]. However, the gain-boosting circuit would slow down the settling tines for large-signal transients compared with the simple cascode circuit. In order to make this "slow" settling component fast enough, the unity-gain frequency of the added gain boosting circuit should be higher than the 3-dB bandwidth of the circuit, which is the closed-loop bandwidth of an SC circuit, and must be lower than the second-pole frequency of the main amplifier for reasons concerning stability [22].

The open-loop gain of the telescopic opamp can be represented as

$$A = G_m \times R_{out} \tag{4.2}$$

where the transconductance G_m is approximately equal to g_{m1} and the output impedance R_{out} enhanced by boosting amplifiers A_p and A_n can be calculated as

$$R_{out} \approx \left[A_N \left(g_{m3} + g_{mb3} \right) r_{O3} r_{O1} \right] \| \left[A_P \left(g_{m5} + g_{mb5} \right) r_{O5} r_{O7} \right] \tag{4.3}$$

Assuming total output capacitance is C_L and the second pole is far away from the origin, the unity-gain frequency ω_u of the telescopic opamp is given by

$$\omega_u = \frac{g_{m1}}{C_L} \tag{4.4}$$

and the dominant pole is equal to

$$\omega_{P1} = \frac{\omega_u}{A} = \frac{g_{m1}}{C_L \times g_{m1} R_{out}} = \frac{1}{R_{out} C_L} \tag{4.5}$$

which locates at the output of the opamp.

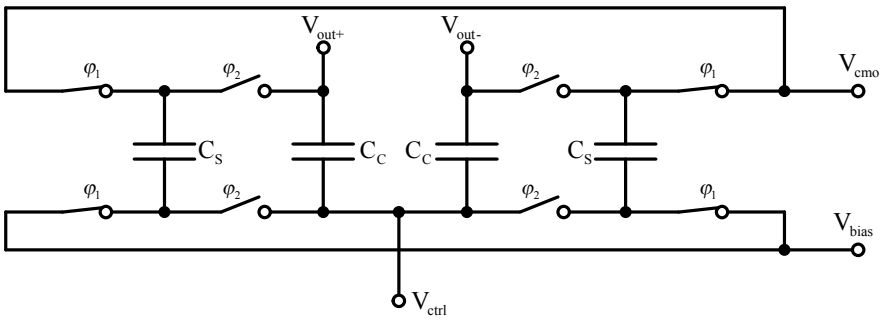


Figure 4.3 A switched-capacitor CMFB circuit.

Since the opamp is adopted in fully-differential architecture, the common-mode feedback (CMFB) circuit is necessary to well define the output common-mode voltage, usually being the half of supply voltage. Figure 4.3 shows the implemented CMFB circuit, which is based on the switched-capacitor circuits and allows a large output signal swing. In this approach, capacitors labeled C_C generate the average of the output voltages, which is used to create control voltages V_{ctrl} for the opamp current sources. The dc voltage across C_C is determined by capacitors C_S, which is used to sense the voltage different from the desired output common-mode voltage V_{cmo} to the desired bias voltage V_{bias}. This circuit acts much like a simple switched-capacitor low-pass filter having a dc input signal. Normally, all of the switches would be realized by minimum-size n-channel transistors only to reduce charge injection effect, except for the switches connected to the outputs, which might be realized by transmission gates (i.e., parallel n-channel and p-channel transistors both having minimum size) to accommodate a wider signal swing [4].

Figure 4.4 shows the AC simulation results of the fully-differential gain-boosting telescopic opamp, including open-loop gain and phase margin in five process corners (TT, FF, SS, FS, SF), which are listed in Table 4.1. The simulated performance is summarized in Table 4.2.

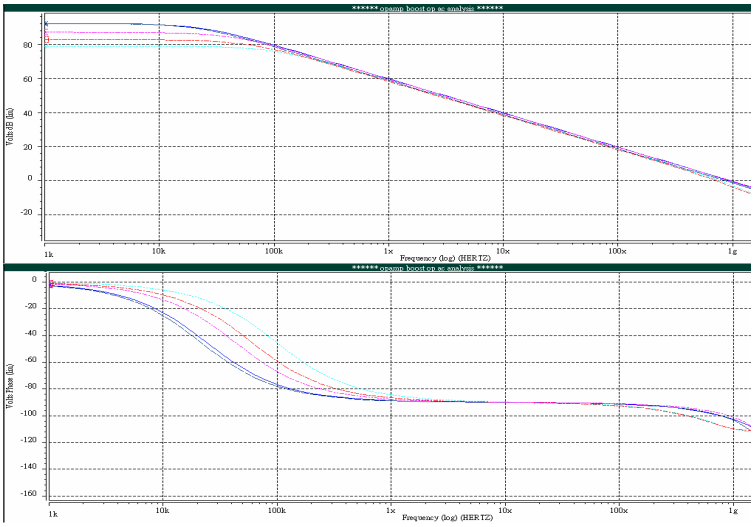


Figure 4.4 AC simulation results of the opamp.

Table 4.1 Simulation results of the opamp in five process corners.

Corner	TT	FF	SS	FS	SF
DC Gain（dB）	92.2	78.9	92.2	82.7	87.1
Phase Margin（deg）	78.2	73.1	78.6	73.3	79.5
Unity-Gain Freq.(MHz)	950.5	770.3	879.5	727.6	974.2

Table 4.2 Performance summary of the opamp.

Gain-Boosting Telescopic Opamp (TT)	
Process	TSMC 0.18μm 1P6M process
Power Supply	1.8V
DC Gain	92dB
Phase Margin	78°
Unity-Gain Frequency	950MHz
Slew Rate	1V/ns
Common-Mode Voltage	0.9V
Signal Swing	$1.6V_{PP}$
C_L	3.5pF
Power	13.3mW

4.2.2 Bootstrapped Switch

In advanced CMOS processes, the decreased supply voltage makes analog NMOS and PMOS transistor switches difficult to have sufficient over-drive voltage, even the transmission gate switch also faces the challenge of reduced dynamic range. Besides, when the switch turns on, the on resistance varies with the different input signal since the gate-to-source voltage of the switch is the difference between the gate voltage and the input signal. The signal-dependent resistance makes the sampled input to be distorted at output and degrades the linearity, especially when the supply voltage is even scaled down. One widely used method to reduce the on resistance signal dependency is the gate-voltage boosting switch, which is implemented in the front-end S/H circuit to enhance the linearity of the sampled signal.

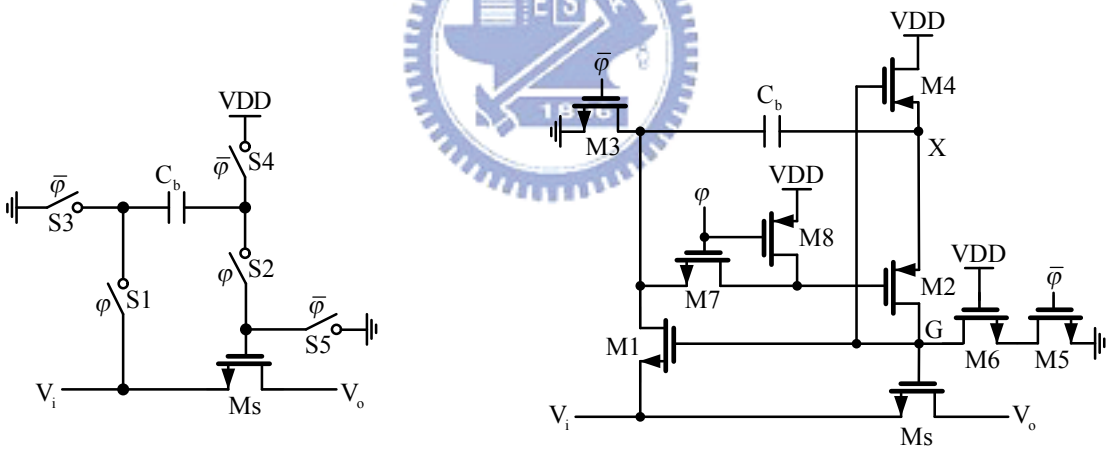


Figure 4.5 (a) The basic circuit of bootstrapped switch and

(b) Transistor-level implementation.

Figure 4.5(a) illustrates the basic circuit of the gate-voltage boosting switch, which contains the signal switch Ms together with five additional switches (S1-S5), and a charging capacitor C_b. During $\bar{\varphi}$ phase, C_b is charged to VDD through S3 and S4, and Ms is turned off by connecting the gate of Ms to ground through S5; while

during φ phase, a loop is formed between gate and source of Ms, that is, VDD stored in C_b is treated as a constant V_{GS}. The on-resistance is given by

$$R_{on} = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{DD} - V_t)}$$

This guarantees the switch resistance independent on V_i and decreases signal distortions. Besides, this switch technique makes the charge injection error to be a constant offset instead of a signal-dependent error deteriorating the accuracy.

Figure 4.5(b) shows the implementation of the bootstrapped switch circuit. Note that transistors M2 and M4 have a little difference from general design. During φ phase, the voltage at X is charged to VDD+V_i, that is, the source voltage of M2 and M4 would be higher than their substrate voltage which is usually connected with VDD. This problem would cause leakage currents due to a biased-forward junction diode between the source and substrate. Thus, sources and substrates of M2 and M4 should be tied together at node X. furthermore, M6 is added to reduce the Vds stress on M5 [24]. The simulation result with a rail-to-rail sinusoidal input signal is shown in Figure 4.6.

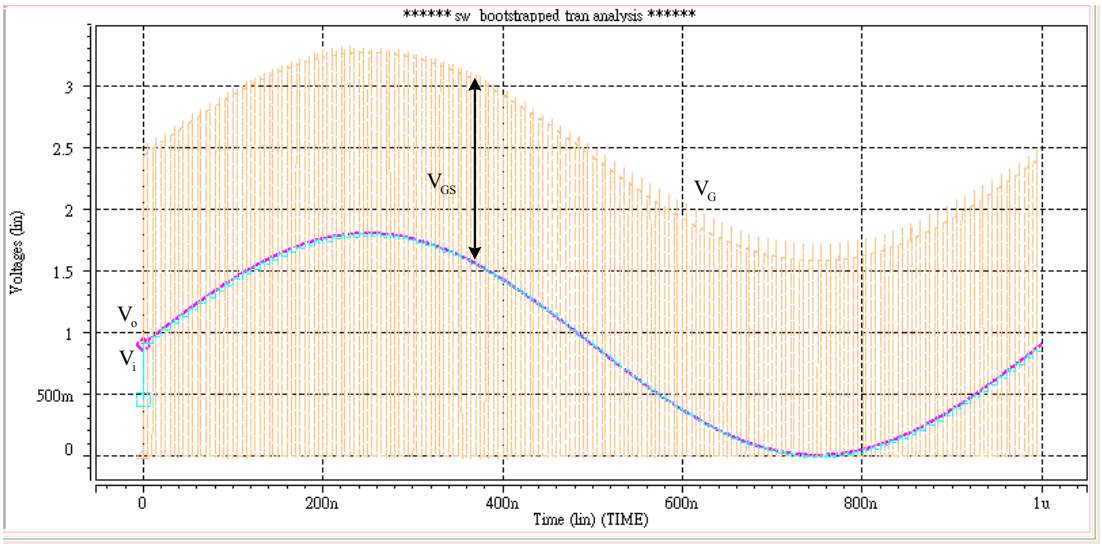


Figure 4.6 Simulation result of the bootstrapped switch.

4.2.3 S/H and Stage 1, 2 with Improved Loading-Free Architecture

Considering the capacitor size scaled down per stage, the improved loading-free architecture is only used in S/H and stage 1, 2. Figure 4.7 illustrates the implemented circuit in singled-ended version, although the real circuit is fully differential. This architecture is operating under two non-overlapped phases, $\phi 1$ and $\phi 2$. Based on SO MDAC, only NMOS switches are required in the proposed MADC architecture except the switches connected to Sub-ADCs. The switch size has a tradeoff between the accuracy and operation speed, since small switch size has less charge injection error but causes higher on resistance, which slows down the settling behavior. By sharing the feedback capacitor between successive stages, the signal memory effect will reduce the stage accuracy, so higher opamp dc gain is require for 8-bit resolution. Considering the thermal noise effect, C is chosen to be 1.6pF, thus the minimum capacitor size (C_{f+2}) is 0.4pF and the maximum capacitor size (C_s) is 3.2pF.

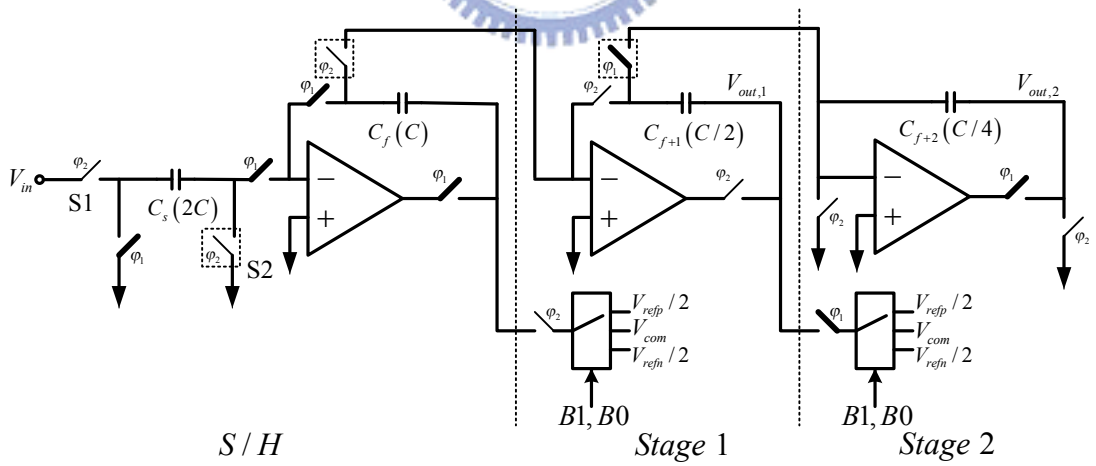


Figure 4.7 Implementation of improved loading-free architecture in S/H and Stage 1, 2.

In order to reduce the charge injection errors, bottom-plate sampling technique is also used. For example in the S/H stage, when it is in the sample phase, switches S1

and S2 are on. If S1 and S2 turn off at the same time, there would be two times of charge injection errors (2Δ) stored in C_s. By using bottom-plate sampling technique, that is, S2 turns off a litter faster than S1, since the turned-off S2 floats the bottom plate of C_s, the charge injection error from S1 would not enter C_s. Thus, the error term could be reduced to Δ, which comes from S2. As shown in Figure 4.7, the switches with a dotted block would be driven by a faster clock phase (ϕ 1a and ϕ 2a), so total four clock phases are required as shown in Figure 4.8. The simulated output waveforms of the stage 1 and stage 2 with a sinusoidal input signal are shown in Figure 4.9.

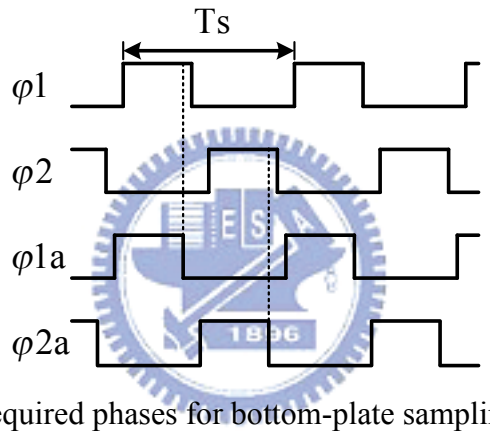


Figure 4.8 Required phases for bottom-plate sampling technique.

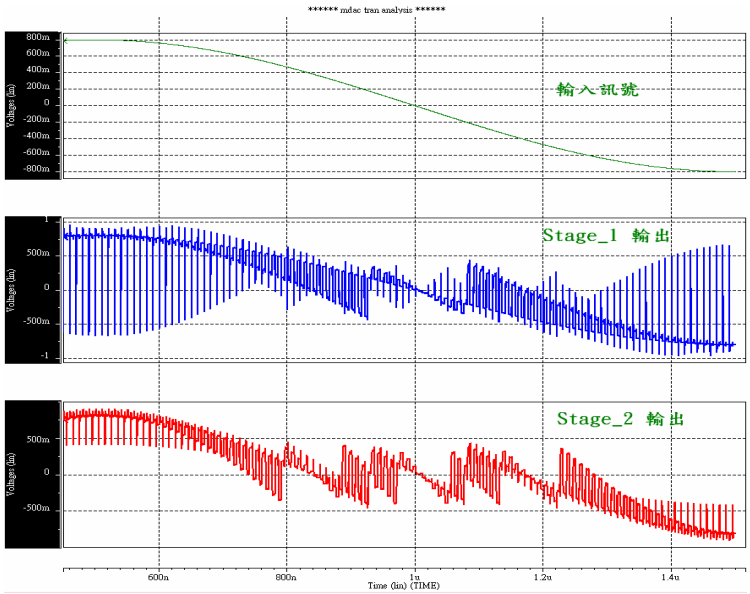


Figure 4.9 Simulation result of stage 1 and stage 2.

4.2.4 Implementation of Opamp-Sharing Technique

Conventional switched-capacitor MDAC with opamp-sharing technique is used in stage 3 to stage 6 of the proposed pipelined ADC. The implementation of opamp-sharing technique between two successive stages in singled-ended version is illustrated in Figure 4.10 [16] [18]. All the switches are realized by transmission gates, except switches M1~M4, which are realized by NMOS transistors. The switch size also has a tradeoff between accuracy and speed as discussed above and the bottom-plate sampling technique is used, too. By using opamp-sharing technique, the number of required opamps for pipelined stages can be reduced half, thus both power dissipation and chip size can be significantly decreased.

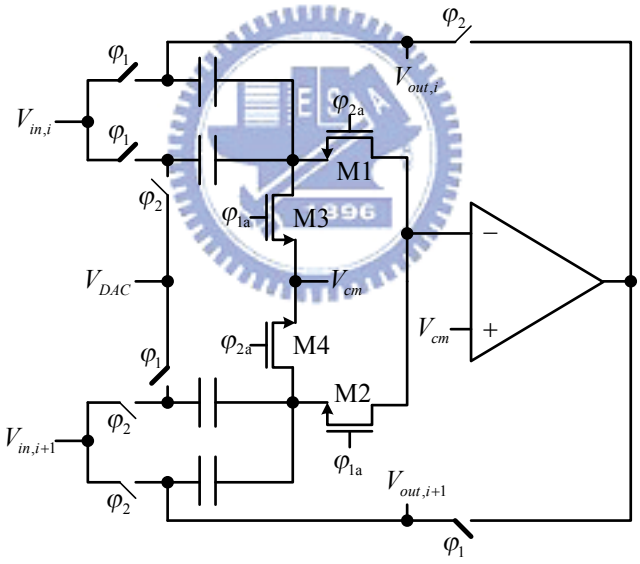


Figure 4.10 MDAC sharing opamp between successive stages.

4.3 Flash Quantizers

Two kinds of flash quantizers are used in the pipelined ADC. One is the 1.5-bit Sub-ADC used in each pipelined stage and the other is the 2-bit flash ADC which is implemented in the last pipelined stage. The quantizers are composed of several

comparators and some sample logic gates. In order to reduce the power consumption, dynamic comparator is chosen and the detail discussions of the designed circuits are described as follows.

4.3.1 Dynamic Comparator

Dynamic comparators are used in the flash quantizers of the pipelined ADC. Without preamplifier, the comparator has less power consumption but larger offset voltage. Since the 1.5-bit per stage architecture can tolerate $\pm V_{ref}/4$ comparator offset by using digital error correction logic, the latch-type comparator would be suitable for the application. The implemented dynamic comparator is shown in Figure 4.11, and the static latch circuit is used to stretch the output of the comparator to the full period. When CK is low, the output nodes of the regenerative latch, X and Y, are reset to VDD and the current source, M0, is turned off. At the same time, the sources of M5 and M6 are also set to VDD, thus M5 and M6 are cut off. Therefore, there is no power dissipation when CK is low. When CK is high, the current source, M0, is switched on. The output nodes, X and Y, and the sources of M5 and M6 are free from VDD. By comparing the input differential voltage with the built-in threshold voltage which is determined by $W3/W1\times(V_{RP}-V_{RN})$, the output result would be amplified by the two inverters in series (M5~M8) and be stored on the static latch. Because the threshold voltages are $\pm V_{ref}/4$ for 1.5-bit per stage architecture, W1 is chosen to be equal to $4\times W3$. For the 2-bit flash ADC in the last stage, W1 is chosen to be equal to $2\times W3$. Besides, both the input pairs (M1~M4) and the current source (M0) are in saturation straightly after latching the signal, that makes the comparator less sensitive to device mismatch and have small offset error. Dynamic comparator is very suitable for flash quantizers in pipelined ADC with low power consumption and easy to be realized,

even though it has larger offset which can be calibrated by DEC logic [25] [26]. The simulation results of $\pm V_{ref}/4$ threshold voltage for 1.5-bit/stage and $\pm V_{ref}/2$ threshold voltage for the 2-bit flash ADC are shown in 4.12.

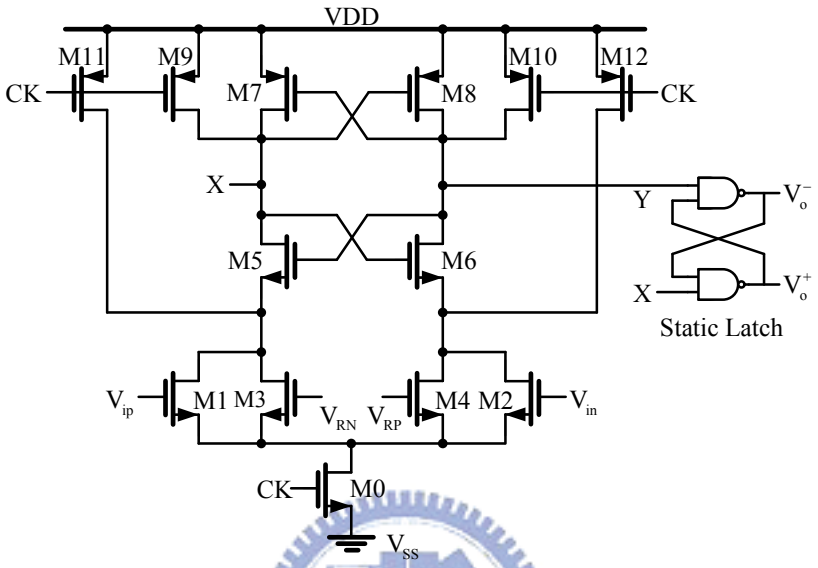
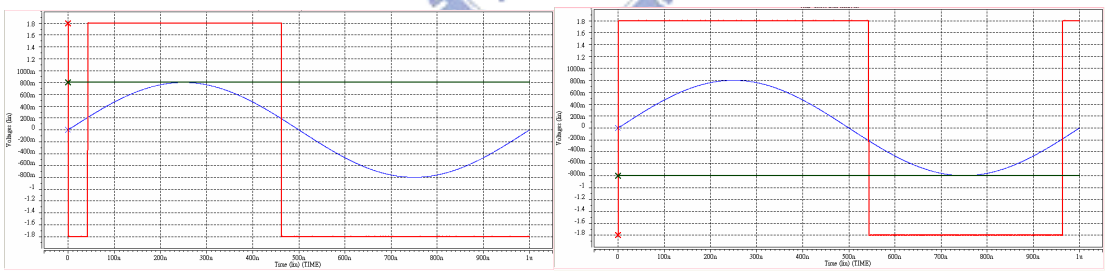
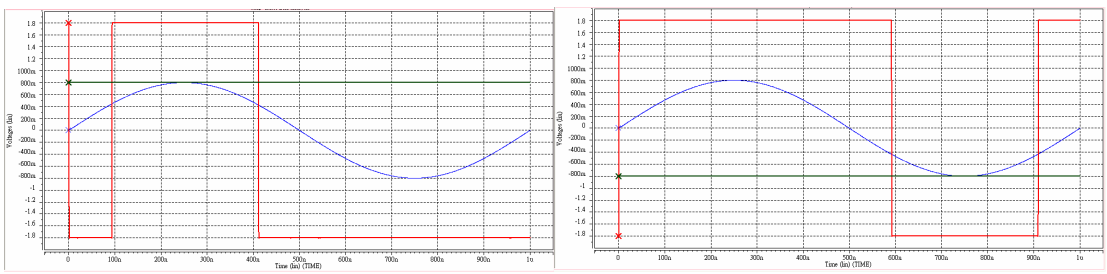


Figure 4.11 Dynamic comparator.



(a)



(b)

Figure 4.12 Simulation results of comparators (a) with $\pm V_{ref}/4$ threshold voltage (b) with $\pm V_{ref}/2$ threshold voltage.

4.3.2 Sub-ADC

The Sub-ADC used in each pipelined stage for 1.5-bit/stage architecture consists two fully-differential comparators and some sample logic gates, as shown in Figure 4.13. The Sub-ADC compares the input signal with two decision levels, $\pm V_{ref}/4$, and generates three digital output codes 00, 01 or 10. [MSN, LSB] are the output codes of the 1.5-bit Sub-ADC and [X Y Z] are the control signals for MDAC. Table 4.3 summaries the digital output codes [MSB, LSB] and the control signals [X Y Z] for differential input signal. Figure 4.14 shows the simulation result of the 1.5-bit Sub-ADC.

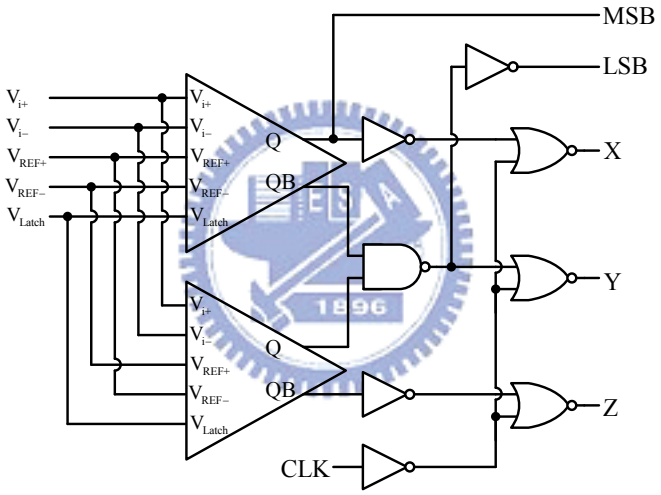


Figure 4.13 1.5-bit Sub-ADC.

Table 4.3 Digital output codes and control signals of 1.5-bit sub-ADC.

Input Signal V_{in}	Digital Output Codes [MSB, LSB]	Control Signals [X Y Z]
$\frac{+V_{ref}}{4} < V_{in} < +V_{ref}$	[1, 0]	[1 0 0]
$\frac{-V_{ref}}{4} < V_{in} < \frac{+V_{ref}}{4}$	[0, 1]	[0 1 0]
$-V_{ref} < V_{in} < \frac{-V_{ref}}{4}$	[0, 0]	[0 0 1]

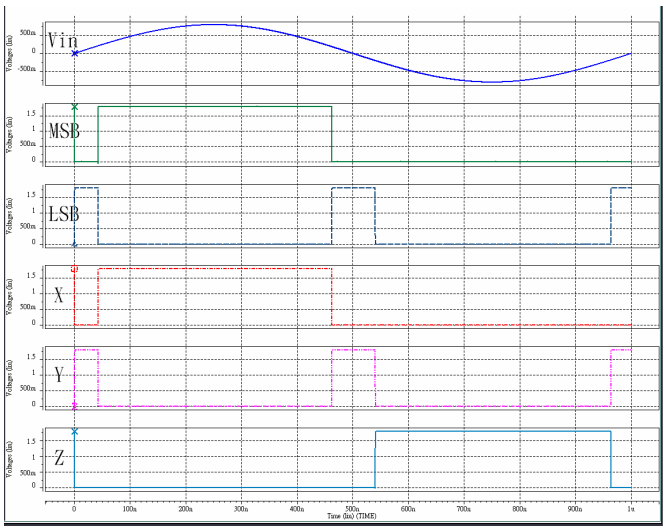


Figure 4.14 Simulation results of output code and control signals.

4.3.3 2-Bit Flash ADC

A 2-bit Flash ADC is used in the last stage of the pipelined ADC. The Flash ADC is similar to the 1.5-bit Sub-ADC as shown in Figure 4.15. The three fully-differential comparators determine three threshold voltages $-V_{ref}/2$, 0 and $V_{ref}/2$, and divide the input signal into four segments which are refer to four digital codes 00, 01, 10 or 11 respectively. The simulation result of the 2-bit Flash ADC is shown in Figure 4.16.

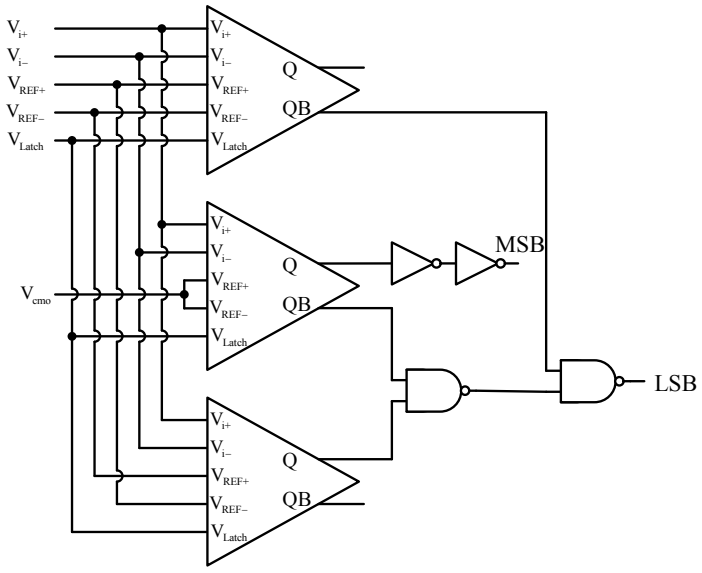


Figure 4.15 2-bit Flash ADC.

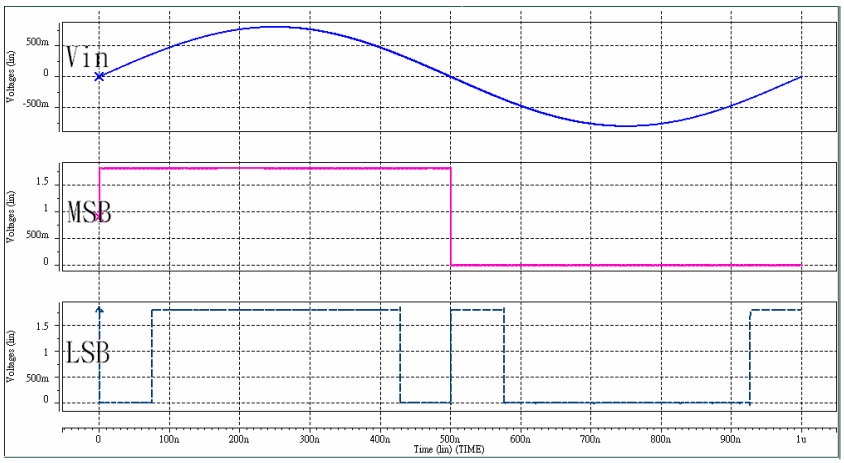


Figure 4.16 Simulation result of the 2-bit Flash ADC.

4.4 Delay Elements and Digital Error Correction Logic

The tail section of the pipelined ADC is composed of large register arrays and the digital error correction logic which is followed by the output buffers, as shown in Figure 4.17. The register arrays are used to synchronize the stages' output data, and then this data would be processed by the correction logic to generate the final 10-bit output code (DO9, … DO0). The digital error correction logic for 1.5-bit/stage architecture can be easily realized by eight full adders and the output buffers can just be implemented by inverter chains. A positive edge-triggered and single-phase clocked D-latch is adopted in the design of shift register which is also shown in Figure 4.17. Because only one clock phase is needed in the register, the complexity of the register arrays can be reduced.

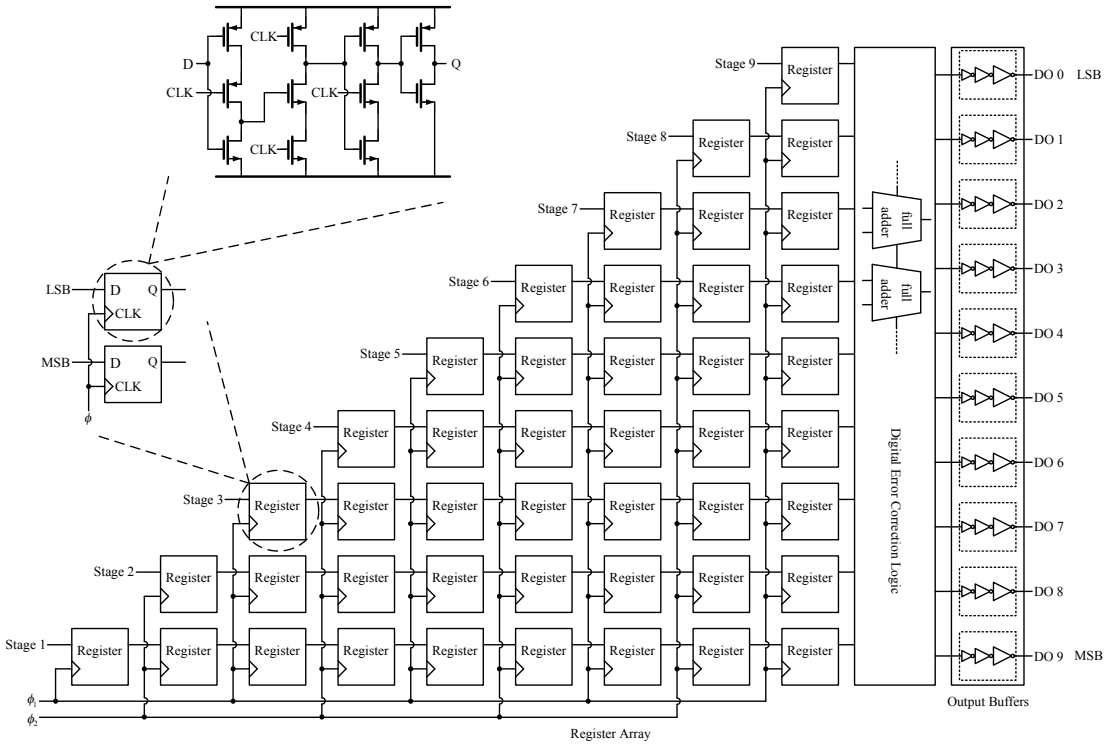


Figure 4.17 Register array and digital error correction logic.

4.5 Clock Generator

The multi-phase non-overlapping clock generator used in the pipelined ADC is illustrated in Figure 4.18. This circuit generates two non-overlapping clock phases ϕ_1 and ϕ_2 which are used to determine the main operations of sample and hold for the ADC. The advance clock phases ϕ_{1a} and ϕ_{2a} are used for bottom-plane sampling technique. The inverters in Block 1 are used to adjust the non-overlapping width between ϕ_1 and ϕ_2, and the inverters in Block 2 are used to increase the delay between ϕ_1 (or ϕ_2) and ϕ_{1a} (or ϕ_{2a}). A transmission gate is also used to balance the transition times of these two clock paths for better symmetrical clock phase and the clock buffers for each clock phase are required for driving the capacitance loading of the MOS gates and the layout lines. The simulation results of these four output clock phases are shown in Figure 4.19.

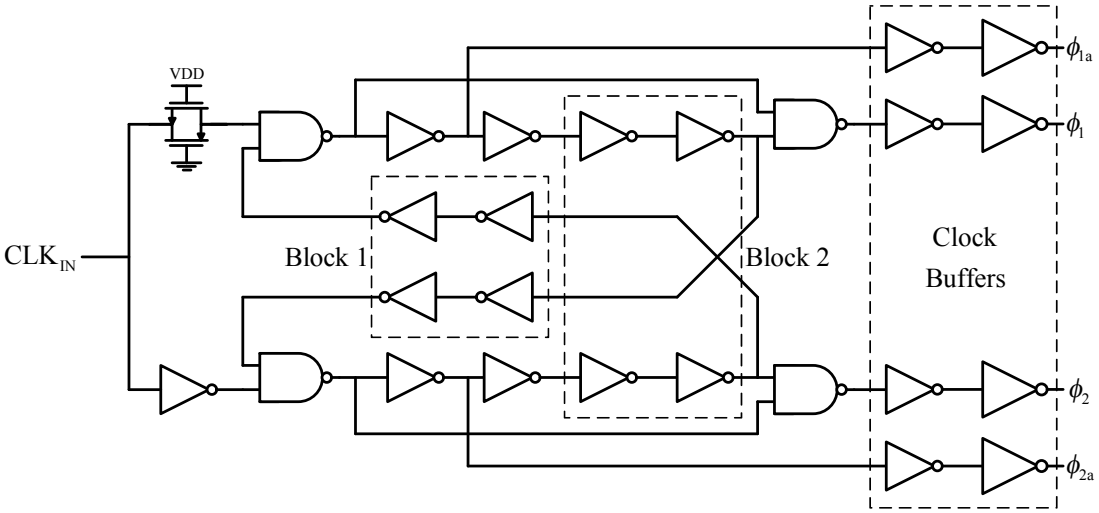


Figure 4.18 Multi-phase non-overlapping clock generator.

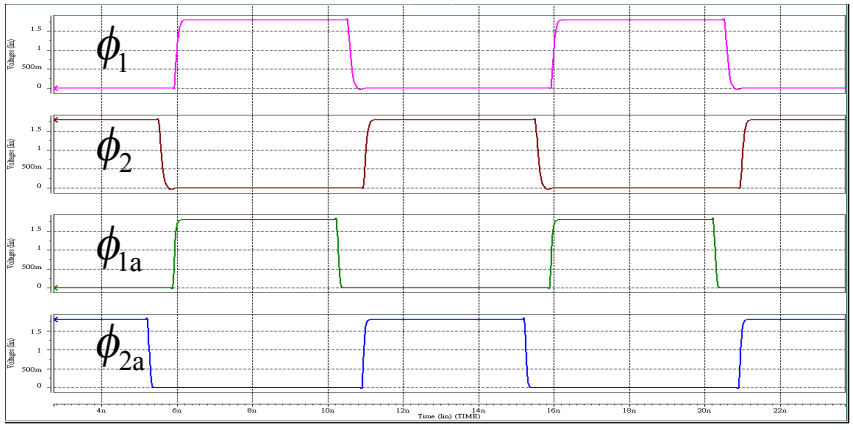


Figure 4.19 Simulation results of the non-overlapping clock phases.

4.6 Simulation Result of Proposed Pipelined ADCs

In this section, the simulation results of two proposed pipelined ADCs discussed in Section 3.5 would be described. The first design is a 10-bit 100MS/s pipelined ADC with opamp-sharing technique. For a power spectrum simulation, a sinusoidal input signal is applied. Usually we take 2^N points from the ADC's output and

converter the binary data to the reference value with an ideal DAC, and then load these 2^N values into Matlab to execute Fast Fourier Transform (FFT). For a 10-bit ADC, N would be best larger than 10. The FFT spectrums of this ADC at 100MHz sampling rate in different corners with different input frequencies are shown in Figure 4.20, which are analyzed by 1024 points output data. This ADC achieves 71.18dB SFDR, 59.95dB SNDR, 9.67bit ENOB for a 5MHz input signal at 100MS/s, and achieves 68.67dB SFDR, 58.59dB SNDR, 9.44bit ENOB for a 40MHz input signal.

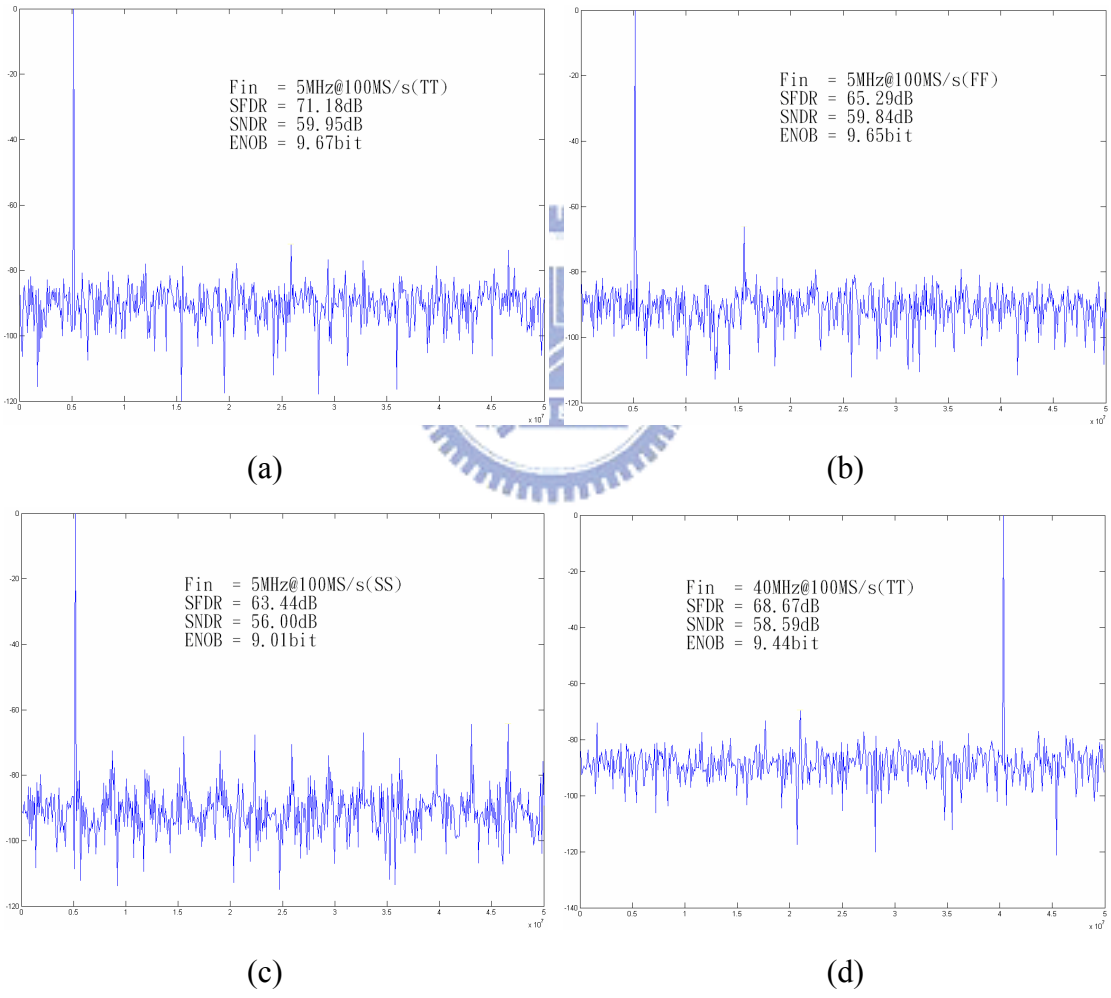


Figure 4.20 FFT spectrums for the first pipelined ADC output with (a)(b)(c) 5MHz sinusoidal input in different corners and (d) 40MHz sinusoidal input.

In addition to the sinusoidal input, we can also apply a ramp input signal to analyze the non-linearity characteristic of the ADC. The simulated results of the DNL and INL for the pipelined ADC are shown in Figure 4.21, and the maximum DNL and INL are 0.4 LSB and 1.07 LSB respectively. Figure 4.22 shows the dynamic performance with various input frequencies, and Table 4.4 summaries the simulation results of the first pipelined ADC.

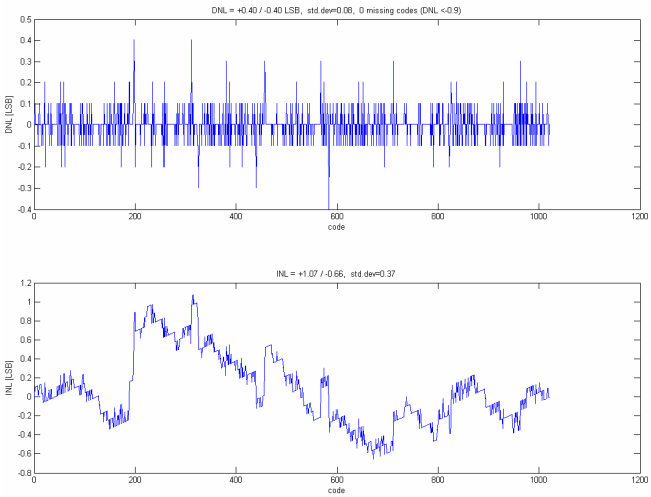


Figure 4.21 Simulation results of DNL and INL for the first pipelined ADC.

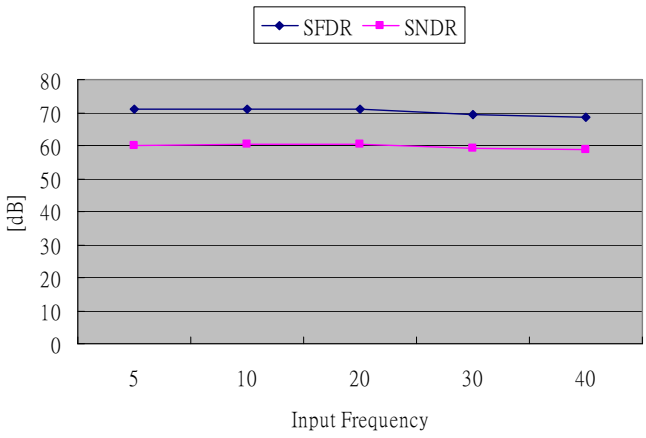
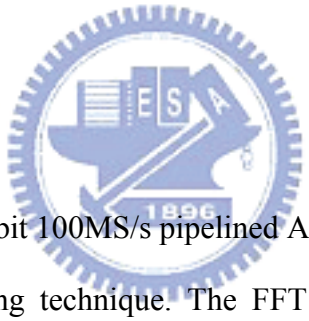


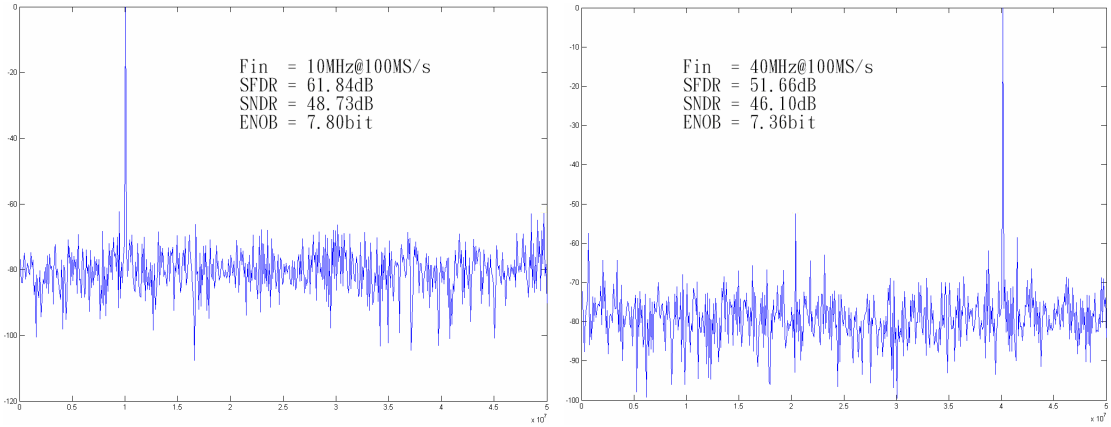
Figure 4.22 Dynamic performance versus input frequency for the first pipelined ADC.

Table 4.4 Performance summary of the first pipelined ADC.

Process	0.18μm CMOS process
Power Supply	1.8V
Signal Swing	$1.6V_{PP}$
Common-Mode Voltage	0.9V
Conversion Rate	100MSample/s
Resolution	10 Bits
SFDR	71.18dB (Fin=5MHz), 68.67dB (Fin=40MHz)
SNDR	59.95dB (Fin=5MHz), 58.59dB (Fin=40MHz)
ENOB	9.67-bit (Fin=5MHz), 9.44-bit (Fin=40MHz)
DNL	-0.4/+0.4 LSB
INL	-0.66/+1.07 LSB
Chip size	$1.95mm^2$
ADC core power	72.6mW



The second design is an 8-bit 100MS/s pipelined ADC with improved loading-free architecture and opamp-sharing technique. The FFT spectrum simulated results at 100MHz sampling rate with different input frequency are shown in Figure 4.23. This ADC achieves 61.84dB SFDR, 48.73dB SNDR, 7.8bit ENOB for a 10MHz input signal, and achieves 51.66dB SFDR, 46.10dB SNDR, 7.36bit ENOB for a 40MHz input signal. The simulated results of the DNL and INL are shown in Figure 4.24, and the maximum DNL and INL are 0.38 LSB and 0.88 LSB respectively. Figure 4.25 shows the dynamic performance with various input frequencies, and Table 4.5 summaries the simulation results of the second pipelined ADC.



(a) (b)

Figure 4.23 FFT spectrums for the second pipelined ADC with (a) 10MHz (b) 40MHz sinusoidal input

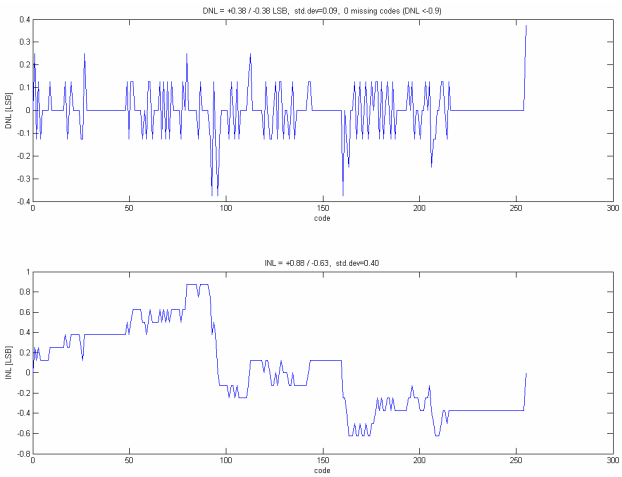


Figure 4.24 Simulation results of DNL and INL for the second pipelined ADC.

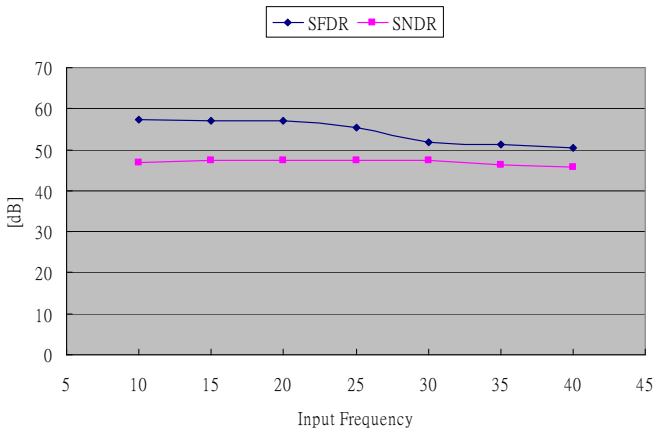


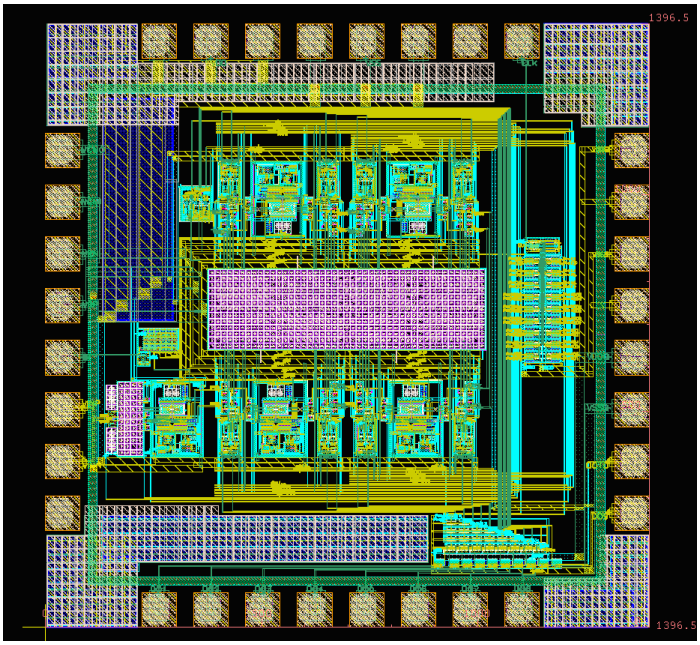
Figure 4.25 Dynamic performance versus input frequency for second pipelined ADC.

Table 4.5 Performance summary of the second pipelined ADC.

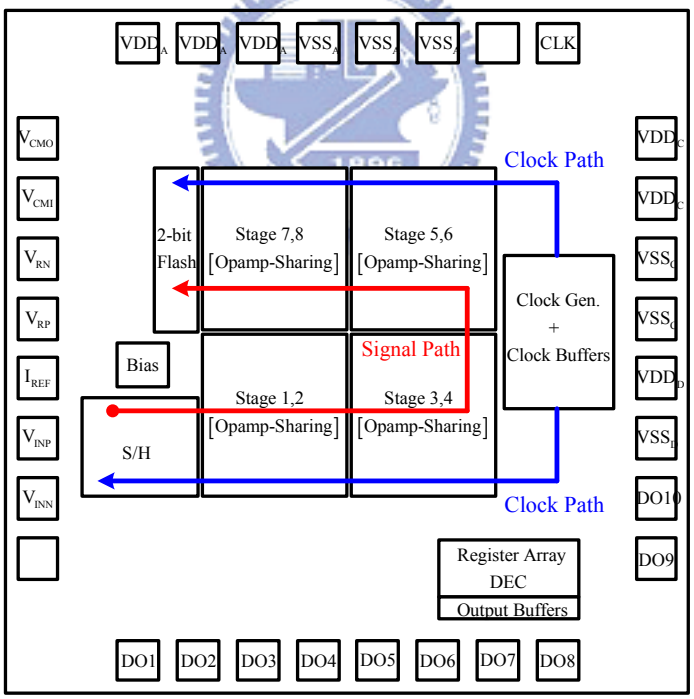
Process	0.18μm CMOS process
Power Supply	1.8V
Signal Swing	$1.6V_{PP}$
Common-Mode Voltage	0.9V
Conversion Rate	100MSample/s
Resolution	8 Bits
SFDR	61.84dB (Fin=10MHz), 51.66dB (Fin=40MHz)
SNDR	48.73dB (Fin=10MHz), 46.10dB (Fin=40MHz)
ENOB	7.80-bit (Fin=10MHz), 7.36-bit (Fin=40MHz)
DNL	-0.38/+0.38 LSB
INL	-0.63/+0.88 LSB
Chip size	$1.89mm^2$
ADC core power	78mW

4.7 Layout and Floor Plan

The layouts and floor plans of the proposed two pipelined ADCs are shown in Figure 4.26 and Figure 4.27 separately. The layout level design is another important topic for the mixed-signal chip. Therefore, some techniques are also used in this layout to decrease the noise from process variations and reduce the distortion effect. In order to avoid the digital noise enter analog circuits, the power lines for analog and digital parts are separated. Since the substrate of whole NMOS should be connected together, we connect the substrate of NMOS to the analog ground that would isolate the digital noise from the buck. Common-centroid layout of a diff-pair is widely used in the devices which are sensitive to mismatch consideration, such as input pairs and tail current devices [6]. Besides, larger capacitor arrays and cross-coupling techniques are also used for better resistance of process variations [23]. Multiple pads for VDD and VSS are adopted for reducing the self-inductance, too.

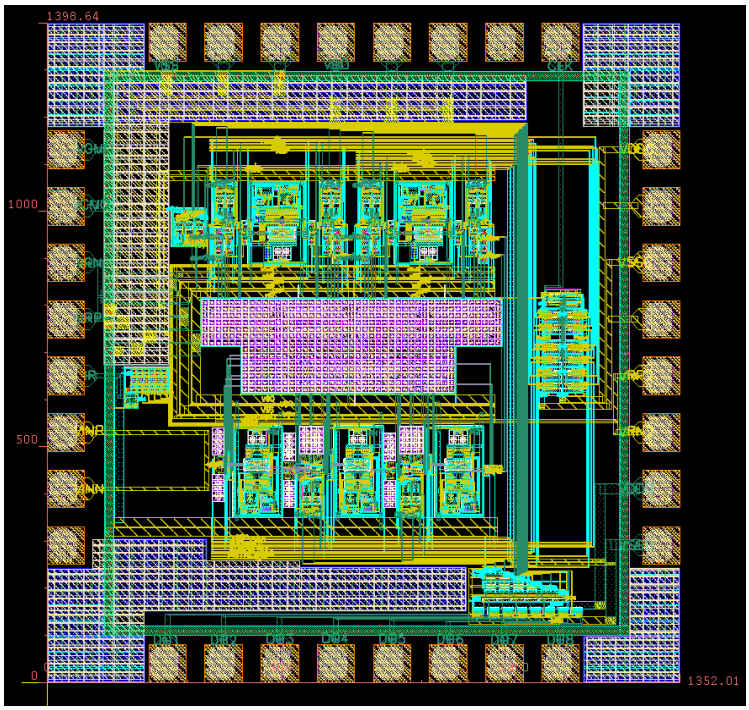


(a)

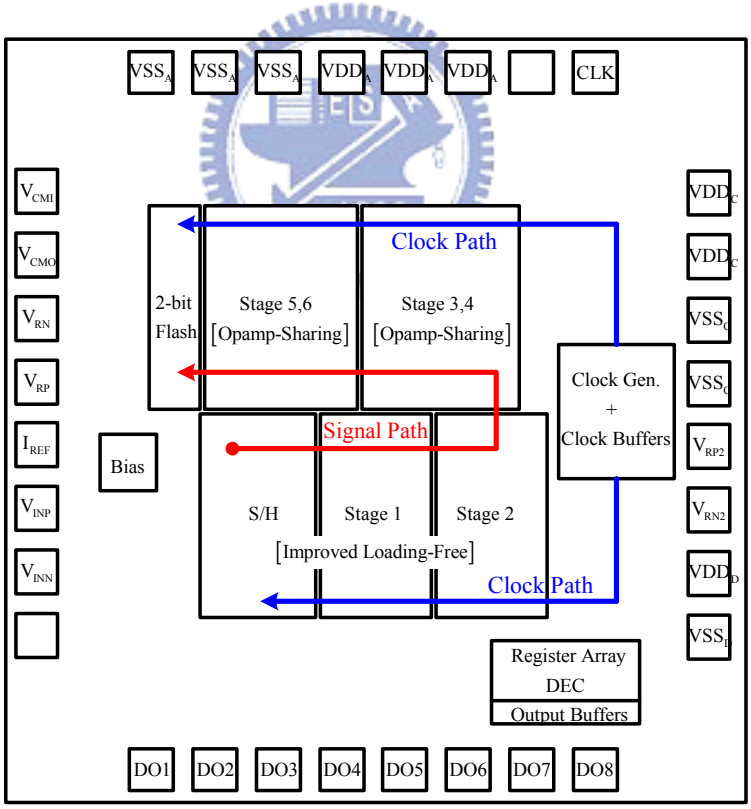


(b)

Figure 4.26 (a) Layout and (b) floor plan of the first pipelined ADC.



(a)



(b)

Figure 4.27 (a) Layout and (b) floor plan of the second pipelined ADC.

4.8 Summary

The design steps for the whole components of pipelined ADC have been discussed above in detail. However, the HSPICE simulations are incapable to cover all non-ideal effects caused by the layout parasitical RC or process variations. These non-ideal terms would induce noise and distortions in the measurement. Thus, for a more robust design, the layout techniques are important to reduce the mismatch effects, and simulations in different corners ensure that the circuit can tolerate wide process variations. Besides, if the noise source from measurement environment can also be considered in HSPICE, the simulation results would be more accurate.

Chapter 5

Test Setup and Experimental Result

5.1 Introduction

This chapter will present the testing environment for the first pipelined ADC including the required instruments and the component circuits on the printed circuit board (PCB). In the following, the experimental measurement results of the proposed pipelined ADC are also presented and summarized.

5.2 Test Setup

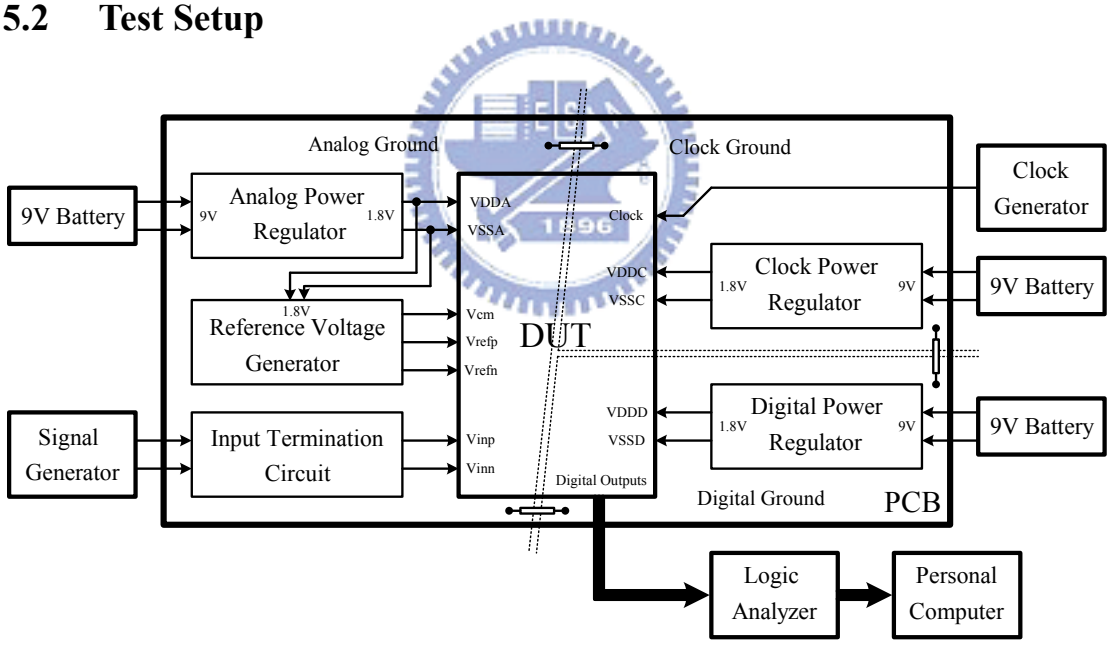


Figure 5.1 Test setup.

The schematic of the test setup used to evaluate the performance of proposed pipelined ADC is illustrated in Figure 5.1. The supply voltages for analog, digital and clock parts of the DUT are generated by separated regulator circuits and batteries. In order to prevent the noise coupling between different parts, the analog ground, digital ground and clock ground are isolated to each other. The single-ended input signal to

the DUT is provided by the signal generator, HP 8656B, as shown in Figure 5.2(a), and the system clock is generated by the clock generator, HP 8133A, as shown in Figure 5.2(b). The output bit streams of the DUT are fed to the logic analyzer, Agilent 16902A, which is also shown in Figure 5.2(c). Figure 5.3 shows a photograph of the PC board used in the experimental measurement. Details of the other components on the PCB are described below.

(a) (b)

(c)

Figure 5.2 The photographs of the (a) signal generator, (b) clock generator and (c) logic analyzer.

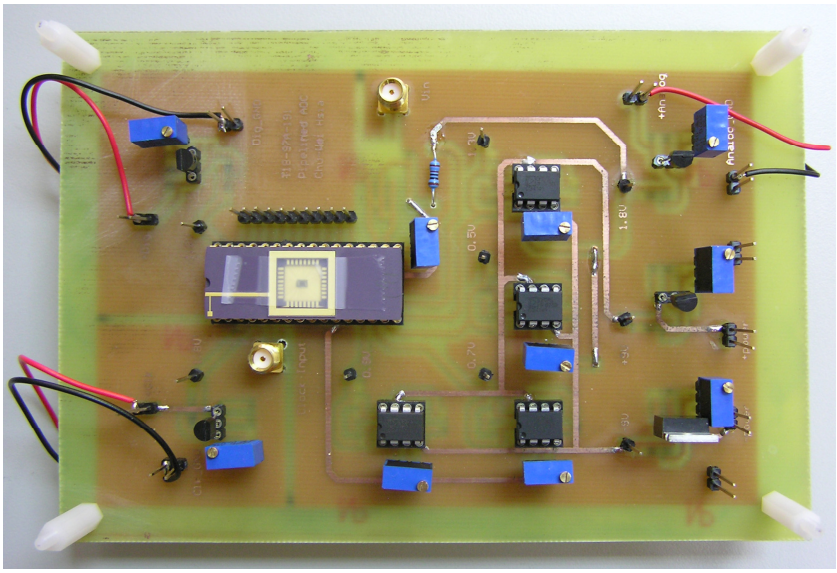


Figure 5.3 The photograph of the experimental measurement PCB.

5.2.1 Power Supply Regulator

For isolating noise signal from different parts, the power sources and grounds of analog, digital and clock are separated to each other. These three grounds on the PCB are connected to each other by a bead inductor as shown in Figure 5.1, which can short the DC value of these grounds and prevent the high frequency noise from digital and clock circuits coupling to the analog circuits.

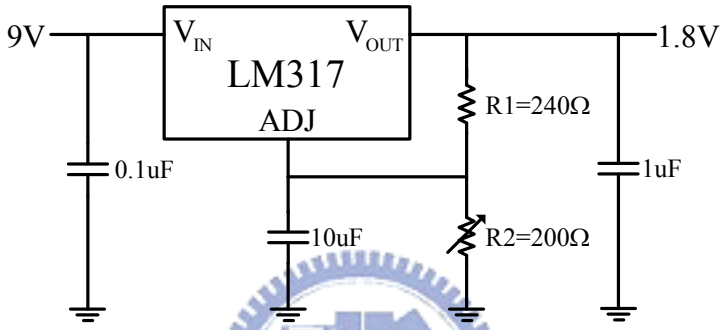


Figure 5.4 Power supply regulator.

The supply voltages for analog, digital and clock parts are generated by the application of LM317 adjustable regulators as shown in Figure 5.4. The input voltage of the regulator circuit is supplied by a 9V battery for small noise disturbance. The regulator circuit is easy to be used. Just two resistor R1 and R2 are required to determine the output voltage, and the output voltage can be expressed as

$$V_{out} = 1.25 \cdot \left(1 + \frac{R2}{R1}\right) + I_{ADJ} \cdot R2 \qquad (5.1)$$

where I_{ADJ} is the DC current that flows out of the adjustment terminal ADJ of the regulator. Usually the I_{ADJ} is too small to be neglected, thus the output voltage is mainly determined the resistance ratio [27].

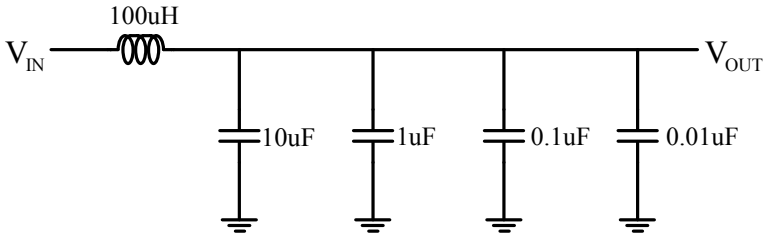


Figure 5.5 Bypass filter at the regulator output.

The output of the regulator is bypassed with a filter tank as shown in Figure 5.5. This bypassed filter network is combined by a 100uH inductor and four 10uF, 1uF, 0.1uF, and 0.01uF capacitors. The capacitor arrangement in Figure 5.5 provides decoupling of both low frequency noise with large amplitude and high frequency noise with small amplitude [28].

5.2.2 Input Termination Circuit

Since the signal source output is single-ended version, a single-to-differential circuit is needed to supply the input signal for the pipelined ADC. In this work, a RF transformer is selected to provide single-ended to differential conversion. Figure 5.6 shows the preferred circuit diagram for implementing a transformer-coupled input. The signal source is ac-coupled and fed to the primary side of the RF transformer. Since the ADC input must be biased to the correct common mode voltage, two 25Ω resistors are in series between the secondary output taps to feed the V_{CMO}.

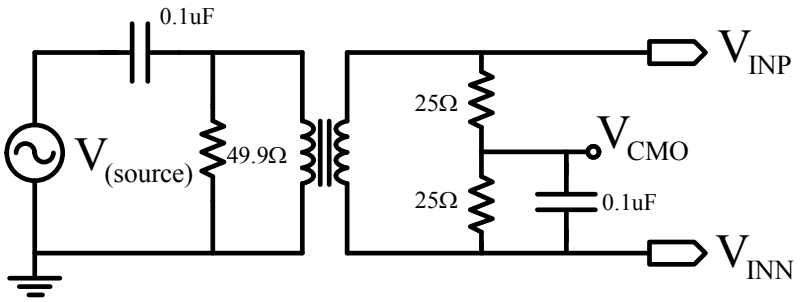


Figure 5.6 Input terminal circuit with a transformer.

5.2.3 Reference Voltage Generator

In this design, the reference voltages of the ADC have to be supplied by unity-gain buffers. Figure 5.7 illustrates an adjustable low noise dc voltage source used in the PC board [29]. The OP27 operational amplifier is implemented as a unity-gain buffer for the reference voltage set by the 5k potentiometer at its input.

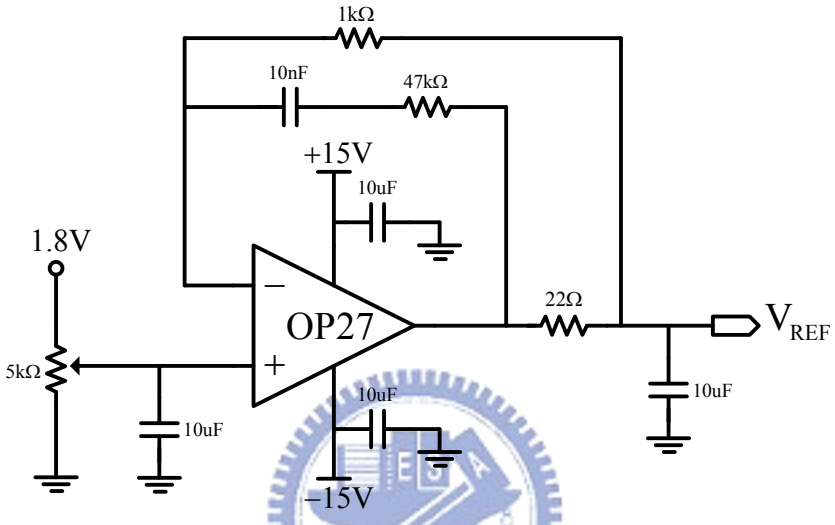


Figure 5.7 Schematic of reference voltage circuit.

Figure 5.8 shows the die photomicrograph of the experimental opamp-sharing pipelined ADC. Figure 5.9 presents the pin configuration and lists the pin assignments of the chip.

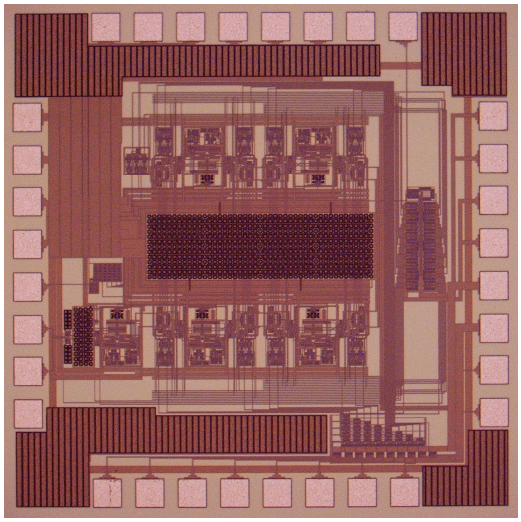
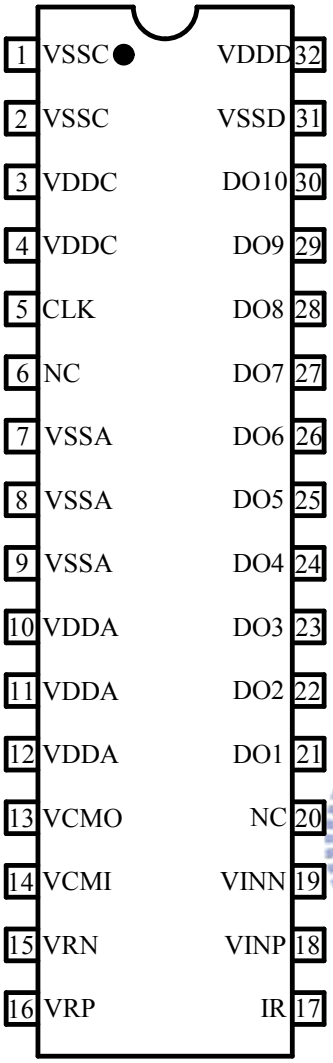


Figure 5.8 Die photomicrograph of the experimental pipelined ADC



Pin	Name	I/O	Description
1	VSSC	Power	Clock power supply
2	VSSC	Power	Clock power supply
3	VDDC	Power	Clock power supply
4	VDDC	Power	Clock power supply
5	CLK	In	System clock input
6	NC	----	No connection
7	VSSA	Power	Analog power supply
8	VSSA	Power	Analog power supply
9	VSSA	Power	Analog power supply
10	VDDA	Power	Analog power supply
11	VDDA	Power	Analog power supply
12	VDDA	Power	Analog power supply
13	VCMO	Ref.	Input common voltage
14	VCMI	Ref.	Output common voltage
15	VRN	Ref.	Reference voltage (-)
16	VRP	Ref.	Reference voltage (+)
17	IR	Ref.	Digital data output
18	VINP	In	Input signal (+)
19	VINN	In	Input signal (-)
20	NC	----	No connection
21	DO1	Out	Digital data output
22	DO2	Out	Digital data output
23	DO3	Out	Digital data output
24	DO4	Out	Digital data output
25	DO5	Out	Digital data output
26	DO6	Out	Digital data output
27	DO7	Out	Digital data output
28	DO8	Out	Digital data output
29	PO9	Out	Digital data output
30	DO10	Out	Digital data output
31	VSSD	Power	Digital power supply
32	VDDD	Power	Digital power supply

Figure 5.9 Pin configuration diagram and assignment list.

5.3 Measurement Result

The measurement results of the 10-bit 100MS/s pipelined ADC with opamp-sharing technique are shown in this section. First, a 0.1MHz input sine wave is applied to the ADC at 50MHz sampling rate. The output 10-bit streams of the DUT collected by the logic analyzer and the plot chart are shown in Figure 5.10

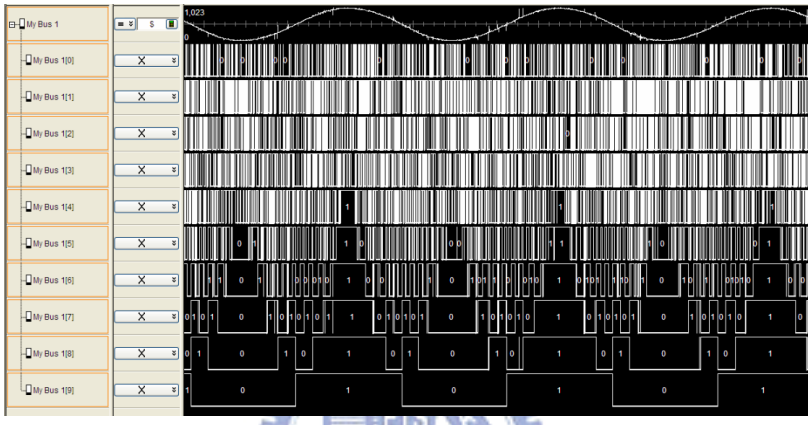


Figure 5.10 Measured results of plot chart and output 10-bit streams.

From the measured results shown in Figure 5.10, the signal to noise plus distortion ratio is calculated by collecting 32768 samples of the input signal and performing a 32768 point fast Fourier transform shown in Figure 5.11. The measured SFDR is about 50.13dB, the SNDR is about 32.34dB, the ENOB is 5.1, and the noise flow is around -65dB.

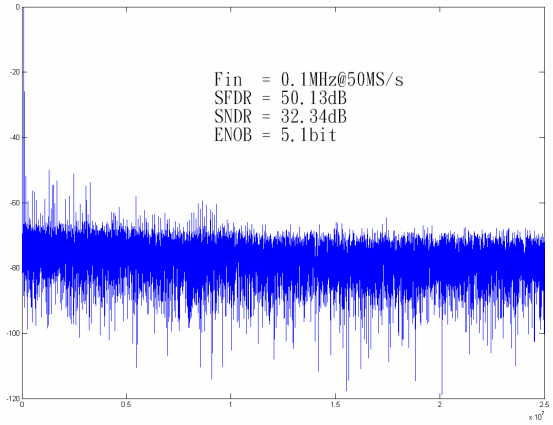


Figure 5.11 32768 point FFT for 0.1MHz input frequency at 50MHz sampling rate.

The measurement results of the DNL and INL for the pipelined ADC are shown in Figure 5.12, and the maximum DNL and INL are 4.58 LSB and 8.38 LSB respectively.

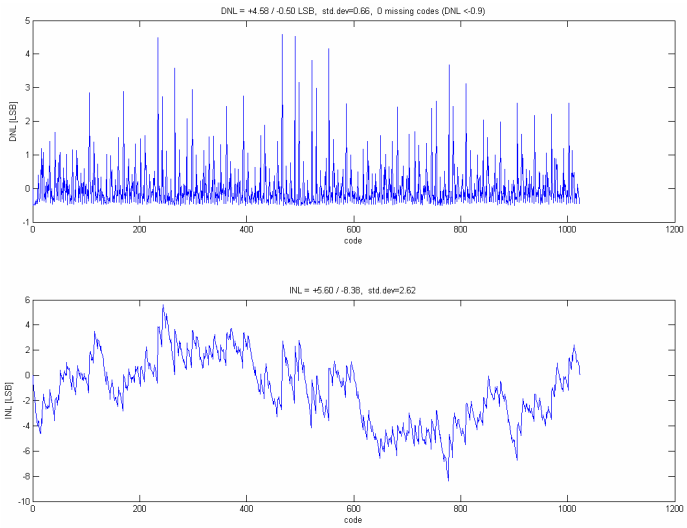


Figure 5.12 Measurement results of the DNL and INL.

The measured result is worse than the simulated performance. We think the harmonic distortion and higher noise flow might be two main reasons. Mismatch of the opamps caused by process variation induces harmonic distortion. Better layout skills might decrease the mismatch issue. The simulated noise flow is around -80dB; however, the measured result shows that the noise flow is around -65dB. Higher noise flow might be caused by the vibration of the reference voltages. The DUT needs four unity-gain buffers to supply the reference voltages, but the stability issue of the unity-gain buffer circuit on the PCB might contribute noise to the chip. One thinkable method is to make the unity-gain buffers designed on chip. Besides, the input signal, power lines and reference voltage are all coupled by the clock signal, and that also increases the noise power. An on-chip clock generator might reduce the influence of clock signal. Figure 5.13 shows the measured SNDR versus different sampling frequency with different input frequency.

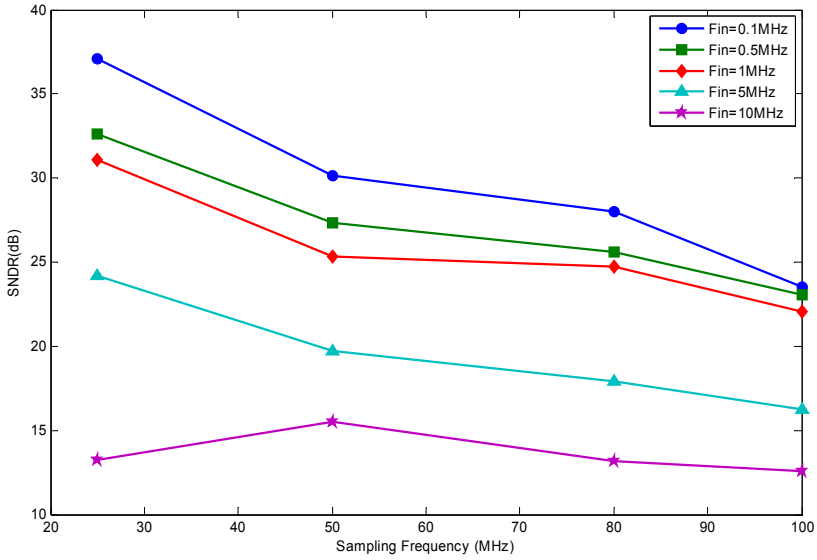


Figure 5.13 Measured SNDR versus different sampling frequency.

5.4 Summary

Table 5.1 summaries the measurement results of the 10-bit 100MS/s pipelined ADC with opamp-sharing technique.

Table 5.1 Summary of the measurement results of the testing chip.

Process	0.18μm CMOS process
Power Supply	1.8V
Signal Swing	$1.6V_{PP}$
Common-Mode Voltage	0.9V
Sampling Frequency	50MHz
SFDR@Fin=0.1MHz	50.13dB
SNDR@Fin=0.1MHz	32.34dB
ENOB@Fin=0.1MHz	5.1bits
DNL/INL	4.58/8.38 LSB
Chip size	$1.95mm^2$
ADC core power	74.8mW

Chapter 6

Conclusions

6.1 Conclusions

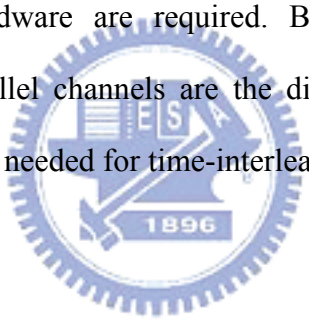
In this thesis, two pipelined ADC chips are implemented in TSMC 0.18μm CMOS process. The first design is a 10-bit 100MS/s pipelined ADC with opamp-sharing technique, and the second design is an 8-bit 100MS/s pipelined ADC with both improved loading-free architecture and opamp-sharing technique. With the improved loading-free architecture, not only the output loading capacitance of the stage amplifier is reduced, but also the feedback factor of the MDAC is enhanced, thus the ADC could achieve a higher operation speed. Besides, by using the opamp-sharing technique, the number of required opamps for the whole pipelined ADC is significantly reduced, so the power consumption and chip size would be more efficient.

The tradeoff between speed and accuracy is regularly happened in analog circuit design. Higher sampling rate usually lead to lower resolution for an A/D converter, and it also has no exception in this research. This proposed loading-free architecture enhances the stage bandwidth by sharing the capacitors between two successive stages, thus additional switches are required to accomplish this work. However, the extra parasitic resistance from these switches and the signal memorization effect of the shared capacitors both induce more distortion and noise contributions to the ADC, thus the accuracy would be reduced. Over-designed opamps and comparators might slightly reduce the non-ideal effect, but much more power consumption and hardware requirement would be demanded.

6.2 Future Works

For further reducing the power consumption of pipelined ADCs, low voltage design can be considered. Since the second pipelined ADC is based on switched-opamp architecture, it would be suitable for low supply voltage. Thus, the low-voltage opamp design would become the dominant topic. Besides, lower overdrive voltage for switch also has to be taken into account which would slow down the settling behavior and causes distortion.

In order to enhance the conversion rate, time-interleaved architecture is a very popular choice for A/D converter. The sampling rate could be sped up by parallel channels without raising the analog component specifications. However, higher power consumption and larger hardware are required. Besides, the timing skew and mismatch issue between parallel channels are the difficult problems. Thus, a well calibration technique might be needed for time-interleaved converter.



Bibliography

[1] *Data Converters*, Analog and Mixed Signal Center, TAMU

[2] J. Goes, J. C. Vital, and J. Franca, *SYSTEMATIC DESIGN FOR OPTIMISATION OF PIPELINED ADCs*, Kluwer Academic Publishers, Boston, 2001.

[3] B. Razavi, *Principles of Data Conversion System Design*, IEEE Press, 1995.

[4] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, John Wiley & Sons, Inc., 1997.

[5] R. J. V. D. Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters*, Kluwer Academic Publishers,1994.

[6] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, IEEE, Inc., 2005.

[7] D. Y. Wang and H. P. Chou, "A Two-Stage Pipelined Cyclic ADC for X/Gamma Spectroscopy", *IEEE Nuclear Science Symposium Conference Record*, vol. 2, pp. 1238-1241, Oct. 2003.

[8] S. H. Lewis and P. R. Gray, "A Pipelined 5-Msamples/s 9-bit Analog-to-Digital Converter", *IEEE J. of Solid State Circuits*, vol. SC-22, pp. 954-961, Dec. 1987.

[9] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd edition, Published by Oxford University Press, Inc., 2002.

[10] J. Goes, J. C. Vital, and J. Franca, *Systematic Design for Optimization of Pipelined ADCs*, Kluwer Academic Publishers, Boston, 2001.

[11] A. M. Abo and P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipelined Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999.

[12] S. H. Lewis, H. S. Fetterman, G. F. Gross Jr., R. Ramachandran, and T. R. Viswanathan, "A 10-b 20Msample/s Analog-to-Digital Converter," *IEEE J. Solid-State Circuits*, vol. 27, no. 3, pp. 351-358, Mar. 1992.

[13] G. Chien, "High-Speed, Low-Power, Low Voltage Pipelined Analog -to- Digital Converter", B.S. (University of California, Los Angeles) 1993.

[14] A. Abo, "Design for Reliability of Low-Voltage, Switched-Capacitor Circuits," Ph.D. Thesis, California University, Berkeley, May 1999.

[15] T. L. Hsieh, J. Han, and T. Hung, “An 8-Bit 100Ms/s 28.8mW ADC,” EECS, University of Michigan, 2003.

[16] B. M. Min, P. Kim, F. W. Bowman, III, D. M. Boisvert and A. J. Aude, “A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2031-2039, Dec. 2003.

[17] H. C. Kim, D. K. Jeong and W. Kim, “A Partially Switched-Opamp Technique for High-Speed Low-Power Pipelined Analog-to-Digital Converters,” *IEEE Trans. Circuits Syst. I*, vol. 53, no. 4, pp. 795-801, Apr. 2006.

[18] J. Li, G. Manganaro, M. Courcy, B. M. Min, L. Tomasi, A. Alam and R. Taylor, “A 10b 170MS/s CMOS Pipelined ADC Featuring 84dB SFDR without Calibration,” in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 226-227, 2006.

[19] Y. Wu, V. S. L. Cheung, and H. Luong, “A 1-V 100 MS/s 8-bit CMOS switched-opamp pipelined ADC using loading-free architecture,” in *Symp. VLSI Circuits Dig. Tech. Papers*, pp. 166-169, 2006.

[20] W. C. Song, H. W. Choi, S. U. Kwak, and B. S. Song, “A 10-b 20-Msample/s Low-Power CMOS ADC,” *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 514-521, May 1995.

[21] M. Waltari and K. A. I. Halonen, “1-V 9-Bit Pipelined Switched-Opamp ADC,” *IEEE J. Solid-State Circuits*, vol. 36, no. 1, pp. 129-134, Jan. 2001.

[22] K. Bult and G. J. G. M. Deelen, “A Fast-Settling CMOS Op Amp for SC Circuits with 90-dB DC Gain ” *IEEE J. Solid-State Circuits*, vol. 25, No. 6, pp. 1379-1384, Dec. 1990.

[23] B. Razavi, *Design of Analog CMOS Integrated Circuit*, McGraw-Hill International Edition, 2001.

[24] M. Dessouky and A. Kaiser, “Input switch configuration suitable for rail-to-rail operation of switched opamp circuits,” *Electronic Letters*, vol. 35, no. 1, pp. 8-10, 7 Jan. 1999

[25] L. Sumanen, M. Waltari, V. Hakkarainen, and K. Halonen, “CMOS dynamic comparators for pipeline A/D converters,” *IEEE ISCAS*, vol. 5, pp. 157-160, May 2002.

[26] L. Sumanen, M. Waltari, and K. Halonen, “A mismatch insensitive CMOS dynamic comparator for pipelined A/D converters,” in *Proc. ICECS*, vol. 1, pp. 32-35, Dec. 2000.

[27] STMicroelectronics, LM217, LM317, Low Current, 1.2V to 37V Adjustable

Voltage Regulator, STMicroelectronics, 2005.

[28] 何俊達, “應用雙倍取樣技術之 10 位元 200 百萬赫茲互補式金氧半導管式類比數位轉換器”, 國立交通大學電信工程研究所碩士論文, 2006.

[29] 鄭光偉, “一伏十位元 CMOS 導管式數位類比轉換器”, 國立台灣大學電機工程研究所碩士論文, 2002.