國 立 交 通 大 學

電信工程學系

碩 士 論 文

應用於超寬頻和硬碟讀取系統之
高速轉導電容式連續濾波器

High Speed Transconductance-C Continuous-Time Filters for UWB and HDD Systems

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摘　　要

本論文提出二種應用於高速系統上的轉導電容式濾波器:超寬頻系統，硬碟讀取系統。使用轉導電容式濾波器的原因是因為轉導電容式濾波器比切換式電容濾波器更適合應用在高速的系統上。但是轉導電容式濾波器的線性度比較差，所以本論文提出二種改善線性度的電路而且又適合應用在高速的系統上。

第一種電路是改良傳統源極衰減電路，使電路在較小的電阻下而能達到所需要的線性度。因為電流回饋方式擁有比電壓回饋方式大的頻寬，所以電流回饋方式比電壓回饋方式較適合於高速的應用上。另外一種電路則是改良固定輸入對汲極到源極電壓的電路，使電路更適合應用在較低電壓及高速的系統上。另外，此電路需要共模前置回饋電路來增加抑制共模信號比例(CMRR)。最後利用轉導放大器組成 4 階濾波器，在此濾波器的輸出端接上輸出緩衝器，如此濾波器在量測的時候才不會受到儀器的負載影響。

量測的結果:電流回饋式濾波器的截止頻寬為 250MHz，這是超頻寬的最低頻率。其群延遲變動約為 5ns，而在輸入訊號 80MHz 時，其第三諧波失真(HD3)為-40dB。在輸入訊號 252MHz 及 248MHz 時，其第三內調變失真(IM3)為-35dB。量測的結果: 用前置電路固定輸入對汲極到源極電壓濾波器的截止頻寬為 250MHz，這是超頻寬的最低頻率。其群延遲變動約為 5ns，而在輸入訊號 80MHz

時，其第三諧波失真(HD3)為-40dB。在輸入訊號 252MHz 及 248MHz 時，其第三內調變失真(IM3)為-36dB。

此二顆低通濾波器的製程為台積電 0.18μm CMOS 製程。源極衰減電流負回饋電路的主動面積為 0.386×0.264mm^2，功率消耗約為 42m 瓦特。用前置電路固定輸入對汲極到源極電壓電路的主動面積為 0.3515×0.3609mm^2，功率消耗約為 42m 瓦特。

High Speed Transconductance-C Continuous-Time Filters for UWB and HDD Systems

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ABSTRACT

In this thesis, two transconductance-C filters are proposed for high frequency applications of ultra wideband and hard-disk driver systems. The transconductance-C filters are more suitable than switch capacitor filters in high frequency application. However, their main drawback is the linearity, so two linearity improvement techniques are proposed in this research.

The first transconductor circuit is an improved source degeneration circuit. Source degeneration circuits usually use large values of resistors to improve linearity. Also, the current feedback works better at high frequency than voltage feedback because the former one has larger bandwidth. Hence, the proposed circuit utilizes negative current feedback to improve the linearity at high frequency, which can achieve the requirement without large resistor. The other transconductor circuit which achieves the constant drain-source voltage of the input pair is proposed. This circuit can be used in the lower power supply and high frequency applications. The transconductor circuit makes use of the common mode feedforward circuit to increase the common mode rejection ratio. Finally, two 4^{th}-order linear phase filters

by using these transconductor cells is presented.Output buffers are connected to avoid the influence of the loading in the measurement.

From the measurement results, the cutoff frequency for the filter of the current feedback transconductor circuit is about 250MHz, which is the bandwidth of the ultra wideband system. The group delay variation is less than 5ns in the passband. The third harmonic distortion (HD3) is about -40dB at 80MHz input signal. The third intermodulation distortion (IM3) is about -35dB by the two-tone measurement of 248MHz and 252MHz. From the measurement results, the cutoff frequency for the filter of Constant-V_{ds} with feedforward circuit is about 250MHz, which is the bandwidth of the ultra wideband system. The group delay variation is less than 5ns in the passband. The third harmonic distortion (HD3) is about -40dB at 80MHz input signal. The third intermodulation distortion (IM3) is about -36dB by the two-tone measurement of 248MHz and 252MHz.

The low-pass filters were fabricated by the TSMC 180-nm CMOS process. Source degeneration with negative current feedback circuit occupies a small area of $0.386\times0.264mm^2$ and the power consumption is 42mW under a 1.8V supply voltage. Constant-V_{ds} with feedforward circuit occupies a small area of $0.3515\times0.3609\ mm^2$ and the power consumption is 42mW under a 1.8V supply voltage.

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郭智龍 于 交通大學電資大樓 710 實驗室

2008.6.19

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Chapter 1

Introduction

1.1 Motivation

In the real world, the received signals are usually interfered with noise and surrounding interference, which would degrade the quality of the received signal. However, the noise and interference could be degraded by filters to receive better quality signals. Although the world we live is a digital generation, the systems communicated with real world must be dealt with analog signals, which because the signals in the real world are analog. In the recent years, high-performance high-frequency filters are required for several applications such as read/write channels for hard-disk drives (HDD), intermediate-frequency (IF) filtering for high-speed communication systems, and ultra wideband (UWB) systems.

For hard disk military, the operational frequency is 50MHz to 10GHz. The magnetic media and Preamplifier stage of the HDD system can be considered as a bandwidth-limited channel. Data is recorded on the magnetic media using binary amplitude levels. The read back signal is analog. This signal is corrupted by distortion, noise and interference. The read channel involves a lot of signal processing and tries to extract reliable binary data from the magnetic media. The corrupting noise in the signal is mostly electronic noise and media noise. But the biggest source of signal corruption is inter-symbol interference (ISI). Inter-symbol

interference is by far the dominant effect of high-density recording. The PRML technique, which helps in reducing ISI, is used widely in the industry. Most of them use an ADC, a FIR filter and a continuous time filter for channel equalization [1].

For ultra wideband systems, the operational frequency is 250MHz and above the frequency. In recent years, the Federal Communications Commission has permitted the ultra wideband technology in commercial products. With the moderate technology, the advantage of low power, high transmission rate, and low cost makes the ultra wideband being a popular issue. Owing to the property of ultra wideband, we can apply the technology in all kinds of the consumptive products, including wireless personal area network, short distance radar, and body area network in medical research or sportsman training. In communication domain, the Federal Communications Commission has mandated that the ultra wideband radio transmit with limited power, the maximum distance of 10 meter, and the transmission rate of 53Mbps to 480Mbps. The data transmission rate can be used within multimedia network connection. Besides, camera, scanner, printer, video camera, and mp3 player can connect with laptop or personal computer which includes USB 2.0 and IEEE 1394 serial port in the future. Owing to the higher channel bandwidth and the advancement of CMOS technology from deep-sub micron to nanometer, the operation frequency of CMOS goes higher than 100GHz. We can achieve the target of higher cutoff frequency in analog filter design.

1.2 Analog Filters

The actual trends of Integrated Circuits (IC) are both to scale down the dimensions of the transistors and to incorporate in a single chip as many building blocks as possible. In the design of the high-performance electronic circuits the use

of analog filters is unavoidable. The advance of the VLSI techniques demands for high-frequency and high-performance active filtering. In telecommunication applications, for instance, active filters ranging from a few kHz up to several MHz are required. In CMOS technologies, the analog filter design techniques can be divided in analog sampled-data and time continuous techniques.

Sampled-data filter techniques use several non-overlapping clock phase. The main characteristics of switched capacitor filters are determined by a clock frequency and by capacitor ratios. Hence, a major advantage of this technique is the high accuracy of its integrator time constant. These advantages of switched capacitor filters are not necessarily maintained for high frequency applications. This is mainly due to the finite parameters of the OPAMP, finite resistance of the switches and clock feed-through. In high-frequency applications the OPAMP has to be fast enough to settle to the right output within a half clock period. For a settling precision of 0.1%, the settling time should be higher than the GBW of the OPAMP at least by a factor 7. However, due to the additional capacitors connected to the OPAMP output the effective settling time increases and as a result even larger GBWs are required. Finally, it should be mentioned that sampled-data filters need an anti-aliasing continuous-time filter to band-limit the frequencies of the input signal.

For continuous-time filters, these filters were developed as complementary of switched-capacitor filters as anti-aliasing and smoothing filters. Nowadays, time continuous filters are an alternative to sampled-data filters in low-frequency applications. Moreover, they allow the integration of filters in the MHz and several hundreds of MHz frequency ranges. This technique avoids the need of pre- and post-filtering that in most of the cases switched-capacitor filters require. Because it is a time continuous technique, the aliasing problems are not present. The precision of these filters is the major disadvantage. For the design of high-performance CMOS

active filters, there are three main types of continuous-time filters, namely, RC active filters, MOSFET-C filters and OTA based filters. The MOSFET-C filters are basically the active RC filters but with the resistors implemented by equivalent CMOS tunable resistors. The limited frequency response of the two or more stages OPAMPs reduces the use of the filters to low-frequency applications. For Operational Transconductance Amplifier-Capacitor (OTA-C) filters, they have already been reported for frequency ranges from a few kHz up to very high frequency. A major drawback of the OTA-C filters is the lack of very linear and efficient voltage- to-current transducers. The relatively higher distortion of continuous-time filters reduces their range of applications. A major advantage of the OTA based continuous-time filters is their extremely large frequency response. A comparison of the useful frequency range for both OPAMP and OTA based circuits is shown in Fig. 1.1. Because the OTA based integrator is implemented in open loop, the useful frequency range of these circuits is limited only by the OTA gain-bandwidth product [2].

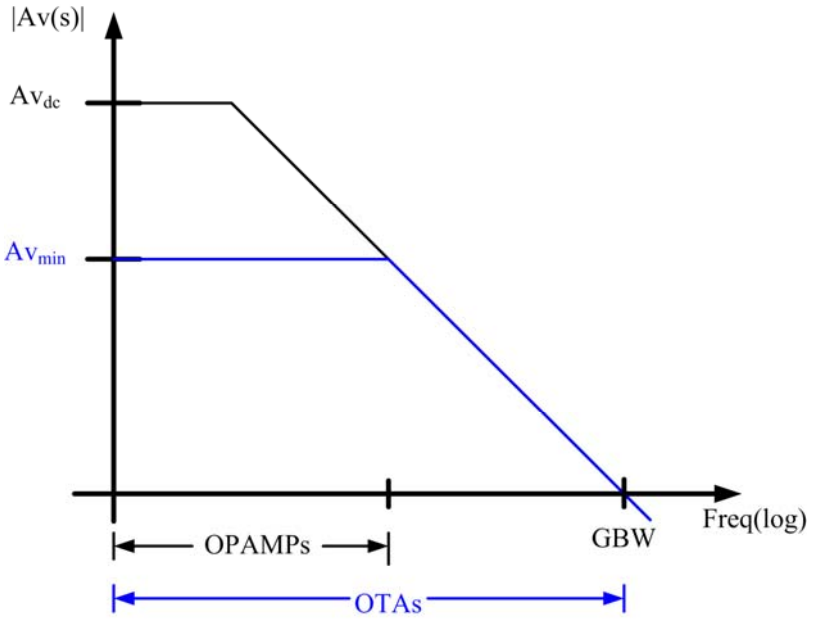


Fig. 1.1 Frequency responses for a typical single pole OPAMP/OTA

1.3 Thesis Overview

Chapter 2 will give some basic structures of OTAs operating at high frequency. It will describe the advantages and disadvantages of these structures as well as its characteristics. As well, some improving circuits will also be described in this chapter.

Chapter 3 will present the proposed OTAs, which modify the basic structures and could operate at high frequency. At first we will discuss the operation of the OTAs and give the math to prove the concept. Then, noise analysis of the OTAs will be presented.

In chapter 4, OTA-C filters will be presented in this chapter. The principle of the filters will be discussed in this chapter, and the output buffer will make a discussion, too.

In chapter 5, the experimental results and simulation results will be presented in the end of this chapter.

Finally, the conclusion to this work is given in chapter 6.

Chapter 2

Operational Transconductance Amplifiers

2.1 Introduction

In this chapter, we will introduce several basic OTAs. Because OTA-C filters can operate at higher frequency than sampled-data filters and RC active filters, the OTA-C filters become more popular in high frequency applications. However, OTAs are the basic blocks of the OTA-C filters, so the performance of the OTAs will determine the performance of the filters. The concept of OTA just linearly converts voltage to current. By considering the power and area issues, the active devices are used in the circuit rather than passive devices. Nevertheless, the linearity performance of active devices is poor than passive devices. Therefore, we must make a trade off between them. As well, comparing the switched capacitor filters and OTAs filters, although OTA-C filters could operate at more higher frequency than the switched capacitor filters, the former has a major disadvantage for poor linearity. Especially, when the size of CMOS technology scales down with power supply voltage, the dynamic range, bandwidth, and power consumption will be limited the linearity. For this reason, there are lots of circuits presented to improve the linearity.

2.2 Basic concepts of High-speed OTAs

Since the OTAs are operated at high frequency, there should not be unnecessary poles. Therefore, the circuits could not be complex. For this reason, we will discuss some basic OTAs, which the most circuits operated in high frequency are improved from these basic OTAs [3].

2.2.1 Differential input

In this subsection, it will describe the differential pair circuit, which is shown in Fig. 2.1.

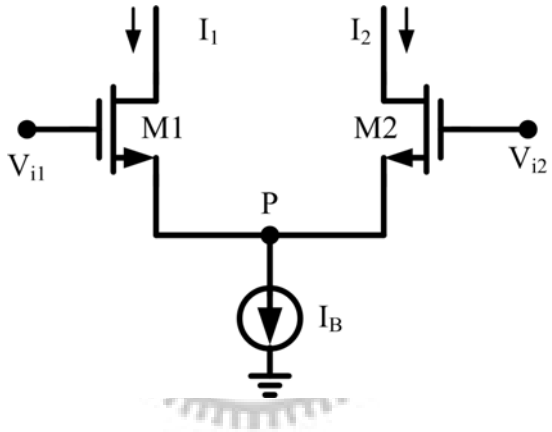


Fig. 2.1 the Differential Pair

For the region of M1 and M2 being saturation region, the output current I_1 and I_2 can be got as:

$$I_1 = \frac{1}{2}\beta_{1,2}(V_{i1} - V_p - V_{thn1,2})^2 \tag{2.1}$$

$$I_2 = \frac{1}{2}\beta_{1,2}(V_{i2} - V_p - V_{thn1,2})^2 \tag{2.2}$$

Therefore, the differential output current can be obtained by subtracting equation (2.1) from equation (2.2) as:

$$I_o = I_1 - I_2 = \beta_{1,2}(V_{i1} - V_{i2})(V_{cm} - V_p - V_{thn1,2}) \tag{2.3}$$

where the value V_{cm} is the input common mode voltage, and it is fixed to a constant DC level. As well, the V_p can be described as:

$$V_p = \sqrt{\frac{2I_B}{\beta_{I_B}}} \tag{2.4}$$

From equation (2.3), the transconductance is proportion to $\beta_{1,2}(V_{cm}-V_p-V_{thn1,2})$. Therefore, the transconductance of the differential pair is constant as long as the voltage V_p is constant. Furthermore, the value G_m could be tuned by the tail current due to the equation (2.4). For ideal tail current, the output resistance of the tail current is infinite, so the point P is virtual ground for small signal. Hence, the transconductance could keep constant ideally. As well, because this circuit has no internal nodes, it could be operate at very high frequency. However, the output resistance of the tail current is not infinite. For this reason, the voltage V_p is not constant, and it varies with input signal variation and technology process. So, technologies to keep V_p constant are presented to improve linearity.

2.2.2 Pseudo-Differential input

Finally, we will talk about the pseudo-differential pair, which just takes off the tail current from the differential pair. Because the point P of the differential pair in Fig. 2.1 is variation in practice, it is grounded to solve this problem. Hence, the linearity will be improved. Furthermore, since the tail current is taken off, it can increase the headroom in the pseudo-differential pair due to cancel the tail current in the differential pair. As well, pseudo-differential pair is suitable in lower power supply than the differential pair. The circuit for pseudo-differential is shown in Fig. 2.2.

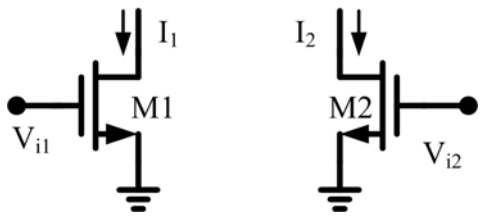


Fig. 2.2 the Pseudo-Differential Pair

Nowadays, we derive the formula to see the operation of the pseudo-differential pair. Since the regions of M1 and M2 are saturation regions, the output currents are described as below:

$$I_1 = \frac{1}{2}\beta_{1,2}(V_{i1} - V_{thn1,2})^2 \tag{2.5}$$

$$I_2 = \frac{1}{2}\beta_{1,2}(V_{i2} - V_{thn1,2})^2 \tag{2.6}$$

Therefore, the differential output current can be shown as:

$$I_o = I_1 - I_2 = \beta_{1,2}(V_{i1} - V_{i2})(V_{cm} - V_{thn1,2}) \tag{2.7}$$

From equation (2.7), the disadvantage of the differential pair is be solved, and the linearity will be improved. However, the pseudo-differential pair has its disadvantage comparing with the differential pair. First, the pseudo-differential pair has a problem about tuning. Unlike differential pair that can be tuned by tail current I_B, the transconductance is proportion to $\beta_{1,2}(V_{cm}-V_{thn1,2})$, which are usually fixed constant after taped out. Nevertheless, this is solved in [5] by tuning the threshold voltage, which can change by body voltage. Second, because the tail current is taken off, the common mode gain will increase. Therefore, the common mode reject ratio (CMRR) is about 0dB. Hence, this circuit needs common mode feedforward circuit to increase CMRR.

2.2.3 Source Degeneration

In the beginning, we introduce the source degeneration structure, which is the common structure in the transconductance circuit. The circuit is shown in Fig. 2.3.

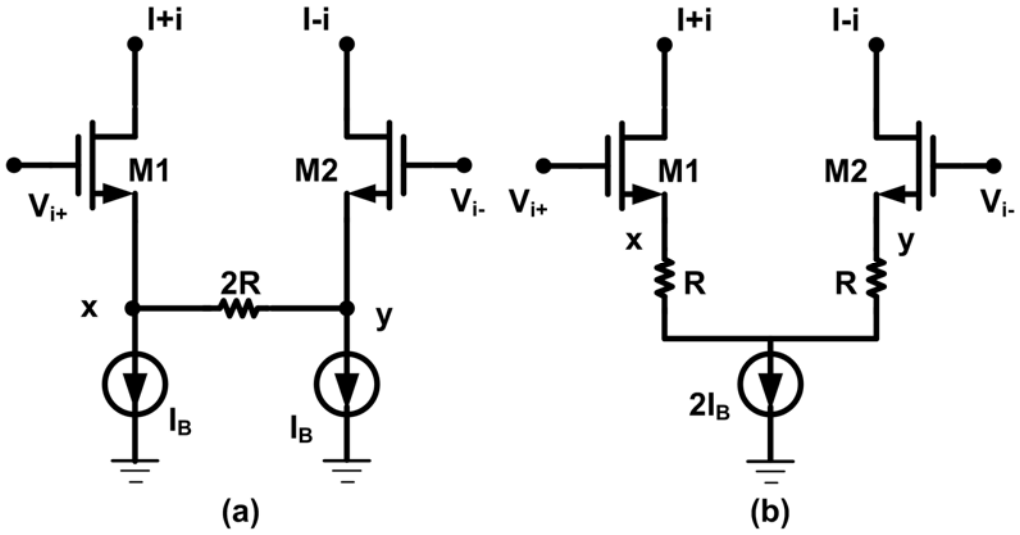


Fig. 2.3 Transconductance using Source Degeneration Pair

In this circuit, the ideal operation of source degeneration is that V_{i+} and V_{i-} perfectly follow to the ends of the resister. Then, the voltage across the ends of the resister, V_{i+} and V_{i-}, will generate the output current. Because the output current is generated by resister R, the linearity would be very great. However, the resisters between the gate and the source of the transistors M1, M2 are not zero, and they vary with the transconductance of M1, M2. Therefore, the input voltages would not perfectly follow to the ends of the resister R, and it would degrade the linearity. For this reason, lots of techniques are presented to solve this problem and increase THD.

As shown in [4], the output current to the input voltage can be got as:

$$i = \sqrt{1-(\frac{v_{id}}{2(1+N)V_{DS(sat)}})^2} \times (\frac{\sqrt{2\mu_n C_{ox} I_B \frac{W_n}{L_n}}}{1+N})v_{id} \tag{2.8}$$

$$G_m = \frac{1}{R}\frac{N}{1+N} \tag{2.9}$$

From equation (2.9), the transconductance is proportional to the factor 1/R, so increasing the linearity by the resistor is also decreasing the transconductance. Using the Taylor series, the third harmonic distortion (HD3) can be derived as:

$$HD3 = (\frac{1}{1+N})^2 \times \frac{1}{32} \times (\frac{v_{id}}{V_{DS(sat)}})^2 \quad (2.10)$$

where the degeneration factor N is $g_{m1,2} \times 2R$. From equation (2.10), the conclusion could be made as: increasing the degeneration factor N, which increases the value R or the transconductances of M1, M2 ($g_{m1,2}$), can improve the HD3; therefore, the linearity will be increased, as well.

Although the circuits in Fig. 2.3(a) and Fig. 2.3(b) shows the same voltage-to-current relationship, they present different properties. For Fig. 2.3(a), the tail currents will contribute differential noise in the output, which will dominate the noise performance. For Fig. 2.3(b), there are voltage drops in the resistors, which will reduce the range of the common mode voltage.

2.2.4 Constant Drain-Source Voltage

Second, MOSFETS with constant drain-source voltage structure will be discussed. The circuit is shown in Fig. 2.4.

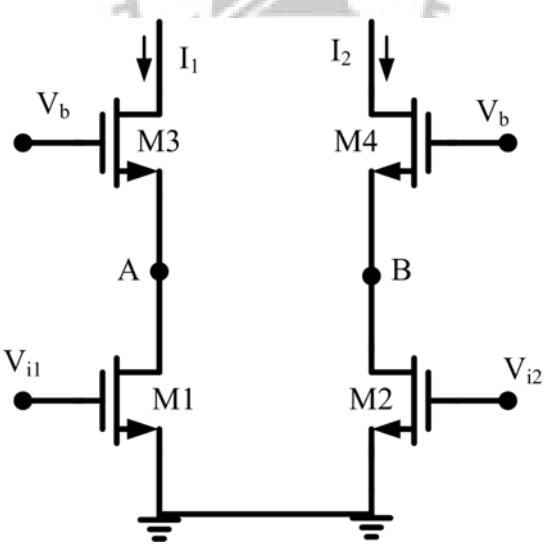


Fig. 2.4 MOSFETS with Constant Drain-Source Voltage

In the circuit, the transistors M1 and M2 are in linear region, and M3 and M4 are in saturation region. Therefore, the output current I_1 and I_2 are as:

$$I_1 = \beta_{1,2}[V_{ds1,2}(V_{i1} - V_{thn1,2}) - \frac{1}{2}V_{ds1,2}{}^2] \quad (2.11)$$

$$I_2 = \beta_{1,2}[V_{ds1,2}(V_{i2} - V_{thn1,2}) - \frac{1}{2}V_{ds1,2}{}^2] \quad (2.12)$$

Then the differential output current is:

$$I_o = I_1 - I_2 = \beta V_{ds1,2}(V_{i1} - V_{i2}) \quad (2.13)$$

From equation (2.13), the transconductance is proportion to $\beta V_{ds1,2}$. In practice, second-order effects like mobility reduction and velocity saturation reduce the linearity somewhat. However, the linearity performance is dominated by the variation of $V_{ds1,2}$. Therefore, some techniques are presented to fix the points A and B to make the voltage $V_{ds1,2}$ constant.

2.3 Linearity-improved OTAs

As above, the four basic OTA circuits are introduced, and the major disadvantages of these circuits are the poor linearity. So lots of linearity enhancement techniques are presented to improve these problems. In this subsection, we will discuss two linearity enhancement techniques, which are already presented to improve the linearity.

2.3.1 Modified Source Degeneration OTA Circuits

As discussion in subsection 2.2.1, the linearity will degrade since the input voltages do not perfectly follow to the ends of the resistor. Hence, the direct idea is that using op amps to make the input voltages follow to the ends of the resistor. This idea is shown in Fig. 2.5. The source voltages of M1 and M2 will be equal to the input voltages due to the virtual ground in each op amp. Hence the op amps would make the input voltages follow to the ends of the resistor more greatly than the original source degeneration.

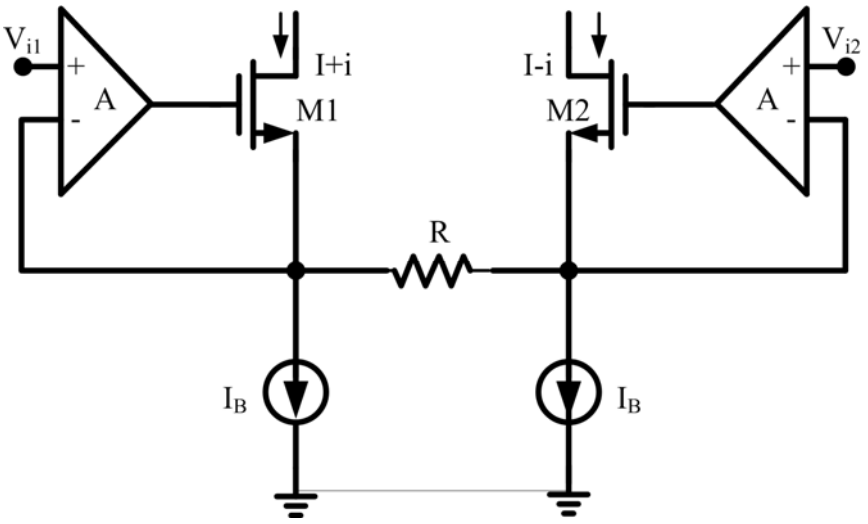


Fig. 2.5 Improving the linearity of a fixed transconductor through the use of op amps

Another method for improving the linearity of a fixed transconductor is to force constant currents through M1 and M2 such that their V_{gs} are fixed which is shown in Fig. 2.6. This modified source degeneration is added the negative voltage feedback, which will make the gate-source voltages of M1 and M2 constant. Therefore, it reduces the variation of the voltage across the resistor due to the constant gate-source voltages of M1 and M2.

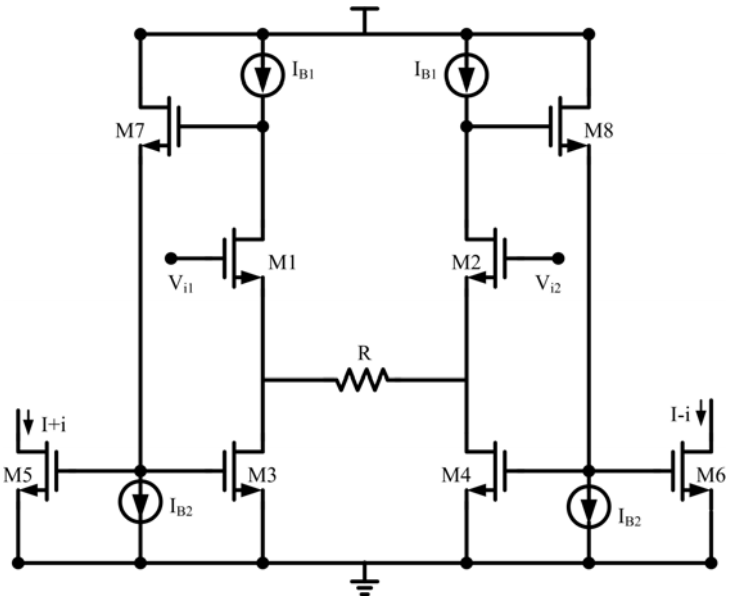


Fig. 2.6 Improving the linearity of a fixed transconductor by maintaining a constant V_{gs} for M1 and M2

The circuits above which use negative voltage feedback to improve the linearity are not suitable for using as high speed OTA. Since the negative current feedback has larger bandwidth than the negative voltage feedback, the circuit using the negative current feedback will be introduced in next chapter.

2.3.2 Modified OTA Circuits with Constant Drain-Source Voltage

In subsection 2.2.2, MOSFETS with constant drain-source voltage are discussed, and the factor for the poor linearity is also discussed. The main factor is the variation of the drain-source voltages of M1 and M2 due to the input pair voltages and the temperature variation. Therefore, it needs a circuit to fix the voltages constant, and the op amps are used for this purpose. The circuit is shown in Fig. 2.7. Due to the virtual ground of the input pairs, the drain-source voltages of M1 and M2 will be fixed to the voltages of the positive input voltages in op amps. Hence, the positive input voltages in op amps could also use to tune the transconductance, which could be seen as below:

$$I_o = I_1 - I_2 = \beta V_{tune}(V_{i1} - V_{i2}) \tag{2.14}$$

Thus, using op amps could fix the voltage which is the main factor for the linearity reduction. The op amps should be designed for simpler circuits to reduce the complexity and noise which the fewer devices using the less noise will be contributed.

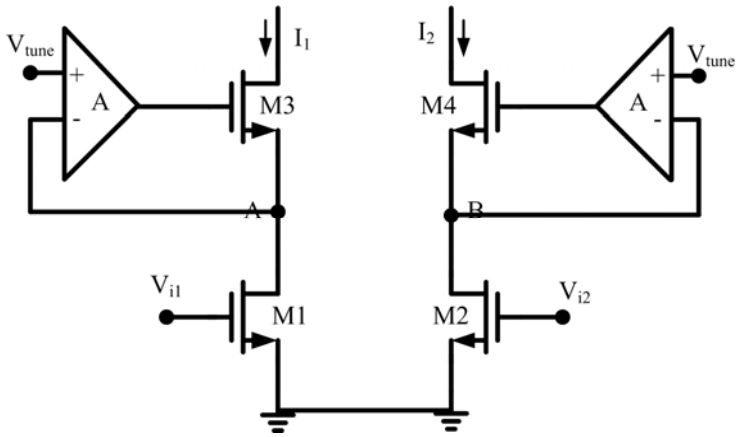


Fig. 2.7 Modified Circuits of MOSFETS with Constant Drain-Source Voltage

Chapter 3

Proposed OTAs for High Speed Applications

3.1 Introduction

As discussion in chapter 2, the main disadvantage of the OTAs is the poor linearity. Therefore, lots of linearity enhancement techniques are presented to improve the shortcoming. In the latter of chapter 2, two techniques of them are introduced. However, these two methods are not suitable to high speed applications, since the negative voltage feedback has lower bandwidth, which will reduce the loop gain at the frequency we wish to operate. Hence, the two modified circuits are proposed to apply in the high speed applications in this chapter.

3.2 Proposed Source Degeneration OTA with Negative Current Feedback

In this section, the linearity enhancement techniques are proposed by using negative current feedback, which is more suitable in high speed applications. Since the resistance in the current feedback is smaller than that in the voltage feedback. Therefore, the current feedback circuit features a very high bandwidth for higher

pole location [7]. This means that the linearity voltage feedback circuit improved will be less because the loop gain in the high frequency will be not sufficient due to the lower bandwidth. For this reason, the modified circuit using negative current feedback is proposed to put in use in the high speed applications.

3.2.1 Characteristics and Operation of the OTA Circuit

The modified circuit using negative current feedback is shown in Fig. 3.1.

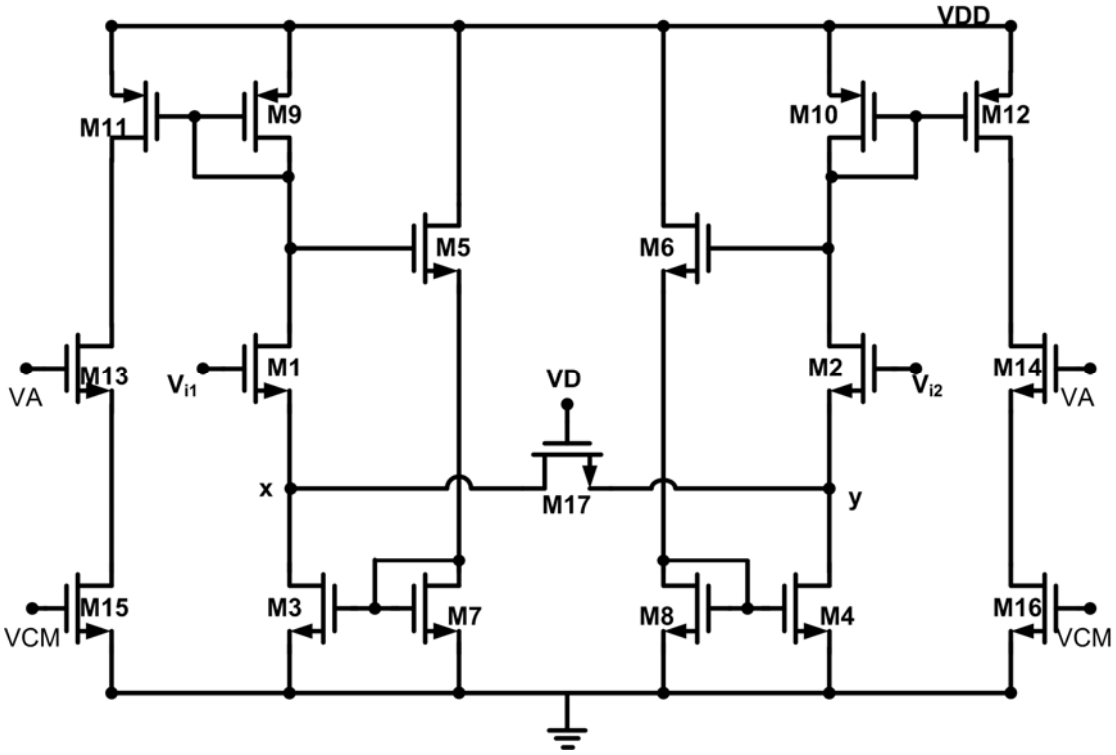


Fig. 3.1 Modified Source Degeneration Circuit using negative current feedback

The transistors M9~M16 are the output stage. The modified structure uses M17 operating in the linear region to replace the resister 2R in the conventional source degeneration circuit. That is because this circuit could utilize the gate voltage (VD) as tuning circuit. Therefore, it can be used to overcome the variation due to the fabrication or temperature variations. The operation of transistors M1~M4 and M17 is the same as the description in subsection 2.2.1. However, the transistors M5~M8 are added to increase the THD. These transistors are composed of the negative current feedback circuit, and it provides a negative feedback gain to degenerate the

HD3. Consequently, it could achieve the requirement of HD3 without large value of R.

At first, the operation of the negative current feedback circuit is presented. Assume input voltage V_{i1} increases, but the voltage at the point x (V_x) does not follow this variation. This will make the voltage between the gate and the source of M1 increase. Therefore, the drain current of M1 increases, and the drain current of M9 increases, too. Because the drain current of M9 increases, the voltage across the drain and the source of M9 also increases. For this reason, the gate voltage of M5 ($V_{g5}=V_{DD}-V_{ds9}$) decreases. Then, the V_{gs} of M5 decreases, and the drain current of M5 also decreases. The decreasing current will flow to the main circuit through the current mirror pair M3 and M7. Therefore, the drain current of M1 will be pulled down, and the voltage V_x will be pushed up. Therefore, the negative current feedback circuit could give the voltage V_x a hand to follow the variation of the input voltage. Similar, the voltage V_y will also follow with the input voltage V_{i2} by the same operation.

By the way, the math formulas for HD3 will be derived to prove the concept of the circuit. First, assuming $V_{i1}= v_{id} + v_{cm}$, $V_{i2}= v_{id} - v_{cm}$, and the voltages at the point x, y are V_x, V_y. Therefore, the drain currents of M1 and M2 are as below:

$$I_{D1} = g_{m1,2}(V_{i1} - V_x) \tag{3.1}$$

$$I_{D2} = g_{m1,2}(V_{i2} - V_y) \tag{3.2}$$

As well, the current across the transistor M17 (r_{ds17}) can be got as:

$$I_{xy} = \frac{V_x - V_y}{r_{ds17}} \tag{3.3}$$

Hence, the drain currents of M1 and M2 can also be described as:

$$I_{D1} = I_{D3} + I_{xy} \tag{3.4}$$

$$I_{D2} = I_{D4} - I_{xy} \tag{3.5}$$

where $I_{D1}+I_{D2}=I_{D3}+I_{D4}=2I_B$, which I_B is the bias current. From equation (3.1), (3.2), (3.4), and (3.5), the differential output current is as below:

$$I_o = I_{D1} - I_{D2} = g_{m1,2}(v_{id} - (V_x - V_y)) = 2I_{xy} + I_{D3} - I_{D4} \tag{3.6}$$

Now, we assume R_o is the resistance looking down the drain of M1, and also assume R_o is constant for simplicity. Thus, the drain currents of M3 and M4 could be determined by the drain currents of M5 and M6 due to the current mirror pairs. So the currents are shown below:

$$I_{D3} = \beta_{5,6}(I_{D1}R_o - V_{gs5,6} - V_{thn5,6})^2 \tag{3.7}$$

$$I_{D4} = \beta_{5,6}(I_{D2}R_o - V_{gs5,6} - V_{thn5,6})^2 \tag{3.8}$$

Using equation (3.7), (3.3), (3.8), and (3.6), the relation between the differential output current and the voltage across M17 is shown in the following:

$$I_{D1} - I_{D2} = 2\frac{V_x - V_y}{r_{ds17}} + (I_{D1} - I_{D2})\alpha \tag{3.9}$$

where we assume the negative current feedback gain is $\alpha = \beta_{5,6}\text{Ro} \times(2V_{gs5,6} + 2V_{thn5,6}-2I_BR_o)$. The value $\beta_{5,6}$ is proportion to 1/RV, so the unit of negative current feedback gain α is V/V. Furthermore, from equation (3.9) and (3.6), the equation about the voltage across M17 can be described as:

$$V_x - V_y = \frac{(1+\alpha)Nv_{id}}{(1+\alpha)N+1} \tag{3.10}$$

where $N=g_{m1,2}\times r_{ds17}$ is the source degeneration factor [4]. Finally, for the drain formulas of M1, M2, and the equation (3.10), we can get the relation about differential output current and the input voltage.

$$I_{D1} = \beta_{1,2}(V_{i1} - V_x - V_{thn1,2})^2 \tag{3.11}$$

$$I_{D2} = \beta_{1,2}(V_{i2} - V_y - V_{thn1,2})^2 \tag{3.12}$$

$$I_o = I_{D1} - I_{D2} = \sqrt{1-(\frac{v_{id}}{2(1+(1+\alpha)N)V_{DS(SAT)}})^2} \times (\frac{\sqrt{4\beta_n I_B}}{1+(1+\alpha)N})v_{id} \quad (3.13)$$

$$G_m = \frac{1}{r_{ds17}} \frac{N}{1+(1+\alpha)N} \quad (3.14)$$

From equation (3.14), the transconductance is approximately proportional to the factor 1/ (1+α), which we can achieve the requirement of linearity with reduction of transconductance with about factor (1+α) rather than the factor r_{ds17} for the traditional source degeneration circuit. Hence, improving the linearity by negative feedback gain would reduce the smaller value of transcoductance than the traditional circuit. Using the Taylor series, the third harmonic distortion (HD3) could be got as:

$$HD3 = (\frac{1}{1+(1+\alpha)N})^2 \times \frac{1}{32} \times (\frac{v_{id}}{V_{DS(SAT)}})^2 \quad (3.15)$$

As compared with equation (2.2), the factor N in equation (2.2) change to (1+α)N in equation (3.15). Therefore, it can also improve the HD3 by the negative current feedback gain, α . Thus, the linearity could be achieved without large value r_{ds17}, and this relaxes the degeneration factor N and reduces the area due to the smaller resistance r_{ds17}.

3.2.2 Common Mode Feedback Circuit

In the filter designs, the output of the OTA must connect to the input of the next OTA, so the common mode voltage is very important. Now, two circuits will be shown to understand the need of the common mode feedback circuit [8]. First, a simple differential amplifier which the inputs and outputs are shorted is shown in Fig. 3.2. We can find the common mode voltages of inputs and outputs are well defined as V_{DD}-$I_{SS}R_D$/2.

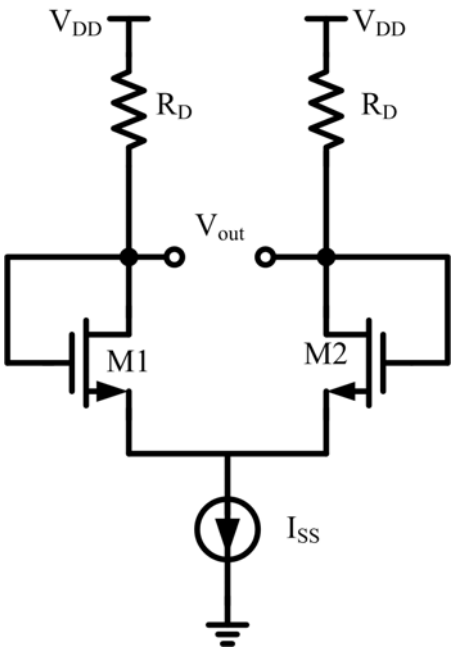


Fig. 3.2 a simple differential amplifier with inputs shorted to outputs

However, another circuit is shown in Fig. 3.3. Due to the fabrication process, the mismatches in the current mirrors will cause finite difference between $I_{D3,4}$ and $I_{SS}/2$. If $I_{D3,4}$ is slightly greater than $I_{SS}/2$, M3 and M4 will enter the linear region to make their drain currents equal to $I_{SS}/2$. Conversely, if $I_{SS}/2$ is slightly greater than $I_{D3,4}$, M5 will enter the linear region to make $I_{SS}/2$ equal to $I_{D3,4}$. Hence, due to the non-well defined common mode output voltages, it would make the transistors enter the wrong regions and would reduce the bias current, as well. Therefore, it needs a common mode feedback circuit for the differential circuits to fix the common mode output voltages at the wished level.

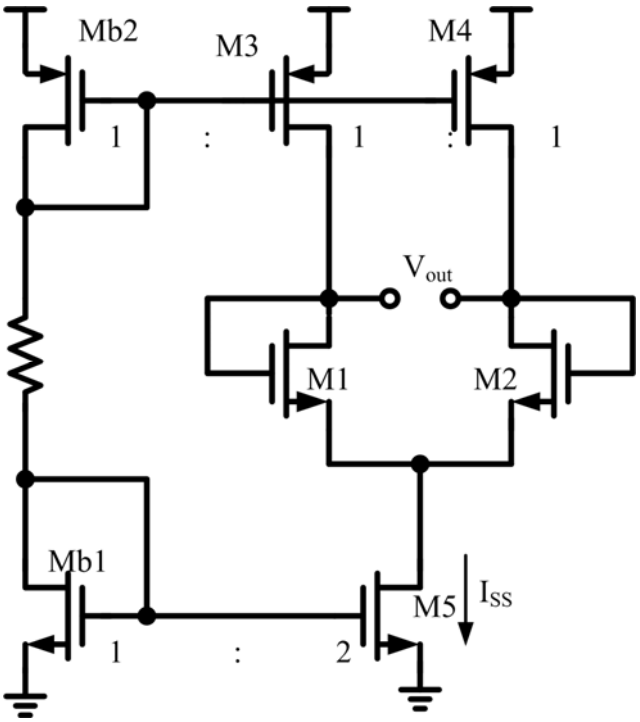


Fig. 3.3 High-gain differential pair with inputs shorted to outputs

Therefore, the common mode feedback circuit is needed to stabilize the output common mode level, which is shown in Fig. 3.4. Note that the output common mode level is fixed to the input common mode level. It is because the outputs of the OTA connect to the inputs of the next OTA by designing a filter. The following will describe the operation of the common mode feedback circuit [9].

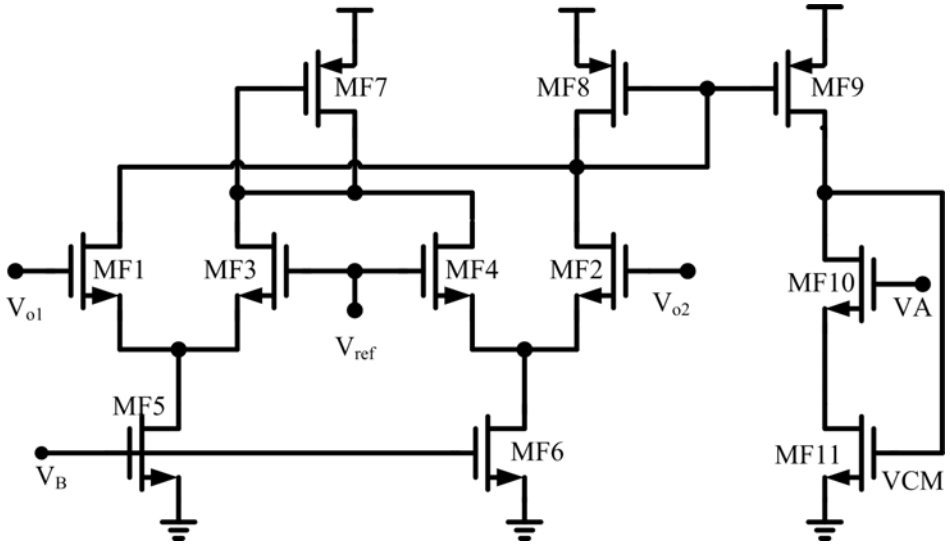


Fig. 3.4 The common mode feedback circuit for modified source degeneration using negative current feedback

MF10 and MF11 connect to the output stage M13, M14, M15, and M16 in Fig. 3.1 and it will adjust the output common mode level due to the feedback current. For example, if the output common mode voltages are larger than the reference voltage V_{ref}, the drain current of MF8 will increase. Hence, the currents in the output stage in Fig. 3.1 will increase, as well. Because the voltage across M11 and M12 increase due to the increased currents, the output common mode voltages decrease. Conversely, if the output common mode voltages are smaller than the reference voltage V_{ref}, the smaller current will flow to the output stage to increase the output common mode voltage. In addition, the operation of the common mode feedback circuit can be interpreted by the voltage concept. There is a negative gain from the gates of MF1, MF2 to the drains of them, and the gain from the gate of MF9 to the outputs in Fig. 3.1 is a positive gain. Therefore, the common mode feedback circuit provides a negative gain for the outputs, so it can fix the output common mode voltages to the reference voltage V_{ref}. When the circuit operates at high frequency, the common mode feedback circuit must also be stable at high frequency. The open loop gain of the common mode feedback circuit is:

$$\begin{aligned} A_{\mathrm{CMFB}}(s) &\cong g_{\mathrm{CMFB}}(s) \times R_{out} \\ &= \frac{g_{mf1,mf2} \times R_{out}}{\left(1 + s\frac{C_A}{g_{mf8}}\right)\left(1 + s\frac{C_B}{g_{mf11}}\right)\left(1 + sC_L \times R_{out}\right)} \end{aligned} \tag{3.16}$$

where C_A and C_B are the total capacitance in the points A and B. From equation (3.16), the pole at $1/ (C_L \times R_{out})$ is the dominated pole, and the poles at g_{mf8}/C_A, g_{mf11}/C_B are the non-dominated poles. They must be pushed far away the unity gain frequency to increase the phase margin.

3.2.3 Noise Analysis

For thermal noise:

For the communication systems, the noise is the major course to avoid that the signal could be received correctly. However, there are noises in the devices such as flicker noise and the thermal noise. If the frequency is less than the corner frequency, the dominated noise is the flicker noise; otherwise, the dominated noise is the thermal noise. Since the cutoff frequency for the implement filter is at high frequency, the dominated noise is the thermal noise. The channel noise can be modeled by a current source connected between the drain and the source with a special density as:

$$\overline{I_n^{\,2}} = 4kT(\frac{2}{3})g_m \tag{3.17}$$

where k is the Botzmann constant, T is the absolute temperature, g_m is the source conductance. Using the thermal noise model, the total output-referred noise spectral density of the modified source degeneration circuit using negative current feedback is derived as:

$$\begin{aligned}\overline{I_{out,n}^{\,2}} = {} & 4[4kT(\frac{2}{3})g_{m9}] + 2[4kT(\frac{2}{3})\frac{1}{g_{m1}}](\frac{g_{m1}}{1+(1+\alpha)g_{m1}r_{ds17}})^2 \\ & + \{2[4kT(\frac{2}{3})g_{m17}] + 4[4kT(\frac{2}{3})g_{m3}]\}(\frac{g_{m1}r_{ds17}}{1+(1+\alpha)g_{m1}r_{ds17}})^2 \\ & + 2[4kT(\frac{2}{3})g_{m5}](\frac{g_{m1}r_{ds17}}{1+(1+\alpha)g_{m1}r_{ds17}})^2\end{aligned} \tag{3.18}$$

where α is the negative current feedback gain. The input-referred noise spectral noise density could be calculated as:

$$\overline{V_{in,n}^{\,2}} = \frac{\overline{I_{out,n}^{\,2}}}{(\frac{g_{m1}}{1+(1+\alpha)g_{m1}r_{ds17}})^2} \tag{3.19}$$

From equation (3.18), the added current feedback circuit provides additional noise in the output, but increasing the current feedback gain could reduce the noise. As well, the large aspect ratios of the input transistors and small aspect ratios of the load transistors should be designed for small output noise. However, the input-referred

noise is larger than the traditional circuit due to the added current feedback circuit.

3.3 Proposed OTA Circuit with Constant Drain-Source Voltage

As mentioned in the chapter 2, MOSFET with constant drain-source voltage would degrade the linearity due to the variation of the drain-source voltage in the input pairs, and the enhancement technique using op amps to fix the drain-source voltages is presented. Therefore, the op amps should be designed as simple as possible to reduce the complexity.

3.3.1 Characteristics and Operation of the OTA Circuit

In [10], an approach uses feedforward method instead of the op amps to fix the drain-source voltage of the input pairs. However, the circuit used in [10] stacks five transistors and could not work at lower power supply, which operated at +-1.4V. As the transistors sizes are smaller, the power supply voltage will be lower. Therefore, the circuit in [10] will be not suitable for lower power supply. For this reason, the modified circuit will be proposed in this section. The whole circuit is shown in Fig. 3.5.

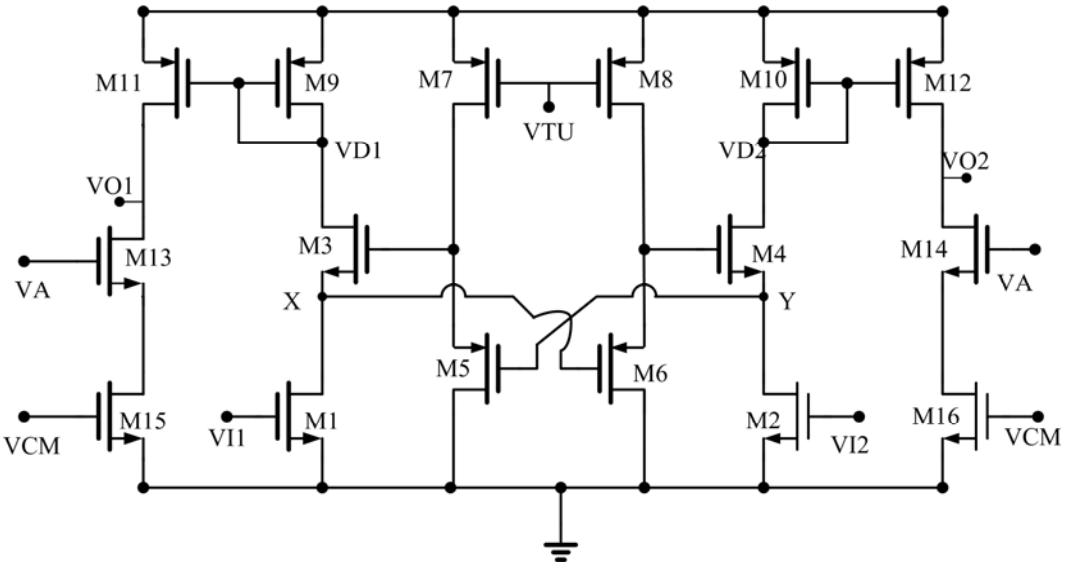


Fig. 3.5 The modified circuit of MOSFET with constant drain-source voltage by using feedforward structure

The transistors M9~M16 are the output stage. The transistors M1~M4 are the same transistors as shown in Fig. 2.7, and the regions and characteristics are the same as before. However, the transistors M5~M8 are used to replace the op amps. The circuits can not only tune the linearity but also the unity gain frequency. Furthermore, the OTA could operate at the lower power supply than the circuit in [10].

At first, the operation of the feedforward circuit is presented. Assume there are large differential signals in the input pairs, which is the voltage in VI1 is increased, and the voltage in VI2 is deceased. If the voltages between the gate and source of M3 and M4 do not follow the variations in the input pairs, the drain voltage of M1 will decrease, and the drain voltage of M2 will increase to make $I_{d1}=I_{d3}$ and $I_{d2}=I_{d4}$. However, the variations in the drains of the input pairs will degrade the linearity, and the feedforward-regulated circuit is used to overcome the problem of the variations. When the source voltage of MOS M3 decreases, the gate voltage of MOS M4 decreases, which is due to the source follower circuit, M6 and M8. Since the gate voltage of M4 decreases, it would make the drain voltage of M2 decreases, too. Therefore, the drain voltage of M2 could be fixed to a constant value by the feedforward-regulated circuit. The drain voltage of M1 will also be fixed to a constant value by the similar operation.

By the way, the math formulas for the output current to the input voltage will be derived to prove the concept of the circuit. First, we make the following assumption VI1 = $V_{CM} + v_{id}$, VI2 = $V_{CM} - v_{id}$, $V_x = V_{DS} + \Delta V_D$, and $V_y = V_{DS} - \Delta V_D$. In Fig. 2.2, if the drain-source voltages of input pairs are constant, the relation between output current and input voltage is:

$$I_{D1} - I_{D2} = 2\beta_{1,2} V_{DS} (VI1 - VI2) = 2\beta_{1,2} V_{DS} (2v_{id}) \qquad (3.20)$$

The transconductance is proportion to $\beta_{1,2}V_{DS}$, and could be very linear. However, since the drain-source voltages of input pairs vary with the temperature, fabrication processing and the input signal, the relation between output current and input voltage will become as:

$$I_{D1} - I_{D2} = 2\beta_{1,2}[V_{DS}(VI1 - VI2) + \Delta V_D(V_{CM} - 2V_{thn1,2}) - 2\Delta V_D V_{DS}]$$

$$= 2\beta_{1,2}[V_{DS}(2v_{id}) + \Delta V_D(V_{CM} - 2V_{thn1,2}) - 2\Delta V_D V_{DS}] \quad (3.21)$$

Due to the variation of the drain-source voltage ΔV_D, the linearity degrades. Therefore, the proposed circuit will reduce the variation, which could find out as follow. By the regions in the transistors M1~M4, the current formulas can be got as:

$$I_{D1} = 2\beta_{1,2}[V_x(VI1 - V_{thn1,2}) - \frac{1}{2}V_x^2]$$

$$= \beta_{3,4}(V_y + V_{gs7,8} - V_x - V_{thn3,4})^2 \quad (3.22)$$

$$I_{D2} = 2\beta_{1,2}[V_y(VI2 - V_{thn1,2}) - \frac{1}{2}V_y^2]$$

$$= \beta_{3,4}(V_x + V_{gs7,8} - V_y - V_{thn3,4})^2 \quad (3.23)$$

From the source follower circuits, based on $I_{D5} = I_{D7}$ and $I_{D6} = I_{D8}$, the voltage $V_{gs7,8}$ could be got as:

$$V_{gs7,8} = \sqrt{\frac{\beta_{5,6}}{\beta_{7,8}}}(V_{DD} - VTU - |V_{thp5,6}|) + |V_{thp7,8}| \quad (3.24)$$

From equation (3.20) as well as (3.21), the differential output current and the variation of the drain-source voltage of the input pairs are as below:

$$V_x - V_y = 2\Delta V_D = \frac{I_{D1} - I_{D2}}{\beta_{3,4}(V_{thn3,4} - V_{gs7,8})}$$

$$= \frac{2\beta_{1,2}V_{DS}v_{id}}{\beta_{1,2}(V_{thn1,2} + \frac{1}{2}V_{DS} - V_{CM}) - \beta_{3,4}(V_{gs7,8} - V_{thn3,4})} \quad (3.25)$$

$$I_o = I_{D1} - I_{D2} = \frac{2V_{DS}v_{id}}{\frac{1}{\beta_{1,2}} + \frac{V_{CM} - V_{thn1,2} - \frac{V_{DS}}{2}}{\beta_{3,4}(V_{gs7,8} - V_{thn3,4})}} \quad (3.26)$$

Based on equation (3.25) and (3.26), the variations on the drain-source voltages on input pair could be tuning by varying the drain-source voltage V_x, V_y of the input pair, which can be also varied by the voltage VTU. As well, reducing the variation in the drains of the input pairs will decrease the transconductance, which means it is tradeoff for the linearity and transconductance. However, increasing $V_{gs7,8}$ will also increase noise as described after.

3.3.2 Common Mode Feedback and Feedforward Circuits

For fully differential circuit, the common mode gain can be reduced by increasing the output resistance of the tail current [11]. However, there is a voltage drop in the tail current, and that would reduce the headroom of the input voltage. So pseudo-differential circuits are used to increase the headroom, which take off the tail current from the fully differential circuit. However, the pseudo-differential circuits have a shortcoming comparing with the fully differential circuits for their common mode rejection ratio (CMRR). Since the half circuits of the pseudo-differential circuits for common mode and differential mode are the same, the common mode gain and the differential gain are almost the same, i.e., CMRR=A_{DM}/A_{CM}=1. This large A_{CM}, in the pseudo-differential circuits, would lead to huge common mode variations at the OTA outputs. Hence, a common mode feedforward circuit is needed for pseudo-differential circuit to reduce the common mode gain. The concept of the common mode feedforward circuit can be shown in Fig. 3.6. It is obviously that the common mode feedforward circuit will generate the common mode current. This current will flow to the output stage and cancel the common mode of the output current. Therefore, the common mode of the output current is reduced, but the

differential mode does not influence, which the CMRR increases.

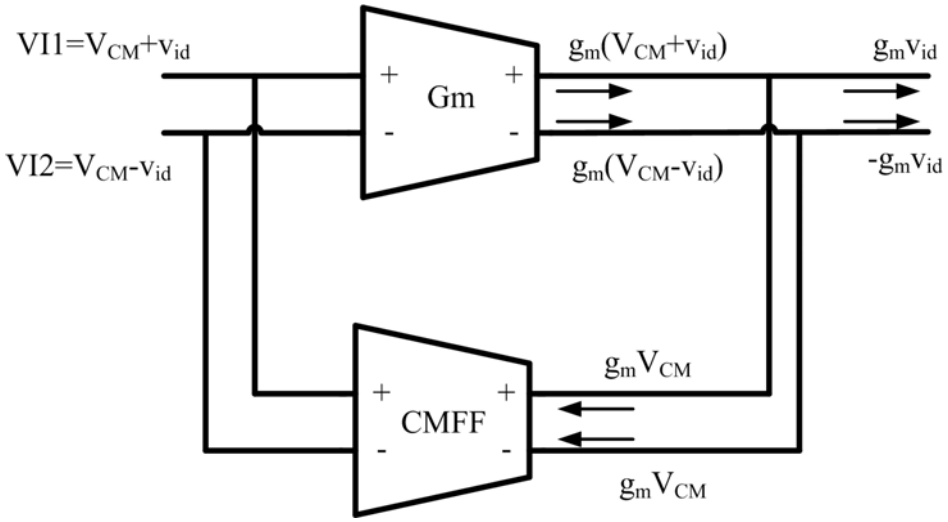


Fig. 3.6 The concept of the common mode feedforward circuit

As well, the common mode feedback circuit is needed to fix the output common mode voltage to the reference voltage V_{ref}. The common mode feedback and feedforward circuit is shown in Fig. 3.7 [12]. Now, we first discuss the common mode feedback circuit. The transistors MF1 and MF2 will detect the output common mode current, and this current will compare the reference current due to the current mirror pair. If the output common current is larger than the reference current which means that the common mode voltage is greater than the reference voltage, the feedback current I_{CMFB} will increase to make the output common mode voltage decreasing. Conversely, the feedback current will decrease to fix the common mode voltage to the reference voltage V_{ref}.

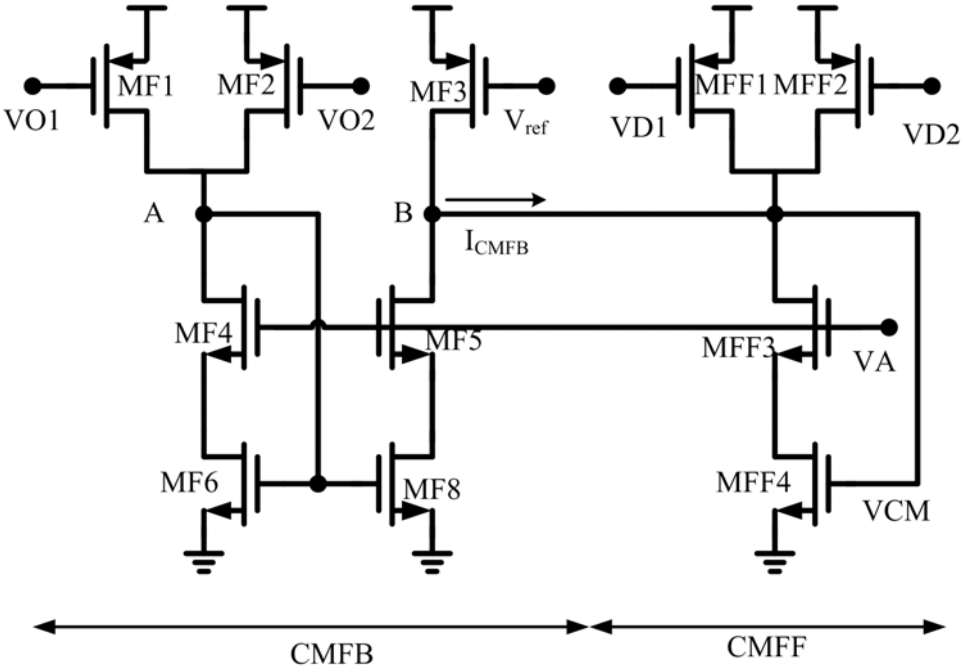


Fig. 3.7 The common mode feedback and feedforward circuit for modified circuit of MOSFET with constant drain-source voltage

Next, we will see the operation of common mode feedforward circuit. The transistors MFF1, MFF2 in Fig. 3.7 and M9, M10 in Fig. 3.5 are current mirrors, so the input common mode current will be detected by the circuit. This current will flow to the output stage to cancel the common mode current as discussion before.

Finally, the common mode control circuit must be also stable at high frequency, which needs enough phase margin at high frequency. The open loop gain for the common mode feedback circuit is:

$$\begin{aligned} A_{\mathrm{CMFB}}(s) &\cong g_{\mathrm{CMFB}}(s) \times R_{out} \\ &= \frac{g_{mf1,mf2} \times R_{out}}{\left(1+s\frac{C_A}{g_{mf6}}\right)\left(1+s\frac{2C_B}{g_{mff4}}\right)\left(1+sC_L \times R_{out}\right)} \end{aligned} \tag{3.27}$$

where C_A and C_B are the total capacitance in the points A and B. From equation (3.27), the pole at $1/(C_L \times R_{out})$ is the dominated pole, and the poles at g_{mf6}/C_A, $g_{mff4}/2C_B$ are the non-dominated poles. They must be pushed far away the unity gain frequency to increase the phase margin.

3.3.3 Noise Analysis

Thermal noise:

As discussion in subsection 3.2.3, the dominated noise is the thermal noise in high frequency. Hence, the output-referred noise spectral density of the constant drain-source voltage using feedforward circuit is as:

$$\overline{I_{out,n}^{\ 2}} = 2[4kT(\frac{2}{3})]\frac{1}{g_{m1}}\left(\frac{2V_{DS}\beta_{1,2}}{1+\frac{\beta_{1,2}(V_{CM}-V_{thn1,2}-\frac{V_{DS}}{2})}{\beta_{3,4}(V_{gs7,8}-V_{thn3,4})}}\right)^2$$
$$+\left[\frac{2[4kT(\frac{2}{3})]g_{m7}}{(g_{ds7}+g_{ds5})^2}+\frac{2[4kT(\frac{2}{3})]g_{m5}}{(g_{ds7}+g_{ds5})^2}+2[4kT(\frac{2}{3})]\frac{1}{g_{m3}}\right]\times\beta_{3,4}^{\ 2}(V_{gs7,8}-V_{thn3,4})^2 \quad (3.28)$$
$$+4[4kT(\frac{2}{3})]g_{m9}$$

where the parameters in (3.28) are the same as subsection 3.2.1. Also, the input-referred noise spectral density could be calculated as:

$$\overline{V_{in,n}^{\ 2}} = \frac{\overline{I_{out,n}^{\ 2}}}{\left(\frac{2V_{DS}\beta_{1,2}}{1+\frac{\beta_{1,2}(V_{CM}-V_{thn1,2}-\frac{V_{DS}}{2})}{\beta_{3,4}(V_{gs7,8}-V_{thn3,4})}}\right)^2} \quad (3.29)$$

For the constant drain-source voltage without feedforward circuit, the thermal noise due to the MOS M3 and M4 is as:

$$2[4kT(\frac{2}{3})]\frac{1}{g_{m3}}\times(\frac{g_{m3}}{1+g_{m3}r_{ds1}})^2 \quad (3.30)$$

However, from the second term in (3.28), the noise due to M3 and M4 is $I_n^{\ 2}*\beta_{3,4}^{\ 2}(V_{gs7,8}-V_{thn3,4})^2=I_n^{\ 2}*g_{m3}^{\ 2}$ for $V_{g3}=V_{g4}$. This is because the drain voltages of M1 and M2 are fixed by the feedforward circuit. Therefore, the points are grounded for

small signal, so the resistance r_{ds1} does not influence the noise due to M3 and M4. As well, the large aspect ratios of the input transistors and small aspect ratios of the load transistors should be designed for small output noise. When the voltage $V_{gs7,8}$ increases to reduce the variation ΔV_{DS} in (3.25) and increase the transconductance in (3.26), the output-referred noise also increases as shown in (3.28). However, the input-referred noise is larger than the traditional circuit due to the added current feedforward circuit.

Chapter 4

Transconductance-C Filters

4.1 Introduction

In recent years, there are lots of filter synthesis techniques presented. In these techniques, not all of them are suitable for the design of high speed filters. As described in chapter 1, the sampled-data analog filters, RC active filters and MOSFET-C filters are not suitable for high speed filter designs. However, the transconductance-C filters could be operated at high frequency. Hence, the transconductance-C filters will be introduced in this chapter [13].

For the transconductance-C filter designs, the basic building elements are transconductors and capacitors. In filters structure, the capacitor could be grounded or floating. In section 4.2, the ransconductance-C integrators will be described, and it will also discuss the non-ideal effects for the first order filters. In section 4.3, the 4^{th} order biquad filter will be introduced, which is the filters we used. The blocks which using transconductors as resistors will discuss in this section, and next the biquad section and 4^{th} order filter cascading two biquad section will also be discussion. Finally, the output buffers will be described, which avoid the influence of the output devices.

4.2 Transconductance-C Integrators

In this section, the fundamental transconductance-C filter is discussed. First, the ideal integrator model for transconductance-C filter is described. For ideal transconductors, they have infinite output resistance, infinite bandwidth etc. However, the transconductors are not ideal in the real world. Hence, the non-ideal effects of the transconductors will be described in subsection 4.2.2.

4.2.1 Integrator Model

Fully differential transconductance-C integrators are shown in Fig. 4.1. For fully differential structures, the even order harmonic distortions could be canceled for ideal condition. Therefore, most of integrators are implemented by fully differential structures. However, the single-ended integrators are discussed in this subsection for simplicity as shown in Fig. 4.2.

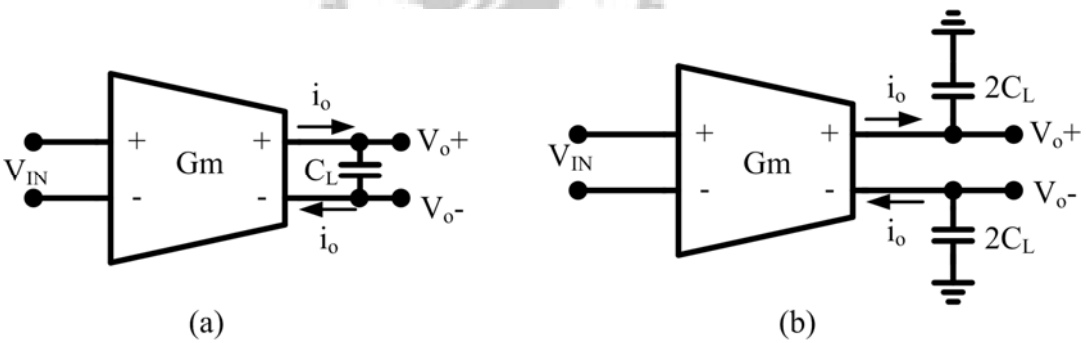


Fig. 4.1 The fully differential integrator

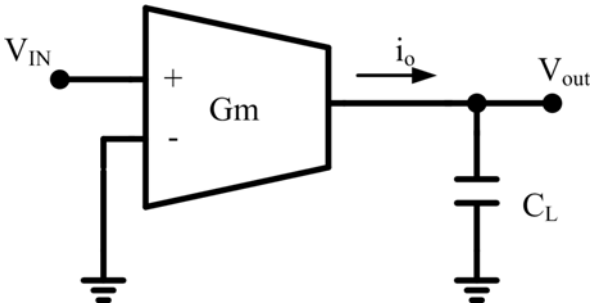


Fig. 4.2 The single-ended integrator

In Fig. 4.2, the ideal transconductanor has an infinite input resistance and

infinite output resistance, and the output voltage in this integrator could be derived as:

$$H(s) = \frac{V_{out}(s)}{V_{IN}(s)} = \frac{g_m}{sC_L} \tag{4.1}$$

with $s=j\omega$, which equation (4.1) could be described as $H(j\omega) = g_m/j\omega \times C_L = [R(j\omega) + jX(j\omega)]^{-1}$. In equation (4.1), we can see that the ideal integrator has infinitely high DC gain. As well, since phase margin defines as $PM=-180^\circ+\tan^{-1}(X(j\omega)/R(j\omega))$ and quality factor defines as $Q(j\omega)=X(j\omega)/R(j\omega)$, the ideal transconductor has $PM=-90^\circ$ for all frequencies and infinite quality factor. Finally, the unity gain frequency for the integrator is:

$$\omega_T = \frac{g_m}{C_L} \tag{4.2}$$

4.2.2 Non-ideal effects in the integrator

For non-ideal tranconductors, they have non-zero output conductance and a delay in transfer function. Since transconductors have parasitic poles and zeros, there is a delay in the integrator transfer function. However, these poles and zeros effects could be modeled with a single effective zero due to parasitic poles and zeros locating at much higher frequency than the unity gain frequency. The zero could be at right complex half-plane (RHP) for the phase lag or at left complex half-plane (LHP) for the phase lead.

The non-ideal integrator could be modeled as Fig. 4.3. From Fig. 4.3, the transfer function for this non-ideal integrator is:

$$H_{nonideal} = \frac{V_{out}(s)}{V_{IN}(s)} = \frac{g_m}{g_o}\frac{1-s\tau_2}{1+s\frac{C_L}{g_o}} = A\frac{1-s\tau_2}{1+s\tau_1} \tag{4.3}$$

Hence, there are finite dominate pole and DC gain due to the non-zero output conductance given as:

$$\tau_1 = \frac{C_L}{g_o}, A = \frac{g_m}{g_o} \tag{4.4}$$

In Fig. 4.4, the ideal as well as non-ideal magnitude and phase responses are given. Normally $|1/\tau_1| << \omega_T << |1/\tau_2|$.

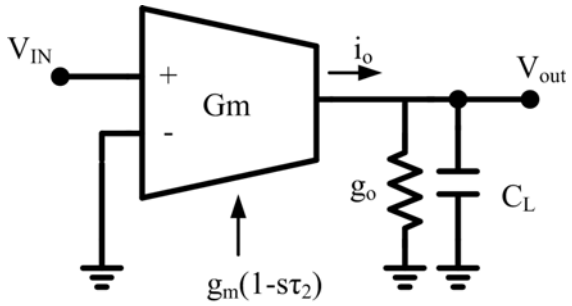


Fig. 4.3 The non-ideal single-ended integrator

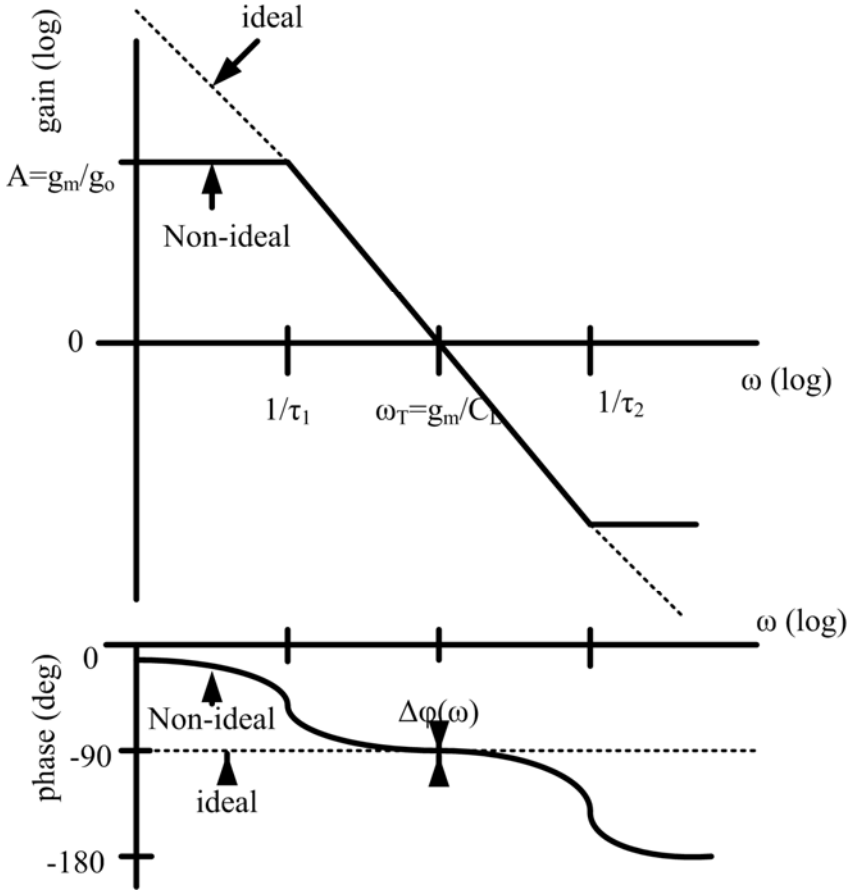


Fig. 4.4 Gain and phase of an ideal integrator and a non-ideal integrator

From Fig. 4.4, the finite DC gain and the parasitic zero cause the deviation of the integrator phase from -90°. The phase error is defined as:

$$\Delta\varphi(\omega) = \arg[H_{nonideal}(\omega)] + 90° \tag{4.5}$$

This error is a principal source of errors in filters. Next, we rewrite the transfer function as:

$$H_{nonideal}(\omega) = \frac{1}{R(\omega) + jX(\omega)} \tag{4.6}$$

Hence, the quality factor of an integrator is defined as:

$$Q_{nonideal}(\omega) = \frac{X(\omega)}{R(\omega)} = \tan(-\arg(H_{nonideal}(j\omega))) \tag{4.7}$$

From equation (4.3), (4.6), and (4.7), we can get the reciprocal value of the quality factor as:

$$\frac{1}{Q_{nonideal}(\omega)} \approx \frac{1}{\omega\tau_1} - \omega\tau_2 \tag{4.8}$$

From equation (4.8), the quality factor is infinite at the frequency which is the geometric mean of the dominant pole and the effective parasitic zero. Note that this condition holds as the output conductance g_o and the delay τ_2 have the same sign. The phase at that frequency is also exactly -90°.

4.3 Fourth order filter by cascading two biquad sections

In this section, the 4th order filter is presented. Since the proposed OTAs are used to compose of 4th order filter, the filter must be introduced. However, we will first introduce the resistor and inductor blocks, and then a biquad section will be discussed. Finally, the 4th order filter and output buffers will be described.

4.3.1 Resistor and inductor blocks

Since RLC are the basic elements for composing of the filters, the following will introduce the methods using the transconductors as resistors and inductors [14]

Resistors:

First, the resistor model is discussed. The Fig. 4.5 shows the resistor configuration for single-ended transconductor and differential transconductor. In Fig. 4.5, since the transconductor input is an open circuit ideally, the input current I_i is

equal to the transconductance output current I_o as:

$$I_i = I_o = g_m V_i \tag{4.9}$$

Thus, the configuration represents a resistor as its equivalent resistance as:

$$R = \frac{V_i}{I_i} = \frac{1}{g_m} \tag{4.10}$$

Note that it must maintain negative feedback when forming the gm-based resistor. If the feedback connection becomes positive, the resistance will be negative.

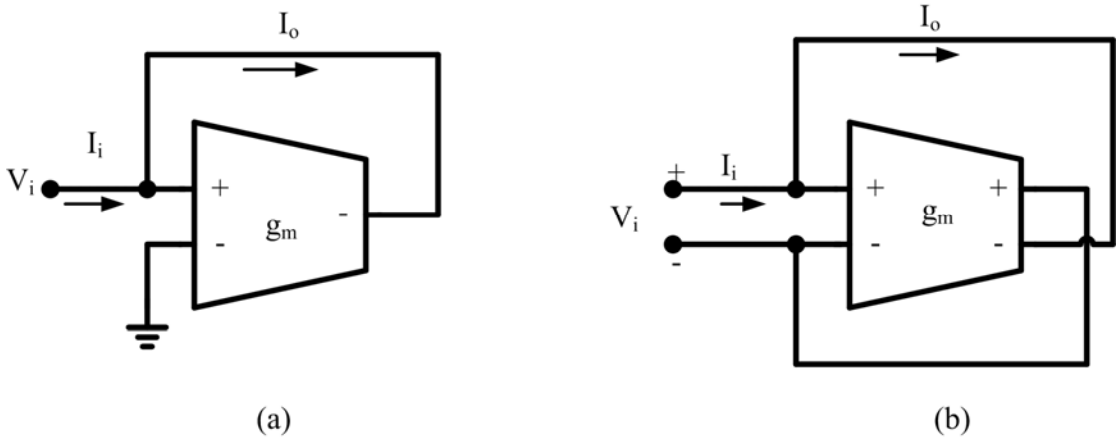


Fig. 4.5 The resistor elements using transconductors

Inductor:

In the following, the inductor element for using transconductor is discussed. The configuration for this element is shown in Fig. 4.6. From Fig. 4.6, the current equations could be:

$$I_1 = g_{m2} V_2 \tag{4.11}$$

$$I_2 = g_{m1} V_1 \tag{4.12}$$

Also, based on the voltage across the capacitor C, the following equation could be got.

$$V_2 = I_2 \times \frac{1}{sC} \tag{4.13}$$

Hence, the inductor using transconductor block can be got as its inductance being:

$$sL = \frac{V_1}{I_1} = \frac{1}{g_{m1} g_{m2}} \frac{I_2}{V_2} = \frac{1}{g_{m1} g_{m2}} sC \tag{4.14}$$

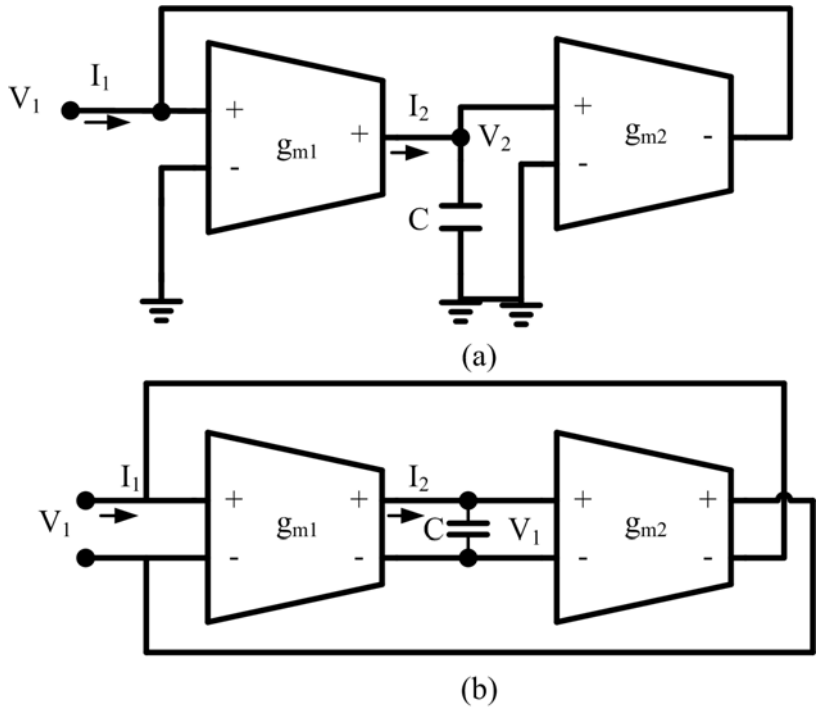


Fig. 4.6 The inductor elements using transconductors

4.3.2 Biquad Section

The passive RLC circuit of the GIC biquad is shown in Fig. 4.7. From this figure, the transfer function is as:

$$\frac{V_2}{V_1} = \frac{\frac{1}{R}}{\frac{1}{R} + sC_1 + \frac{1}{sL}} \tag{4.15}$$

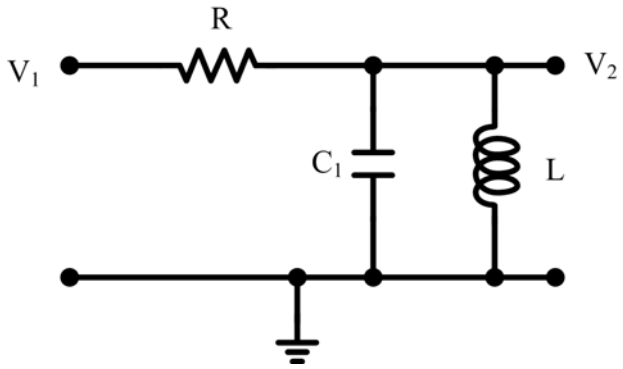


Fig. 4.7 The second order bandpass filter for passive RLC prototype

Using the elements discussed in subsection 4.3.1, the active biquad section could be shown in Fig. 4.8 for the single-ended and differential models.

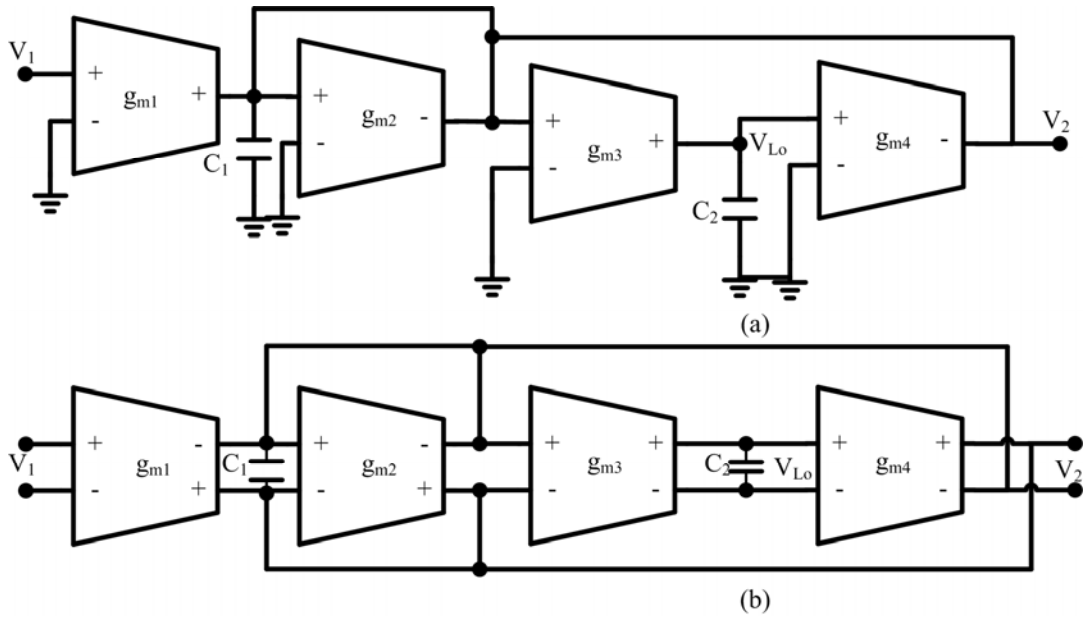


Fig. 4.8 The second order bandpass and lowpass filter for active transconductance-C prototype

For $R = 1/g_{m1}$ and $L = C_2/g_{m3}g_{m4}$, the transfer function for bandpass filter will be:

$$\frac{V_2}{V_1} = -\frac{sC_2g_{m1}}{s^2C_1C_2 + sC_2g_{m2} + g_{m3}g_{m4}} \tag{4.16}$$

Using the fact that

$$V_{Lo} = -\frac{g_{m3}}{sC_2}V_2 \tag{4.17}$$

The transfer function for lowpass filter is:

$$\frac{V_{Lo}}{V_1} = \frac{g_{m1}g_{m3}}{s^2C_1C_2 + sC_2g_{m2} + g_{m3}g_{m4}} \tag{4.18}$$

The advantage of the biquad section is the cascade fashion, and the loop is very stable at higher order filter. The disadvantage is the loading effect, and the sensitivity of the biquad section to component variation is larger than the LC-ladder structure.

4.3.3 4th Order linear-phase Filter

The implement 4th order filter by cascading two biquad sections is shown in Fig. 4.9. Since the outputs in second and fourth transconductors of a biquad section are

connected together with the output in first transconductor, it needs a common mode feedfack circuit to fix the outputs of the three transconductors to the reference voltage. The common mode feedforward circuit in each transconductor depends on the requirement of the transconductor.

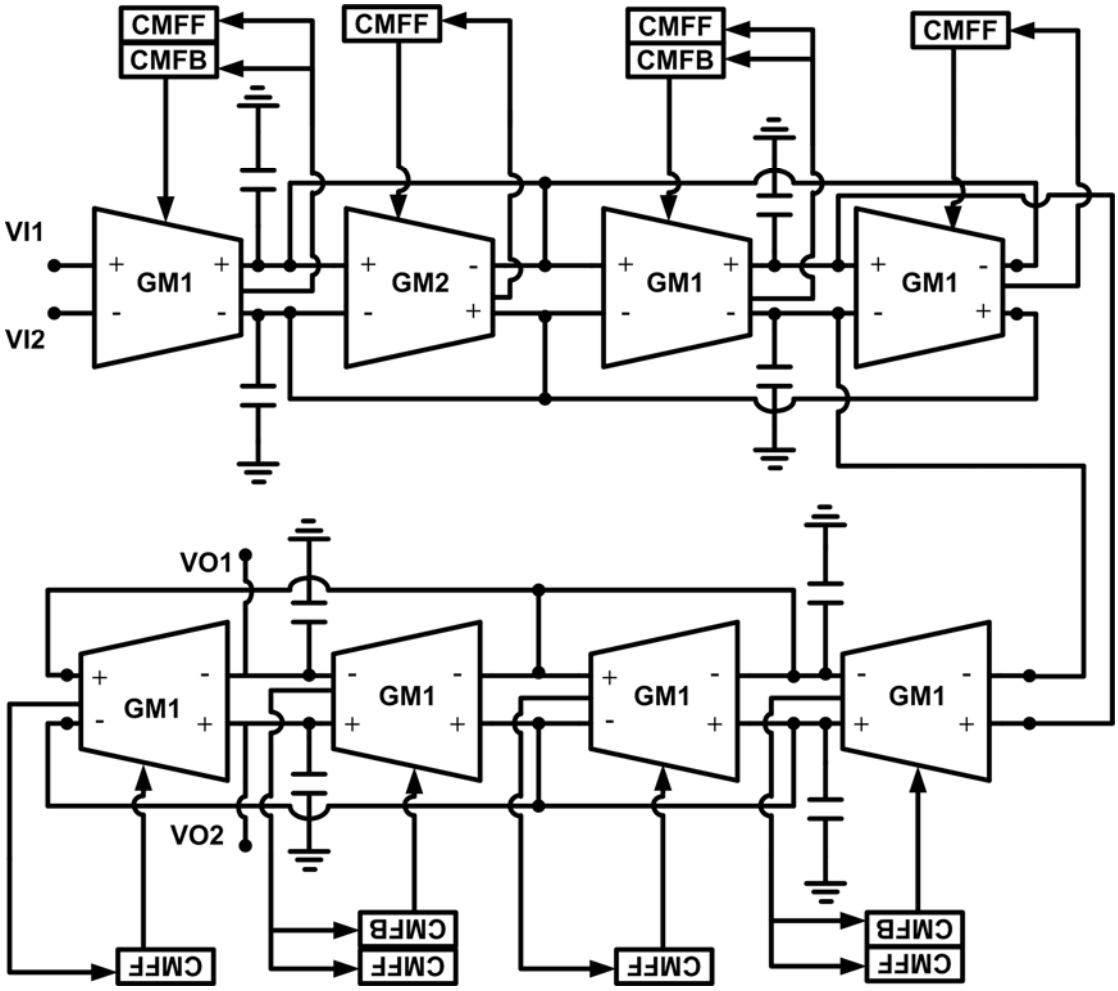


Fig. 4.9 The 4th order lowpass filter

From equation (4.18), the cutoff frequency ω_0 and the quality factor Q for a biquad section can be expressed as:

$$\omega_0 = \frac{g_{m1}}{C} \tag{4.19}$$

$$Q_p = \frac{g_{m1}}{g_{m2}} \tag{4.20}$$

$$K = 1 \tag{4.21}$$

From equation (4.19), the unity gain frequency of the first transconductor in the

biquad section is equal to the cutoff frequency of the biquad. The denominator of the biqurad section and the changed phase of the implement 4th order filter are given in Table 4.1.

TABLE 4.1 Denominator of biquad section transfer function

Filter order N	E(s) for △θ= 0.05°
4	$(s^2+1.929s+1.156)\times(s^2+1.489s+2.57)$

For this filter, the changed phase should less than 0.05°. From Table 4.1, the quality factors and normalized cutoff frequencies for first and second biquad section are Q_1=0.5573, ω_{01}=1.0752, Q_2=1.0652, ω_{02}=1.5865.

4.3.4 Output Buffers

When measuring the filter, the loads in the measurement devices will influence the filter. Therefore, the filter requires an output buffer to avoid the loading effects from the measurement devices. The following introduces two output buffer circuits: one is using a transconductor-based resistor as the output buffer, and the other is using source follower as output buffer, which is used in the implement filter.

Fig. 4.10 shows the output buffer using transconductor-based resistor. For adding this output buffer, the transfer function becomes as:

$$T(s)=\frac{V_{obuff}}{V_i}=\frac{V_{obuff}}{V_o}\times\frac{V_o}{V_i}=T_{buff}(s)\times T_{filter}(s) \tag{4.22}$$

Hence, the total transfer function must be divided by the output buffer transfer function to get the filter transfer function.

$$\frac{T(s)}{T_{buff}(s)}=\frac{T_{filter}(s)\times T_{obuff}(s)}{T_{buff}(s)}=T_{filter}(s) \tag{4.23}$$

However, the signal in filter's output will be attenuated by the output buffer. This will make it difficult for measurement since the signal in the output buffer will be very small.

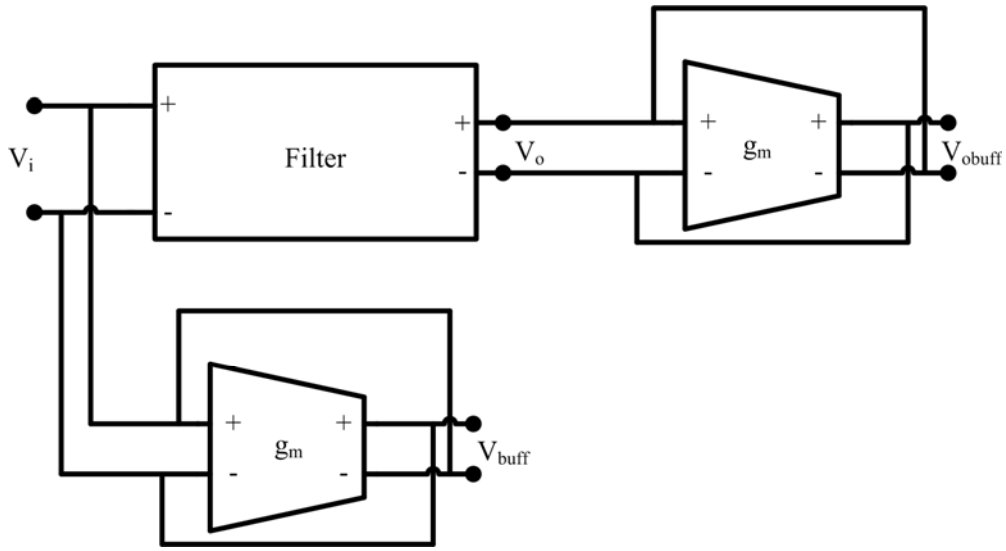


Fig. 4.10 The output buffer using transconductor-based resistor

Another output buffer circuit is source follower as shown in Fig. 4.11. Since the gain of the source follower is about 1, so the signal in the output node would not be attenuated a lot for which the measurement will be more easily. Also, there is no need for another path to give the transfer function back to the filter transfer function due to the transfer function for the source follower being about 1. However, the current in source follower must be large to make the DC gain of the filter be about 0 dB.

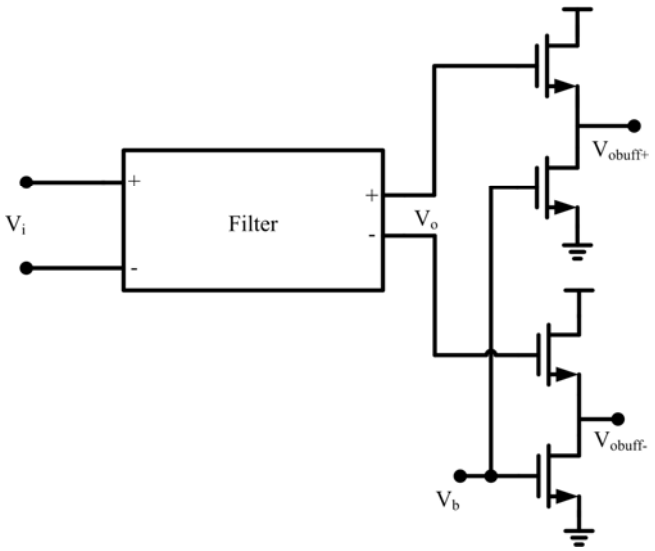


Fig. 4.11 The output buffer using source follower

Chapter 5

Simulation and Experimental Results

5.1 Introduction

In order to express the performances of the transconductors and filters, the following results about OTAs and filters must be given.

Common Mode Rejection Ratio (CMRR):

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| \tag{5.1}$$

where $A_{CM\text{-}DM}$ denotes common-mode to differential-mode conversion.

Power Supply Rejection Ratio (PSRR):

In order to prevent the noise from the power supply node, the circuits must have good PSRR, which definition is:

$$PSRR = \frac{V_{out}/V_{in}}{V_{out}/V_{DD}} = \frac{A_{DM}}{A_{PS-DM}} \tag{5.2}$$

Power Consumption or Current Consumption:

The circuits must provide about their power consumption or current consumption, and their relation is as below:

$$P = I \times V \tag{5.3}$$

Linearity:

As described before, the linearity is the main disadvantage for the transconductance-C filter. Hence, the linearity is the main consideration for the

transconductor. The following expresses two methods to describe the linearity performance about the transconductors and filters.

Total Harmonic Distortion (THD):

When a signal applies to the transcoductors or filters at a reference frequency, the linear output signal must have the same frequency. However, the output in practice will have frequency components at harmonics of the input waveform, including fundamental harmonic. Therefore, the total harmonic distortion of a signal is defined to be the ratio of the total power of the second and higher harmonic components to the power of the fundamental for that signal, as shown below in units of dB:

$$THD = 10 \times \log\left(\frac{V_{h2}^{\ 2} + V_{h3}^{\ 2} + V_{h4}^{\ 2} + \cdots}{V_f^{\ 2}}\right) \tag{5.4}$$

Usually, the higher harmonic distortions are very small and can be neglect. As well, the even harmonic distortions are canceled for fully differential circuits. Therefore, the third harmonic distortion is the dominant distortion and another definition for the third harmonic distortion is equal to THD approximately. The definition in units of dB is:

$$HD3 = 10 \times \log\left(\frac{V_{h3}^{\ 2}}{V_f^{\ 2}}\right) \tag{5.5}$$

Third-order intermodulation (IM3):

Filter linearity is often worse when higher input signal frequencies are applied due to nonlinear capacitances or nonlinear signal cancellation. Thus, it is useful to measure filter linearity with input signals near the upper edge of the passband. However, the harmonic components fall in the stopband of the filter, thus the THD value is falsely improved. So the IM3 is used to measure filter linearity near the upper passband edge. Consider a nonlinear system for which the higher harmonic

distortions can be neglect and the even order distortions are cancelled due to fully differential. Therefore, the relation about input and output is:

$$V_o(t) \cong a_1 V_{in}(t) + a_3 V_{in}^{\ 3}(t) \tag{5.6}$$

If a sinusoidal signal is given as:

$$V_{in}(t) = A\cos(\omega t) \tag{5.7}$$

Using equation (5.6) and (5.7), the output signal could be:

$$V_o(t) = H_{D1}\cos(\omega t) + H_{D3}\cos(3\omega t) \tag{5.8}$$

where $H_{D1} = a_1 A$ and $H_{D3} = a_3 A^3/4$. Thus, the third-order harmonic distortion ratio is:

$$HD3 \equiv \frac{H_{D3}}{H_{D1}} = (\frac{a_3}{a_1})(\frac{A^2}{4}) \tag{5.9}$$

As discussed above, this distortion term lies at 3ωt which will be improved by filter due to falling in the stopband. Hence, the intermodulation test is used to move the distortion term back near the frequency of the input signal.

Nowadays, if the input signal consists two equally sized sinusoidal signal as:

$$V_{in}(t) = A\cos(\omega_1 t) + A\cos(\omega_2 t) \tag{5.10}$$

From equation (5.6) and (5.10), the output signal can be shown to be approximated by:

$$\begin{aligned} V_o(t) \cong & (a_1 A + \frac{9a_3}{4} A^3)[\cos(\omega_1 t) + \cos(\omega_2 t)] \\ & + \frac{a_3}{4} A^3[\cos(3\omega_1 t) + \cos(3\omega_2 t)] \\ & + \frac{3a_3}{4} A^3[\cos(2\omega_1 t + \omega_2 t) + \cos(2\omega_2 t + \omega_1 t)] \\ & + \frac{3a_3}{4} A^3[\cos(\omega_1 t - (\omega_2 - \omega_1)t) + \cos(\omega_2 t + (\omega_2 - \omega_1)t)] \end{aligned} \tag{5.11}$$

where the second and third terms express the distortions lied in the stopband. The fourth term means that two distortions are very close to the input signal. Now, the intermodulation distortion levels are given as:

$$I_{D1} = a_1 A \tag{5.12}$$

$$I_{D3} = \frac{3a_3}{4} A^3 \tag{5.13}$$

where it assume $a_1A >> 9a_3A^3/4$.Thus, the ratio of these two is the third-order intermodulation value, given by:

$$IM3 = \frac{I_{D3}}{I_{D1}} = (\frac{a_3}{a_1})(\frac{3A^2}{4}) \tag{5.14}$$

5.2 Performance of the source degeneration Current Feedback OTA and filter

5.2.1 Simulation Results of Transconductor

Transconductance:

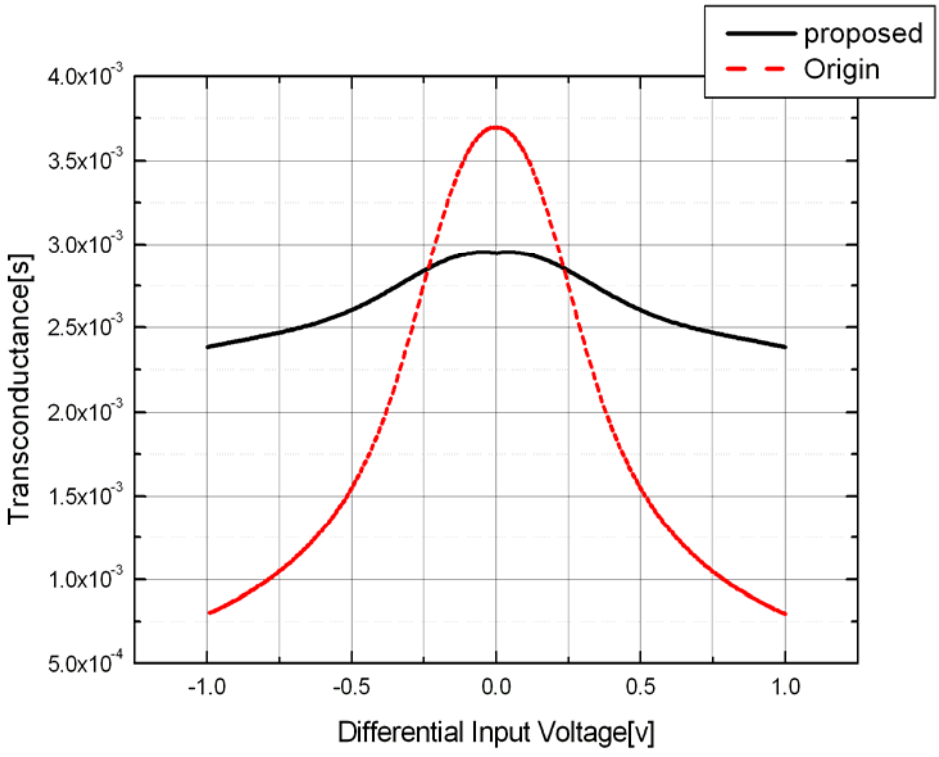
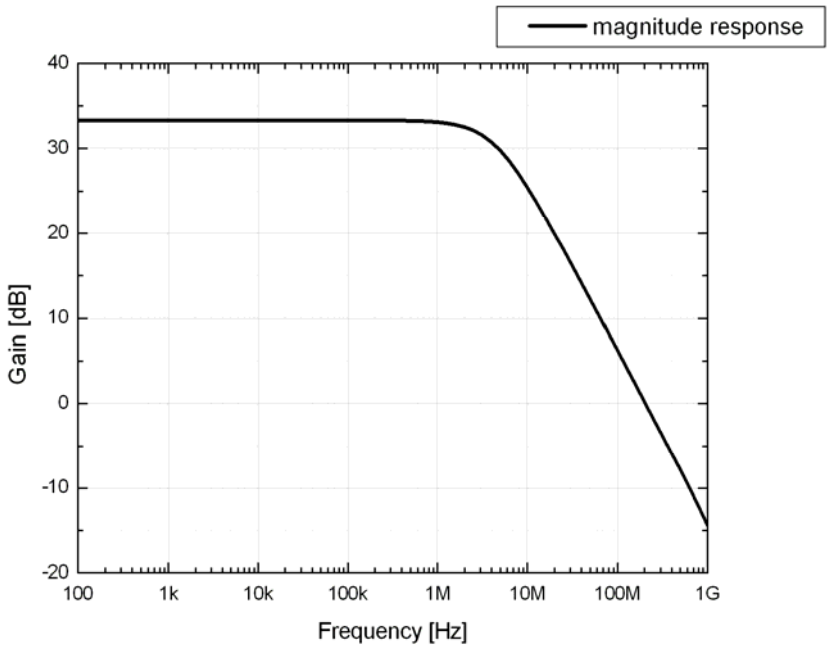


Fig. 5.1 Transconductance of OTA for traditional and proposed source degeneration circuit

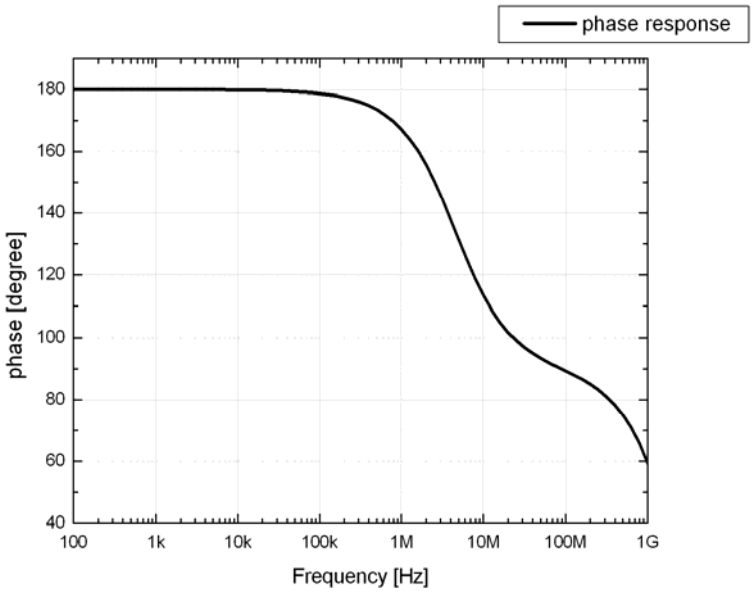
In Fig. 5.1, the proposed circuit has more flatness transconductance than the

traditional circuit, which means the proposed circuit has better linearity than the traditional circuit.

Magnitude & Phase Response:



(a)



(b)

Fig. 5.2 (a) Magnitude response (b) phase response for the transconductor

In Fig. 5.2 (a), the DC gain is 33.3dB and the unity gain frequency is 205MHz. As shown in Fig. 5.2 (b), the phase margin is 84.9°.

THD:

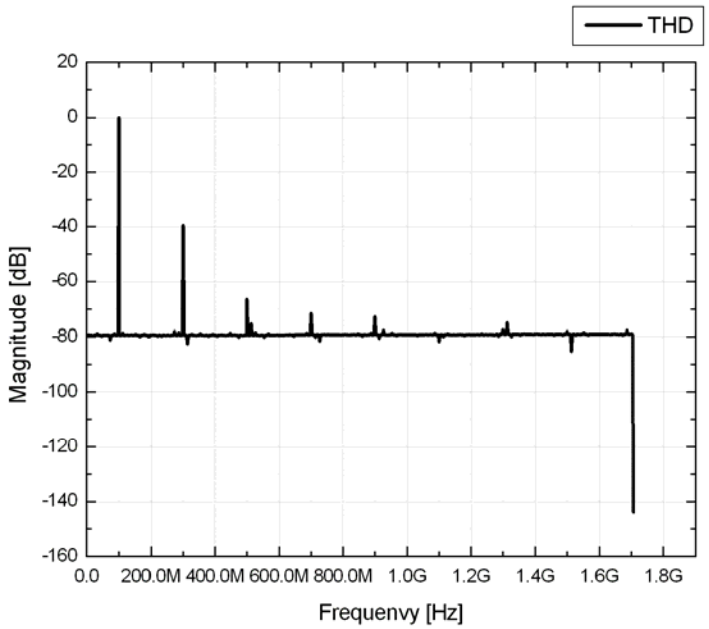


Fig. 5.3 The total harmonic distortion for the transconductor

In Fig. 5.3, the HD3 is about -40dB for 100MHz 400mV V_{pp} input signal. The proposed circuit has better HD3 about 6dB than the traditional circuit.

CMRR & PSRR:

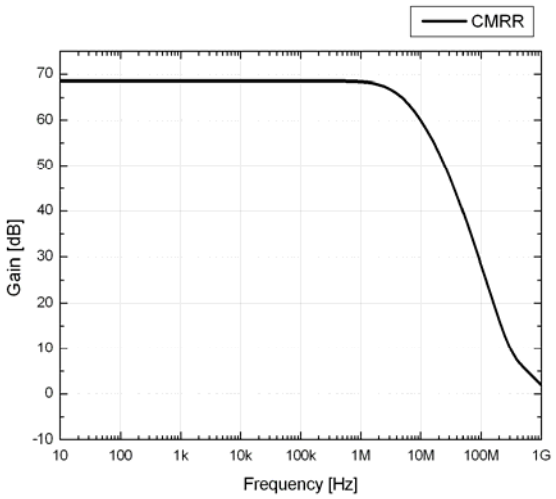


Fig. 5.4 The common mode rejection ratio for the transconductor

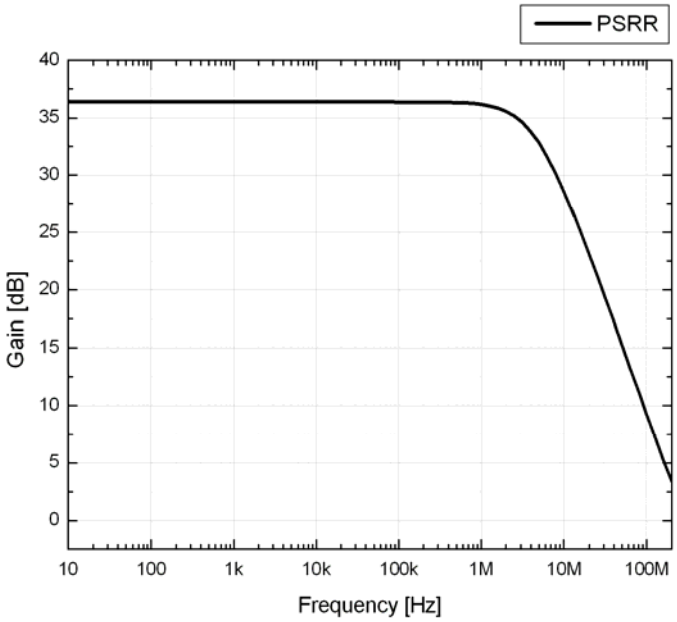
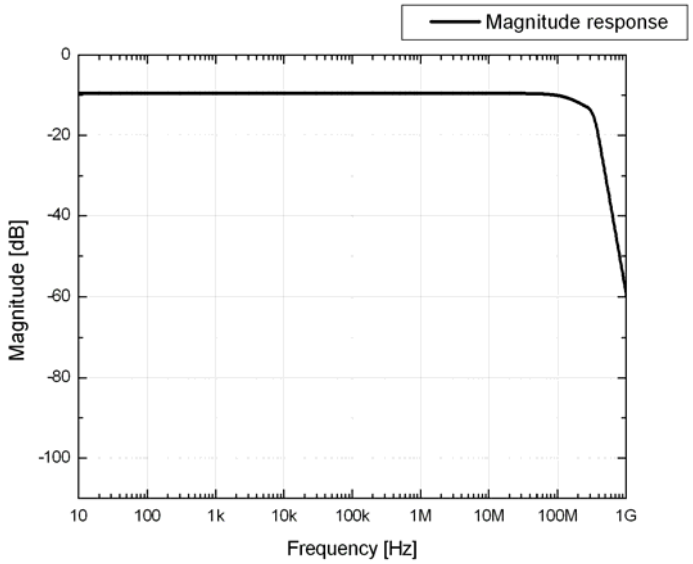


Fig. 5.5 The power supply rejection ratio for the transconductor

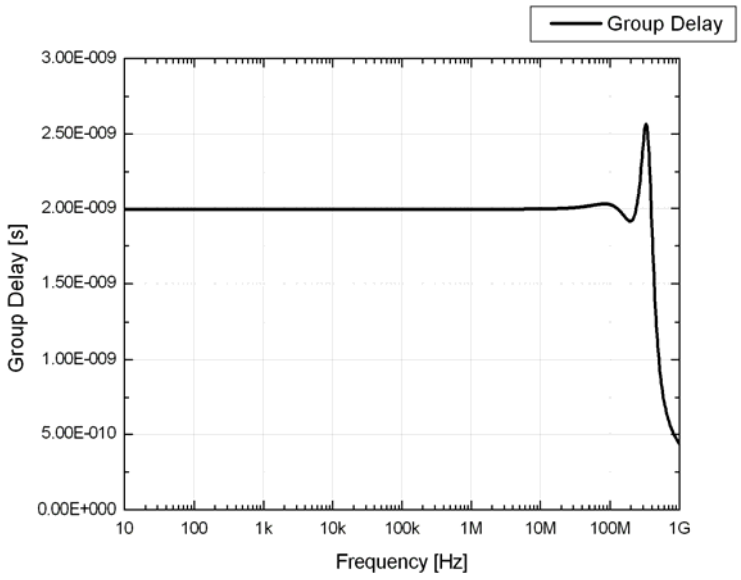
In Fig. 5.4 and Fig. 5.5, there are 68.6dB CMRR and 36.4dB PSRR at DC for the transconductor.

5.2.2 Simulation Results of Filter

Cutoff Frequency & Group Delay:



(a)



(b)

Fig. 5.6 The magnitude and group delay response for filter

From Fig. 5.6, the cutoff frequency is about 250MHz, which is the least requirement of the ultra wideband application. The group delay variation is about 3% at the cutoff frequency. The maximum value of the magnitude response is not 0dB due to the drivers, which need very large current to push the DC gain of filter to 0dB.

THD/IM3:

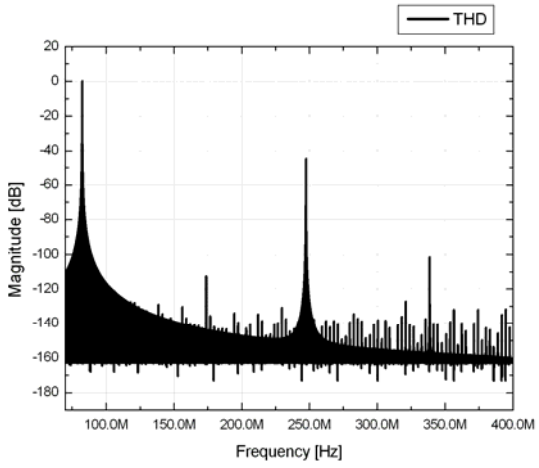


Fig. 5.7 The total harmonic distortions for filter

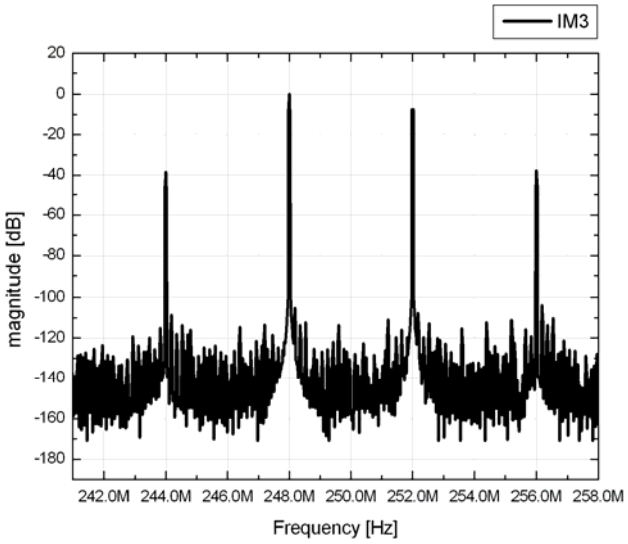


Fig. 5.8 The third-order intermodulation distortions for filter

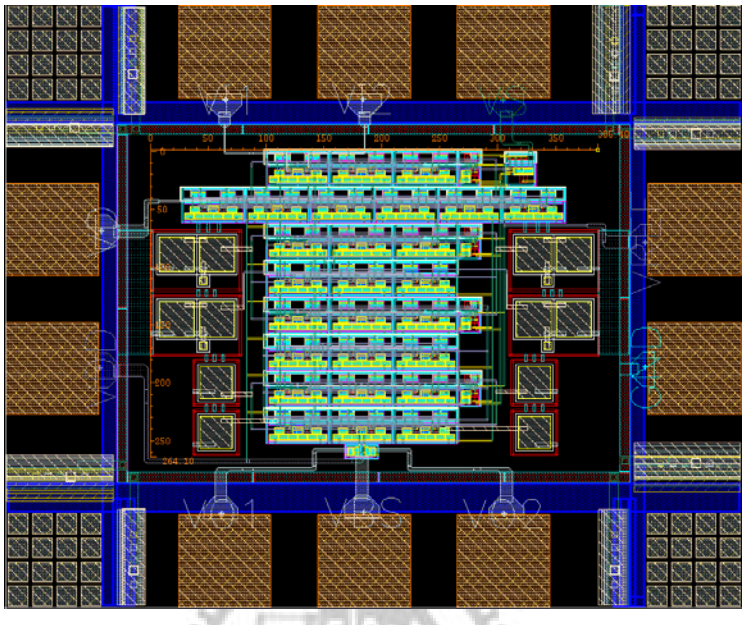
From Fig. 5.7 and Fig. 5.8, the HD3 is -44.9dB for 82.5MHz input signal and the IM3 is -38.5dB for 252MHz and 248MHz input signal. IM3 is usually worse than the HD3 for which IM3 = $(a_3/a_1)\times(3A^2/4)$ and HD3 = $(a_3/a_1)\times(A^2/4)$.

TABLE 5.1 The spec for the filter

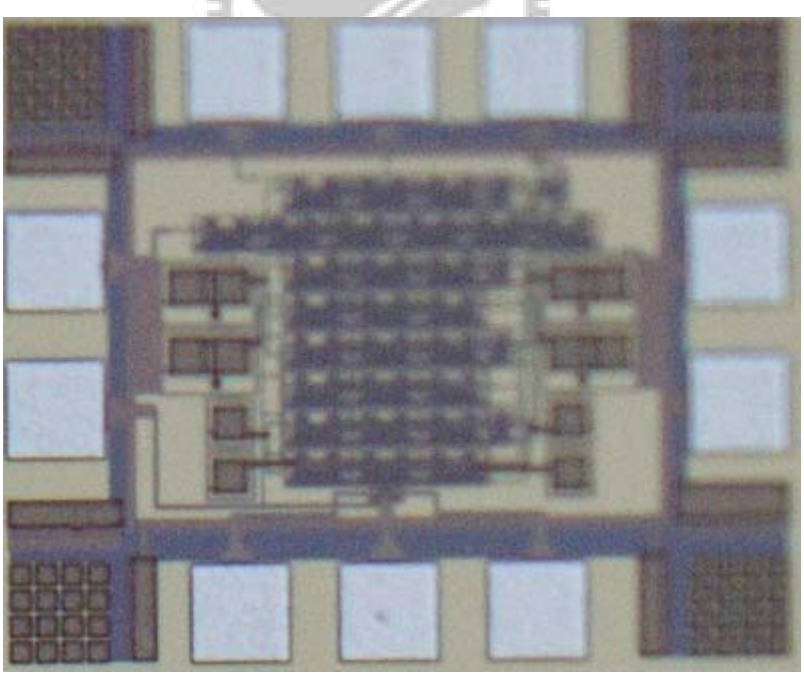
	spec
Power supply	1.8v
Filter type	4th order equiriplple linear phase filter
Cutoff frequency	250MHz
Input swing	$0.2V_{pp}$
HD3 IM3	-44.9dB @ 82MHz input signal -38.5dB @ 250MHz input signal
Group delay variation	$3\%@f_{cutoff}$
Active area	$0.386*0.264mm^2$
Power consumption	42mW

5.2.3 Measurement Results of Filter

The layout for this circuit is shown in Fig. 5.9 (a) and the die photo is shown in Fig. 5.9 (b). The active area is 0.386*0.264mm^2.



(a)

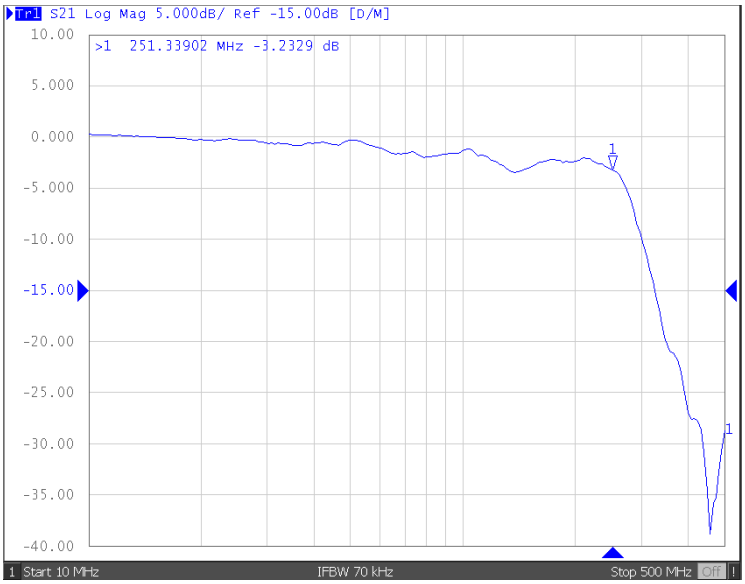


(b)

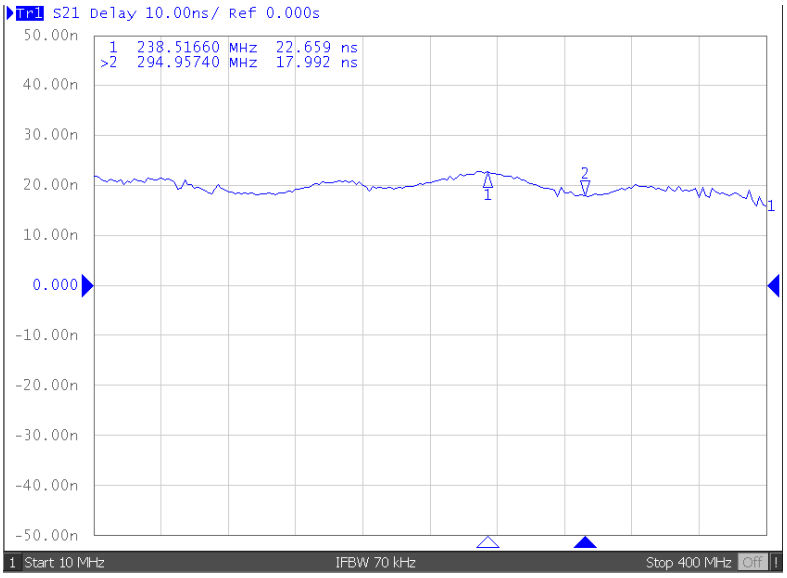
Fig. 5.9 (a) The layout for the filter (b) The die photo for the filter

The magnitude response and the group delay for the filter is shown in Fig. 5.10. The cutoff frequency is about 250MHz, which is least requirement for the UWB,

and the group delay variation is less than 5ns at the cutoff frequency.



(a)



(b)

Fig. 5.10 (a) The magnitude response for the filter (b) The group delays for the filter

The following measurements express the linearity performance. The Fig. 5.11 is the THD. From this figure, the HD3 is about -40dB for 80MHz input signal. By the way, the HD2 is -42.57dB, which is due to the mismatch for the current mirror pairs and mismatch for the input pair causing input offset. As described in before, the upper band of the filter will falsely improve the HD3, so the IM3 is used to express the linearity for the upper band of the filter. In Fig. 5.12, the IM3 is shown

to be about -35dB for 252MHz and 248MHz input signals.

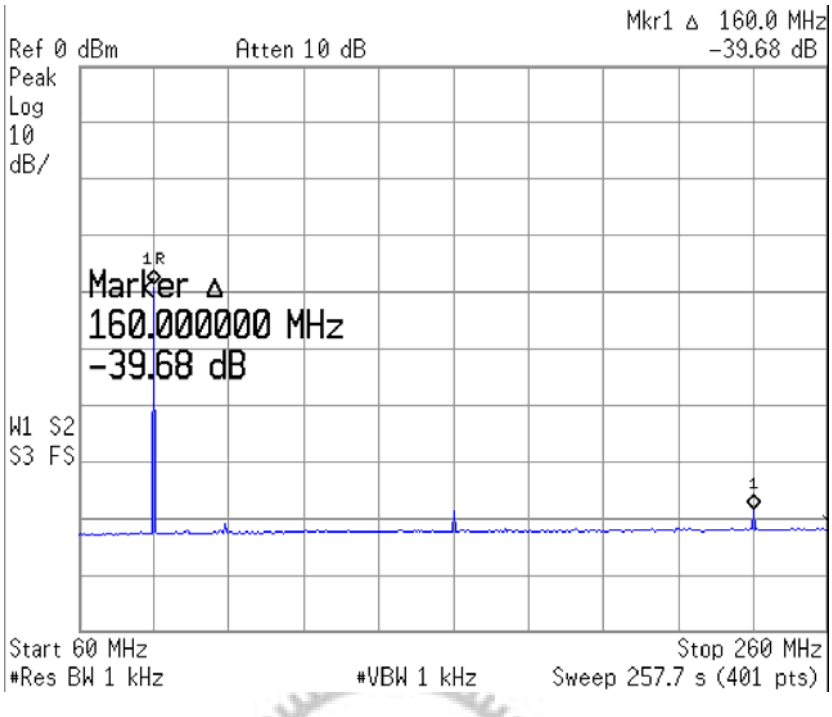


Fig. 5.11 The total harmonic distortions for the filter

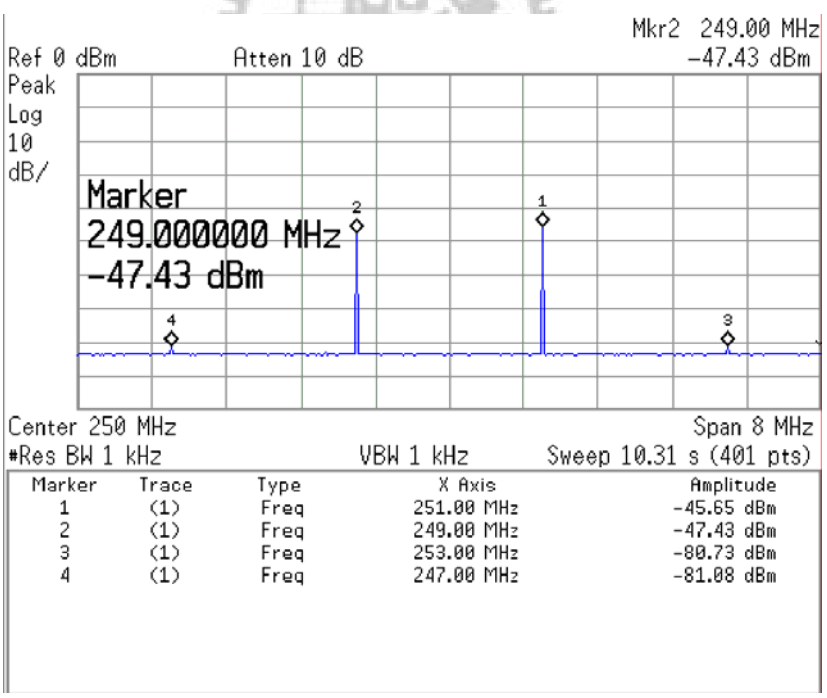


Fig. 5.12 The intermodulation distortions for the filter

The output noise is 251.9uV for the frequency from 10MHz to 250MHz as shown in Fig. 5.13.

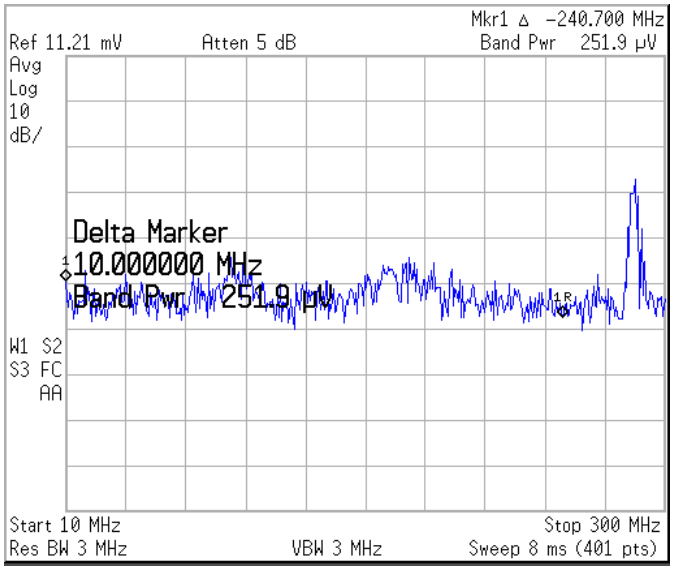


Fig. 5.13 The output noise for the filter

5.3 Performance of the Feedforward constant-Vds OTA and filter

5.3.1 Simulation Results of Transconductor

Transconductance:

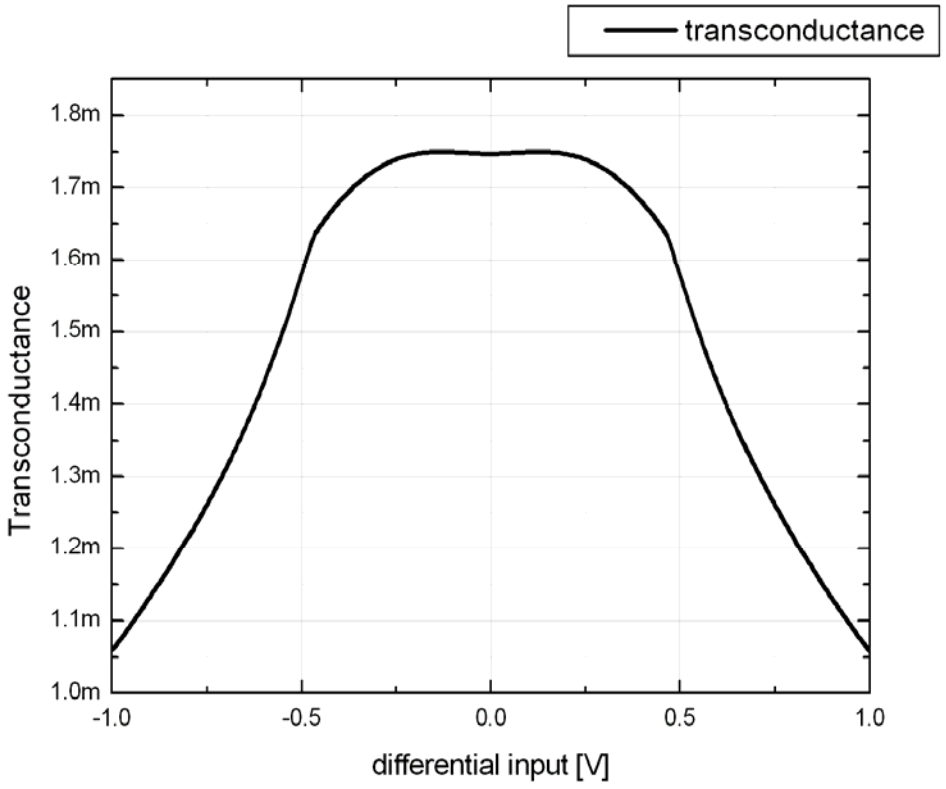
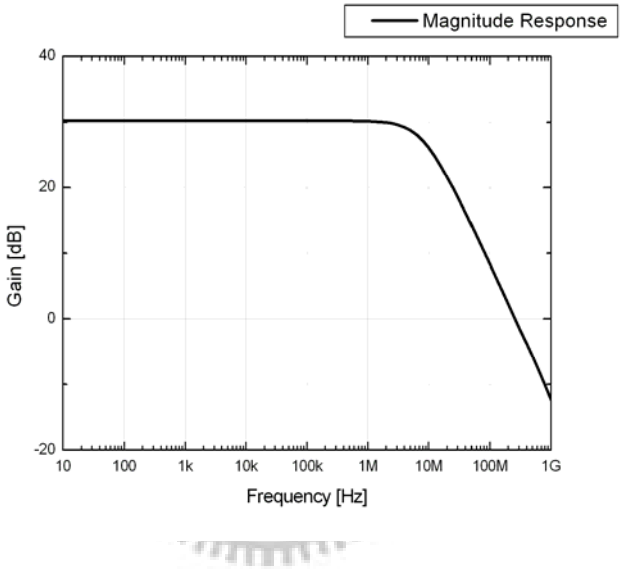


Fig. 5.14 Transconductance of OTA for low power feedforward-regulated circuit

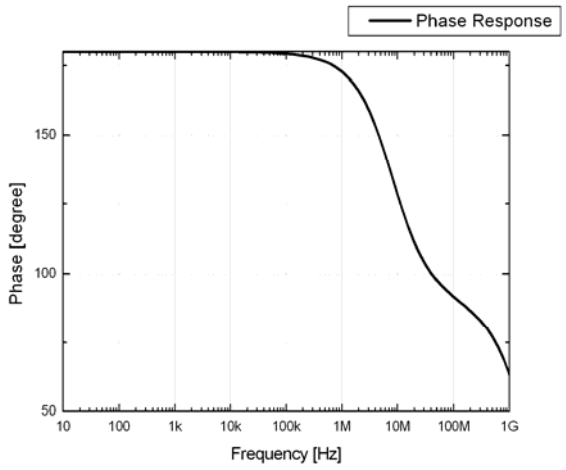
In Fig. 5.14, the proposed circuit has flatness transconductance at +0.25V~-0.25V differential input signal, and the maximum transcoductance value is about 1.75m (1/Ω).

Magnitude & Phase Response:

In Fig. 5.15 (a), the DC gain is 30.2dB and the unity gain frequency is 260MHz. As shown in Fig. 5.15 (b), the phase margin is 84.5°.



(a)



(b)

Fig. 5.15 (a) Magnitude response (b) phase response for the transconductor

THD:

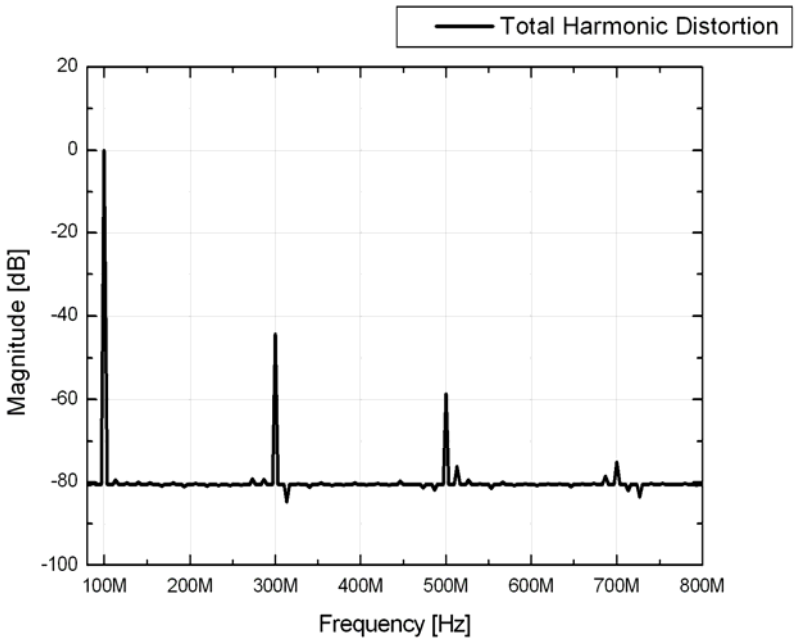


Fig. 5.16 The total harmonic distortion for the transconductor

In Fig. 5.16, the HD3 is about -44.4dB for 100MHz 600mV V_{pp} input signal.

CMRR & PSRR:

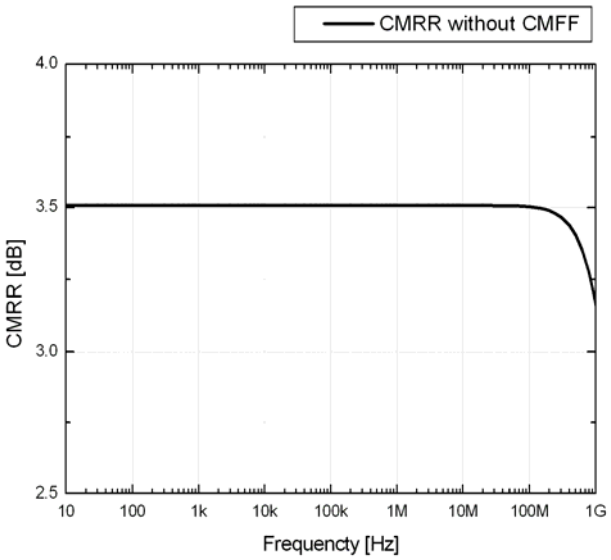


Fig. 5.17 The common mode rejection ratio for the transconductor without CMFF

From Fig. 5.17, the value of CMRR is 3.6dB for the transconductor without

common mode feedforward, which means a large value of common mode gain for the circuit. This means common mode noise will appear in the differential output to interfere the signal.

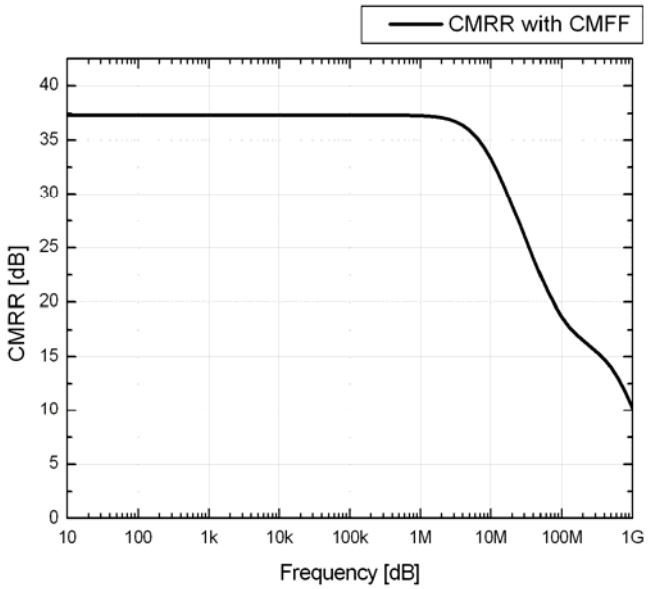


Fig. 5.18 The common mode rejection ratio for the transconductor with CMFF

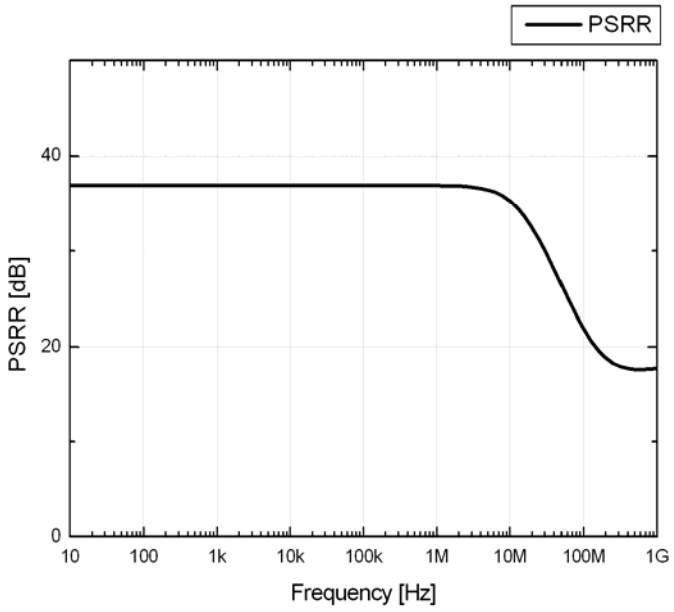


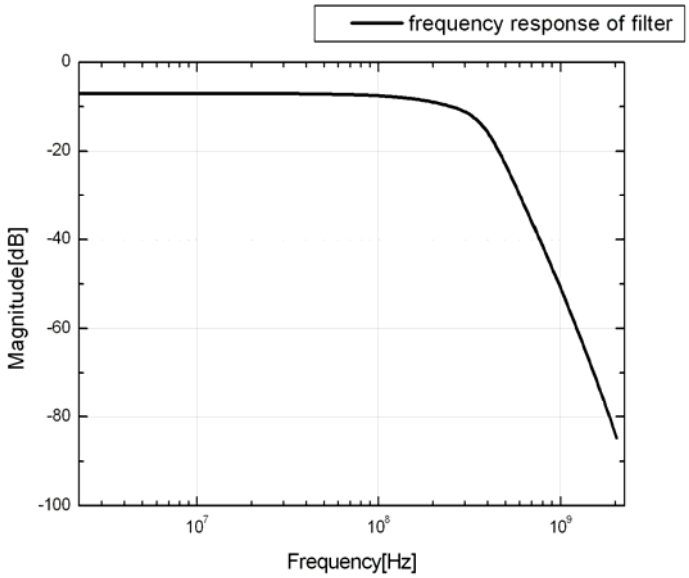
Fig. 5.19 The power supply rejection ratio for the transconductor

From Fig. 5.18, the value of the CMRR is improved from 3.6dB to 37.4dB with common mode feedforward circuit. In Fig. 5.19, there is 36.4dB PSRR at DC for the

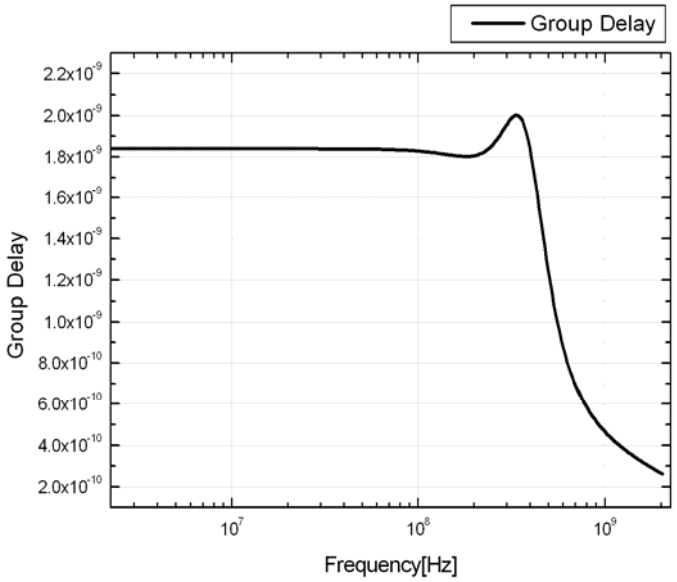
transconductor.

5.3.2 Simulation Results of Filter

Cutoff Frequency & Group Delay:



(a)



(b)

Fig. 5.20 The magnitude and group delay response for filter

From Fig. 5.20, the cutoff frequency is about 255MHz. The group delay variation is less than 5% up to 1.26 times the value of the cutoff frequency. The

maximum value of the magnitude response is not 0dB due to the drivers, which need very large current to push the DC gain of filter to 0dB.

THD/IM3:

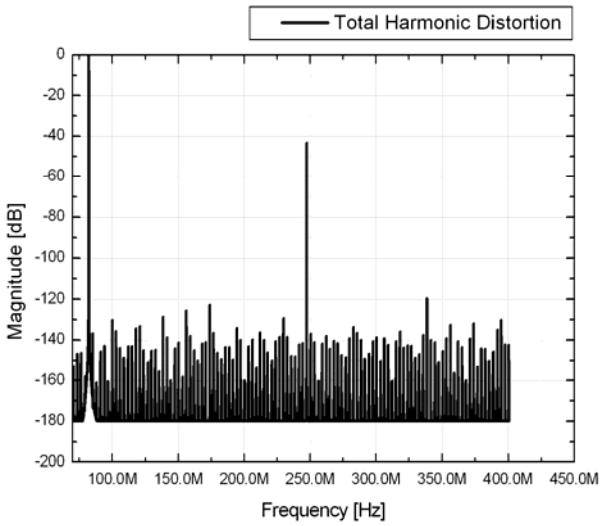


Fig. 5.21 The total harmonic distortions for filter

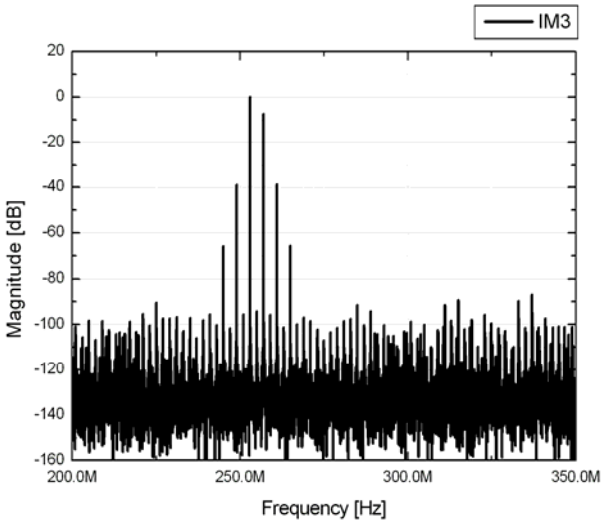


Fig. 5.22 The third-order intermodulation distortions for filter

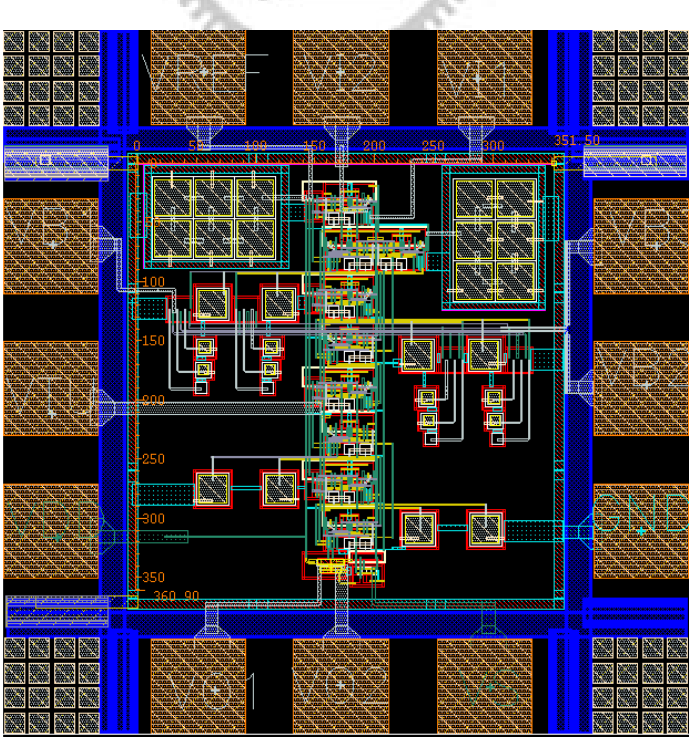
From Fig. 5.21 and Fig. 5.22, the HD3 is -43.3dB for 82.5MHz 400m input signal and the IM3 is -38.9dB for 257MHz and 253MHz input signal.

TABLE 5.2 The spec for the filter

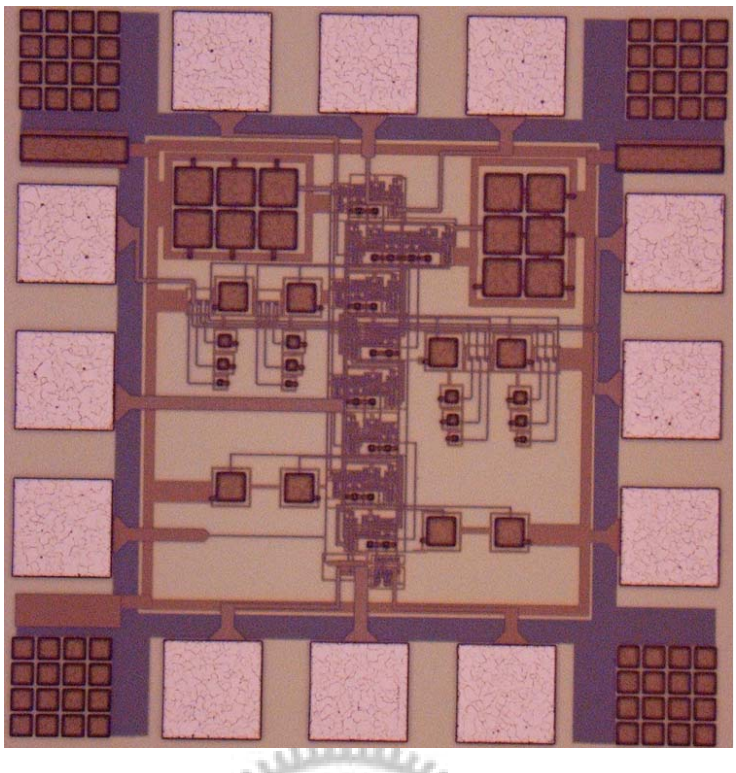
	spec
Power supply	1.8v
Filter type	4th order equiriplple linear phase filter
Cutoff frequency	255MHz
Input swing	$0.4V_{pp}$
HD3	-43.3dB @ 82MHz input signal
Group delay variation	$<5\%@1.26f_{cutoff}$
Active area	$0.3515*0.3609mm^2$
Power consumption	42mW

5.3.3 Measurement Results of Filter

The layout for this circuit is shown in Fig. 5.23 (a) and the die photo is shown in Fig. 5.23 (b). The active area is $0.3515*0.3609mm^2$.



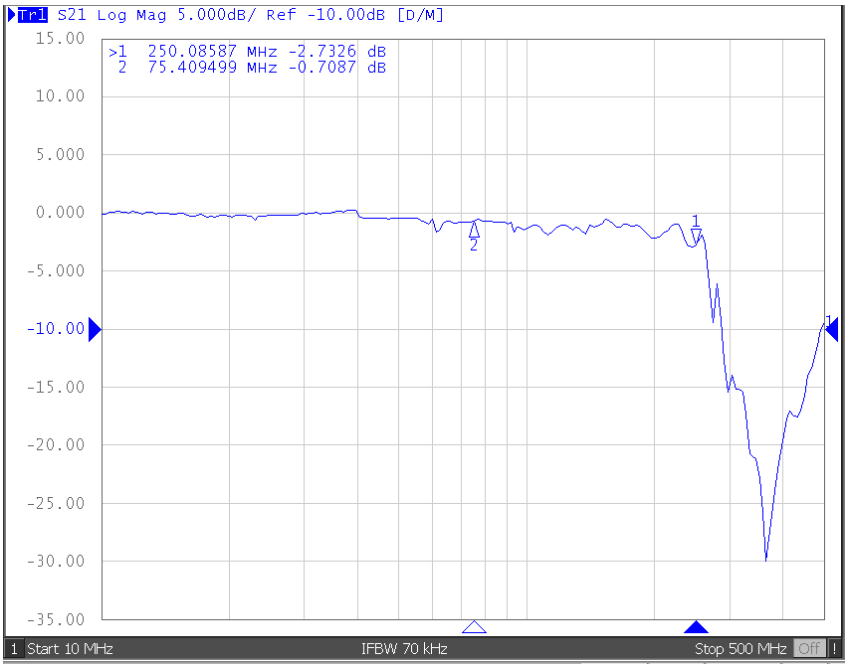
(a)



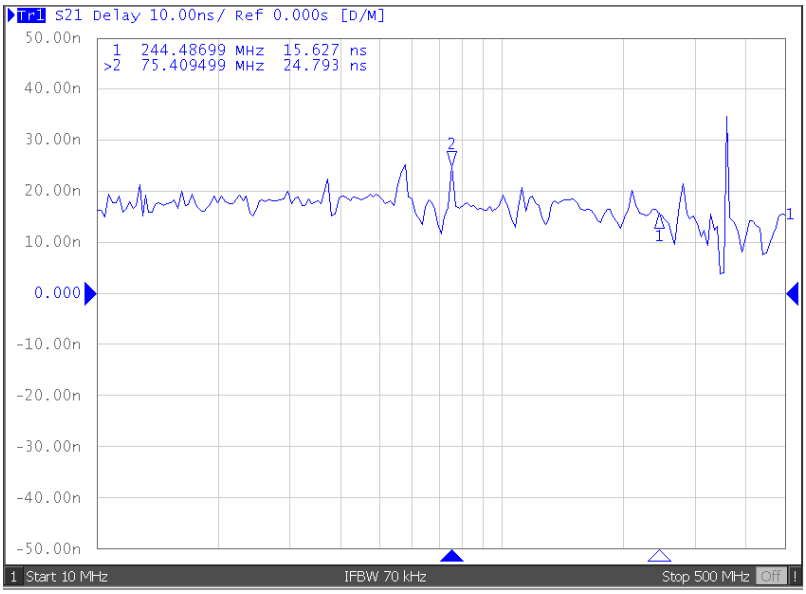
(b)

Fig. 5.23 (a) The layout for the filter (b) The die photo for the filter

The magnitude response and the group delay for the filter is shown in Fig. 5.24. The cutoff frequency is about 250MHz, which is least requirement for the UWB, and the group delay variation is less than 5ns at the cutoff frequency.



(a)



(b)

Fig. 5.24 (a) The magnitude response for the filter (b) The group delays for the filter

The following measurements express the linearity performance. The Fig. 5.25 is the THD. From this figure, the HD3 is about -40dB for 80MHz input signal. By the way, the HD2 is about -20dB, which is due to the mismatch for the current mirror pairs and mismatch for the input pair causing input offset. The second harmonic distortion maybe contributed due to the lower CMRR which is lower than the source degeneration with current feedback. As described in before, the upper band of the filter will falsely improve the HD3, so the IM3 is used to express the linearity for the upper band of the filter. In Fig. 5.26, the IM3 is shown to be about -36dB for 252MHz and 248MHz input signals.

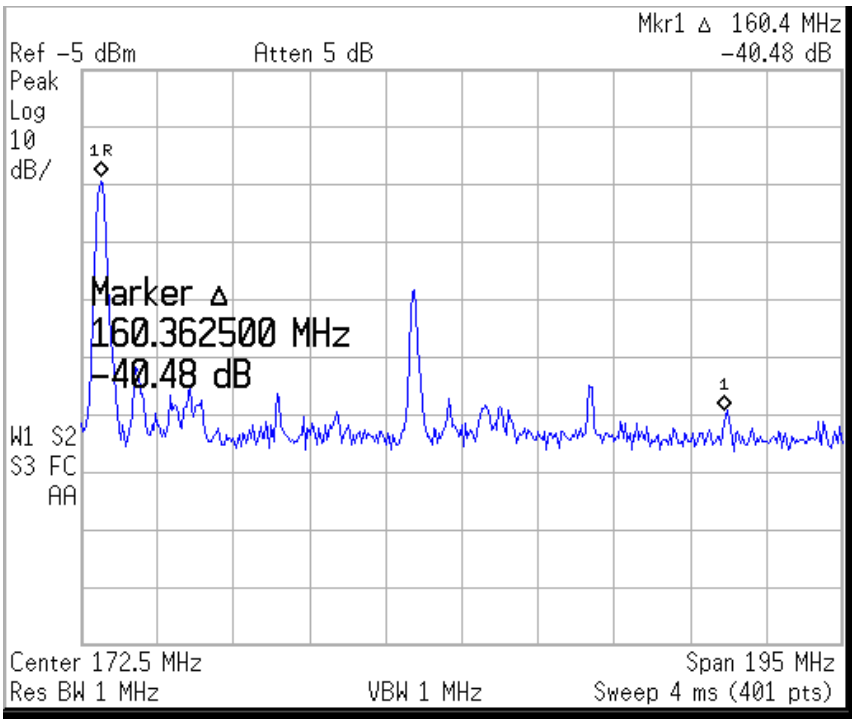


Fig. 5.25 The total harmonic distortions for the filter

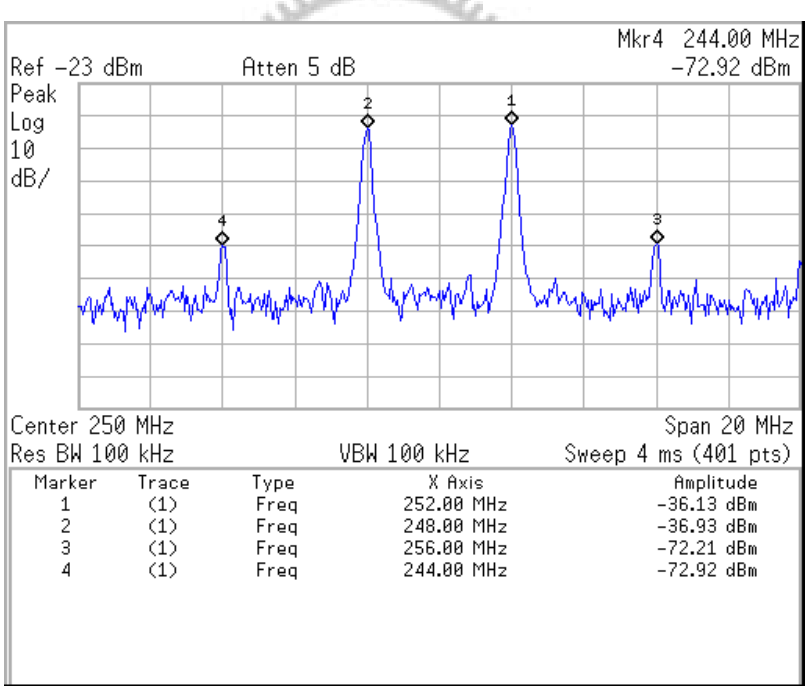


Fig. 5.26 The intermodulation distortions for the filter

The output noise is 182.7uV for the frequency from 10MHz to 250MHz as shown in Fig. 5.27.

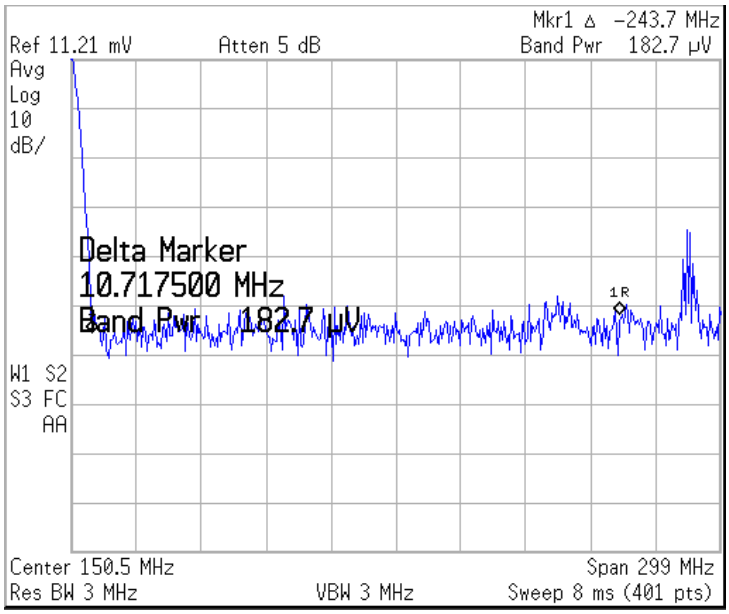


Fig. 5.27 The output noise for the filter

TABLE 5.3 The comparison of the proposed filters with other papers

Reference	[34]JSSC 2003	[35]TCAS-I 2006	The filter with negative feedback	The filter with constant V_{ds}
Technology	0.5u CMOS	0.35u CMOS	0.18u CMOS	0.18u CMOS
Supply Voltage	3.3	3.3	1.8	1.8
Filter Order	4	4	4	4
-3dB Frequency	100MHz	550MHz	250	250
HD3/IM3	-40dB	-40dB	-39.68dB	-40.48dB
Output noise level/density	$700uV_{rms}$	-147dBm/Hz	251.9uV (10MHz~250MHz)	182.7uV (10MHz~250MHz)
Power Consumption	86mW	140mW	42mW	42mW

Chapter 6

Conclusions

6.1 Conclusions

Since the transconductance-C filters are more suitable than switch capacitor filters in high frequency application, they are usually used in high frequency applications. However, their mainly poor are linearity, so linearity improvement techniques are required. In this thesis, there are two transconductance-C filters are proposed to apply in high frequency applications such as ultra wideband and hard-disk driver.

Source degeneration circuit must use large value of resistor to improve linearity. Also, the current feedback works well at high frequency than voltage feedback due to the former has larger bandwidth. Hence, the proposed circuit adds negative current feedback to improve the linearity, which can achieve the requirement without large resistor. Another circuit modifying the constant drain-source voltage of input pair is proposed, which is more suitable in the lower power supply and high frequency applications. In this circuit, the common mode feedforward circuit is introduced to increase the common mode rejection ratio.

Finally, 4^{th} order linear phase filter by cascading two biquad sections is expressed. In the next, the simulation results and the measurement results for the

transconductors and filters are shown in the chapter 5.

6.1 Future Research

Some suggestions for the future work are given as follows. The cutoff frequency of the filter could be at 60MHz~100MHz. It has high priority over the linearity enhancement. Additionally, the tuning range should be improved, as well.

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