# 國 立 交 通 大 學

# 電信工程學系

# 碩 士 論 文

## 應用數位錯誤截取之混合式
## 三角積分調變器

## Hybrid Sigma-Delta Modulator with
## Digital Error Truncation

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中 華 民 國 九十七 年 九 月

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電 信 工 程 學 系 碩 士 班

碩 士 論 文

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## 摘要

三角積分類比數位轉換器傳統地被使用在低訊號頻帶和高解析度的儀器、聲音和音頻訊號的應用上。在最近幾年，已經有著成長趨勢在發展類比數位轉換器向系統的前端。由於超大型積體電路技術在尺寸上的縮減，高效能的數位系統能被實現。類比數位轉換器必須在類比和數位資料的介面提供更高的動態範圍。因此，能完成用在寬輸入頻帶的無線和有線通訊系統上的高解析度三角積分類比數位轉換器變成愈來愈重要。

在這論文裡，連續時間調變器的設計流程將被呈現，並且一個應用於藍芽技術之100MHz取樣頻率和1MHz訊號頻帶的運算放大器連續時間三角積分類比數位轉換器被實現。此設計被製造於台積電 0.18 微米互補式金氧半導體製程。量測的訊號失真雜訊比為 56.8dB 而動態輸入範圍為 60dB。功率消耗在 1.8V 電源供給下為 22.2 毫瓦。

另一個三角積分設計是去結合連續和離散時間調變器的優點。它是應用數位錯誤截取之混合式三角積分調變器。此設計製造於台積電 0.13 微米互補式金氧半導體製程。模擬結果在 62.5MHz 取樣頻率和 2MHz 訊號頻帶下，訊號失真雜訊比為 60.6dB。這樣規格的調變器可以應用在無線通訊系統 WCDMA 上。功率消耗在 1.2V 電源供給下為 12.17 毫瓦。

# Hybrid Sigma-Delta Modulator with Digital Error Truncation

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## Abstract

Sigma-delta analog-to-digital converters (ADCs) are traditionally used in instrumentation, voice, and audio applications that require low signal bandwidth and high resolution. In recent years, there has been a growing trend to move ADC towards the system front-end. Due to the scaling in VLSI technology, high performance digital systems can be realized. The ADC has to provide a higher dynamic range for the interface between analog and digital data. Therefore, sigma-delta ADCs which can achieve high resolution with wide input bandwidth for wireless and wireline communication systems becomes more and more important.

In this thesis, the design flow of the continuous-time (CT) modulator is presented and a 100MHz CT single-bit active-RC sigma-delta modulator with 1MHz signal bandwidth for Bluetooth application is implemented. The design has been fabricated by TSMC 0.18μm CMOS process. The measured SNDR is 56.8dB and the dynamic range is about 60dB. The power consumption is about 22.2mW at 1.8V supply.

The other sigma-delta design is to combine the advantages of the CT and discrete-time (DT) modulators. It is a hybrid sigma-delta modulator with digital error truncation. The work is designed in TSMC 0.13μm CMOS process. The simulation result shows 60.6dB SNDR for 62.5MHz sampling frequency and 2MHz signal bandwidth. With such specification, the modulator can be applied to WCDMA wireless communication system. The power consumption is about 12.17mW at 1.2V supply.

# 誌謝

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楊文霖 于 交通大學工程四館 718 實驗室

2008.8.20

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# *Introduction*

## *1.1 Motivation*

Sigma-delta analog-to-digital converter (ADC) is traditionally used in instrumentation, voice, and audio applications that are low signal bandwidth and high resolution. In recent years, there has been a growing trend to move ADC towards the system front-end. This implies that more signal processing is shifted from analog domain to digital domain. Due to the scaling in VLSI technology, high performance digital systems can be realized. However, ADC has to provide higher dynamic range in the interface between analog and digital data. Therefore, sigma-delta ADC which can achieve high resolution with wide input bandwidth for wireless and wireline communication systems becomes more and more important [1] [2].

In sigma-delta ADC, the use of continuous-time (CT) loop filter provides several advantages over discrete-time (DT) implementations. Without critical slewing and settling issues, as in switched-capacitor circuits, CT integrators are often promised to achieve better power-performance efficiency [3]. Moreover, CT integrators are praised for better noise immunity due to their inherent anti-aliasing filtering which are especially advantageous in RF receivers [4]. However, CT integrators are sensitive to process variation thereby require extra tuning circuit to adjust the time constant. DT integrators, on the contrary, set the pole-zero locations by capacitor ratios, which are highly accurate. Another advantage of using DT loop filter is that its signal transfer function and noise transfer function scale with the clock frequency which could be

handy for a multi-standard system design. Alternative hybrid CT/DT loop filter approach tends to exploit the performance by keeping all the pros.

In this thesis, a CT single-bit active-RC sigma-delta modulator for Bluetooth application and a hybrid sigma-delta modulator with 60.6dB SNDR and 2MHz signal bandwidth are achieved. Various design techniques which are truncation error shaping, cancellation and switched-capacitor with resistive element (SCR) feedback are utilized to have better performance. The modulators with such specifications can be applied to Bluetooth and WCDMA wireless communication systems.

## *1.2 Thesis Organization*

This thesis is organized into seven chapters.

Chapter 1 briefly introduces the motivation of the thesis.

Chapter2 first explains the performance parameters of the sigma-delta A/D and describes the background of the sigma-delta A/D conversion. Then, the concepts and advantages of quantization, oversampling and noise shaping are introduced. Finally, the common architectures of the sigma-delta modulator, single-loop and multi-stage, are illustrated and discussed.

Chapter 3 introduces the comparison of the CT and DT loop filter. Then, how to transform between the DT and the CT loop filter is described and the non-idealities of the CT modulator are explained.

Chapter 4 presents a continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application. The design of the loop is illustrated, including the architecture and coefficients. The system and circuit level designs are introduced in detail. Non-idealities and important simulation results are included. Finally, in mixed-signal design, the considerations of the layout are discussed.

Chapter 5 presents the design of the hybrid sigma-delta modulator with digital error truncation. First, the principles of the truncation error shaping, cancellation and SCR feedback are introduced. The design considerations including non-idealities are analyzed in system level in order to implement a power- and area-efficient modulator in circuit level. Finally, the simulation results and layout design are presented.

Chapter 6 presents the testing environment, including the components on the printed circuit board (PCB) and instruments. The measurement results of the continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application is shown and summarized.

Finally, the conclusions and the future works of this thesis are summarized in Chapter 7.

# *CHAPTER 2*
# *Basic Understanding of Sigma-Delta A/D Conversion*

In this chapter, first, the performance parameters of the sigma-delta A/D are explained. Then we describe the background of the sigma-delta A/D conversion and introduce the concepts of quantization, oversampling and noise shaping. Finally, the common architectures of the sigma-delta modulator, single-loop and multi-stage, are illustrated and discussed.

## *2.1 Performance Parameters*

There are commonly the most important performance parameters when sigma-delta A/D is compared. These performance parameters are described as follows:

### *2.1.1 Signal-to-Noise Ratio (SNR)*

The signal-to-noise ratio of an A/D is the ratio of the signal power to the noise power over the interest band at the output of a converter. The theoretical value of SNR for sinusoidal inputs in a Nyquist rate A/D is given by

$$SNR_{max} = 6.02N + 1.76 \tag{2.1}$$

The derivation of the equation (2.1) is described in section 2.3.

### 2.1.2 Signal-to-Noise and Distortion Ratio (SNDR)

The signal-to-noise and distortion ratio of an A/D is the ratio of the signal power to the noise and all distortion power over the interest band at the output of a converter. In general, the SNDR is lower than SNR due to the distortion power.

### 2.1.3 Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is defined as the ratio of the signal power to the maximum distortion component in the range of interest, as shown in Fig. 2.1.

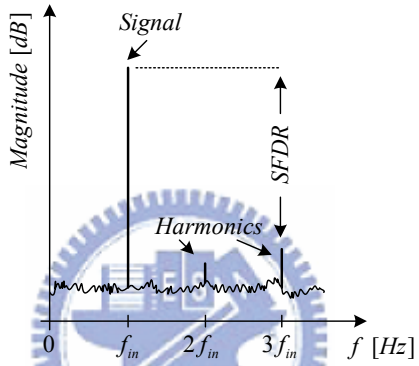



Fig. 2.1 Performance of the SFDR

### 2.1.4 Dynamic Range (DR)

The dynamic range of an A/D for sinusoidal inputs is defined as the ratio of the maximum signal power to the signal power for a small input which the SNR is unity [5].

### 2.1.5 Effective Number of Bits (ENOB)

Equation (2.2) relates the number of bits to the SNDR used in an A/D when the input signal is a sinusoidal.

$$ENOB = \frac{SNDR - 1.76}{6.02} bits \tag{2.2}$$

### 2.1.6 Overload Level (OL)

Overload level is defined as the maximum input sinusoidal signal which the structure still operates correctly. Usually, the maximum stable amplitude is at the 6dB reduction of the peak SNR.

The performance parameters discussed above are summarized in Fig. 2.2, where $SNR_p$ and $SNDR_p$ are the peak SNR and the peak SNDR, respectively [6].

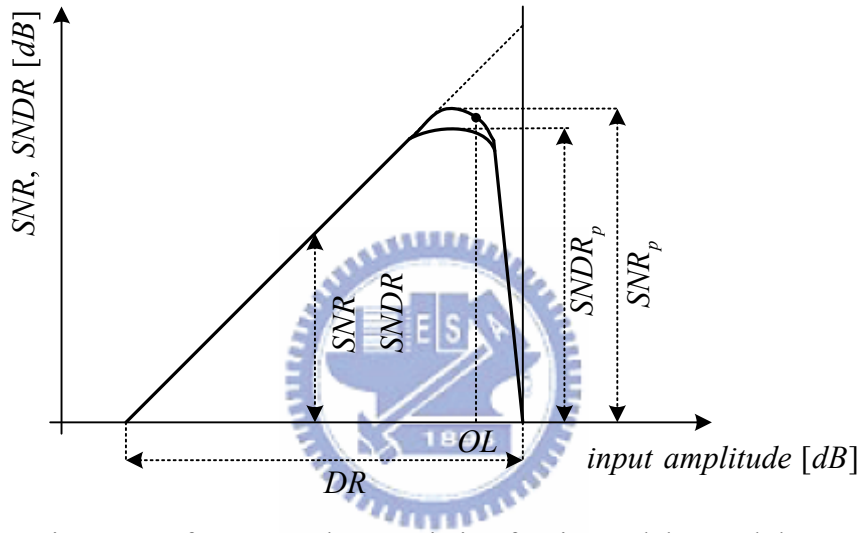



Fig. 2.2 Performance characteristic of a sigma-delta modulator

## 2.2 Sampling and Quantization

The conversion of analog signals to digital domain can simply be separated into two basic operations: sampling in time and quantization in amplitude.

Sample at the time $T_s$, or with a fixed frequency $f_s$, results in a periodicity of the original signal spectrum at multiples of $f_s$, as shown in Fig. 2.3. From Fig. 2.3, the original spectrum can be reconstructed by a simple low pass filter but the criterion known as Nyquist theorem

$$f_s \geq 2f_B \tag{2.3}$$

must be satisfied, where $f_B$ is the signals of interest. Otherwise, the aliasing maybe occur, as shown in Fig. 2.4. In order to assure the condition in (2.3), an analog lowpass filter must be used to limit the signal bandwidth, called anti-aliasing filter. The ideal lowpass filter characteristic is called a brick wall response. However, in real implementations, the characteristic is impossibly to realize. On the contrary, the filter having n-pole roll-off in the transition band is easier to design and more inexpensive. We define the oversampling ratio (OSR) as

$$OSR = \frac{f_s}{2f_B} \tag{2.4}$$

It means that how much faster we sample in the oversampling converters than in a Nyquist rate converters. With higher OSR, the transition band of the anti-aliasing can be relaxed.

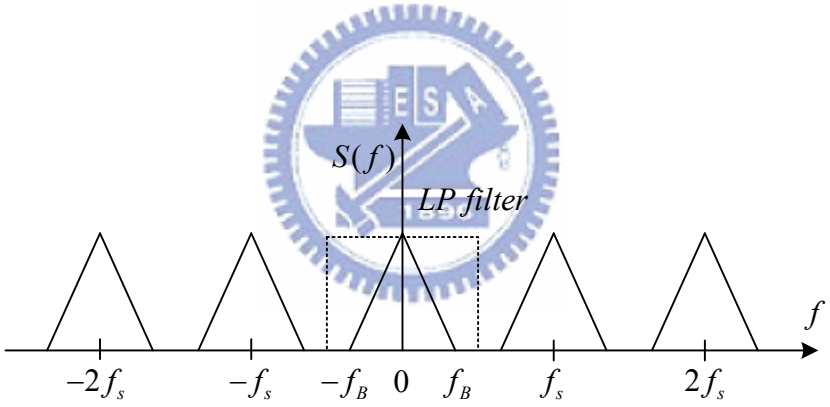



Fig. 2.3 Spectral of the sampling operation

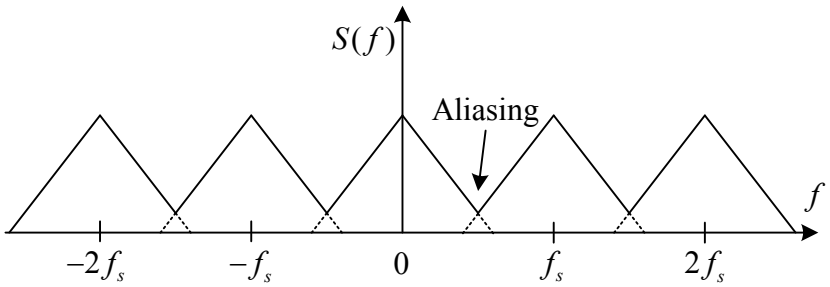



Fig. 2.4 Aliasing phenomenon

The process of quantization in amplitude encodes a continuous range of analog values into a set of discrete levels. The device which realizes the quantization is called a quantizer or ideal A/D converter. There are two types of the quantizers which are mid-rise and mid-tread [7], as shown in Figs. 2.5 and 2.6. In Fig. 2.5 (a), the mid-rise quantizer has $u = 0$ in a rise of $v$. On the other hand, $u = 0$ occurs in the middle of a flat portion of the curve and hence it is called a mid-tread quantizer. In ideal both cases, the straight line $v = ku$ is the desirable A/D transfer curve, where the gain $k$ of the quantizer is determined by the ratio of the step size to the adjacent input thresholds known as the least-significant bit size (LSB size or $\Delta$). The deviation between the straight line $v = ku$ and the real A/D characteristic is called quantization error or quantization noise. Figs. 2.5 (b) and 2.6 (b) illustrate the quantization error $e$. In the range from $-M-1$ to $M+1$, the quantization error is within $\pm\Delta/2$. This range is called no-overload input range and the difference between lowest and highest levels is named full scale (FS). Therefore, the FS is equal to

$$FS = \Delta \cdot 2^N \tag{2.5}$$

where $N$ is quantizer resolution. Table 2.1 summarizes the quantizers of the Figs 2.5 and 2.6.

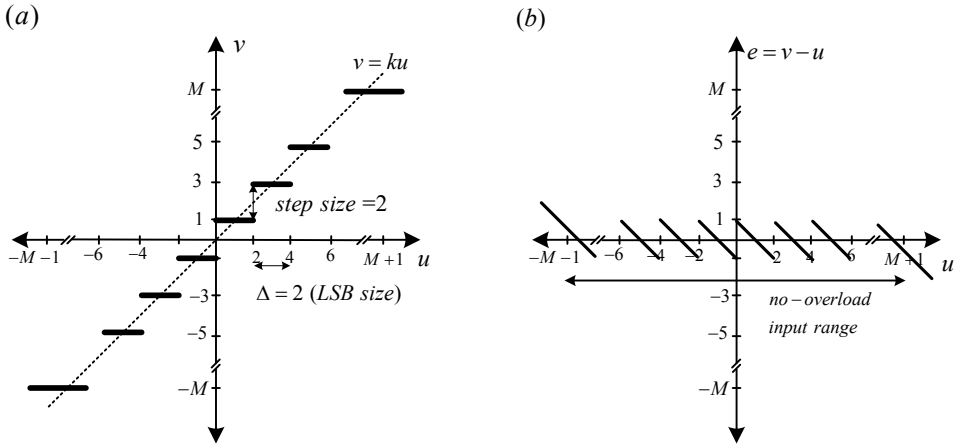



Fig. 2.5 M-step mid-rise quantizer (M is odd) (a) transfer curve (b) error function

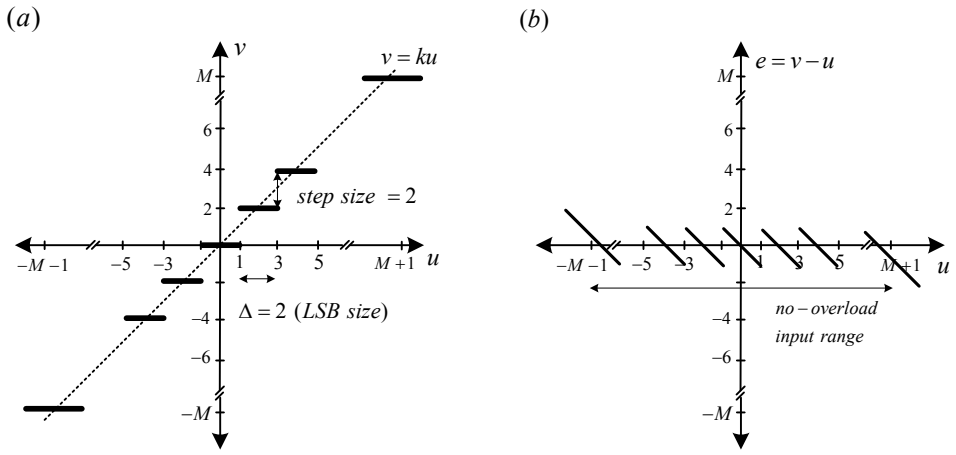



Fig. 2.6 M-step mid-tread quantizer (M is even) (a) transfer curve (b) error function

Table 2.1 Properties of quantizers in Figs 2.5 and 2.6

| Parameter | Value |
|---|---|
| input step size (LSB size) | 2 |
| output step size | 2 |
| number of steps | M |
| number of levels | M+1 |
| number of bits | $[\log_2(M+1)]$ |
| no-overload input range | [-(M+1), M+1] |
| full-scale | 2M |
| input thresholds | 0, ±2, ….., ±(M-1), M odd<br>±1, ±3, ….., ±(M-1), M enen |
| output levels | ±1, ±3, ….., ±M-, M odd<br>0, ±2, ±4….., ±M, M enen |

The basic A/D structure is shown in Fig. 2.7.

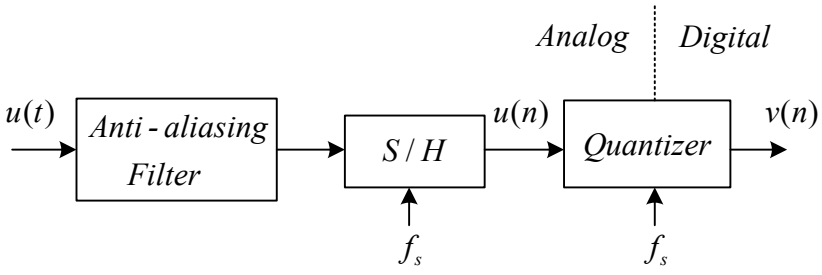



Fig. 2.7 Basic A/D structure

## 2.3 White Noise

The quantizer can be modeled linearly as adding quantization error $e(n)$ in Fig. 2.8. If we assume that the input signal changes rapidly from sample to sample and the quantization error is independent of it, then the quantization error has equal probability density function (pdf) in the no-overload input range, as shown in Fig. 2.9 (a). The probability density function is

$$f_Q(e) = \begin{cases} \frac{1}{\Delta}, & \frac{-\Delta}{2} \le e(n) \le \frac{\Delta}{2} \\ 0, & otherwise \end{cases} \tag{2.6}$$

Therefore, it is possible to assume the quantization error to have statistical properties. A common assumption is that the quantization error has the following properties, usually referred to as the input-independent additive white noise approximation [8]:

Property 1 : $e(n)$ is statistically independent of the input signal or $e(n)$ is uncorrelated with the input signal.

Property 2 : $e(n)$ is uniformly distributed in the no-overload input range.

Property 3 : $e(n)$ is an independent identically distributed sequence or $e(n)$ has a flat power spectral density (PSD).

This assumption simplifies the analysis of an ADC system because a non-linear system is replaced by a linear one.

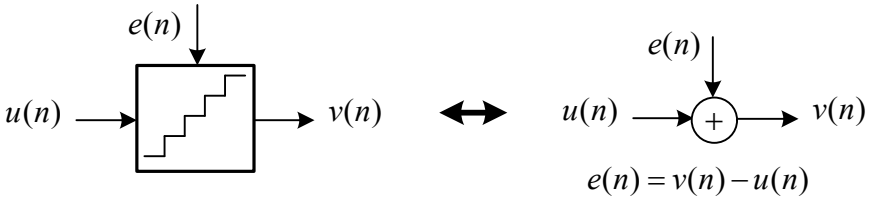



Fig. 2.8 A quantizer and its linear quantizer model

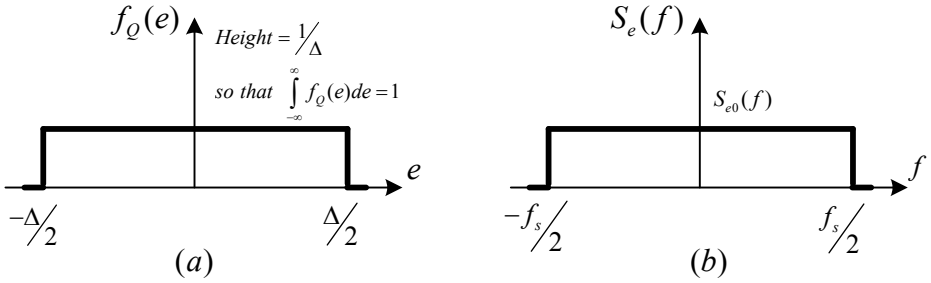



Fig. 2.9 (a) Probability density function (b) Power spectral density of quantization noise

From Fig. 2.9 (a), we can calculate the total quantization noise power as:

$$\sigma_e^2 = \int_{-\infty}^{\infty} e^2 f_Q(e)de = \frac{\Delta^2}{12} \tag{2.7}$$

In (2.7), the quantization noise power is only related to the quantizer resolution and is independent of sampling frequency. In Fig. 2.9 (b), the power spectral density of the quantization noise is

$$S_e(f) = \frac{\Delta^2}{12}\frac{1}{f_s} \tag{2.8}$$

Assuming the input signal is a sinusoidal wave and using (2.5), its maximum amplitude $A$ without clipping is $2^N(\Delta/2)$. For this assumption, the signal power is

$$P_s = \left(\frac{2^N\Delta}{2\sqrt{2}}\right)^2 = \frac{2^{2N}\Delta^2}{8} \tag{2.9}$$

Using (2.7) and (2.9), the SNR in Nyquist rate converters, which is the ratio of the signal power to the total quantization noise power, is calculated as follows:

$$SNR_{max} = 10\log\left(\frac{P_s}{\sigma_e^2}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) = 6.02N + 1.76 \tag{2.10}$$

## 2.4 Oversampling

In (2.4), we have defined OSR. It represents how much faster the oversampling converters operate than the Nyquist rate converters. Oversampling can relax the requirement of the anti-aliasing filter, as shown in Fig. 2.10. In Fig 2.10, the transition band of the lowpass filter with oversampling is wider than without oversampling. The characteristic gives a favor in the design of anti-aliasing filter. Therefore, we don't need a brick wall lowpass response. Instead of it, the filter having n-pole roll-off in the transition band is easier to design and more inexpensive.

From Fig. 2.10, due to the oversampling technique, the inband quantization noise is reduced. Consequently, the inband quantization noise power becomes

$$P_e = \frac{1}{f_s}\int_{-f_B}^{f_B} \sigma_e^2 df = \frac{\Delta^2}{12}\frac{2f_B}{f_s} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.11}$$

Using (2.9) and (2.11), the SNR of a oversampling converters is as follows:

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log(OSR) \\ &= 6.02N + 1.76 + 10\log(OSR) \end{aligned} \tag{2.12}$$

Compared to (2.10), the SNR is enhanced by 3dB with doubling OSR. Therefore, the oversampling gives a SNR improvement with the OSR at a rate of 3dB/octave, or 0.5bit/octave.

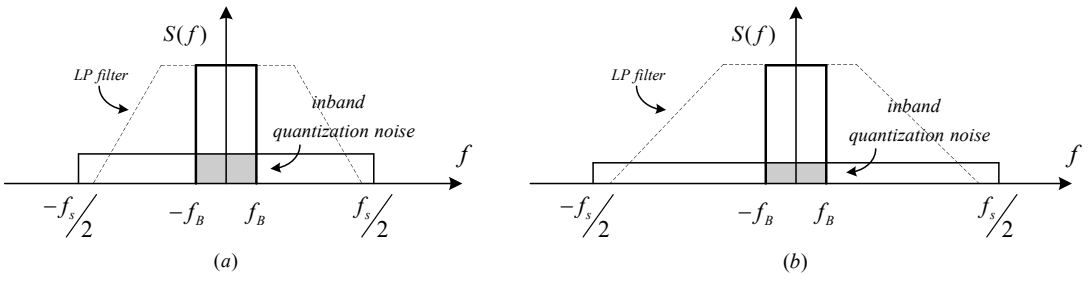



Fig. 2.10 Power spectral density (a) without oversampling (b) with oversampling

## 2.5 Noise shaping strategy

The advantage of quantization noise shaping through the use of the feedback path is introduced in this section. With an additional feedback path, the different transfer functions can be obtained which are signal transfer function (STF) and noise transfer function (NTF).

A general noise shaping sigma-delta modulator (SDM) is shown in Fig. 2.11 (a), where $H(z)$ is loop filter. Assuming the input signal and the quantization noise are independent signals discussed in section 2.3 and using 1-bit quantizer to simplify the analysis. The linear model of the modulator in z domain is shown in Fig. 2.11 (b). With this linear model, we can derive a STF and a NTF as defined

$$STF(z) \equiv \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} \tag{2.13}$$

$$NTF(z) \equiv \frac{V(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.14}$$

According to (2.14), we can find out that the zeros of $NTF(z)$ is equal to the poles of $H(z)$. It means that when $H(z)$ go to infinity, $NTF(z)$ will be zero. In other words, by choosing $H(z)$ such that its magnitude is large in signal bandwidth, $STF(z)$ should approximate unity and $NTF(z)$ should be close zero over the same bandwidth. For the output signal, we can express it in linear combination of the input signal and the noise signal in (2.15), which are filtered by STF and NTF, respectively.

$$V(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.15}$$

In general cases, the $STF(z)$ has all-pass or lowpass frequency response and the $NTF(z)$ has highpass characteristic. Based on (2.15), the inband quantization noise can be shaped to high frequency band and then it doesn't affect the input signal [9]. Therefore, the SNR can be improved effectively by using noise shaping.

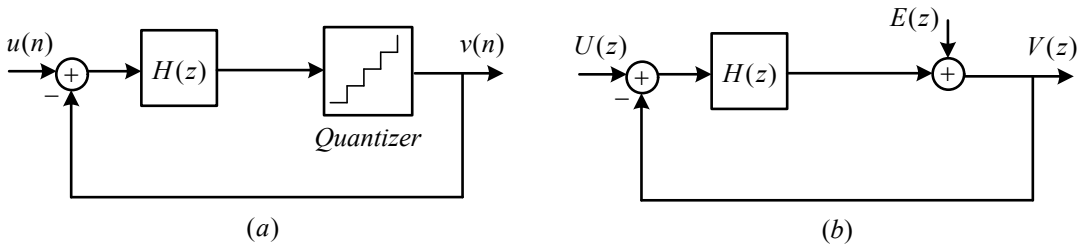



Fig. 2.11 (a) A general sigma-delta modulator (b) Its linear model in z domain

### 2.5.1 First-Order Sigma-Delta Modulator

From above discussion, for a first-order noise shaping, the $NTF(z)$ should have a zero at dc (i.e., z=1), that is a lowpass frequency response, equivalently $H(z)$ has a pole at dc. So the quantization noise has highpass characteristic. By letting $H(z)$ be a discrete-time integrator, the function is

$$H(z) = \frac{1}{z-1} \tag{2.16}$$

where $H(z)$ has a pole at dc (i.e., z=1). For this choice, the block diagram in z domain is shown in Fig. 2.12. In frequency domain, the $STF(z)$ is given by

$$STF(z) \equiv \frac{V(z)}{U(z)} = \frac{\frac{1}{z-1}}{1+\frac{1}{z-1}} = z^{-1} \tag{2.17}$$

and the $NTF(z)$ is given by

$$NTF(z) \equiv \frac{V(z)}{E(z)} = \frac{1}{1+\frac{1}{z-1}} = 1-z^{-1} \tag{2.18}$$

According to (2.15), the output signal becomes

$$V(z) = z^{-1} \cdot U(z) + (1-z^{-1}) \cdot E(z) \tag{2.19}$$

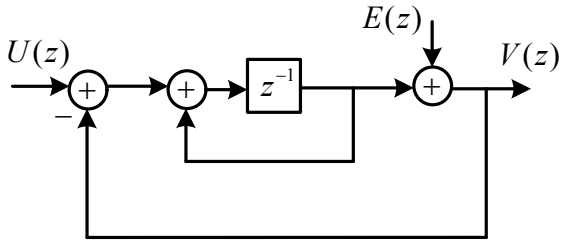



Fig. 2.12 A first-order lowpass sigma-delta modulator

From (2.19), the $STF(z)$ is just a delay while the $NTF(z)$ is a discrete-time differentiator (i.e., a highpass filter). To estimate the inband quantization noise power, the squared magnitude of the $NTF(z)$ needs to be found in frequency domain. By setting $z = e^{j2\pi f/f_s}$, the $NTF(f)$ becomes as follows:

$$\begin{aligned} NTF(f) &= 1 - e^{-j2\pi f/f_s} = \frac{e^{j\pi f/f_s} - e^{-j\pi f/f_s}}{2j} \times 2j \times e^{-j\pi f/f_s} \\ &= \sin(\frac{\pi f}{f_s}) \times 2j \times e^{-j\pi f/f_s} \end{aligned} \tag{2.20}$$

Therefore, the squared magnitude of the $NTF(f)$ is given by

$$\left|NTF(f)\right|^2 = \left[2\sin(\frac{\pi f}{f_s})\right]^2 \tag{2.21}$$

Using (2.8) and (2.21), the inband quantization noise power is

$$P_e = \int_{-f_B}^{f_B} S_e(f)\left|NTF(f)\right|^2 df = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\sin\left(\frac{\pi f}{f_s}\right)\right]^2 df \tag{2.22}$$

For frequencies which satisfy $f_B \ll f_s$ (i.e., OSR>>1), $\left|NTF(f)\right|^2 \approx (2\pi f/f_s)^2$. By this approximation, we have [9]

$$P_e = \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_s}\left[2\left(\frac{\pi f}{f_s}\right)\right]^2 df = \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_s}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.23}$$

According to (2.9), the SNR for this case is given by

$$SNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right] \qquad (2.24)$$
$$= 6.02N + 1.76 - 5.17 + 30\log(OSR)$$

With doubling OSR, the SNR performance is improved by 9dB, i.e., 1.5bit/octave. Compared to (2.12), the SNR has the improvement of 1bit/octave.

### 2.5.2 Second-Order Sigma-Delta Modulator

To realize a second-order sigma-delta modulator, the $NTF(z)$ should be a second-order highpass function. The block diagram of the modulator is shown in Fig. 2.13. For this modulator, the $STF(z)$ is given by

$$STF(z) = z^{-1} \qquad (2.25)$$

and the $NTF(z)$ is given by

$$NTF(z) = \left(1 - z^{-1}\right)^2 \qquad (2.26)$$

Similarly, we are interested in the squared magnitude of the $NTF(z)$. It is

$$\left|NTF(f)\right|^2 = \left[2\sin(\frac{\pi f}{f_s})\right]^4 \qquad (2.27)$$

Using the same assumption OSR>>1, the quantization noise power over the frequency band of interest becomes

$$P_e = \int_{-f_B}^{f_B} S_e(f)\left|NTF(f)\right|^2 df = \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{2f_B}{f_s}\right)^5 = \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5 \qquad (2.28)$$

Again, according to (2.9), the SNR for this case is given by

$$SNR_{max} = 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right] \qquad (2.29)$$
$$= 6.02N + 1.76 - 12.9 + 50\log(OSR)$$

With doubling OSR, the SNR performance is improved by 15dB, i.e., 2.5bit/octave. Comparison with different noise shaping transfer functions which are zero-, first- and second-order is shown in Fig. 2.14. In signal bandwidth $f_B$, we can see that the quantization noise power decreases as the noise shaping order increases, as discussed above.

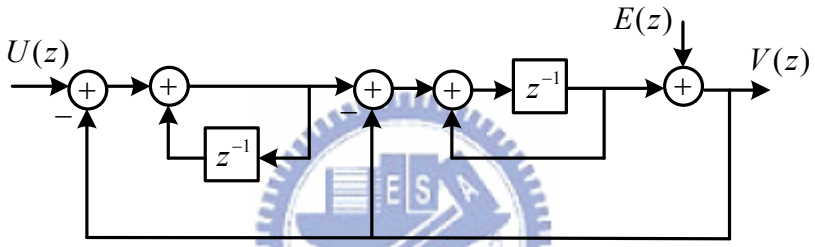



Fig. 2.13 A second-order lowpass sigma-delta modulator

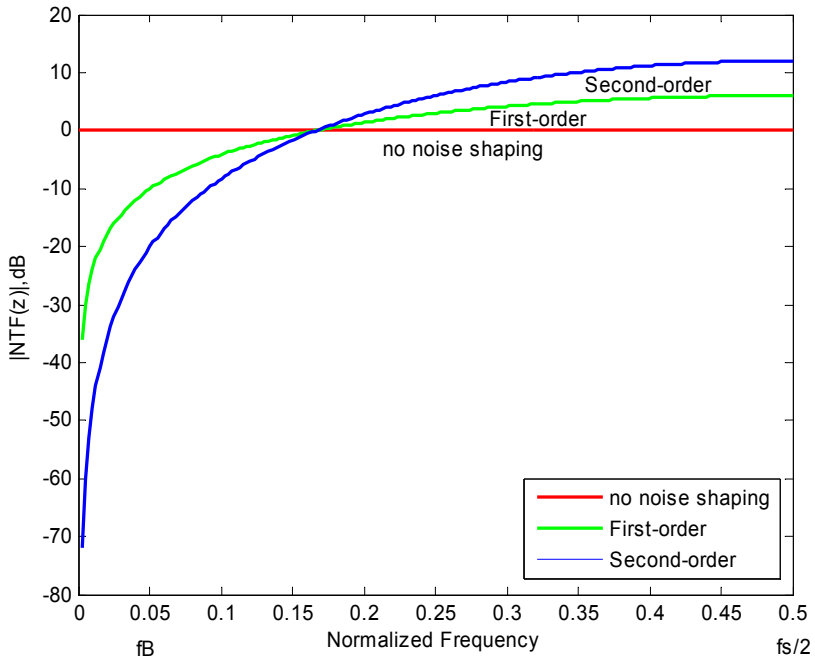



Fig. 2.14 Comparison with different noise shaping transfer functions

### 2.5.3 Higher-Order Sigma-Delta Modulators

Fig. 2.18 shows the block diagram of the L-order sigma-delta modulator. As the first- and second-order SDM, the $NTF(z)$ of the L-order SDM should be chosen to have an L-order highpass function. This gives

$$NTF(z) = (1 - z^{-1})^L \tag{2.30}$$

In the same manner and assumption, we can find out the inband quantization noise power is

$$P_e \approx \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{2f_B}{f_s}\right)^{2L+1} = \frac{\Delta^2\pi^{2L}}{12(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1} \tag{2.31}$$

Therefore, the maximum SNR for this case is given by

$$\begin{aligned} SNR_{max} &= 10\log\left(\frac{P_s}{P_e}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{2L+1}{\pi^{2L}}(OSR)^{2L+1}\right] \\ &= 6.02N + 1.76 - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) + (20L+10)\log(OSR) \end{aligned} \tag{2.32}$$

From (2.32), the SNR performance can be improved by (6L+3) dB with doubling OSR, or at a rate of (L+0.5) bit/octave. However, higher than second-order SDM suffers from potential instability due to the accumulation of large signals in the integrators. Consequently, stability problems reduce the achievable resolution to a lower value than the equation (2.32).

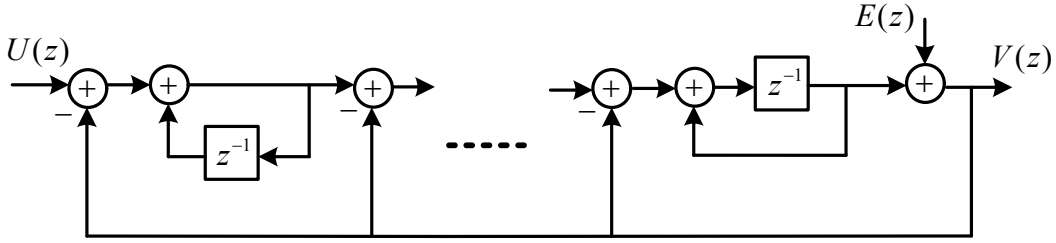



Fig. 2.15 A higher-order lowpass sigma-delta modulator

### 2.5.4 Multi-Stage Modulators

Another realization of the higher order SDM is the cascade modulator, also called the multi-stage or MASH (Multi-stAge noise-SHaping) modulator. The MASH modulator is constructed from lower order SDMs. Therefore, it can ease the stability problems. The basic second-order block diagram is illustrated in Fig. 2.16. The output signal of the first stage is given by

$$V_1(z) = STF_1(z)U(z) + NTF_1(z)E_1(z) = z^{-1}U(z) + (1-z^{-1})E_1(z) \qquad (2.33)$$

where $STF_1(z)$ and $NTF_1(z)$ are signal transfer function and noise transfer function of the first stage, respectively. From Fig. 2.16, the input signal of the second stage is the quantization noise of the first stage $E_1(z)$. Therefore, the output signal of the second stage is given by

$$V_2(z) = STF_2(z)E_1(z) + NTF_2(z)E_2(z) = z^{-1}E_1(z) + (1-z^{-1})E_2(z) \qquad (2.34)$$

where $STF_2(z)$ and $NTF_2(z)$ are signal transfer function and noise transfer function of the second stage, respectively. The digital filter $H_1(z)$ and $H_2(z)$ are designed to cancel the quantization noise $E_1(z)$ of the first stage in the overall output $V(z)$. By using (2.33) and (2.34), the condition is

$$(1-z^{-1})H_1(z) - z^{-1}H_2(z) = 0 \qquad (2.35)$$

The simplest choices for $H_1(z)$ and $H_2(z)$ are $H_1(z) = z^{-1}$ and $H_2(z) = (1-z^{-1})$. So, the overall output is given by

$$V(z) = z^{-2}U(z) + (1-z^{-2})^2 E_2(z) \qquad (2.36)$$

Therefore, the second-order MASH modulator has second-order noise shaping but the stability behavior is first order one. However, if the condition (2.35) is not satisfied due to the imperfection of the analog and digital transfer functions, the SNR performance is degraded greatly.

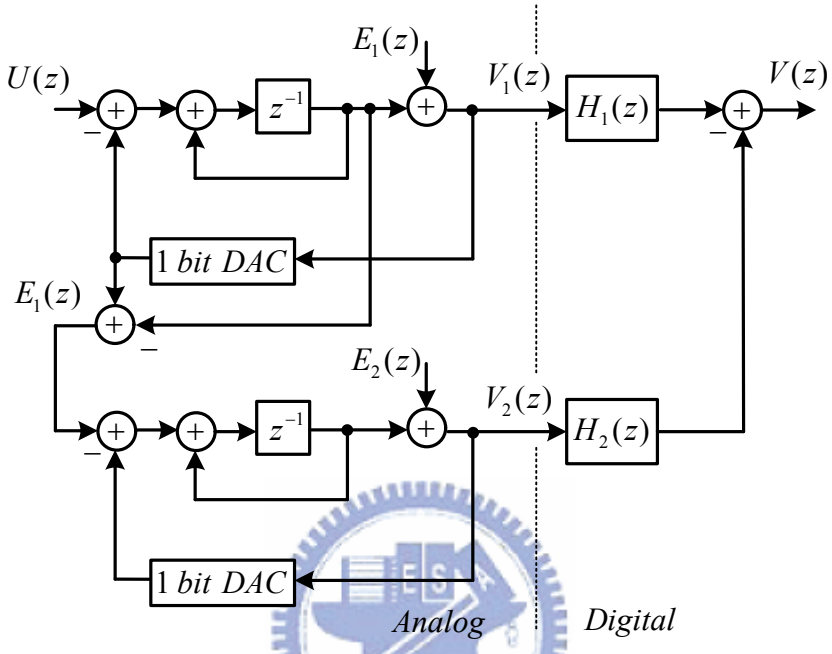



Fig. 2.16 A second-order MASH modulator

## 2.6 Summary

In this chapter, performance parameters of a sigma-delta modulator are first explained. Then, we introduce the basic concept of the SDM and the fundamental principles of how a modulator works are described. Through the use of oversampling and noise shaping, the SNR performance can be improved in the band of interest. Finally, the common architectures of the SDM, single-loop and multi-stage, are illustrated and discussed.

# *CHAPTER 3*

# *Continuous-Time Sigma-Delta Modulators*

## *3.1 Discrete-Time / Continuous-Time Modulators*

Sigma-delta A/D converters are widely used in wireless and wireline communication system. In recent years, continuous-time (CT) sigma-delta A/D gains growing interest in wireless application for their lower power consumption and wider input bandwidth as compared to the discrete-time counterparts. In other words, the opamp of CT SDM can be relaxed at speed requirements or CT SDM can operate at higher sampling frequency. Moreover, CT SDM is praised for better noise immunity due to their inherent anti-aliasing filtering which are especially advantageous in RF receivers [4]. Besides, the absence of the switches makes CT SDM has less glitch and less digital switching noise.

DT SDM, on the contrary, is insensitivity to clock jitter and exact shape of opamp settling waveform as long as full settling occurs. Another advantage of DT SDM is that the integrator gain and transfer functions are accurately defined.

The main advantages of CT and DT SDM are summarized in Table3.1 and their block diagrams are shown in Fig. 3.1 [6] [8].

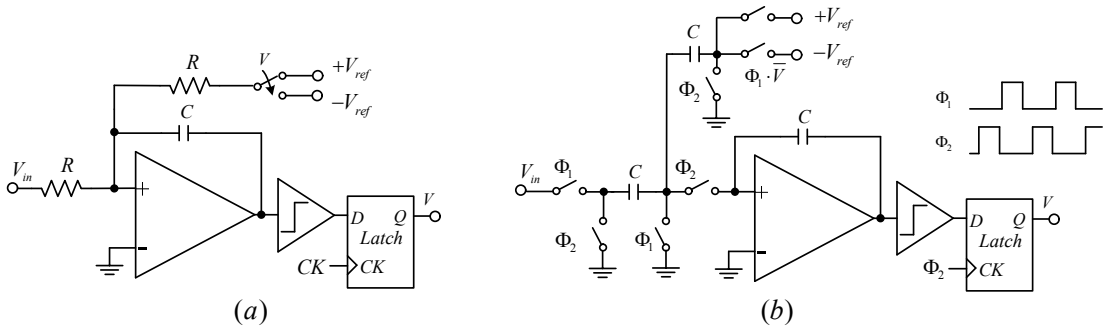



Fig. 3.1 (a) A first order CTSDM (b) A first order DT SDM

Table 3.1 Comparison with the main advantages of CT and DT SDM

| | **Advantages** |
|---|---|
| **CT SDM** | • Inherent anti-aliasing filter<br>• Higher sampling frequency possible<br>• Relaxed opamp speed requirements<br>• Less glitch sensitive<br>• Less digital switching noise<br>• Lower simulation time (circuit level) |
| **DT SDM** | • Accurately defined integrator gains and transfer function by capacitor ratios<br>• Transfer functions scaled with clock frequency<br>• Low sensitivity to clock jitter<br>• Low sensitivity to excess loop delay<br>• Low sensitivity to DAC waveform<br>• Lower simulation time (high level) |

## *3.2 Transformation of a Discrete-Time to a Continuous-Time*

In section 3.1, we have introduced why the CT SDM gains growing interest. Due to the widely used sigma-delta toolbox [7], the DT loop filter can be obtained easily. By contrast, the loop filter design of a CT SDM is nontrivial because it has a strong dependence on the pulse shape of the feedback digital-to-analog converter (DAC). Fortunately, we can find a CT loop filter through the equivalent DT loop filter and transforming it to continuous-time.

Fig. 3.2 shows a CT and a DT SDM, respectively. In DT SDM, the sampling is at the front-end input while it is at the input of the quantizer in CT SDM. If they have the same output sequences in the time domain for the same time instants, they can be considered equivalent. This is shown in Fig. 3.3 (a) and (b) which are open-loop of

the CT and DT SDM. As mentioned above, the criterion for the two equivalent modulators is

$$x(n) = x(t)|_{t=nT_s} \tag{3.1}$$

This can be satisfied if their impulse responses are equal at each sampling instants. This results in the condition [10]

$$Z^{-1}\{H(z)\} = L^{-1}\{H_{DAC}(s)H(s)\}|_{t=nT_s} \tag{3.2}$$

or, in the time domain [11]

$$h(n) = [h_{DAC}(t) * h(t)]|_{t=nT_s} = \int_{-\infty}^{\infty} h_{DAC}(\tau) * h(t-\tau)d\tau\,|_{t=nT_s} \tag{3.3}$$

where $h_{DAC}(t)$ is the impulse response of the DAC. The transformation between CT and DT is called the impulse-invariant transformation. Although forward Euler integration, back Euler integration, bilinear transformation and midpoint integration are known and popular in linear filter designs for transformation between DT filters and CT filters. However, they are not suitable for transforming between DT SDM and CT SDM. The reason is that SDM is essentially a non-linear system. Thus, the impulse-invariant transformation is the most proper method to transform DT modulators to CT modulators.

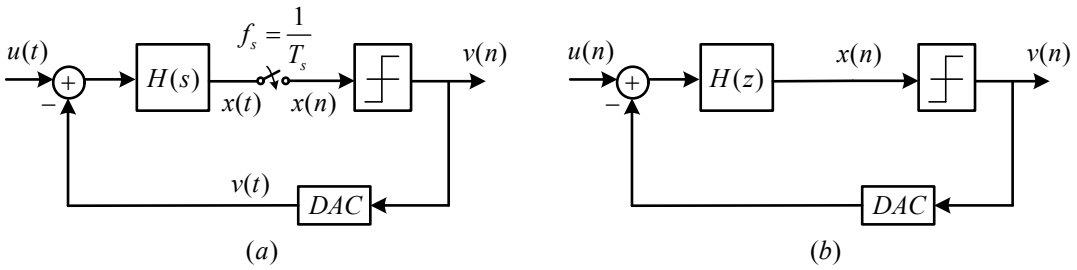



Fig. 3.2 (a) CT (b) DT sigma-delta modulator

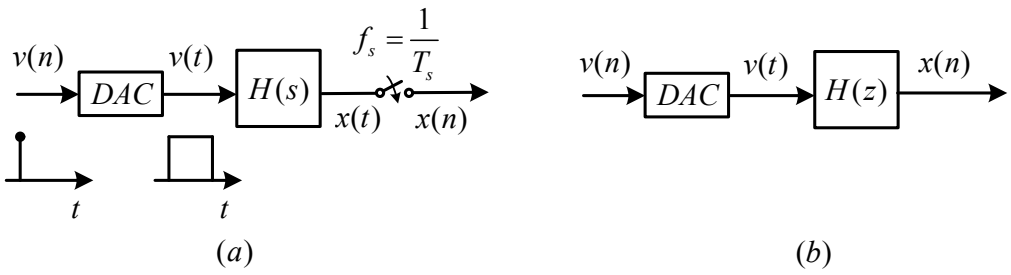



Fig. 3.3 Open-loop (a) CT (b) DT sigma-delta modulator

According to (3.2) and (3.3), different DAC feedback pulse shape results in different transformation between DT modulators and CT modulators. In consequence, before doing this transformation, the pulse shape has to be selected first. There are three commonly used rectangular DAC feedback pulse shapes which are non-return-to-zero (NRZ), return-to-zero (RZ) and half-delay-return-to-zero (HRZ) [12], as shown in Fig. 3.4. For simplicity, the magnitudes of the rectangular DAC pulses are assumed to be 1 and in the time domain, this is given by

$$h_{DAC}(t) = \begin{cases} 1, & \alpha \le t < \beta, \ 0 \le \alpha < \beta \le 1 \\ 0, & otherwise \end{cases} \tag{3.4}$$

where $\alpha$ and $\beta$ are feedback starting and ending times. So, the three rectangular DAC feedback pulses are

$$\begin{cases} NRZ & \alpha = 0, & \beta = 1 \\ RZ & \alpha = 0, & \beta = 0.5 \\ HRZ & \alpha = 0.5, & \beta = 0 \end{cases} \tag{3.5}$$

By the Laplace transform of (3.4), their responses in s-domain can be described as follows

$$H_{DAC}(s) = \frac{\exp(-\alpha s) - \exp(-\beta s)}{s} \tag{3.6}$$

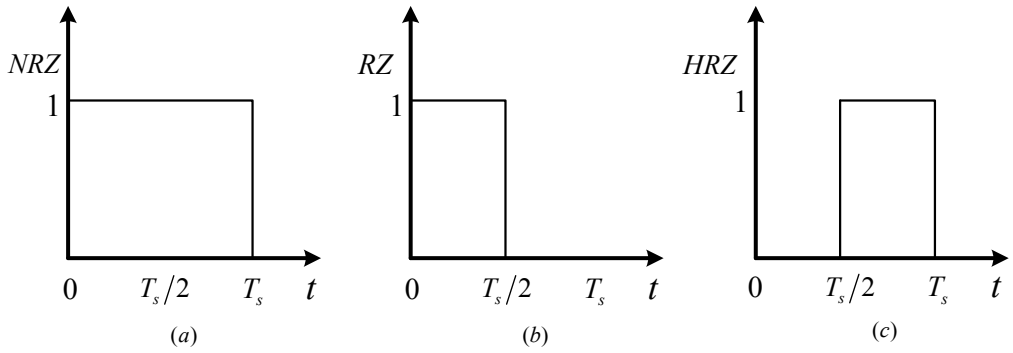



Fig. 3.4 DAC feedback pulse shapes (a) NRZ (b) RZ (c) HRZ

After determining the DAC feedback pulse shape and its response, impulse-invariant transformation can be used in following steps. First, we need to express the $H(z)$ as a partial fraction expansion and then convert each partial fraction expansion from z-domain to s-domain. Finally, the $H(s)$ can be derived by recombining the results.

Table 3.2 lists the results of impulse-invariant transformation between CT loop filters and DT loop filters for the commonly used DAC feedbacks [13].

Table 3.2 S-domain equivalent for z-domain partial expansion

| **z-domain partial fraction** | **s-domain equivalent** | | |
|---|---|---|---|
| $\frac{z^{-1}}{1-z_k z^{-1}}$ | NRZ | General $z_k$ | $\frac{s_k}{z_k-1}\frac{1}{sT_s-s_k}$ |
| | | $z_k=1$ | $\frac{1}{sT_s}$ |
| | RZ | General $z_k$ | $\frac{s_k}{z_k-z_k^{0.5}}\frac{1}{sT_s-s_k}$ |
| | | $z_k=1$ | $\frac{2}{sT_s}$ |
| | HRZ | General $z_k$ | $\frac{s_k}{z_k^{0.5}-1}\frac{1}{sT_s-s_k}$ |
| | | $z_k=1$ | $\frac{2}{sT_s}$ |
| $\frac{z^{-2}}{(1-z_k z^{-1})^2}$ | NRZ | General $z_k$ | $\frac{(-s_k+1-1/z_k)sT_s-s_k^2}{(z_k-1)^2}\frac{1}{(sT_s-s_k)^2}$ |
| | | $z_k=1$ | $\frac{1}{(sT_s)^2}-\frac{0.5}{sT_s}$ |
| | RZ | General $z_k$ | $\frac{\left[(0.5z_k^{-0.5}-1)s_k+1-z_k^{-0.5}\right]sT_s+(0.5z_k^{-0.5}-1)s_k^2}{(z_k-z_k^{0.5})^2}\frac{1}{(sT_s-s_k)^2}$ |
| | | $z_k=1$ | $\frac{-1.5}{sT_s}+\frac{2}{(sT_s)^2}$ |
| | HRZ | General $z_k$ | $\frac{(-0.5z_k^{-0.5}s_k+z_k^{-0.5}-z_k^{-1})sT_s-0.5z_k^{-0.5}s_k^2}{(z_k^{0.5}-1)^2}\frac{1}{(sT_s-s_k)^2}$ |
| | | $z_k=1$ | $\frac{-0.5}{sT_s}+\frac{2}{(sT_s)^2}$ |

## 3.3 Non-idealities of Continuous-Time Modulators

In this section, non-idealities of CT modulators, including opamp in CT integrators, excess loop delay and clock jitter, are explained. These different non-idealities can cause different effects which are performance degradation or even making modulators unstable. Through understanding of these non-idealities and modeling their behaviors in system level simulations, we can analyze and overcome them in circuit level.

### 3.3.1 Opamp in CT Integrators

For a typical active-RC integrator shown in Fig. 3.5, the ideal transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{1}{sRC} \tag{3.7}$$

where R is the input resistor and C is the integration capacitor.

In presence of finite DC gain $A_0$ and by assuming $A_0 >> 1$, the transfer function becomes

$$\frac{V_{out}}{V_{in}} \approx -\frac{1}{sRC + 1/A_0} \tag{3.8}$$

Considering the finite DC gain, gain bandwidth and only the dominant pole of the opamp, the transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} \approx -\frac{1}{s(1+\alpha \cdot f_s/GBW) + \alpha \cdot f_s/A_0} \tag{3.9}$$

where $\alpha$ is the scaling coefficient, $f_s$ is sampling frequency while $GBW$ and $A_0$ represent the gain bandwidth and the DC gain of the opamp, respectively.

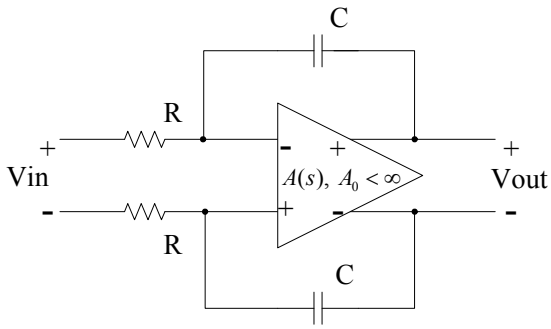



Fig. 3.5 A fully differential integrator with finite gain and bandwidth

Through the equation (3.9), we can analyze the requirement of the opamp in CT integrators in system level and design power-efficient CT modulators in circuit level.

### 3.3.2 Excess Loop Delay

Ideally, the feedback DACs respond immediately to the quantizer clock edge, but in practice, the quantizer of the sigma-delta modulators has non-zero time to generate the correct outputs. The time including quantizer delay and the response time of the feedback DAC is called excess loop delay as illustrated in Fig.3.6 [12].

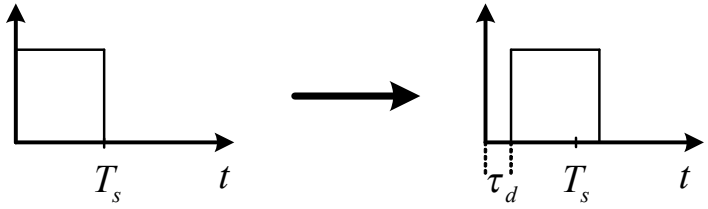



Fig. 3.6 Excess loop delay for NRZ DAC pulse

The excess loop delay can cause the deviation of the transfer function or even the modulator unstable. For example, supposing a second-order CT modulator has the transfer function:

$$H(s) = -\frac{1+1.5s}{s^2} \tag{3.10}$$

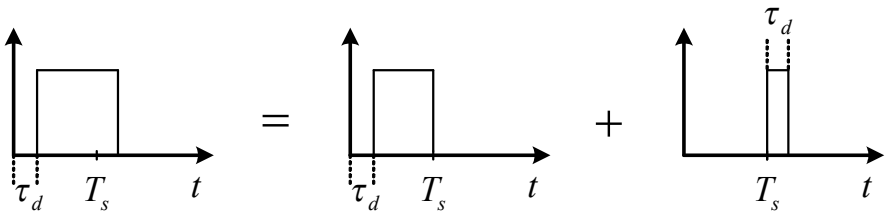



Fig. 3.7 Delayed NRZ pulse as a linear combination

We select the NRZ feedback DAC pulse and assume that the excess loop delay is $\tau_d$ as shown in Fig 3.6. It is possible to write the delayed NRZ pulse as a linear combination as shown in Fig. 3.7.

$$h_{(\tau_d,1+\tau_d)}(t) = h_{(\tau_d,1)}(t) + h_{(0,\tau_d)}(t-1) \tag{3.11}$$

By using impulse-invariant transformation to transform CT loop filter to DT loop filter, the DT transfer function is

$$H(z,\tau_d) = \frac{(-2+2.5\tau_d-0.5\tau_d^2)z^2+(1-4\tau_d+\tau_d^2)+(1.5\tau_d-0.5\tau_d^2)}{z(z-1)^2} \tag{3.12}$$

Letting $\tau_d = 0$, the transfer function becomes

$$H(z) = \frac{-2z+1}{(z-1)^2} \tag{3.13}$$

as it should. If we design $\tau_d = T_s$ on purpose, the result is

$$H(z) = z^{-1}\cdot\frac{-2z+1}{(z-1)^2} \tag{3.14}$$

It is just a delayed version of (3.13). Therefore, the block diagram of the modulator can be shown in Fig. 3.8. However, due to the full clock delay, the design results in that the impulse response is zero at the first sampling instant $T_s$. To compensate the response, an extra feedback branch is added directly to the front of the quantizer as shown in Fig. 3.9. Because the extra branch includes no integrators, the loop is called

by zero-order loop. Consequently, with the method, we can modify the modulator slightly and overcome the non-ideality of the excess loop delay.

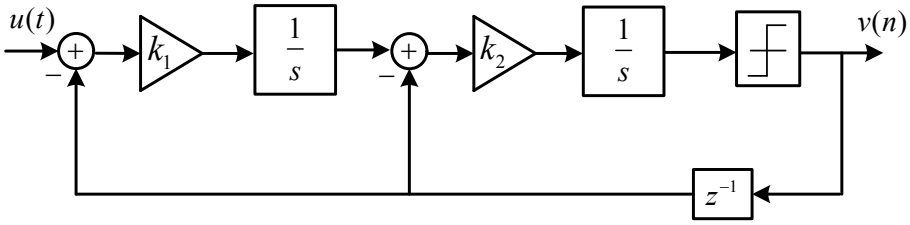



Fig. 3.8 Second-order CT modulator with $\tau_d = T_s$

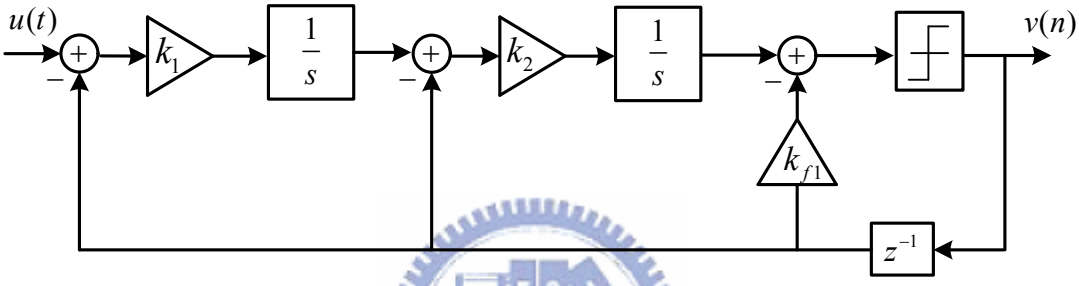



Fig. 3.9 Modified second-order CT modulator

### 3.3.3 Clock Jitter

In CT sigma-delta modulators, one of the most important non-idealities is clock jitter. The clock jitter arises from both the quantizer and the feedback DACs. Due to the same order noise shaping, the sampling error at the quantizer only adds little noise to the modulator output. Nevertheless, the clock jitter in the feedback DACs generates non-shaped noise. It is the primary reason to affect the modulator performance significantly.

Fig. 3.10 shows the model of the jitter-induced noise for NRZ feedback DAC. In each sampling instant, the error area $\Delta A(n)$ between ideal waveform and jittered waveform can be modeled as an equivalent error in the signal magnitude $e(n)$. In

other words, the equivalent error $e(n)$ can be expressed as follows

$$e(n) = \frac{\Delta A(n)}{T_s} = \left(v(n) - v(n-1)\right) \cdot \frac{\Delta t(n)}{T_s} \tag{3.15}$$

From (3.15), we can observe that if the difference between $v(n-1)$ and $v(n)$ is less, the clock jitter has lees effect upon the modulator performance. Therefore, the multi-bit quantizer has better jitter noise immunity.

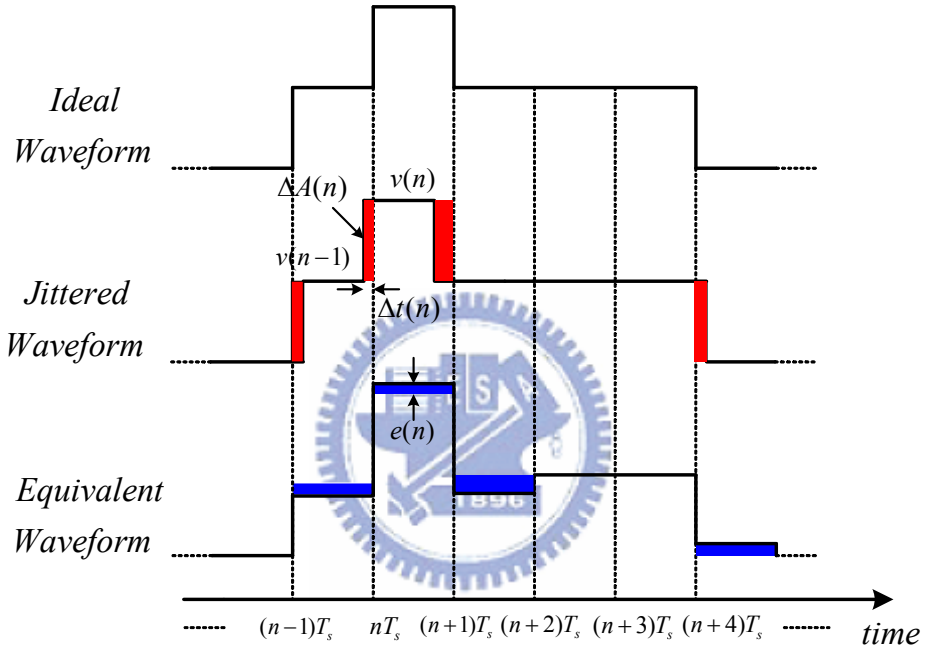



Fig. 3.10 Model of the jitter-induced noise for NRZ feedback DAC

DAC shape also affects the jitter sensitivity of CT modulators. This can be illustrated by Figure 3.11, where single-bit NRZ, RZ and HRZ feedback DAC shapes are described. In Fig. 3.11, the solid lines indicate the affected clock edges. In NRZ aspect, the NRZ DACs are only affected by clock jitter when the outputs change. On the contrary, the RZ and HRZ DACs suffer from the effect of the clock jitter in rising and falling edges of every clock cycle. They are more frequently affected than NRZ. So, the NRZ DAC is more resistant to the clock jitter. A good rule of thumb is that CT modulators employing RZ or HRZ DACs experience jitter noise about 6dB worse in

the signal band than if NRZ DACs are used [12].

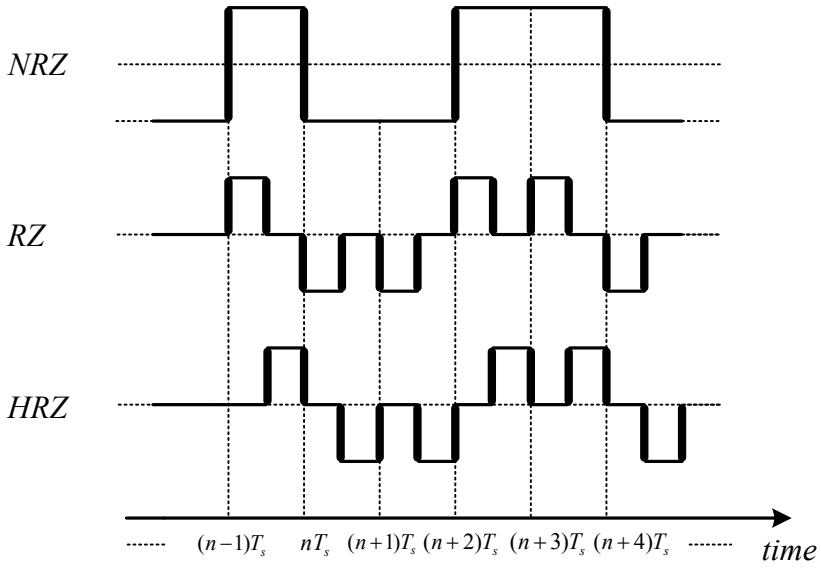



Fig. 3.11 Error sequence energy in different DAC shapes

# *CHAPTER 4*
# *A Continuous-Time Single-Bit Active-RC Sigma-Delta Modulator for Bluetooth*

## *4.1 Introduction*

In this chapter, we implement a continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application. The order of the loop filter is third and through the use of the architecture, cascade of resonators with distributed feedback (CRFB) [7], we can improve the bandwidth without increasing the order of the loop filter.

We use the typical type, active-RC integrator, to implement the first, second and third stage. Due to the closed-loop operation, the active-RC integrator has better linearity than the $g_m$-C integrator. However, because of the loading effect, the active-RC integrator requires an additional output buffer which consumes much power. This is a trade off between the two typical integrators.

Finally, the system and circuit level implementations are presented and the design considerations are explained. The chip is designed in TSMC 0.18μm CMOS process and the chip size is 1.32mm x 1.23mm. This work achieves 69.5dB SNDR performance and consumes 21.9mW at 1.8V supply voltage.

## *4.2 Loop Filter Architecture*

### *4.2.1 Architecture*

The loop filter of the CT third-order modulator uses CRFB architecture, as shown in Fig. 4.1. The transfer function in Fig. 4.1 can be derived by

$$H(s)=\frac{a_3\cdot c_3\cdot s^2+(c_2\cdot c_3\cdot a_2)s+c_1\cdot c_2\cdot c_3\cdot a_1}{s^3+g\cdot c_2\cdot c_3} \tag{4.1}$$

The advantage of the architecture is capable of realizing NTF zeros as two conjugate complex pairs on the unit circle to obtain wider bandwidth. For example, the pole-zero plot of the third-order architecture is illustrated in Fig. 4.2. In Fig. 4.2, we can observe that there are one zero at DC and two conjugate zeros on the unit circle as the described advantage. The power spectral density is shown in Fig. 4.2 (a).

It is expected that even greater benefits can be obtained by optimizing the location of the zeros of higher-order NTF. The resulting values for the zeros are given in Table 4.1 for NTF with degrees from 1 to 8 [7].

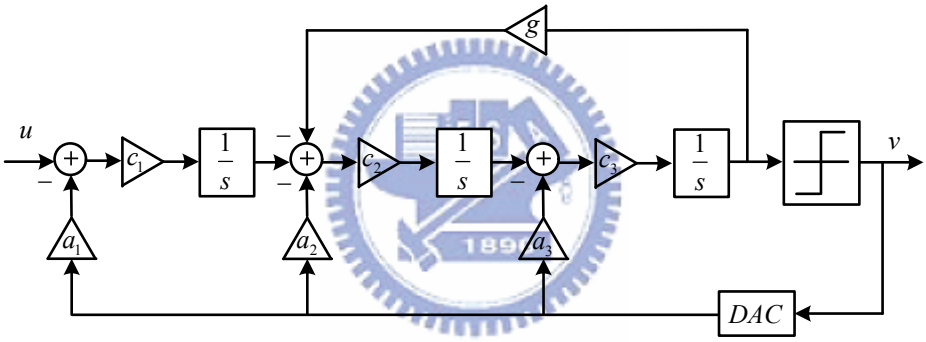



Fig. 4.1 CRFB architecture

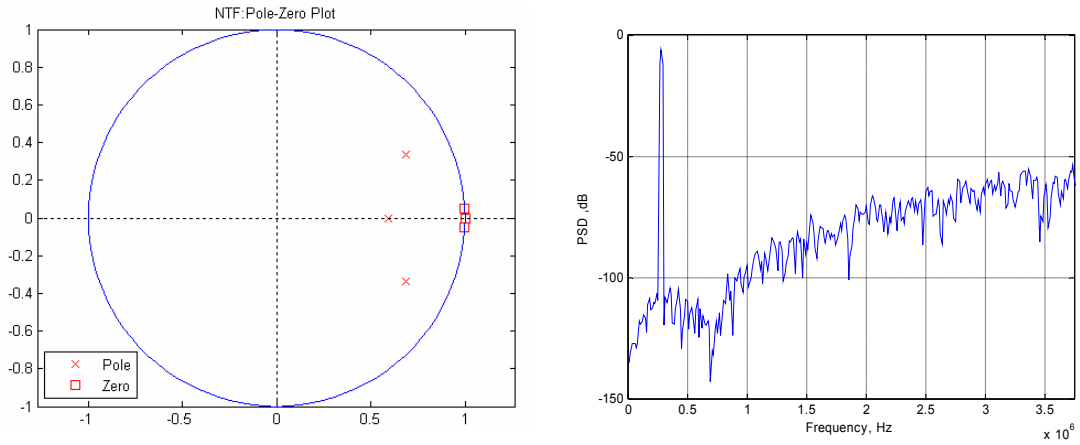



Fig. 4.2 (a) Pole-zero plot (b) PSD of CRFB

Table 4.1 Zero placement for minimum in-band noise

| N | Zero locations, normalized to bandwidth $\omega_B$ | SNR improvement |
|---|---|---|
| 1 | 0 | 0 dB |
| 2 | $\pm 1/(\sqrt{3})$ | 3.5 dB |
| 3 | $0,\ \pm\sqrt{3/5}$ | 8 dB |
| 4 | $\pm\sqrt{3/7 \pm \sqrt{(3/7)^2 - 3/35}}$ | 13 dB |
| 5 | $0,\ \pm\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$ | 18 dB |
| 6 | $\pm 0.23862,\ \pm 0.66121,\ \pm 0.93247$ | 23 dB |
| 7 | $0,\ \pm 0.40585,\ \pm 0.74153,\ \pm 0.94911$ | 28 dB |
| 8 | $\pm 0.18343,\ \pm 0.52553,\ \pm 0.79667,\ \pm 0.96029$ | 34 dB |

### 4.2.2 Coefficients

One of the most important designs in sigma-delta modulator is the coefficients. Different coefficients have different noise shaping and stability issues. Fortunately, by the widely used sigma-delta toolbox [7], the DT loop filter can be obtained easily. For example, the *synthesizeNTF* function in sigma-delta toolbox is used to synthesize a NTF according to the order of the modulator, OSR and so on. In other words, we can obtain the STF and the loop filter function from the NTF. Therefore, through the use of the impulse-invariant transformation introduced in section 3.2, the CT loop filter function can be derived.

For example, first, by using the *synthesizeNTF* function and assuming the third-order lowpass modulator, where the OSR is equal to 50 and the maximum out-of-band gain of the NTF is 1.7, the DT NTF can be derived by

$$NTF(z) = \frac{(z-1)(z^2 - 1.998z + 1)}{(z - 0.5932)(z^2 - 1.37z + 0.5824)} \tag{4.2}$$

and the DT loop filter can be expressed as

$$H(z) = \frac{1.0349(z^2 - 1.549z + 0.6325)}{(z-1)(z^2 - 1.998z + 1)} \tag{4.3}$$

Second, by applying impulse-invariant transformation in Matlab, the CT loop filter can be obtained by

$$H(s) = \frac{0.8306s^2 + 0.3804s + 0.0864}{s^3 + 0.002s} \tag{4.5}$$

Finally, from (4.1), (4.5) and by assigning the initial values of the feedback coefficients $a_1 = 1$, $a_2 = 1$ and $a_3 = 1$, the CT coefficients can be acquired as

$$c_1 = 0.2272,\ c_2 = 0.458,\ c3 = 0.8306,\ g = 0.0053 \tag{4.6}$$

This is not the only solution and many other more systemic methods proposed in [7] can also effectively resolve the coefficient issues.

## *4.3 System Level Analysis*

The first step of design sigma-delta modulator is to determine the NTF. By the sigma-delta toolbox, the NTF can be easily derived according to the specifications. In this work, we design a third-order modulator, where the OSR is equal to 50 and the maximum out-of-band gain of the NTF is 1.7, as shown in Fig. 4.3. In Fig. 4.3 (a), we simulate the maximum out-of-band gain of the NTF versus the peak SNR in system level. Due to the stability issue, we can find that the maximum out-of-band gain of the NTF is limited. The plot of the input level versus the SNR is shown in Fig. 4.3 (b). Therefore, we choose that the maximum out-of-band gain of the NTF is equal to 1.7 and the peak SNR is 86dB.

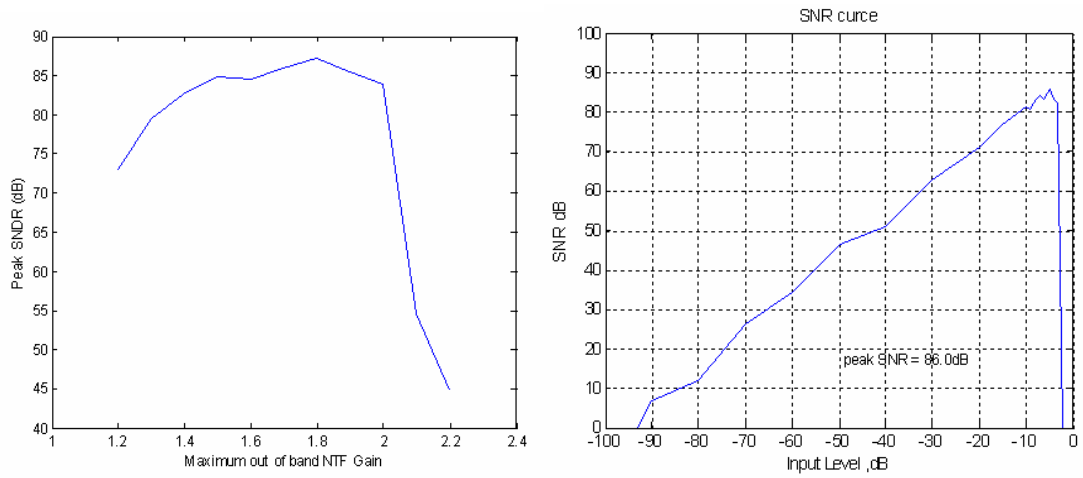



Fig. 4.3 (a) Maximum out-of-band gain of the NTF versus the peak SNR (b) Input level versus the SNR in system level

Based on the architecture of Fig. 4.1, the SIMULINK model of the system level is shown in Fig. 4.4. By the SIMULINK model, we can analyze different non-idealities to estimate the noise budget and achieve attainable performance.

The CT third-order sigma-delta modulator operates at 100MHz and the signal bandwidth is 1MHz. The oversampling ratio is equal to 50.

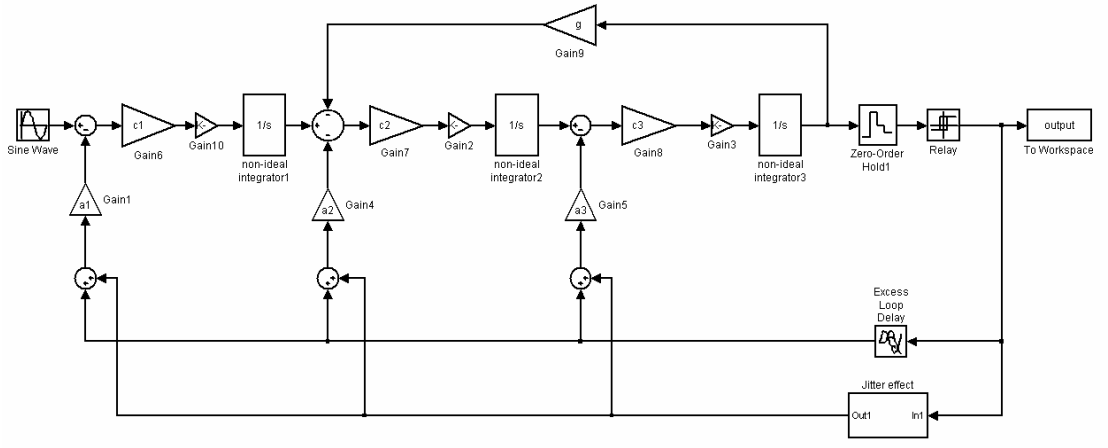



Fig. 4.4 SIMULINK model with non-idealities

### 4.3.1 RC Variation

One of the circuit imperfections in CT sigma-delta modulators is variation of the RC time constant. In modern standard digital process, the actual value of resistors and capacitors can vary as large as ±20%. For CT modulators, ±20% variation is more than enough to derive the modulator into unstable operation. Therefore, by analyzing the behavior model, the SNDR performance for -7.9 dBFS input under the variation of the time constant is shown in Fig. 4.5. We can find that a time constant variation of about +50% can also make the modulator stable and achieve the 65dB SNDR performance. However, a negative time constant variation results in the unstable modulator instead. Consequently, we need an additional tuning circuit discussed in section 4.4.6 to vary the time constant of the CT modulator and ensure that the modulator is in stable operation.

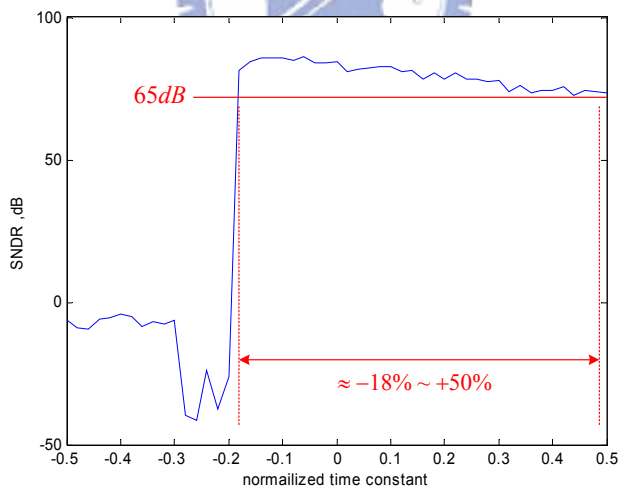



Fig. 4.5 Simulated SNDR for -6 dBFS input under the variation of the time constant

### 4.3.2 Excess Loop Delay

In section 3.3.2, we have introduced the non-ideality of the excess loop delay. The excess loop delay can cause the deviation of the transfer function to degrade the

performance or even seriously make the modulator unstable. By the behavior model analysis, we can estimate the allowable excess loop delay and achieve the limitation in circuit level design. Fig. 4.6 shows the simulated SNDR performance for -6 dBFS input under the non-ideality of the excess loop delay. We can find that when the excess loop delay is larger than 25% $T_s$, the modulator will be unstable. Therefore, we have about 20% $T_s$ to tolerate the circuit delay.

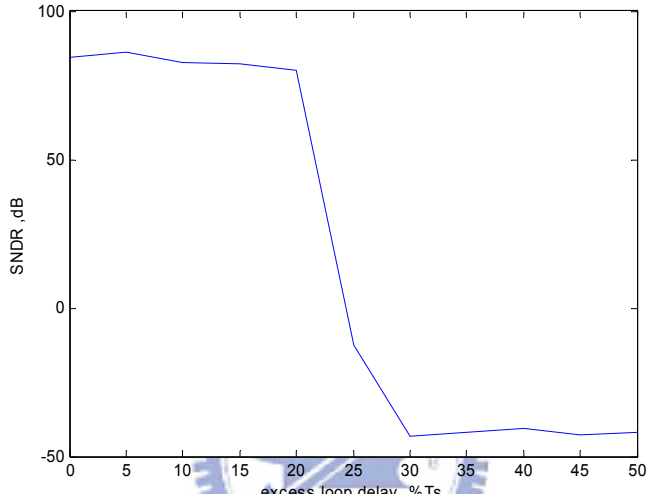



Fig. 4.6 Simulated SNDR for -6 dBFS input under the effect of the excess loop delay

### 4.3.3 Clock Jitter

The effect of the clock jitter has been introduced in section 3.3.3. The main influence is that the clock jitter in the feedback DACs generates non-shaped noise. The noise can degrade the modulator performance significantly. Thereby, by the behavior model analysis, we can estimate the performance degradation generated by clock jitter noise. Fig. 4.7 shows the simulated SNDR for -6 dBFS input under the effect of the clock jitter. If we want to achieve the 65dB SNDR performance, the effect of the clock jitter should be smaller than 0.1% $T_s$. This can be accomplished by low-jitter clock generator [13].

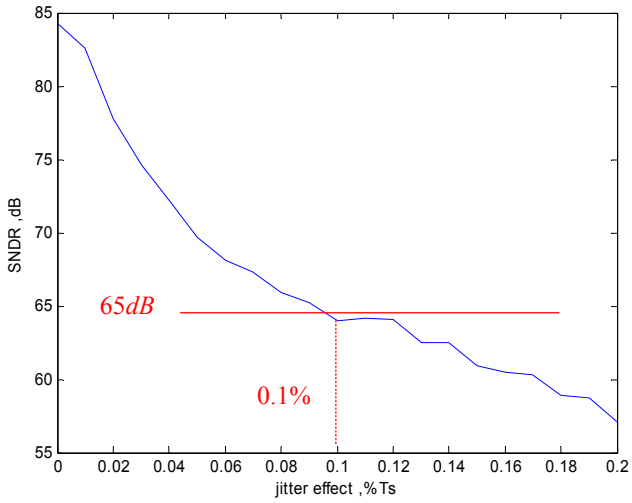



Fig. 4.7 Simulated SNDR for -6 dBFS input under the effect of the clock jitter

### 4.3.4 Simulation Result

Assuming the +10% time constant variation, 10% $T_s$ excess loop delay and 0.05% $T_s$ clock jitter, the whole behavior model simulation is shown in Fig. 4.8. For Fig. 4.8, the input sine wave is set to be -6dBFS at 280.76 kHz. The noise floor is around -100dB and the SNDR performance is about 70.6dB.

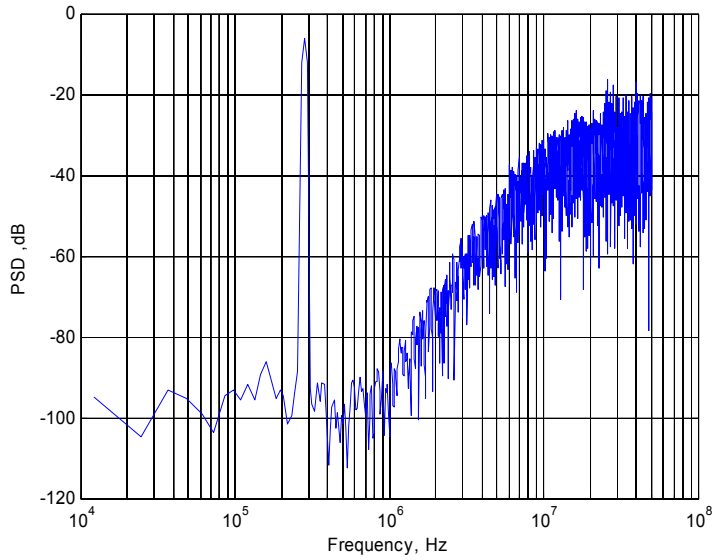



Fig. 4.8 Behavior model simulation result

## 4.4 Circuit Level Implementation

In this section, the circuit level implementation of the continuous-time single-bit active-RC sigma-delta modulator for Bluetooth is introduced in detail. The modulator is designed in a standard TSMC 0.18μm CMOS process with 1.8V supply voltage.

Fig. 4.9 shows the simplified block diagram of the CT third-order modulator. The architecture of the three integrators uses the typical type, active-RC. Because of the closed-loop operation, the active-RC integrator has better linearity than the $g_m$-C type. The single-bit quantizer is composed of the preamplifier, the regenerative latch and the SR latch which realizes the NRZ shape. The output of the quantizer is to control the switches of the current steering DACs which form the feedback loop.

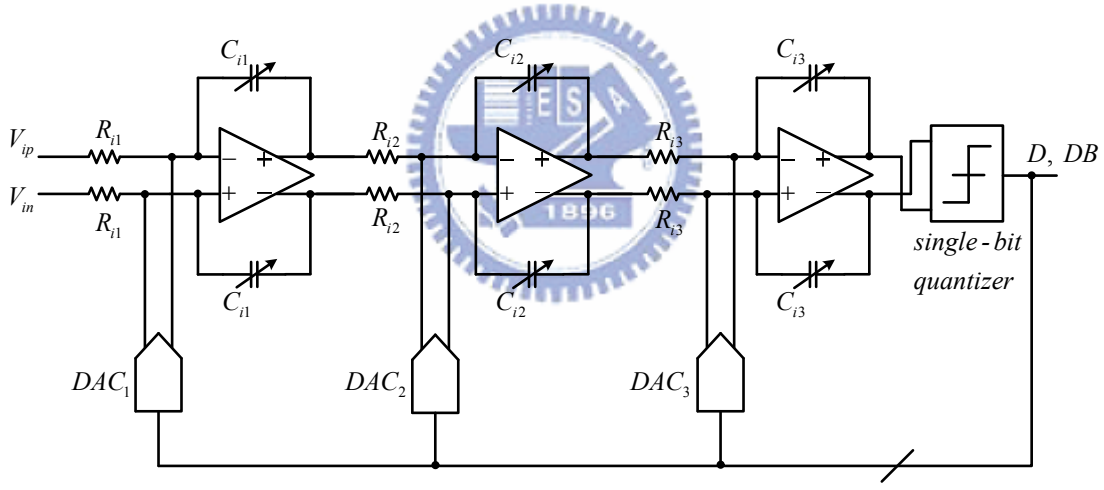



Fig. 4.9 Simplified block diagram of the CT third-order modulator

In the following subsection, other important analog parts are described and the design considerations are explained in detail.

### 4.3.1 Operation Amplifier of the First Stage

Due to the Bluetooth application in our design, where the sampling frequency is 100MHz and the bandwidth is 1MHz, the opamp in the first stage integrator uses a

telescopic topology. Compared with the two-stage and folded cascode opamps, telescopic opamps achieve the highest speed with the lowest power consumption and generate low noise. In order to make sure that the modulator can be function work, we apply gain boosting to the differential cascade stage, as shown in Fig. 4.10. The objective is to maximize the output impedance so as to attain a high voltage gain. The common-mode feedback (CMFB) circuit is shown in Fig. 4.11 and it generates the common-mode voltage of the output signals (minus a dc level shift) at node $V_A$. This voltage is then compared to the reference voltage using a separate amplifier [9].

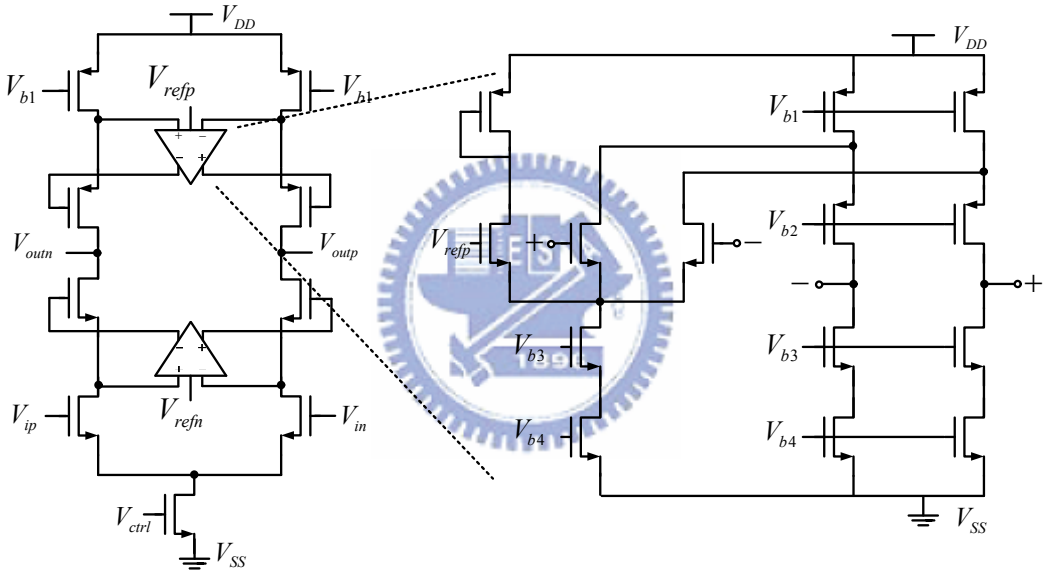



Fig. 4.10 Telescopic opamp with gain boosting of the first stage

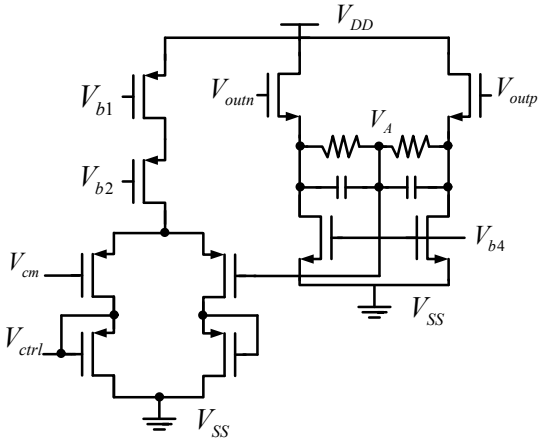



Fig. 4.11 CMFB of the first stage

Because of the loading effect of the second stage, as shown in Fig. 4.9, we need to design an output buffer, which is the class AB operation, illustrated in Fig 4.12 [14]. However, the output buffer will cause the opamp unstable. Therefore, in order to compensate the opamp, the capacitor and the resistor are used to improve the phase margin and stability.

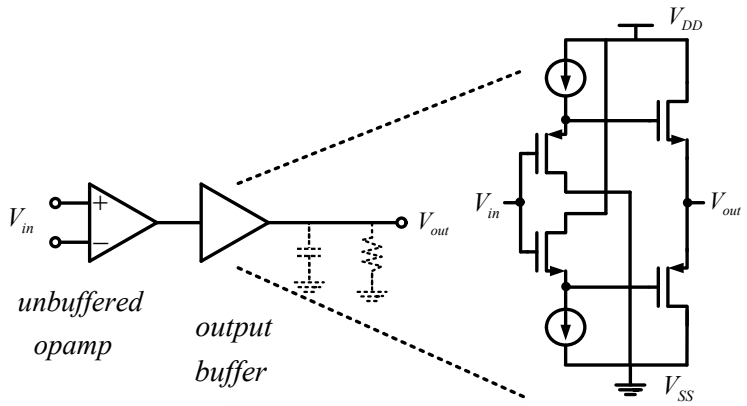



Fig. 4.12 Class AB output buffer of the first stage

Fig. 4.13 shows the AC simulation results in TT, FF and SS corner and the performance of the telescopic opamp with gain boosting is summarized in Table 4.2.

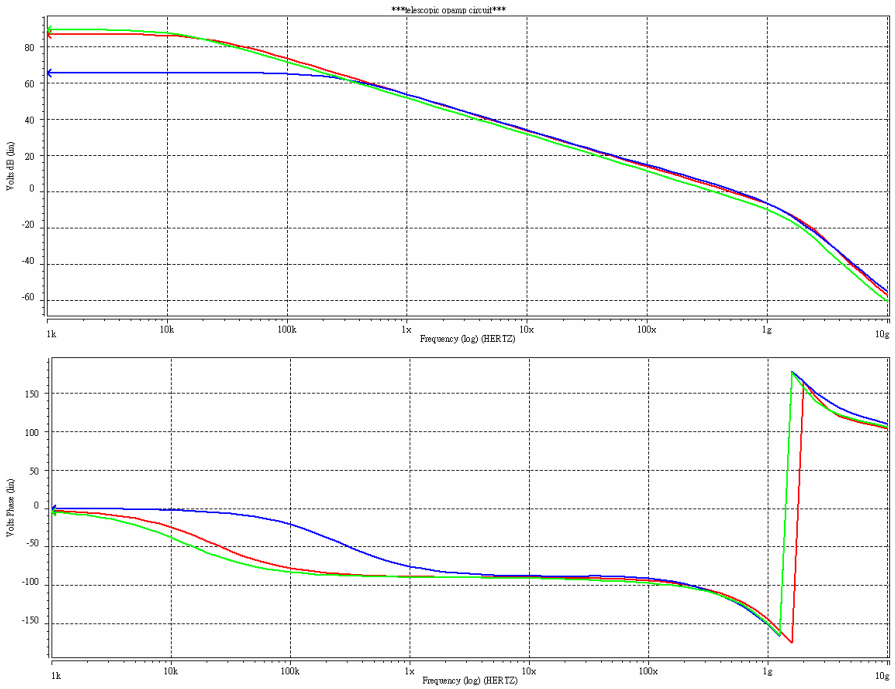



Fig. 4.13 Frequency response of the first stage opamp

Table 4.2 Performance of the first stage opamp

| Simulation Results | Red Line TT @ 50°C | Blue Line FF @ 0°C | Green Line SS @ 100°C |
|---|---|---|---|
| **Differential Gain** | 86.9 dB | 64.79 dB | 89.88 dB |
| **Phase Margin** | 64.58° | 56.27° | 69.5° |
| **Unity-Gain Frequency (5p)** | 497.9 MHz | 566.33 MHz | 356.15 MHz |
| **Output Swing** | 1.2V | | |
| **Power Dissipation** | 8.76mW | | |

### *4.3.2 Operation Amplifier of the Second & Third Stage*

Due to the noise shaping, the requirements of the opamp in the second and third stage could be less than the first stage. For this design, we use the folded-cascode opamp without gain boosting to implement the second and third stage, as shown in Fig. 4.14. For the same reason, loading effect, the class AB output buffer is also used in the second stage. Moreover, because of no loading effect, the third opamp could be without an output buffer.

Fig. 4.15 shows the AC simulation results in TT, FF and SS corner and the performance of the folded cascade opamp is summarized in Table 4.3.

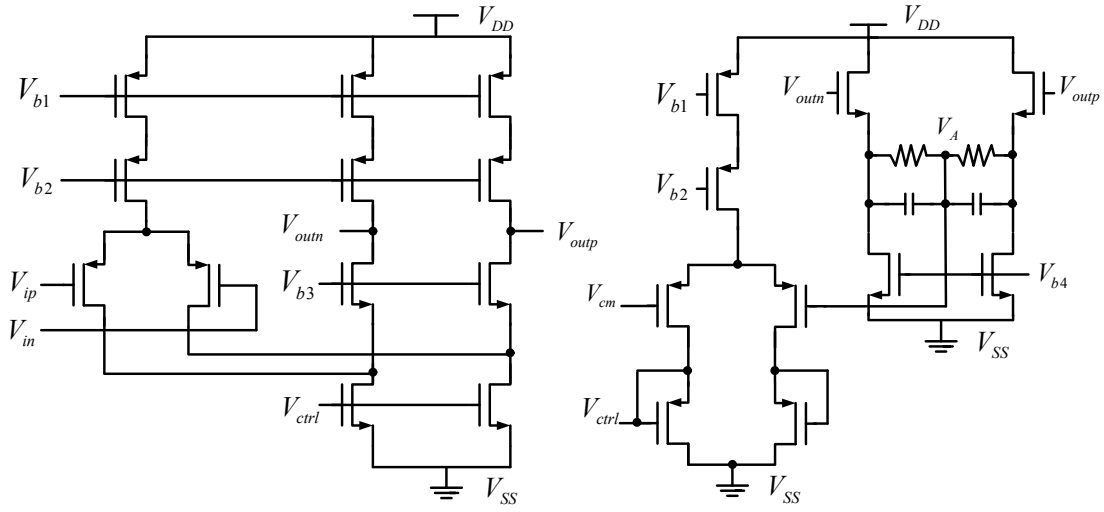



Fig. 4.14 Operation amplifier and CMFB of the second and third stage

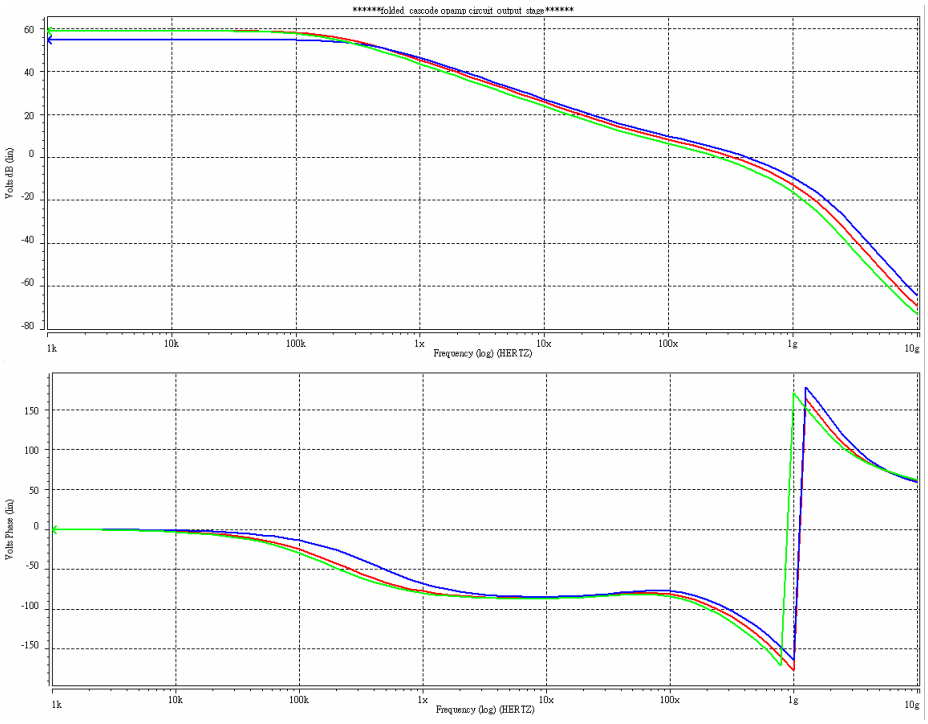



Fig. 4.15 Frequency response of the first second and third opamp

Table 4.3 Performance of the second and third stage opamp

| Simulation Results | Red Line TT @ 50°C | Blue Line FF @ 0°C | Green Line SS @ 100°C |
|---|---|---|---|
| **Differential Gain** | 59.03 dB | 54.88 dB | 58.86 dB |
| **Phase Margin** | 68.2° | 65.77° | 73.31° |
| **Unity-Gain Frequency (1.8p)** | 332.56 MHz | 430.12 MHz | 251.16 MHz |
| **Output Swing** | 1.4V | | |
| **Power Dissipation** | 4.64mW | | |

### *4.3.3 Comparator*

Fig. 4.16 shows the circuit of the comparator including a preamplifier and a low-offset regenerative latch [15]. In Fig. 4.16 (a), using a cross-coupled load to increase $R_o$, the differential gain can be improved and it can be expressed as

$$A_{dm} = g_{m1,2} \cdot \frac{1}{g_{m3,4} - g_{m5,6}} \tag{4.7}$$

In Fig. 4.16 (b), when $V_{CK}$ goes to high, the $M_1$ and $M_2$ work in saturation region and due to the mismatched current in the $M_1$ and $M_2$, the outputs are resulted from the cross-coupled inverters which form the positive feedback loop. In this phase, since the $M_1$ and $M_2$ are in saturation region so that the comparator has low offset voltage. When $V_{CK}$ goes to low, the outputs are reset to $V_{DD}$ and the SR latch maintains previous outputs to form the NRZ shape. The truth table of the SR latch is shown in Table 4.4. Another advantage of the regenerative latch is that when $V_{CK}$ goes to low, there is no power dissipation.

In order to reduce the influence of the excess loop delay, we add an additional preamplifier to improve the speed. Fig.4.17 shows the simulation result of the comparator. The sine wave is the input and the square is the output of the SR latch.

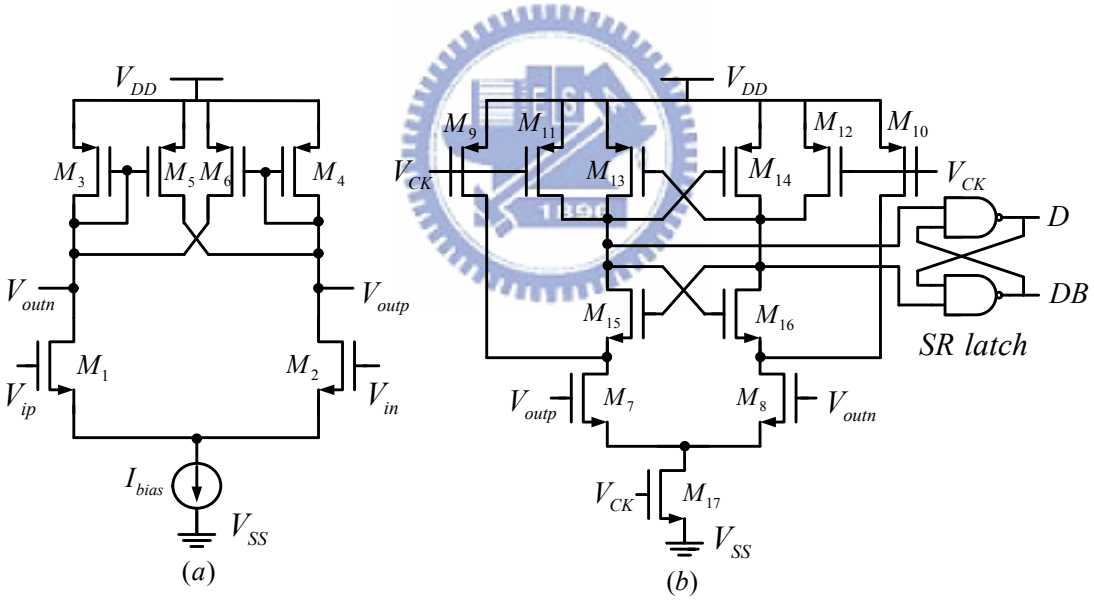



Fig. 4.16 (a) A cross-coupled preamplifier (b) Low-offset regenerative latch

Table 4.4 Truth table of the SR latch

| S | R | D | DB |
|---|---|---|---|
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | D | DB |

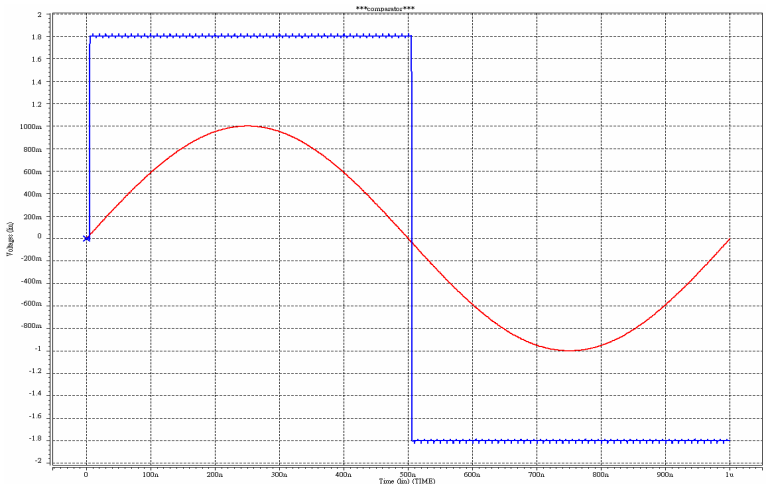


Fig. 4.17 Simulation result of the comparator

### 4.3.4 Current Steering DAC

Fig. 4.18 is the active-RC integrator with simplified representation of the current steering DAC [13]. The pair of current switches is controlled by feedback digital codes. The operation of the current steering DAC is described as follows:

When the output of the digital code $D$ is high, the $0.5I_{DAC}$ current source passes through the switch $D$ so that $0.5I_{DAC}$ is pulled from the $V_{ip}$ to $I_{DAC}$ current source. Since the switch $DB$ turns off, the $0.5I_{DAC}$ current source above the switch injects current into the $V_{in}$ to form the feedback loop.

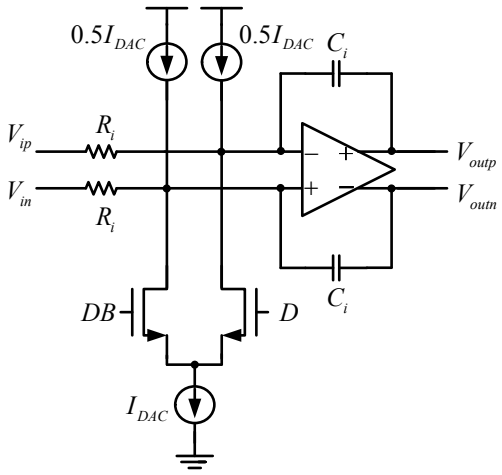



Fig. 4.18 Active-RC integrator with current steering DAC

### 4.3.5 Clock Generator

Fig. 4.19 shows the circuit of the low-jitter clock generator [13]. Through the cross-coupled load, it can attain high voltage gain. The differential input is sine wave and by means of the high voltage gain, the amplified signal forms the clock phase. Therefore, the circuit can reduce effectively clock jitter through the amplification.

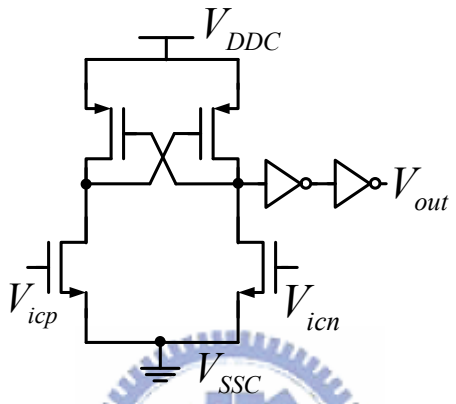



Fig. 4.19 Low-jitter clock generator

### 4.3.6 Tuning Circuit

From behavior model simulation in section 4.4.1, we only allow about −18% time constant variation to maintain 65dB SNDR performance for Bluetooth application. Due to the limitation, the tuning circuit shown in Fig. 4.20 must be needed [16]. For example, in Fig. 4.20 (a), it is an active-RC integrator realized by a tunable capacitor array. In Fig. 4.20 (b), there are an always-in-use capacitor which is 16C and five in-use capacitors which are 1C, 2C, 4C, 8C and 16C. The normal value of the capacitances is 32C. Through the use of the digital control signals, the minimum and maximum available capacitances are 16C and 47C, respectively. Thereby, the minimum tuning range is from -50% (16C/32C) to +46.875% (47C/32C) and the tuning resolution is 3.125% (C/32C), where C is the tuning step.

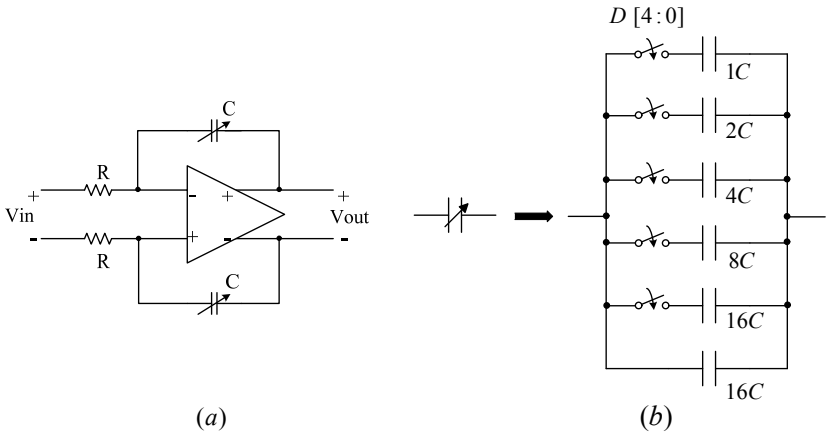
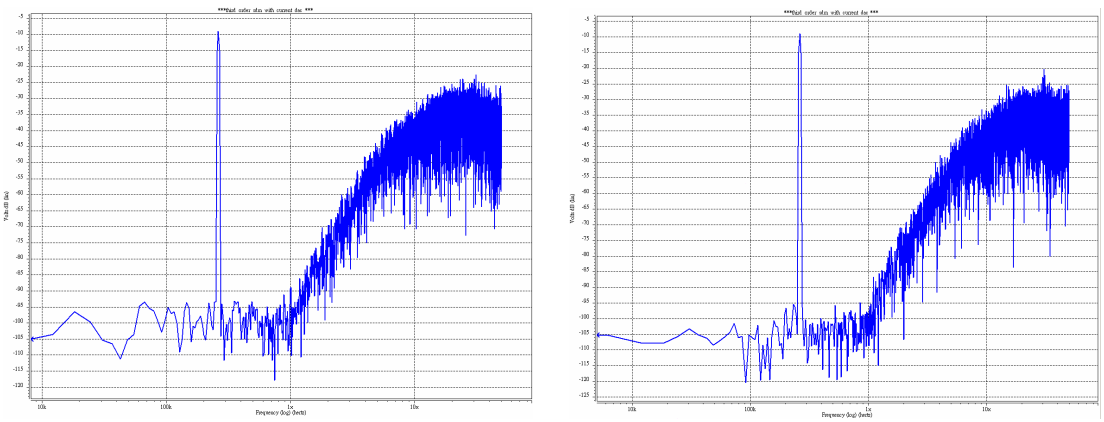


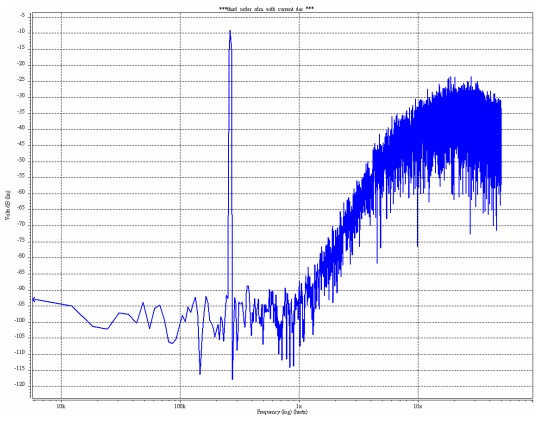

Fig. 4.20 (a) Active-RC integrator (b) Tuning circuit

### 4.3.7 Simulation Result

The simulated power spectral density of the continuous-time third-order single-bit active-RC sigma-delta modulator for Bluetooth is shown in Fig. 4.21. In Fig. 4.21, the sampling frequency is 100MHz and the signal bandwidth is 1MHz. The OSR is equal to 50 and the SNDR of the TT corner is about 69.5dB for -7.9 dBFS 262.45kHz input. The power consumption is 21.9mW at 1.8V supply voltage. The performance of this work is summarized in Table 4.5.



(a) (b)



(c)

Fig. 4.21 Simulated power spectral density of this work (a) TT (b) FF (c) SS corner

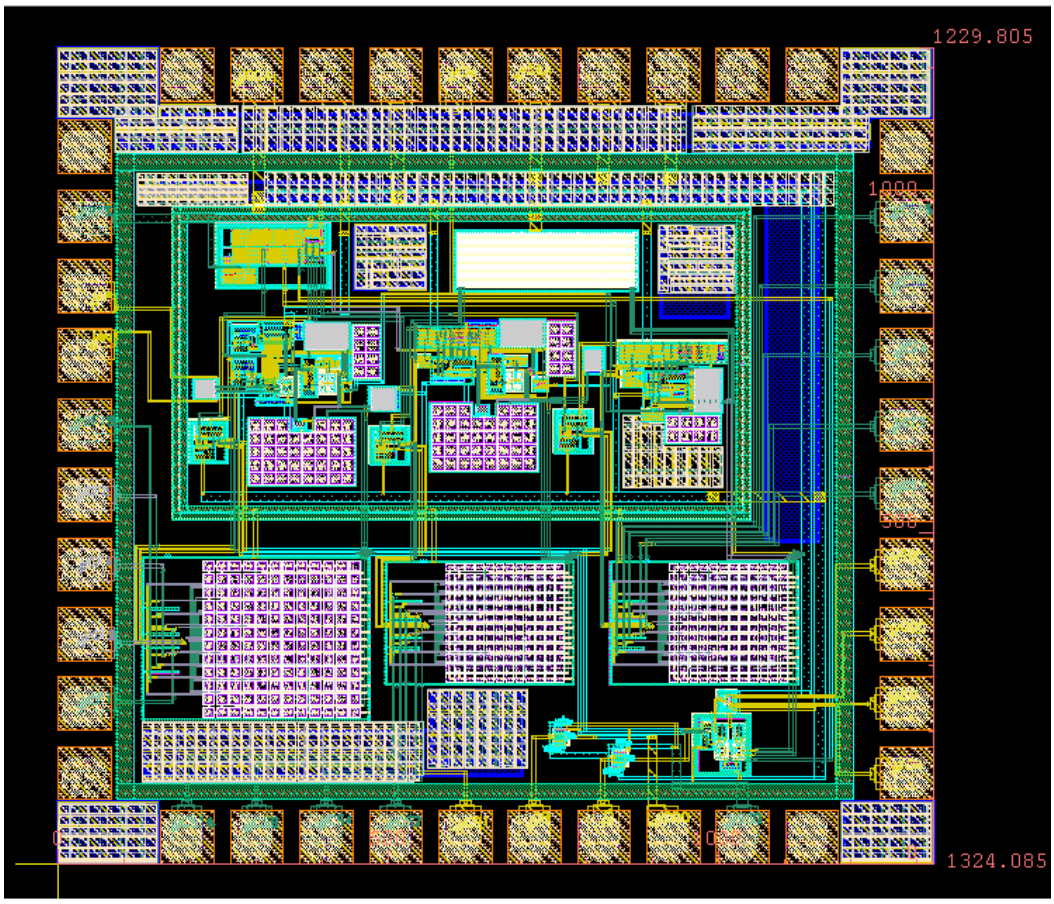
Table 4.5 Performance summary of this work

| | TT @ 50°C | FF @ 0°C | SS @ 100°C |
|---|---|---|---|
| **Sampling Frequency** | 100MHz | | |
| **Signal Bandwidth** | 1MHz | | |
| **SNDR (Fin=262.45kHz)** | 69.5dB | 73.6dB | 66.6dB |
| **Power Consumption @1.8V** | 21.9mW | | |
| **Area** | 1.32mm x 1.23mm | | |
| **Technology** | TSMC 0.18μm CMOS | | |

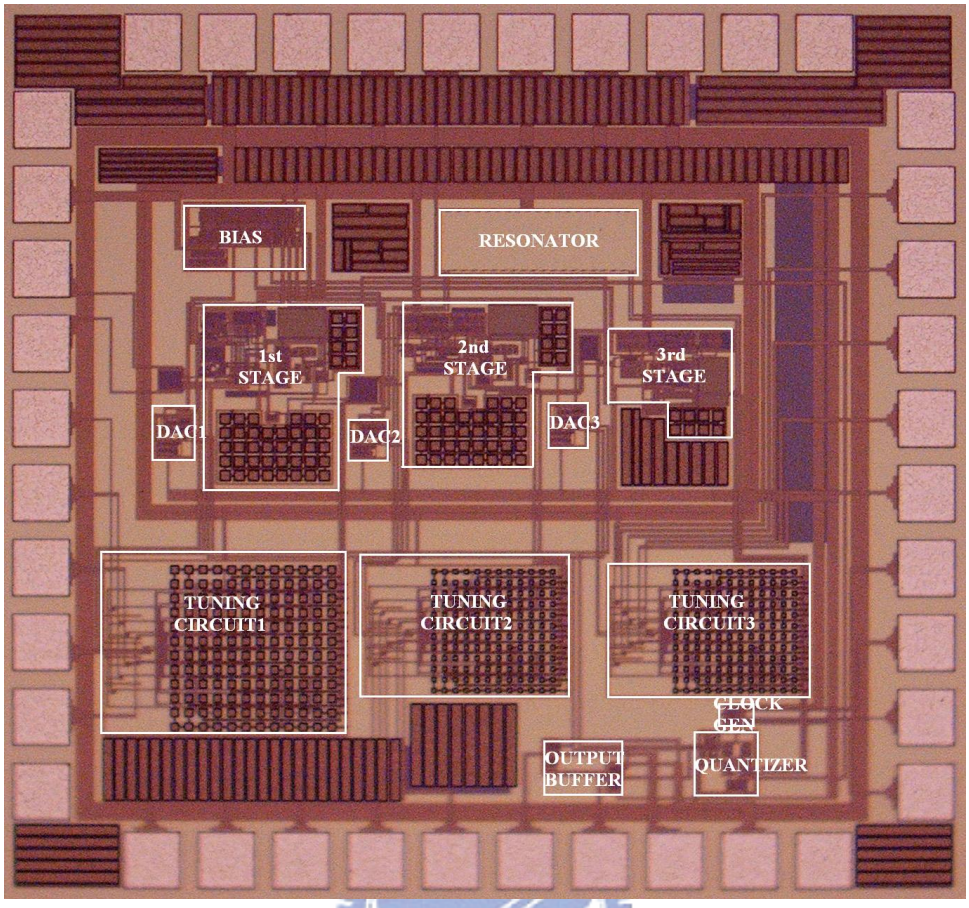
## *4.5 Layout Design*

In mixed-signal layout level design, the analog parts are more sensitive to noise than the digital parts. Therefore, we must take more considerations in mixed-signal layout. First, when the digital and analog circuits use the same substrate, the body of NMOS in digital must be tied to the digital ground which we have separated the power and ground of the analog and digital. This can avoid the noise in digital parts entering the analog parts through the substrate. Second, guard rings should be widely

used throughout a mixed-signal environment. More sensitive circuits should be placed in another well with guard rings attached to the power or ground. Third, the devices such as input pairs, resistors, capacitors and so on need to be symmetrized in the center of the device to reduce harmonic distortion and common centroid layout is a technique for this [17]. Fourth, using multiple pads $V_{DD}$ or $V_{SS}$ can reduce self-inductance [18]. The layout design and die photo are shown in Fig. 4.22 and the chip size is 1.32mm x 1.23mm.




(a)




(b)

Fig. 4.22 (a) Layout design (b) Die photo of this work

## 4.6 Summary

A continuous-time third-order single-bit sigma-delta modulator for Bluetooth application is designed in TSMC 0.18μm digital CMOS process. The architecture of the modulator utilizes CRFB structure to improve the signal bandwidth. The integrators are implemented by active-RC type to have better linearity. Additionally, in order to reduce the effect of the clock jitter, the feedback DAC shape is realized by NRZ. The CT third-order single-bit modulator achieves 69.5dB SNDR and the power consumption is 21.9mW.

# *CHAPTER 5*
# *Hybrid Sigma-Delta Modulator with Digital Error Truncation*

## *5.1 Introduction*

In chapter 2, we have introduced the advantages and disadvantages of the CT and DT modulators. The main advantages of the CT integrators are low power designs and better noise immunity due to inexistence critical slewing, settling issues and their inherent anti-aliasing filtering. The primary characteristics of the DT modulators have high accurate transfer functions and arbitrary scaled clock frequency for a multi-standard system. Alternative hybrid CT/DT loop filter approach tends to exploit the performance by keeping all the pros.

One way to achieve better dynamic range of the sigma-delta modulator is to increase the resolution of quantizer. However, the mismatched resistors or capacitors can cause the deviation of the feedback DACs and induce harmonic distortions to degrade modulator performance. The methodology—truncation error shaping and cancellation—applies digital sigma-delta modulators to reduce the feedback DAC levels and simplify the complexity of the dynamic element matching (DEM) or even avoid using it [19].

Due to the digital sigma-delta modulators, the hybrid sigma-delta modulator has a glitch problem. To solve the problem, a modified switched-capacitor with resistive element in CT feedback DAC is used. It is called SCR feedback configuration [20]. This method also relaxes the influence of the clock jitter which is a critical non-ideality.

Finally, the system and circuit level implementations are presented and the design considerations are explained. The chip is designed in 0.13μm digital CMOS process and the chip size is 0.698mm x 0.53mm. This work achieves 60.6dB SNDR performance and consumes 12.17mW at 1.2V supply voltage.

## 5.2 Truncation error shaping and cancellation

The two methods for reducing the feedback DAC levels are truncation error shaping and cancellation. They are combined to reduce the complexity of the DEM or possibly eliminate it. In other words, they improve the linearity of the feedback DACs to avoid appearance of the harmonic distortions.

Because of truncation error shaping and cancellation, it must add many digital processes in feedback paths. The digital processes need extra time to operate in the loop filter and could delay the modulator. In some cases, before the values of the digital processes are settled, the CT feedback DAC could induce glitches to influence the feedback pulsewidth and decrease SNR performance. Therefore, by using the SCR feedback configuration, the unnecessary glitches can be absorbed. Besides, it also decreases the limitation of the excess loop delay and clock jitter.

### 5.2.1 Truncation Error Shaping

The result of the truncation error shaping comes from a digital sigma-delta modulator as shown in Fig. 5.1. It is a first-order digital sigma-delta modulator with the delay moved after the output. The word-length of the input $X$ and the intermediate stage $X_1$ are N bits while the output $Y$ is M bits where N is larger than M. The truncation from $X_1$ to $Y$ is to inject the truncation error $E_1$. Under

the same assumption for the quantization error, the truncation error can be modeled as the additive white noise. Therefore, the output of the Fig. 5.1 can be easily expressed as

$$Y = X + (1 - z^{-1})E_T \tag{5.1}$$

In the same manner, the output of the second-order digital sigma-delta modulator shown in Fig. 5.2 can be also expressed as

$$Y = X + (1 - z^{-1})^2 E_T \tag{5.2}$$

Higher order truncation error shaping is more aggressive. However, as the analog sigma-delta modulators, the digital counterparts have stability problems as well and the number of the truncation bits cannot be arbitrarily large.

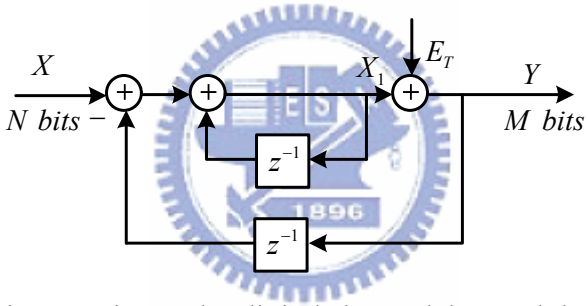



Fig. 5.1 First-order digital sigma-delta modulator

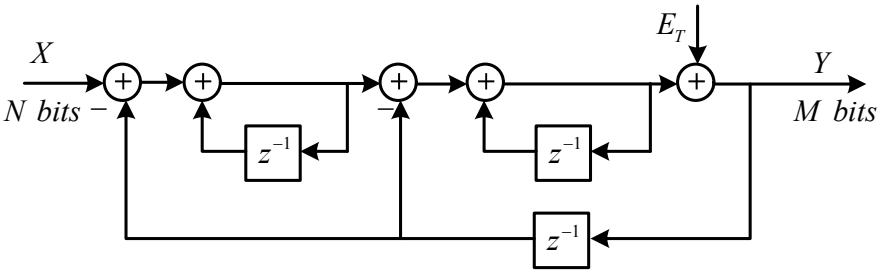



Fig. 5.2 Second-order digital sigma-delta modulator

The block diagram of the truncation error shaping in a DT second-order sigma-delta modulator is shown in Fig. 5.3, where the $Y_1$ and $Y_2$ are the output of the A-order and B-order digital sigma-delta modulators, respectively. By using the method, we can reduce the feedback DAC levels and shape the truncation error.

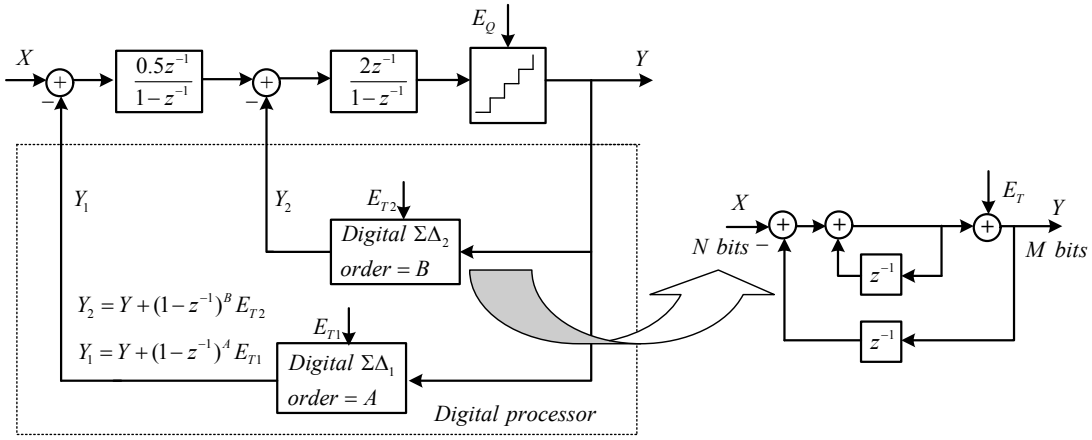



Fig. 5.3 Truncation error shaping in a second-order sigma-delta modulator

### 5.2.2 Truncation Error Cancellation

Since truncation is the result of a logic operation, the digital value of the truncation error is known. The truncation error passed through the integrator can be eliminated at the input of the next stage by adding another branch. For example, in the Fig. 5.3, the first truncation error $E_{T1}$ passed through the first integrator $0.5z^{-1}/1-z^{-1}$ becomes

$$E_{T1,out1} = 0.5z^{-1}(1-z^{-1})^{A-1}E_{T1} \tag{5.3}$$

and the second truncation error $E_{T2}$ passed through the second integrator $2z^{-1}/1-z^{-1}$ becomes

$$E_{T2,out2} = 2z^{-1}(1-z^{-1})^{B-1}E_{T2} \tag{5.4}$$

By adding branches at the first and second feedback paths, it can cancel the truncation error ideally if the analog integrators perfectly match digital processing, as shown in Fig. 5.4. In Fig. 5.4, the output of the first feedback path is equal to

$$Y_1 = Y + (1-z^{-1})^A E_{T1} \tag{5.5}$$

and due to the adding branch, the output of the second feedback path becomes

$$Y_2 = (Y - 0.5z^{-1}(1-z^{-1})^{A-1} E_{T1}) + (1-z^{-1})^B E_{T2} \tag{5.6}$$

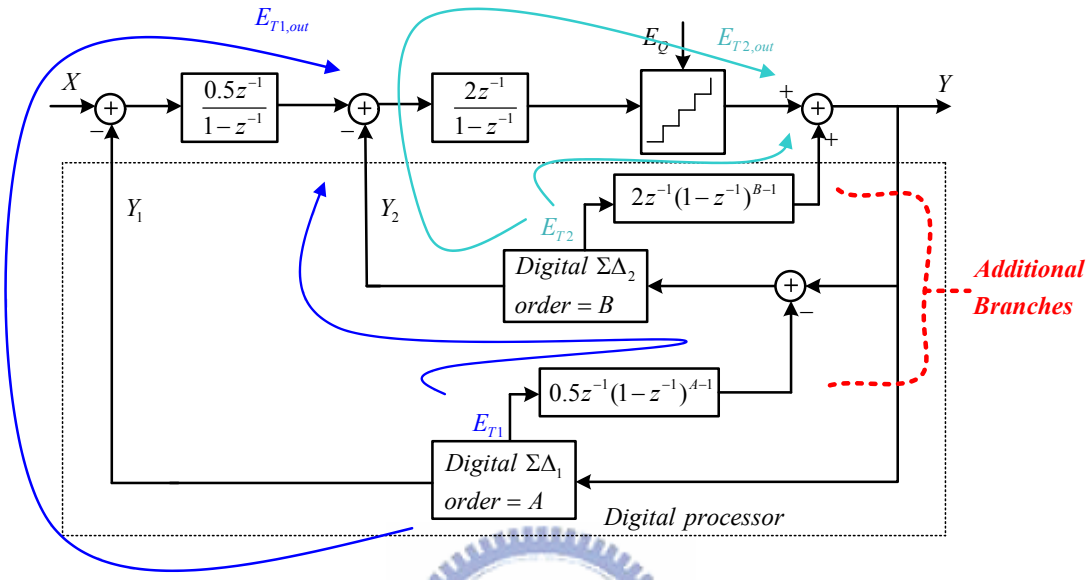



Fig. 5.4 Truncation error cancellation in a second-order sigma-delta modulator

By the combination of the (5.4) and (5.6), we can cancel the first truncation error $E_{T1}$ and in the same method, the second truncation error $E_{T2}$ can be also cancelled perfectly if the analog and digital parts are matched with each other. Therefore, the final system transfer function is

$$Y = z^{-2} X + (1-z^{-1})^2 E_Q \tag{5.7}$$

If the analog and digital parts have a possible mismatch $\delta_1$ and $\delta_2$, the transfer function may produce some errors. The system transfer function having mismatches becomes

$$Y = z^{-2} X + (1-z^{-1})^2 E_Q - \delta_1 z^{-2}(1-z^{-1})^A E_{T1} - 2\delta_2 z^{-1}(1-z^{-1})^{B+1} E_{T2} \tag{5.8}$$

However, the effect of the errors is likely negligible due to the noise shaping.

## 5.3 Switched-Capacitor Resistor (SCR) Feedback DAC

The technique uses a capacitor $C_R$ and a resistor $R_R$ in series to replace original CT feedback DAC, as shown in Fig. 5.5.

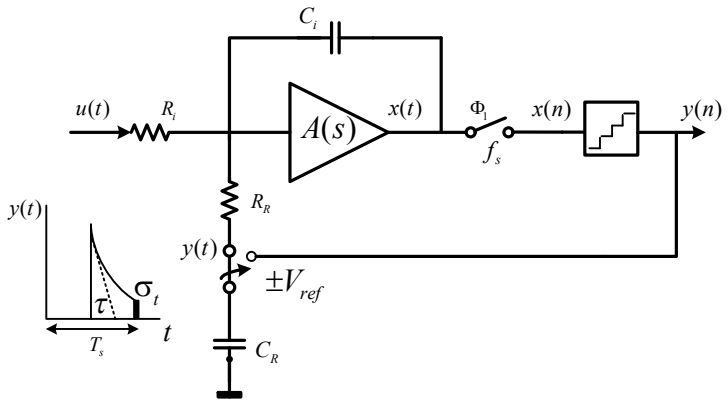



Fig. 5.5 CT sigma-delta modulator with SCR feedback

In Fig. 5.5, the $\phi_1$ is the sampling clock. When $\phi_1$ is high, the capacitor is charged by $\pm V_{ref}$ depended on the digital feedback signal; while $\phi_1$ is low, the capacitor is discharged through the resistor.

During the former half cycle, the capacitor is charged so that the feedback DAC has no effect in the modulator. Due to the characteristic of the technique, the issue of the glitches shown in Fig. 5.6 can be solved. Moreover, the excess loop delay cannot influence the loop filter in this phase. In Fig. 5.6, since the digital processor introduced in last section isn't ideal, it causes the DAC control signals to appear at different time. Therefore, it results in an unstable glitch phenomenon. The glitches make the DAC control signals incorrect transitorily that induce errors while integration.

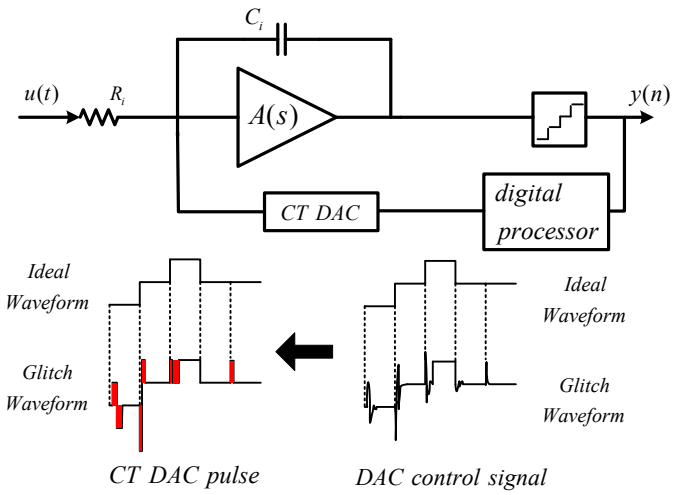



Fig. 5.6 Glitch issue due to digital processing in hybrid sigma-delta modulator

During the latter half cycle, the capacitor is discharged and the feedback DAC is realized with exponential decaying pulse form. In contrast with NRZ or RZ, the exponential decaying pulse form experiences less clock jitter due to the decaying quality, as shown in Fig. 5.5.

This technique overcomes the glitch phenomenon and decreases the non-idealities of clock jitter and excess loop delay to avoid making the function errors or even the modulator unstable. Thereby, the performance degradation of the modulator is keep minimum.

In Fig. 5.5, we define the feedback time constant $\tau$ and it can be expressed as

$$\tau = R_R C_R = b \cdot T_s \tag{5.9}$$

In section 3.2, we have known that different feedback DAC shapes influence the different transformation between CT and DT modulators. According to [20], the s-domain equivalences for simple z-domain loop filter are given in Table 5.1.

Table 5.1 CT equivalences for DT loop filter with SCR feedback

| DT | CT s-domain equivalent with $\tau = b \cdot T_s$ |
|---|---|
| $\frac{1}{z-1}$ | $\frac{r_0}{s}$ , $r_0 = \frac{f_s}{b}\frac{1}{(1-e^{(\frac{\alpha-\beta}{b})})}$ |
| $\frac{1}{(z-1)^2}$ | $\frac{r_1 s + r_0}{s^2}$ , $r_0 = \frac{f_s^2}{b}\frac{1}{(1-e^{(\frac{\alpha-\beta}{b})})}$ , $r_1 = \frac{f_s}{b}\frac{(\alpha+b-1)-e^{\frac{\alpha-\beta}{b}}(\beta+b-1)}{(1-e^{(\frac{\alpha-\beta}{b})})^2}$ |
| $\frac{1}{(z-1)^3}$ | $\frac{r_2 s^2 + r_1 s + r_0}{s^3}$ , $r_0 = \frac{f_s^3}{b}\frac{1}{(1-e^{(\frac{\alpha-\beta}{b})})}$ , $r_1 = \frac{f_s^2}{2b}\frac{(2\alpha+2b-3)+(e^{\frac{\alpha-\beta}{b}})^2(2\beta+2b-3)+e^{\frac{\alpha-\beta}{b}}(6-2\beta-2\alpha-4b)}{(1-e^{(\frac{\alpha-\beta}{b})})^2}$ <br> $r_2 = \frac{f_s}{2b}\frac{(\alpha^2+2b\alpha-3\alpha-3b+2)+(e^{\frac{\alpha-\beta}{b}})^2(\beta^2+2b\beta-3\beta-3b+2)+e^{\frac{\alpha-\beta}{b}}(\alpha^2+\beta^2-4\alpha\beta-2b\alpha-2b\beta+3\alpha+3\beta+6b-4b)}{(1-e^{(\frac{\alpha-\beta}{b})})^3}$ |

## *5.4 Hybrid Sigma-Delta Modulator with Digital Error Truncation*

The architecture of the second-order hybrid sigma-delta modulator with digital error truncation is shown in Fig. 5.7. The blocks in the dotted line are digital processor and others are analog parts. The first stage uses CT integrator to obtain inherent anti-aliasing filtering and low power design while the second stage uses DT one to achieve the characteristic of the robust transfer function and arbitrary scaled clock frequency. The 17-level quantizer is employed to improve the dynamic range.

The hybrid sigma-delta modulator operates at 62.5MHz which is sampling frequency and the signal bandwidth is 2MHz. The oversampling ratio is 16.

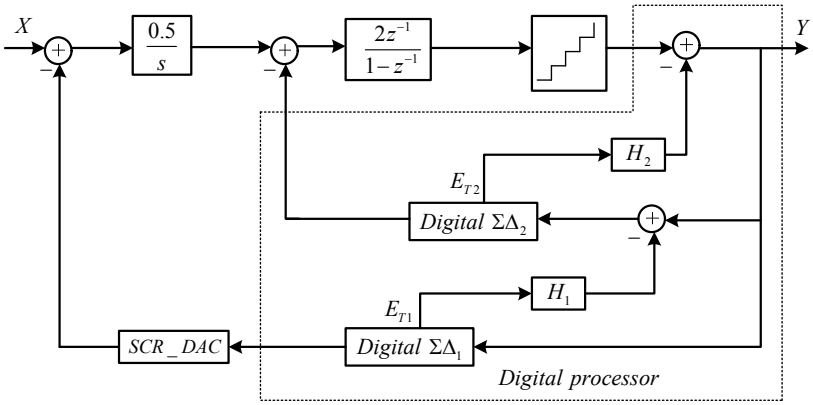



Fig. 5.7 Second-order hybrid sigma-delta modulator with digital error truncation

### 5.4.1 System Level Analysis

Based on the architecture of Fig. 5.7, the SIMULINK model of the system level is shown in Fig. 5.8. Through the use of the truncation error shaping and cancellation, the minimum required levels of the first and second feedback DAC are 3-level and 5-level so that the linearity of the feedback DACs can be improved to avoid using DEM. By behavior model analysis, the order of the first digital sigma-delta modulator is second-order while the second one is first-order. These are sufficient for the truncation error shaping and don't make the modulator unstable.

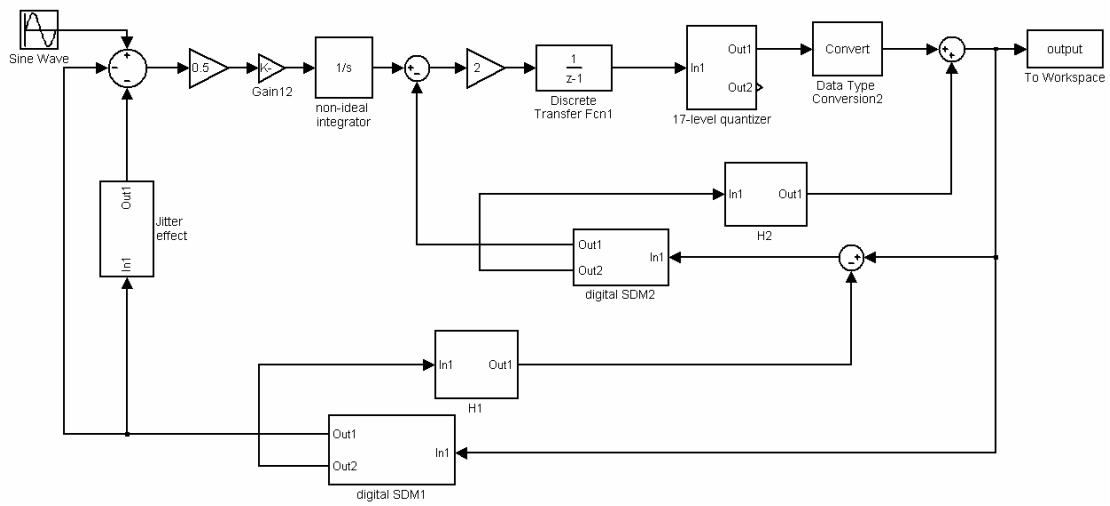
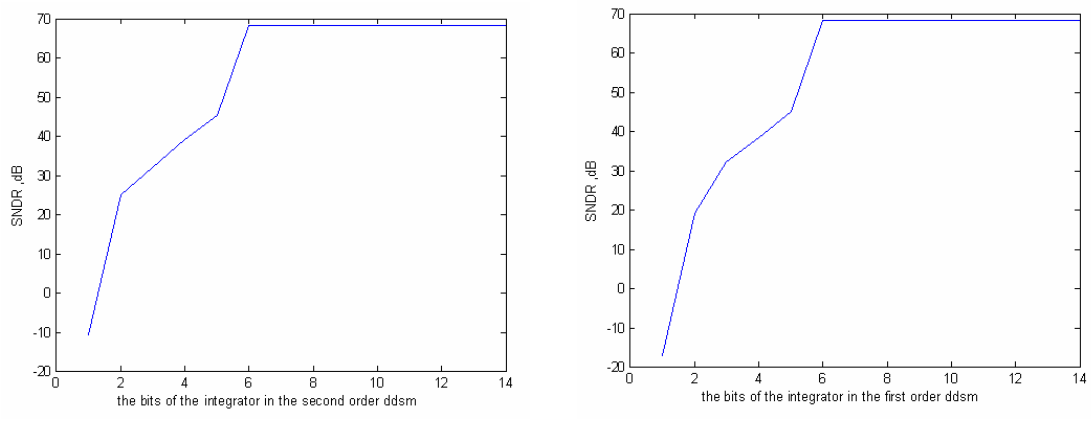



Fig. 5.8 SIMULINK model with non-idealities

#### 5.4.1.1 The Word-length of Digital Sigma-Delta Modulator

The word-length of the digital processor can be scaled down to save the power and area while still having the same performance [7]. Therefore, by analyzing the behavior model, the word-length of digital sigma-delta modulator can be estimated and reduced. The simulation result shows that the first and second digital modulator should be at least 6 bits to maintain SNDR performance for -6 dBFS input, as shown in Fig. 5.9. Keeping the digital processor simple, we set all the word-length to 6 bits.

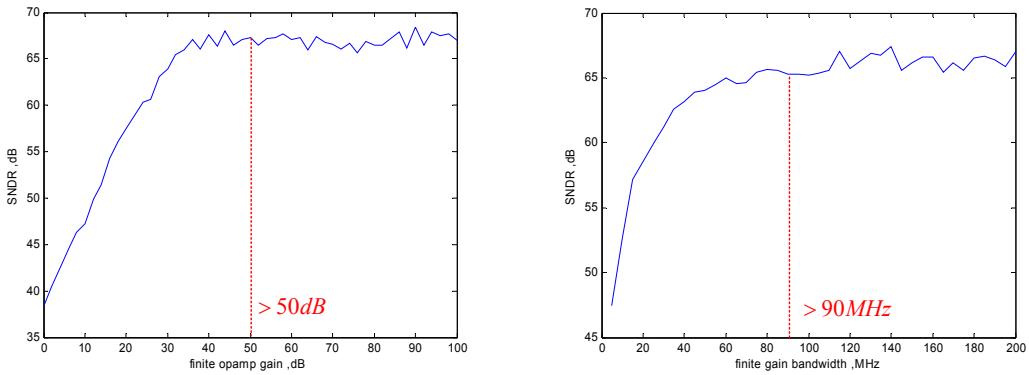



(*a*) (*b*)

Fig. 5.9 Simulated SNDR for -6 dBFS input in different bits of the (a) second-order (b) first-order digital sigma-delta modulator

### *5.4.1.2 Non-idealities of Integrators*

In sigma-delta modulators, the power consumption is usually dominated by first integrator. So, in a power-efficient design, the requirements of the first opamp should be considered in detail. In section 3.3, we have described the non-ideality of opamp in integrators. By utilizing these equations to analyze the behavior model, the simulation results for -6 dBFS input are shown in Fig. 5.10. From Fig. 5.10, we can observe that the requirements are larger than 50dB finite opamp gain and 90MHz bandwidth.




(*a*) (*b*)

Fig. 5.10 Simulated SNDR for -6 dBFS input under (a) finite DC gain and (b) finite gain bandwidth

### 5.4.1.3 RC Variation

One of the circuit imperfections in CT sigma-delta modulators is variation of the RC time constant. In modern standard digital process, the RC time constant of the integrators can vary as much as ±30%. In some situations, this variation makes the noise shaping inefficient or the modulator unstable. Therefore, by analyzing the behavior model, the SNDR performance for -6 dBFS input under the variation of the time constant is shown in Fig. 5.11. A time constant variation of ±10% results in about 5dB performance loss and about 10dB performance loss around ±20% variation. Hence, the modulator can be ensured stable.

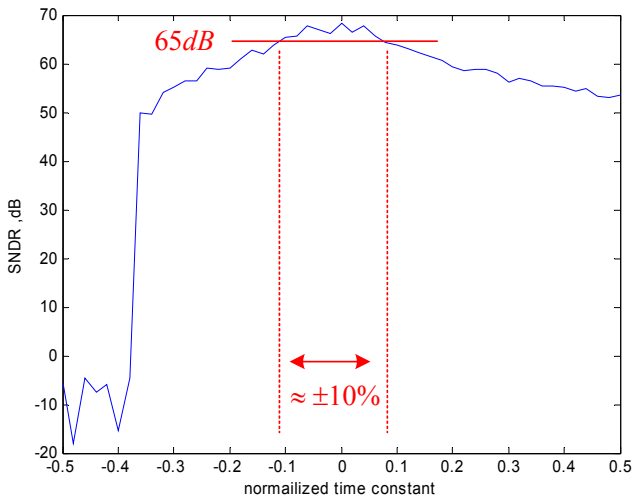



Fig. 5.11 Simulated SNDR for -6 dBFS input under the variation of the time constant

### 5.4.1.4 Clock Jitter

In section 3.3, we have introduced the non-ideality of clock jitter. For example, through the use of the truncation error shaping and cancellation, the first feedback DAC of the hybrid sigma-delta modulator is 3-level and the effect of the clock jitter with the SCR feedback is shown in Fig. 5.12. The result of using the DAC NRZ shape is also illustrated in Fig. 5.12. By behavior model simulation, the comparison of the two types for -6 dBFS input is shown in Fig. 5.13. From Fig. 5.13, we can discover

that the effect of the clock jitter in $0.2\%\ T_s$ only have 1dB SNDR decrease in SCR feedback type and attenuate about 8dB in NRZ feedback. Therefore, the SCR feedback technique not only solves the glitch phenomenon but also reduces the influence of the clock jitter.

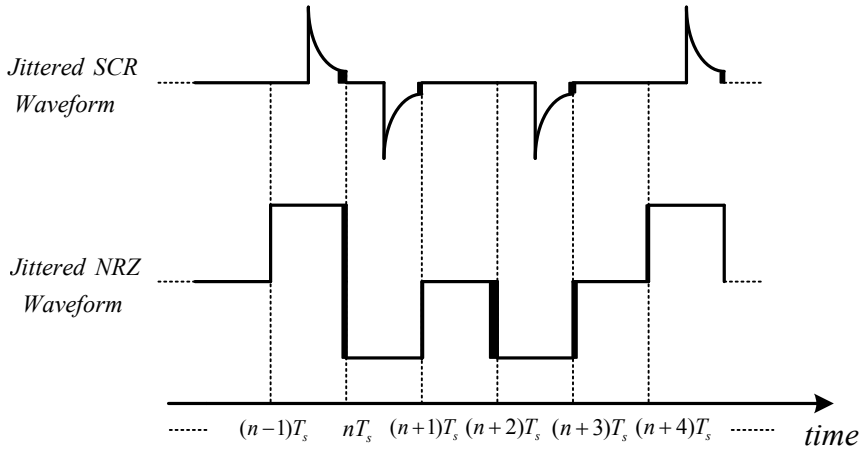



Fig. 5.12 Jittered SCR and NRZ waveform

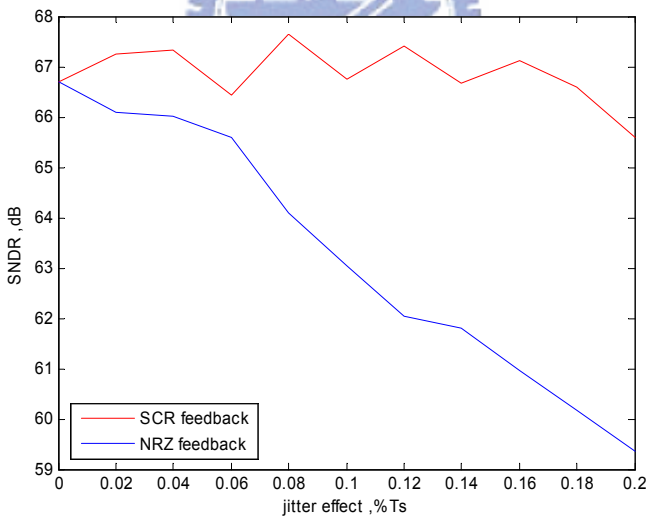



Fig. 5.13 Comparison of the SCR and NRZ feedback for -6 dBFS input under the effect of the clock jitter

### *5.4.1.5 Simulation Result*

Assuming the $0.1\%\ T_s$ clock jitter and the non-idealities of the first integrator including 50dB DC gain and 90MHz gain bandwidth, the whole behavior model

simulation is shown in Fig. 5.14. For Fig. 5.14, the input sine wave is set to be -6dBFS at 172.5 kHz. The noise floor is around -100dB and the SNDR performance is about 63.2dB.

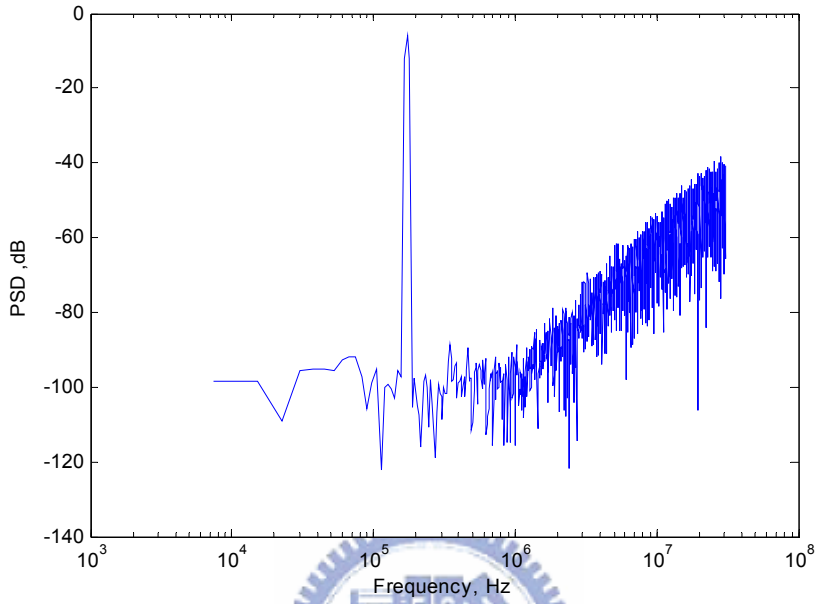



Fig. 5.14 Behavior model simulation result

### 5.4.2 Circuit Level Implementation

In this section, the circuit level implementation of the hybrid sigma-delta modulator is introduced in detail. The proposed modulator is designed in a standard digital 0.13μm CMOS process with 1.2V supply voltage.

Fig. 5.15 shows the analog parts of the first and second stage integrators. Because of digital error truncation with cancellation, the minimum required levels of the first and second feedback DAC are 3-level and 5-level. The first CT feedback DAC uses SCR feedback to solve the glitch issue while the second DAC utilizes the one proposed in [19] to avoid using DEM.

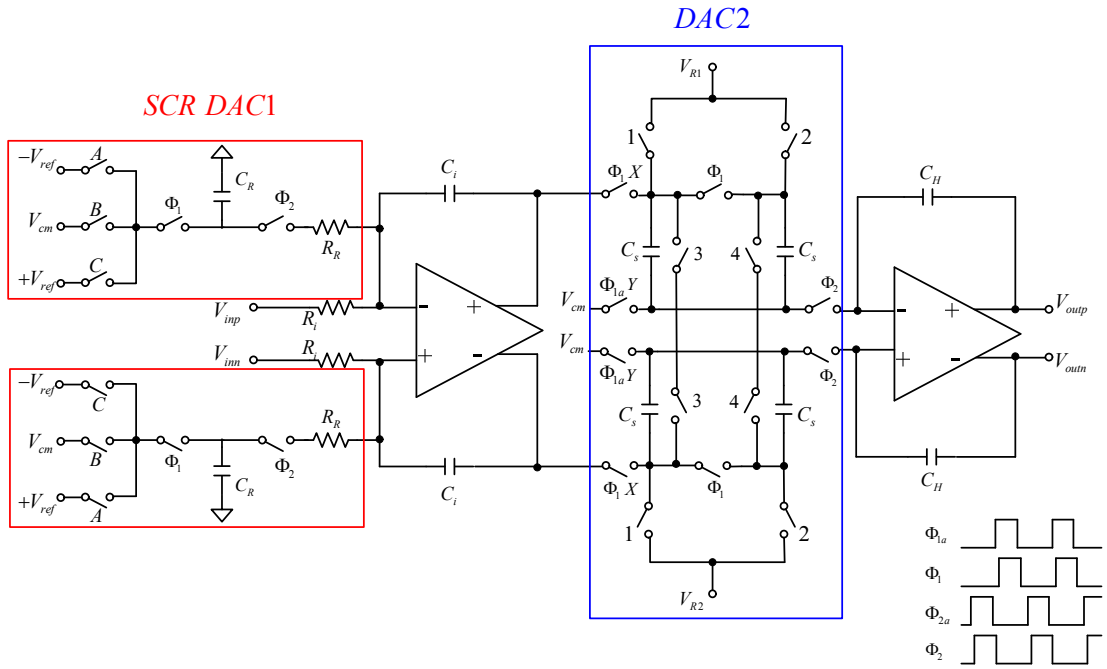



Fig. 5.15 First and second stage integrators

In the first stage, the SCR feedback circuit is described in Fig. 5.16. The control signals of the digital processor control the switch A, B and C. Since $+V_{ref}$ is near $VDD$, the switch A is implemented by PMOS. In contrast, the others use NMOS to avoid voltage loss. Table 5.2 shows the truth table of SCR DAC1 switches.

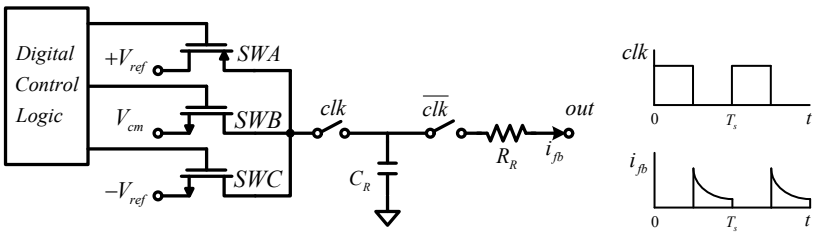



Fig. 5.16 Implementation of the SCR feedback circuit

Table 5.2 Truth table of SCR DAC1 switches

| SCR DAC1 | SWA | SWB | SWC |
|---|---|---|---|
| **1** | ON | OFF | OFF |
| **0** | OFF | ON | OFF |
| **-1** | OFF | OFF | ON |

In the second stage, $\phi_1$ and $\phi_2$ are non-overlapping clocks. $\phi_{1a}$ and $\phi_{2a}$ phase are the advance version of $\phi_1$ and $\phi_2$, respectively. In $\phi_1$ phase, the signals to the integrator are sampled to the capacitor $C_s$. By setting the switch Y off before the switch X, the charge injection of the switch X can be reduced. The technique is called bottom-plate sampling. In $\phi_2$ phase, the charge stored on $C_s$ is transferred to $C_H$ and the subtraction from the 5-level feedback DAC realized in series or parallel connection with the capacitors is executed. Table 5.3 shows the truth table of DAC2 switches [19].

Table 5.3 Truth table of DAC2 switches

| DAC2 | VR1 | VR2 | SW1 | SW2 | SW3 | SW4 |
|---|---|---|---|---|---|---|
| **1** | $-V_{ref}$ | $+V_{ref}$ | ON | ON | OFF | OFF |
| **0.5** | $-V_{ref}$ | $+V_{ref}$ | ON | OFF | OFF | ON |
| **0** | $+V_{ref}$ | $-V_{ref}$ | OFF | OFF | ON | ON |
| **-0.5** | $+V_{ref}$ | $-V_{ref}$ | ON | OFF | OFF | ON |
| **-1** | $+V_{ref}$ | $-V_{ref}$ | ON | ON | OFF | OFF |

In the following subsection, other important analog parts are described and the design considerations are explained in detail.

### *5.4.2.1 Operation Amplifier of the First Stage*

The opamp is one of the most important circuits in sigma-delta modulator. Different opamp architectures are adaptable for different applications. For low voltage design and medium speed modulator, we choose the folded cascode opamp topology. In order to resist the device variation, PMOS input pair is used. Fig. 5.17 shows the circuits of the opamp and CMFB [9].

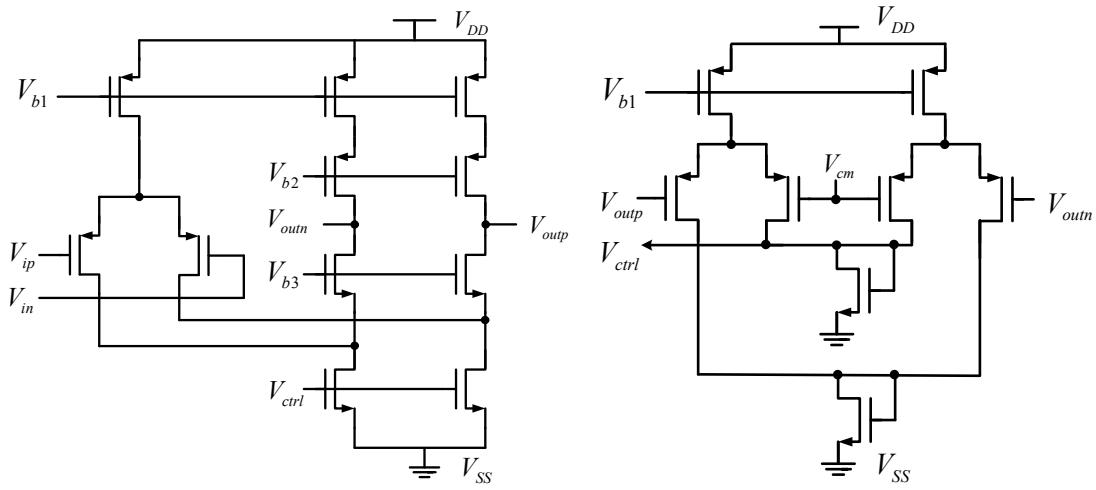



Fig. 5.17 Operation amplifier and CMFB of the first stage

In our opamp design, the DC gain can be expressed as [18]

$$\begin{aligned} |A_v| &= G_m \times R_{out} \\ &\approx g_{m,input} \times \left\{ \left[ (g_{m,PMOS} + g_{mb,PMOS}) r_{o,PMOS}^2 \right] \| \left[ (g_{m,NMOS} + g_{mb,NMOS}) r_{o,NMOS}^2 \right] \right\} \end{aligned} \tag{5.10}$$

where $R_{out}$ is the output resistance. Since folded cascode opamp is single-stage topology, the second pole is far away from the unity-gain frequency. Therefore, the frequency response of the opamp can be derived by

$$A(s) = \frac{g_{m,input} R_{out}}{1 + sR_{out} C_L} \tag{5.11}$$

where $C_L$ is the loading capacitance. For high frequency response ($sR_{out}C_L \gg 1$), it can be simplified as follows

$$A(s) = \frac{g_{m,input}}{sC_L} \tag{5.12}$$

So, we can get the unity-gain frequency as

$$\omega_u = \frac{g_{m,input}}{C_L} \tag{5.13}$$

Fig. 5.18 shows the AC simulation results in TT, FF and SS corner. The design considerations are according to the behavior model simulation in section 5.4.1. The

performance of the folded cascode opamp is summarized in Table 5.4.

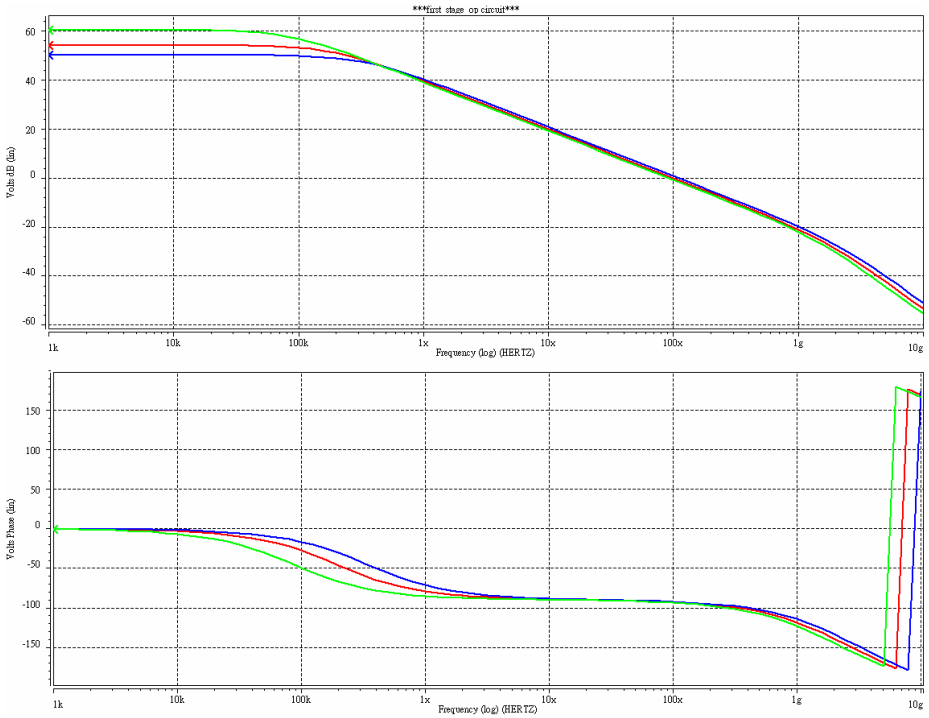



Fig. 5.18 Frequency response of the first stage opamp

Table 5.4 Performance of the first stage opamp

| Simulation Results | Red Line TT @ 50°C | Blue Line FF @ 0°C | Green Line SS @ 100°C |
|---|---|---|---|
| **Differential Gain** | 54.29 dB | 50.26 dB | 60.55 dB |
| **Phase Margin** | 87.11° | 87.4° | 86.74° |
| **Unity-Gain Frequency (3.5p)** | 99.1 MHz | 110.7 MHz | 92.22 MHz |
| **Output Swing** | 1V | | |
| **Power Dissipation** | 1.13mW | | |

### *5.4.2.2 Operation Amplifier of the Second Stage*

In the hybrid modulator, the second stage is DT operation. Because of the same reason introduced in last subsection, the architecture of the second stage also uses folded cascode. For the settling issues, we choose the NMOS input pair to achieve higher bandwidth. Fig. 5.19 shows the circuit of the opamp and dynamic CMFB [17].

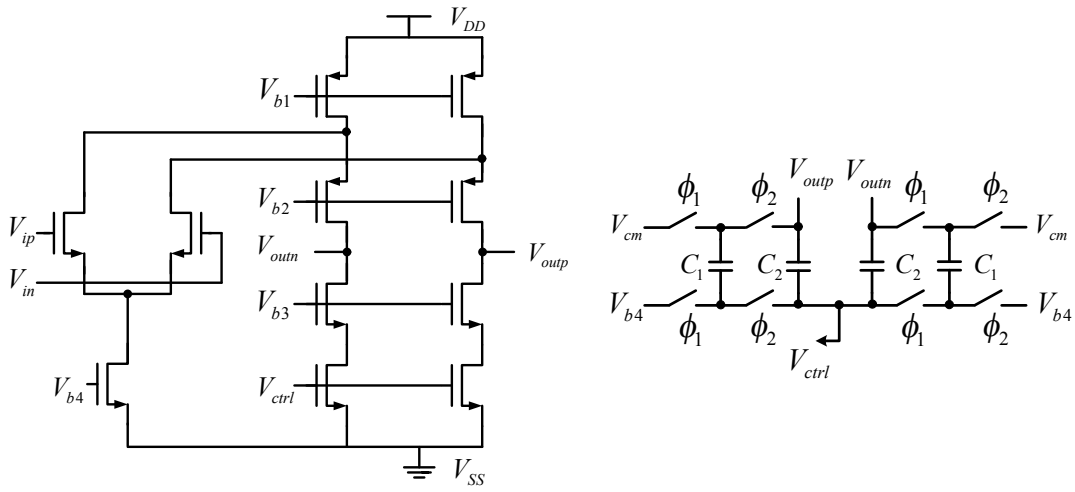



Fig. 5.19 Operation amplifier and CMFB of the second stage

In the dynamic CMFB, $\phi_1$ and $\phi_2$ are non-overlapping clock. If the $\phi_2$ controlled switches connected to the output of the opamp, $V_{outp}$ and $V_{outn}$, are transmission gates, the circuit can provide balancing from $VDD$ to ground [17].

The frequency responses of the second stage opamp in TT, FF and SS corner are shown in Fig. 5.20 and its performance is summarized in Table 5.5.

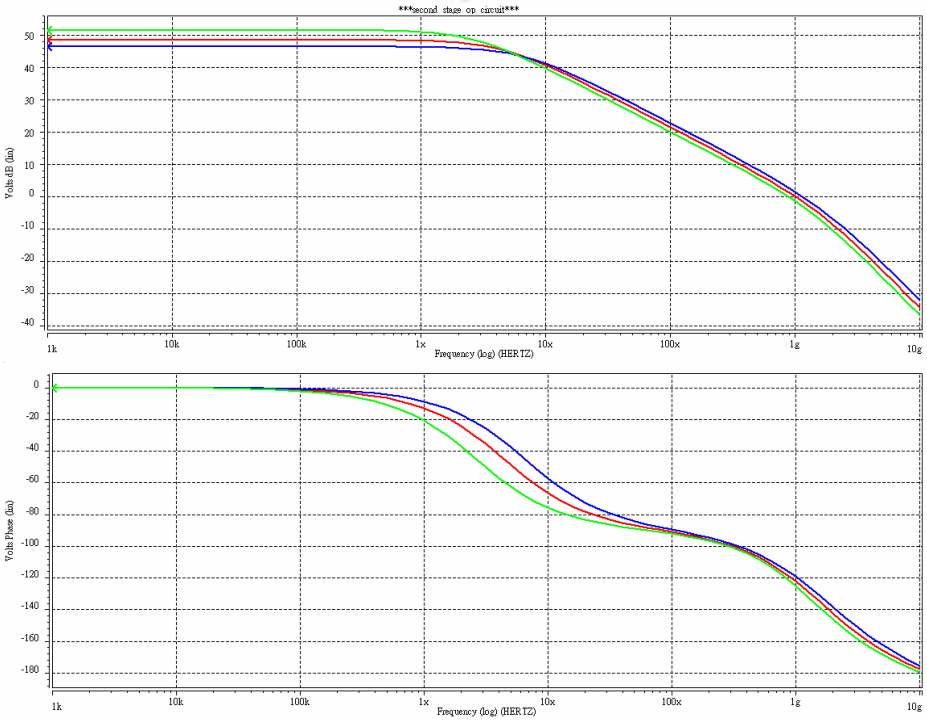



Fig. 5.20 Frequency response of the second stage opamp

Table 5.5 Performance of the second stage opamp

| Simulation Results | Red Line TT @ 50°C | Blue Line FF @ 0°C | Green Line SS @ 100°C |
|---|---|---|---|
| **Differential Gain** | 48.51dB | 46.44 dB | 51.6 dB |
| **Phase Margin** | 57.7° | 57.21° | 58.36° |
| **Unity-Gain Frequency (0.1p)** | 1.01 GHz | 1.16 GHz | 890.8 MHz |
| **Output Swing** | 1V | | |
| **Power Dissipation** | 2.2mW | | |

### *5.4.2.3 17-level Quantizer*

The 17-level quantizer is composed of 16 comparators shown in Fig. 5.21. Fig. 5.21 (a) is a differential-difference preamplifier and Fig. 5.21 (b) is a low-offset regenerative latch introduced in section 4.4.3 [15]. In Fig. 5.21 (a), if we assume that

$$V_{ip} = +\Delta V_i + V_{cmi},\ V_{in} = -\Delta V_i + V_{cmi}\ \text{and}\ V_{refp} = +\Delta V_r + V_{cmr},\ V_{refn} = -\Delta V_r + V_{cmr} \quad (5.14)$$

then

$$\begin{aligned} I_o = I_{o+} - I_{o-} &= G_{m1}\left[(+\Delta V_i + V_{cmi}) - (+\Delta V_r + V_{cmr})\right] - G_{m2}\left[(-\Delta V_i + V_{cmi}) - (-\Delta V_r + V_{cmr})\right] \\ &= (G_{m1} + G_{m2})\cdot(\Delta V_i - \Delta V_r) + (G_{m1} - G_{m2})\cdot(V_{cmi} - V_{cmr}) \end{aligned} \quad (5.15)$$

Therefore, it can reduce the offset by matched source-coupled pairs or matched common-mode voltage.

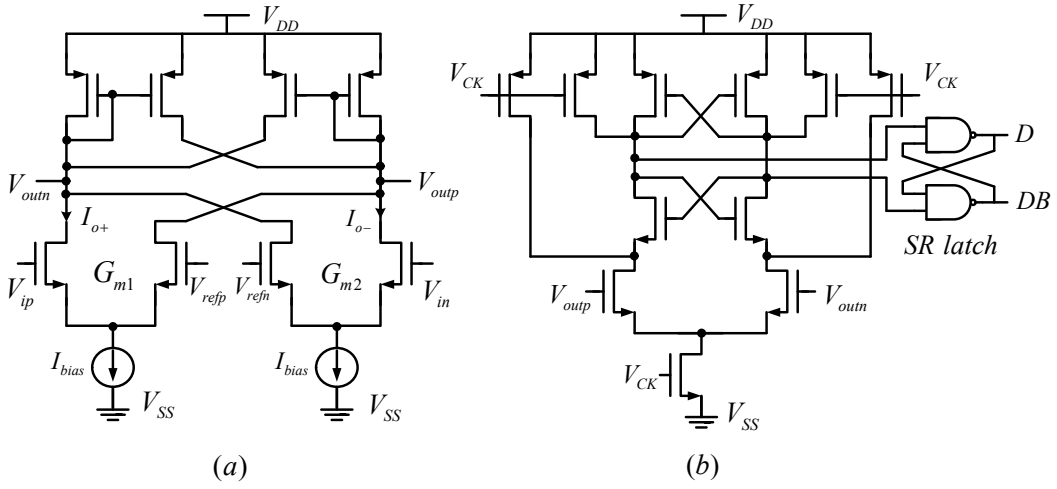



Fig. 5.21 (a) Differential-difference preamplifier (b) Low-offset regenerative latch

The architecture of the 17-level quantizer is shown in Fig. 5.22 (a) and the threshold levels are provided by the resister ladder. It can be shown that the i[th] threshold level is expressed as

$$V_{th,i} = \frac{V_{refp} - V_{refn}}{16} \cdot (2i - 16 - 1) \tag{5.16}$$

Fig. 5.22 (b) shows the analysis of the 17-level quantizer in the time-domain. The first row is the input sine wave and the others in sequence are $D_{16}$ (MSB, most significant bit), $D_{15}$ and so on. When the input sine wave exceeds the threshold levels, the output code is high and vice versa.

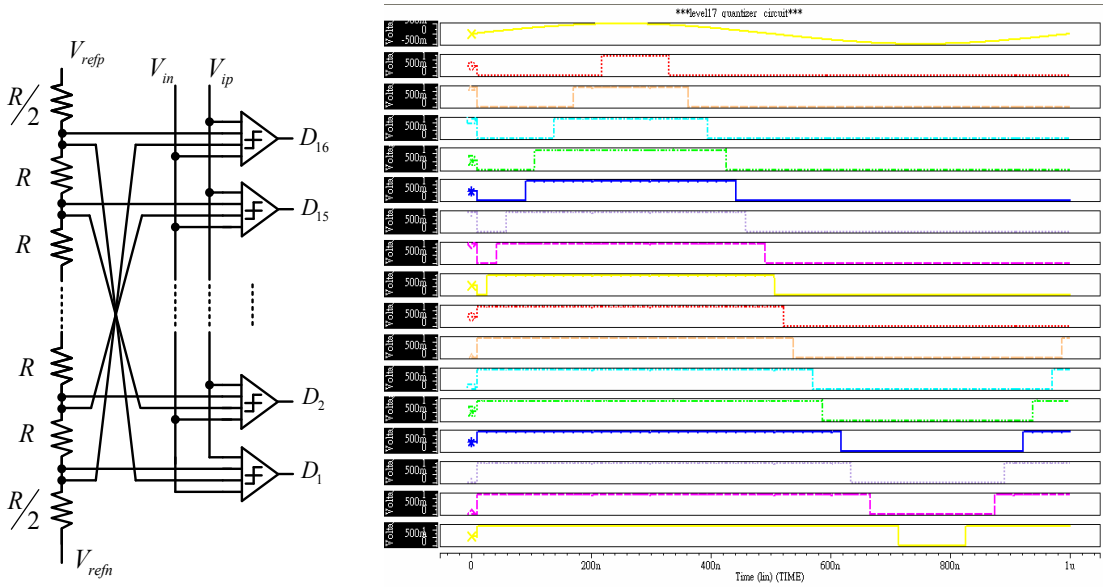



Fig. 5.22 (a) 17-level quantizer (b) Simulation result in time-domain

### 5.4.2.4 Clock Generator

Fig. 5.23 shows the circuit diagram to generate clocks in Fig. 5.15. To reduce the effect of the clock jitter, the differential-to-single end converter circuit of Fig. 5.23 (a) described in section 4.4.5 is used [13]. Through the use of the circuit in Fig. 5.23 (b), the non-overlapping clocks are generated, including the advance $\phi_{1a}$ and inverting

$\phi_{1b}$ phases. In order to have the same delay time for $\phi_1$ and $\phi_{1b}$ phases, we adds a non-inverter in front of the $\phi_{1b}$ output to increase the delay time. In the same consideration, the technique is also used in $\phi_2$ and $\phi_{2b}$ phases. Process variations are taken into account in the design and simulations to make sure the timing is always correct. Fig. 5.24 shows the simulation results of the non-overlapping clock generator.

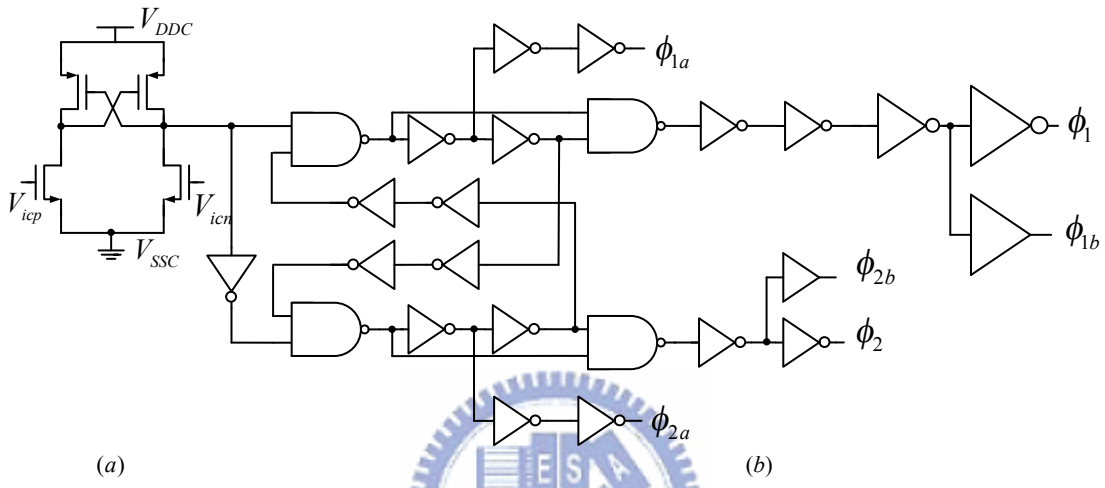



Fig. 5.23 (a) Low-jitter clock generator (b) Non-overlapping clock generator

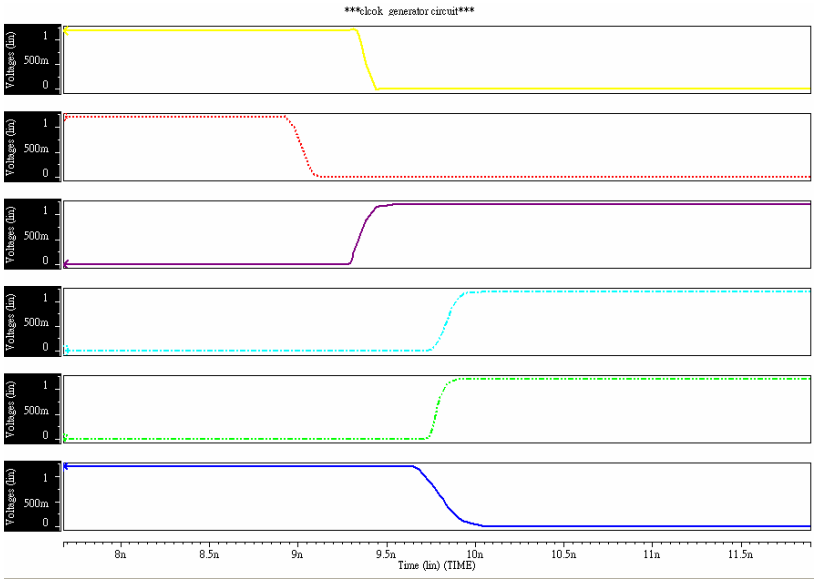



Fig. 5.24 Simulation results of the non-overlapping clock generator

### 5.4.2.5 Tuning Circuit

In section 5.4.1.3, non-ideality of RC variation is introduced and from behavior model simulation, we only allow about ±10% time constant variation to maintain 65dB SNDR performance.

Therefore, in order to achieve 65dB SNDR for applications in wireless communication, the tuning circuit shown in Fig. 5.25 must be needed. For example, in Fig. 5.25 (a), it is an active-RC integrator realized by a tunable capacitor array. In Fig. 5.25 (b), there are an always-in-use capacitor which is 8C and three in-use capacitors which are 1C, 2C and 4C. The normal value of the capacitances is 12C. Through the use of the digital control signals, the minimum and maximum available capacitances are 8C and 15C, respectively. Thereby, the minimum tuning range is from -33% (8C/12C) to +25% (15C/12C) and the tuning resolution is 8.33% (C/12C), where C is the tuning step.

Due to the characteristic of the transfer function scaled with clock frequency in DT modulator, the tuning circuit in the hybrid modulator is modified to add the control signal *Mode* for a multi-standard system design.

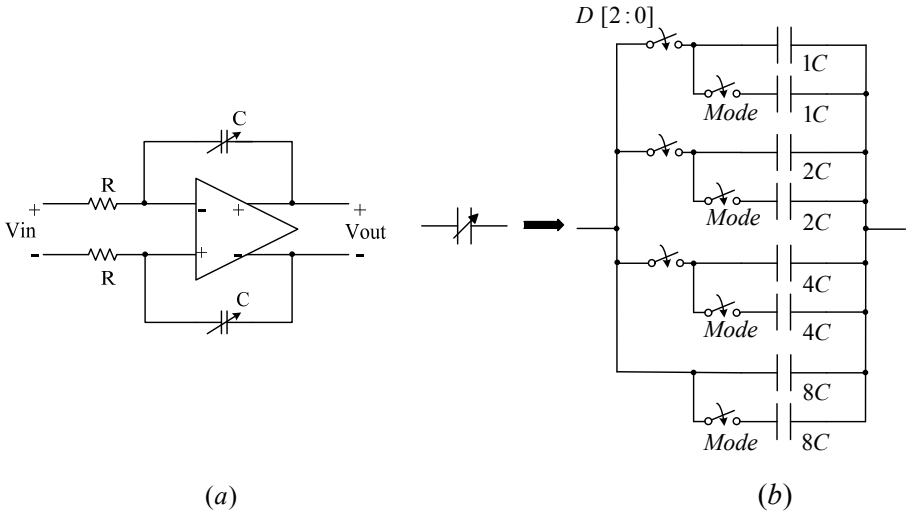



Fig. 5.25 (a) Active-RC integrator (b) Tuning circuit

### 5.4.2.6 Encoder

The outputs of the quantizer are 16-bit thermometer coded signals. Because of the digital processor where we use signed 2's complement representation, we separate the 16-bit thermometer code to two parts which are encoded, respectively and then use a 2:1 MUX to select the correct value. The block diagram shown in Fig. 5.26 is called Wallace-Tree thermometer-to-binary encoder. The encoder counts the number of "1s" in the input signal to realize the conversion. It isn't the fastest solution for thermometer-to-binary conversion but it is the most hardware economic one. Another advantage of the Wallace-Tree encoder is that it can effectively kill the bubbles which may occur at the output of the flash ADC [21]. For example, assuming that the thermometer code is "01011111" with one bubble, the encoder will generate a binary code as "00110" as if the output is "00111111".

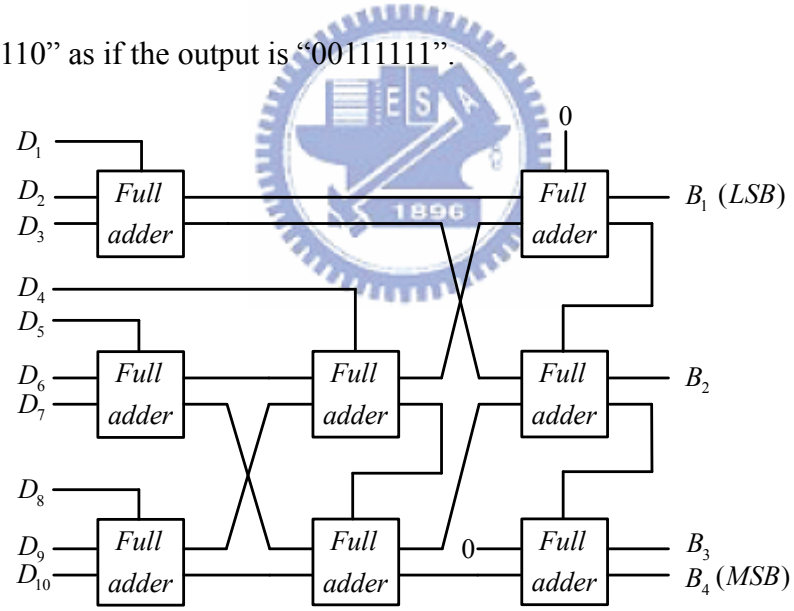



Fig. 5.26 Wallace-Tree encoder

### 5.4.2.7 Adder & DFF

We use signed 2's complement representation to operate the data in digital processor of the Fig. 5.7. It is mainly constructed from digital adders and D flip-flops (DFF). Fig. 5.27 shows the illustrated 3-bit adder with carry lookahead [22]. The

adder is defined two binary variables

$$\begin{aligned} P_i &= A_i \oplus B_i \\ G_i &= A_i B_i \end{aligned} \tag{5.17}$$

The output sum and carry can be expressed as

$$\begin{aligned} S_i &= P_i \oplus G_i \\ C_{i+1} &= G_i + P_i C_i \end{aligned} \tag{5.18}$$

where $G_i$ is called a carry generate and $P_i$ is called a carry propagate. Therefore, we can write the Boolean functions for the carry outputs of each stage and substitute for each $C_i$ as follows

$$\begin{aligned} C_0 &= input\ carry \\ C_1 &= G_0 + P_0 C_0 \\ C_2 &= G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0 \\ C_3 &= G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0 \end{aligned} \tag{5.19}$$

The technique is to increase the hardware complexity in such a way that the carry delay time is reduced.

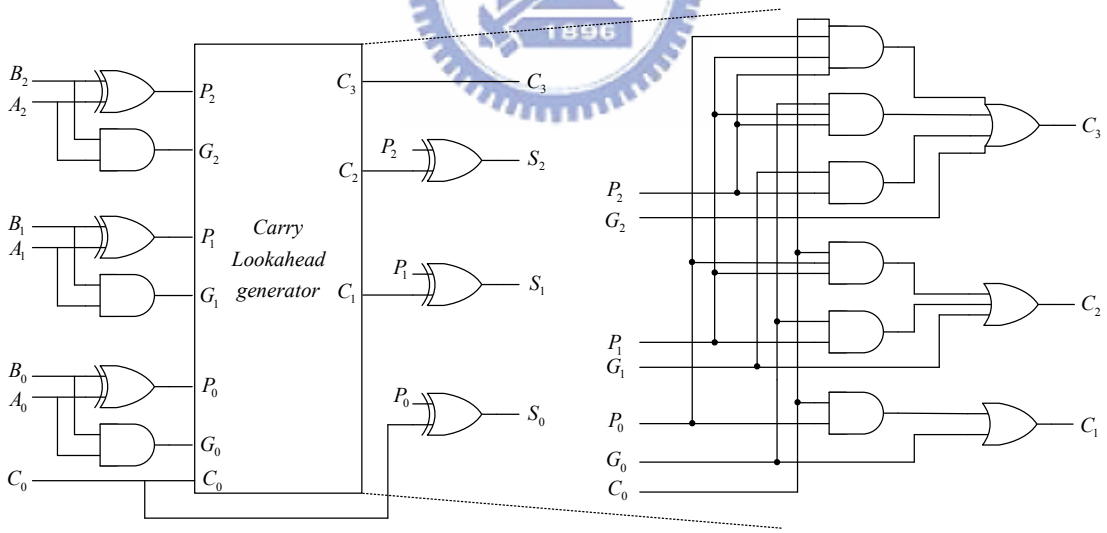



Fig. 5.27 3-bit adder with carry lookahead

The logic diagram of the edge-triggered DFF is shown in Fig. 5.28 [17]. The DFF has clear property and when clear goes to low, the outputs of the NAND go to high. If $T_1$ or $T_2$ is on, the output of DFF is forced to $Q = 0$. The simulated

operation of the edge-triggered DFF is shown in Fig. 5.29. The first row is *clk* and the others in sequence are *clear*, *D* and *Q*.

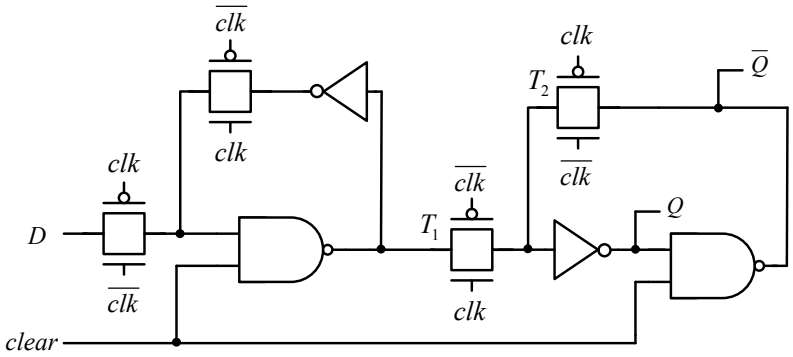



Fig. 5.28 Logic diagram of the DFF

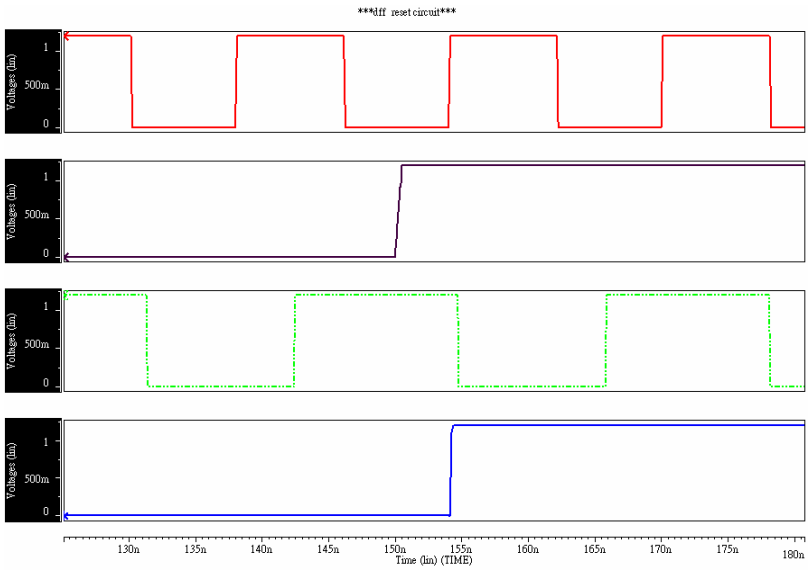



Fig. 5.29 Simulated operation of the edge-triggered DFF

### 5.4.2.8 Simulation Result

The simulated power spectral density of the hybrid sigma-delta modulator with digital error truncation is shown in Fig. 5.30. In Fig. 5.30, the sampling frequency is 62.5MHz and the signal bandwidth is 2MHz. The OSR is equal to 16 and the SNDR is about 60.6dB for -6 dBFS 0.6825MHz input. The power consumption is 12.17mW at 1.2V supply voltage. The performance of this work is summarized in Table 5.6.

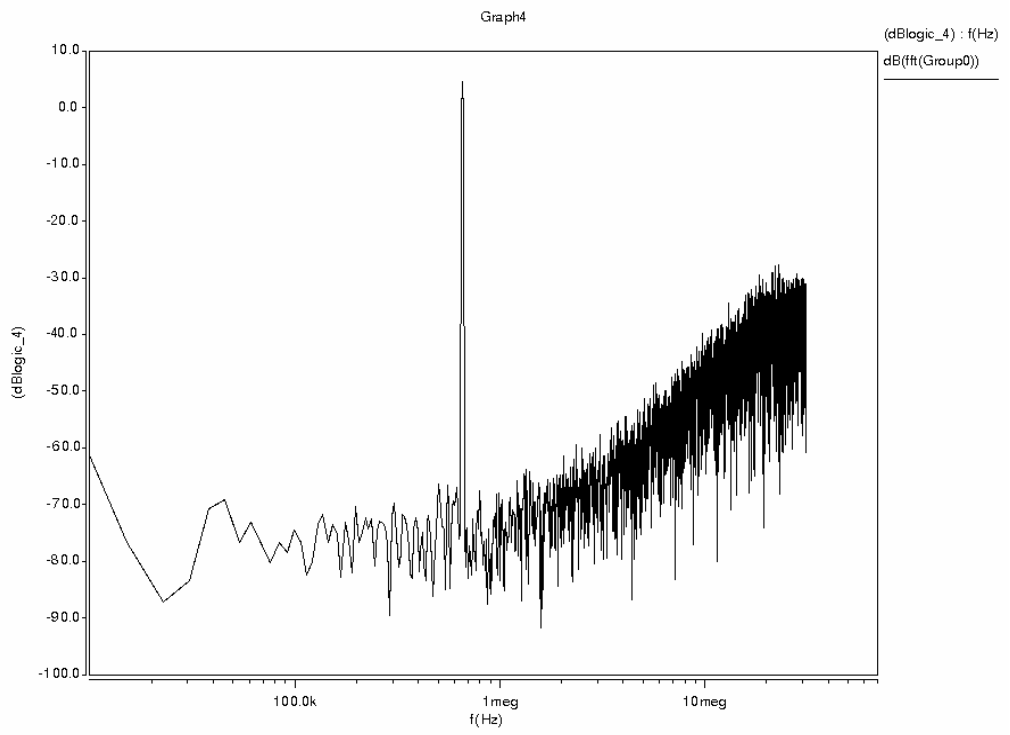


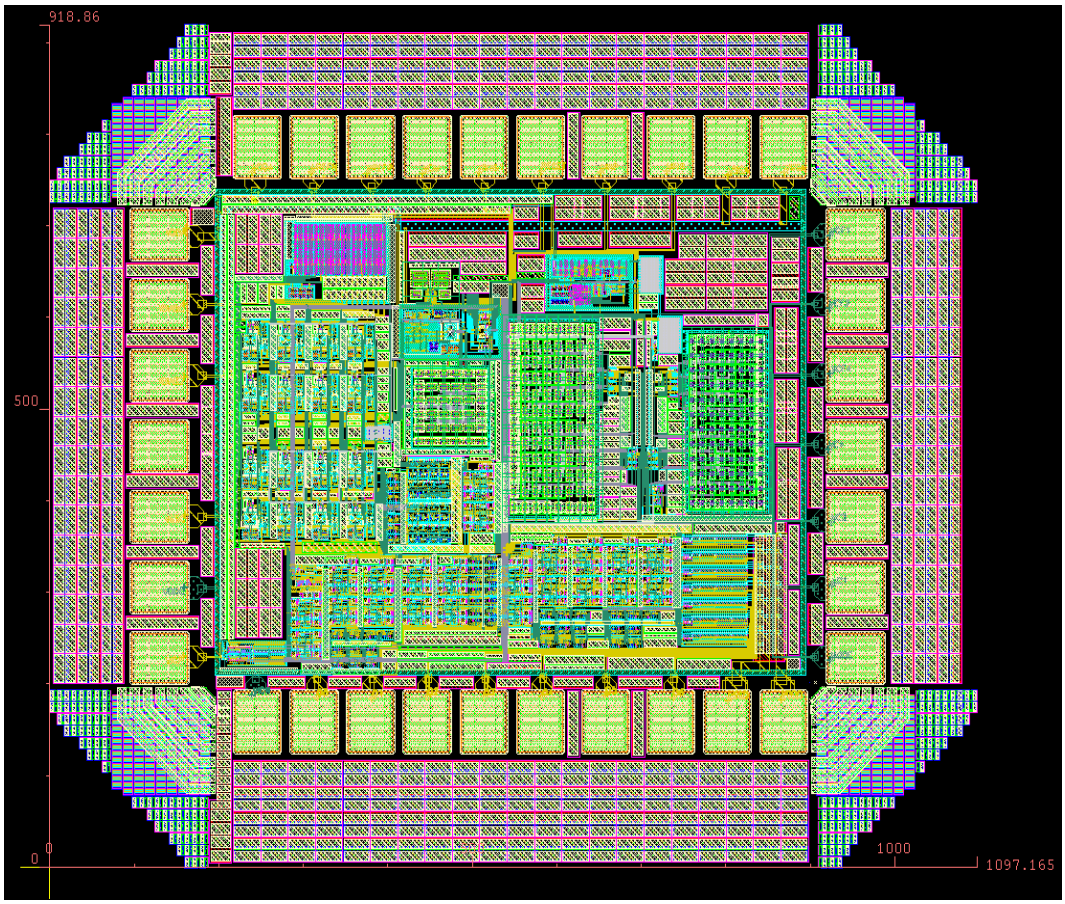

Fig. 5.30 Simulated power spectral density of this work

Table 5.6 Performance summary of this work

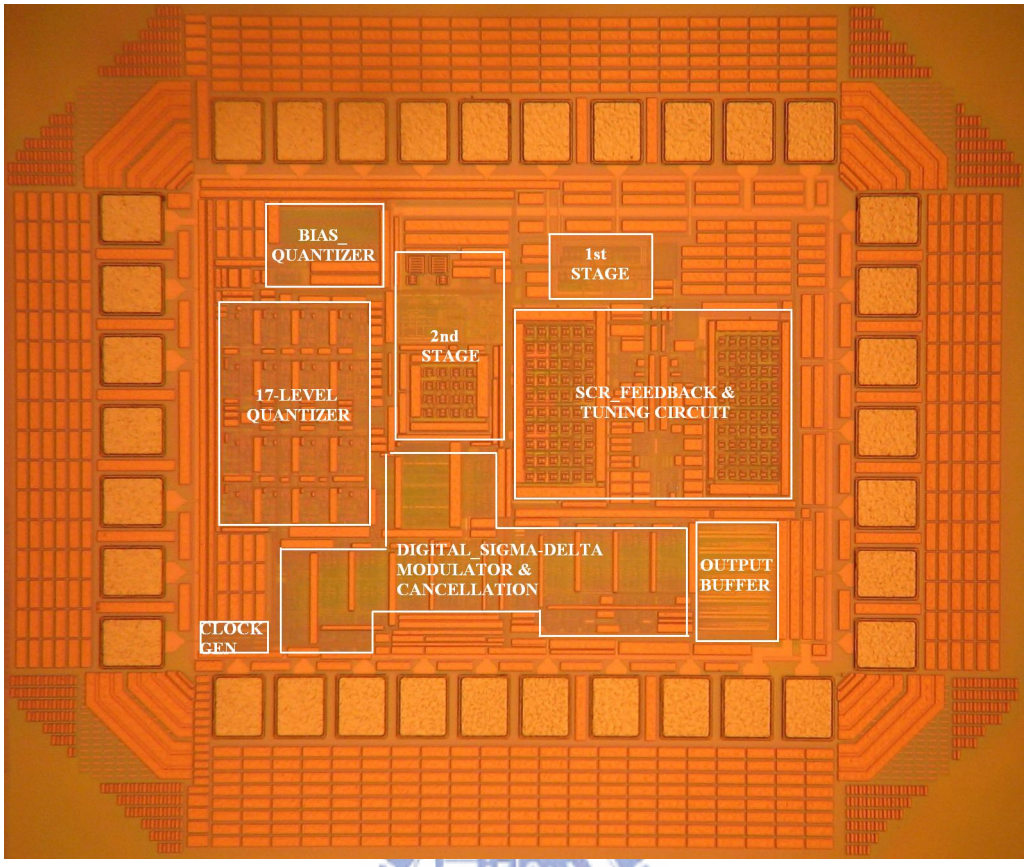
| | |
|---|---|
| **Sampling Frequency** | 62.5MHz |
| **Signal Bandwidth** | 2MHz |
| **SNDR (Fin=0.6825MHz)** | 60.6dB |
| **Power Consumption @1.2V** | 12.17mW |
| **Area (without PAD)** | 0.37mm$^2$ |
| **Technology** | TSMC 0.13μm CMOS |

### 5.4.3 Layout Design

In mixed-signal layout level design, the analog parts are more sensitive to noise than the digital parts. The design considerations and the used techniques are introduced and discussed in chapter 4. The layout design and die photo are shown in Fig. 5.31 and the chip size is 0.698 mm x 0.53 mm without PAD.




(a)




(b)

Fig. 5.31 (a) Layout design (b) Die photo of this work

## 5.5 Summary

A hybrid multi-bit sigma-delta modulator with digital error truncation is designed in TSMC 0.13μm digital CMOS process. The modulator utilizes a continuous-time integrator in the first stage to aim for low power design and embedded anti-aliasing filtering. By using the methodology of truncated error shaping and cancellation, the error levels of the feedback DACs are also truncated while none of them requires DEM to prevent the performance degradation. Additionally, the CT SCR feedback DAC is utilized for tackling the glitch issue of digital processing and also relaxes the excess loop delay and clock jitter problem. The hybrid sigma-delta modulator achieves 60.6dB SNDR and the power consumption is 12.17mW.

# *CHAPTER 6*

# *Test Setup and Measurement Results*

## *6.1 Introduction*

The continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application and the hybrid sigma-delta modulator with digital error truncation have been fabricated by TSMC 0.18μm and TSMC 0.13μm CMOS mixed-signal process, respectively. In this chapter, we present the testing environment, including the components on the printed circuit board (PCB) and instruments. Finally, the measurement results are shown and summarized.

## *6.2 Measuring Environment*

Fig. 6.1 shows the measurement process. We use three power supplies, two function generators, an oscilloscope and a PC for Matlab processing to measure the device under test (DUT). The PCB contains single-to-differential transformers, bias, reference voltage generator and regulators which are analog, digital and clock parts. The separated regulators are supplied by power supplies respectively to isolate noise interference. The input signal and clock are provided by function generator hp 8656B and ROHDE & SCHWARZ SML03 shown in Fig. 6.2 and 6.3. The output waveform can be observed through the use of the oscilloscope and the digital output signals are fed into logic analyzer Agilent 16902A, as shown in Fig. 6.4. The output data are loaded into a PC and then by using Matlab, the power spectral density performance can be obtained.

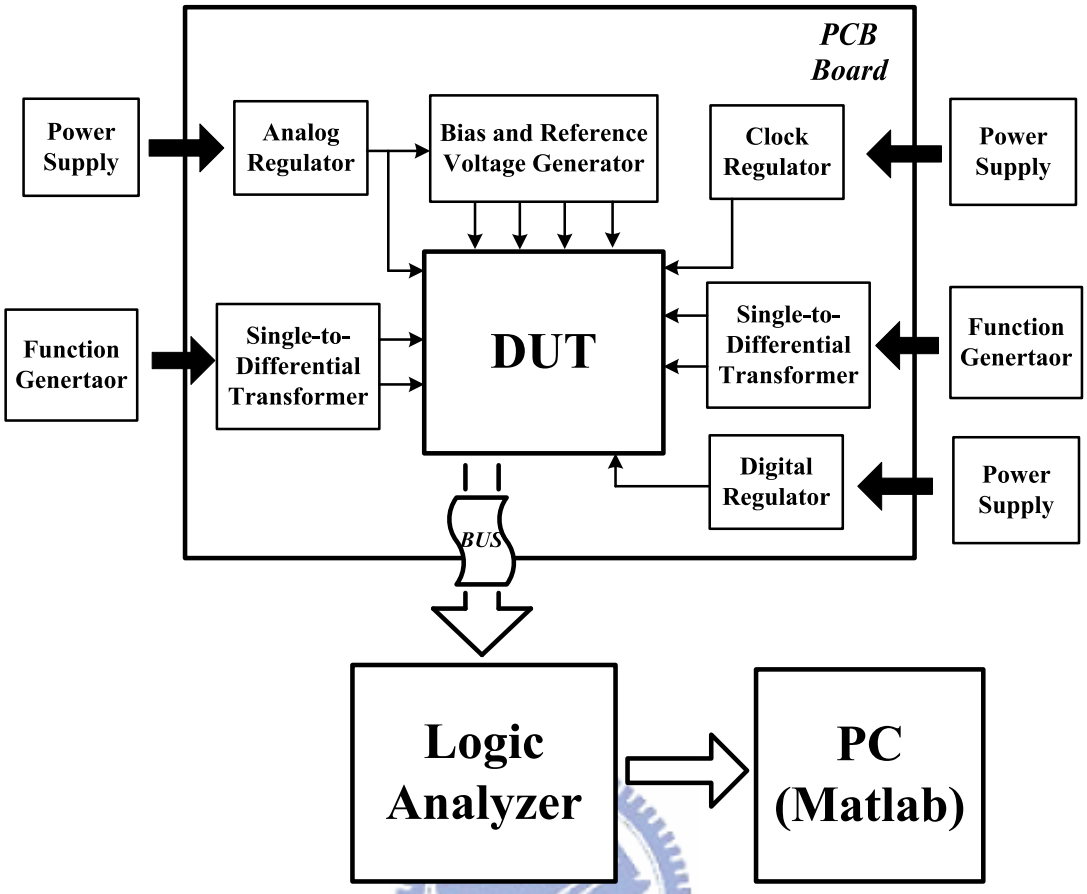



Fig. 6.1 Test setup

Fig. 6.2 Function generator hp 8656B for input signal

Fig. 6.3 Function generator ROHDE & SCHWARZ SML03 for clock

Fig. 6.4 Logic analyzer Agilent 16902A

### 6.2.1 Power Supply Regulator

The supply voltages are generated by LM317 adjustable regulators as shown in Fig. 6.5. The $C_{in}$ is the bypass capacitor and the $C_{out}$ is added to improve the transient response. The $C_{ADJ}$ is used to increase the supply voltage rejection. The regulator provides an internal reference voltage of 1.25V between the output and adjustments. This is used to set a constant current. The output voltage of the regulator can be expressed as [23]

$$V_{out} = 1.25 \cdot (1 + \frac{R_2}{R_1}) + I_{ADJ} \cdot R_2 \qquad (6.1)$$

where $I_{ADJ}$ is the DC current that passes through the variable resistor $R_2$. The device is designed to minimize the term $I_{ADJ}$ and to maintain it very constant with line and load changes.

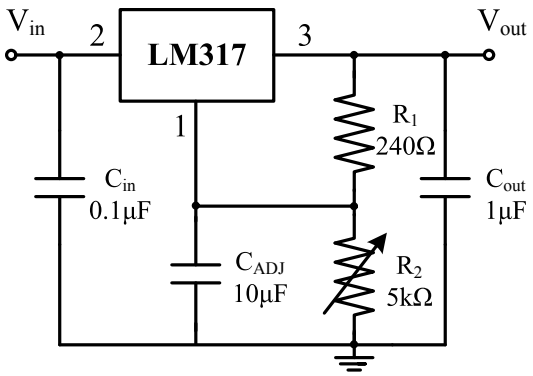



Fig. 6.5 Power supply regulator

### 6.2.2 Single-to-Differential Transformer

In Fig. 6.2 and 6.3, the output signal of the function generators is single-ended and only provides the ac component. Therefore, for our fully differential design, the single-to-differential transformer is needed as shown in Fig 6.6. Through the transformer, the differential output signal can be obtained and by using reference voltage generator, the common-mode voltage $V_{cm}$ can be added to ensure the DC bias. Since the output impendence of the RF terminal is 50Ω, we use two 25Ω-resistors to match the resistance. The capacitor is used to steady the voltage, as the decoupling capacitor.

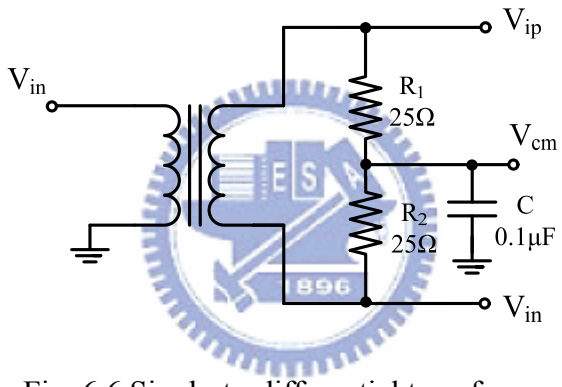



Fig. 6.6 Single-to-differential transformer

### 6.2.3 Reference Voltage Generator

In hybrid sigma-delta modulator with digital error truncation, due to the influence of the loading effect, the reference voltage can be varied to result in errors. Hence, we need to add a buffer to avoid the effect. Fig. 6.7 shows the use of the OP27 operated as the unity-gain buffer. The OP27 is supplied by ±9V voltage.

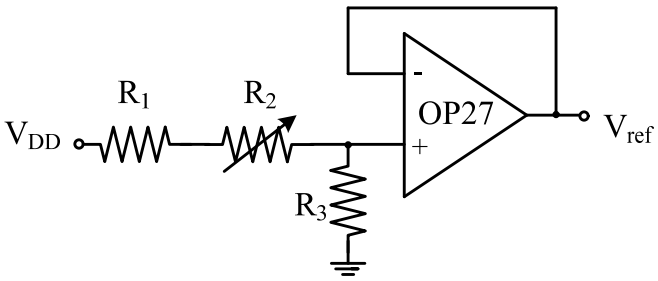



Fig. 6.7 Reference voltage generator

## 6.3 PCB and Pin Configurations

Fig. 6.8 shows the PCB of the continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application. Fig. 6.9 presents the pin configurations and lists the pin assignments of the CT modulator.

Fig. 6.10 shows the PCB of the hybrid sigma-delta modulator with digital error truncation. Fig. 6.11 presents the pin configurations and lists the pin assignments of the hybrid modulator.

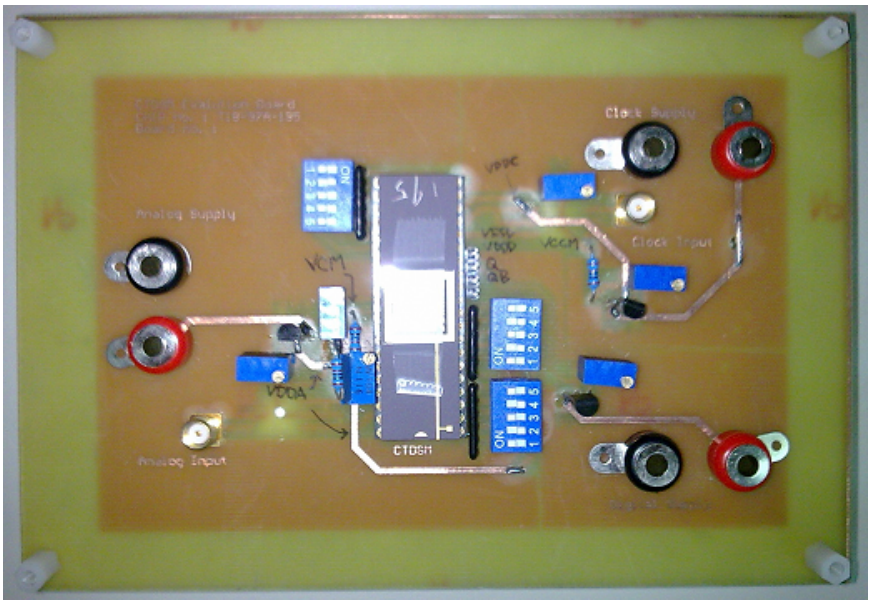
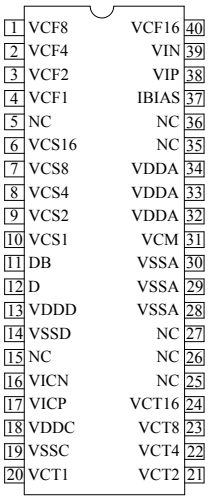



Fig. 6.8 PCB of the CT modulator




| Pin | Name | I/O | Description | Pin | Name | I/O | Description |
|---|---|---|---|---|---|---|---|
| 1 | VCF8 | In | 8C control signal in 1st stage | 21 | VCT2 | In | 2C control signal in 3rd stage |
| 2 | VCF4 | In | 4C control signal in 1st stage | 22 | VCT4 | In | 4C control signal in 3rd stage |
| 3 | VCF2 | In | 2C control signal in 1st stage | 23 | VCT8 | In | 8C control signal in 3rd stage |
| 4 | VCF1 | In | 1C control signal in 1st stage | 24 | VCT16 | In | 16C control signal in 3rd stage |
| 5 | NC | - | No connection | 25 | NC | - | No connection |
| 6 | VCS16 | In | 16C control signal in 2nd stage | 26 | NC | - | No connection |
| 7 | VCS8 | In | 8C control signal in 2nd stage | 27 | NC | - | No connection |
| 8 | VCS4 | In | 4C control signal in 2nd stage | 28 | VSSA | In | Analog ground |
| 9 | VCS2 | In | 2C control signal in 2nd stage | 29 | VSSA | In | Analog ground |
| 10 | VCS1 | In | 1C control signal in 2nd stage | 30 | VSSA | In | Analog ground |
| 11 | DB | Out | Digital output signal (180°) | 31 | VCM | In | Common-mode voltage |
| 12 | D | Out | Digital output signal (0°) | 32 | VDDA | In | Analog power supply |
| 13 | VDDD | In | Digital power supply | 33 | VDDA | In | Analog power supply |
| 14 | VSSD | In | Digital ground | 34 | VDDA | In | Analog power supply |
| 15 | NC | - | No connection | 35 | NC | - | No connection |
| 16 | VICN | In | Clock input signal (180°) | 36 | NC | - | No connection |
| 17 | VICP | In | Clock input signal (0°) | 37 | IBIAS | In | Bias current control |
| 18 | VDDC | In | Clock power supply | 38 | VIP | In | Input signal (0°) |
| 19 | VSSC | In | Clock ground | 39 | VIN | In | Input signal (180°) |
| 20 | VCT1 | In | 1C control signal in 3rd stage | 40 | VCF16 | In | 16C control signal in 1st stage |

Fig. 6.9 (a) Pin configurations (b) Pin assignments of the CT modulator

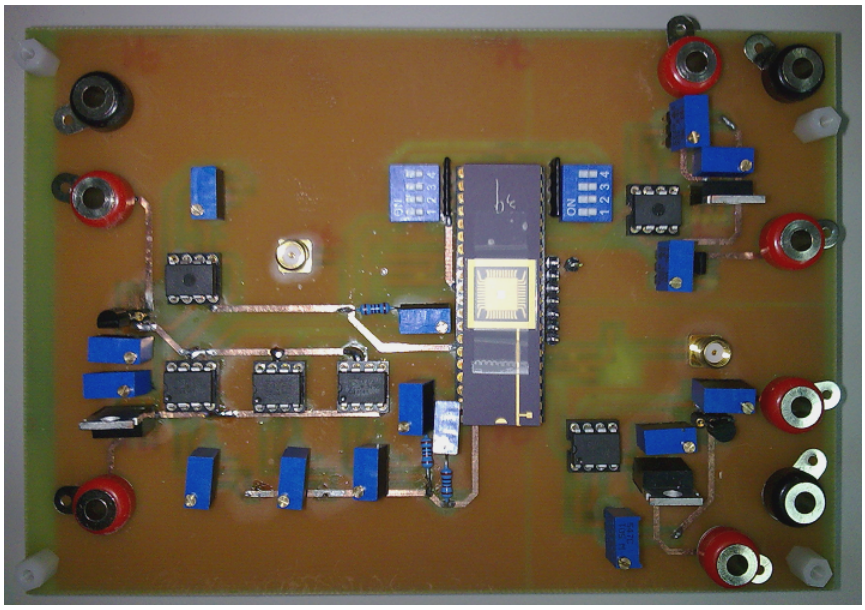
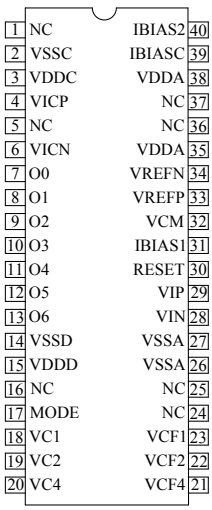


Fig. 6.10 PCB of the hybrid modulator




| Pin | Name | I/O | Description | Pin | Name | I/O | Description |
|---|---|---|---|---|---|---|---|
| 1 | VCF8 | In | 8C control signal in 1st stage | 21 | VCT2 | In | 2C control signal in 3rd stage |
| 2 | VCF4 | In | 4C control signal in 1st stage | 22 | VCT4 | In | 4C control signal in 3rd stage |
| 3 | VCF2 | In | 2C control signal in 1st stage | 23 | VCT8 | In | 8C control signal in 3rd stage |
| 4 | VCF1 | In | 1C control signal in 1st stage | 24 | VCT16 | In | 16C control signal in 3rd stage |
| 5 | NC | - | No connection | 25 | NC | - | No connection |
| 6 | VCS16 | In | 16C control signal in 2nd stage | 26 | NC | - | No connection |
| 7 | VCS8 | In | 8C control signal in 2nd stage | 27 | NC | - | No connection |
| 8 | VCS4 | In | 4C control signal in 2nd stage | 28 | VSSA | In | Analog ground |
| 9 | VCS2 | In | 2C control signal in 2nd stage | 29 | VSSA | In | Analog ground |
| 10 | VCS1 | In | 1C control signal in 2nd stage | 30 | VSSA | In | Analog ground |
| 11 | DB | Out | Digital output signal (180°) | 31 | VCM | In | Common-mode voltage |
| 12 | D | Out | Digital output signal (0°) | 32 | VDDA | In | Analog power supply |
| 13 | VDDD | In | Digital power supply | 33 | VDDA | In | Analog power supply |
| 14 | VSSD | In | Digital ground | 34 | VDDA | In | Analog power supply |
| 15 | NC | - | No connection | 35 | NC | - | No connection |
| 16 | VICN | In | Clock input signal (180°) | 36 | NC | - | No connection |
| 17 | VICP | In | Clock input signal (0°) | 37 | IBIAS | In | Bias current control |
| 18 | VDDC | In | Clock power supply | 38 | VIP | In | Input signal (0°) |
| 19 | VSSC | In | Clock ground | 39 | VIN | In | Input signal (180°) |
| 20 | VCT1 | In | 1C control signal in 3rd stage | 40 | VCF16 | In | 16C control signal in 1st stage |

Fig. 6.11 (a) Pin configurations (b) Pin assignments of the hybrid modulator

## 6.4 Measurement Results

### 6.4.1 A Continuous-Time Single-Bit Active-RC Sigma-Delta Modulator for Bluetooth

The continuous-time single-bit active-RC sigma-delta modulator for Bluetooth application has been fabricated by TSMC 0.18μm CMOS mixed-signal process. It is supplied by the 1.8V output of the regulator. The input sine wave is 0.798MHz and the sampling frequency is 100MHz. The signal bandwidth is 1MHz and the oversampling ratio is equal to 50. The output data of the modulator are saved through the logic analyzer. By using Matlab in a PC to do fast Fourier transformation with 65536 points, the power spectral density can be obtained as shown in Fig. 6.12. The SNDR is about 56.8dB for -5.04 dBFS input and the ENOB is 9.14bits. Fig. 6.13 is the post-simulation power spectral density and the SNDR is 65.5dB. Fig. 6.14 shows the dynamic range plot which is the SNDR versus the normalized input level. The measured power consumption is 22.2mW at 1.8V supply voltage. The performance of this CT modulator is summarized in Table 6.1.

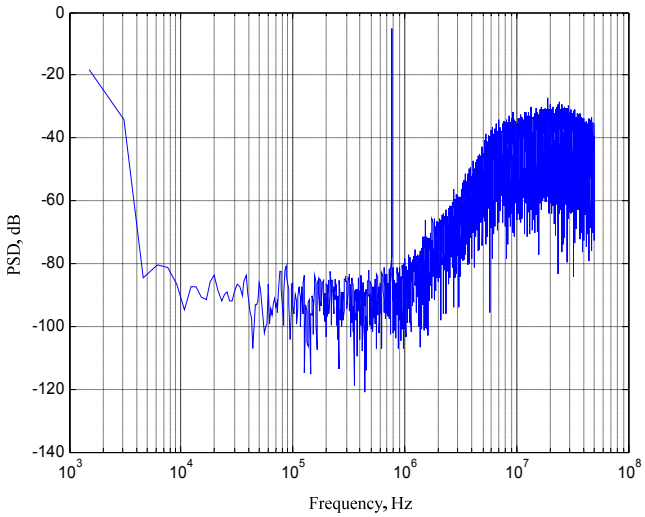



Fig. 6.12 Measured power spectral density of the CT modulator

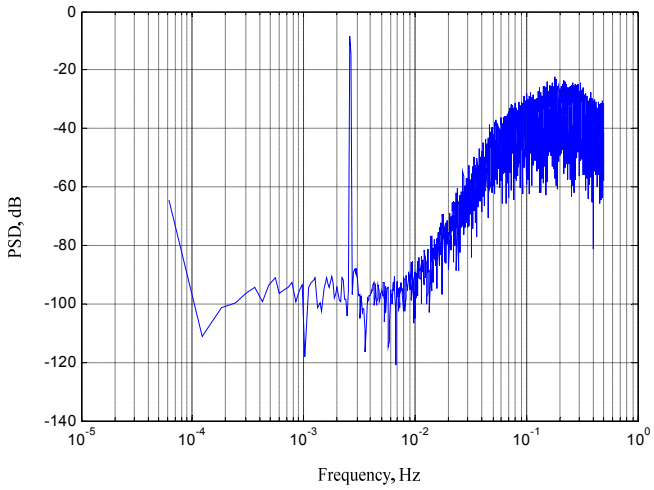



Fig. 6.13 Post-simulation power spectral density of the CT modulator

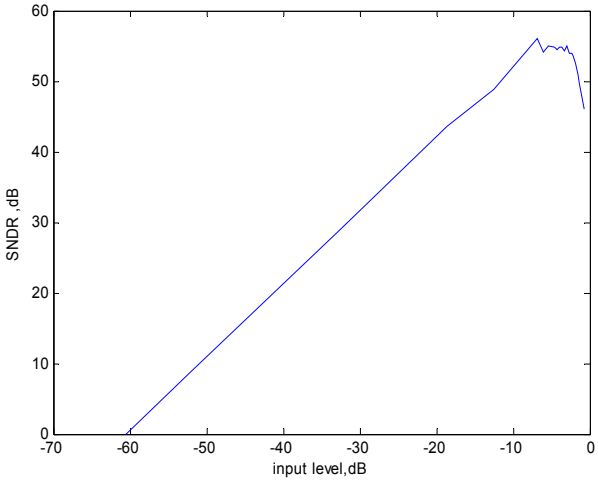



Fig. 6.14 Dynamic range plot of the CT modualtor

Table 6.1 Measurement results of the CT modulator

| **Parameters** | **Measurement Results** |
|---|---|
| Technology | TSMC 0.18μm process |
| Power Supply | 1.8V |
| Sampling Frequency | 100MHz |
| Signal Bandwidth | 1MHz |
| SNDR | 56.8dB |
| ENOB | 9.14bits |
| Dynamic Range | 60dB |
| Area | 1.32mm x 1.23mm |
| Power Consumption | 22.2mW |

### 6.4.2 Hybrid Sigma-Delta Modulator with Digital Error Truncation

The hybrid sigma-delta modulator with digital error truncation has been fabricated by TSMC 0.13μm CMOS mixed-signal process. It is supplied by the 1.2V output of the regulator. The input sine wave is 0.3786MHz and the sampling frequency is 62.5MHz. The signal bandwidth is 2MHz and the oversampling ratio is equal to 16. The output data of the modulator are saved through the logic analyzer. By using Matlab in a PC to do fast Fourier transformation with 65536 points, the power spectral density can be obtained as shown in Fig. 6.15.

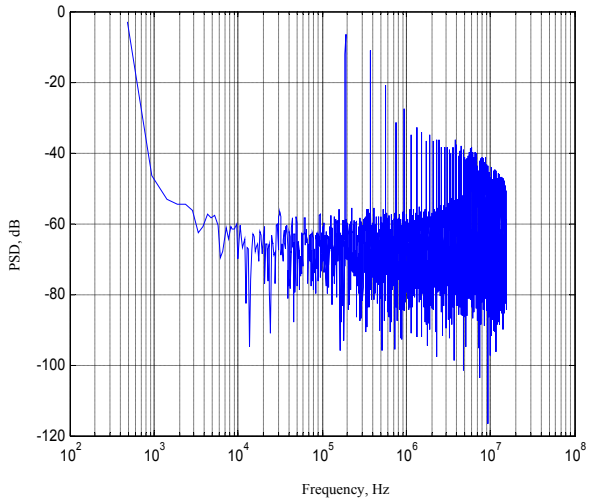



Fig. 6.15 Measured power spectral density of the hybrid modulator

## 6.5 Summary

In the CT modulator, the SNDR performance between the measurement result and post-simulation has about 10dB decay. The possible reason is that the signal isolation is not good enough. When the high frequency clock function generator is

attached to the PCB, the power supply and reference voltage of the analog and digital parts suffers the influence to vibrate slightly. For the solution, it perhaps decreases the path from the BNC to chip and increases the distance from BNC to others in order to reduce the effect. Table 6.2 lists the comparison between previously reported DT SDM and the CT modulator. The FOM is described as follows

$$FOM = \frac{Power}{2 \cdot BW \cdot 2^{((SNDR-1.76)/6.02)}} \tag{6.2}$$

Table 6.2 Comparison between DT SDM and the CT modulator

| Reference | Architecture | SNDR (dB) | BW (MHz) | $F_s$ (MHz) | Process | Power (mW) | FOM (pJ/conv.) |
|---|---|---|---|---|---|---|---|
| [24] | 2-2 MASH | 72 | 1.1 | 52.5 | 0.35 $\mu$m | 187 | 26.26 |
| [24] | 2-2-2 MASH | 79 | 1.1 | 52.5 | 0.35 $\mu$m | 248 | 15.48 |
| This work Post-simulation | 3rd-order | 65.5 | 1 | 100 | 0.18 $\mu$m | 21.9 | 7.11 |
| This work Measurement result | 3rd-order | 56.8 | 1 | 100 | 0.18 $\mu$m | 22.2 | 19.6 |

In the hybrid modulator, according to Fig. 6.15, the measurement result presents the modulator is not function work. A possible reason is that the RC variation of the SCR feedback results from the process. This variation causes the deviation of the feedback time constant so that the scaling relationship between the first and feedback coefficients is broken. This problem would make the data of the digital processor exceed the FS. Therefore, the data are unable to express in 2's complement representation. Probably, this error would make the modulator unstable.

# *CHAPTER 7*
# *Conclusions and Future Works*

## *7.1 Conclusions*

The continuous-time third-order single-bit sigma-delta modulator for Bluetooth application has been implemented. The CT modulator utilizes CRFB architecture to improve signal bandwidth and we use active-RC integrators in order to have better linearity. However, the active-RC integrators need an additional output buffer to avoid loading effect which increases the power consumption. For reducing the influence of the clock jitter, the feedback DAC shape is realized by NRZ.

The chip has been fabricated by TSMC 0.18μm CMOS mixed-signal process. The sampling frequency is 100MHz and the signal bandwidth is 1MHz. the CT modulator achieves 56.8dB SDNR performance and 60dB dynamic range for Bluetooth application. The measured power consumption is about 22.2mW at 1.8V supply.

The hybrid sigma-delta modulator with digital error truncation has been implemented. The modulator not only has embedded anti-aliasing filtering and low power design which are the characteristics of the CT modulator but also keeps the high accurate transfer functions and arbitrary scaled clock frequency for a multi-standard system which are the advantages of the DT modulator. By applying the truncation error shaping and cancellation, the linearity of the feedback DAC can become better. Additionally, the CT SCR feedback DAC is utilized for tackling the glitch issue of digital processing and also relaxes clock jitter problem.

## 7.2 Future Works

For the design of the sigma-delta modulator, the dynamic range mainly depends on three factors: oversampling ratio, the order of the modulator and quantizer resolution. For wideband communication system applications, it is impossible to enhance the dynamic range by increasing the oversampling ratio. On the contrary, the others can be increased to achieve the objective.

In the hybrid sigma-delta modulator, the truncation error shaping and cancellation techniques are applied to the second-order loop filter. If we could apply the techniques to higher order sigma-delta modulator, the linearity of the feedback DAC can be maintained and the modulator can also achieve higher order noise shaping and performance. Besides, through the use of these techniques, we could further increase the resolution of the quantizer to obtain better dynamic range.

In the digital processor, we could use error feedback structure to implement the digital sigma-delta modulator. The advantages are that the digital hardware and the digital processing time can be decreased due to the reduction of the digital adders. Therefore, the effect of excess loop delay can be relaxed.

For above discussion, several design issues can be further explored to achieve wider signal bandwidth with high resolution in the future.

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