國 立 交 通 大 學

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碩 士 論 文

應用半均等量化及改良式延遲時間補償連續時間之三角積分調變器

A Continuous-Time DSM Using Improved Zero-Order loop Compensation with Semi-Uniform Quantization

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中 華 民 國 九十七 年 九 月

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摘　　要

隨著無線通訊的蓬勃發展，應用於無線通訊中的類比數位轉換器也受到更多的矚目。在所有的類比數位轉換器的架構中，三角積分（Delta-sigma）類比數位轉換器優於快閃（Flash）和導管式（Pipeline）類比數位轉換器的地方，在於擁有較佳的頻寬和解析度的經濟效益。近年來，由於有著更低的功率消耗及較大的訊號頻寬，連續時間三角積分類比數位轉換器比起離散時間三角積分類比數位轉換器更為廣泛應用於無線通訊中。

在此篇論文中，我們著重於連續時間三角積分調變器的設計概念，且實現一 1 MHz 訊號頻寬，並具有 60 dB 動態範圍（Dynamic Range）及最大訊號雜訊失真比（SNDR）為 59.6 dB 的電路，此電路使用電阻取代原先轉導當作零點轉移的功用，以節省面積和功率。此外，我們也提出另一架構，此電路具有 2MHz 的訊號頻寬及最大訊號雜訊失真比 63 dB 且使用改良式延遲時間補償及半均等量化的技巧來節省面積和功率。

晶片分別以台積電 180 奈米互補式金氧半導體製程及 130 奈米互補式金氧半導體製程所製造。量測結果顯示第一顆晶片操作在 100 MHz 取樣頻率下，消

耗 13.7 mW 的功率在 1.8 V 的供應電壓下。模擬結果顯示另一顆晶片操作在 62.5 MHz 取樣頻率下，消耗 10 mW 的功率在 1.2 V 的供應電壓下。

A Continuous-Time DSM Using Improved Zero-Order loop Compensation with Semi-Uniform Quantization

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ABSTRACT

With the growth of wireless communication, there has been more focus on the analog-to-digital converter (ADC) for wireless applications. Among all of ADCs, delta-sigma converters are preferable over flash and pipeline converters because they offer the most economic bandwidth and accuracy trade-off. Recently, continuous-time delta-sigma ADCs get growing interests in wireless applications for their lower power consumption and wider bandwidth as compared with the discrete-time counterparts.

In this thesis, it focuses on the design procedure of the continuous-time delta-sigma modulator and the first chip is presented to achieve 60 dB dynamic range and 59.6 dB SNDR within a 1MHz signal bandwidth. This work replaces the transconductor with resistors as the function of zero shifts to save chip area and power consumption. Besides, we also show the other architecture to achieve 63 dB SNDR within a 2MHz signal bandwidth and this work uses the techniques of improved zero-order loop compensation and semi-uniform quantization to save chip

area and power consumption.

The first chip has been fabricated by TSMC 180 nm CMOS process and the other has been fabricated by TSMC 130 nm CMOS process. The test results show that the first work consumes 13.7 mW with 100 MHz sample rate in 1.8 V supply voltage. The simulation results show that the other work consumes 10 mW with 62.5 MHz sample rate in 1.2 V supply voltage.

誌　　謝

隨著這份碩士論文的完成，兩年來在交大的求學生涯也跟著告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，最先要感謝的，當然是我的指導教授洪崇智老師。這兩年的研究生涯中，給予我無微不至的指導與照顧，且讓我在研究主題上有無限的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝李育民教授和溫宏斌教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

另一方面，要感謝所有類比積體電路實驗室的成員兩年來的互相照顧與扶持。首先，感謝博士班的學長薛文弘、羅天佑、黃哲揚以及已畢業的碩士班學長白逸維、林明澤、高正昇、邱建豪、吳國璽和廖德文在研究上所給予我的幫助與鼓勵。特別是文弘學長，由於他平時不吝惜的賜教與量測晶片時給予的幫助，使得我的論文研究得以順利完成，對於他的無私幫助，我沒齒難忘。另外我要感謝郭智龍、夏竹緯、楊文霖、邱楓翔、黃介仁和張維欣等諸位同窗，透過平日與你們的切磋討論，使我不論在課業上，或研究上都得到了不少收穫。尤其是工四718實驗室的同學們，兩年來陪我一塊兒努力奮鬥，一起渡過那段同甘共苦的日子，也因為你們，讓我的碩士班生活更加多采多姿，增添許多快樂與充實的回憶。此外也感謝學弟們李尚勳、黃聖文、許新傑和簡兆良的熱情支持，因為你們的加入，讓實驗室注入一股新的活力與朝氣，我祝你們研究順利。

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林永洲 于 交通大學工程四館 718 實驗室

2008.9.05

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Chapter 1

Introduction

1.1 Motivation

Delta-Sigma AD converters can achieve both high resolution and high linearity for low bandwidth applications, such as audio signal processing. Among all the ΔΣ converters (discrete-time (DT) and continuous-time (CT)), DT modulators are less suitable for high speed conversions. Because of the settling time requirement for the charge transfer between the switched-capacitor integrators, it boosts its power consumption. Therefore, they are used for low bandwidth applications. On the contrary, the sampling speed in CT isn't limited by any settling requirements. Besides, there is no need for sample-and-hold circuit in the front-end and benefit from having inherent anti-aliasing filter. This leads to lower power consumption and less chip area. However, CT modulators suffer from the severe process-varying RC time constant, excess loop delay and clock jitter issues which require extra care.

As the IC technologies advanced, it resulted in lower power supply voltages, which caused the input range of the transconductor decrease and made the dynamic range of ΔΣ modulators decrease sorely, as presented in Fig. 1.1. To overcome this problem, improved ΔΣ modulator architecture is proposed. This architecture achieves high out of-band gain and use improved zero-order loop compensation with semi-uniform quantization.

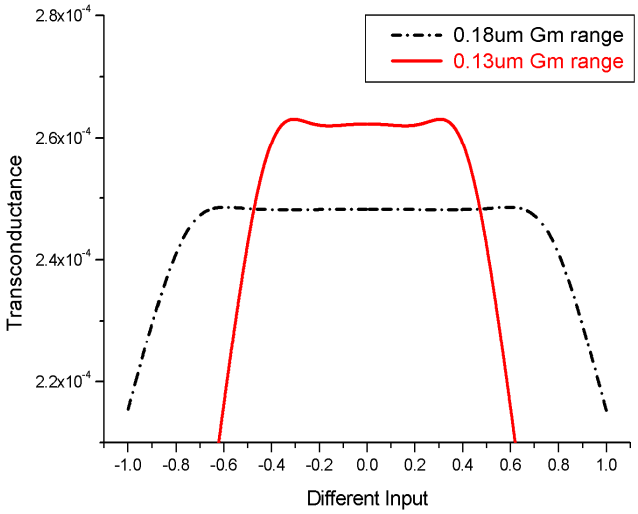


Fig. 1.1 The transconductance range

1.2 Thesis Overview

This thesis covers theoretical analysis of the CT ΔΣ modulator and the method of the CT loop filter from its DT function. After discussing the design issues of the CT ΔΣ modulator as well as the solutions, the detailed design procedure of the prototype modulator are presented. The thesis is organized as following:

Chapter 2 reviews some basic concepts about ΔΣ ADCs to help understand the rest of the thesis.

Chapter 3 describes the equivalence between the DT and CT loop filters in terms of impulse-invariant transformation (IIT). Besides, effects of various non-idealities and potential solutions to deal with them are discussed.

Chapter 4 proposes a CT ΔΣ modulator using feedback resistors. The system level design procedure which combines many aspects of the design considerations and detailed circuit level design are discussed.

Chapter 5 presents a CT ΔΣ modulator we propose. We also show the system

level design procedure which combines many aspects of the design considerations and circuit design of this CT ΔΣ modulator.

Chapter 6 covers the issues of test board design as well as the chip evaluation work.

Chapter 7 concludes the thesis and discusses some future work.

Chapter 2

Overview of Oversampling ΔΣ Modulator

In this chapter, we describe some basic background knowledge about ΔΣ ADCs. The concepts of quantization, oversampling and noise-shaping are introduced and illustrated with examples. The tradeoffs of the various sigma-delta modulator architectures will be discussed.

2.1 Sampling and Quantization

In order to properly interface the analog world which is composed of continuous-time signal (e.g. voice, audio or video) with the digital signal processor which can only process discrete-time signal, analog-to-digital conversion is required. We describe it into two basic operations: uniform sampling in time and quantization in amplitude.

Under the assumption that the signal information of the continuous input waveform $u(t)$ is contained in the signal band, i.e., $|f_{sig}| \leq f_B$, where f_B is defined as the signal bandwidth, the sampling in time is a completely invertible process. This is easily understood when considering a quantization in time as a periodization in frequency [1], which is illustrated in Fig. 2.1. There, the considered input signal is sampled at uniform time intervals T_S, the sampling time, or with a fixed frequency, f_S, resulting in a periodicity of the original signal

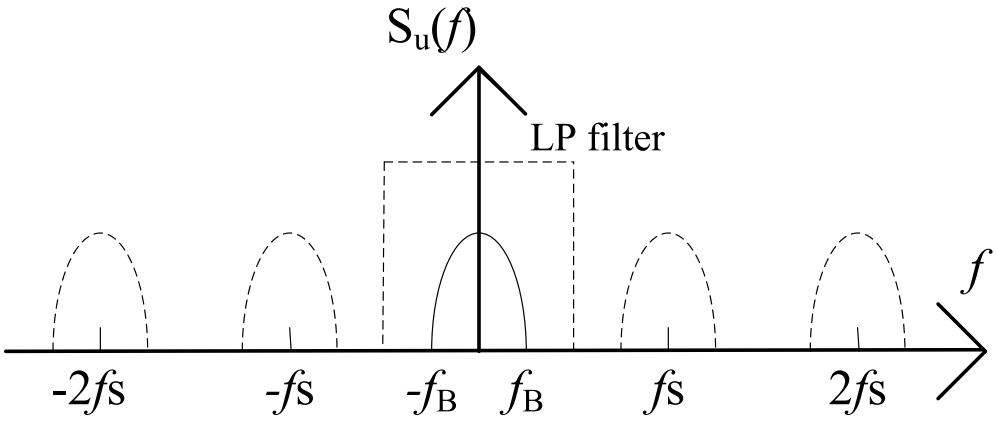


Fig. 2.1 The sampling spectral

spectrum at multiples of f_S . From Fig. 2.1 it is obvious that by sample low-pass filtering, the original base-band spectrum can be reconstructed, provided that the sampling itself does not result in overlap or aliased regions. This is achieved when:

$$f_S \geq 2 f_B = f_N \tag{2.1}$$

which is known as the *Nyquist theorem*, where f_N is the *Nyquist frequency*. To assure a proper sampling operation, the condition in (2.1) is enforced by an analog filter preceding the sampling operation, called the *antialiasing filter* (AAF).

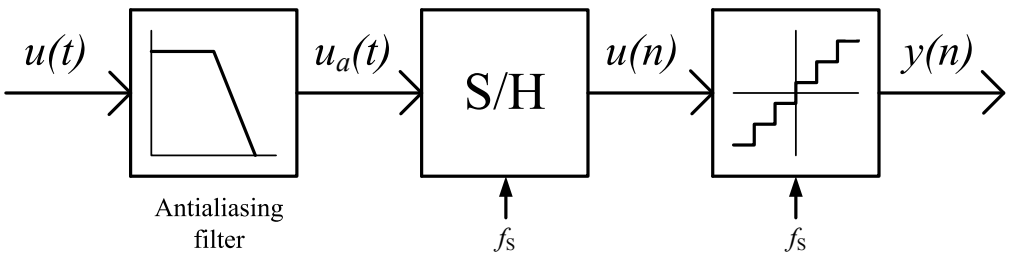


Fig. 2.2 Analog-to-digital conversion

The basic ADC structure is shown in Fig. 2.2. An ADC working with a sampling frequency of f_N is called a *Nyquist Rate* converter. But in real implementations, this results in a zero transition band for the filter to cut off the unwanted high frequency signals, making it hard to design. On the other hand, analog filters with a gentle roll in their transition band are less costly, easier to design; require less power, and smaller chip area while introducing less phase distortion. Therefore, many ADCs work with sampling rates higher than f_N , and one defines:

$$OSR = \frac{f_S}{2 f_N} \tag{2.2}$$

as the *oversampling ratio* of the ADC.

The process of quantization in amplitude, usually referred to as the quantization, encodes a continuous range of analog values into a set of discrete levels. The quantizer is assumed to be a memoryless nonlinear device completely defined by its static input-output characteristics, i.e., by its *y*-*v* transfer curve. An example of such a curve is shown in Fig. 2.3(a), where the number of quantization level is 4 which can be represented by a 2-digit binary code, and the difference of two adjacent quantized values Δ is the same as the difference between input thresholds, also known as least-significant bit size or LSB size, given by V_{LSB}. The difference between the lowest and the highest levels is called the full-scale (FS) of the quantizer, given by $2V_{Ref}$. The deviation between the sampled input and the quantized output is called the quantization error, or the quantization noise. Fig. 2.3(b) shows the relationship between the quantization noise q and the input y. From this figure, it can be seen that as long as y is between $-(V_{Ref} + V_{LSB}/2)$ and $+(V_{Ref} + V_{LSB}/2)$, the error q is between $-V_{LSB}/2$ and $+V_{LSB}/2$. The range of y where this condition is satisfied is called the non-overload input range. For an N bit ADC, the

quantization step as well as the LSB size is given by $\Delta = V_{LSB} = FS/(2^N-1)$, which is in the case $2V_{Ref}/3$.

The ideal quantizer is a deterministic device. The output v and hence the error q are fully determined by the input *y*. However, under certain circumstances, for example, if the input y stays within the non-overload input range of the quantizer, and changes by sufficiently large amounts from sample to sample so that its position within a quantization interval is essentially random, then it is permissible to assume

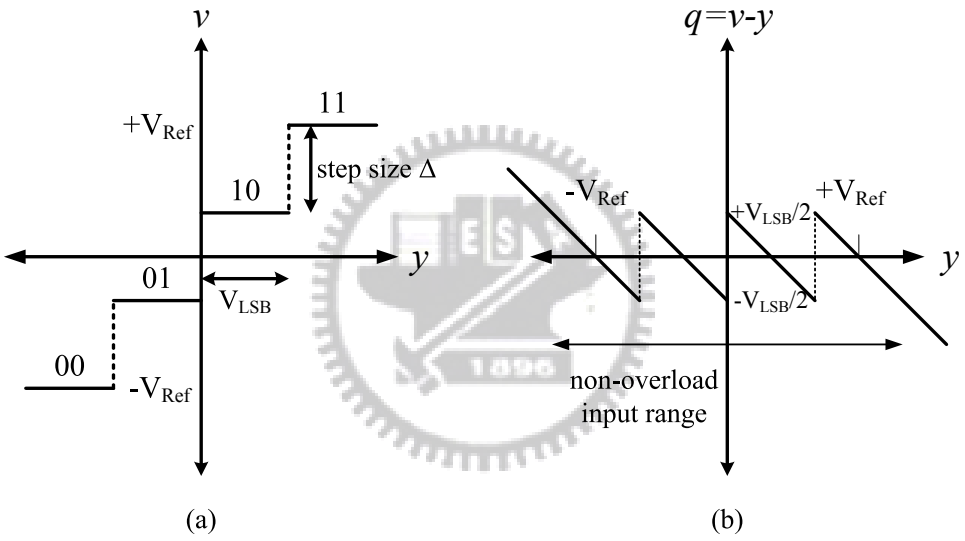


Fig. 2.3 (a) Transfer curve and (b) error function of a 4-level quantizer

that *q* is a white noise process with samples uniformly distributed between $-V_{LSB}/2$ and $+V_{LSB}/2$. The probability density function (PDF) and power spectral density (PSD) of the quantization noise are shown in Fig. 2.4.

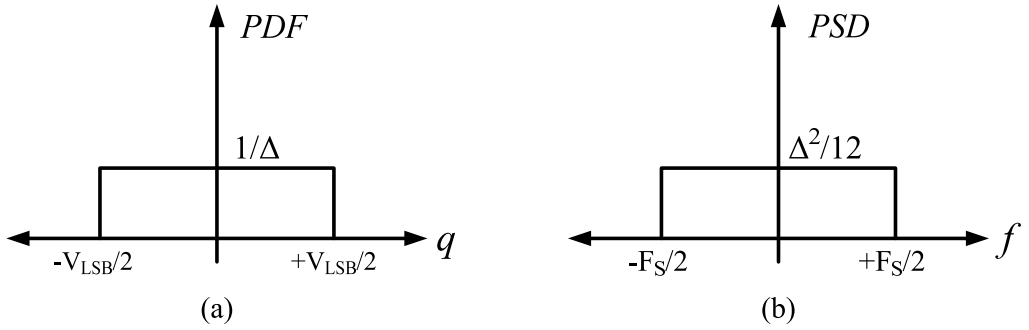


Fig. 2.4 (a) Probability density function of quantization noise (b) power spectral density of quantization noise

The impact of the quantization noise on the ADC's performance can be found by calculating its maximum signal-to-quantization-noise ratio (SQNR). This parameter is obtained by dividing the power of a sinusoidal input signal by the power of the quantization noise. The power of a sinusoidal signal is given by $Amp^2/2$, where Amp is the amplitude of the signal. The power of the quantization noise is given in (2.3).

$$\sigma_q^2 = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} q^2 \, dq = \frac{\Delta^2}{12} \tag{2.3}$$

To get the SQNR, Amp should be equal to half of the non-overload input range of the quantizer, which is $V_{Ref}+V_{LSB}/2$.

$$SQNR = \frac{\left(V_{Ref} + \frac{\Delta}{2}\right)^2}{\frac{\Delta^2}{12}} = \frac{\left(2^{N-1}\Delta\right)^2}{\frac{\Delta^2}{12}} = \frac{3}{2} 2^{2N} \tag{2.4}$$

(2.4) is expressed in dB, this becomes (2.5), which is widely used to assess the performance of the data converter.

$$SQNR\ [dB] = 10 \log_{10} SQNR = 6.02N + 1.76 \tag{2.5}$$

2.2 Oversampling

A way to calculate the power of the quantization noise is to integrate the power spectral density over the full bandwidth which we interest:

$$\sigma_q^2 = \frac{1}{f_S}\int_{-f_S/2}^{f_S/2}\frac{\Delta^2}{12}df = \frac{\Delta^2}{12} \tag{2.6}$$

From above equation, it is obvious that if the bandwidth of interest is much lower than the bandwidth which we interest, the resolution of the ADC can be improved by filtering the output to the desired bandwidth which reduces the total power of the quantization noise. This technique, illustrated in Fig. 2.5, is called oversampling.

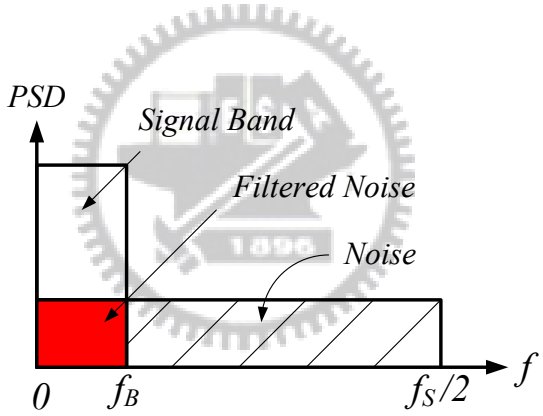


Fig. 2.5 Oversampling

Now, the power of the in-band quantization noise is given in (2.7).

$$N_q^2 = \frac{1}{f_S}\int_{-f_S}^{f_S}\sigma_q^2 df = \sigma_q^2\frac{2f_B}{f_S} = \frac{\sigma_q^2}{OSR} \tag{2.7}$$

where OSR, defined as $\frac{f_S}{2f_B}$, is called oversampling ratio which is one of the most important parameters used to characterize the oversampling data converters. The power of input signal is not modified since it is assumed that it has no frequency content above f_B. Therefore, the maximum SQNR is given by:

$$SQNR\ [dB] = 6.02N + 1.76 + 10\log OSR \qquad (2.8)$$

It is obvious that if the sampling rate is equal to twice the *Nyquist rate* (OSR = 2), the SQNR is improved by 3 dB. (2.8) shows that oversampling can improve the SQNR with the OSR at a rate of 3 dB/octave, or 0.5 bit/octave [2].

2.3 Noise Shaping

In the previous section, we show that oversampling can be used to trade speed for resolution of ADC. It is noticed that the quantization noise in previous section has a flat power spectral density over the full bandwidth $[-f_S/2, f_S/2]$. A more efficient way to use oversampling is to shape the spectral density such that most of the quantization noise power is outside the band of interest. A general noise-shaped sigma-delta modulator and its linear model have been shown in Fig. 2.6.

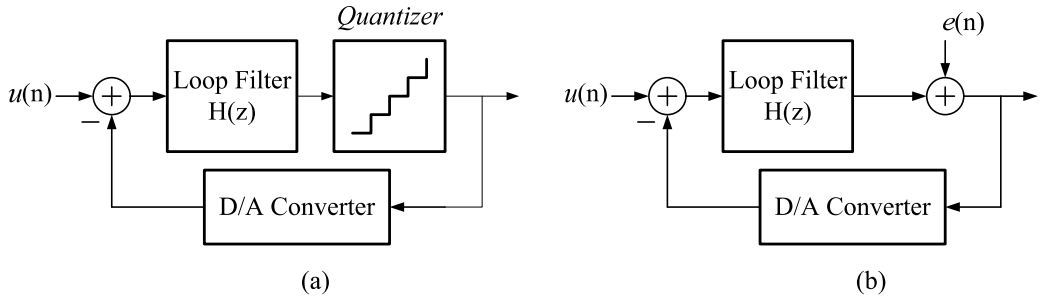


Fig. 2.6 (a) A general noise-shaping delta-sigma modulator (b) Linear model of the modulator showing injected quantization noise

Treating the linear model shown in Fig. 2.6 as having two independent inputs, $u(n)$ and $e(n)$, we can derive a signal transfer function $STF(z)$, and a noise transfer function $NTF(z)$.

$$STF(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{2.9}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \tag{2.10}$$

According to (2.9) and (2.10), the zeros of the noise transfer function $NTF(z)$, will be equal to the poles of $H(z)$. In other words, we can control the zeros of the noise transfer function by choosing the function of the loop filter. We can also using super position to combine two signals, and find out the output as

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \tag{2.11}$$

The $STF(z)$ generally have all-pass or low-pass frequency response and the $NTF(z)$ have high-pass frequency response. In other words, the $STF(z)$ will be approximately unity over the signal band and the $NTF(z)$ will be approximately zero over the same frequency band. The quantization noise will be removed to high frequency band when using noise-shaping strategy [3]. The quantization noise over the frequency band which we interest will be reduced and do not affect the input signal. This would improve the SNR significantly for overall system.

2.3.1 First-Order Delta-Sigma Modulator

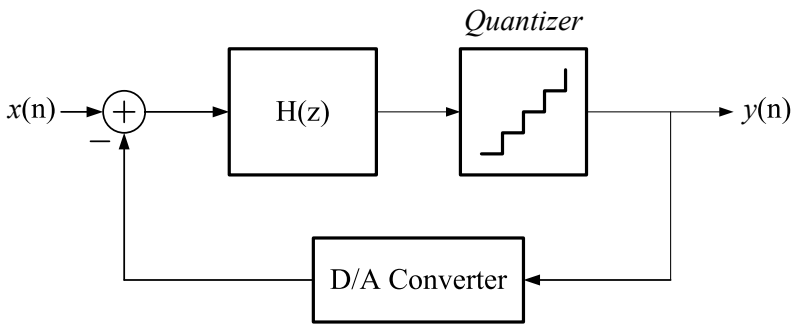


Fig. 2.7 The block diagram of the first-order low-pass delta-sigma modulator

In Fig. 2.7, it is a block diagram of the first-order low-pass delta-sigma modulator. It includes an integrator and a quantizer. The input of the integrator is the input signal minus the output signal of the modulator through the DAC. In this example, since the loop filter is a high-pass filter, the noise function should have a zero at dc (i.e., z = 1). The transfer function of the discrete-time integrator (i.e., have a pole at z = 1) is

$$H\ (z) = \frac{1}{z - 1} \tag{2.12}$$

Its block diagram for such a choice is shown in Fig. 2.8.

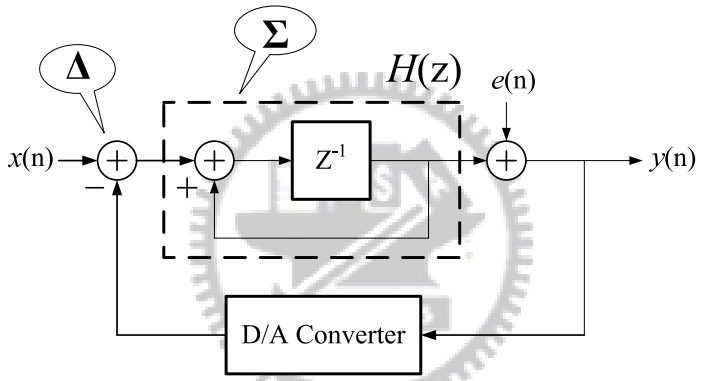


Fig. 2.8 First-order delta-sigma modulator

According to (2.9) and (2.10), we can obtain the signal transfer function $STF\ (z)$, is given by

$$STF\ (z) = \frac{Y\ (z)}{U\ (z)} = \frac{\frac{1}{z - 1}}{1 + \frac{1}{z - 1}} = z^{-1} \tag{2.13}$$

and the noise transfer function $NTF\ (z)$, is given by

$$NTF\ (z) = \frac{Y\ (z)}{E\ (z)} = \frac{1}{1 + \frac{1}{z - 1}} = 1 - z^{-1} \tag{2.14}$$

Combining the two signal transfer function, we can obtain the output as

$$Y(z) = z^{-1}U(z) + (1 - z^{-1})E(z) \tag{2.15}$$

We see that the input signal is just a delay through the input to the output, and the quantization noise is through a discrete-time differentiator (i.e., a high-pass filter) to the output. We are interesting in the magnitude of the noise transfer function, $|NTF(f)|$, we let $z = e^{j\omega T} = e^{j2\pi f/f_S}$ and get the following:

$$\begin{aligned} NTF(f) &= 1 - e^{-j2\pi f/f_S} \\ &= \frac{e^{j\pi f/f_S} - e^{-j\pi f/f_S}}{2j} \times 2j \times e^{-j\pi f/f_S} \\ &= \sin\left(\frac{\pi f}{f_S}\right) \times 2j \times e^{-j\pi f/f_S} \end{aligned} \tag{2.16}$$

Taking the magnitude of both sides, we have the high-pass function

$$|NTF(f)| = 2\sin(\frac{\pi f}{f_S}) \tag{2.17}$$

Now we can integrate the quantization noise power over the frequency bandwidth we interest as below

$$\begin{aligned} P_e &= \int_{-f_B}^{f_B} S_e^{\,2}(f)\,|NTF(f)|^2\,df \\ &= \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_S}\left[2\sin\left(\frac{\pi f}{f_S}\right)\right]^2 df \end{aligned} \tag{2.18}$$

When $f_B \ll f_S$ (i.e., OSR>>1), we can approximate $\sin(\frac{\pi f}{f_S})$ to be $(\frac{\pi f}{f_S})$, so we have

$$P_e \cong \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^2}{3}\right)\left(\frac{2f_B}{f_S}\right)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{1}{OSR}\right)^3 \tag{2.19}$$

Now we can estimate the maximum SNR by assuming the input signal having maximum amplitude. We can obtain as

$$SNR = 10\log\left(\frac{P_S}{P_E}\right) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{3}{\pi^2}(OSR)^3\right] \tag{2.20}$$

or, equivalently,

$$SNR = 6.02N + 1.76 - 5.17 + 30\log(OSR) \tag{2.21}$$

We can see that the first-order noise shaping can give an SNR improvement for 9 dB or 1.5 bits by doubling the OSR. This result should be compared to the 0.5 bits/octave when oversampling with no noise shaping.

2.3.2 Second-Order Delta-Sigma Modulator

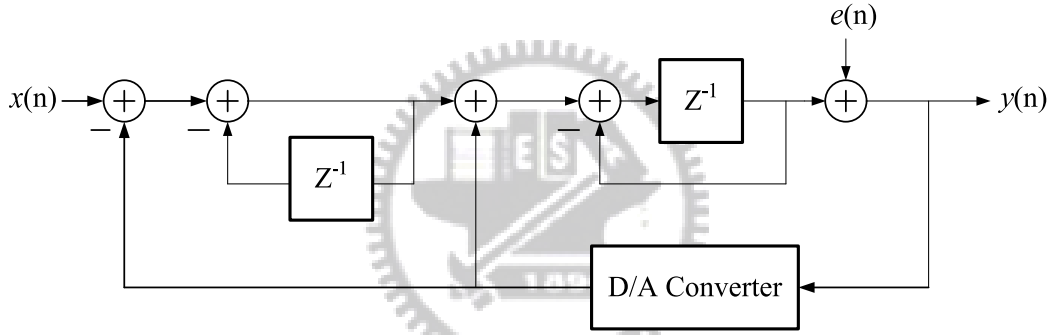


Fig. 2.9 The block diagram of the second-order low-pass ΔΣ modulator

The second-order low-pass delta-sigma modulator is shown in Fig. 2.9. Through the arrangement of the block diagram, we can obtain the noise transfer function $NTF(f)$, as a second-order high-pass function

$$NTF(f) = (1 - z^{-1})^2 \tag{2.22}$$

and the signal is just a delay to output. The signal transfer function is given by

$$STF(f) = z^{-1} \tag{2.23}$$

Combining the two signal transfer function, we can obtain the output as

$$Y(z) = z^{-1}U(z) + (1 - z^{-1})^2 E(z) \tag{2.24}$$

The same as before, we interest in the magnitude of the noise transfer function can be show to given by

$$\left|NTF(f)\right| = \left[2\sin(\frac{\pi f}{f_S})\right]^2 \tag{2.25}$$

Integrating the quantization noise power over the frequency band which we interest and using the approximation, we can get the result:

$$P_e = \int_{-f_B}^{f_B} S_e^2(f)\left|NTF(f)\right|^2 df$$

$$= \int_{-f_B}^{f_B} \left(\frac{\Delta^2}{12}\right)\frac{1}{f_S}\left[2\sin\left(\frac{\pi f}{f_S}\right)\right]^4 df$$

$$= \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^4}{5}\right)\left(\frac{2f_B}{f_S}\right)^5 = \frac{\Delta^2\pi^4}{60}\left(\frac{1}{OSR}\right)^5 \tag{2.26}$$

Again, assuming the maximum signal power is used, the maximum SNR for this case is given by

$$SNR = 10\log(\frac{P_S}{P_E}) = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{5}{\pi^4}(OSR)^5\right] \tag{2.27}$$

or, equivalently,

$$SNR = 6.02N + 1.76 - 12.9 + 50\log(OSR) \tag{2.28}$$

We can see that the second-order noise shaping can give an SNR improvement for 15 dB or 2.5 bits by doubling the OSR.

Fig. 2.10 shows the noise-shaping curves compared with shape of zero-, first-, second- and third-order. The noise power decreases as the noise-shaping order increases over the band which we interest. But the out-of-band noise power increases for the higher-order modulators.

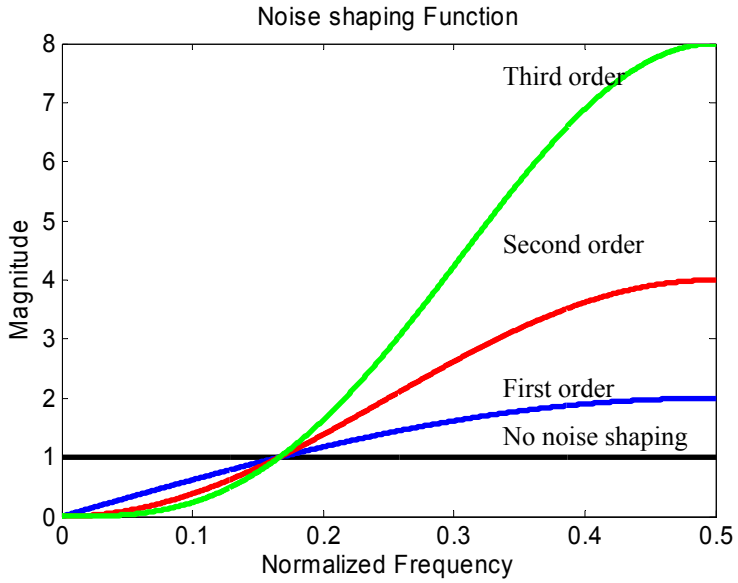


Fig. 2.10 Different order noise shaping curves

2.3.3 High-Order Delta-Sigma Modulator

As mentioned before, we extend the delta-sigma modulator to L order, and get the noise transfer function

$$NTF(f) = (1 - z^{-1})^{L} \tag{2.29}$$

We let $z = e^{j\omega T} = e^{j2\pi f / f_S}$ and get the magnitude response

$$\left|NTF(f)\right| = \left[2\sin(\frac{\pi f}{f_S})\right]^{2} \tag{2.30}$$

Integrating the quantization noise power over the frequency band which we interest and using the approximation, we can get the result:

$$P_e = \int_{-f_B}^{f_B} S_e^{2}(f)\left|NTF(f)\right|^{2} df$$

$$= \int_{-f_B}^{f_B} \left(\frac{\Delta^{2}}{12}\right)\frac{1}{f_S}\left[2\sin\left(\frac{\pi f}{f_S}\right)\right]^{2L} df$$

$$= \left(\frac{\Delta^2}{12}\right)\left(\frac{\pi^{2L}}{2L+1}\right)\left(\frac{2f_B}{f_S}\right)^{2L+1} = \frac{\Delta^2\pi^{2L}}{12\bullet(2L+1)}\left(\frac{1}{OSR}\right)^{2L+1} \quad (2.31)$$

Again, assuming the maximum signal power is used, the maximum SNR for this case is given by

$$SNR = 10\log\left(\frac{3}{2}2^{2N}\right) + 10\log\left[\frac{2L+1}{\pi^{2L}}(OSR)^{2L+1}\right] \quad (2.32)$$

or, equivalently,

$$SNR = 6.02N + 1.76 + (20L+10)\log OSR - 10\log\left(\frac{\pi^{2L}}{2L+1}\right) \quad (2.33)$$

In general case, the SNR will improve with the OSR at a rate of 6L+3 dB/octave, or equivalently, L+0.5 bit/octave with the L-order noise shaping. Fig. 2.11 shows the SQNR tradeoff between order and OSR.

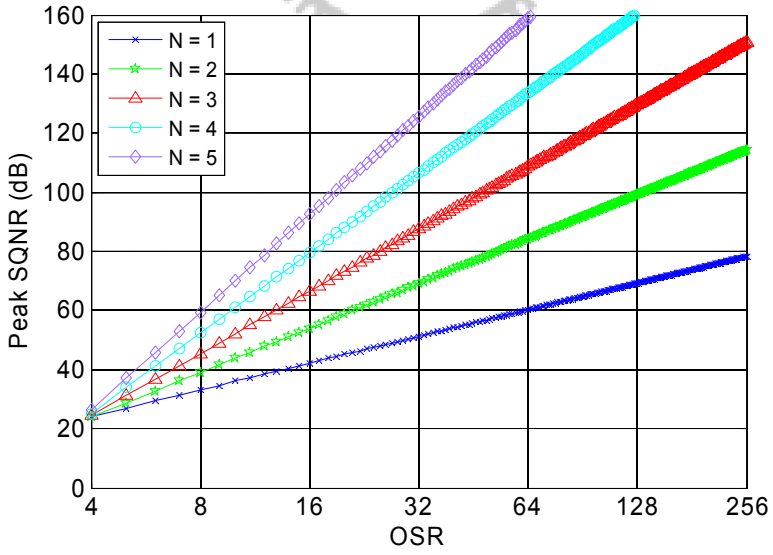


Fig. 2.11 Empirical SQNR limit for 1-bit modulators of order N

Chapter 3

Design of Continuous-Time ΔΣ Modulator

In this chapter, we illustrate the procedure to choose the feedback DAC pulse shapes and design the loop filter function for CT ΔΣ modulator. Besides, various non-idealities will affect the performance, even the stability of the CT ΔΣ modulator. These non-idealities, including finite OpAmp gain and gain-bandwidth, excess loop delay, element mismatch in the multi-bit feedback DAC and clock jitter, would be analyzed in detail.

3.1 DT to CT Conversion of ΔΣ Modulator

3.1.1 Impulse-Invariant Transformation

The quantizer in a CT ΔΣ modulator is clocked, that is, there is an implicit sampling action inside the modulator. Because sampled circuits are DT circuits, we can make the sampling explicit by placing the sampler immediately prior to the quantizer without changing the behavior of the modulator, as Fig. 3.1 shown. As mentioned above, the two modulators are equivalent if their quantizers have the same inputs at each sampling instant, which means

$$x(n) = x_C(t)\,|_{t=nT_S} \tag{3.1}$$

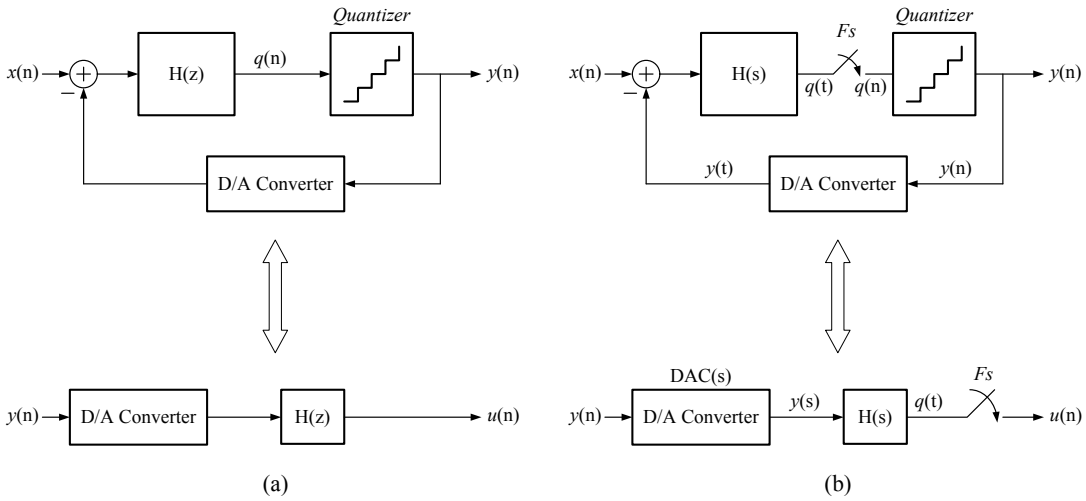


Fig. 3.1 The loop filter representation for (a) DT modulator and (b) CT modulator

This can be satisfied if the open loop impulse responses are the same at sampling instants, which can be written as

$$\mathbb{Z}^{-1}\{H(z)\} = L^{-1}\{DAC(s)H(s)\}|_{t=nT_S} \tag{3.2}$$

In the time domain, this leads to the condition

$$h(n) = DAC(t) * h(t)|_{t=nT_S} \tag{3.3}$$

where $h(n)$, $DAC(t)$ and $h(t)$ are the impulse responses of the DT loop filter $H(z)$, the CT feedback DAC and the CT loop filter $H(s)$, respectively. This transformation between the DT and CT domains is called the ***Impulse Invariant Transformation*** [4], because it makes the open loop impulse response equal at the sampling times.

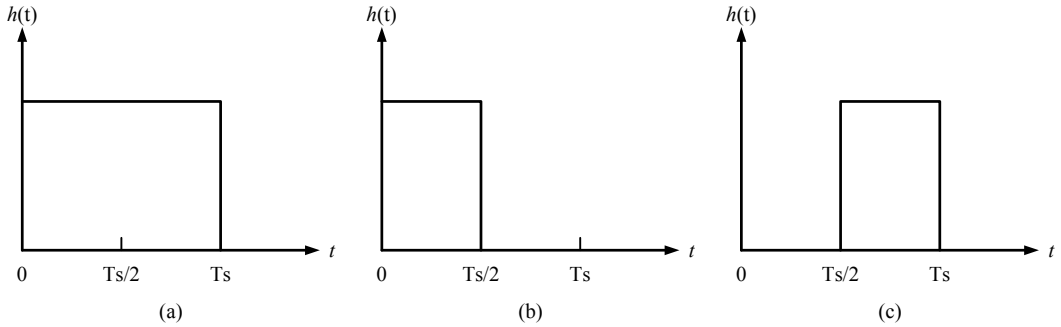


Fig. 3.2 DAC feedback impulse response (a) NRZ (b) RZ (c) HRZ

3.1.2 Synthesis of CT ΣΔ Feedback DAC

To actually perform the ***Impulse Invariant Transformation***, the continuous-time DAC feedback pulse shape has to be decided first. Different pulse shapes result in different transformations between the DT and CT modulators. We will shortly discuss their practical advantages. There are three commonly used rectangular DAC feedback pulses: non-return-to-zero (NRZ), return-to-zero (RZ) and half-delay-return-to-zero (HRZ) [5]. Their impulse responses are shown in Fig. 3.2. DACs with NRZ shapes provide constant output over a full period; DACs with RZ shapes produce constant valid output only from 0 to T/2 and DACs with HRZ produce a half clock cycle delayed version of RZ. The transfer function of NRZ, RZ and HRZ can be described by the same equation:

$$H_{DAC}(s) = \frac{\exp(-\alpha s) - \exp(-\beta s)}{s} \tag{3.4}$$

where α and β are valid feedback starting and ending times respectively, so we have

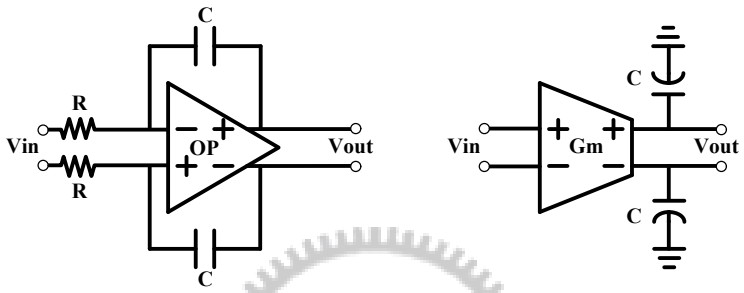
$$\begin{cases} \alpha = 0, \beta = T_S & NRZ \\ \alpha = 0, \beta = 0.5T_S & RZ \\ \alpha = 0.5T_S, \beta = T_S & HRZ \end{cases} \tag{3.5}$$

After determining the DAC feedback pulse shape and its transfer function, the impulse invariant transform can be executed following the steps below. At first, we will write $H(z)$ as a partial fraction expansion. Following, we convert each

partial fraction from z-domain to s-domain. At the last, we recombine the results from step 2 to get $H_C(s)$ [6].

3.2 Non-idealities in ΔΣ Modulator

3.2.1 Non-idealities in CT Integrators



$$V_{out} = -\frac{1}{sRC}V_{in} \qquad V_{out} = \frac{Gm}{sC}V_{in}$$

(a) **(b)**

Fig. 3.3 (a) Active-RC (b) Gm-C integrators

The basic circuit blocks of a CT loop filter are the CT integrators. Many kinds of CT integrators are available but the most commonly used are active-RC integrators and Gm-C integrators, as shown in Fig. 3.3.

The advantages of the active-RC integrators over the Gm-C counterparts include higher linearity and larger input signal swing. Because the active-RC integrators are based on the closed loop applications of the operational amplifiers (OpAmps), the OpAmp's inputs are virtual ground and only experience very small signal swing regardless of the integrator's input. On the contrary, the transconductor, which performs voltage-to-current (V-I) transformation with a known

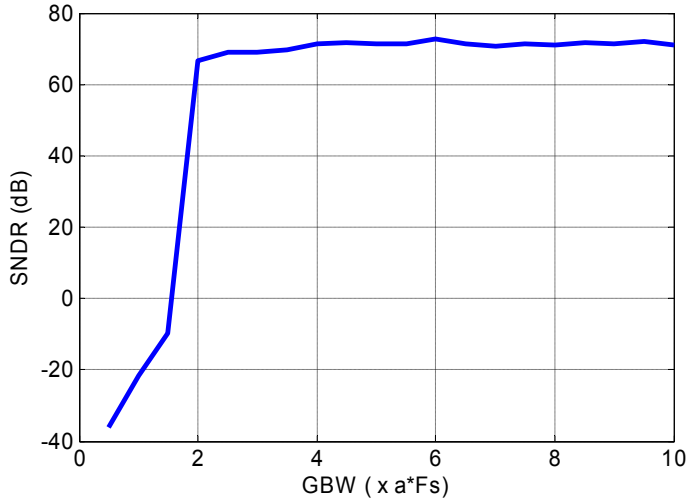


Fig. 3.4 The GBW requirement of the OpAmp in the integrator

transconductance, operates under the open-loop condition in the Gm-C integrators, so its inputs have to experience the full swing of the integrator's input, which degrades the linearity of the integrator. Due to this reason, the input signal of the Gm-C integrator has to be small enough to keep a reasonable linearity. When using active-RC integrators to build a CT ΔΣ modulator, the virtual ground provided by the closed loop OpAmp application will also greatly improve the linearity of the feedback current DAC whose outputs are connected with the inputs of the OpAmp. However, in a CT ΔΣ modulator based on Gm-C integrators, the feedback DAC's outputs have to be connected with the output of the integrator and hence experience the full output swing, which degrades the linearity of the DAC.

As shown in Fig. 3.4, we find **"the gain-bandwidth requirement of the OpAmp in the integrator of the CT ΔΣ modulator is two times as high as the sampling frequency or similar"**. Therefore, the relative bandwidth normalized to rad/s is

$$GBW\ [rad/s] = 2 \times 2\pi\alpha\ f_S = \frac{gm_{OP}}{C_L} \qquad (3.6)$$

Table 3.1 Overview of various advantages and drawbacks of various CT integrator approaches

	Gm-C	Active-RC	MOSFET-C
Frequency Range	☆☆☆☆	☆☆☆	☆☆
Tunability	☆☆☆	☆	☆☆☆
Linearity	☆	☆☆☆☆	☆☆
Dynamic range	☆☆	☆☆☆	☆☆
Mismatch insensitivity	☆☆☆	☆	☆
Power requirements	☆☆☆	☆☆	☆☆
Low-voltage capability	☆	☆☆☆	☆☆

On the other hand, due to the same open loop working condition, the GBW of the Gm-C integrator is

$$GBW\ [rad/s] = \alpha\ f_S = \frac{gm_{Gm}}{C_L} \tag{3.7}$$

If we give the same C_L, we will find the gm_{OP} is 4π times as high as the gm_{Gm} and get the speed performance of the Gm-C integrator is better than the active-RC integrator. In other words, the power consumption of the Gm-C integrator will be lower for a given bandwidth requirement.

A qualitative overview is given in Table 3.1 [6]. The log approach shows advantages, if low voltage capability and power consumption are of high interest while the desired frequency range is limited to a few MHz. If a higher frequency range is additionally demanded in connection with a high linearity, the active-RC integrator is the preferred structure. For linearity requirements limited to about

$THD = -60\ dB$, Gm-C integrators are favorable, if low power is a major interest [6].

According to the above analysis, the active-RC integrator is preferred as the first stage integrator, and following are Gm-C integrators to save power.

3.2.2 Finite OpAmp Gain and Gain-Bandwidth

Operational amplifiers (OpAmps) are the basic blocks of the active-RC integrators. An ideal opamp can be seen as a voltage-controlled voltage source whose voltage gain is infinitely large across the whole frequency domain. However, a real opamp has a finite DC gain and several poles and zeros in its transfer function. In analysis, we assume an OpAmp be a single pole system and the model is given by:

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_A}} \tag{3.8}$$

where A_{DC} is OpAmp DC gain and ω_A is the dominant pole of the OpAmp. Besides, the unity gain bandwidth of the OpAmp can be express as:

$$GBW = A_{DC} \times \omega_A \tag{3.9}$$

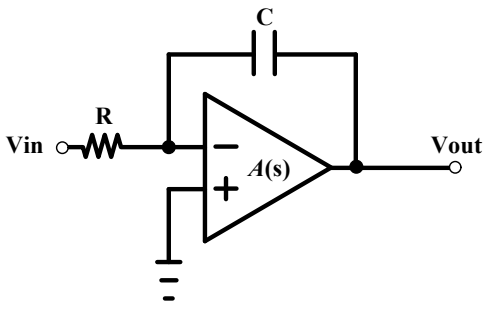


Fig. 3.5 The active-RC integrator with single pole OpAmp

As shown in Fig. 3.5, the integrator transfer function (ITF) from one input to the output can be expressed as:

$$ITF(s) = \frac{\alpha f_S}{s\left(1 + \frac{1}{A(s)}\right) + \frac{\alpha f_S}{A(s)}} \tag{3.10}$$

We incorporate (3.8) and (3.9) into (3.10), and get the modified transfer function as followed:

$$ITF_{GBW}(s) = \frac{\alpha f_S}{s\left(1 + \frac{1}{A_{DC}} + \frac{s}{GBW}\right) + \frac{\alpha f_S}{GBW}s + \frac{\alpha f_S}{A_{DC}}}$$

$$= \frac{\alpha f_S}{\frac{s^2}{GBW} + s\left(1 + \frac{1}{A_{DC}} + \frac{\alpha f_S}{GBW}\right) + \frac{\alpha f_S}{A_{DC}}} \tag{3.11}$$

This ITF consists of a scaled integrator in series with a gain error and an additional second integrator pole. According to this model, finite GBW in CT ΔΣ modulators has a rather similar influence as RC variation and decrease the modulator performance.

3.2.3 Excess Loop Delay

When we synthesize the CT loop filter $H(s)$ from a DT filter $H(z)$ for a given feedback DAC waveform in the section 3.1.2, it is assumed that there is no delay time between the sampling instant of the loop filter output and the generation of new output digital codes. However, in the real circuits, due to the finite speed of transistors, this delay known as excess loop delay could not be zero. The excess loop delay usually consists of the delays introduced by the quantizer (including the dynamic element matching (DEM) logic if necessary), feedback DAC,

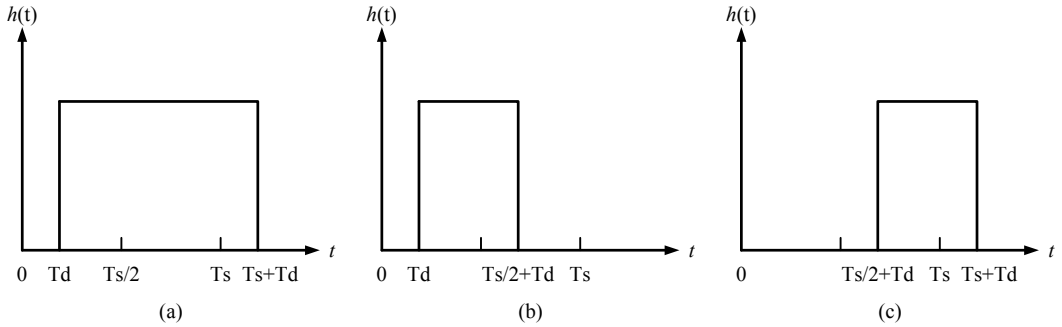


Fig. 3.6 DAC feedback impulse response including Excess Loop Delay (a) NRZ (b) RZ (c) HRZ

and loop filter. Considering the feedback DAC, the impulse response of those three rectangular DAC pulses shown in Fig. 3.2 is changed to be that in Fig. 3.6.

As analyzed in [5], if the falling edge of the DAC pulse exceeds the time instant T_S, the order of the equivalent DT loop filter of the CT one is higher by one than under ideal conditions, which makes the CT modulator uncontrolled. The excess loop delay degrades the dynamic range of the modulator by reducing the effectiveness of the noise shaping as well as the maximum stable input signal swing. If the excess loop delay is too large compared with the clock period, the CT modulator will be unstable.

In order to compensate the excess loop delay, the RZ pulse can be used as the DAC waveform. As shown in Fig.3.6 (b), it can be seen that if the excess loop delay is smaller than half clock period, then the falling edge is still within the range $0 \sim T_S$, and hence the equivalent DT loop filter has the same order of the CT one. However, in most CT ΔΣ modulators, the NRZ DAC pulse is superior to the RZ (or HRZ) counterpart in terms of the clock jitter sensitivity issue. In addition, because the exact value of the excess loop delay t_d is unknown while synthesizing the CT loop filter, the resulting CT modulator still cannot realize the same noise shaping as

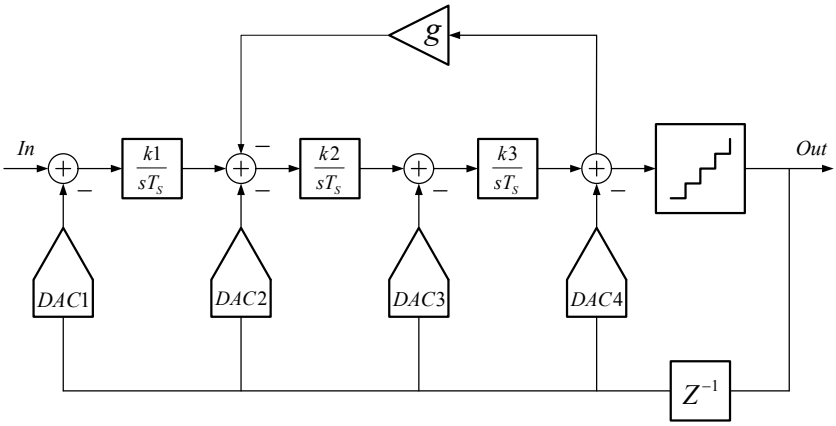


Fig. 3.7 Continuous-Time ΔΣ modulator with zero-order loop compensation

the DT target even using RZ DAC pulse.

While using NRZ DAC pulse, a common solution to the excess loop delay is to introduce a full clock delay in the feedback path to absorb the varying quantizer delay as well as the other delays, as shown in Fig. 3.7. However, due to this full clock delay, the impulse response of the CT loop at the sampling instant T_S is zero. To compensate this response sample, an extra feedback branch is added directly to the quantizer input to make the total impulse response equivalent to the DT function [7]. Because the loop formed by the extra feedback branch doesn't include any integrator, we call it zero-order loop compensation.

3.2.4 Clock Jitter

In the DT ΔΣ modulator, the continuous-time signal is sampled at the modulator input, so the sampling error caused by the clock jitter is directly added to the output without any attenuation. However, the sampling action in the CT ΔΣ modulator happens at the input of the quantizer, so the jitter-induced error is shaped by the loop filter before it appears at the output and hence may be negligible. But,

the DAC output of the CT ΔΣ modulator is continuous, that is, the feedback signal affects the loop filter at all time instead of just at the sampling instants. Therefore, the timing error of the feedback signal transition edges caused by the DAC clock jitter is equivalent to the feedback signal error itself. Because the DAC error also appears at the modulator output without any attenuation, the DAC clock jitter is one of the most important issues which should be considered while designing the CT ΔΣ modulator.

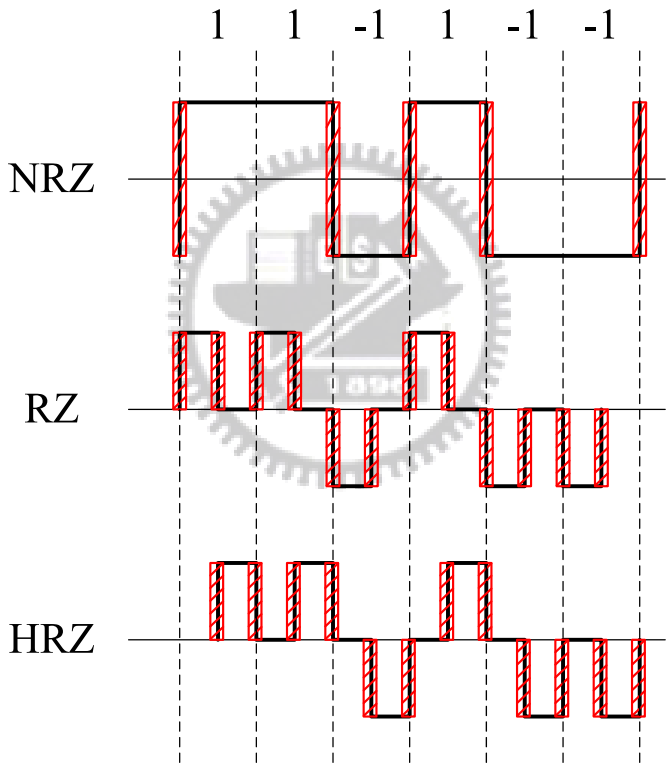


Fig. 3.8 Single-bit NRZ, RZ and HRZ DAC feedback pulse with jitter noise

DAC shapes affect the jitter sensitivity of the CT ΔΣ modulator. This can be illustrated by Fig. 3.8, where single-bit NRZ, RZ and HRZ DAC shapes are shown. The obilque lines indicate that the clock edges are affected by jitter. We can find NRZ DACs are less affected by clock jitter because clock jitter only causes errors

when the output digital code changes. However, for RZ and HRZ DACs, both rising and falling edges of the pulse occur every clock cycle so that they are affected by clock jitter more frequently.

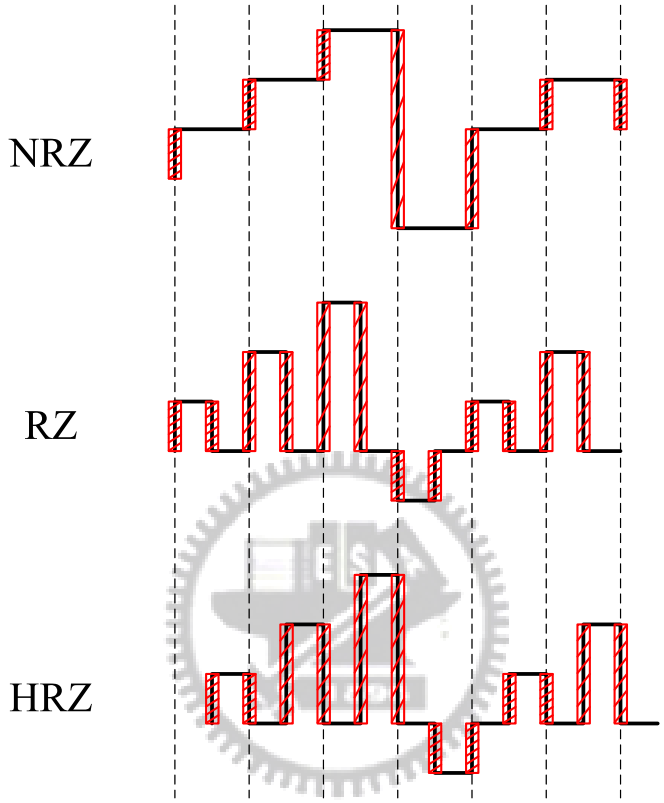


Fig. 3.9 Multi-bit NRZ, RZ and HRZ DAC feedback pulse with jitter noise

We find the jitter noise power can be lowered by reducing the standard deviation of the adjacent modulator output difference. In other words, if the step size of the quantizer is reduced, the jitter noise is lowered. This implies that using multi-bit DACs can reduce the sensitivity to clock jitter. Fig. 3.9 shows multi-bit NRZ, RZ and HRZ DAC feedback pulses with jitter noise. Intuitively NRZ multi-bit DACs should provide best jitter noise immunity than the other two in that its outputs do not need to reset to zero for every clock cycle and hence the average adjacent output difference is smaller [8].

3.2.5 Element Mismatch in a Multi-bit DAC

When we design the CT ΔΣ modulator, the oversampling ratio is usually limited by the circuit speed and power consumption. At the same time, the order and the aggressiveness of the noise shaping are also limited by the stability issue. Therefore, in order to decrease the in-band noise power, an effective way is to use a multi-bit quantizer to reduce the quantization noise in the modulator. Besides, an extra bonus of using multi-bit quantizer is the reduction of the jitter sensitivity.

However, the use of a multi-bit quantizer leads to a multi-bit DAC in the feedback path. The nonlinearity of this DAC severely limits the performance of the modulator. Because the loop filter gain is very high in the signal band, the in-band gain of the STF is almost equal to one, which means the power of the DAC error will be directly added to the modulator output without much attenuation. So, the linearity of the modulator cannot be higher than that of the DAC.

A very common DAC structure is built from unit elements, in which the nonlinearity of the DAC is mainly caused by the element mismatch. For this DAC structure, an extensively used technique to reduce the DAC error is dynamic element matching (DEM). Using DEM, the bits in the thermometer-code output of the quantizer are rearranged following certain rules by a digital process before they are applied to the DAC. This rearrangement does not affect the data value, but it changes the priority on the selecting of the unit elements in the DAC, which can result in two effects. First, the DAC error becomes uncorrelated with the DAC input, eliminating the signal dependent tones that will appear in the modulator output otherwise. Second, the so-called mismatch shaping will move the error power from low frequencies to high frequencies [2].

Chapter 4

A Continuous-Time Delta-Sigma Modulator Using Feedback Resistors

In this chapter, the system level and circuit level design of our first work is presented in detail, which includes the determination of the system level parameters, and the system level simulations with non-idealities. After that, the circuit blocks will be discussed, and the modulator is realized with a 0.18 μm CMOS technology and 1.8 V power supply voltage.

4.1 System Level Design

First of all, to design the ΔΣ modulator is determining the most important system level parameters based on the modulator specifications and the semiconductor technology which will be used to realize this modulator. In our first work, the target is to successfully design a CT ΔΣ modulator to reach 68 dB SNDR (signal-to-noise-and-distortion-ratio) within a 1 MHz bandwidth (BW) in a 0.18 μm mixed-signal CMOS process.

However, for a CT ΔΣ modulator, the important specification is the clock jitter sensitivity. It will significantly affect the selection of the system level parameters. We usually assume that the modulator will be evaluated with a clock signal generated by the instrument. Therefore, the jitter value of the clock signal entering

the modulator is determined by the quality of the instrument signal. In our first work, the RMS value of the target jitter tolerance is 20 ps.

The system-level parameters include the oversampling ratio (OSR), the loop filter order (L), the number of the quantizer level (M) and the aggressiveness of the noise shaping which is determined by the maximum out-of-band quantization gain (Q_{max}) in the MATLAB Control System toolbox. Considering the gain-bandwidth requirement of the OpAmp with acceptable power consumption and the clock jitter sensitivity, we choose 50 as our OSR value.

The power consumption of the quantizer increases proportionally to the number of quantization levels. Therefore, for this chip, we determine the number of the quantizer be single. On the other hand, increasing the loop filter order is cheap, but the loop stability issue limits the loop order. Usually, the order should be no more than 5, so we choose 3 as our loop order. Besides, the aggressiveness of the noise shaping is also limited by the stability issue. After MATLAB Control System toolbox simulation, as shown in Fig. 4.1, we choose 1.6 as our out-of-band gain. Based on these requirements, a large amount of simulations were performed by using the MATLAB toolbox to explore the parameter space.

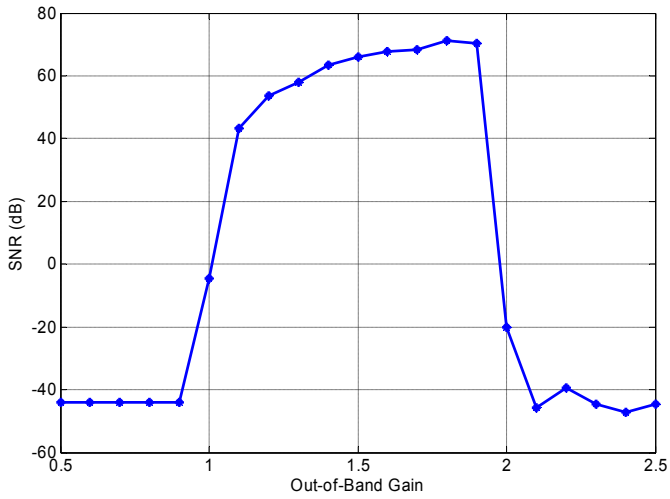


Fig. 4.1 Simulated SNR as a function of out-of-band-gain for single bit

4.2 Architecture of the Loop Filter

4.2.1 NTF Zero Optimization

When designing wide band ΔΣ modulator, a technique is usually used. That is separating zeros on the unit circle, which means it spreads over the signal range, as shown in Fig. 4.2. By shifting the two zeros from dc (ω = 0) to an optimized value, we can get the 8 dB SQNR improvement. The principle of optimization can be got by the following steps: the normalized noise power, given by the integral of the squared magnitude of the NTF over the signal band, is minimized with respected to the values of all its zeros. The optimal zeros are found by equating the partial derivatives of the integral to zero [9].

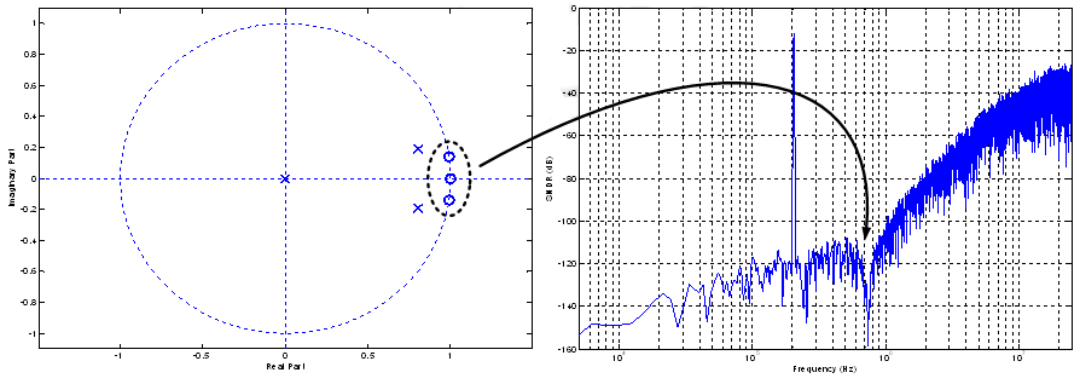


Fig. 4.2 Optimal third-order NTF for OSR = 50

In Fig. 4.3, we show the architecture of CT ΔΣ modulator using feedback resistors. The loop filter architecture we use is general feedback structure.

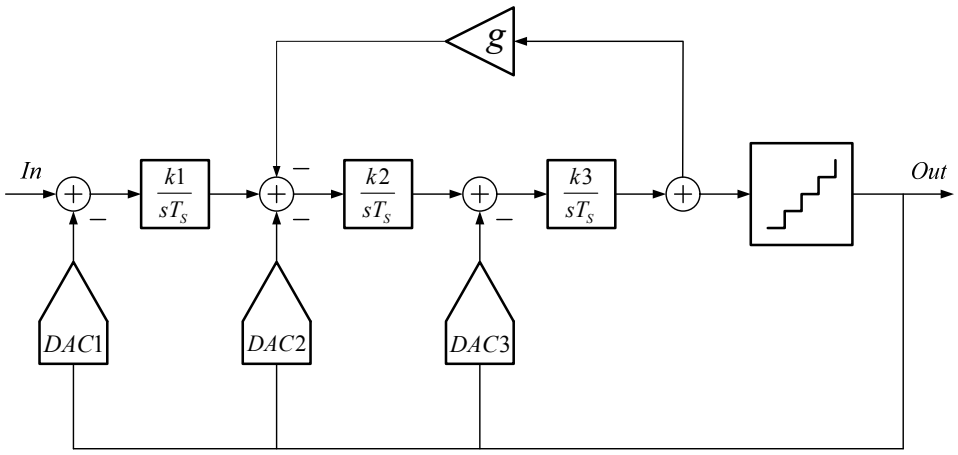


Fig. 4.3 The architecture of CT ΔΣ modulator using feedback resistors

4.3 System Level Simulation

As mentioned before, taking the non-idealities into account, we show the output spectrum in this system level simulation of the modulator, which includes all the non-idealities except the thermal noise, as shown in Fig. 4.4. As a comparison, the ideal noise transfer function is also plotted in this figure.

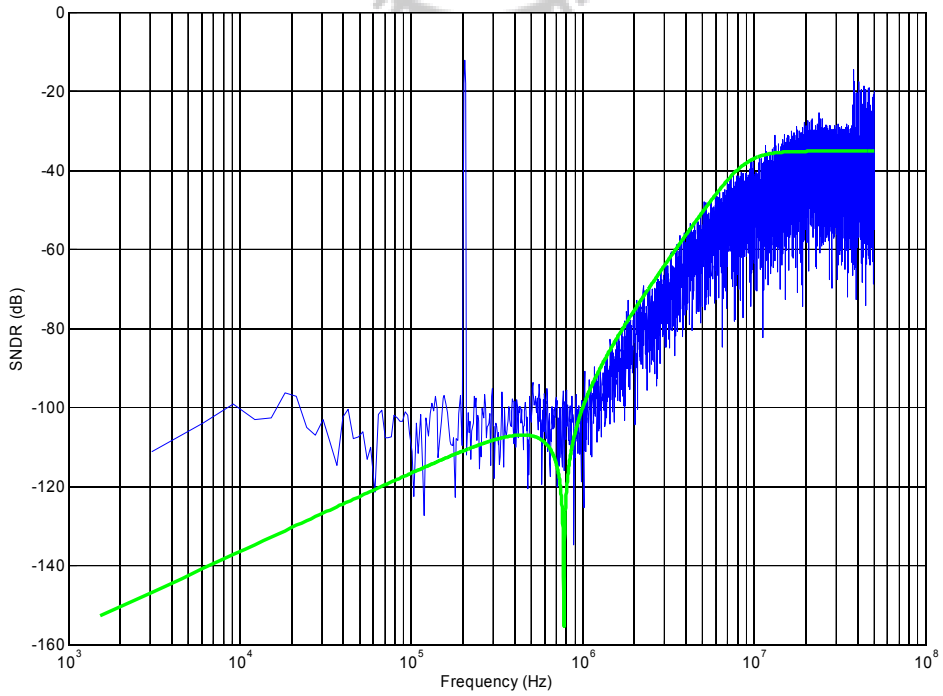


Fig. 4.4 The system simulation of CT ΔΣ modulator using feedback resistors

4.4 Circuit Level Design

4.4.1 Loop Filter

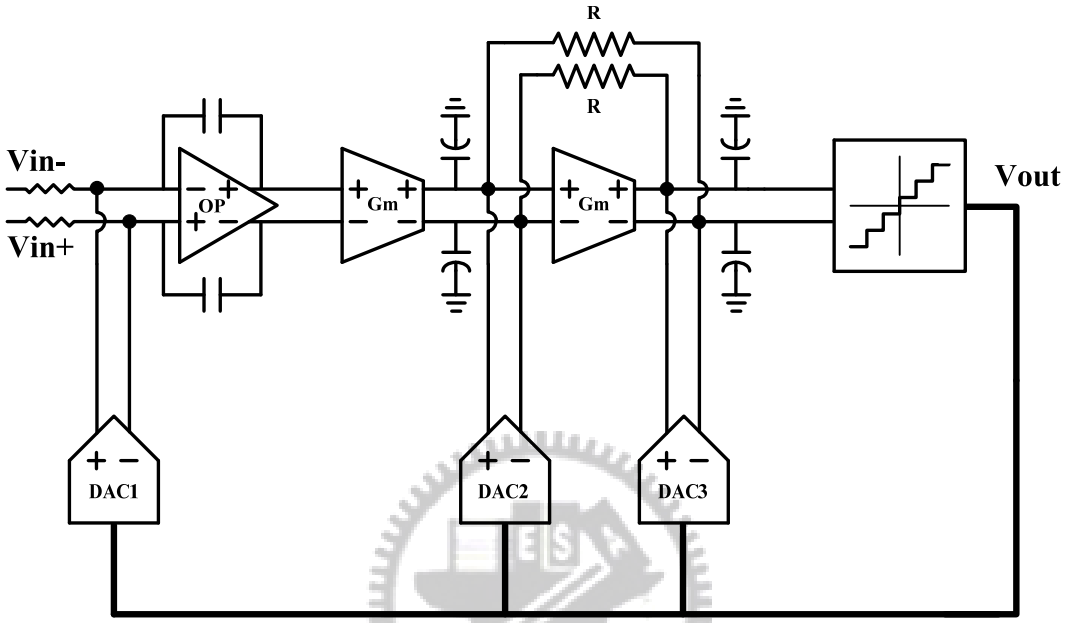


Fig. 4.5 Simplified block diagram of CT ΔΣ modulator using feedback resistors

The third-order loop filter of our first work design is implemented with CRFB architecture, as shown in Fig. 4.5. The first stage is an active-RC integrator and the following resonators are realized by Gm-C integrators and the resistor. The role of the resonators is to shift the poles of the loop filter to optimum non-zero frequencies in order to reduce in-band quantization noise and get more performance, as mentioned in section 4.2.1.

There are three types of commonly used continuous-time integrators: active-RC integrators, Gm-C integrators and MOSFET-C integrators. In our design, the first stage uses an active-RC integrator rather than Gm-C and MOSFET-C integrators for its superior linearity. Gm-C integrators are chosen for the two resonators to save power. If they were active-RC or MOSFET-C integrators, it would increase the

power consumption considerably because two stage opamps are needed to increase the drive capabilities.

4.4.2 First Stage – Active-RC Integrator

As Fig. 4.6 shown, the current steering DAC feedbacks current to the virtual grounds of the active-RC integrators, therefore good DAC linearity can be achieved. Besides better integrator linearity, this is another advantage compared with using a Gm-C integrator for the first stage. Because the error generated in the first stage could not be shaped to high frequency for ΔΣ modulator, the first stage is especially important. If we use Gm-C integrator as first stage, the DAC would have to connect to the high-swing integrator outputs, and hence DAC linearity would be poor and cause the system performance worse.

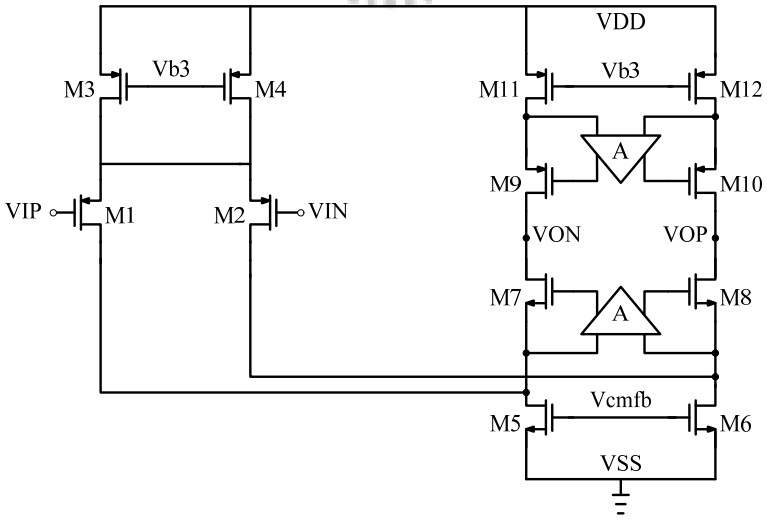


Fig. 4.6 Schematic of gain-boosting folded-cascode OpAmp

The OpAmp in the active-RC integrator uses a folded-cascode topology with a gain enhancement method by adding additional stages to increase DC gain. This method is called gain-boosting [10] [11]. Fig. 4.6 shows the schematic of the gain-boosting folded-cascode OpAmp used in this design. The spice simulation results are shown in Fig. 4.7, including DC gain and phase margin. The detailed specifications are summarized in Table 4.1.

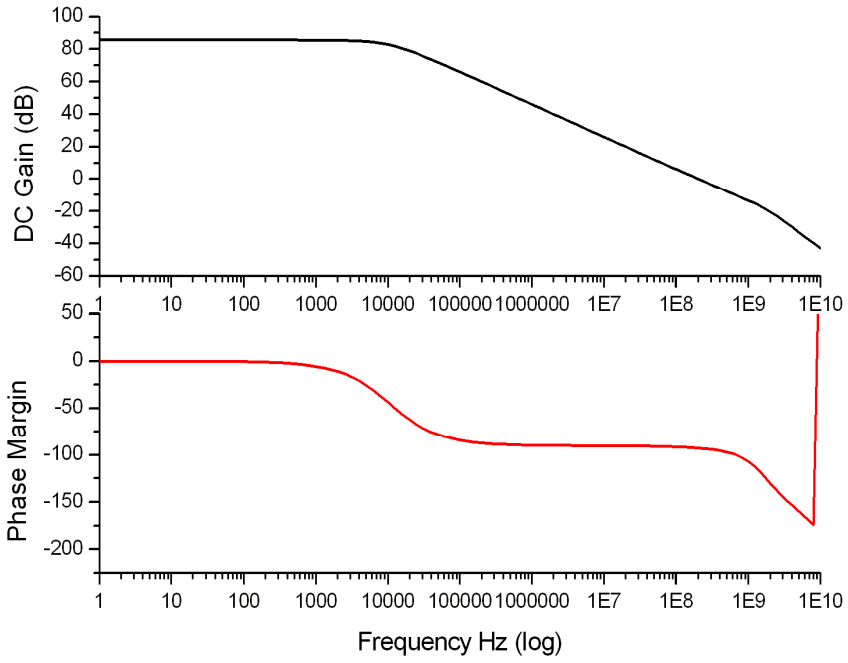


Fig. 4.7 The spice simulation, including DC gain and phase margin

Table 4.1 Summary of spice simulation results

Specification	***Simulation Results***
Technology	TSMC 0.18 μ m 1P6M
Unit Gain Frequency	100 MHz (C_{load} = 3p)
Phase Margin	85°
DC Gain	87 dB
Out Range	1.6 Vpp
Power Supply	1.8 V
Power Dissipation	4.68 mW

Fig. 4.8 shows the common-mode feedback (CMFB) circuit for the folded-cascode OpAmp. We first assume the two pairs have the same differential voltage, therefore, the current in Q_1 will be equal to the current in Q_3, while the current in Q_2 will equal the current in Q_4. This result is valid independent of the nonlinear relationship between a differential pair's input voltage and its large signal differential drain currents. Now, letting the current in Q_2 be denoted as

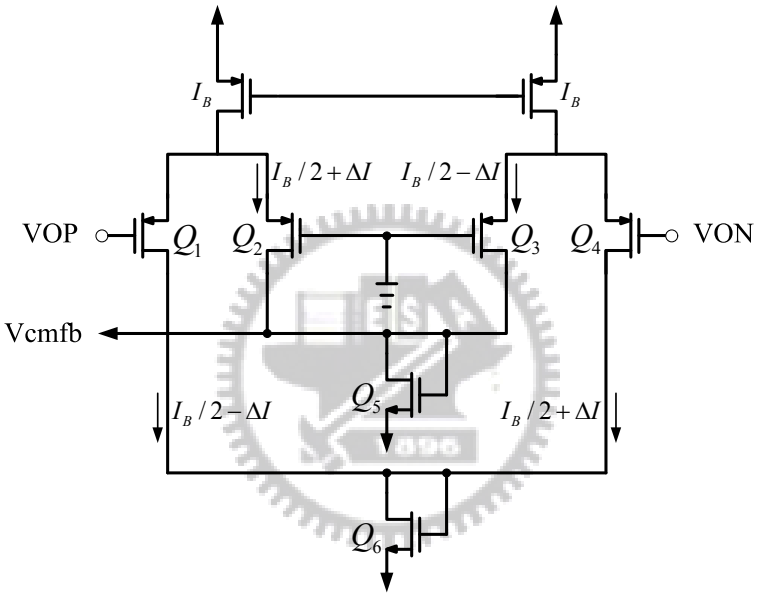


Fig. 4.8 Schematic of CMFB circuit

$I_{D2} = I_B / 2 + \Delta I$, where I_B is the bias current of the differential pair and ΔI is the large signal current change in I_{D2}, the current in Q_3 is given by $I_{D3} = I_B / 2 - \Delta I$ and the current Q_5 in is given by

$$I_{D5} = I_{D2} + I_{D3} = I_B / 2 + \Delta I + I_B / 2 - \Delta I = I_B \qquad (4.1)$$

Thus, as long as the voltage V_{outp} is equal to the negative value of V_{outn}, the current through diode-connected Q_5 will not change even when large differential signal

voltage are present. Since the voltage across diode-connected Q_5 is used to control the bias voltages of the output stage of the OpAmp, this means that when no common mode voltage is present, the bias currents in the output stage will be the same regardless of whether a signal is present or not.

Next, we consider one thing, what happens when a common mode voltage other than zero is present. We first assume a positive common mode signal is present. This positive voltage will cause the currents in both Q_2 and Q_3 to increase, which causes the current in diode-connected Q_5 to increase, which in turn causes its voltage to increase. This voltage is the bias voltage that sets the current levels in the n-channel current sources at the output of the OpAmp. Thus, both current sources will have larger currents pulling down to the negative rail, which will cause the common mode voltage to decrease, bring the common mode voltage back to zero. By this way, as long as the common mode loop gain is large enough, and the differential signals are not as large as to cause transistors into turn-off, the common mode output voltage will be kept very close to ground [3].

The same method is used for the following two Gm-C integrators to obtain output common-mode voltages since each integrator is followed by a transconductor gain stage with the same architecture.

4.4.3 Following Stage – Gm-C Integrator

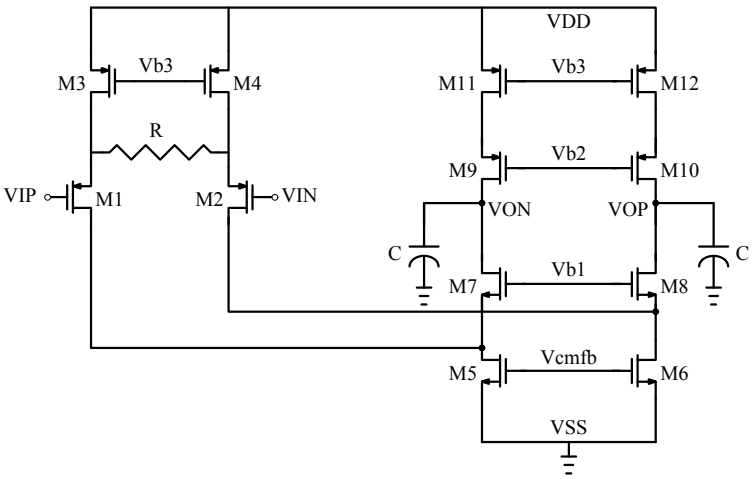


Fig. 4.9 Schematic of Gm with source degeneration resistor

With the exception of the first stage integrator, the following two integrators are implemented with Gm-C integrators to save power. A folded-cascode architecture is used with source degeneration resistor, as shown in Fig. 4.9. It achieves the required linearity and it has independent input-output common mode voltages as well. The constant transconductance is shown in Fig. 4.10, it shows the linear range between -0.5V to 0.5V. The spice simulation results are shown in Fig. 4.11, including DC gain and phase margin. The detailed specifications are summarized in Table 4.2.

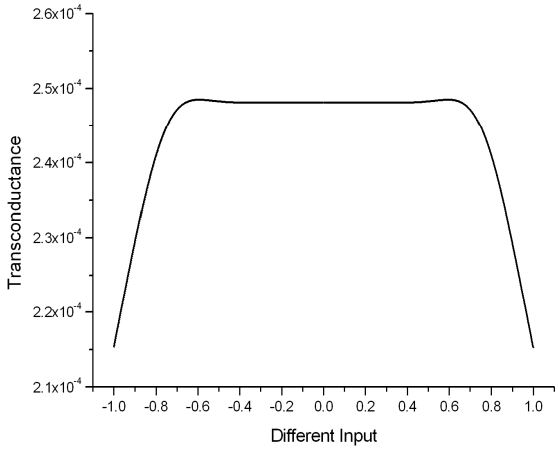


Fig. 4.10 The simulated transconductance range

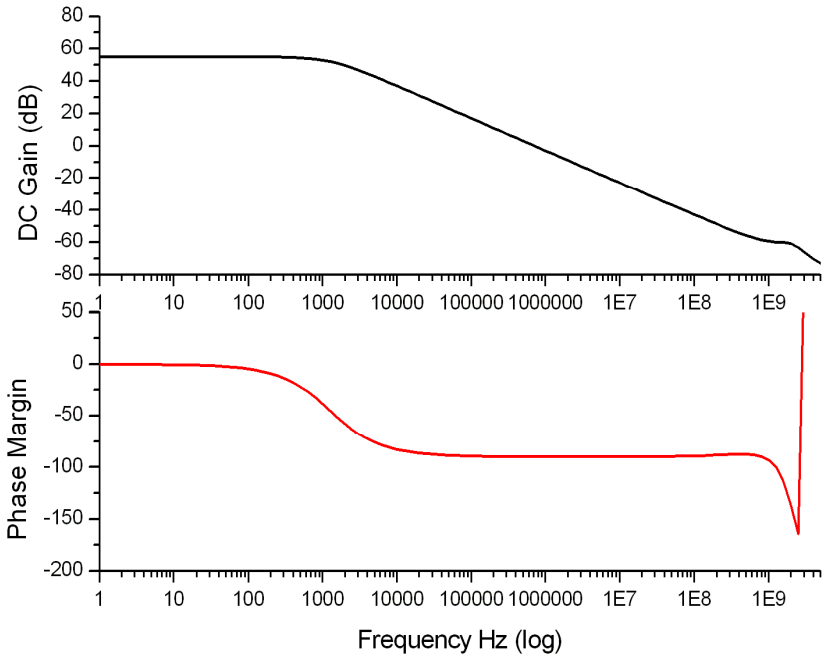


Fig. 4.11 The spice simulation, including DC gain and phase margin

Table 4.2 Summary of spice simulation results

Specification	***Simulation Results***
Technology	TSMC 0.18 μ m 1P6M
Unit Gain Frequency	16 MHz (C_{load} = 3p)
Phase Margin	90°
DC Gain	56 dB
Out Range	1.6 Vpp
Power Supply	1.8 V
Power Dissipation	3.45 mW

4.4.4 Feedback Resistors

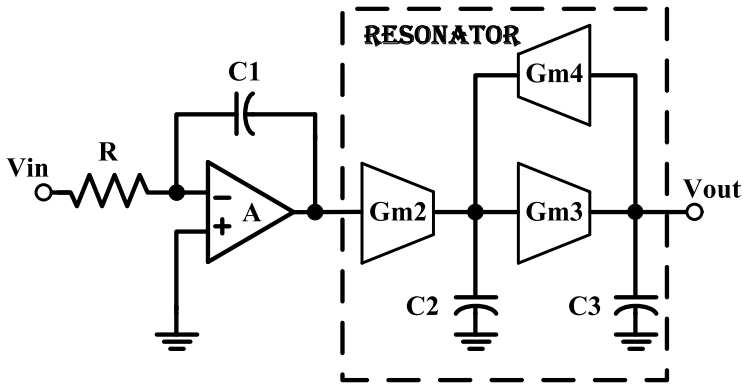


Fig. 4.12 The simplified schematic of loop filter

As previous section mentioned, the role of the resonators is to shift the poles of the loop filter to optimum non-zero frequencies in order to reduce in-band quantization noise and get more performance. In the circuit level, we simplify Fig. 4.5 as Fig. 4.12 to express. We can get the transfer function,

$$\left(-\frac{1}{sRC_1} \times V_{in} \times \frac{Gm_2}{sC_2} - \frac{Gm_4}{sC_2} \times V_{out} \right) \times \frac{Gm_3}{sC_3} = V_{out}$$

$$\frac{V_{out}}{V_{in}} = \frac{-\frac{Gm_2 Gm_3}{RC_1C_2C_3}}{s\left(s^2 + \frac{Gm_3 Gm_4}{C_2C_3} \right)} \qquad (4.2)$$

From (4.2), we can get three poles $s = 0$ and $s^2 + \frac{Gm_3 Gm_4}{C_2C_3} = 0$. Therefore, we can find the shift frequency $f_Z = \frac{1}{2\pi}\sqrt{\frac{Gm_3 Gm_4}{C_2C_3}}$. In general, the implementation of Gm_4 is Gm cell. Considering the chip area and power consumption, due to the Gm_4 is small enough (about $2\mu A/V$), we can replace Gm cell with the resistor. That is, $Gm = \frac{1}{R}$.

4.4.5 Tuning Circuit

The time constant shift due to process variations in practical continuous time circuits can degrade system performance to an unacceptable level. For CT ΔΣ modulators, $\pm 20\%$ variation is more than enough to drive the modulator into unstable operation. To solute this issue, we apply a capacitor array tuning method to adjust the time constants, as shown in Fig. 4.13 [7].

The capacitors in the arrays are binary-sized except the always-in-use capacitors. This sizing method is to provide constant tuning step with the least number of capacitors and to ease layout. The 4-bit digital control codes are fed externally to choose which capacitors to use.

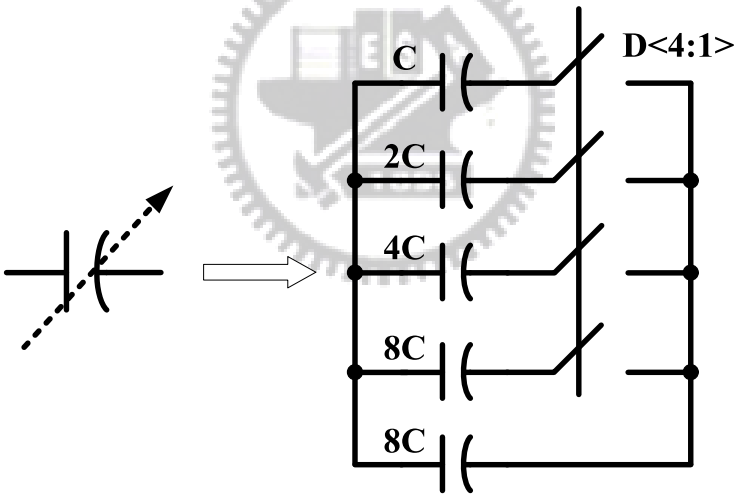


Fig. 4.13 Tunable capacitor array

The total in use capacitor value is:

$$C_{in\ use} = 8C + k \cdot C \quad (k = 0 \sim 15) \tag{4.3}$$

The maximum available capacitance in the array is $C_{max} = 23C$, and the minimum available capacitance in the array is $C_{min} = 8C$. For normal

operation, the capacitor value is $C_{normal} = 16C$. Therefore, the tuning range of the integration capacitor arrays is $\frac{23C - 16C}{16C} \sim \frac{8C - 16C}{16C}$ $(+43.75\% \sim -50\%)$, which suffice for the requirements of this modulator according to 20% capacitor process variations.

4.4.6 Low Jitter Clock Generation

All the system blocks are synchronized by a clock to implement the function. As previous sessions discuss, CT ΔΣ modulators are sensitive to clock jitter. Therefore, this clock needs to have sufficiently low jitter in order not to increase the modulator output noise floor due to non-shaped jitter noise. In our design, system level simulations show that less than 20ps clock jitter is required. Some design strategies are adopted to minimize clock jitter due to device and supply noise. Fig. 4.14 shows the simplified circuit to generate the low jitter clock.

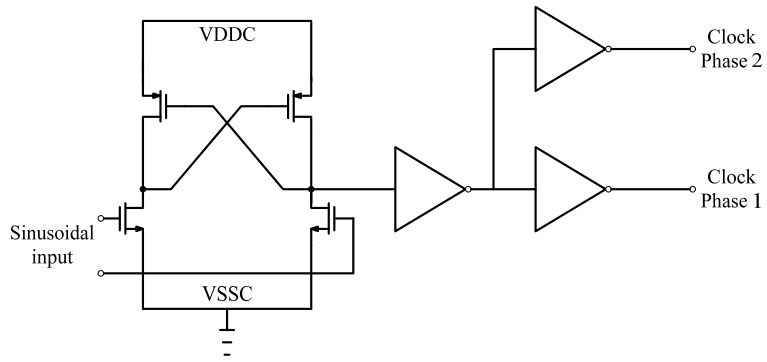


Fig. 4.14 Schematic of low jitter clock generation

To reduce common mode noise probably coupled to the testing board and to obtain the least amount of clock jitter from the external clock source, sinusoidal

differential clock inputs are generated on board and fed to the modulator. It is critical to use as few clock driver stages as possible to generate the low jitter clock with sufficient driving capability because any extra stages generate extra device noise, hence larger clock jitter. To reduce the supply noise, a dedicated and clean supply is used solely for the low jitter clock generation circuit [12].

4.5 Circuit Level Simulation

The circuit level results are simulated by Hspice. The captured output digital data is windowed by a Hann window and a Fourier transformation is applied using Matlab. The spectra resulting (16384 bins from 0 to FS) from -6 dB 94.6 kHz input signal can be seen in Fig. 4.15. The total power consumption is 13.6 mW. The finial specifications are summarized in Table 4.3. The chip photo is shown in Fig. 4.16. The total area, including pad is 1.14 x 0.945 mm^2.

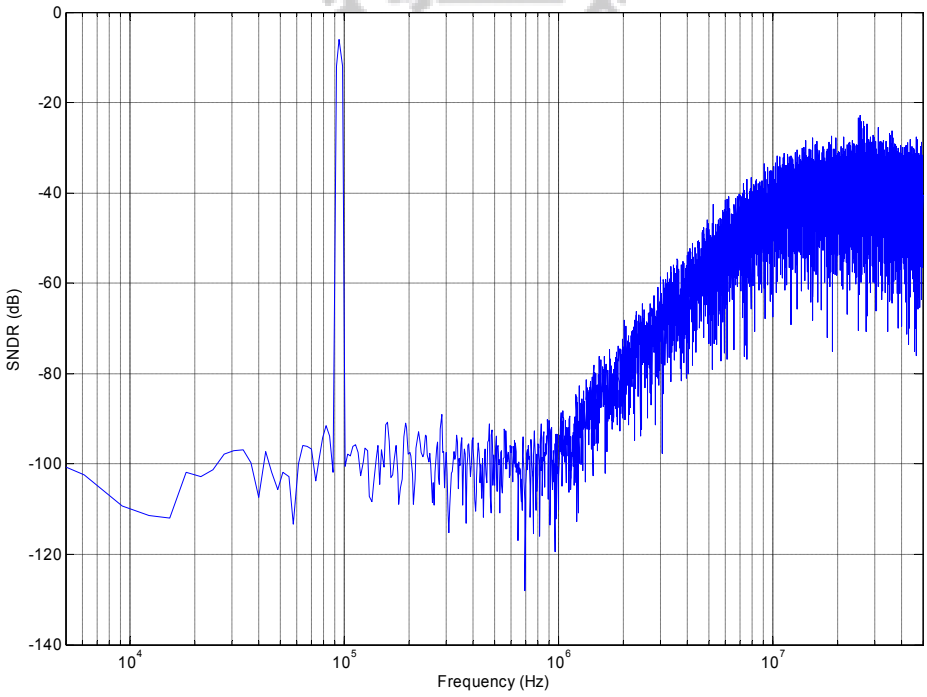


Fig. 4.15 The circuit simulation of this work using feedback resistors

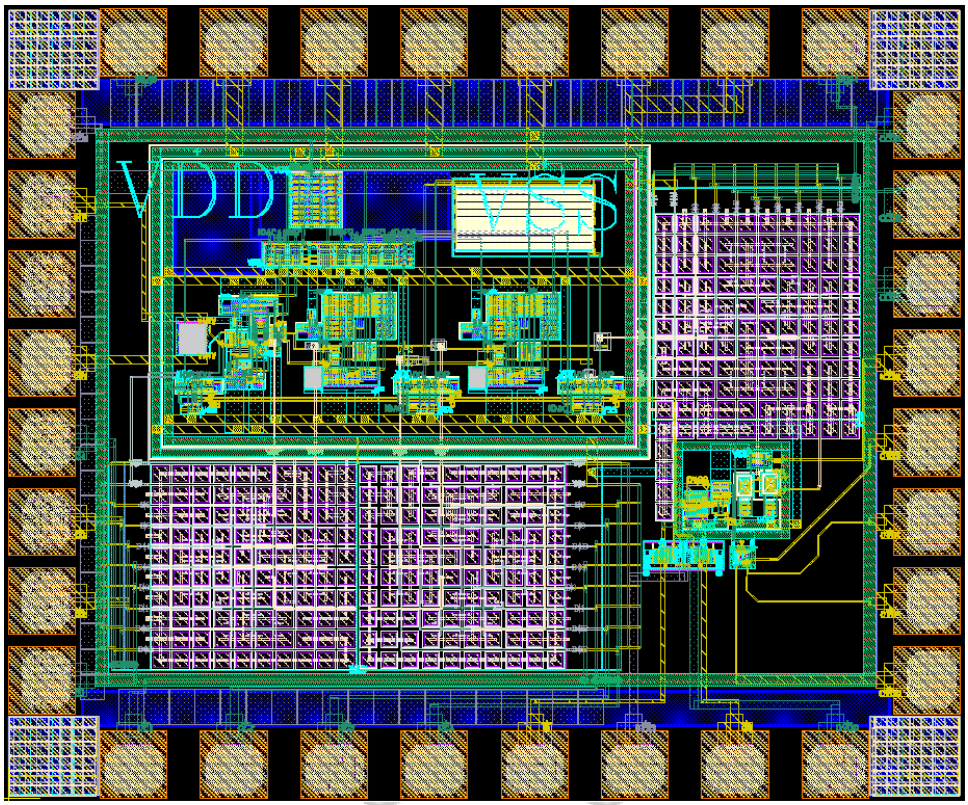


Fig. 4.16 Chip photo of this work using feedback resistors

Table 4.3 Summary of circuit level simulation results

Specification	***Simulation Results***
Technology	TSMC 0.18μm 1P6M
Signal bandwidth	1 MHz
Sampling frequency	100 MHz
SNDR	67.3 dB
SFDR	78 dB
ENOB	11
Power Supply	1.8 V
Power Dissipation	13.6 mW
Chip area (with pad)	1.14 mm x 0.945 mm

Chapter 5

A Continuous-Time DSM with Improved Zero-Order Loop Compensation and Semi-Uniform Quantization

In this chapter, the system level and circuit level design of our second chip is presented in detail, which includes the determination of the system level parameters, and the system level simulations with non-idealities. After that, the circuit blocks would be discussed and the modulator is realized with a 0.13 μm CMOS technology and 1.2 V power supply voltage.

5.1 System Level Design

In this second work, the target is to successfully design a CT ΔΣ modulator to reach 63 dB SNDR (signal-to-noise-and-distortion-ratio) within a 2 MHz bandwidth (BW) in a 0.13 μm mixed-signal CMOS process.

For this second work, the clock jitter sensitivity is still the important specification. It will significantly affect the selection of the system level parameters. Therefore, we still assume that the modulator will be evaluated with a clock signal generated by the instrument and determine the RMS value of the target jitter tolerance is 20 ps. Here, for lower power consumption and clock jitter sensitivity, we choose 13 as our OSR value.

For this design, we determine the number of the quantizer be eight. On the other hand, we also choose 3 as the loop order. The aggressiveness of the noise shaping is also limited by the stability issue. In addition, the real input amplitude cannot reach the peak input value because of the input range of Gm-C which as our second and third integrator. The finite RC time constant accuracy will also reduce the effectiveness of the noise shaping. Based on these requirements, a large amount of simulations were performed by using the MATLAB toolbox to explore the parameter space.

5.2 Architecture of the Loop Filter

5.2.1 Out-of-Band Quantization Gain

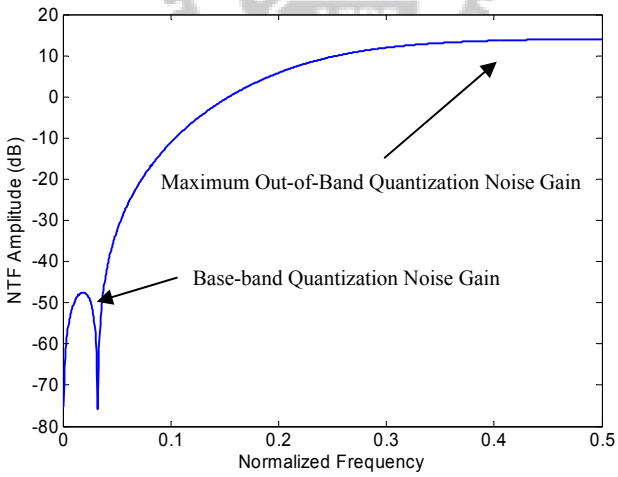


Fig. 5.1 Noise transfer function amplitude of a ΔΣ modulator

In Fig. 5.1, we illustrate the design of ΔΣ ADCs with the maximum out-of-band quantization noise gain Q_{max}. When the out-of-band quantization noise gain is high, we find the in-band noise shaping provide greater attenuation of the quantization

noise. However, increasing Q_{max} will cause the ΔΣ system more unstable. According to Lee criterion [13], the Q_{max} of a ΔΣ modulator with a 1-bit quantizer must be less than 1.5 to maintain stable modulator performance. If a multibit quantizer is used, the quantization noise error is much lower. It is very natural to think that a much higher value of Q_{max} can be used to improve the signal to noise ratio (SNR) [14].

Fig. 5.2 shows the simulated signal-to-noise ratio (SNR) of different quantization bit third order ΔΣ modulators. When Q_{max} increases, SNR also increases and the performance gain is almost 20 dB when Q_{max} is much greater than 1.5. Thus, Q_{max} plays an important role in the performance of ΔΣ modulators. When advanced CMOS processes, the power supply voltage becomes lower and it also causes the input range of the transconductor lower. This leads to the dynamic range of delta-sigma modulator decrease because we usually define the output swing of the OpAmp in the first integrator or the input range of the transconductor in the second integrator as our full scales (FS) range which is also our maximum dynamic input range. When the value of the FS is decreased as the power supply voltage been lowered, one thing we can do is to make the in-band noise flow lower to maintain the same SNR.

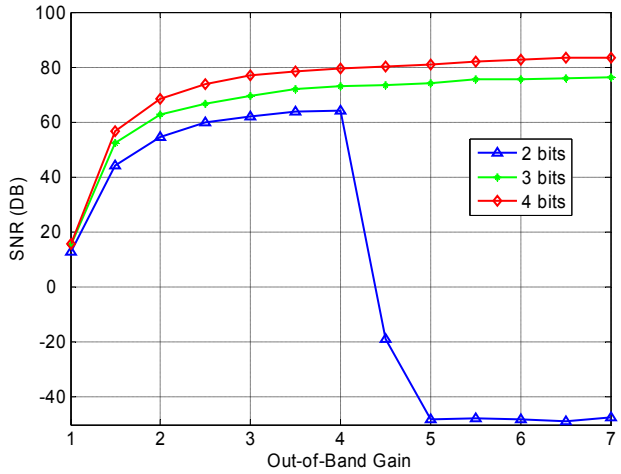


Fig. 5.2 Simulated SNR as a function of Q_{max} for different quantization bit third order ΔΣ modulators (OSR = 16)

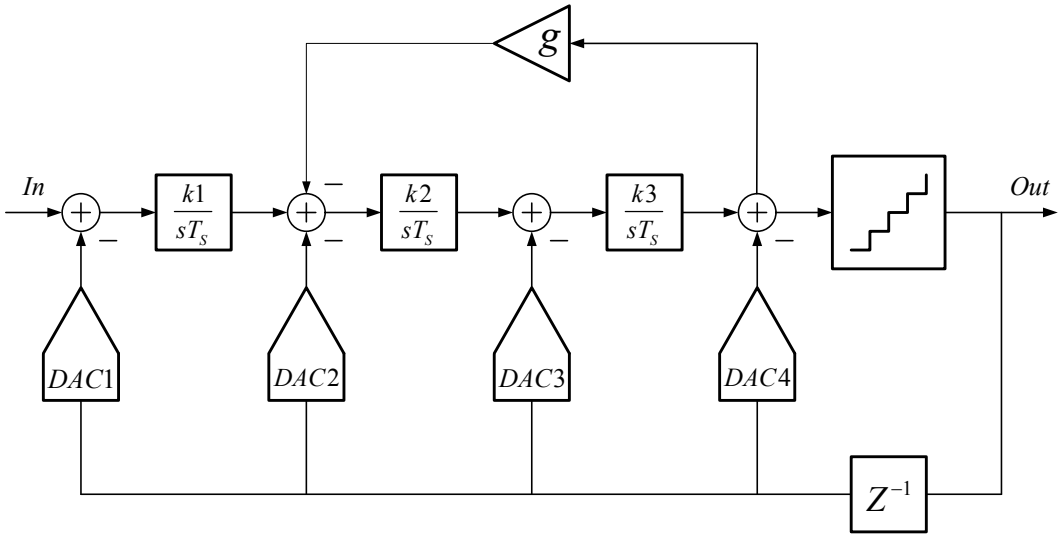


Fig. 5.3 Continuous-Time ΔΣ modulator architecture with compensation loop

Although increasing out-of-band quantization noise gain we can get some advantage, we also must pay for the cost. The cost is that it causes the system unstable easily. To overcome the problem, a D-flip-flop (DFF) that is in front of the DAC is used to fix the timing of the feedback pulse, as the Fig. 5.3 shown.

5.2.2 Improved Zero-Order Loop Compensation

Fig. 5.3 shows a block diagram of the 4-bit CT ΔΣ modulator including improved zero order loop compensation. With the exception of three integrators, DAC1, DAC2 and DAC3 realize the feedback paths, and together with DAC4 which it is used to realize the direct zero-order path around the semi-uniform quantizer, as will be explained later [15]. The digital input of DAC4 is delayed by a DFF to realize a full clock period delay. Generally, the implementation of the zero-order loop would require a summing amplifier. This leads to higher power consumption. Moreover, the implementation of the RZ DAC increases design complexity and power consumption. To avoid this problem, we use the differentiation operation

which means the DAC4 is introduced in the direct feedback path. It allows the signal to be fed to the input of the third integrator. As Fig. 5.4 shown, we generate a loop filter function with a half sample delay using the MATLAB Control System Toolbox at first. Then, we make the DAC4 feed to the input of the third integrator and multiply $s\,T_S$ together to make the equation equal. Following, we replace the continuous-time differentiation operation by discrete-time differentiation operation. Finally, expanding the parameter of DAC3 and DAC4, we get the results

$$\begin{aligned} & DAC3 \times Z^{-\frac{1}{2}} + DAC4 \times \left(1 - Z^{-\frac{1}{2}}\right) \times Z^{-\frac{1}{2}} \\ &= \left(DAC3 + DAC4\right) \times Z^{-\frac{1}{2}} - DAC4 \times Z^{-1} \\ &= DAC3' \times Z^{-\frac{1}{2}} - DAC4 \times Z^{-1} \end{aligned} \tag{5.1}$$

By this way, an additional summing amplifier could be avoided. Because the continuous time differentiation is difficult to implement, this is instead carried out in discrete time. In order to make the direct feedback signal available at the correct time, the differentiation operation works at a half clock period delay. By this excess loop delay compensation, we avoid the need for an additional summing amplifier which would increase power consumption.

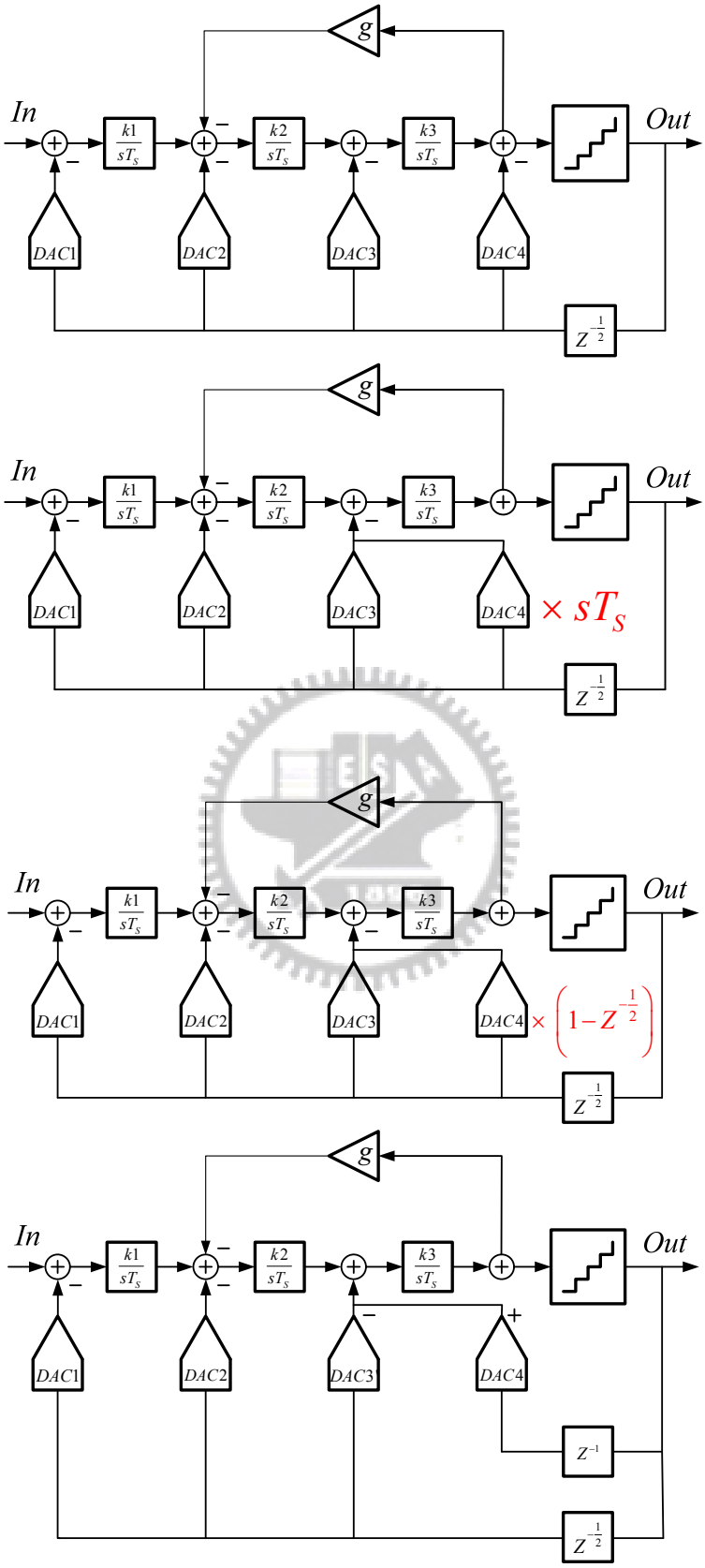


Fig. 5.4 Realization of the zero-order loop feedback path

5.2.3 Non-Uniform Quantization

Most of the quantization performed in A/D conversion is uniform quantization, which means the quantization steps are equal. Considering the low input range of the transconductor in the low power supply voltage design, to reduce the overall quantization error power, which is expressed in (5.2).

$$P_{\varepsilon} = \int_{-\infty}^{\infty} \rho(x)\varepsilon^{2}(x)\,dx \tag{5.2}$$

Its quantization error $\varepsilon(x)$ is smaller when the amplitude of x is small, and its $\varepsilon(x)$ is larger when the amplitude of x is large. Therefore, the precondition to use a non-uniform quantizer is that the quantizer input distribution concentrates in the small-amplitude range, so that the overall noise power can be reduced by using a non-uniform quantizer. Fortunately, this precondition is satisfied with our low input range of transconductor.

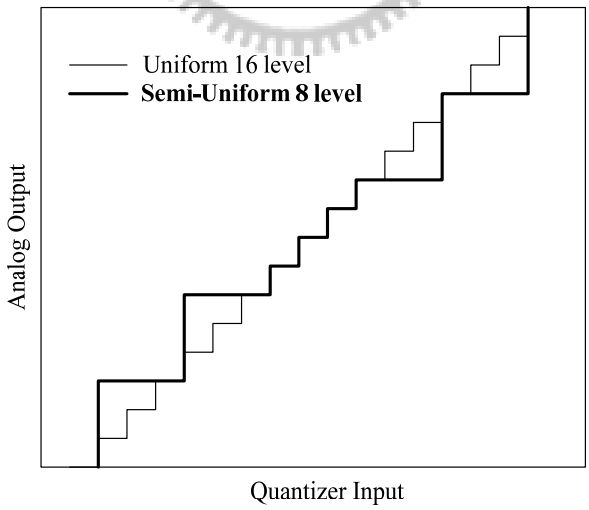


Fig. 5.5 The transfer curve of semi-uniform quantization

The name "semi-uniform" means that there are only two different-size quantization steps [16] [17] [18]. In other words, the small quantization step is for

small inputs and the large step for large inputs. In effect, for this 8-level semi-uniform quantizer with normalized full scale range of -1 ~ +1, the center four quantization steps have a step size of $\Delta_1 = \Delta$, and the outer four quantization steps have a step size of $\Delta_2 = 3\Delta_1$.

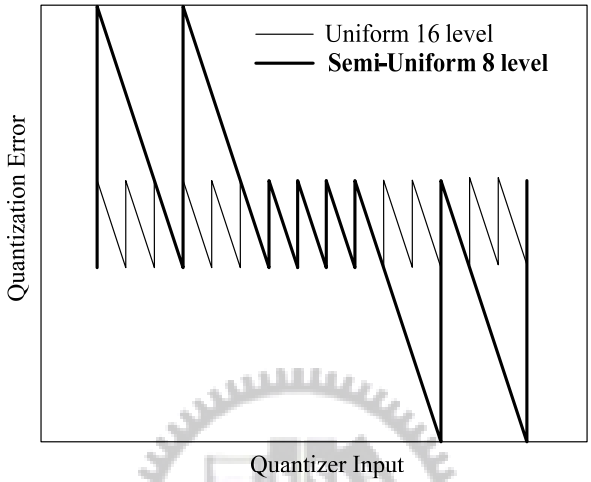


Fig. 5.6 The quantization error of semi-uniform quantization

Fig. 5.5 and Fig. 5.6 show the quantization levels and quantization error of an 8-level semi-uniform quantizer, compared with a 16-level uniform quantizer. At the five center steps, the quantization error of both the 8-level semi-uniform and 16-level uniform quantizers are the same, while at the outer steps the semi-uniform quantization error can be three times as large as that of the 16-level uniform quantizer. This implies that if most of the quantizer inputs fall into those small quantization steps, a k-bit semi-uniform quantizer could achieve the same dynamic range as a (k+1)-bit uniform quantizer. This helps us saving a lot of power and chip area for our low voltage input.

5.2.4 Dynamic Element Matching

Dynamic element matching (DEM) algorithms are often used in multi-bit modulators to increase DAC linearity. Because of the element mismatches in the multi-bit DAC, they introduce an output error which consists of the harmonics of input signal as well as an increased noise floor due to the folding of high frequency quantization noise into the baseband [9]. To convert the energy of the harmonic spurs into a pseudo-random noise, an error randomization technique is used. The process can be carried out if the input of DAC is a thermometer coded digital signal, and the DAC is built from unit elements (Here we use current sources). The error randomization conversion is performed by activating K unit elements if the value of input code is K, as Fig 5.7 shown. The error randomization is achieved by choosing these K unit elements circularly each time. For the use of DEM, the DAC error e(n) at time n will not be correlated with the value of its input v(n). Therefore, the signal distortion is replaced by random noise in the DAC output.

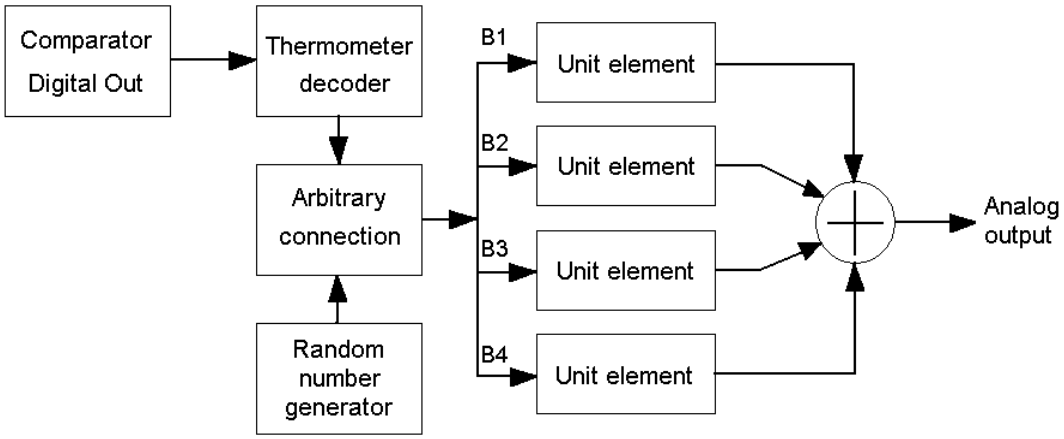


Fig. 5.7 Unit element DAC with randomized element selection

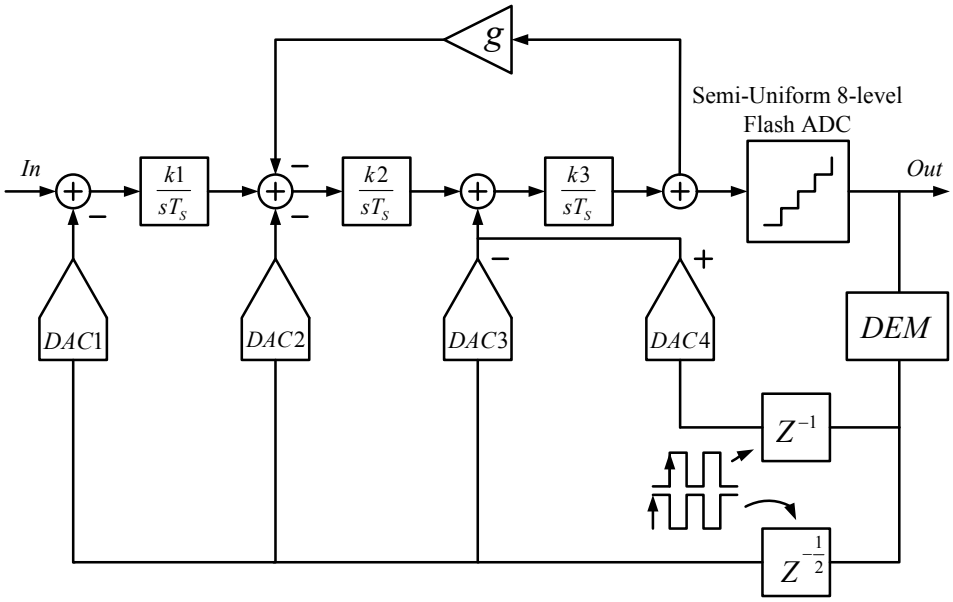


Fig. 5.8 The architecture of CT ΔΣ modulator we propose

In Fig. 5.8, we show the architecture of CT ΔΣ modulator we propose. The loop filter architecture we use is feedback structure with improved zero-order loop compensation, semi-uniform quantization and DEM.

5.3 System Level Simulation

As mentioned before, taking the non-idealities into account, we show the system analysis of DC gain and HD3 in the first active-RC integrator, as illustrated in Fig. 5.9 and Fig. 5.10. In Fig. 5.11 and Fig. 5.12, we show the system analysis of DC gain and HD3 in the second Gm-C integrator. We find the DC gain 60dB and 40dB are sufficient in the first integrator and second integrator, respectively. And the HD3 90dB and 70dB are sufficient in the first integrator and second integrator, respectively. Fig. 5.13 shows the output spectrum in this system level simulation of the modulator, which includes all the non-idealities except the thermal noise. As a comparison, the ideal noise transfer function is also plotted in this figure.

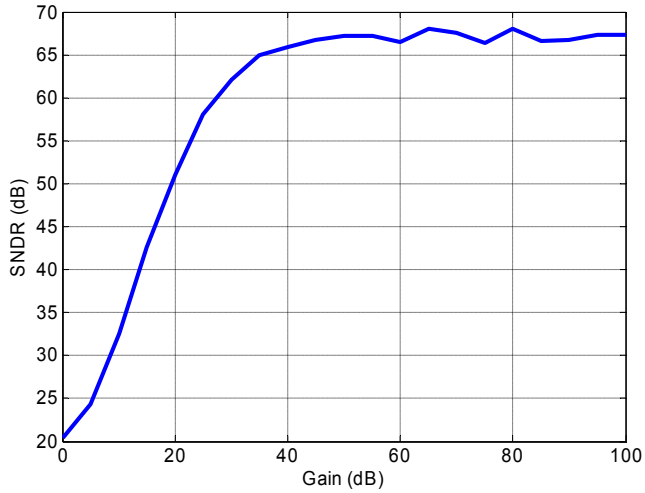


Fig. 5.9 The simulation of DC gain in first active-RC integrator

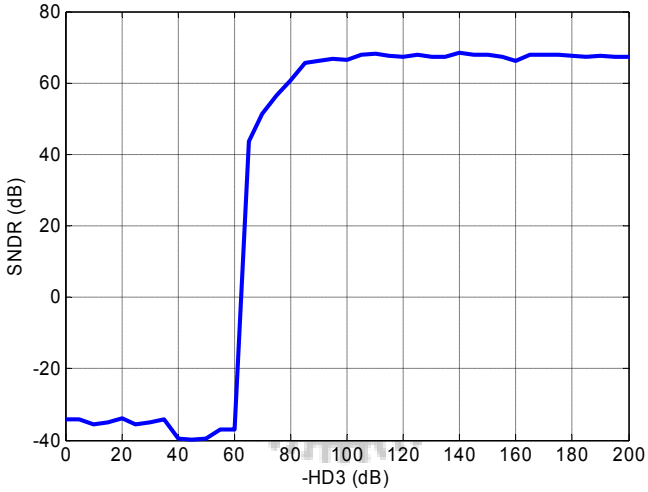


Fig. 5.10 The simulation of HD3 in the first active-RC integrator

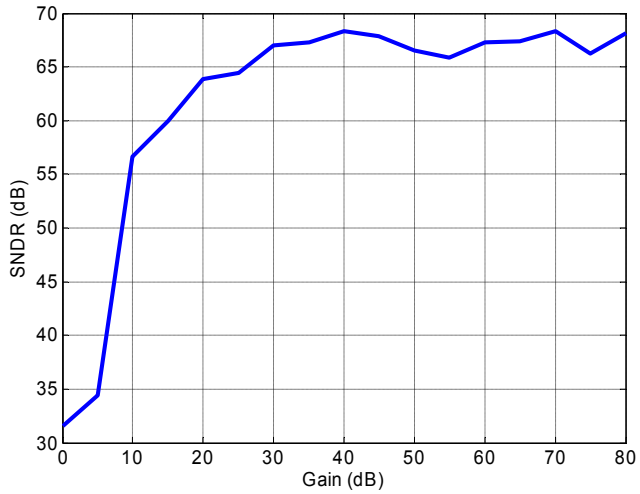


Fig. 5.11 The simulation of DC gain in the second Gm-C integrator

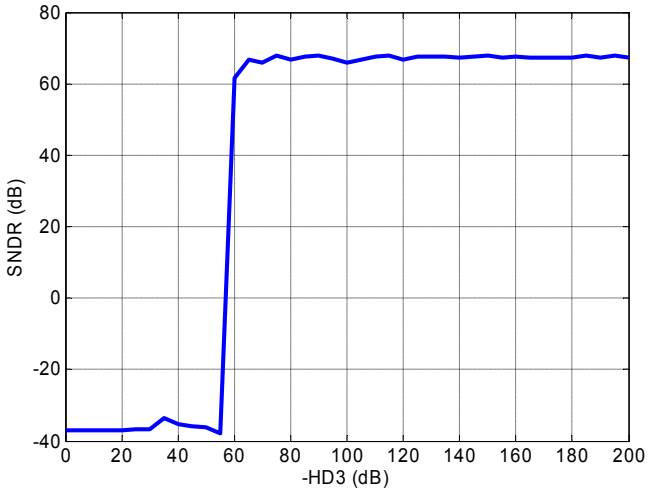


Fig. 5.12 The simulation of HD3 in the second Gm-C integrator

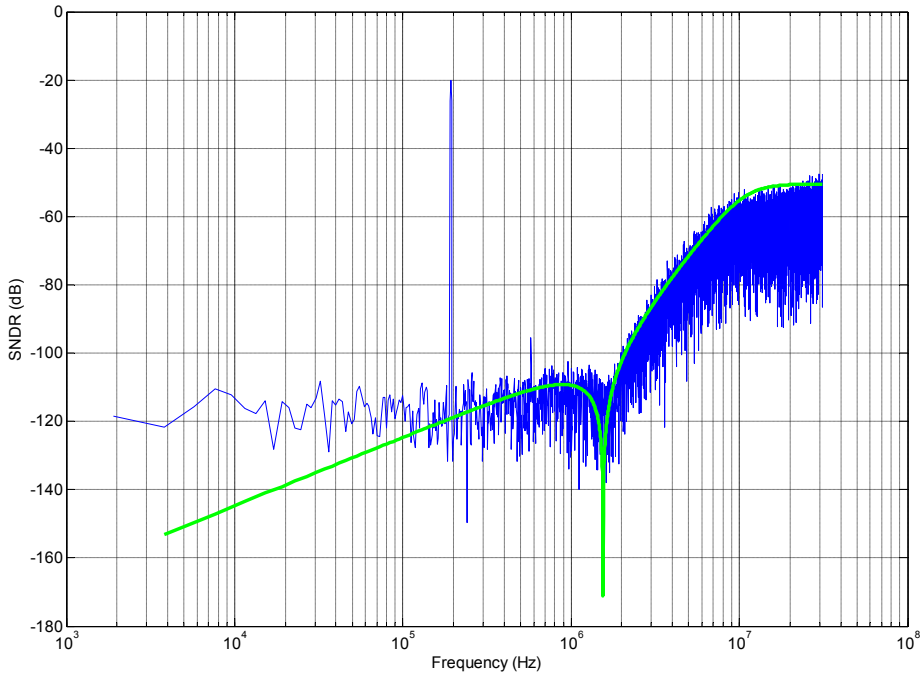


Fig. 5.13 The system simulation of CT ΔΣ modulator we propose

5.4 Circuit Level Design

5.4.1 Loop Filter

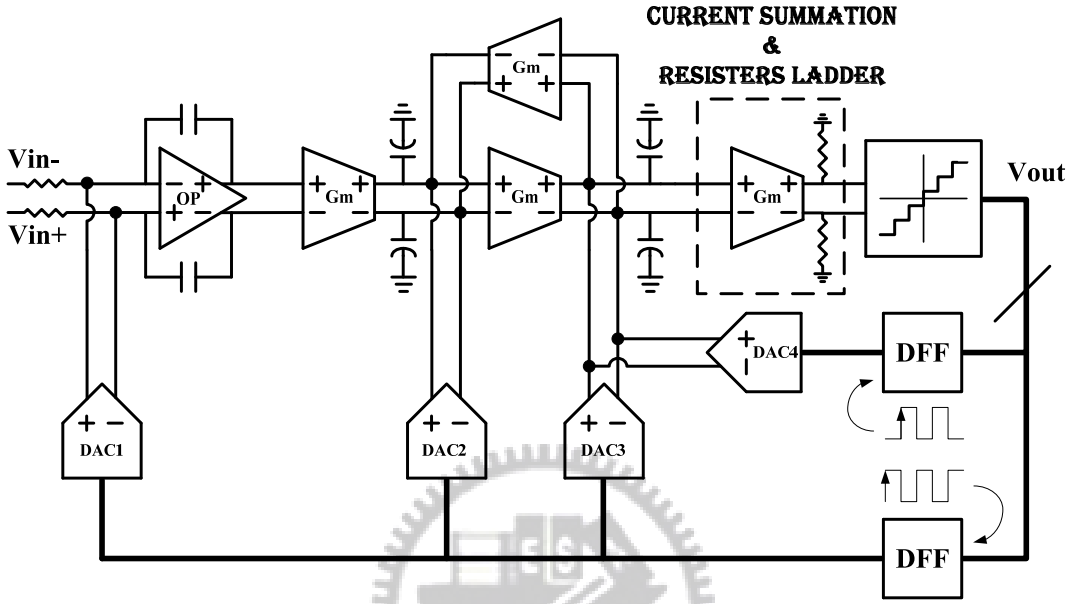


Fig. 5.14 Simplified block diagram of the third-order CT ΔΣ modulator

The third-order loop filter of our second design is implemented with CRFB architecture, as shown in Fig. 5.14. The first stage is an active-RC integrator and the following resonators are realized by Gm-C integrators. The role of the resonators is to shift the poles of the loop filter to optimum non-zero frequencies in order to reduce in-band quantization noise and get more performance. The two gain stages are also transconductors which convert the integrators' outputs from voltages to currents and then convert back to voltages through a resistors ladder. The voltages on the resistors ladder are sampled by the semi-uniform multi-bit quantizer to generate the modulator digital outputs. The thermometer-coded outputs control the four current steering DACs to generate feedback currents, feeding to the each stage of modulator input.

In this design, the first stage also uses an active-RC integrator for its superior linearity. Gm-C integrators are chosen for the two resonators to save power.

5.4.1 First Stage – Active-RC Integrator

The OpAmp in the active-RC integrator uses a folded-cascode topology. Compared with the telescopic OpAmp and the two-stage OpAmp, the folded-cascode OpAmp achieve the tradeoff between the power consumption and output swing in our 0.13 μm CMOS design (VDD = 1.2 V). Fig. 5.15 shows the schematic of the folded-cascode OpAmp used in this design. NMOS transistors are used for the input pair to provide a high speed path for the input. In addition, given the same biasing current and size, a NMOS transistor has larger transconductance than a PMOS transistor. Therefore, input referred thermal noise is lower when NMOS transistors are used for the input pair than if PMOS transistors are used. The spice simulation results are shown in Fig. 5.16, including DC gain and phase margin. The detailed specifications are summarized in Table 5.1.

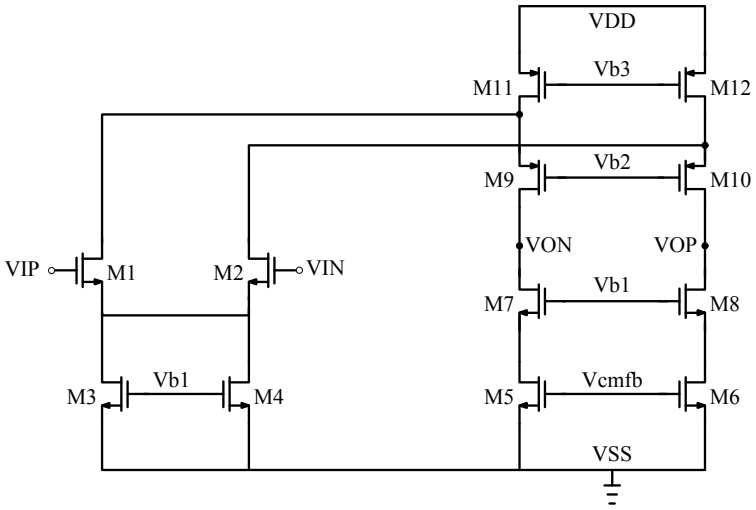


Fig. 5.15 Schematic of folded-cascode OpAmp

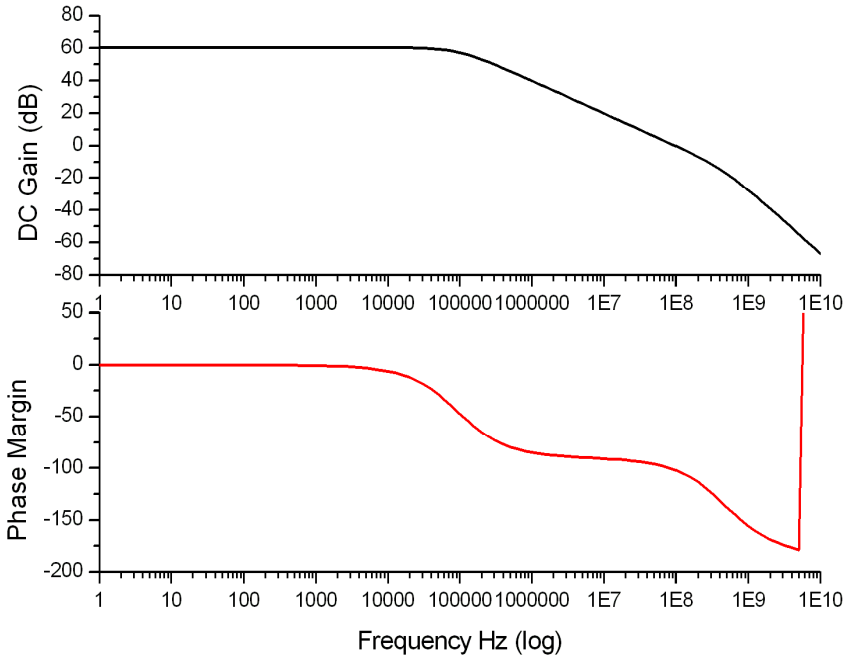


Fig. 5.16 The spice simulation, including DC gain and phase margin

Table 5.1 Summary of spice simulation results

Specification	***Simulation Results***
Technology	TSMC 0.13 μm 1P8M
Unit Gain Frequency	100 MHz (C_{load} = 8p)
Phase Margin	78°
DC Gain	61 dB
Out Range	1.0 Vpp
Power Supply	1.2 V
Power Dissipation	2.45 mW

5.4.3 Following Stage – Gm-C Integrator

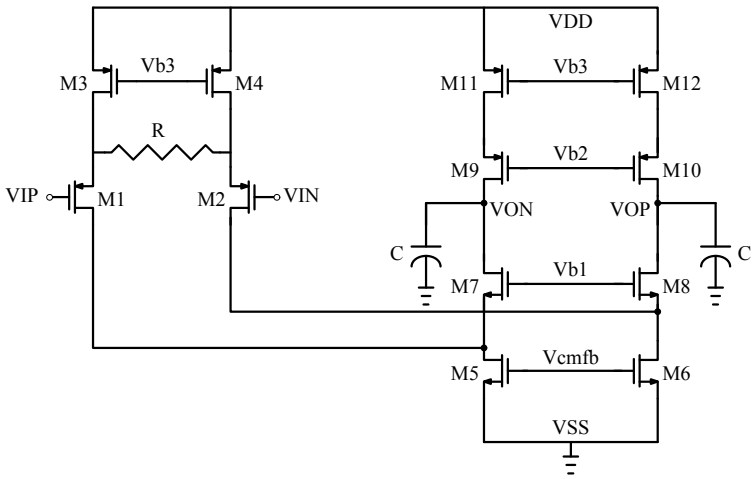


Fig. 5.17 Schematic of Gm with source degeneration resistor

A folded-cascode architecture is used with source degeneration resistor, as shown in Fig. 5.17. It achieves the required linearity and it has independent input-output common mode voltages as well. The constant transconductance is shown in Fig. 5.18, it shows the linear range between -0.2V to 0.2V. The spice simulation results are shown in Fig. 5.19, including DC gain and phase margin. The detailed specifications are summarized in Table 5.2.

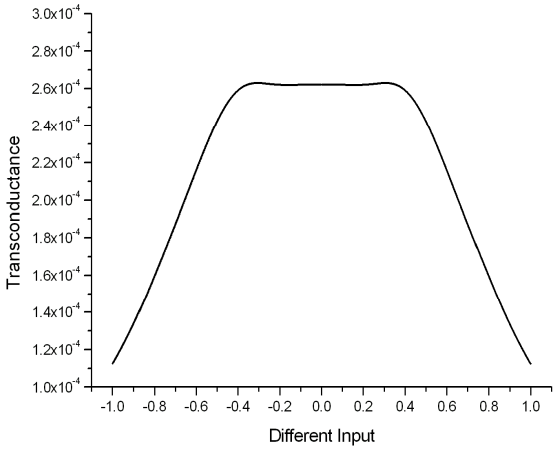


Fig. 5.18 The simulated transconductance range

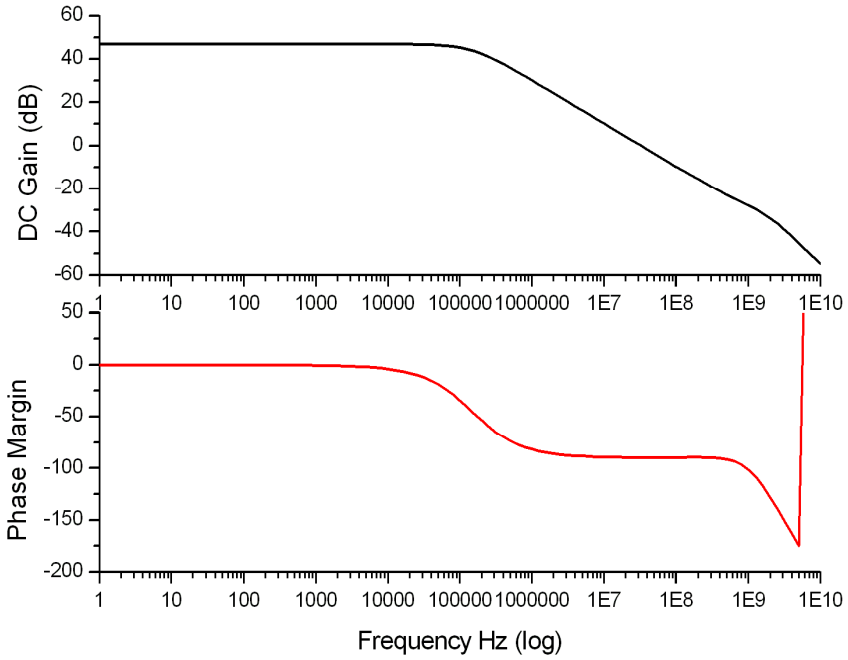


Fig. 5.19 The spice simulation, including DC gain and phase margin

Table 5.2 Summary of spice simulation results

Specification	***Simulation Results***
Technology	TSMC 0.13 μm 1P8M
Unit Gain Frequency	33 MHz (C_{load} = 3p)
Phase Margin	90°
DC Gain	47 dB
Out Range	1.0 Vpp
Power Supply	1.2 V
Power Dissipation	1.51 mW

5.4.4 Current Steering DAC with Semi-Uniform Quantization

Fig. 5.20 shows the schematic of the unit current steering DAC cell. The current cell is composed of four transistors which are current source M1, cascode transistor M2 and two switches (M3 and M4). The cascode transistor is used to increase the output impedance of the current source, and at the same time, to prevent the dynamic glitches at the node A from impacting the current in M1. However, adding this cascode transistor reduces the allowable saturation voltage of M1 and hence the noise performance of the current DAC. The gates of the switch transistors are controlled by the complementary digital feedback signals, D and Db.

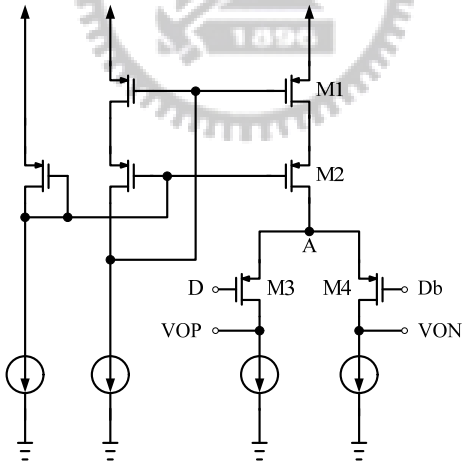


Fig. 5.20 Schematic of the unit current steering DAC cell

When the 8-bits digital codes are high, the system must minus the value of FS. For the use of active-RC integrator, the current value of FS is

$$I_{DAC} = \frac{V_{Ref}}{R} \tag{5.3}$$

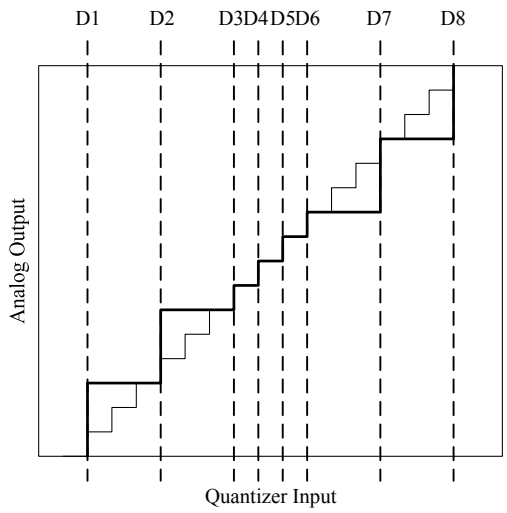


Fig. 5.21 The determination of digital codes in semi-uniform quantization

where V_{Ref} is the voltage value of FS and the R is resistor value of aictive-RC. For the use of Gm-C integrator, the current value of FS is

$$I_{DAC} = Gm \times V_{Ref} \tag{5.4}$$

where V_{Ref} is the voltage value of FS and the Gm is the transconductance value of Gm-C. Considering the semi-uniform quantizer, there are two kinds of quantization intervals, that is to say, the feedback current could not be the same when one bit digital code changes. As Fig. 5.21 shown, when one of D3, D4, D5 and D6 changes, the variation of current would be $I_{DAC}/16$; when one of D1, D2, D7 and D8 changes, the variation of current would be $3I_{DAC}/16$.

5.4.5 Current Summation Circuit

Before the quantizer, a current summation circuit (adder) is needed. The speed of this adder is one of the most critical issues in the modulator design. If a passive adder is used, it will be very sensitive to the parasitic input capacitors of the quantizer. If an active voltage adder is used, an extremely fast OpAmp is needed, which will cost large power. In our design, a fast and low power active current adder is used to realize this summation operation [19], as shown in Fig. 5.22.

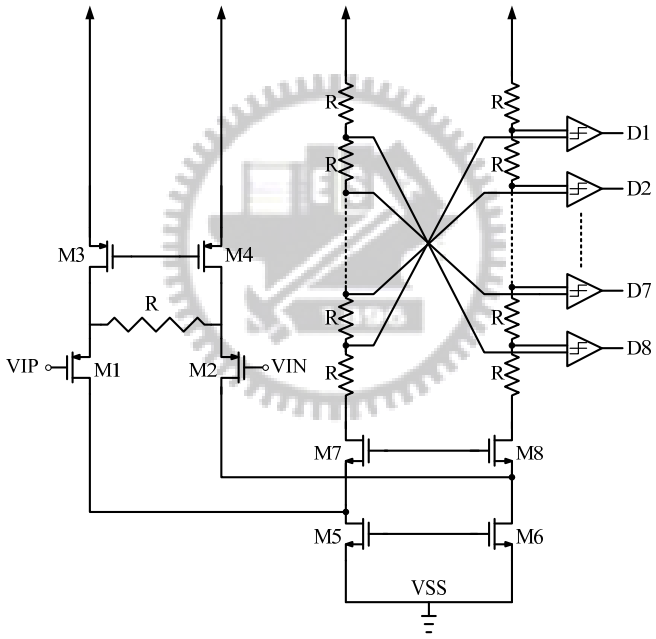


Fig. 5.22 Schematic of the current summation circuit

In the summation circuit, the loop filter output are transformed from voltage to current with the transconductor (Gm) cell which are shown in left side of Fig. 5.22, and then fed into the resistor ladder at the cascode nodes of the two current sources (M5, M6, M7 and M8). In order to increase the linearity of the Gm cell, the input voltage-current (V-I) conversion is realized with source degeneration resistor, as the

same before. Due the use of source degeneration resistor, a very linear V-I conversion is obtained without difficult matching requirements for the MOS transistors.

5.5 Circuit Level Simulation

The circuit level results are simulated by Hspice. The captured output digital data is windowed by a Hann window and a Fourier transformation is applied using Matlab. The spectra resulting (16384 bins from 0 to FS) from -20 dB 156 kHz input signal can be seen in Fig. 5.23. The total power consumption is 10 mW. The finial specifications are summarized in Table 5.3. The chip photo is shown in Fig. 5.24. The total area, including pad is 1.1 x 0.9 mm^2.

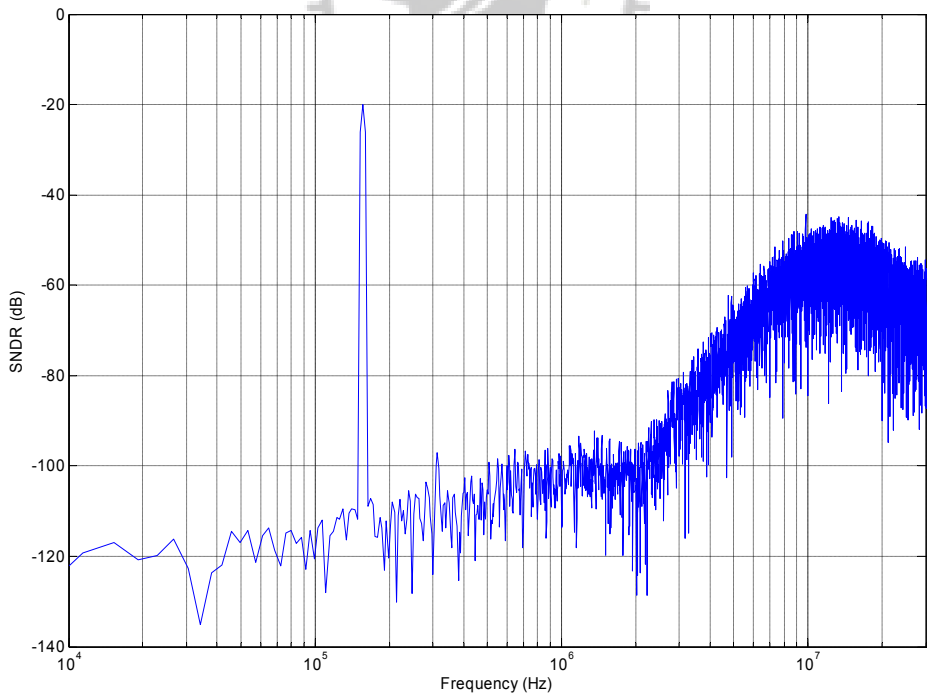


Fig. 5.23 The circuit simulation of this work (16384pt, 156 kHz input)

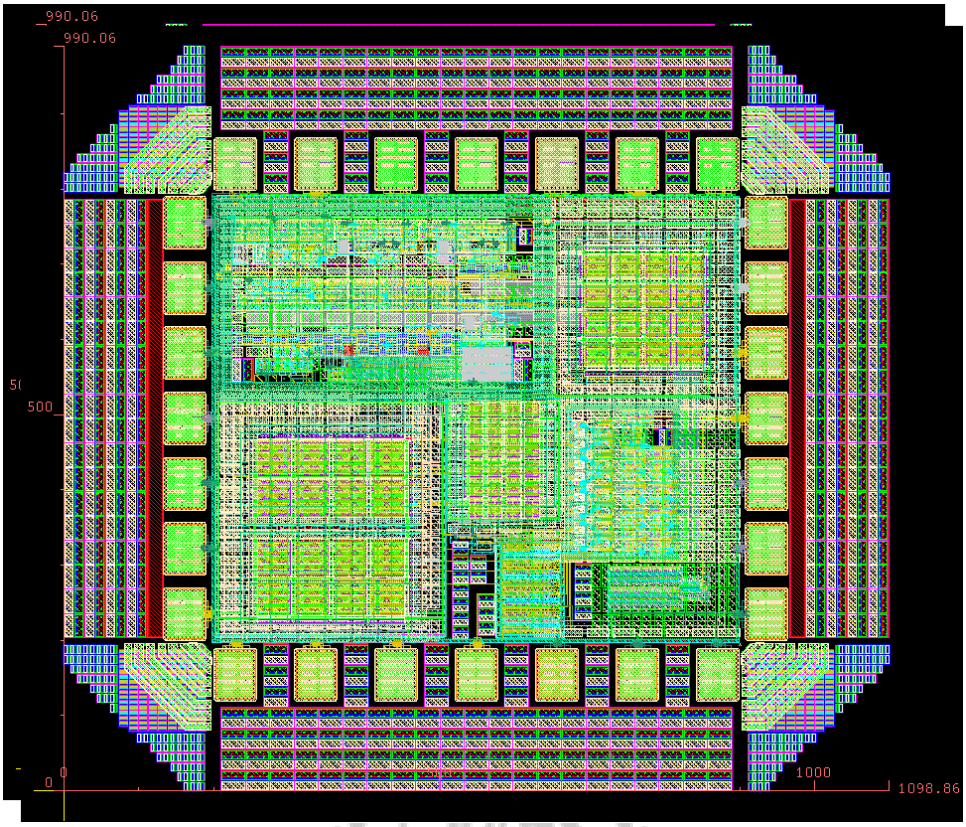


Fig. 5.24 Chip photo of this work

Table 5.3 Summary of circuit level simulation results

Specification	***Simulation Results***
Technology	TSMC 0.13μm 1P8M
Signal bandwidth	2 MHz
Sampling frequency	62.5 MHz
SNDR	63 dB
SFDR	76 dB
ENOB	10
Power Supply	1.2 V
Power Dissipation	10 mW
Chip area (with pad)	1.1 mm x 0.9 mm

Chapter 6

Test Setup and Experimental Results

These two works have been fabricated by TSMC 0.18 μm CMOS Mixed-Signal process and TSMC 0.13 μm CMOS Mixed-Signal process. In this chapter, we present the testing environment, including the component circuits on the DUT (device under test) board and the instruments. The measured results are presented in this chapter, too.

6.1 A Continuous-Time Delta-Sigma Modulator Using Feedback Resistors

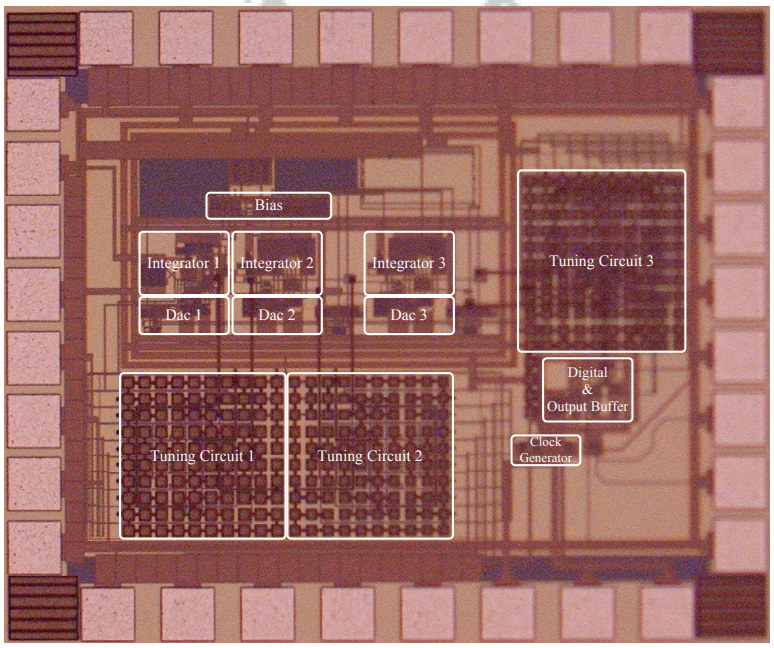


Fig. 6.1 Die photo of this work using feedback resistors

Fig. 6.1 shows the die photo of first work using feedback resistors, in which some important blocks are annotated. Several commonly used layout techniques were employed, such as common-centroid layout for all fully differential input pairs, inter-digitation for current sources, guard ring and shielding. Between the analog and digital areas, a deep n-well was inserted to further reduce the noise coupling.

6.1.1 Test Setup

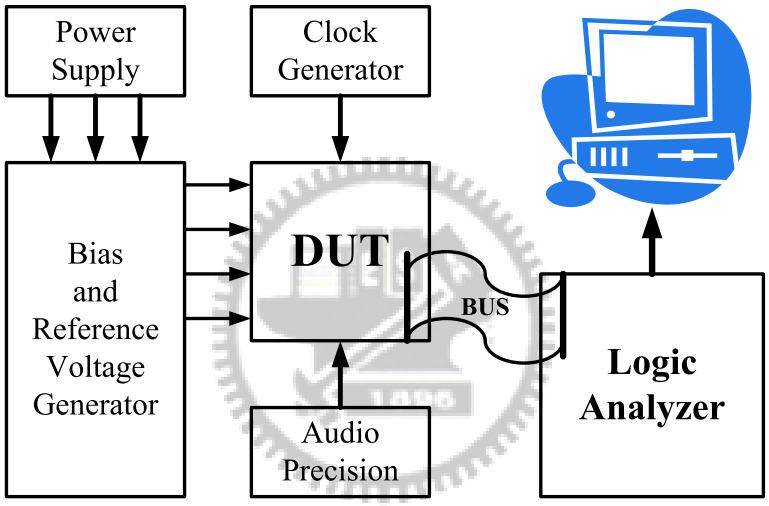


Fig. 6.2 Test environment

Fig. 6.2 presents the configuration of the instruments used to evaluate the performance of the chips. The testing printed circuit board (PCB) contains voltage regulator, single to differential transformer circuit for input signals and clock, tuning resistors, tuning switches, and the DUT, as shown in Fig. 6.3. The differential sinusoidal input signals are produced by the audio precision. The clock generator is used to provide low jitter clock signal for the modulator. The modulator digital outputs are captured by the logic analyzer. The FFT analysis of the output data are performed in MATLAB using a PC connected to the logic analyzer.

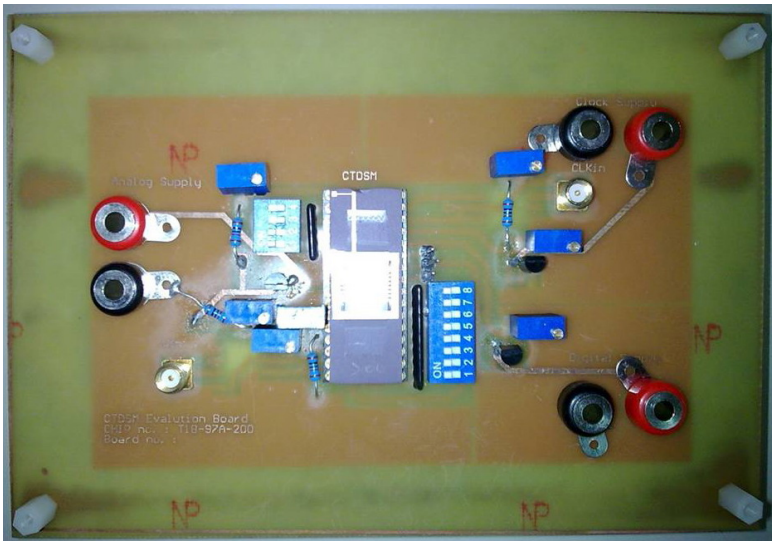


Fig. 6.3 Photograph of the first test board

6.1.2 Measurement Results

The chips have been tested with a 798 KHz input signal and 100 MHz sampling rate. Fig. 6.4 shows the relationship between the post-simulation and the measured. The achieved peak SNDR is 59.6 dB and the dynamic range (DR) is 60dB, as plots in Fig. 6.5. The complete measured results of this work using feedback resistors are summarized in Table 6.1.

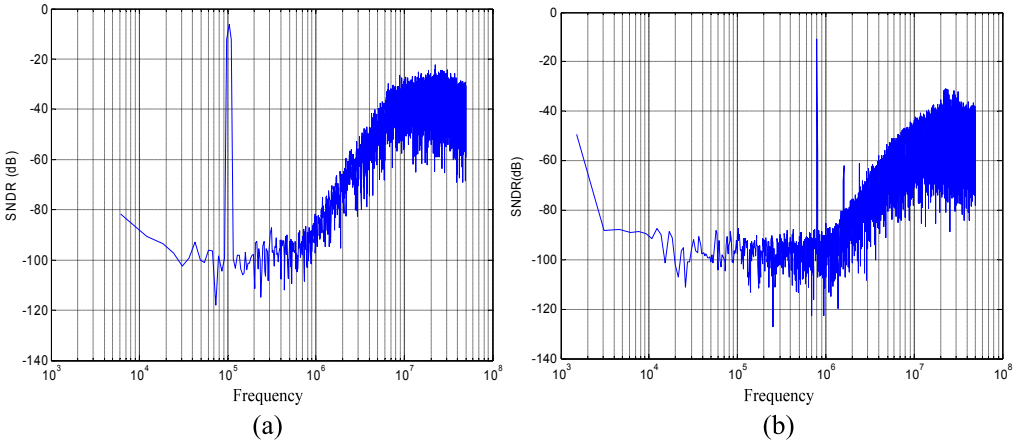


Fig. 6.4 Output spectrum of this work (a) post-simulation (b) measured

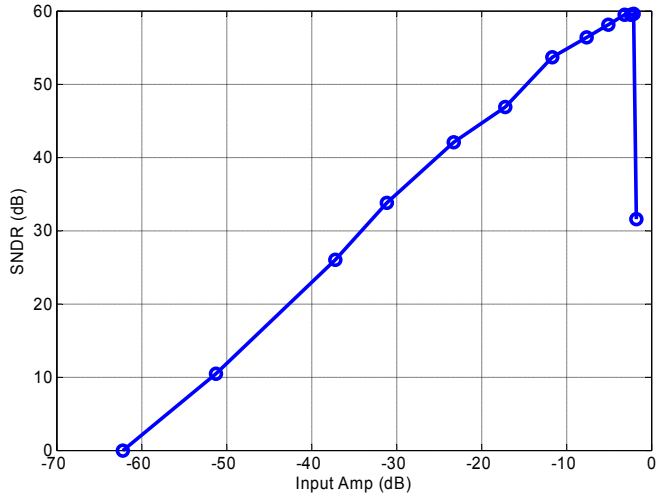


Fig. 6.5 Dynamic ranges of this work using feedback resistors

Table 6.1 Summary of measured results

Specification	***Measured Results***
Technology	TSMC 0.18μm 1P6M
Signal bandwidth	1 MHz
Sampling frequency	100 MHz
SNDR	59.6 dB
ENOB	9.6
Dynamic Range	60 dB
Power Supply	1.8 V
Chip area (with pad)	1.14 mm x 0.945 mm
Power Dissipation	13.7 mW

6.1.3 Comparison between this work and reported designs

To quantitatively evaluate the efficiency among power dissipation, signal bandwidth, and SNDR. We use the formulas for the effective number of bits (ENOB) and the figure-of-merit (FOM) as described below,

$$ENOB = \frac{SNDR - 1.76}{6.02}$$

$$FOM = \frac{Power}{2 \times BW \times 2^{ENOB}} \quad (6.1)$$

and smaller FOM is better.

Table 6.3 lists previously reported SC delta-sigma modulators about 1 MHz signal bandwidth. Compared with them, the SNDR is not the best, but FOM is top. Therefore, we can find continuous-time delta-sigma get growing apply to wireless applications for their lower power consumption and wider bandwidths as compared with the discrete-time counterparts.

Table 6.2 Performance comparison between reported designs and this work

Refs	1999 JSSC [20]	2000 JSSC [21]	2002 JSSC [22]	This work simulation	This work measured
SNDR	82 dB	79 dB	74 dB	67 dB	60 dB
Signal Bandwidth	1.1 MHz	1.1 MHz	2 MHz	1 MHz	1 MHz
OSR	24	24	24	50	50
Architecture	MASH 2-1-1	MASH 2-2-2	4^{th}-order	3^{rd}-order	3^{rd}-order
Process	0.5-μm CMOS	0.35-μm CMOS	0.25-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Power Supply	3.3 V	3.3 V	2.5 V	1.8 V	1.8 V
Die Size	5.06 mm^2	4.3 mm^2	2.6 mm^2	1.08 mm^2	1.08 mm^2
Power Dissipation	200 mW	248 mW	105 mW	13.6 mW	13.7 mW
FOM (pJ/conv)	8.84	15.48	6.4	3.717	8.4

6.2 A Continuous-Time DSM with Improved Zero-Order Loop Compensation and Semi-Uniform Quantization

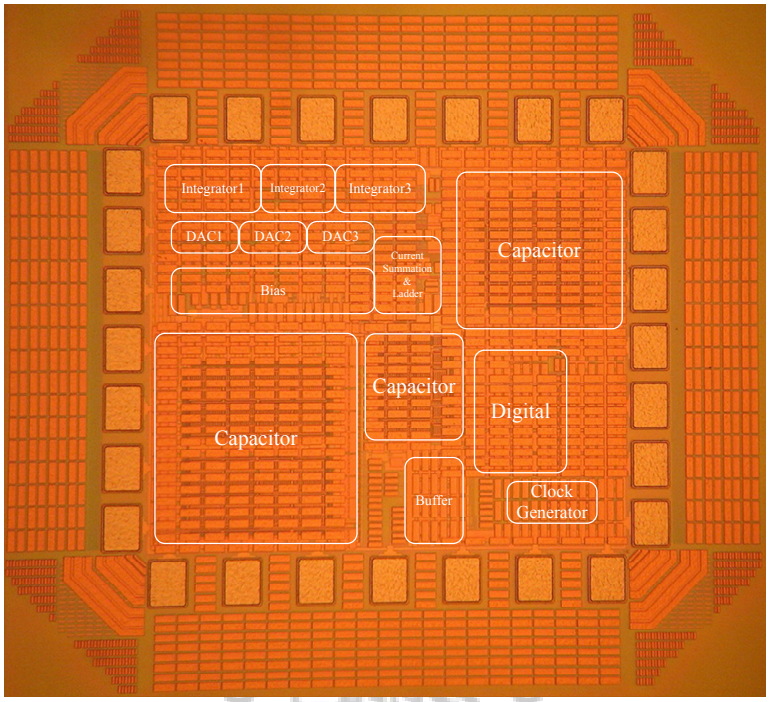


Fig. 6.6 Die photo of this work we propose

Fig. 6.6 shows the die photo of second work we propose, in which some important blocks are annotated. Several commonly used layout techniques were still employed, such as common-centroid layout for all fully differential input pairs, inter-digitation for current sources, guard ring and shielding. Between the analog and digital areas, a deep n-well was inserted to further reduce the noise coupling.

6.2.1 Test Setup

The configuration of the instruments used to evaluate the performance of the chips is present in Fig. 6.2. The testing printed circuit board (PCB) contains voltage regulator, single to differential transformer circuit for input signals and clock, tuning resistors and the DUT, as shown in Fig. 6.7. The differential sinusoidal input signals

are produced by the audio precision. The clock generator is used to provide low jitter clock signal for the modulator. The modulator digital outputs are captured by the logic analyzer. The FFT analysis of the output data are performed in MATLAB using a PC connected to the logic analyzer.

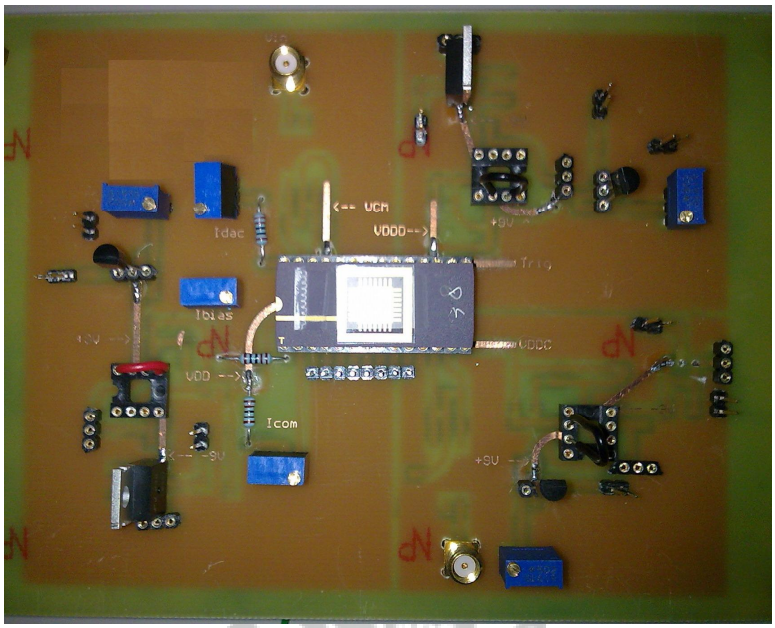


Fig. 6.7 Photograph of the second test board

6.2.2 Measurement Results

Fig. 6.8 shows the output spectrum of second work, we find it be not function work. There are two possible reasons. First, the resistor value shift in the current summation ladder, it makes the wrong compare value, and causes the dac values error to do wrong function. Second, the RC time constant variation is too large to under control. Taking the first reason into account, the system level simulation show that if there is a gain before the quantizer, it will change the transfer function and cause the system unstable, as shown in Fig. 6.9.

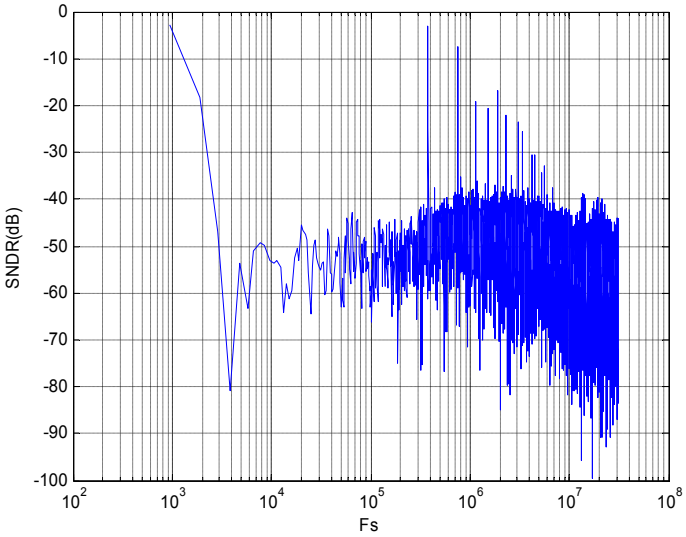


Fig. 6.8 Output spectrum of this work

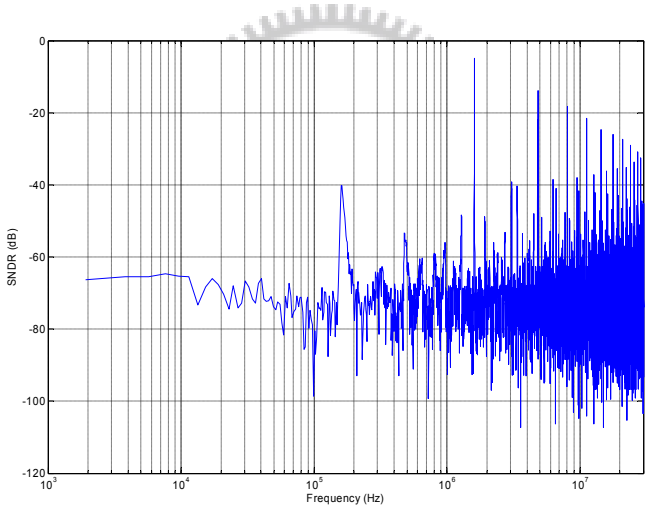


Fig. 6.9 Unstable system level simulation

Chapter 7

Conclusions

7.1 Conclusions

In this thesis, we show two works. A continuous time ΔΣ modulator using feedback resistors is first presented. This work is designed using 180nm CMOS technology in 1.8 V power supply voltage. With a 100 MHz clock, this modulator achieves 59.6 dB SNDR and 60 dB dynamic ranges with a 1MHz signal bandwidth. A technique of using feedback resistors is realized, the low jitter clock generator have the CT ΔΣ modulator not be sensitive to clock jitter, and tuning circuits are employed to calibrate the time constant shift due to process variations.

After that, a continuous time ΔΣ modulator using improved zero order loop with semi-uniform quantization is described. The effect of out-of-band gain is discussed. This work is designed using 130nm CMOS technology in 1.2 V power supply voltage. With a 62.5 MHz clock, this modulator achieves 63 dB SNDR with a 2MHz signal bandwidth. Highlights of the proposed architecture include: (1) high frequency quantization noise gain for low input dynamic range (2) improved zero order loop with NRZ feedback DAC (3) the technique of semi-uniform quantization for low input voltage (4) simple dynamic element matching for linearity improved.

7.2 Future Works

To improve the two works, several design issues can be further explored in the future.

- Some other loop filter topologies may have less coefficient sensitivity so that they are more resistant to time constant variations. Otherwise, tuning circuits should be added to calibrate the time constant variation. Furthermore, automatic on-chip tuning circuits are better choice.
- For wide band applications, the signal bandwidth is more than 10MHz. Therefore, the clock frequencies will be as large as a few hundreds MHz. Hence the clock jitter issue becomes more critical. Other non-rectangular DAC shapes, such as an exponentially decaying DAC, might be worth exploring to reduce further clock jitter sensitivity.
- Some different methods of addressing excess loop delay may be found to achieve the same goal without introducing one more DAC path.
- Various design strategies can be adopted in the future to lower the power consumption.

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