國 立 交 通 大 學

電信工程學系

碩 士 論 文

針對溫度及電壓變異所做之 Logical Effort Model

之延伸

Logical Effort Model Extension with Temperature and Voltage Variations

研究生：吳春慧

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中　華　民　國　九　十　七　年　九　月

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摘要

在積體電路設計中，電路效能的估計與電路最佳化設計是兩個最需要被重視的課題。”Logical Effort Delay Model”是一個可讓電路設計者以簡便的手算方式快速估計電路延遲並完成初步電路最佳化的方法。但是在已發表的各項關於logical effort model的改進或延伸的研究中，並沒有提出一個可適當處理製程、電壓或溫度變異的方法，而這些變異卻可能造成嚴重的錯誤估計。根據在 90 奈米製程下所得到的模擬結果，電路的延遲時間在溫度由 0°C升高到 125°C時會增加 21%，而當供應電壓由 1V降到 0.5V時則會提高到原先的兩倍。因此，本論文對原始的 logical effort *g*提出一個簡單的線性方式的延伸：$1/g = (m_t t+b_t)V_{DD}+C$，使其能適用於溫度*t*及供應電壓$V_{DD}$的變異，並利用其線性特性使設計者能便於計算，在CAD tool上的應用也較易於整合。本論文中所提出的logical effort model extension可讓電路設計者能在不同的溫度及電壓條件下，正確的估計整體電路的效能並完成電路最佳化設計。更進一步來說，在一個晶片中的各個區塊都可依其不同的溫度及電壓條件，各自完成最佳化的設計，此優點能使整體電路的效能得到更好的提升。經過驗證後可確認本論文所提出的延伸模型能達到大約 90%的準確率。

Logical Effort Model Extension with Temperature and Voltage Variations

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Abstract

In the integrated circuits design, performance estimation and circuit optimization are two of the most important issues. The method of "Logical Effort Delay Model" allows designers to quickly estimate delay time and optimize logic paths, but the previous variances of logical effort models do not mention how to handle process, voltage, and temperature (PVT) variations appropriately, which may induce a serious misestimate. According to simulation results in 90nm process, delay time increases 21% while temperature increasing from 0°C to 125°C. In the mean time, delay time increases 2X while supply voltage decreasing from 1V to 0.5V. Thus a simple linear extension of logical effort g, $1/g = (m_t t+b_t)V_{DD}+C$, supporting for temperature t and supply voltage V_{DD} variations is presented. The linear characteristic is convenient for designers to calculate and the integration of proposed model and CAD tools is easier. The proposed model enables designers to estimate the logic path delay and to optimize an N-stage logic network under different temperature and supply voltage conditions. Furthermore, each functional block on a chip can be optimized under different PVT conditions through this simple model. After validation, the accuracy of this new extended logical effort model can achieve about 90%.

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吳春慧

中華民國九十七年九月於新竹

Content

List of Tables

List of Figures

Chapter 1
Introduction

1.1 Motivation

In the 1960s, Gordon Moore predicted that the number of transistors on an integrated circuit would grow exponentially with time [1]. This prediction is called "Moore's Law" and the law quite realistically represents the fast improvement of this industry. Owing to many researchers who work hard in this field, the technique of circuits design is advanced all the time and the law can be maintained for several decades. In the integrated circuits design, good productions are usually constructed with some factors such as high performance, low power, well reliability, and inexpensive to manufacture [2]. In order to fulfill these requirements, a lot of researches, design methodologies, circuit simulation models, and computer-aided design (CAD) tools have been proposed to improve the accuracy of circuit estimation, decrease design cycle time, and reduce entire cost of the productions.

The delay of switching signals propagation through the logic gates is the primary performance measure of digital logic [3]. In the procedure of designing circuits, timing constraint is one of the most important issues and should be noticed at each step of the design flow. An accurate circuit delay model can help designers to handle the arrangement of transistors or logic gates more confidently. A precise timing analysis can also be used to assist in performance, power, and area optimizations. For

the accuracy, design-oriented delay modeling must be done with complete information on the process evolution, the size, and the structure of the considered cell and its complete environment [4]. Therefore, many researchers have presented several kinds of delay models to perform accurate delay estimation for different situations [3]-[7].

In addition to delay estimation, circuit optimization is also a key point for designers to achieve high performance and increase work efficiency. While designers successfully accomplish circuit optimization, the entire chip performance will be boosted, chip area and power dissipation will be reduced, and the total cost will be decreased massively. In order to improve the quality and competitiveness of the design, a correct estimation and the inspection in all aspects of the circuit are necessary. For above reasons, an appropriate method used to estimate circuit performance and achieve design optimization in all kinds of situations is in demand.

In all kinds of factors effecting circuit performance, process, voltage, and temperature (PVT) variations are important elements which may induce a serious misestimate. For temperature variation, with the increasing clock rate and transistor count of today's microprocessors, thermal issue becomes critical for high-performance computing systems [8]. It is important to model temperature effects on the devices correctly and to predict their scaling [9], [10]. In [11], it has been reported that a temperature variation of 50°C exists on a modern microprocessor chip. Moreover, the functional blocks on a chip will not keep performance coherence at the same target frequency due to temperature difference, and circuit delay will become worse when temperature rising [12]. Figure 1.1 and Figure 1.2 are the thermal maps

of a 115W packaged POWER4 chip and a 90nm Cell/B.E. processor [13], [14]. According to these two figures, the temperature gradient on a chip is demonstrated.

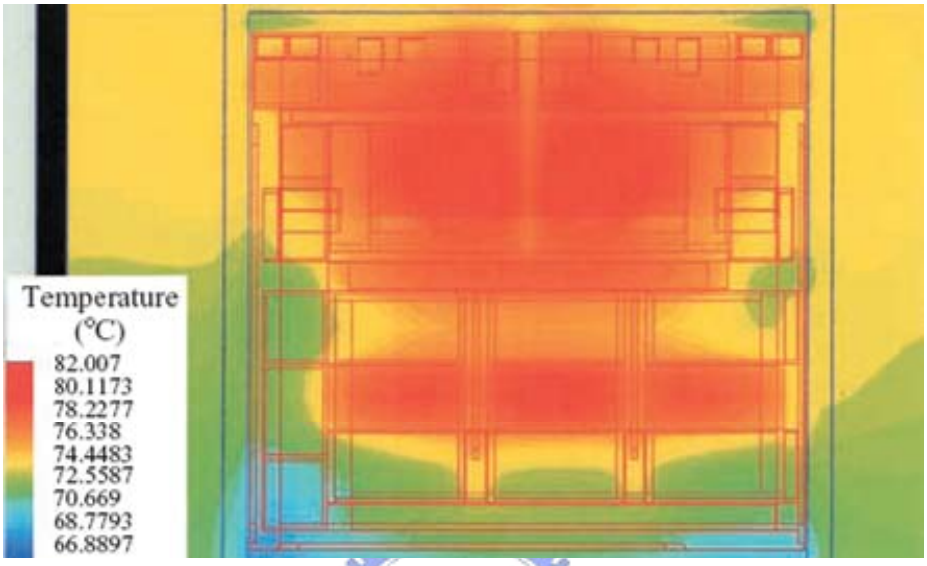


Figure 1.1 The thermal map of a 115W packaged POWER4 chip [13].

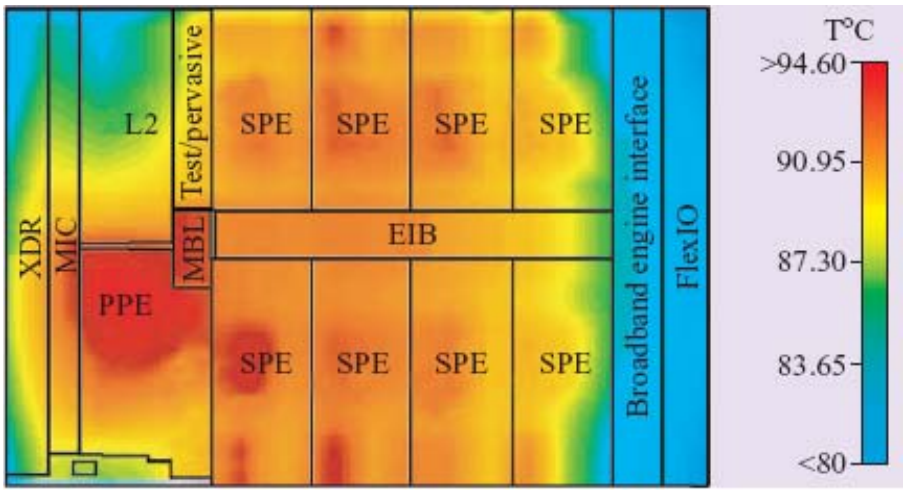


Figure 1.2 Die thermal map of the 90nm Cell/B.E. processor [14].

While an integrated circuit is operating, the power dissipation will increase with circuit frequency, and thus the chip temperature increases as well [15]. As shown in Figure 1.3, delay time increases 21% while temperature increasing from 0°C to 125°C in 90nm process. Besides temperature variation, supply voltage fluctuation is another cause of incorrect circuit estimation. As shown in Figure 1.4, delay time increases 2X while supply voltage decreasing from 1V to 0.5V in 90nm process. This effect due to the change of supply voltage can also be discussed with dynamic voltage scaling (DVS), which is a low-power technique [16]-[19].

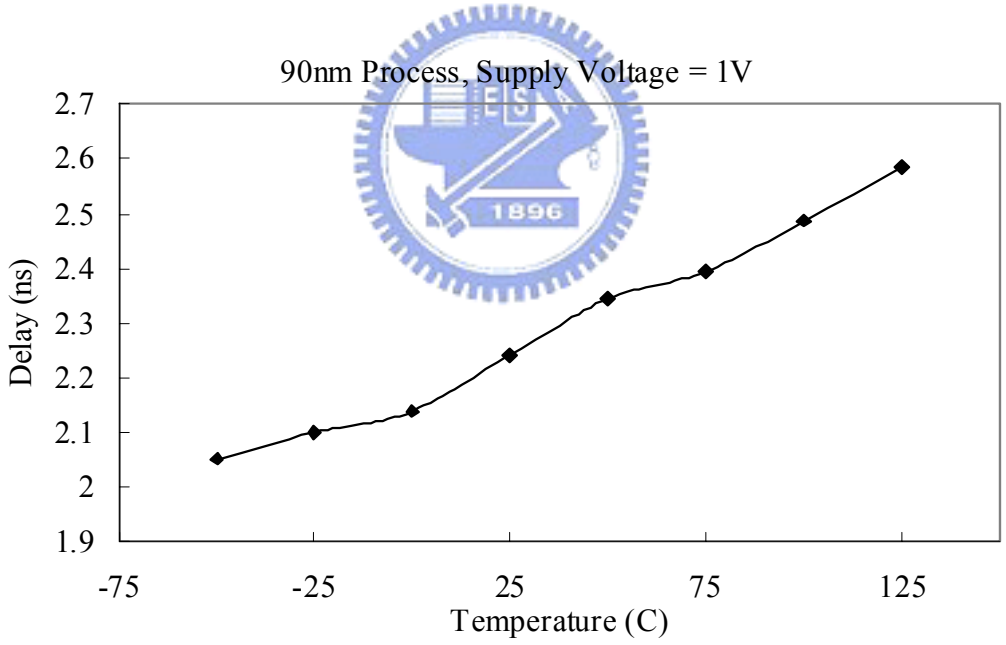


Figure 1.3 Delay time of 101 stages ring oscillator with different temperatures.

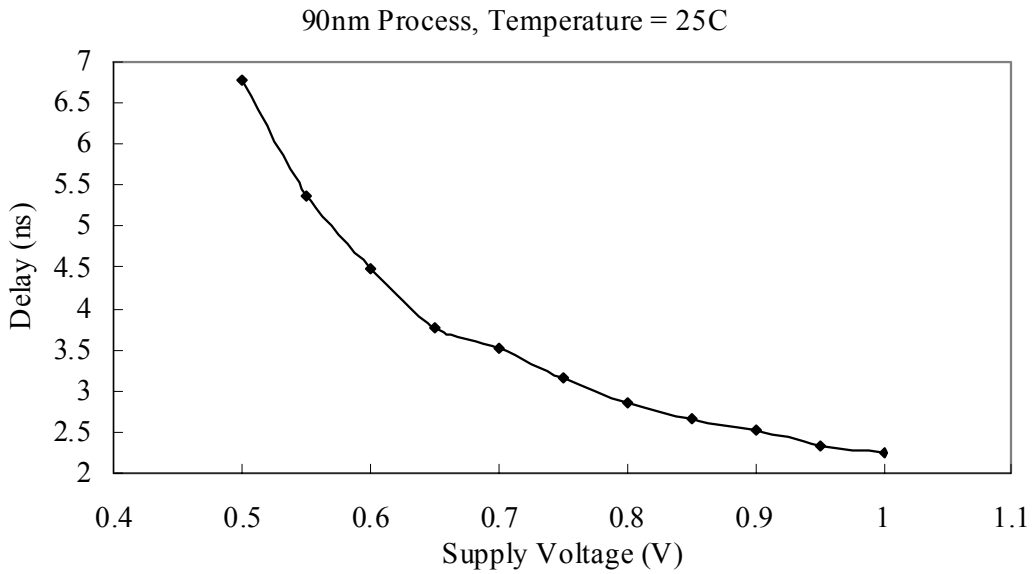


Figure 1.4 Delay time of 101 stages ring oscillator with different supply voltages.

Because the influence of these variations on chip performance can not be ignored, the possible solution to reduce the impact should be presented. Therefore, we hope to propose a simple delay model and take temperature and supply voltage into account. Furthermore, each functional block on a chip can be optimized under different PVT conditions through this simple model. In this thesis, we are concerned about the accuracy of estimating circuit delay when temperature and supply voltage variations are happening. To propose a simple model to estimate and optimize circuit delay easily and correctly, the method of "Logical Effort Delay Model" will be used to develop an extended model which can support for temperature and supply voltage variations. Moreover, we can reveal the difference between calculated results of the proposed extended model and hardware experimental results in the future. We can also improve our research by these comparisons and increase the reliability of the proposed model.

1.2 Organization

In Chapter 2, an overview of the method of logical effort is introduced. In the beginning of this chapter, the traditional circuit delay models are presented and the concepts of these models are interpreted, too. After that, the theory and the derivation of logical effort are defined and clarified. In the end of this chapter, several design examples with the method of logical effort are demonstrated and the related researches of logical effort are discussed.

In Chapter 3, the effects of temperature and supply voltage variations are revealed first. We focus on how these two factors influence the parameters of the delay model. According to these phenomena, a new extension based on logical effort model is proposed and the consideration to temperature and supply voltage variations is included. Finally, a simulation and analysis flow is established and the validation of the proposed model is shown.

In Chapter 4, we provide some application scenarios of the proposed extended model in different situations and under distinct temperature and supply voltage conditions. These examples can help designers to understand how to perform circuit estimation and optimization by the proposed model. Also, the circuit design flow with proposed extended logical effort model is presented in this chapter. How to utilize the proposed model with the thermal simulator in the circuit design flow is described clearly through the flowchart.

In Chapter 5, the conclusion of our research in this thesis and the future works for the improvement are presented.

Chapter 2

Overview of Logical Effort

2.1 RC Delay Model

As we introduced in Chapter 1, an accurate timing analysis can help designers to handle the arrangement of transistors or logic gates more confidently and can be used to assist in performance, power, and area optimizations. The RC delay model provides a useful method to estimate the delay of a gate without complex or time-consuming circuit simulation. It is commonly used in digital integrated circuits to model long wires, transmission gates, and pass transistor chains [20].

The RC delay model treats transistors as switches in series with resistors. Figure 2.1 shows equivalent RC circuit models for NMOS and PMOS transistors. Although the transistor has complex nonlinear current-voltage characteristics practically, it can be approximated to the average current delivered by the transistor. The capacitances in Figure 2.1 represent gate and diffusion capacitances, and the scales of the resistance and the capacitance depend on the size of the transistor. If the transistor has fixed length, it will have smaller resistance and bigger capacitance when the transistor has bigger width. Based on the simple equivalent RC delay model, the propagation delay of the logic gate can be estimated.

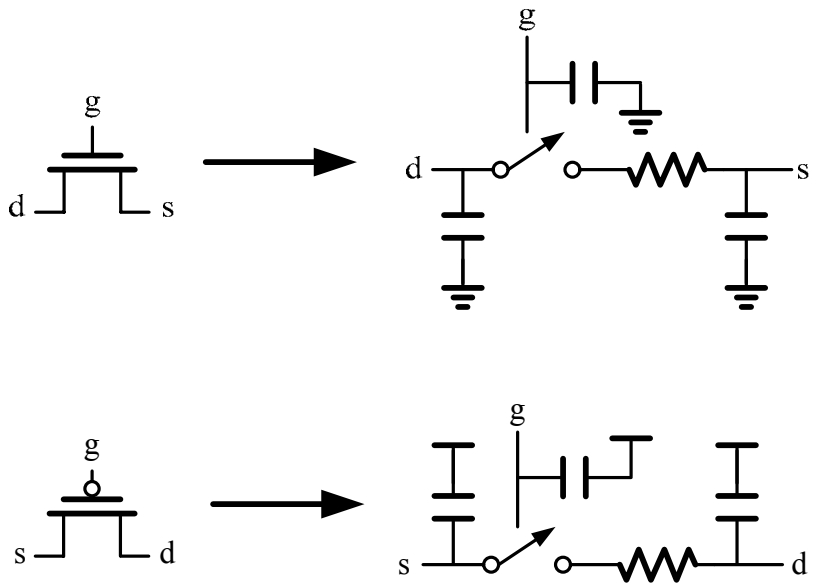


Figure 2.1 Equivalent RC circuit models [2].

Figure 2.2 shows a conceptual model of a CMOS logic gate. As shown in the figure, a CMOS logic gate consists of the PMOS pull-up network and the NMOS pull-down network. Parallel and series transistors in each network can be combined like conventional resistors, the gate capacitance and the diffusion capacitance construct input capacitance and the parasitic capacitance, and the load capacitance is usually the input capacitance of the next CMOS logic gate. In this figure, R_{up} and R_{down} represent the pull-up and pull-down resistance, C_{in}, C_p, and C_{out} are the input, parasitic, and load capacitance.

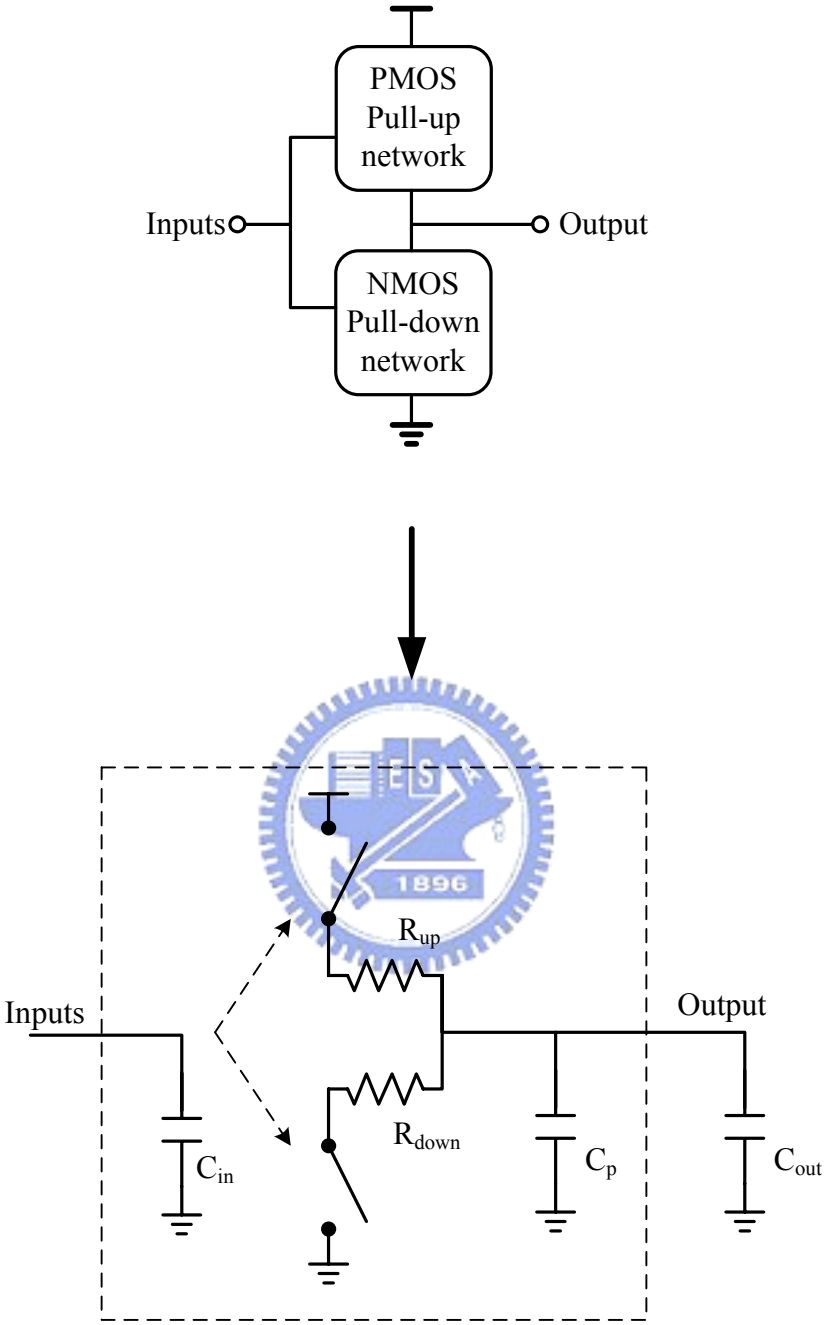


Figure 2.2 Conceptual model of a CMOS logic gate.

According to the logic levels at the inputs, the output of the CMOS logic gate is driven "high" or "low" when C_p and C_{out} are charged by R_{up} or discharged by R_{down}. Based on this conception, the propagation delay of the logic gate can be estimated as the RC product of the effective resistance and the parasitic and load capacitances. Since the delay of the CMOS logic gate can be estimated through simple RC delay model, the delay of a logic path can also be obtained by summing up the delay of each stage. Furthermore, the basic performance estimation of the integrated circuits can be accomplished.

2.2 Logical Effort Model

In a complete circuit design, there will be some critical paths needing most attention of designers to ensure that whole circuit can meet the performance requirement. Moreover, quick delay estimation is necessary for designing these critical paths. The method of "Logical Effort Delay Model" allows designers to quickly estimate and optimize single paths by modeling equivalently delay time. Through this simple hand-calculated method, designers can do timing evaluation with less effort and the design cycle time can be reduced efficiently.

In 1999, Sutherland, Sproull, and Harris wrote a book to introduce the theory of logical effort delay model [21]. The method of logical effort is founded on a simple model of the delay through a single CMOS logic gate. The conception is derived from the RC delay model as shown in Figure 2.3.

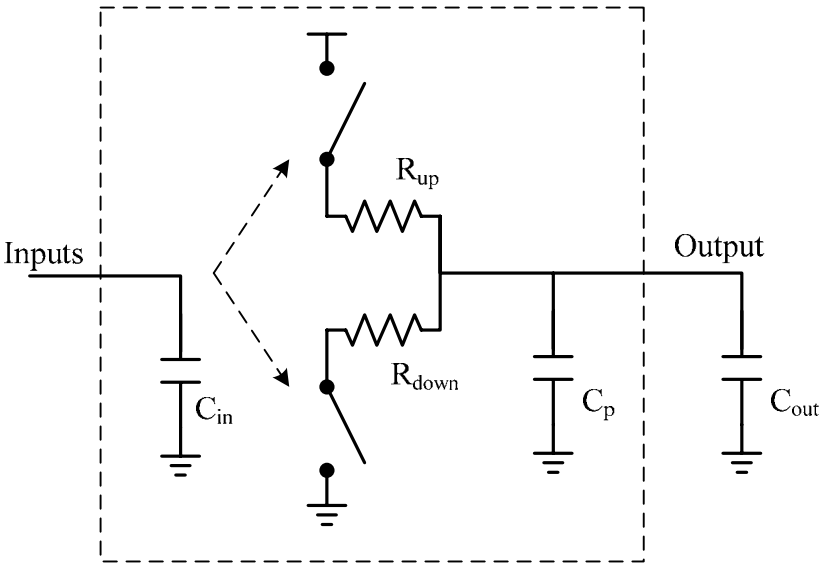


Figure 2.3 An illustration of the RC delay model of a CMOS logic gate.

Based on RC delay model, the delay of the logic gate can be expressed as

$$\begin{aligned} d_{abs} &= \kappa R\left(C_{out}+C_p\right) \\ &= \kappa R\left[C_{in}\left(\frac{C_{out}}{C_{in}}\right)+C_p\right] \\ &= \kappa\left(\frac{R_t}{\alpha}\right)\left[\alpha C_{\text{int}}\left(\frac{C_{out}}{C_{in}}\right)+\alpha C_{pt}\right] \\ &= \kappa R_t C_{int}\left(\frac{C_{out}}{C_{in}}\right)+\kappa R_t C_{pt} \end{aligned} \tag{2.1}$$

where d_{abs} is the absolute delay, κ is a constant, R is the pull-up or pull-down resistance, C_{in}, C_{out} and C_p are the input, load and parasitic capacitances, R_t, C_{int} and C_{pt} are the resistance, input capacitance and parasitic capacitance of different logic gate templates, and α is a scale factor [21]. In the final form of the derivation, the

scale factor α is hidden in C_{in}. It means that all values of R_t, C_{int}, and C_{pt} are unrelated to the size of the logic gate, they only depend on what kind of logic gate it is, and only the values of C_{in} and C_{out} depend on the size of the logic gate.

According to the final form of above equation, the delay equation of logical effort delay model can be defined as

$$d_{abs} = \kappa R_t C_{int}\left(\frac{C_{out}}{C_{in}}\right) + \kappa R_t C_{pt} = \kappa\left[R_t C_{int}\left(\frac{C_{out}}{C_{in}}\right) + R_t C_{pt}\right] = \tau\left(gh + p\right) \qquad (2.2)$$

where τ is the basic delay unit, g, h, and p are the logical effort, electrical effort or fanout, and parasitic delay.

From equation (2.2), the definitions of these parameters are

$$\tau = \kappa R_{inv} C_{inv},\ g = \frac{R_t C_{int}}{R_{inv} C_{inv}},\ h = \frac{C_{out}}{C_{in}},\ \text{and}\ p = \frac{R_t C_{pt}}{R_{inv} C_{inv}} \qquad (2.3)$$

where R_{inv} and C_{inv} are resistance and input capacitance of an inverter template. Also, the values of τ, g, and p only depend on the topology of the logic gate, not the size of the logic gate; only the value of h depends on the ratio of size between loading and the characterized logic gate.

For a clearer interpretation, Table 2.1 shows the values of g of different gate types, assuming the ratio of PMOS transistor width to NMOS transistor width in the inverter is 2.

Table 2.1 Logical effort *g* of common gates.

Gate Type	Number of Inputs				
	1	**2**	**3**	**4**	**n**
Inverter	1				
NAND		4/3	5/3	6/3	(n+2)/3
NOR		5/3	7/3	9/3	(2n+1)/3
Multiplexer		2	2	2	2

In addition to estimate the delay, logical effort is also used to optimize an *N*-stage logic path. Here we will introduce some factors first.

- Stage effort: $f=gh$.
- Path logical effort: $G = \prod g_i$.
- Path branching effort: $B = \prod b_i$.
- Path electrical effort: $H = \frac{C_{out}}{C_{in}}$.
- Path effort: $F = GBH$.
- Path effort delay: $D_F = \sum f_i$.
- Path parasitic delay : $P = \sum p_i$.
- Path delay: $D = \sum d_i = D_F + P$.

Because the sum of a set of numbers is minimized by choosing all the numbers to be equal, the path delay is minimized when each stage bears the same stage effort

$$\hat{f} = g_i h_i = F^{1/N}. \tag{2.4}$$

According to equation (2.4), the minimum path delay will be performed when the input capacitance of each gate are

$$C_{in_i} = \frac{g_i C_{out_i}}{\hat{f}}. \tag{2.5}$$

Based on above simple equations, designers can easily manage the logic paths arrangement and obtain the optimized path delay. Actually, evaluating the exact delay of the logic paths is not the most worthful use of this model because there are many powerful CAD tools can do more precise timing verification. But this simple hand-calculated model is accurate enough to do basic performance prediction in a short time. Furthermore, using this simple model to derive the best logic gate arrangement for minimum path delay is the primary contribution indeed.

2.3 Design Example

There are two key purposes of logical effort model:

1. Estimate the delay of logic paths simply and quickly.
2. Find out the best arrangement of logic paths for minimum delay.

The following is an example for how to use logical effort model.

Example:

Figure 2.4 shows an example logic path to explain how to use logical effort model. The initial NOR2 gate presents a load of 5λ of transistor width on the input

and the output load is equivalent to 225λ of transistor width. How to estimate the minimum delay of the path from A to B and how to choose transistor sizes to achieve this delay?

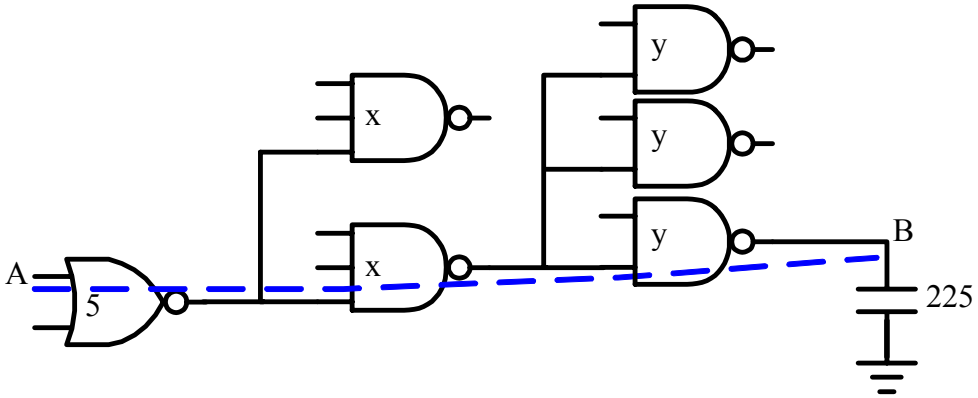


Figure 2.4 An example logic path.

Solution:

The number of stages $N = 3$, and path branching effort $B = 2\times3 = 6$.

$g_{nor2} = 5/3$, $g_{nand3} = 5/3$, and $g_{nand2} = 4/3$.

→ Path logical effort $G = (5/3)\times(5/3)\times(4/3) = 100/27$.

Path electrical effort $H = (2x/5)\times(3y/2x)\times(225/3y) = 225/5 = 45$.

→ Path effort $F = G\times B\times H = 1000$.

The delay of a gate $d = f+p$.

The path delay is minimum when each stage has the same stage effort

→ $\hat{f} = \sqrt[N]{F} = \sqrt[3]{1000} = 10$.

$p_{nor2} = 2$, $p_{nand3} = 3$, and $p_{nand2} = 2$.

→ Path parasitic delay $P = 2+3+2 = 7$.

The minimum path delay $D = N\times\hat{f} + P = 3\times10 + 7 = 37$ in unit of τ.

Decide the transistor sizes:

$\hat{f} = g \times h = g \times (C_{out} / C_{in}) \rightarrow C_{in} = (g \times C_{out}) / \hat{f}$.

→ $y = [(4/3) \times 225]/10 = 30$, and $x = [(5/3) \times (30 \times 3)]/10 = 15$.

If $\mu_p : \mu_n = 1:2$

→ *Wp:Wn* in NAND2 gate is *15:15*.

→ *Wp:Wn* in NAND3 gate is *6:9*.

Figure 2.5 shows the recommended solution of this example through logical effort delay model.

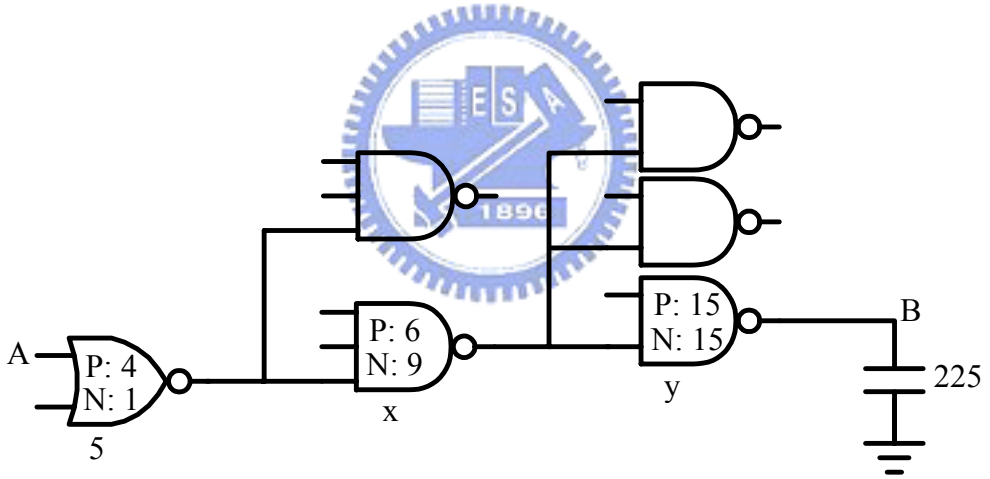


Figure 2.5 The recommended solution of the example.

2.4 Related Research

Because of the simplicity and clarity of logical effort model, many studies have been presented to improve the accuracy of logical effort model to adapt to different design conditions. The effects of a linear input transition time and wiring RC delay is introduced in [22] and the simulated value of g and p in 0.18um process also been shown. A modified logical effort model, which accounts for the behavior of series connected MOSFET structure, switching input transition time, and internodal charges, is presented in [23]. And reference [24] introduces an extension of the logical effort model that considers the I/O coupling capacitance and the input ramp effect.

Furthermore, logical effort delay model has been used to develop new algorithms for designing circuits and been applied in some CAD tools. Based on logical effort model, reference [25] presented an algorithm which can produce the optimum fanout tree solution if the fanout tree topology is restricted to a chain of buffers. Also, a new algorithm to approach to delay-optimal mapping for solving the load-distribution problem based on the principle of logical effort is presented in [26].

All of the above are some examples of a lot of researches about logical effort model. However, the modified logical effort model been presented before do not mention how to handle temperature and supply voltage variations appropriately. Therefore, we hope to extend the simple logical effort model and take temperature and supply voltage into account. In Chapter 3, how these two factors influence the parameters of logical effort model will be discussed. According to these phenomena, a new extension based on logical effort model will be proposed subsequently.

Chapter 3

Logical Effort Model Extension

3.1 Effects of Temperature and Supply Voltage Variations

In Chapter 2, it has been shown that logical effort delay model is expressed as $d_{abs}=\tau(gh+p)$. In this model, τ and h are constant in each process, but g and p will be impacted by temperature and voltage variations since they are functions of effective resistance and capacitance of the logic gate. In order to understand how temperature and supply voltage variations affect the logical effort model, we establish a test circuit as Figure 3.1 to imitate a real logic path [2]. Gate A and B are used to shape the input slope, gate C is the gate being characterized, gate D and E are the load, and h is the fanout.

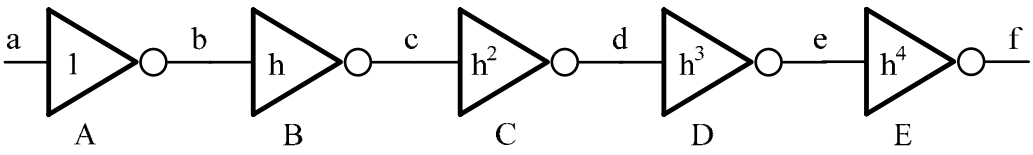


Figure 3.1 Test circuit for calibrating the logical effort model.

Based on the equation $d_{abs}=\tau(gh+p)$, it can be rewritten as (3.1).

$$d_{abs} = \tau(gh + p) = \tau gh + \tau p. \quad (3.1)$$

According to (3.1), we utilize the test circuit, change h from 1 to 8, and then obtain the curve of delay time d_{abs} vs. fanout h as shown in Figure 3.2. In Figure 3.2, the straight line is the linear regression trendline of the curve of d_{abs} vs. h, and the equation $y=mx+b$ is the linear regression equation. Matching Figure 3.2 with (3.1), the slope of the curve is τg, and then we define the value of g is 1 under typical temperature and supply voltage conditions. τ is a constant in each process.

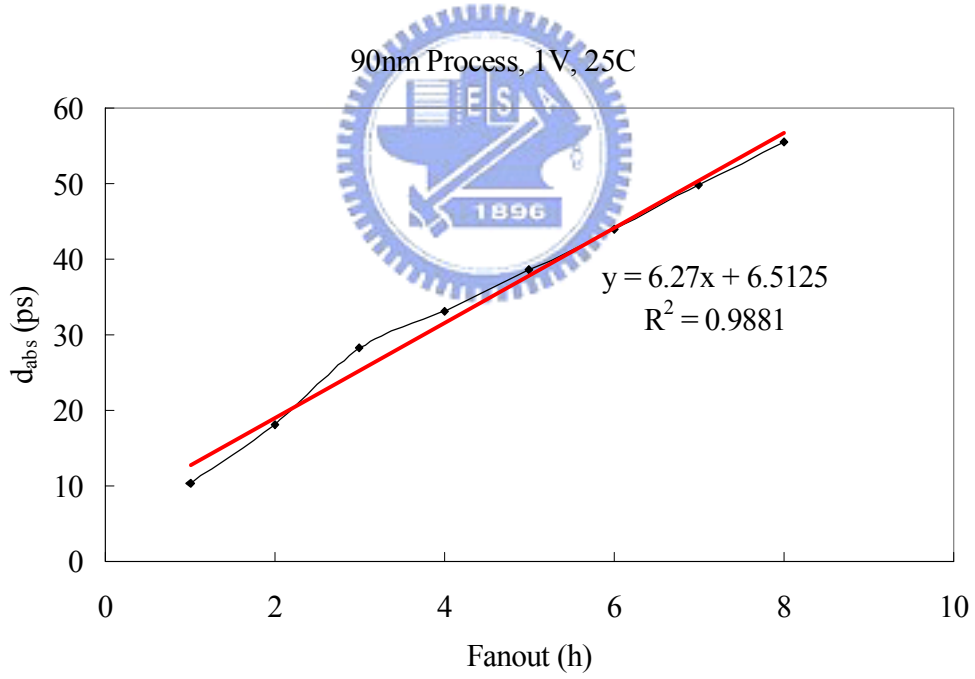


Figure 3.2 The curve of delay vs. fanout and the linear regression trendline.

Under different temperature and supply voltage conditions, we can plot the curves of delay time d_{abs} vs. fanout h as shown in Figure 3.3 and other charts with different values of supply voltage. The slope τg of each curve is different under different conditions and τ is a constant in each process, thus we can obtain distinct values of logical effort g with different temperatures and supply voltages as shown in Table 3.1. According to the definition of g mentioned in Chapter 2, these values describe temperature and supply voltage effects on RC delay of the logic gate practically.

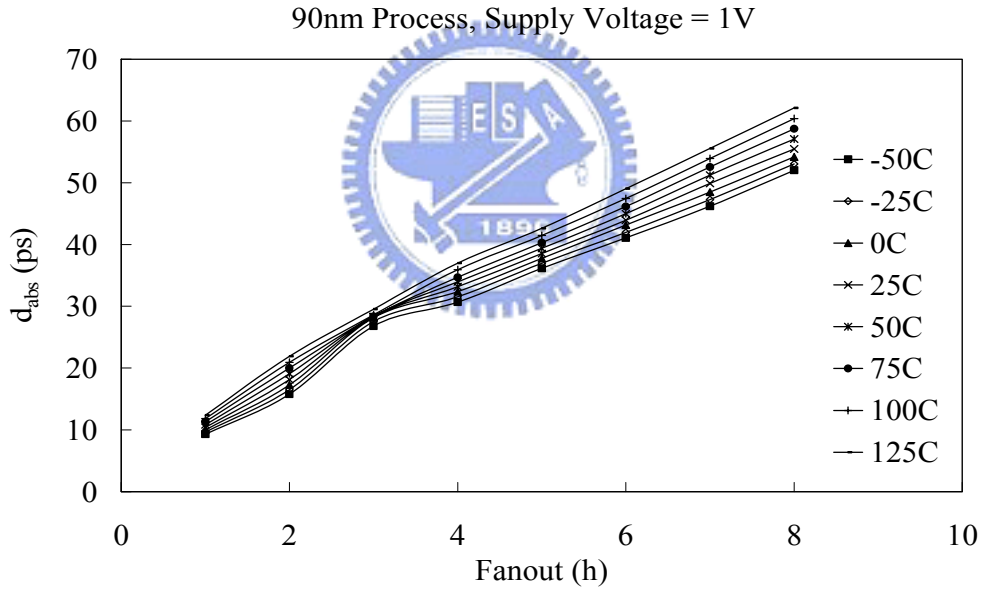
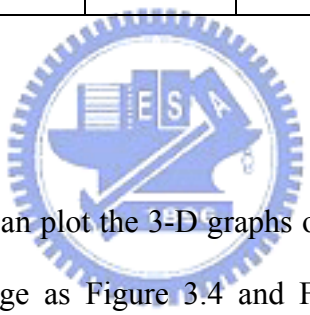


Figure 3.3 Simulated values of delay time with different temperature.

Table 3.1 Simulated values of *g* with different temperatures and supply voltages. (In 90nm Process)

g	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	0.9483	1.0421	1.1428	1.3638	1.7770	2.8651
-25°C	0.9611	1.0571	1.1608	1.3731	1.7701	2.7500
0°C	0.9792	1.0736	1.1799	1.3887	1.7751	2.6747
25°C	1.0000 (Def.)	1.0888	1.2036	1.4096	1.7871	2.6227
50°C	1.0250	1.1053	1.2326	1.4346	1.8039	2.5876
75°C	1.0509	1.1292	1.2688	1.4637	1.8258	2.5632
100°C	1.0764	1.1497	1.3030	1.4958	1.8484	2.5475
125°C	1.1019	1.1750	1.3399	1.5164	1.8724	2.5373



Based on Table 3.1, we can plot the 3-D graphs of the value of *g* and *1/g* versus temperature and supply voltage as Figure 3.4 and Figure 3.5. According to these graphs, we can utilize linear regression to perform curve fitting and derive the new extended logical effort model as a simple linear format from *1/g* because the shape of the surface in Figure 3.5 is flatter.

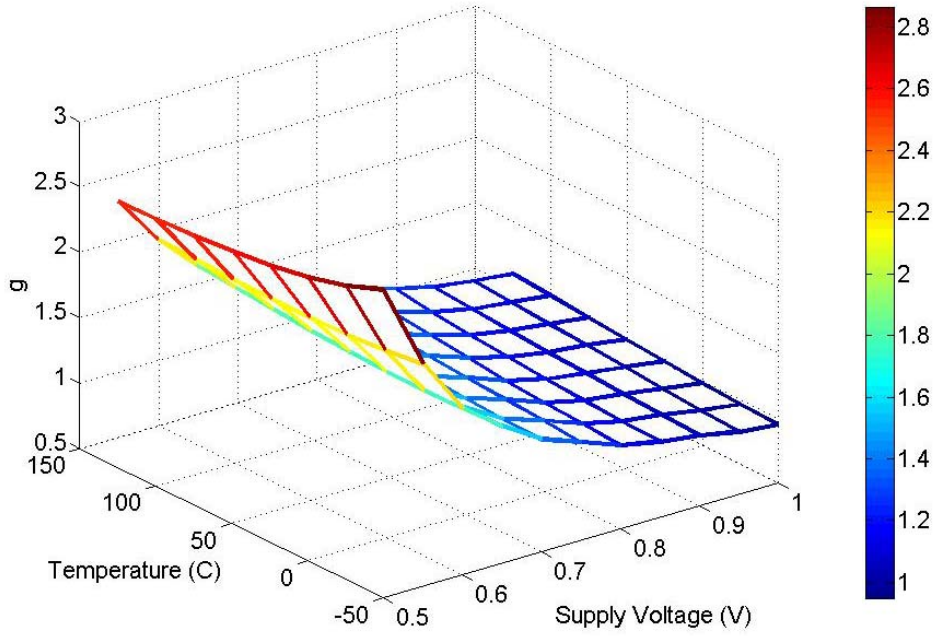


Figure 3.4 The values of *g* with different values of temperature and supply voltage.

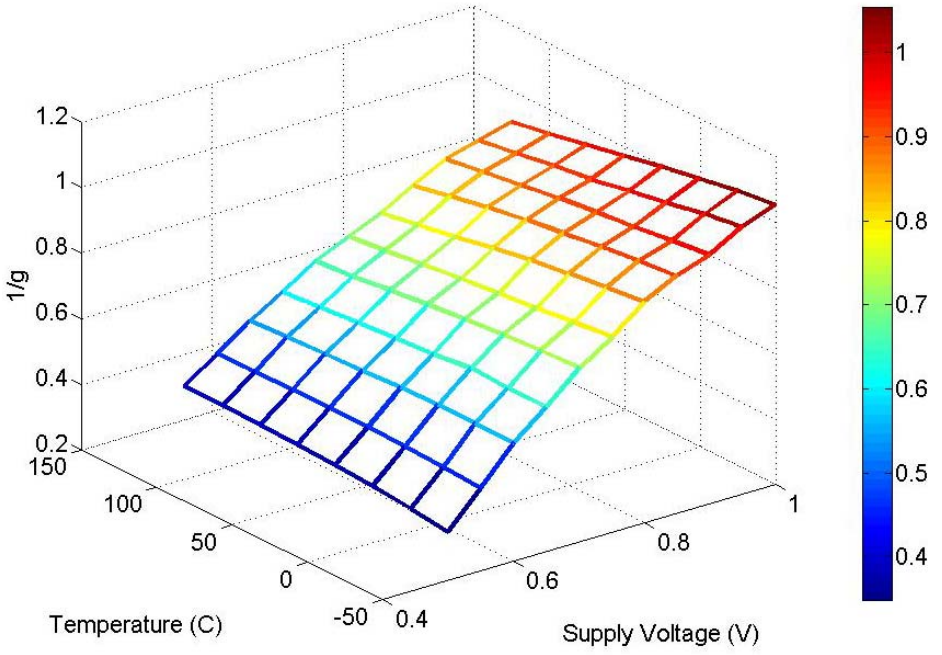


Figure 3.5 The values of *1/g* with different values of temperature and supply voltage.

3.2 Derivation of Extended Logical Effort Model

Based on the definition of g, we rewrite the equation of g as

$$g = \frac{R_t C_{int}}{R_{inv} C_{inv}} = kR_{eff} C_{in} = \frac{kV_{DD} C_{in}}{I_d} \tag{3.2}$$

where R_{eff} and C_{in} are effective resistance and input capacitance of the gate, V_{DD} is the supply voltage, and I_d is the saturation current. As shown in Table 3.2, according to simulation results, k is close to a constant under different temperature and supply voltage conditions.

Table 3.2 Simulated values of k with different temperatures and supply voltages. (In 90nm Process)

k=g*Id/(Vdd*Cin) (10^12)	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	0.1859	0.1845	0.1778	0.1786	0.1826	0.2031
-25°C	0.1850	0.1844	0.1787	0.1791	0.1831	0.2009
0°C	0.1847	0.1840	0.1790	0.1794	0.1834	0.1988
25°C	0.1843	0.1826	0.1791	0.1792	0.1830	0.1963
50°C	0.1840	0.1807	0.1790	0.1785	0.1819	0.1935
75°C	0.1831	0.1793	0.1791	0.1774	0.1804	0.1906
100°C	0.1815	0.1767	0.1781	0.1760	0.1784	0.1877
125°C	0.1793	0.1742	0.1770	0.1729	0.1763	0.1850

3.2.1 Saturation Current I_d

Table 3.3 shows the values of saturation current I_d under different temperature and supply voltage conditions in 90nm process. According to this table, we can observe that the factors of temperature and voltage influence I_d enormously. Thus, I_d is the key factor for deriving the extended logical effort model.

Table 3.3 Simulated values of I_d with different temperatures and supply voltages. (In 90nm Process)

I_d (uA)	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	154.6342	125.8323	98.2861	72.2842	48.3234	27.2964
-25°C	152.0374	124.1019	97.3316	72.0113	48.6453	28.1285
0°C	149.5167	122.3091	96.1961	71.4747	48.6730	28.6917
25°C	146.9099	120.3315	94.8045	70.6507	48.4272	29.0279
50°C	144.1031	118.0980	93.1331	69.5606	47.9594	29.1926
75°C	141.0290	115.5845	91.2000	68.2549	47.3333	29.2411
100°C	137.6620	112.8041	89.0504	66.7967	46.6112	29.2204
125°C	134.0091	109.7944	86.7418	65.2486	45.8458	29.1665

Because of the effect of velocity saturation, the saturation current model is expressed as $I_d=KW(V_{gs}-V_t)$, where K is the drive ability factor, W is the transistor width, and V_t is the threshold voltage [27]. In this equation, K and V_t are temperature and supply voltage-dependent. In order to perform a simple extended logical effort model, we try to express K and V_t as simple linear functions of temperature t and supply voltage V_{DD}. Figure 3.6 and Figure 3.7 describe the temperature and supply voltage effects on K and V_t.

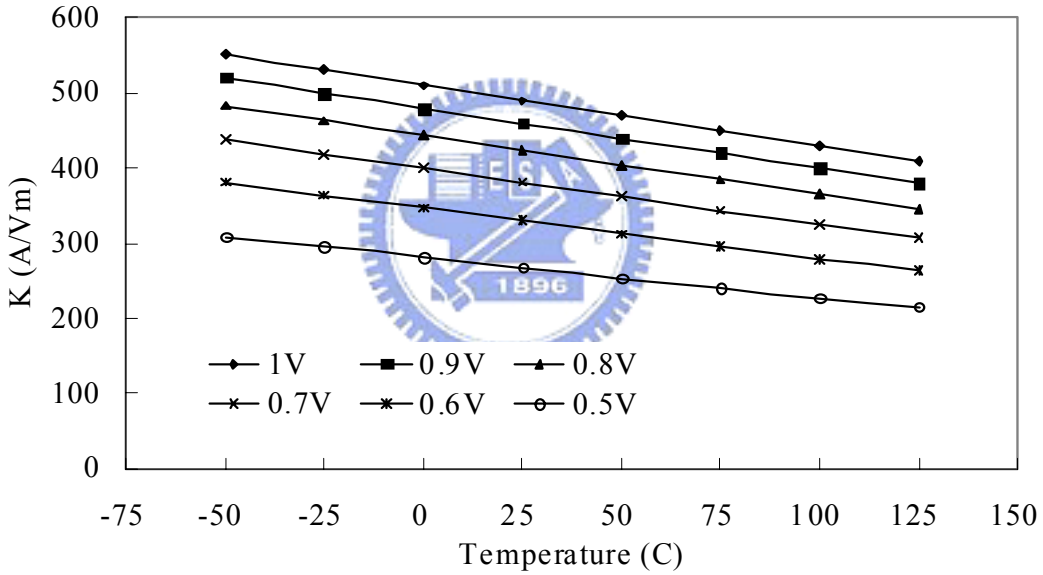


Figure 3.6 The values of K with different temperatures and supply voltages.

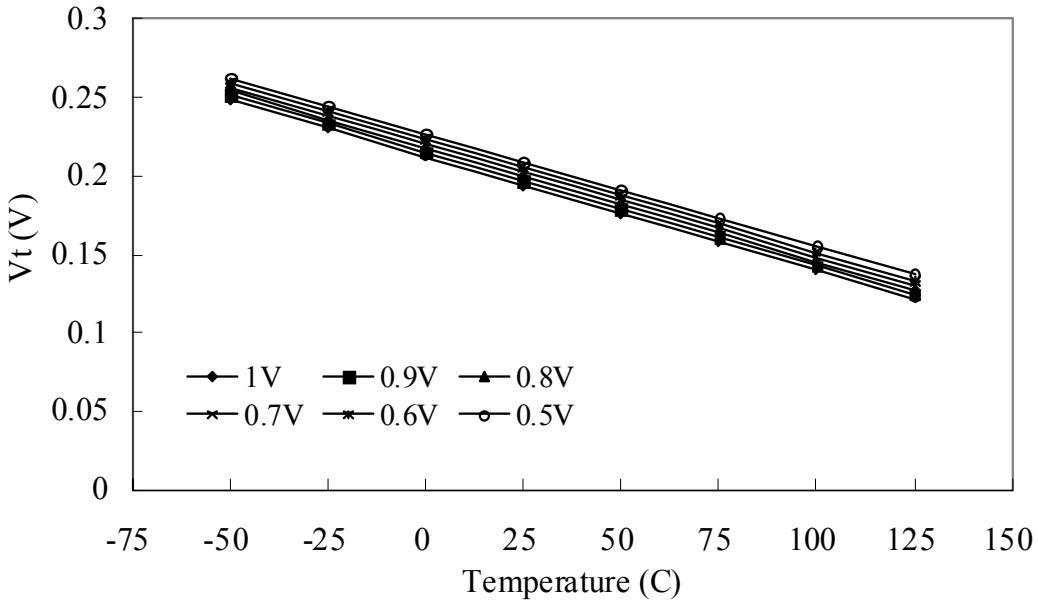


Figure 3.7 The values of V_t with different temperatures and supply voltages.

3.2.2 Drive Ability Factor *K*

Based on Figure 3.6, we can observe that K is close to a linear function of temperature t with different V_{DD}. Thus, we assume K as the equation $K=mt+b$, where m is the slope and b is the intercept. With different supply voltages, we can obtain different values of m and b. Figure 3.8 and Figure 3.9 show the simulation results of m and b in 90nm process. According to simulation results shown as Figure 3.8, b can be rewritten as an approximate equation $b=m_{KV}V_{DD}+K_0$, where m_{KV} and K_0 are constant. With Figure 3.9, since the value of t is in a range of -50~125, the effect of the value of m is much smaller than b, thus we replace m with the average value m_{Kt}. The final approximate equation of K is expressed as

$$K=m_{Kt}t+m_{KV}V_{DD}+K_0. \quad (3.3)$$

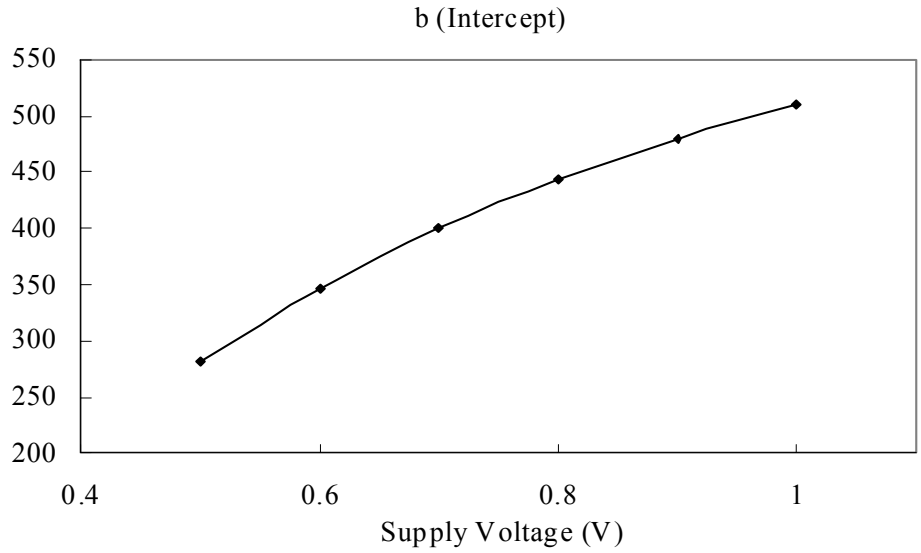


Figure 3.8 The values of *b* with different supply voltages.

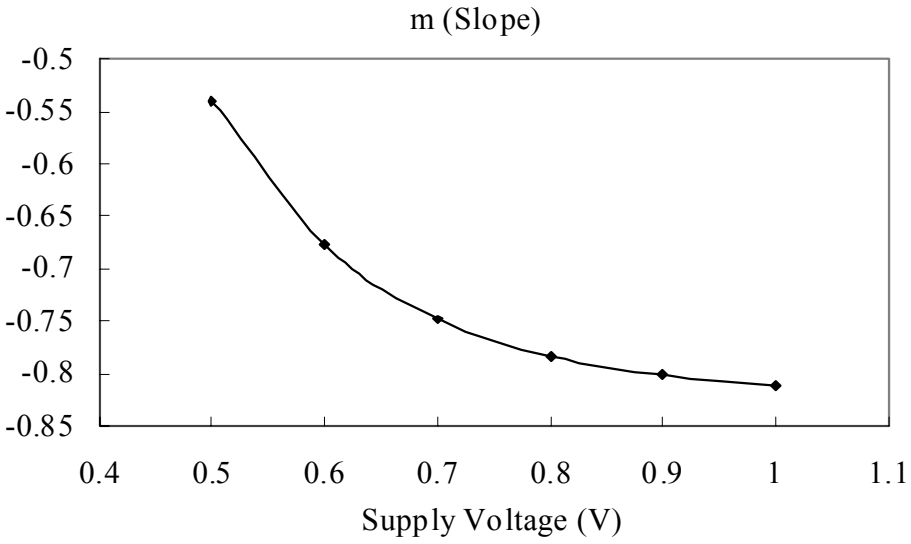


Figure 3.9 The values of *m* with different supply voltages.

3.2.3 Threshold Voltage V_t

V_t is a linear function of temperature t and the effect of supply voltage V_{DD} on V_t is small. In order to simplify the extended logical effort model, the effect of V_{DD} on V_t is ignored and V_t is expressed as the equation

$$V_t = m_{Vt} t + V_{t0} \tag{3.4}$$

where m_{Vt} and V_{t0} are constant.

3.2.4 Input Capacitance C_{in}

According to simulation results, we observed that the effects of temperature and voltage on C_{in} are much smaller than on I_d. In order to simplify the extended logical effort model, the value of C_{in} is assumed as a constant in the proposed model.

Table 3.4 Simulated values of C_{in} with different temperatures and supply voltages. (In 90nm Process)

C_{in} (fF)	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	0.7886	0.7895	0.7898	0.7887	0.7840	0.7701
-25°C	0.7897	0.7904	0.7903	0.7888	0.7836	0.7703
0°C	0.7925	0.7929	0.7925	0.7905	0.7850	0.7721
25°C	0.7970	0.7971	0.7963	0.7939	0.7881	0.7756
50°C	0.8028	0.8026	0.8015	0.7987	0.7927	0.7806
75°C	0.8094	0.8089	0.8076	0.8045	0.7984	0.7866
100°C	0.8163	0.8157	0.8142	0.8109	0.8047	0.7933
125°C	0.8234	0.8226	0.8209	0.8175	0.8113	0.8002

Based on previous analysis results, the equation of logical effort g can be rewritten as (3.5) and (3.6).

$$g = \frac{kV_{DD}C_{in}}{I_d} = \frac{kV_{DD}C_{in}}{KW(V_{DD}-V_t)}. \tag{3.5}$$

$$\frac{1}{g} = \frac{KW(V_{DD}-V_t)}{kV_{DD}C_{in}} = const \cdot \frac{K(V_{DD}-V_t)}{V_{DD}} = const \cdot K(1-\frac{V_t}{V_{DD}}) \tag{3.6}$$

where $const=W/kC_{in}$ is a constant. The expression of K and V_t are $K=m_{KV}V_{DD}+m_{Kt}t+K_0$ and $V_t=m_{Vt}t+V_{t0}$ as shown in Section 3.2.2 and Section 3.2.3. After replacing K and V_t in the formula of $1/g$ with these equations, we simplify the formula by Taylor expansion.

A Taylor expansion of $f(x)$ at $x=a$ is

$$f(x) = \sum \frac{f^n(a)(x-a)^n}{n!} \tag{3.7}$$

where $n=0, 1, 2, ..., \infty$. First, we try to derive $1/g$ into a linear function of supply voltage V_{DD} through Taylor expansion:

$$\frac{1}{g} = f(V_{DD}) \approx f(a) + f'(a)(V_{DD}-a) = A(t)\cdot V_{DD} + B(t) \tag{3.8}$$

where

$$\begin{aligned} A(t) &= \frac{const \cdot m_{Kt} \cdot m_{Vt}}{a^2} \cdot t^2 \\ &+ \frac{const(m_{Kt} \cdot V_{t0} + K_0 \cdot m_{Vt})}{a^2} \cdot t \\ &+ const(m_{KV} + \frac{K_0 \cdot V_{t0}}{a^2}) \end{aligned} \tag{3.9}$$

and

$$B(t) = \frac{-2 \cdot const \cdot m_{Kt} \cdot m_{Vt}}{a} \cdot t^2 + const\left(m_{Kt} - m_{KV} \cdot m_{Vt} - \frac{2(m_{Kt} \cdot V_{t0} + K_0 \cdot m_{Vt})}{a} \right) \cdot t + const\left(-m_{KV} \cdot V_{t0} + K_0 - \frac{2K_0 \cdot V_{t0}}{a} \right). \quad (3.10)$$

For presenting a simple linear extended logical effort model and after evaluating *A(t)* and *B(t)*, the final extended model of *g* is presented as the following formula:

$$1/g = (m_t t + b_t) V_{DD} + C \quad (3.11)$$

where t is the temperature, V_{DD} is the supply voltage,

$$m_t t + b_t = \frac{const(m_{Kt} \cdot V_{t0} + K_0 \cdot m_{Vt})}{a^2} \cdot t + const(m_{KV} + \frac{K_0 \cdot V_{t0}}{a^2}), \quad (3.12)$$

and C is the average of the value of *B(t)*. The values of m_t, b_t, and C are constant in each process.

3.3 Analysis Flow

To sum up above steps, Figure 3.10 shows an overview of the simulation and analysis flow.

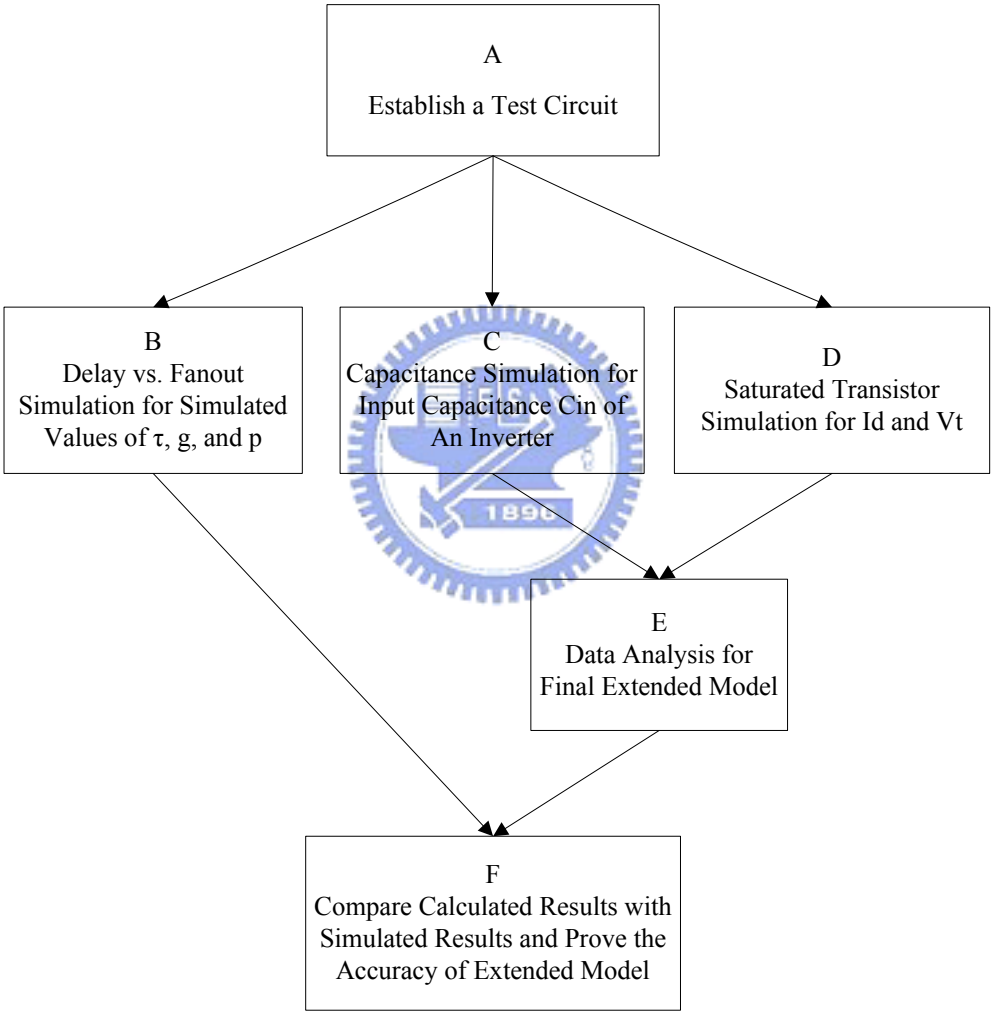


Figure 3.10 An overview of the simulation and analysis flow.

The following is the statement of Figure 3.10:

A. Select an inverter with suitable transistor size as a unit inverter, and then establish a 5-stage inverter chain as the test circuit to imitate a real logic path.

B. Obtain simulated values of delay d_{abs} with different values of fanout h through the test circuit. Then evaluate the simulated values of τ, g, and p by the equation $d_{abs}=\tau(gh+p)$ and the curves of d_{abs} vs. h under different temperature and supply voltage conditions.

C. Simulate with a unit inverter, give input 0 and 1, and then obtain the average value of input capacitance C_{in} under different temperature and supply voltage conditions.

D. Simulate with each PMOS and NMOS transistor, and obtain the values of saturation current I_d and threshold voltage V_t under different temperature and supply voltage conditions.

E. Use the data received from above steps, calculate the values of equation $1/g=(m_t t+b_t)V_{DD}+C$, and obtain the calculated values of g.

F. Compare the calculated values of g with simulated values, then, we can prove that the proposed extended model is accurate enough.

A new extended logical effort model which takes temperature and voltage into account has been established. The proposed model enables designers to estimate the logic path delay and to optimize an *N*-stage logic network under different temperature and supply voltage conditions with minimum effort by (2.2), (2.4), (2.5), and (3.11). It can avoid a serious misestimate induced by temperature and supply voltage variations.

Additionally, because the parasitic delay *p* will be dominated by the style and area of layout and wire routing, we don't discuss these issues here.

3.4 Validation

Figure 3.11and Figure 3.12 show the comparison between simulated and calculated values of *g* and *1/g* in 90nm process in 2-D and 3-D charts. The calculated value of *g* is obtained from (3.11). In Figure 3.11, we can find that the calculated values are close to the simulated values. In 90nm process, the transistors work approaching triode region at 0.5V and the inaccuracy of the simulation tools inherently are the occasions of the big difference between calculated and simulated values at 0.5V. In Figure 3.12, we provide a 3-D chart to emphasize the linear relationship between *1/g* and temperature and voltage. After validation, the accuracy of this simple extended logical effort model can achieve about 90%.

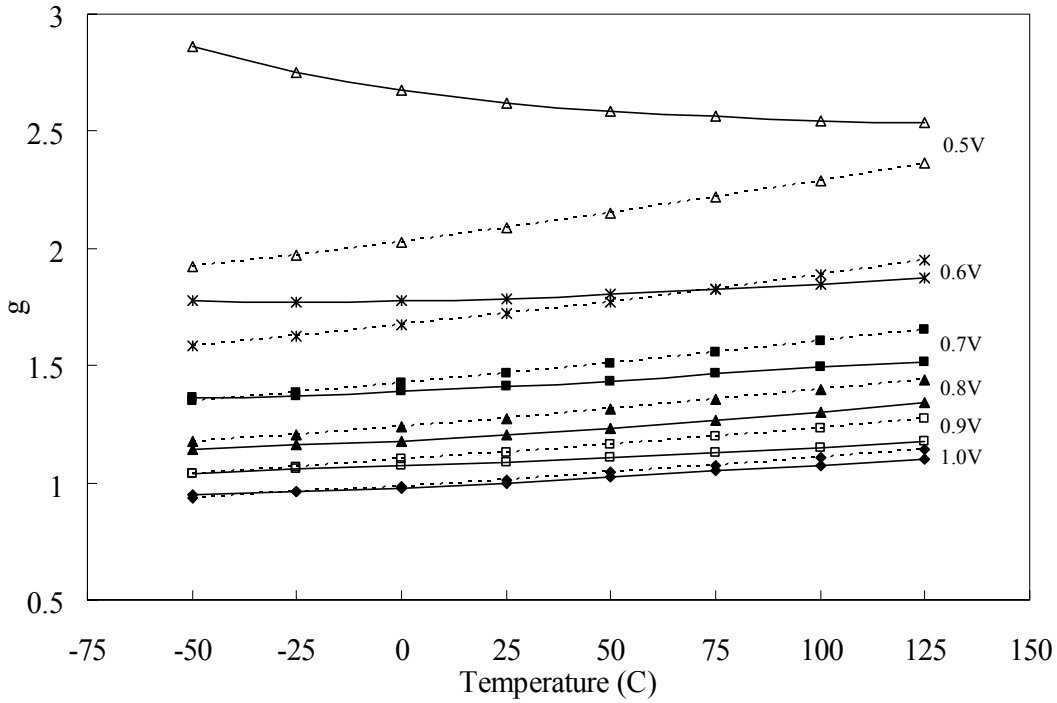


Figure 3.11 The comparison between simulated and calculated values of *g* in 2-D. Simulated values are solid lines and calculated values are dotted lines.

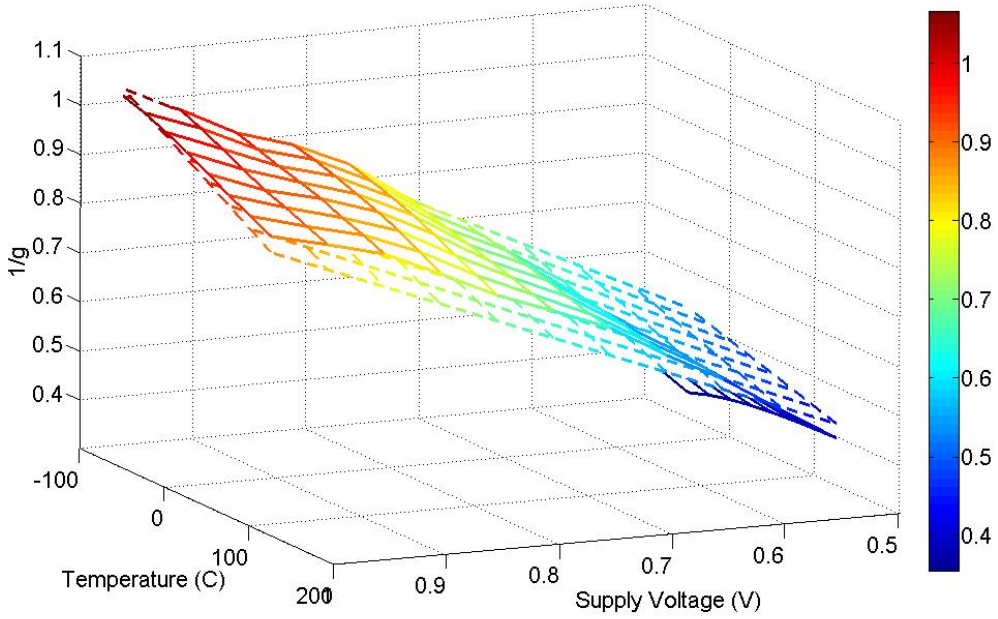


Figure 3.12 The comparison between simulated and calculated value of 1/g in 3-D. Simulated values are solid lines and calculated values are dotted lines.

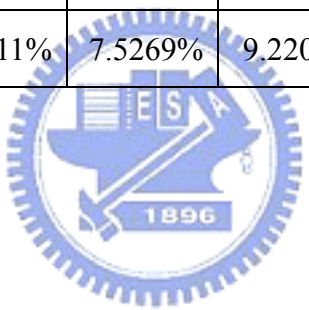
The simulated values of logical effort *g* are shown in Table 3.1, and the calculated values of logical effort *g'* are shown in Table 3.5. Table 3.6 demonstrates the variation between the calculated value *g'* and the simulated value *g*. All statistics shown in these tables are in 90nm process.

Table 3.5 Calculated values of *g'* with different temperatures and supply voltages. (In 90nm Process)

g'	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	0.9346	1.0415	1.1761	1.3505	1.5858	1.9203
-25°C	0.9596	1.0695	1.2078	1.3871	1.6290	1.9731
0°C	0.9860	1.0990	1.2412	1.4257	1.6747	2.0289
25°C	1.0139	1.1302	1.2766	1.4666	1.7230	2.0880
50°C	1.0434	1.1632	1.3140	1.5098	1.7741	2.1506
75°C	1.0747	1.1982	1.3537	1.5556	1.8284	2.2171
100°C	1.1079	1.2353	1.3959	1.6044	1.8861	2.2879
125°C	1.1432	1.2748	1.4407	1.6563	1.9476	2.3633

Table 3.6 The variation between simulated and calculated values of *g*.
(In 90nm Process)

(g'-g)/g	1V	0.9V	0.8V	0.7V	0.6V	0.5V
-50°C	-1.4429%	-0.0555%	2.9105%	-0.9751%	-10.7603%	-32.9781%
-25°C	-0.1573%	1.1733%	4.0485%	1.0204%	-7.9686%	-28.2516%
0°C	0.7012%	2.3666%	5.1941%	2.6654%	-5.6585%	-24.1423%
25°C	1.3902%	3.8021%	6.0639%	4.0418%	-3.5891%	-20.3865%
50°C	1.7992%	5.2345%	6.6090%	5.2402%	-1.6493%	-16.8856%
75°C	2.2666%	6.1049%	6.6884%	6.2844%	0.1446%	-13.5008%
100°C	2.9255%	7.4494%	7.1243%	7.2608%	2.0375%	-10.1914%
125°C	3.7496%	8.5011%	7.5269%	9.2208%	4.0170%	-6.8574%



Chapter 4

Design Procedure and Application Scenarios

4.1 Circuit Design Flow with Proposed Model

In Chapter 3, the effects of temperature and supply voltage variations are revealed and the logical effort model extension for temperature and voltage variations is proposed. In this section, the circuit design flow with proposed model will be interpreted clearly.

As discussed in previous chapters, the increasing transistor density and operation frequency of the integrated circuits will induce the raising chip temperature. And the temperature variation will influence the speed of the circuits and may cause incorrect operation or an error. Due to the thermal problems which can not be ignored, the thermal simulation of the integrated circuits is necessary indeed. Combining the proposed extended logical effort model with existing thermal simulators, the utility of the proposed model can be fulfilled. Figure 4.1 is the flowchart for circuits design with proposed extended logical effort model and thermal simulation. For temperature variation, thermal simulation is an important procedure for acquiring temperature information of the chip.

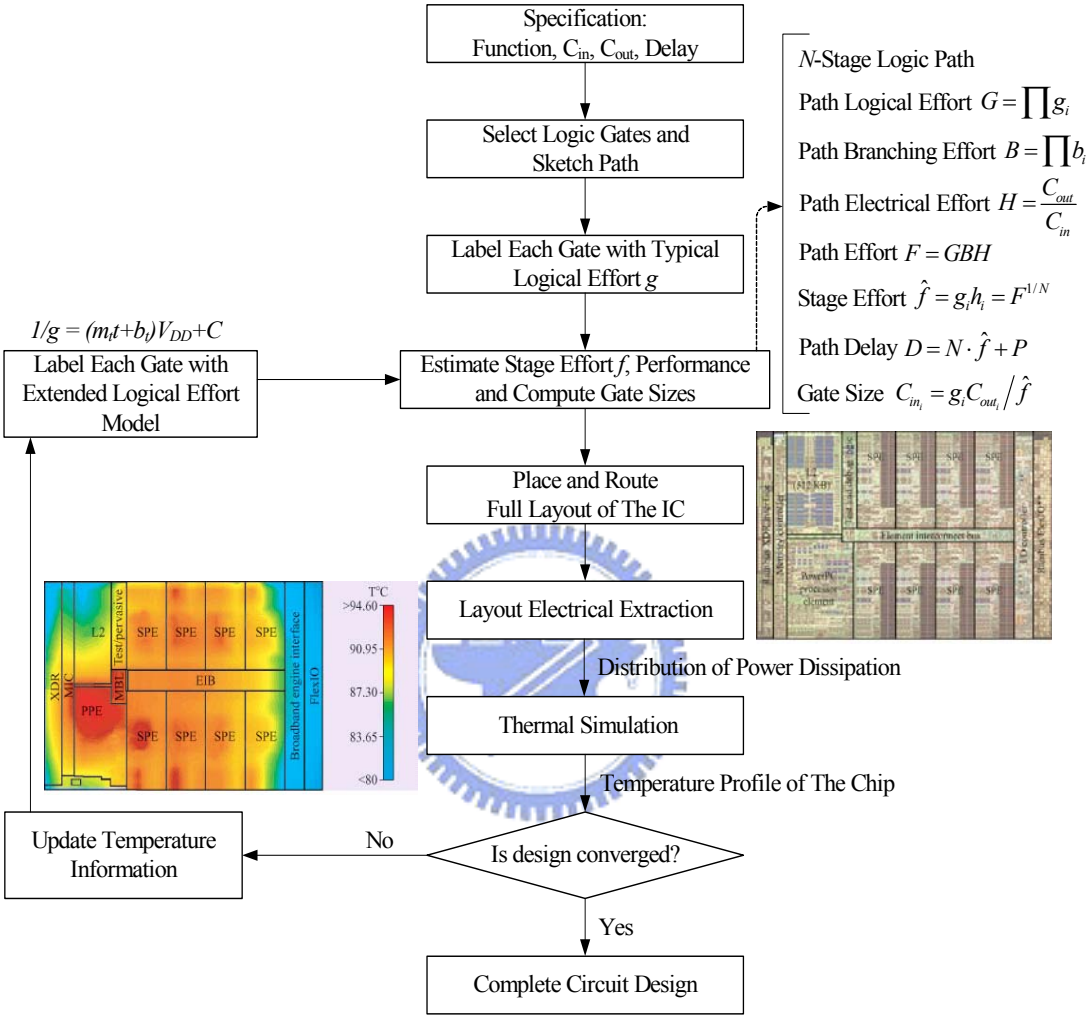


Figure 4.1 The circuit design flow with proposed extended model [14], [21], [28].

The flowchart illustrates a simple design procedure from the given specification to the circuit completion, and the design example in Section 2.3 can help to realize this chart.

In the beginning, the function, input and output capacitances, and the delay constraint of the logic paths should be confirmed. Based on the requested functions, designers can choose what kinds of logic gates are used and the logic paths of the functional blocks can be established. When the logic gates and paths are decided, the typical logical effort g of each kind of logic gate will be used to compute the stage effort f and the size of each gate. Then, the performance of the circuits can be estimated.

After determining the each gate size of the circuits, the gate placement and wire routing will be executed, and the electrical parameters can be extracted subsequently. According to the information of electrical extraction, the distribution of power dissipation will be supplied to thermal simulator to calculate the chip temperature by solving the heat equation [28]. When first time the temperature information is obtained, the updated operating temperature will be used as the variable of the proposed extended logical effort model. And then the new values of logical effort g with temperature information can be calculated. As the more accuracy values of g are obtained, the new estimations of stage effort f and the circuit performance are also more realistic.

According to new estimation results, the size of each gate and the layout of the chip will be rearranged, and the electrical extraction and thermal simulation will be executed again. While updated electrical and thermal information is generated, circuit

designers can determine whether the design is convergent in performance or temperature constraint or not. The condition of design convergency is decided by designers. If the circuit characteristics satisfy the condition of convergency, the design flow is completed. Otherwise, the simulation loop will run continually.

4.2 Application Scenarios

In Section 4.1, the design procedure with proposed model is presented with the flowchart and the description. As we mentioned before, estimating circuit performance and optimizing circuit design for minimum delay are two key purposes of logical effort model. For estimating circuit delay, the accuracy is one of the most important considerations. Clock tree is a cogent example which needs high accuracy and reliability.

Figure 4.2 is an illustration of a clock tree, and the dotted circles represent the hotspots in the functional block or a chip. When hotspots appear, the temperature gradients occur and will also influence the performance coherence of the system. In addition to the hotspots which are generated by other circuits, the elevated temperature in the clock driver area also reduces the performance of the clock drivers and other local logic, directly impacting circuit performance [29]. These variations may induce intolerable and unrecoverable errors of the chip function.

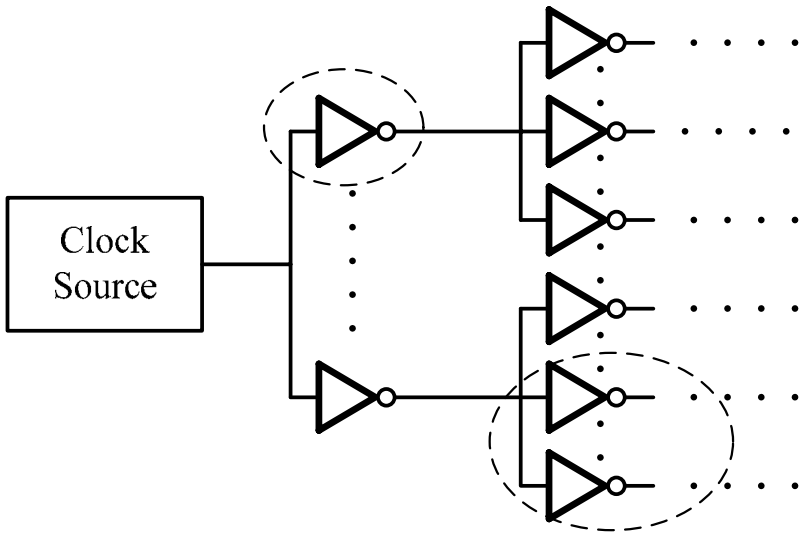


Figure 4.2 An illustration of clock tree.

To illustrate the relationship between clock distribution, chip temperature, and clock skew over the chip, the following are three figures showing some features of Alpha 21164 microprocessor [29]. Figure 4.3 shows the clock driver location of Alpha 21164 microprocessor. According to Figure 4.4, the temperature gradients of the microprocessor are exhibited. And Figure 4.5 shows the results of the Alpha 21164 clock skew analysis. In fact, these three appearances are interactive; the temperature gradient is induced by the clock driver location, and the clock skew over the chip is affected by both clock driver location and the temperature.

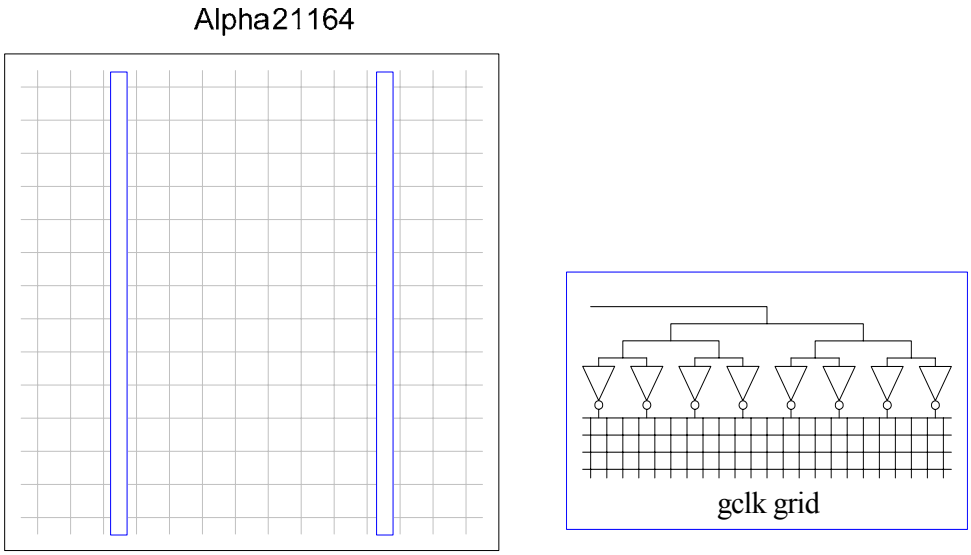


Figure 4.3 The clock driver location of Alpha 21164 microprocessor [29].

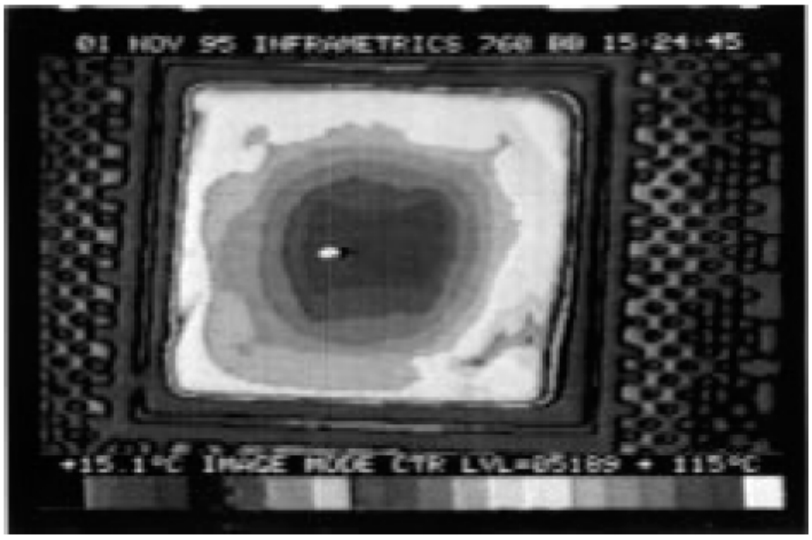


Figure 4.4 The thermal image of Alpha 21164 microprocessor [29].

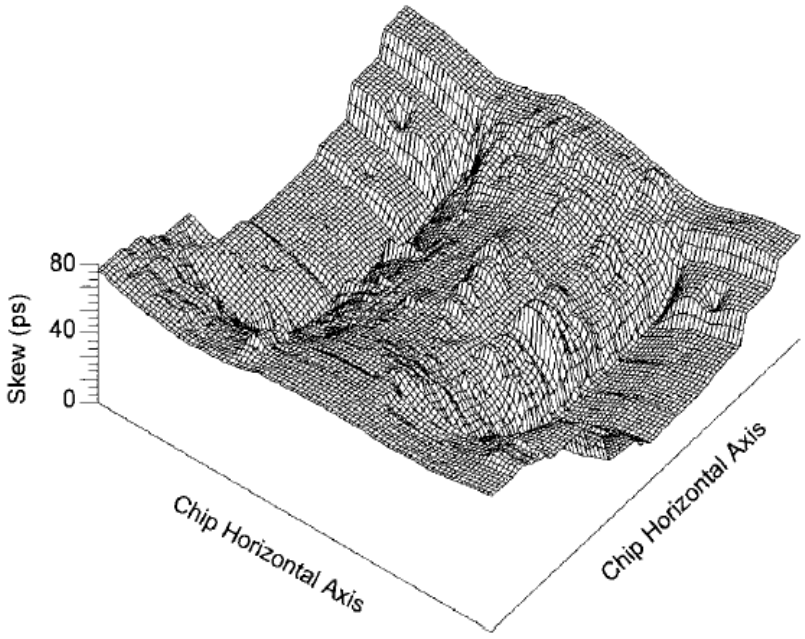


Figure 4.5 The clock skew of Alpha 21164 microprocessor [29].

In addition to the clock tree, the critical path of the chip is another example to highlight the importance of the accuracy of delay model. Figure 4.6 is an illustration of a critical path, and the dotted circles represent the hotspots in the functional block or a chip. It has been known that higher temperature will induce longer delay. When hotspots appear in the critical path, it will slow the path and may violate the timing constrain. Also, these variations may induce unrecoverable errors of the chip function.

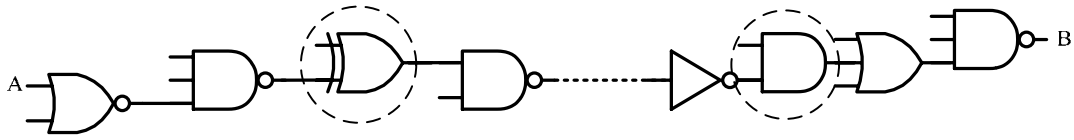


Figure 4.6 The illustration of a critical path and the hotspots.

Based on proposed temperature-aware logical effort model and thermal simulation, the thermal effect of the chip can be considered more completely. The information of temperature distribution and an accurate temperature-aware delay model can be used to design the clock network and the critical paths properly, and the misestimate caused by thermal non-uniformity can be compensated. The layout of the integrated circuits can be rearranged and logic gates in the hotspots can be resized under higher temperature conditions, therefore the circuit can meet the performance constraints and the design will have better reliability.

In the beginning, we have declared that the purpose of this thesis is presenting an extended model which supports for temperature and voltage variations. Above discussions are about the consideration of temperature variation for the most part. While mentioning the supply voltage effect, the design of voltage islands and the technique of dynamic voltage scaling are some examples for describing the application of proposed model.

In the conception of power management, voltage islands and dynamic voltage scaling are common and useful techniques to reduce power consumption. The main procedures of these two techniques are accomplishing individual voltage optimization of each functional block and scaling the supply voltage dynamically with system operational requirements. While reducing supply voltage, the circuit performance will also be reduced and the operational frequency should be adaptive. For this reason, an accurate voltage-aware delay model is needed to adjust the clock frequency and evaluate the timing information correctly under different supply voltage conditions.

4.3 Design Examples

4.3.1 Example of Traditional Logical Effort Model

Figure 4.7 shows an example of the critical path in a circuit block. The initial NOR2 gate presents a load of 5λ of transistor width on the input and the output load is equivalent to 2000λ of transistor width.

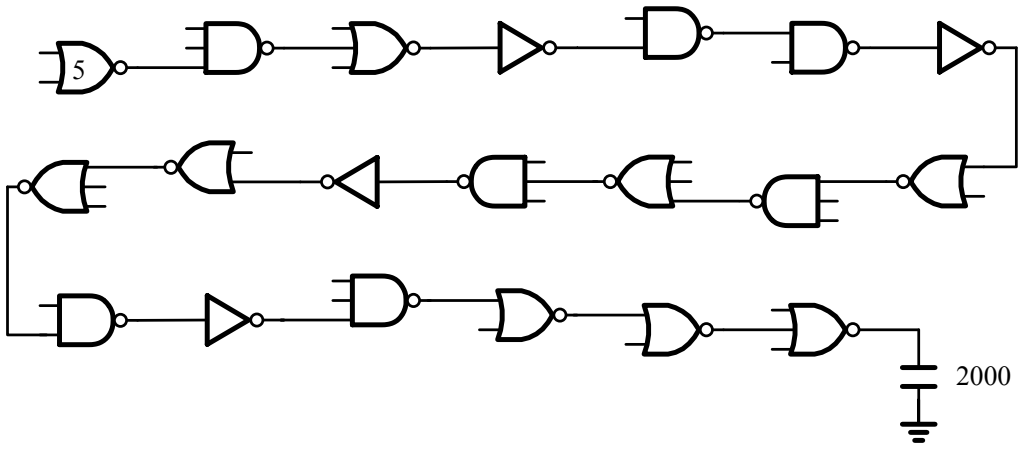


Figure 4.7 An example of the critical path.

If we ignore the factor of temperature and analyze this logic path with traditional logical effort model, the computation process is shown as follows:

The number of stages $N = 20$, and path branching effort $B = 1$.

$g_{inv} = 1$, $g_{nand2} = 4/3$, $g_{nand3} = 5/3$, $g_{nor2} = 5/3$, and $g_{nor3} = 7/3$.

→ Path logical effort $G = 6972.0758$.

Path electrical effort $H = 2000/5 = 400$.

→ Path effort $F = G \times B \times H = 2788830.3037$.

The delay of a gate $d = f + p$.

The path delay is minimum when each stage has the same stage effort

→ $\hat{f} = \sqrt[N]{F} = \sqrt[20]{2788830.3037} = 2.1003$.

$p_{inv} = 1$, $p_{nand2} = p_{nor2} = 2$, and $p_{nand3} = p_{nor3} = 3$.

→ Path parasitic delay $P = 44$.

The minimum path delay $D = N \times \hat{f} + P = 86.0050$ in unit of τ.

Decide the transistor sizes:

$\hat{f} = g \times h = g \times (C_{out} / C_{in}) \rightarrow C_{in} = (g \times C_{out}) / \hat{f}$.

The sizes of each gate are shown in Table 4.1.

Table 4.1 The sizes of logic gate in the example path.

(1) 5.0000	(2) 6.3008	(3) 7.9399	(4) 7.1468	(5) 15.0100
(6) 23.6435	(7) 37.2430	(8) 78.2197	(9) 98.5685	(10) 124.2112
(11) 111.8034	(12) 140.8891	(13) 295.9024	(14) 372.8815	(15) 335.6334
(16) 528.6856	(17) 1110.3723	(18) 1399.2360	(19) 1763.2477	(20) 2221.9571

4.3.2 Computation with Extended Logical Effort Model

In fact, each gate in the logic path has different temperature conditions. When temperature variation occurs, how will the delay of the path be effected? In this section, we take temperature condition into account and analyze the same logic path with proposed extended logical effort model again. The example logic path is shown as Figure 4.8. The computation process is shown as follows:

According to the proposed model, $1/g = (m_t t + b_t)V_{DD} + C$, different temperature t will cause different values of logical effort g.

Here we take 90nm process as an example:

$m_t = -1.1157e\text{-}3$, $b_t = 1.0426$, $C = -0.0284$, and $V_{DD} = 1V$.

The path delay with temperature condition is:

$$D = \sum_i (g_i h_i + p_i) = \sum_i g_i h_i + P = 88.4305 \text{ in unit of } \tau.$$

Comparing with $D = 86.0050$ which is obtained in previous section, this new value is more practical.

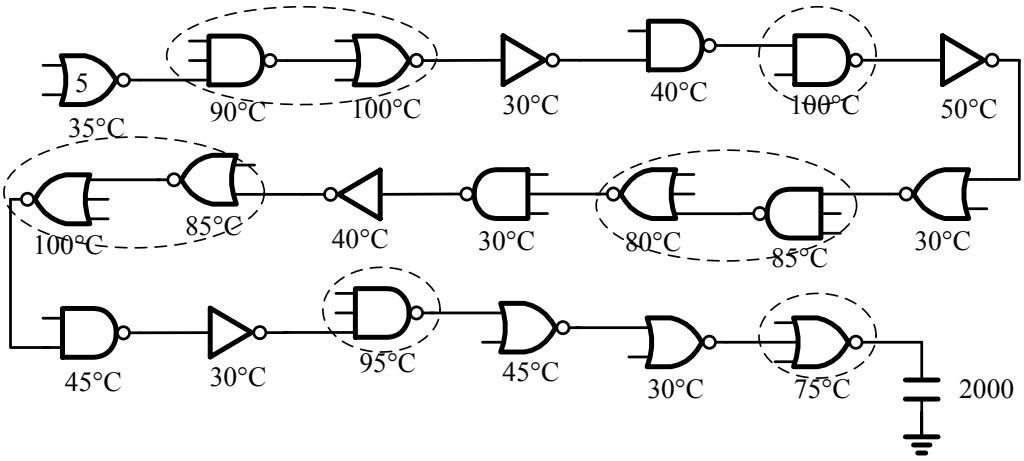


Figure 4.8 An example of the critical path with temperature condition.

4.3.3 Design Optimization with Extended Logical Effort Model

Based on the temperature condition shown in Figure 4.8, we can do optimization with proposed model and obtain better circuit performance:

Similarly, according to the proposed model, $1/g = (m_t t+b_t)V_{DD}+C$, different temperature t will cause different values of logical effort g.

Here we take 90nm process as an example:

$m_t = -1.1157e-3$, $b_t = 1.0426$, $C = -0.0284$, and $V_{DD} = 1V$.

→ Path logical effort $G = 21198.4871$.

Path electrical effort $H = 2000/5 = 400$.

The minimum stage effort: $\hat{f} = \sqrt[N]{F} = \sqrt[20]{8479394.8333} = 2.2203$

The minimum path delay: $D = N \times \hat{f} + P = 20 \times 2.2203 + 44 = 88.4067$ in unit of τ.

According to $C_{in} = (g \times C_{out}) / \hat{f}$, new sizes of each gate are shown in Table 4.2.

After resizing, the delay of the path becomes smaller indeed.

Table 4.2 The new sizes of logic gate in the example path.

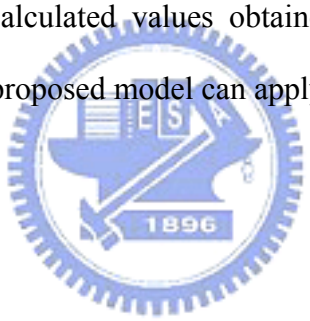
(1) 5.0000	(2) 6.4955	(3) 7.9073	(4) 6.7917	(5) 14.7892
(6) 23.8783	(7) 35.8916	(8) 76.3774	(9) 99.7891	(10) 122.2196
(11) 107.5717	(12) 140.5453	(13) 302.5622	(14) 370.5718	(15) 318.2905
(16) 510.9485	(17) 1112.6139	(18) 1346.1689	(19) 1728.7936	(20) 2258.7162

4.4 Verification of Logic Gates

In this section, the application of the extended logical effort model to other logic gates is demonstrated. The following statistics are obtained in 90nm process.

In Chapter 3, the proposed model is presented as $1/g = (m_t t+b_t)V_{DD}+C$. And according to the introduction in Chapter 2, the values of g of other logic gates should be the value of g of unit inverter multiplied by different constants. The constants are decided by the topology and the transistor size of each gate.

The following figures show the comparison between simulated values obtained by simulation tool and the calculated values obtained by proposed model. These analysis results show that the proposed model can apply to other kinds of logic gate.



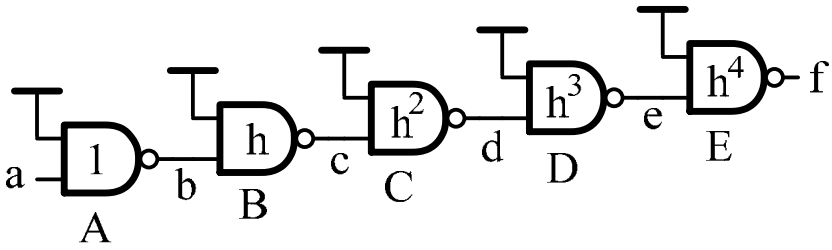


Figure 4.9 Test circuit for calibrating the logical effort model of NAND2.

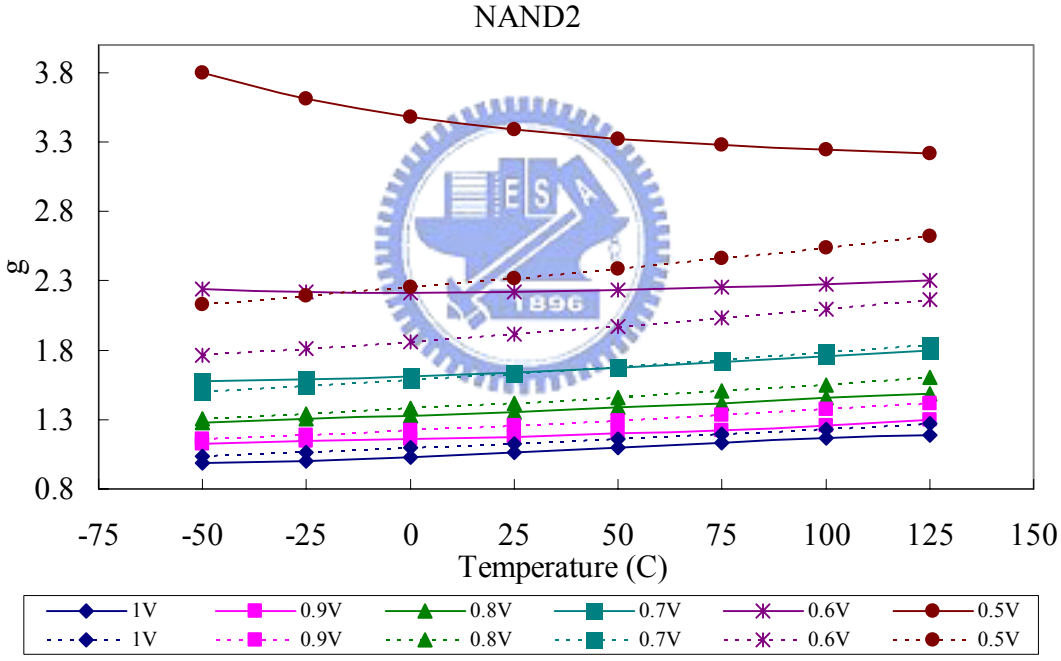


Figure 4.10 The comparison between simulated and calculated values of *g*. Simulated values are solid lines and calculated values are dotted lines.

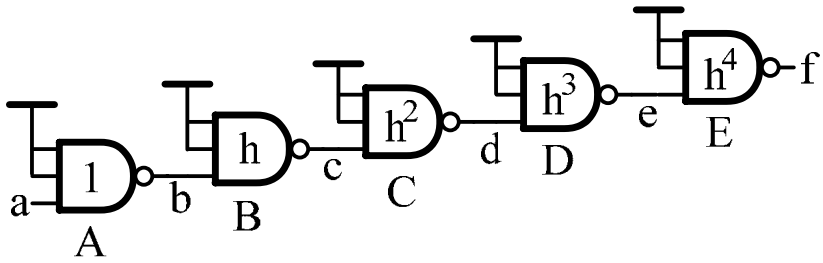


Figure 4.11 Test circuit for calibrating the logical effort model of NAND3.

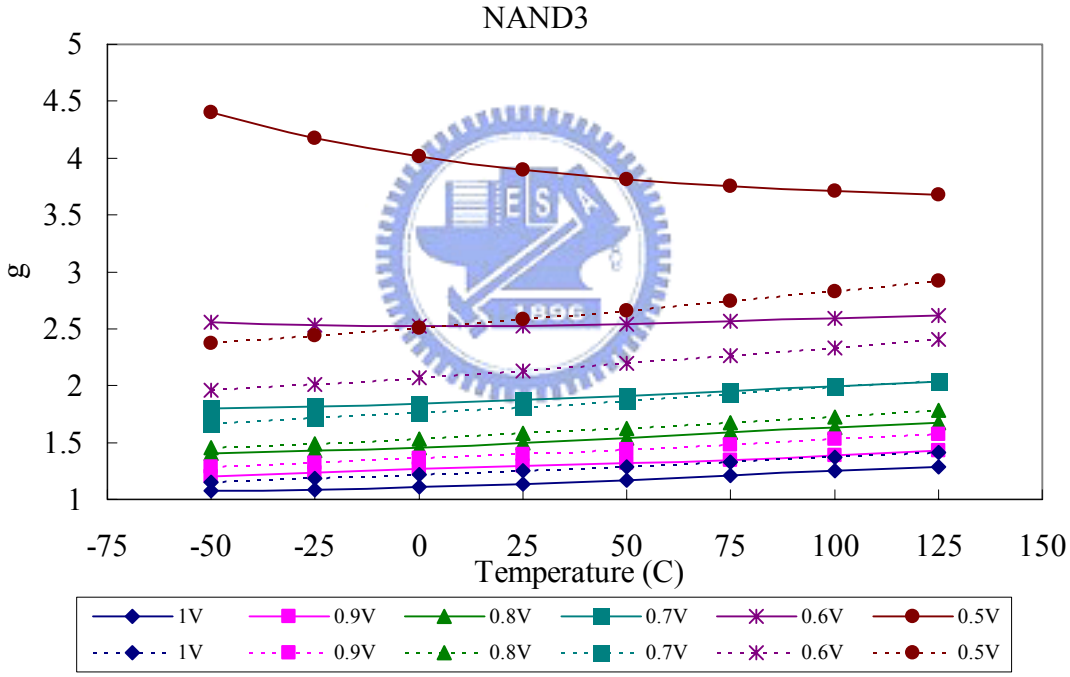


Figure 4.12 The comparison between simulated and calculated values of *g*. Simulated values are solid lines and calculated values are dotted lines.

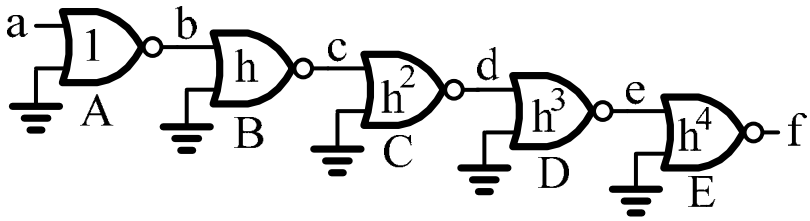


Figure 4.13 Test circuit for calibrating the logical effort model of NOR2.

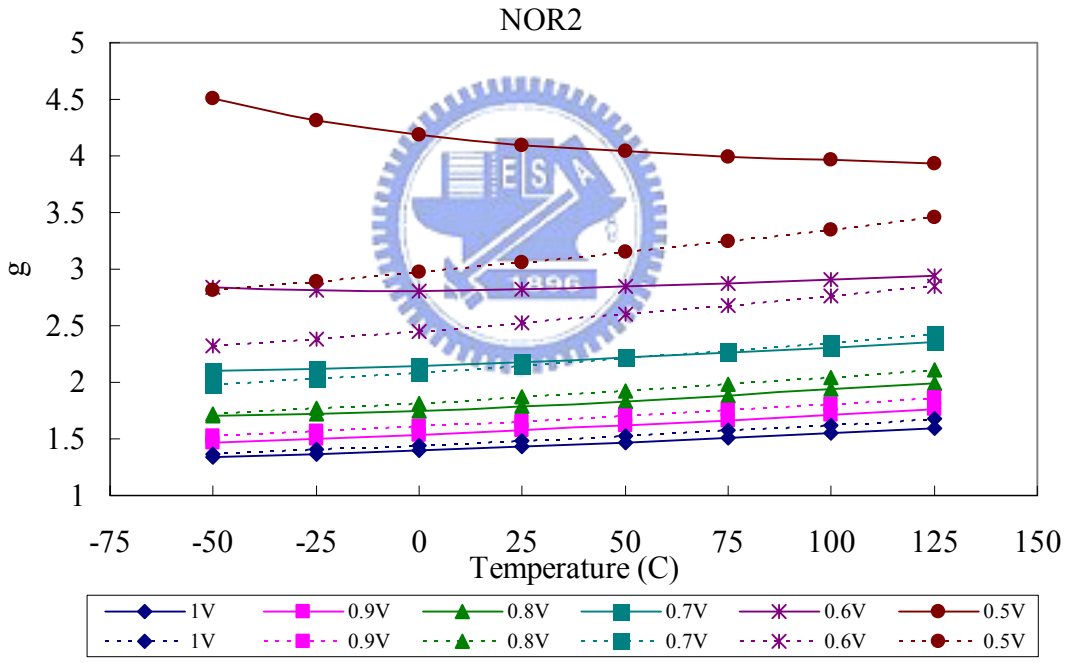


Figure 4.14 The comparison between simulated and calculated values of *g*. Simulated values are solid lines and calculated values are dotted lines.

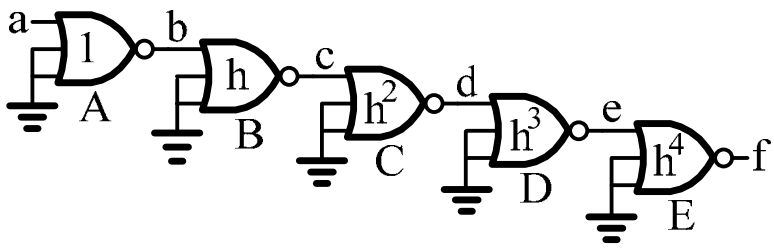


Figure 4.15 Test circuit for calibrating the logical effort model of NOR3.

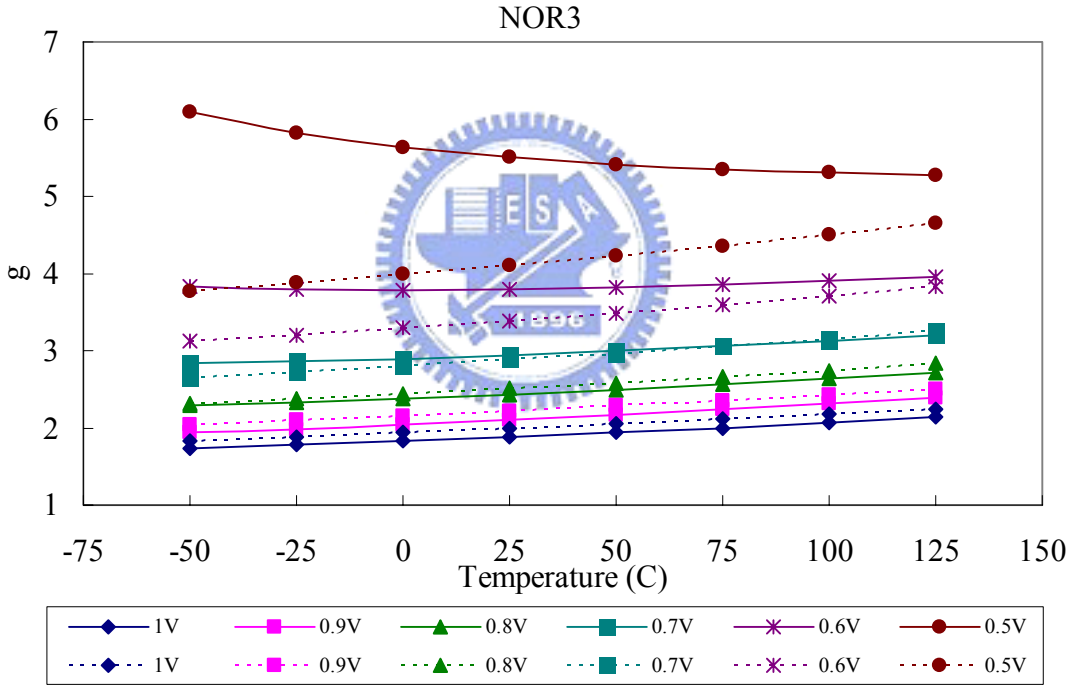


Figure 4.16 The comparison between simulated and calculated values of *g*. Simulated values are solid lines and calculated values are dotted lines.

Chapter 5

Conclusion

5.1 Conclusion

In the integrated circuits design, good productions are usually constructed with some factors such as high performance, low power, well reliability, and inexpensive to manufacture. In order to fulfill these requirements, a lot of researches, design methodologies, circuit simulation models, and computer-aided design (CAD) tools have been proposed to improve the accuracy of circuit estimation, decrease design cycle time, and reduce entire cost of the productions.

The method of "Logical Effort Delay Model" allows designers to quickly estimate delay time and optimize logic paths. But the traditional logical effort model may not estimate logic path delay correctly while temperature and supply voltage changing. According to simulation results, delay time increases 21% while temperature increasing from 0°C to 125°C, and increases 2X while supply voltage decreasing from 1V to 0.5V in 90nm process.

To propose a simple model to estimate and optimize circuit delay with variations easily and correctly, we present a simple linear extended logical effort model, $1/g = (m_t t+b_t)V_{DD}+C$, to support for temperature and supply voltage variations. The linear characteristic is convenient for designers to quickly estimate logic path delay and

optimize an *N*-stage logic network, and the integration of proposed model and CAD tools is easier.

The simulation and analysis flow is established and the validation of the proposed model is shown in Chapter 3. The circuit design flow with proposed extended logical effort model is presented in Chapter 4. Moreover, we provide some application scenarios of the proposed extended model in different situations and under distinct temperature and supply voltage conditions. For instance, the clock network and the critical paths are cogent examples which need high accuracy and reliability. And the low power techniques of voltage islands and dynamic voltage scaling are some examples for describing the application of supply voltage consideration. These examples can help designers to understand how to perform circuit estimation and optimization by the proposed model.

In addition to delay estimation and circuit optimization, each functional block on a chip can be optimized under different PVT conditions through this simple model further. After validation, the accuracy of this new extended logical effort model can achieve about 90%. And the proposed model is demonstrated that it can apply to different kinds of logic gate.

5.2 Future Works

The theory of logical effort is based on the simple RC delay model, and thus it is convenient to estimate delay and optimize circuits design, but it also ignores some factors like input transition time, I/O coupling capacitance or the delay of interconnect wire. Nevertheless, many logical effort model researches adapting to different design conditions have been presented to improve the accuracy. For a more precise application of logical effort model, the extended model for temperature and voltage variations introduced in this thesis can be combined with other proposed models.

The proposed model in this thesis is a simple linear extension for temperature and voltage variations. In fact, the relationship between the reciprocal of logical effort and temperature or voltage is not linear absolutely. Although it is fast to complete delay estimation and is easy to integrate into CAD tools, the proposed model also has the limitation when more accuracy is needed.

Finally, we can reveal the difference between the calculated results of the proposed extended model and the hardware experimental results afterward. We can also improve our research by these comparisons and increase the reliability of the proposed model. These results will become reference materials for the better delay model design and other applications in the future.

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