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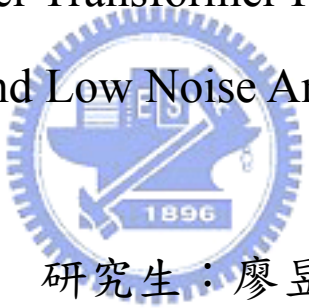
低功率變壓器回授與低電壓多頻之壓控震盪器和超寬頻系統之低雜訊放大器設計與研究

Design of Low Power Transformer Feedback and Low voltage Multi-Band VCO and Low Noise Amplifier for UWB System



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中 華 民 國 九 十 七 年 六 月

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摘　　要

本論文討論的第一主題是壓控震盪器的分析和設計。在第一主題中：探討三種不同類型的壓控震盪器：基底回授與超低功率之變壓器型式壓控震盪器和低電壓多頻之帶壓控震盪器與其除頻器。為了達到高頻的操作，變壓器架構基底回授的方式，量測結果顯示：在供應電壓 1.5V 功率消耗 6.2 毫瓦的條件下，可調範圍 8.14~8.61 GHz，相位雜訊為-113dBc/Hz@1MHz。採用汲極與源極端的回授，則可達到超低功率的應用，量測結果顯示出：可調範圍 5.13- 5.42 GHz，相位雜訊為-114dBc/Hz@1MHz，而在 0.5V 供應電壓下，功率消耗僅 0.57mW。另外，提出壓控震盪器適用於多頻帶正交分頻多工超寬頻的系統，其中壓控震盪器產生 Band 6~9 的載波頻率，而除頻器產生 Band 1,2，並且由二對一多工器輸出選擇信號來自壓控震盪器或是除頻器，量測結果顯示出：可調範圍 5.85- 7.93 GHz，相位雜訊為-116dBc/Hz@1MHz，總功率消耗共 36.2mW。

第二主題為：介紹一個寬頻的低雜訊放大器，其輸入匹配利用電晶體雜散電容來達成，此方法可以使輸入匹配網路簡化，並且減少雜訊的貢獻。其模擬結果顯示 3.1GHz~10.6GHz，其輸入返回損耗和輸出返回損耗皆在-10dB 以下，增益為 15dB，最小雜訊指數為 4. 2dB，電路功率消耗為 19.8 毫瓦。

Design of Low Power Transformer Feedback and Low voltage Multi-Band VCO and Low Noise Amplifier for UWB System

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ABSTRACT

This thesis about part one discusses the design and analysis of voltage-controlled oscillator. In part one, we discuss three kinds of VCO：Back-gate feedback and ultra low power transformer based VCO and low voltage multi-band VCO with its divider. In order to achieve higher frequency operation, transformer is feedback to the back gate. The measured results reveal that the power consumption is 6.2mW for 1.5V supply voltage, the tuning rage is between 8.14~8.61 GHz, the phase noise is -113dBc/Hz@1MHz. Adopting transformer feedback from drain to source enables ultra-low power application. The measured results reveal that the tuning rage is between 5.13~5.42 GHz, the phase noise is -114dBc/Hz @1MHz, the power consumption is only 0.57mW under 0.5V supply voltage. Besides, for MB-OFDM UWB system, the VCO generates the carrier frequency for Band 6~9, the divider generate Band 1,2, and multiplexer select the signal from the VCO or Divider. The measured results reveal that the tuning rage is between 5.85~7.93 GHz, the phase noise is -113dBc/Hz @1MHz, the total power consumption is 36.2mW.

The second part introduces an ultra-wide band low noise amplifier. It uses the intrinsic capacitance of transistors to achieve the input matching and the complicated input matching network is replaced. The simulation result of UWB LNA demonstrates S11 <

-10dB and S22 < -10dB from 3.1 to 10.6 GHz. The power gain (S21) is 15dB. The minimum noise figure is 4.2dB.

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昱舜 *Sirius* 於 2008 年 風城 夏

CONTENTS

Chinese Abstract I

English Abstract II

Acknowledgement IV

Contents V

List of Tables VII

List of Figures VIII

Chapter 1 Introduction ..... - 1 -
1.1 Background and motivation ..... - 1 -
1.2 Thesis organization ..... - 3 -
Chapter 2 CMOS voltage-controlled oscillator with transformer feedback. - 4 -
2.1 Introduction ..... - 4 -
2.2 Circuit Design Consideration ..... - 5 -
2.2.1 X-band Low phase noise QVCO with back-gate transformer feedback - 5 -
2.2.2 5.25GHz Low power VCO with drain-source Transformer feedback - 9 -
2.3 Chip layout and simulation results ..... - 16 -
2.3.1 X-band Low phase noise QVCO with back-gate transformer feedback - 16-
2.3.2 5.25GHz Low power VCO with drain-source Transformer feedback - 19 -
2.4 Measurement results and Discussions ..... - 21 –
2.4.1 Measurement consideration ..... - 21 -
Chapter 3 Low Voltage Multi-Band VCO and its Frequency Divider . - 30 -
3.1 Introduction ..... - 30 -
3.2 Circuit Design and Consideration ..... - 31 -
3.2.1 Volatage Controlled Oscillator ..... - 32 -
3.2.2 Divider ..... - 36 -
3.2.3 2-to-1 Multiplexer ..... - 38 -
3.3 Chip layout and simulatoin results ..... - 39 -
3.4 Measurement results and Discussions ..... - 47 -
Chapter 4 Conclusion and Future Work ..... - 54 -
4.1 Conclusion ..... - 54 -
4.2 Future Work ..... - 55 -
Appendix CMOS Low Noise Amplifier for UWB system ..... - 56 -

A.1 Introduction ..... - 56 -
A.2 Design Consideration ..... - 62 -
A.2.1 Wideband matching technique ..... - 62 -
A.2.2 Ultra Wide-band Low-Noise Amplifier ..... - 64 -
A.3 Chip implementation and Measured results ..... - 66 -
A.4 Discussion and Conclusions ..... - 76 -
Reference ..... - 78 -

LIST OF TABLE

Table 1-1 Wireless communication system characteristc 2

Table 2-1~2 QVCO performance in different corner conditions 18

Table 2-3~4 VCO performance in different corner conditions 21

Table 2-5 Performance summary of the TF-QVCO 25

Table 2-6 Comparison of TF-QVCO 26

Table 2-7 Performance summary of the TF-VCO 29

Table 2-8 Comparison of TF-VCO 29

Table 3-1 Power consumption of each block 40

Table 3-2 Summary performance of the carrier frequencies 46

Table 3-3~6 VCO corner simulation 46

Table 3-7 K_{VCO} comparison between the simulation and measurement 48

Table 3-8 Measurement of output power and phase noise performance.....50

Table 3-9 Performance summary of the multi-band VCO 53

Table 3-10 Comparison with the multi-band VCOs 53

Table 3-7 K_{VCO} comparison between the simulation and measurement 48

Table 3-8 Measurement of output power and phase noise performance.....50

Table 3-9 Performance summary of the multi-band VCO 53

Table 3-10 Comparison with the multi-band VCOs 53

Table A-1 Performance summary of Ultra-wideband LNA 75

Table A-2 The comparisons of this work and recent LNA papers. 76

LIST OF FIGURE

Figure 1-1 DS-UWB spectrum allocation....2
Figure 1-2 Multi-band spectrum allocation....3
Figure 2-1 Differential VCOs with transformer feedback....4
Figure 2-2 Proposed architecture of TFQVCO....5
Figure 2-3 Two interleaved VCO configuration....6
Figure 2-4 The primary and secondary self-inductances....7
Figure 2-5 The lumped model of the MOS varactor....8
Figure 2-6 The Proposed TF-VCO....9
Figure 2-7 Half circuits (a) Colpitts (b) TF-VCO....12
Figure 2-8 *I-V* characteristics of the MOSFET with and without FBB....14
Figure 2-9 Simulated Vth and drain current of the MOSFET with FBB....14
Figure 2-10 The primary and secondary self-inductances....15
Figure 2-11 The drain and source voltage waveform....16
Figure 2-12 The Chip layout....17
Figure 2-13 The frequency tuning range....17
Figure 2-14 The phase noise....18
Figure 2-15 The chip layout....19
Figure 2-16~17 The phase noise and the tuning range....20
Figure 2-18 The measurement equipment....22
Figure 2-19 Chip Photograph....23
Figure 2-20~22 The measured tuning range and phase noise and spectrum....24
Figure 2-23 The Chip photograph....26
Figure 2-24~26 The measured tuning range and phase noise and spectrum....28
Figure 2-27 Transformer topology....30
Figure 3-1 Forecast of the CMOS supply voltage by ITRS....31
Figure 3-2 Frequency allocation of MB-OFDM proposal....31
Figure 3-3 Architecture of this circuit....32
Figure 3-4 Schematic of the proposed VCO with switched capacitor array....33
Figure 3-5 Simplified half-circuit model of the proposed VCO....33
Figure 3-6 The drain and source voltage waveform....35
Figure 3-7~8 Block diagram and shcematic of the CML frequency dividers....37
Figure 3-9 Schematic and gain of multiplexer....39
Figure 3-10 The chip layout....34
Figure 3-11~12 Tuning range curves of different banks and switching time....41
Figure 3-13~14 Output waveform and phase noise of 7.92GHz....42
Figure 3-15~16 Output waveform and phase noise of 7.392GHz....43

Figure 3-17~18 Output waveform and phase noise of 6.864GHz 44
Figure 3-19~20 Output waveform and phase noise of 6.336GHz 45
Figure 3-21 Chip photograph 47
Figure 3-22 Measured tuning range curves with different banks 48
Figure 3-23 Measurement of output power and phase noise 50
Figure 3-24 Output power of the carrier frequency 51
Figure 3-26 Maximal frequency in the locking range of the divider 52
Figure 4-1 Revised architecture of back gate TF-QVCO 55
Figure A-1 Basic input matching topology 57
Figure A-2 Basic four single-end distributed amplifier 58
Figure A-3 Narrowband LNA topology. 59
Figure A-4 Fourth-order bandpass ladder filter used for impedance matching 59
Figure A-5 Configuration of a common-gate input stage 60
Figure A-6 The small signal equivalent circuit of common-source with inductive source degeneration 61
Figure A-7 The small signal equivalent circuit of source degeneration 62
Figure A-8 The equivalent small signal circuit of resistive loading 62
Figure A-9 The equivalent small signal circuit of capacitive loading 63
Figure A-10 The equivalent circuit of input impedance 64
Figure A-11 The schematic of the proposed UWB LNA 65
Figure A-12 The equivalent circuit of first stage UWB LNA 65
Figure A-13 (a) the chip layout (b) the chip photograph 67
Figure A-14 Measurement setups 69
Figure A-15 (a) Power gain vs. Frequency(b) Isolation vs. Frequency(c) Input return loss coefficient vs. Frequency(d) Output return loss coefficient vs. Frequency 71
Figure A-16 Noise Figure vs. Frequency 72
Figure A-17 (a)~(c) P1db at 3,6,9 GHz 73
Figure A-18 (a)~(c) IIP3 at 3,6,9 GHz 75
Figure A-19 (a)The modified S21 simulation(b) The modified NF simulation 77

Chapter 1 Introduction

1.1 Background and motivation

The continuous growth of personal wireless communications demands low-cost low-power in the design of wireless systems. Wireless transceivers for many standards, including GSM, Bluetooth, WLAN, and Wireless Personal Area Network (WPAN) require low-power design techniques to enhance their battery lifetime and to improve their portability. Having being aggressively scaled down, CMOS becomes an attractive process choice to implement low-cost integrated transceiver systems.

Due to the flexibility, the demand for high-speed data transmission is increasing, such as real-time video and wireless USB. But according to Table 1-1, most wireless communication systems support the data rate up to a few tens megabits per second only. For the personal short-range use, Bluetooth is very popular and able to integrate several wireless devices. However, there is a disadvantage of Bluetooth: poor data rate (1Mbps). In other words, longer time is inevitable when a lot of data are accessed or different wireless devices work simultaneously. In order to raise the data rate, Ultra Wide-Band (UWB) can be a solution.

In 2002, the Federal Communications Commission (FCC) has allocated 7500-MHz of spectrum for ultra-wideband (UWB) applications in the 3.1–10.6 GHz frequency range [1]. There are two mainly modulation technologies for UWB communications：Direct sequence code division multiple access (DS-CDMA) and multi-band orthogonal frequency division multiple access (MB-OFDM).

Table 1-1 Wireless communication system characteristc

System	Cellular phone	WLAN		WPAN	
	WCDMA	802.11 b/g	802.11 a	Bluetooth	UWB
Frequency (GHz)	1.92~1.98 2.11~2.17	2.4~2.4835	5.15~5.35	2.4~2.48	3.1~10.6
Modulation	QPSK	QPSK/OFDM	OFDM	GFSK	DSSS/QPSK
Channel Bandwith	5 MHz	20 MHz	20 MHz	1 MHz	528 MHz
Date Rate (bit/sec)	384 k/ 2 M	11/54 M	54 M	1 M	110/ 480 M

DS-CDMA uses a sequence of Gaussian monocycle pulses which their spectrum is spread as in Fig. 1-1. The lower band occupies the spectrum from 3.1-4.85GHz and the upper band occupies the spectrum from 6.2-9.7GHz [2]. The 5-6GHz band is dedicated to WLAN 802.11a systems.

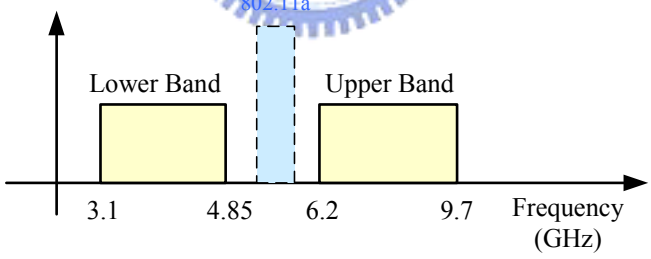


Figure 1-1 DS-UWB spectrum allocation

In Multi-Band-OFDM (MB-OFDM) UWB, frequency span is grouped into 5 major Band Groups which are in turn sub-divided into 14 bands in total, as shown in Fig. 1-2. Each band is 528MHz bandwidth [3].

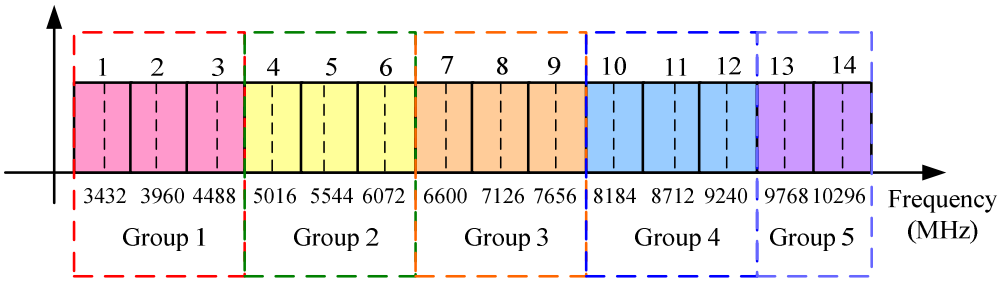


Figure 1-2 Multi-band spectrum allocation

1.2 Thesis organization

In this thesis, three voltage-control oscillators for X-band, WLAN 802.11a, Multi-band operation and an Ultra-wideband Low noise amplifier are realized in TSMC RF 1P6M 0.18 μm CMOS technology.

Chapter 2 will include two kinds of transformer feedback techniques in two voltage-controlled oscillators separately. One of this is to achieve higher oscillating frequency and the other is for ultra-low power operation.

Chapter 3 will introduce a multi-band voltage-controlled oscillator and its frequency divider. The characteristic of wide tuning range under low voltage operation covers some group of MB-OFDM UWB system. Both the simulation and the measurement results are further discussed.

Chapter 4 will give some discussions of these circuits to compare the simulation and measurement results. Besides, the future work will be mentioned to propose the possible improvement.

Finally, appendix will present the design and implementation of 3.1~10.6 GHz UWB LNA. In this chapter we study the input matching technique.

Chapter 2

CMOS Voltage-Controlled Oscillator with transformer feedback

2.1 Introduction

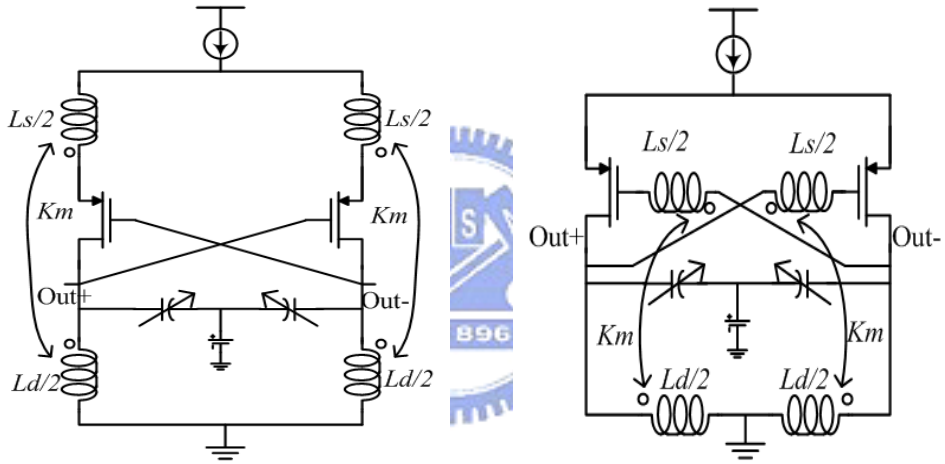


Fig. 2-1 Differential VCOs with (a) transformer feedback to the source and (b) transformer feedback to the front gate

As shown in Fig. 2-1(a), the drain terminal is magnetically feedback to source terminal with an impedance transformation of n^2/g_m, where n is the transformer turns-ratio and g_m is the transconductance of the transistor [4][5]. Since the impedance seen at the source terminal is $1/g_m$, a relatively high turns-ratio is required for the transformer to make an impedance transformation, thereby entailing complexity in transformer design, making it possible to lower the oscillation frequency.

If we feedback the drain voltage to the front-gate like Fig. 2-1(b). Since the impedance seen at the gate of the switching transistor is relatively high, the turns-ratio

of the transformer can be optimized with a smaller number of turns. However, the parasitic capacitances of the transformer directly couple to the tank, and lower the oscillation frequency significantly.

2.2 Circuit Design Consideration

2.2.1 X-band Low phase noise QVCO with back-gate transformer feedback

A. Transformer Feedback to the Back-gate

To obtain both higher frequency and simplify the transformer design (small number of turns ratio), the front-gate feedback path can be modified to have a feedback to the back-gate as shown in Fig. 2-2.

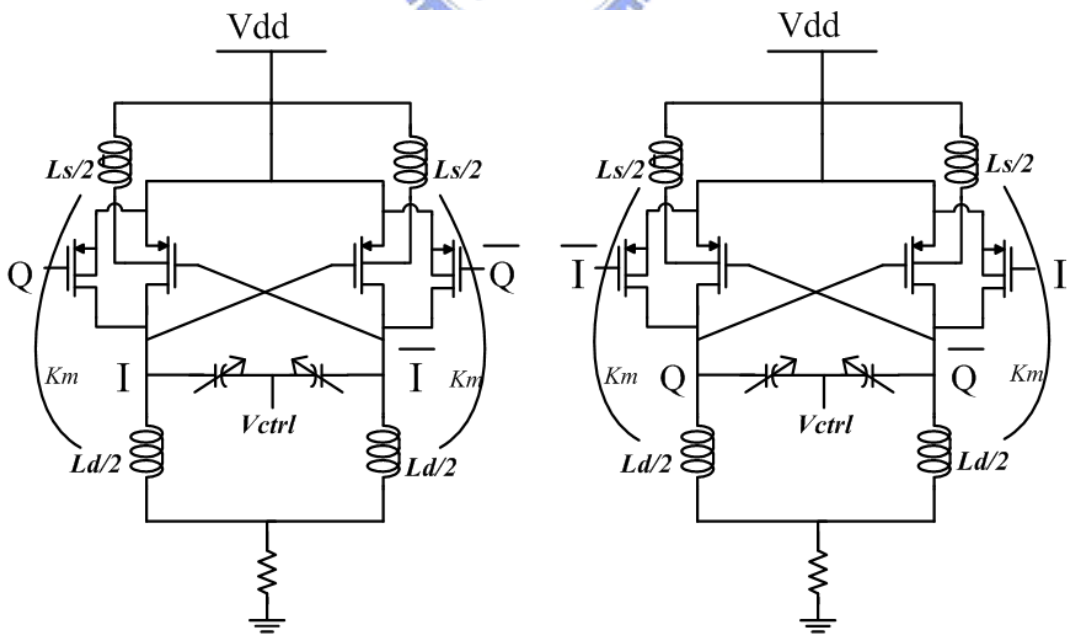


Fig. 2-2 Proposed architecture of TFQVCO

B. Harmonic Filtering Resistor

Because the current source is the main contributor to the phase noise, the current source is replaced by resistor providing bias condition and wide-band operation, it can suppress not only second harmonic but also all the other harmonics [6]. The thermal noise of the resistor will be up converted into $1/f^2$ phase noise by the switching transistors. So there is a tradeoff between the harmonic filtering and its thermal noise contribution. As we increase the resistance, the $1/f^2$ phase noise performance will reach its optimum value and begin to degrade in the same way. This is because the thermal noise contribution overwhelms the phase noise reduction by the harmonic filtering. In this design, R=170Ω is selected.

C. Quadrature Generation

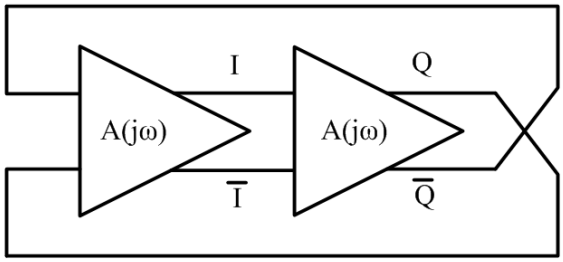


Fig. 2-3 Two interleaved VCO configuration

There are several ways to obtain quadrature signals: RC poly-phase filters, divider-by-2 circuit, and two interleaved voltage-controlled oscillators. RC poly-phase filters attenuate the signal and increase the effective capacitance of the tank. A lot of chip area is needed for a good matching of the filters. The divider-by-2 circuit needs and oscillator operating at 2 times higher than the desired frequency and a high-speed frequency. Both circuits dissipate a lot of power. For the low power consumption and quadrature phase accuracy, two interleaved VCO configuration is adopted as shown in Fig. 2-3.

With parallel coupling transistor to generate the I-Q phase. From the Barkhausen

criterion, oscillation only occurs when the loop gain is $[A(j\omega)]^4=1$, which means $A(j\omega)=1\angle 90^o$ [7]. Therefore, this configuration provides quadrature-phase signals from the four outputs of these two proposed VCOs.

The all-PMOS topology is preferred since PMOS has lower corner frequency of flicker noise, which means less low frequency noise [8].

D. Transformer Design

A 2-μm-thick top AlCu metal is used for the windings to increase the quality factor. The transformer is designed with 1-μm line spacing, 150-μm outer dimension. Besides, the quality factor of transformer can be optimized by increasing the metal width progressively from the inner to the outer turn [5][9]. As such, the series loss in the outer turn is reduced while its substrate loss associated with the wider metal width does not degrade the performance due to the virtual ground at the inductor's center tap. Fig. 2-4(a) shows the transformer is simulated by ADS Momentum with primary inductance (L_d) 0.46nH, and the secondary inductance (L_s) 0.13nH, with quality factors 6.8 and 4.4 respectively. The transformer coupling coefficient k_m is modeled as shown in Fig. 2-4(b), which is calculated by Eq. (2-1) as 0.4 [10].

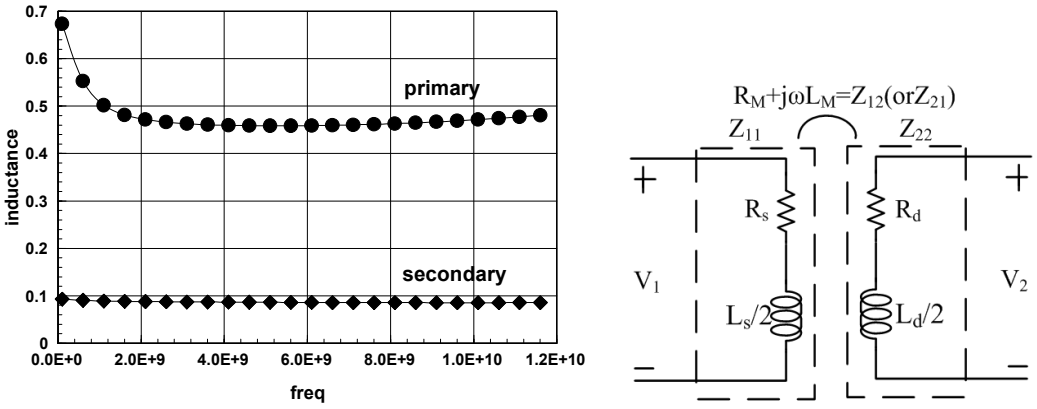


Fig. 2-4 (a) The primary and secondary self-inductances (b) Transformer lump model

$$K_{im} = \frac{\mathrm{Im}(Z_{12})}{\sqrt{\mathrm{Im}(Z_{11})\,\mathrm{Im}(Z_{22})}} = \frac{L_M}{\sqrt{L_s/2 \times L_d/2}} \tag{2-1}$$

MOS varactors are used to provide the frequency tuning capability. AM noise originating from the upconversion of low frequency noise cannot be neglected due to AM-PM conversion through the varactors. So the frequency tuning capability will be controlled as varactor's selectivity and traded for lower phase noise [11]. The accumulation-mode MOS varactor is adopted in one group with 10 fingers.

The equivalent capacitance Ceq is about 42~122 fF and its equivalent lumped model is shown as in Fig. 2-5.

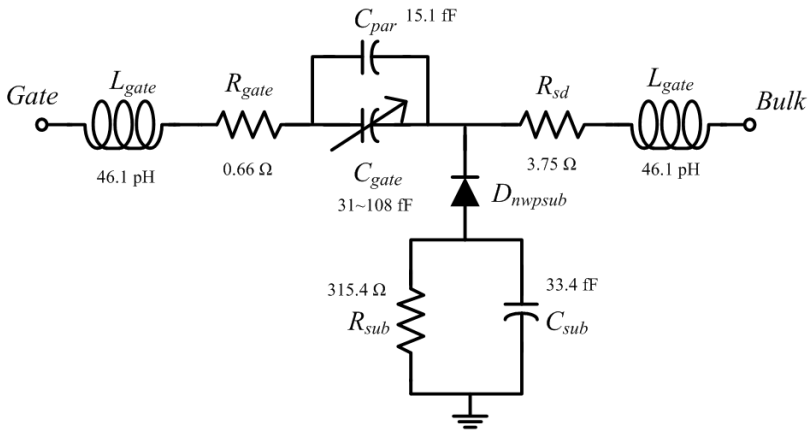
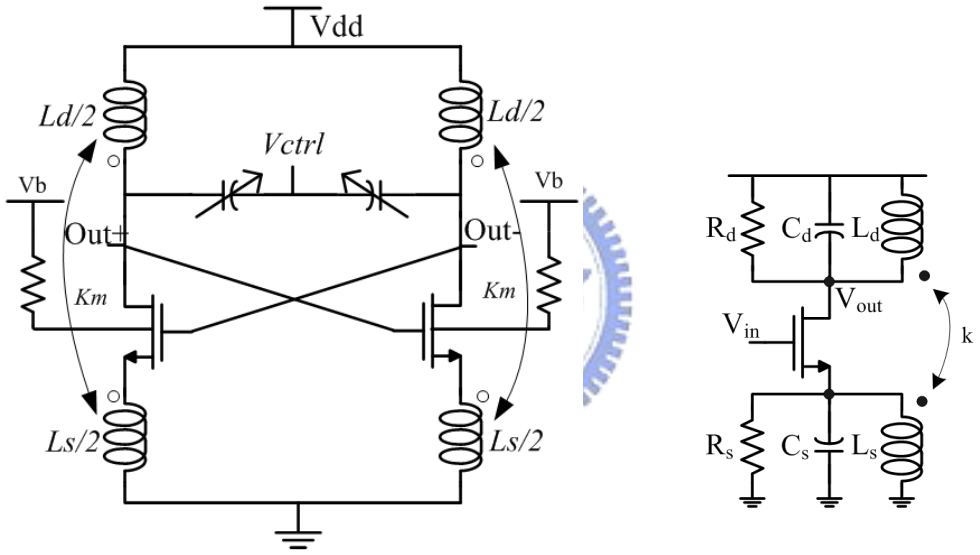


Fig. 2-5 The lumped model of the MOS varactor

2.2.2 5.25 GHz Low power VCO with drain-source Transformer feedback

The continuous growth of personal wireless communication demands low-cost low-power solutions in the design of wireless system. Low-voltage operation may save the power consumption of the analog as long as the total bias current does not need to be increased to maintain the same performance. Low voltage, however, limits the signal amplitude, which in turn limits the signal-to-noise ratio and degrades system performance.



(a) (b)

Fig. 2-6 The Proposed (b) TF-VCO and its (b) half circuit

To improve the VCO performance in terms of low supply voltage, low power, and low phase noise, a TF-VCO is proposed to provide extra voltage swings, improved loaded quality factor, minimum noise-to-phase-noise transfer [5] as shown in Fig. 2-6.

A. Enhanced voltage swings

The main limitation of the signal amplitude is overcome by the concept of dual signal swing, which enables the output signals to swing above the supply voltage and

below the ground potential with transformer feedback to increase the carrier power. Besides, the drain and source signal oscillate in phase to enhanced the swing amplitude. For an ideal coupling factor k=1, the source signal amplitude $V_{s,p}$ is related to the drain signal amplitude $V_{d,p}$ by $V_{s,p}=V_{d,p}/K_L$ for $K_L=L_d/L_s$ and the maximum peak-to-peak oscillation amplitude at the drain would be increased to $2.V_{DD}(1+1/K_L)$

B. Improved loaded quality factor

The TF-VCO could also be analyzed by the half circuit VCO's transfer function. In Fig. 2-6(b), the tanks at the source and the drain are modeled by two *RLC* networks with a magnetic coupling coefficient k between Ld and Ls. For simplicity, the coupling coefficient k is assumed to be unity for now.

Defining $K_L=L_d/L_s$, $K_C=C_d/C_s$, $R_d=Q_d.\omega.L_d$ and $R_s=Q_s.\omega.(L_d/K_L)$ with Q_d and Q_s being the parallel quality factors of L_d and L_s, respectively, and ω being the angular frequency.

$$\frac{V_{out}}{V_{in}}=\frac{sg_m\left(L_d+L_s-2\sqrt{L_dL_s}\right)}{s\left(\sqrt{\frac{L_s}{L_d}}-1\right)\left[\frac{1+sR_sC_s}{R_s}L_s+\frac{1+sR_dC_d}{R_d}L_d\right]+sg_mL_s\left(\sqrt{\frac{L_d}{L_s}}+\sqrt{\frac{L_s}{L_d}}-2\right)+\sqrt{\frac{L_s}{L_d}}-1}$$

$$=\frac{sg_mL_d\left(\frac{K_L+1-2\sqrt{K_L}}{\sqrt{K_L}(1-\sqrt{K_L})}\right)}{s^2L_dC_d(1+\frac{1}{K_LK_c})+s\left[g_mL_d(\frac{K_L+1-2\sqrt{K_L}}{K_L(1-\sqrt{K_L})})+\frac{1}{\omega}\frac{Q_d+Q_s}{Q_dQ_s}\right]+1} \quad (2\text{-}2)$$

The oscillation frequency of the half-circuit VCO is determined by definition as the transfer function V_{out}/V_{in} having a magnitude of unity and a phase shift of 180^o, which corresponds to a unity loop gain with a zero phase shift for the closed loop. By solving (2-2), the oscillation frequency of TF-VCO is

$$\omega_o = \frac{1}{L_d C_d} \frac{1}{1+\frac{1}{K_L K_C}} \approx \frac{1}{L_d C_d} \tag{2-3}$$

where the approximation is a valid assumption because the resonant frequency of the tank at the source is much larger than that of the tank at the drain.

An important parameter is the loaded quality factor Q_{loaded} of the tank circuit, which is defined as the Q factor of the second-order transfer function V_{out}/V_{in}. From (2-2), the quality factor is given by

$$Q_{loaded} = \left[\frac{1}{Q_d} \left(1 - g_m R_d \frac{1+K_L-2\sqrt{K_L}}{K_L(1-\sqrt{K_L})} \right) + \frac{1}{Q_s} \right]^{-1} \tag{2-4}$$

which indicates the loaded quality factor increases as g_m increase. The term $(1+K_L-2\sqrt{K_L}) / K_L(1-\sqrt{K_L})$ could be optimized with a maximum value of 1/4. Because the resonant frequency of the secondary tank $\omega_{resonance}$ of the TF-VCO is far above the oscillation frequency ω_o, the unloaded parallel quality factor $Q_{parallel}$ of the secondary inductor at ω_o is

$$Q_{parallel} = Q_{series} \times \left(\frac{\omega_{resonance}}{\omega_o} \right)^2 \tag{2-5}$$

and thus $Q_s >> Q_d$ and (2-4) could be approximated as

$$Q_{loaded} \approx Q_d \frac{4}{4 - g_m R_d} \tag{2-6}$$

C. Minimum noise-to phase-noise transfer

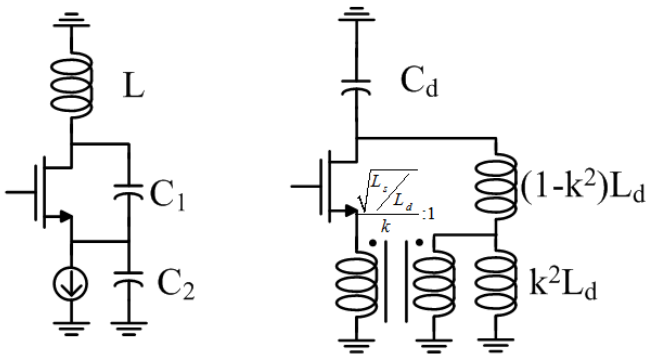


Fig. 2-7 Half circuits (a) Colpitts (b) TF-VCO

Fig.2-7 shows a comparison between a common-gate Colpitts VCO and the half-circuit TF-VCO, where the transformer is represented by an equivalent model. For the Colpitts oscillator, the capacitors C_1 and C_2 form the feedback network of the total tank capacitance and thus limit the maximum achievable *L/C* ratio. This contradicts the requirements for high tank quality factor and high tank impedance, and thus the Colpitts VCO is not favorable for low-power VCO design. The TF-VCO, on the other hand, uses a single transformer for the feedback and does not impose extra capacitance to the tank circuit, which could be similar to the Hartley design.

Since the proposed VCO is operated under an ultra-low dc voltage, the cross-coupled transistors are potentially biased in the weak-inversion region. Therefore, the drain noise of the transistors is no longer dominated by the thermal noise as [12] , $\frac{i_{n,d}}{\Delta f} = 4kT\gamma g_{d0}$, where g_{d0} is the channel conductance with V_{GS}=0, and γ is the thermal noise coefficient. Instead, the drain noise is expressed as [13]

$$\frac{i_{n,d}}{\Delta f} = \frac{4kT\gamma g_{d0}}{1+\exp(-\frac{V_{GS}-V_t}{2mV_T})} + \frac{2qI_D}{1+\exp(\frac{V_{GS}-V_t}{2mV_T})} \qquad (2\text{-}7)$$

where I_D is the drain current, V_T is the thermal voltage, and m is the weak inversion slope factor. From (2-7), $i_{n,d}/\Delta f$ includes not only the contribution from the thermal noise, but also that of the shot noise since the drain current consists of both drift and

diffusion components as the gate overdrive V_{GS}-Vt approaches V_T.

Due to the fact that $2qI_D$ is generally greater than $4kT\gamma g_{d0}$ for low-power operation, the cross-coupled transistors may contribute more noise to the *LC* tank as the supply voltage decreases. Therefore, it imposes a fundamental limitation on the phase noise of the VCO for ultra-low-power and ultra-low-voltage applications.

D. Forward Body Bias

For deep-submicrometer MOSFETs, the threshold voltage V_t is no longer constant, but influenced by circuit parameters such as gate length, channel width, and drain-to source voltage due to the short-channel and narrow-channel effects. Typically, transistors with a large channel width and a minimum gate length exhibit a reduced V_t, which is preferable for low-voltage operations. In this VCO topology, the fundamental limitation on the supply voltage is imposed by the threshold voltage of the cross-coupled transistors. To further reduce the supply voltage, the FBB technique is adopted [14] as shown in Fig. 2-8.

For a MOSFET device, the threshold voltage is governed by the body effect as

$$Vt = V_{t0} + \left(\sqrt{2qN_A\varepsilon_s}\,/\,C_{ox}\right)\bullet\left(\sqrt{\left|2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right) \qquad (2\text{-}8)$$

Where V_{t0} is the threshold voltage for V_{SB}=0V, ϕ_F is a physical parameter with a typical value of 0.3V, N_A is the substrate doping, and ε_s is the permittivity of silicon. By applying a forward bias voltage to the body through a current-limiting resistor R_B, the effective threshold voltage is thus reduced while maintaining a minimum forward junction current between the body and the source terminals. The simulated effective threshold voltage and the drain current of a MOSFET with W=60 μm and L=0.18 μm are demonstrated in Fig. 2-8, indicating a threshold voltage reduction more than 80mV due to the FBB technique.

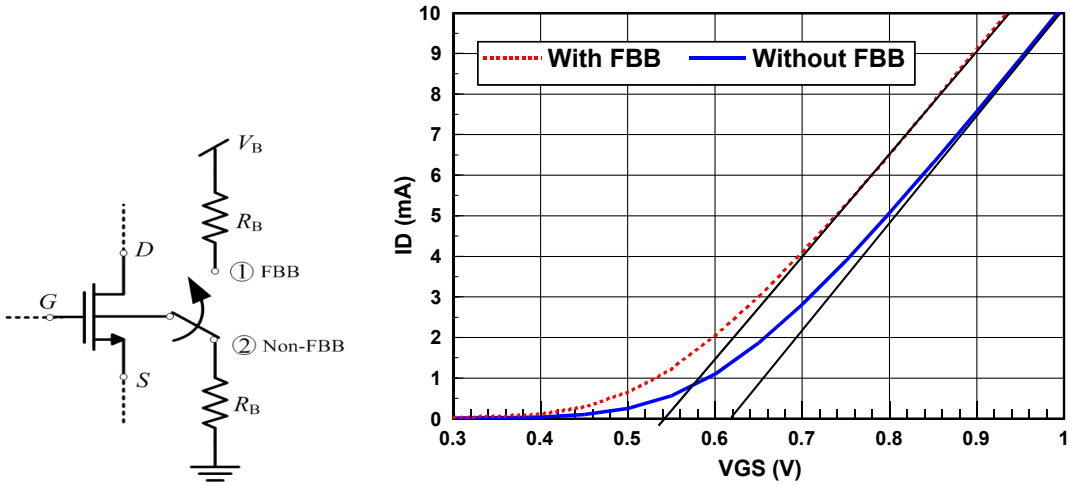


Fig. 2-8 *I-V* characteristics of the MOSFET with and without FBB

Besides, Fig. 2-9 shows the threshold voltage and its corresponding drain current under different forward body bias conditions.

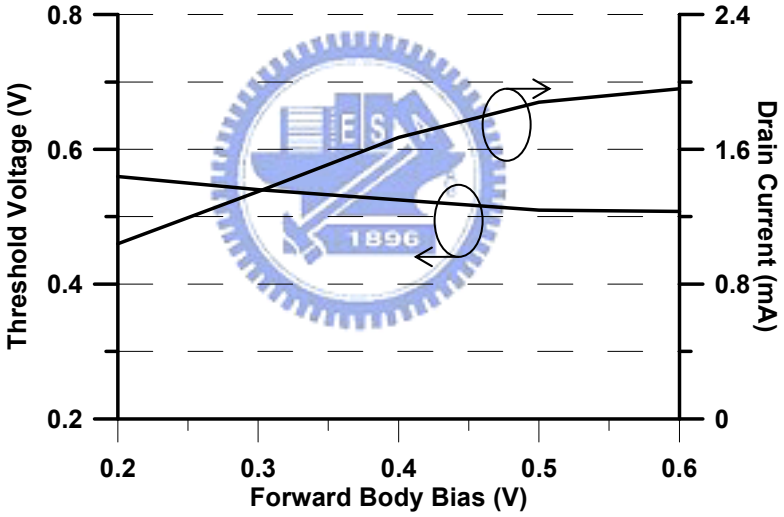


Fig. 2-9 Simulated threshold voltage and drain current of the MOSFET with FBB

E. Transformer Design

The design takes advantage of the higher mobility of the NMOS devices compared to PMOS and the higher quality factor of differential inductors over simple single-ended inductors for differential circuits with a deep n-well as the source-bulk isolation to the substrate. For differential inductors, the quality factor is improved by a factor of two, without special processing steps because the magnetic coupling between

the two coils ideally doubles the inductance value while the series loss is unchanged.

Fig. 2-10 shows the transformer is simulated by ADS Momentum with primary inductance (L_d) 0.786nH, and the secondary inductance (L_s) 0.221nH, with quality factors 7 and 5 respectively. The transformer coupling is calculated by Eq. (2-1) as 0.5 [10].

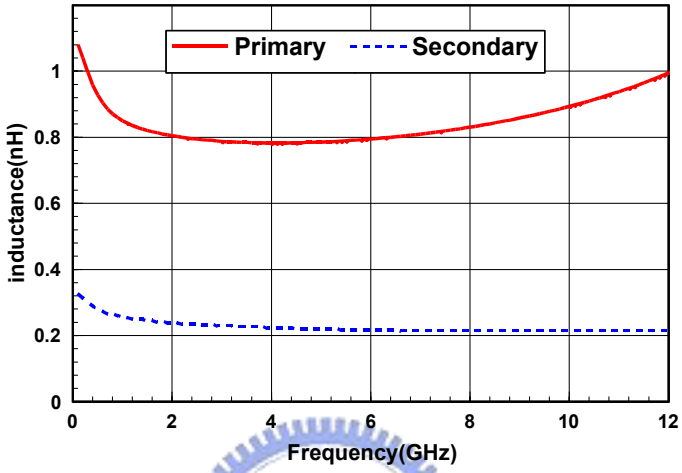
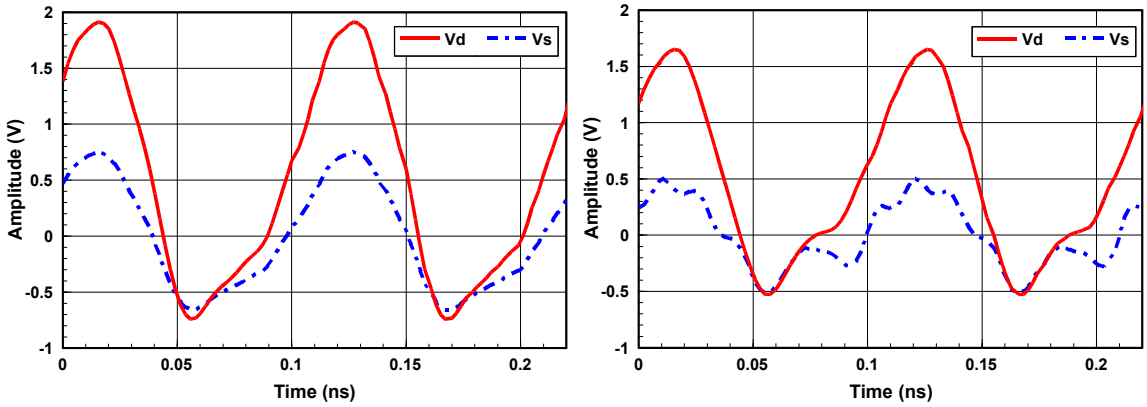
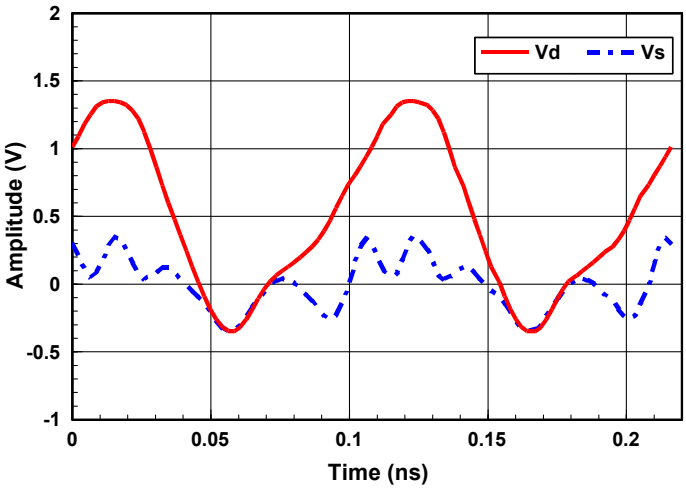


Fig. 2-10 The primary and secondary self-inductances

Fig. 2-11 shows the drain voltage swing under different coupling coefficient, which implies the actual carrier power is reduced for lower coupling coefficient, and the source voltage swing is no longer sinusoidal to help enhance the voltage swing. This will unavoidably degrade the phase noise.



(a) (b)



(c)

Fig. 2-11 The drain and source voltage waveform for (a) k=1 (b) k=0.75 (c) k=0.5

2.3 Chip Layout and Simulation Results

2.3.1 X-band Low phase noise QVCO with back-gate transformer feedback

Fig. 2-12 shows the layout designed and processed using TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip size is 0.88×0.49mm^2 including the pads. The simulation result shows the phase noise is about -114dBc/Hz at 1MHz offset in Fig. 2-13 and Fig. 2-14 shows the output frequency tuning range of the QVCO is around 800 MHz ranging from 8.9 to 9.7 GHz. The QVCO core circuit draws only 4.1mA from a 1.5-V supply.

The figure-of-merit (FOM) is expressed as [15].

$$FOM = 10\log[(\frac{\omega_0}{\Delta\omega})^2 \frac{1}{L\{\Delta\omega\} \times V_{DD} \times I_{DD}}] \quad (2\text{-}9)$$

where ω_0 is the center frequency, $\Delta\omega$ is the frequency offset, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$, V_{DD} is the supply voltage, and I_{DD} is the supply current. To further compare the performance of the proposed VCO, the power-frequency-normalized figure-of-merit (FOM) is used in (2-9) as -185.5@1MHz.

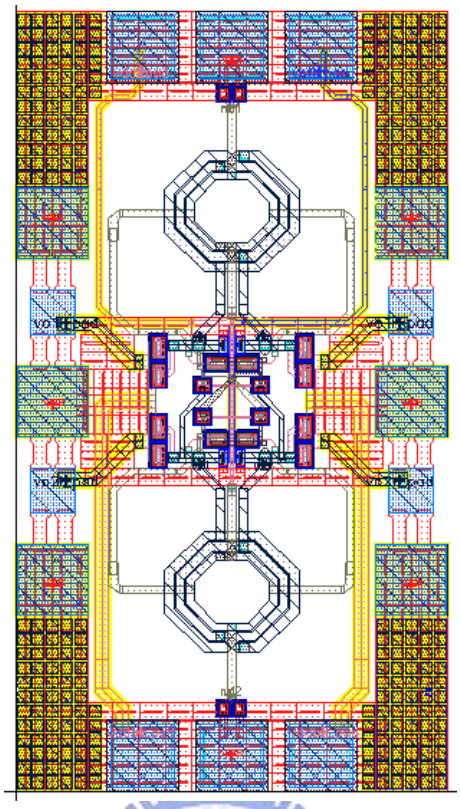


Fig. 2-12 The Chip layout

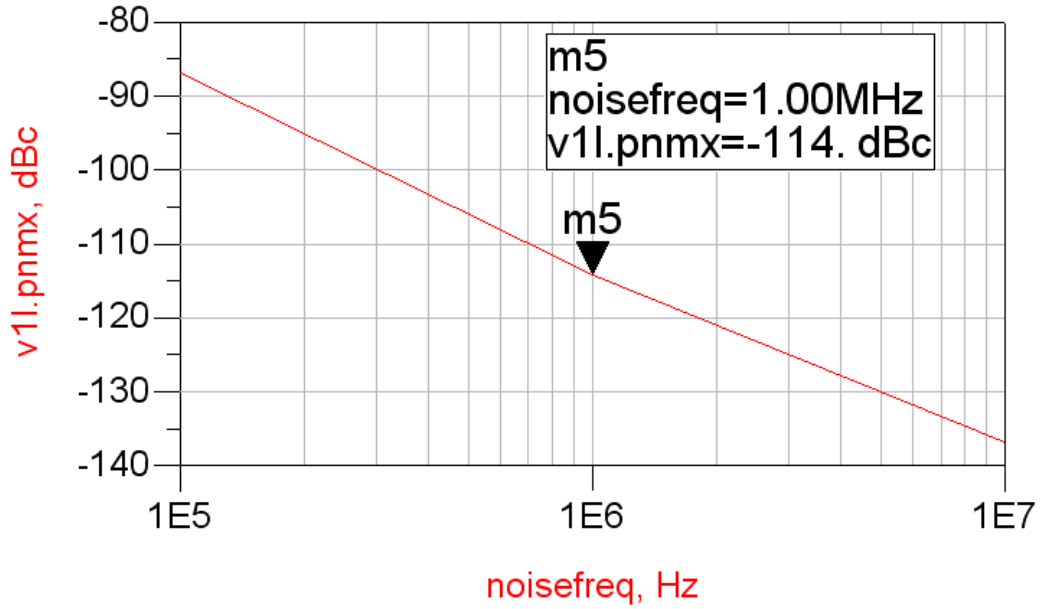


Fig. 2-13 The frequency tuning range

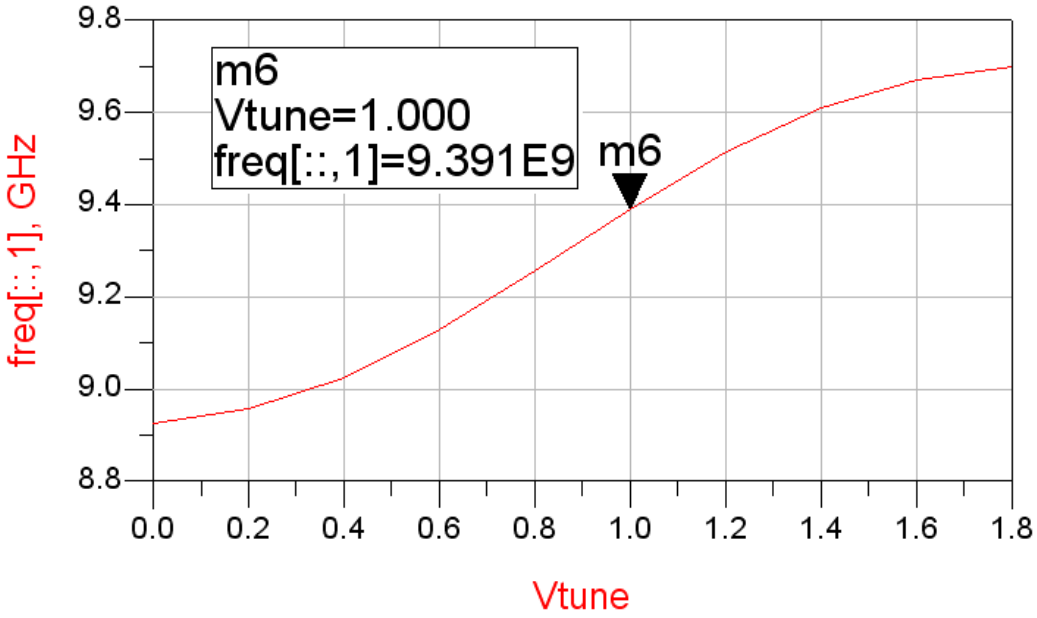


Fig. 2-14 The phase noise

Table 2-1 QVCO performance in different corner conditions

Corner	TT	FF	SS
Tuning Range	8.9~9.7GHz	9.05~9.8 GHz	8.8~9.65 GHz
Phase Noise@1MHz	-114dBc/Hz	-113dBc/Hz	-115dBc/Hz
Total Power	6.2+16.2mW	7.75+32.2mW	5.1+5.9mW
(with buffer)	22.4mW	39.95mW	11mW

Table 2-2 QVCO performance under different supply voltage

Supply Voltage	1.5V	1.65V	1.35V
Tuning Range	8.9~9.7 GHz	8.85~9.6 GHz	8.95~9.75 GHz
Phase Noise@1MHz	-114dBc/Hz	-114dBc/Hz	-113dBc/Hz
Total Power	6.2+16.2mW	8.1+30.5mW	4.6+5.6mW
(with buffer)	22.4mW	38.6mW	10.2mW

2.3.2 5.25 GHz Low power VCO with drain-source Transformer feedback

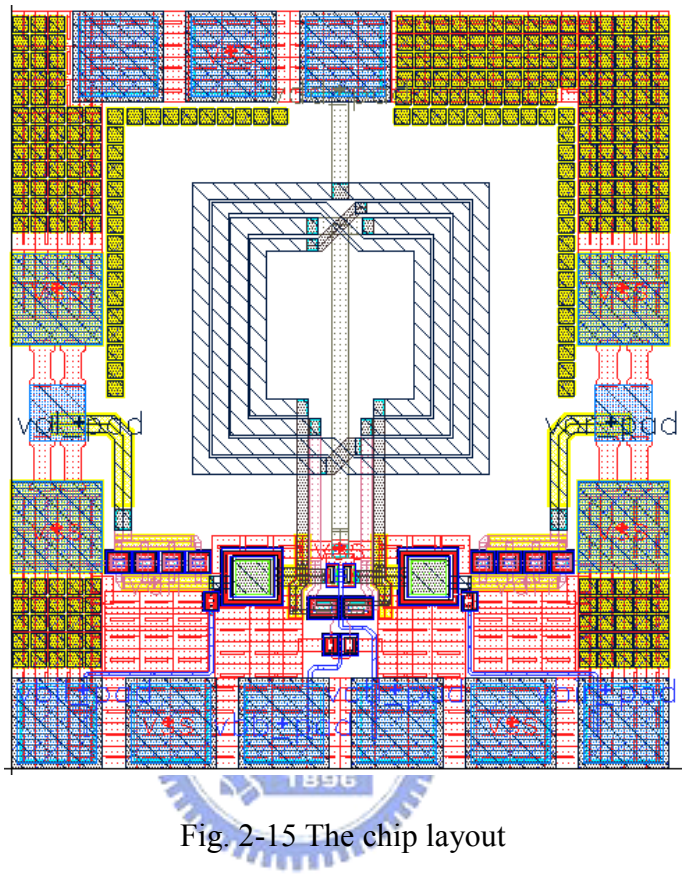


Fig. 2-15 The chip layout

Fig. 2-15 shows the layout designed and processed using TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip size is 0.66×0.58mm^2 including the pads. The simulation result shows the phase noise is about -113dBc/Hz at 1MHz offset in Fig. 2-16 and Fig. 2-17 shows the output frequency tuning range of the TF-VCO is around 310 MHz ranging from 5.05 to 5.36 GHz. The power dissipation of the TF-VCO core circuit draws only 0.57mW from a 0.5-V supply. The figure-of-merit (FOM) is about -192@1MHz.

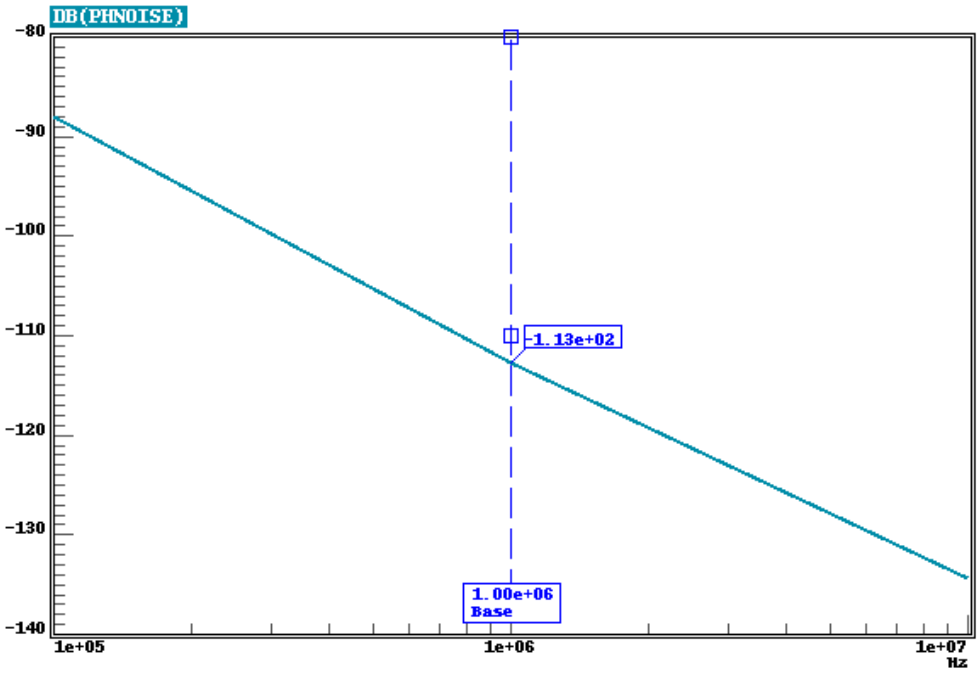


Fig. 2-16 The phase noise

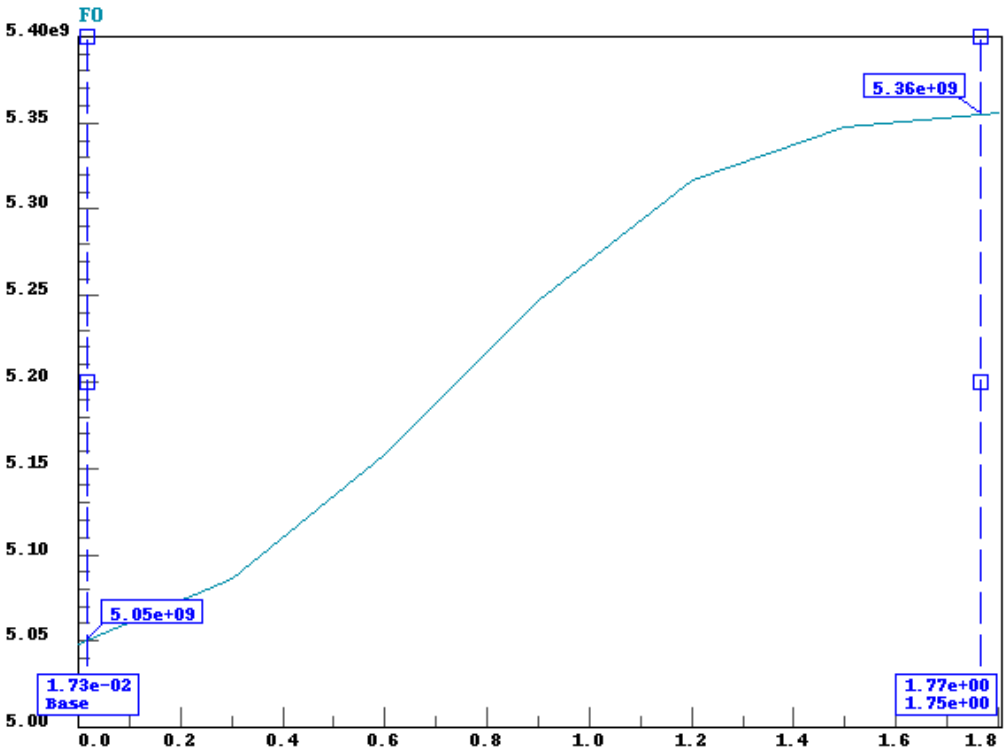


Fig. 2-17 The tuning noise

Table 2-3 VCO performance in different corner conditions

Corner	TT	FF	SS
Tuning Range	5.05~5.36GHz	5.08~5.38GHz	5.03~5.34GHz
Phase Noise@1MHz	-113	-115	-112
Core Power	0.6mW	1.1mW	0.4mW
Buffer Power	16.3mW	22mW	12mW

Table 2-4 VCO performance under different supply voltage

Supply Voltage	0.5V	0.55V	0.45V
Tuning Range	5.05~5.36GHz	5.03~5.35GHz	5.05~5.36GHz
Phase Noise@1MHz	-113	-114	-112
Core Power	0.6mW	1.2mW	0.46mW
Buffer Power	16.3mW	16.3mW	16.3mW

2.4 Measurement Results and Discussions

2.4.1 Measurement Consideration

The two voltage controlled oscillator are designed for on-wafer testing. Therefore the arrangement of each pad must satisfy rules of CIC's (Chip Implementation Center's) probe station testing rules. The measurement equipments contain Agilent E5052A signal source analyzer, E4407B spectrum analyzer, and E3615A DC power supply in Fig. 2-18.

(a)

(b)

(c)

Fig. 2-18 (a) Agilent E5052A signal source analyzer (b) E4407B spectrum analyzer

(c) E3615A DC power supply

A. X-band Low phase noise Quadrature CMOS VCO with back-gate transformer feedback

The chip photograph is shown in Fig. 2-19.

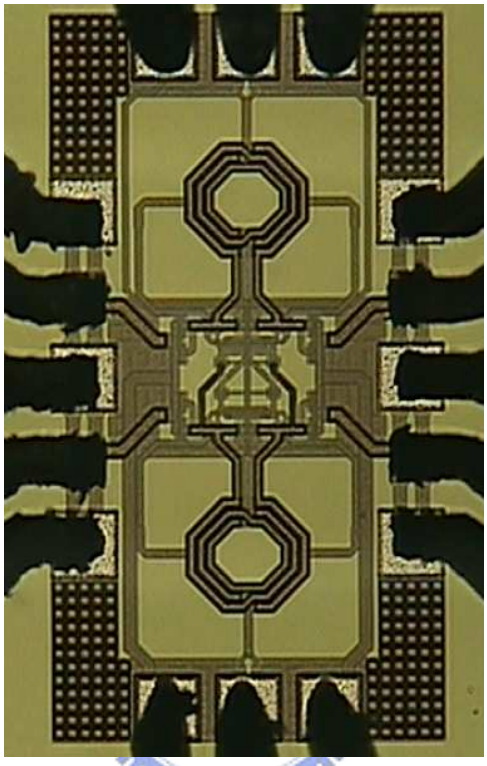


Fig. 2-19 Chip Photograph

According to Fig. 2-20 , the measured output frequency tuning range of the fabricated TF-QVCO is 470kHz ranging from 8.14 GHz to 8.61 GHz. Fig. 2-21 shows the phase noise of -113dBc/Hz at 1MHz offset when the frequency is 8.45GHz and the output spectrum is -6.5dBm as show in Fig. 2-22. The VCO core draws 4.2mA from 1.5V supply.

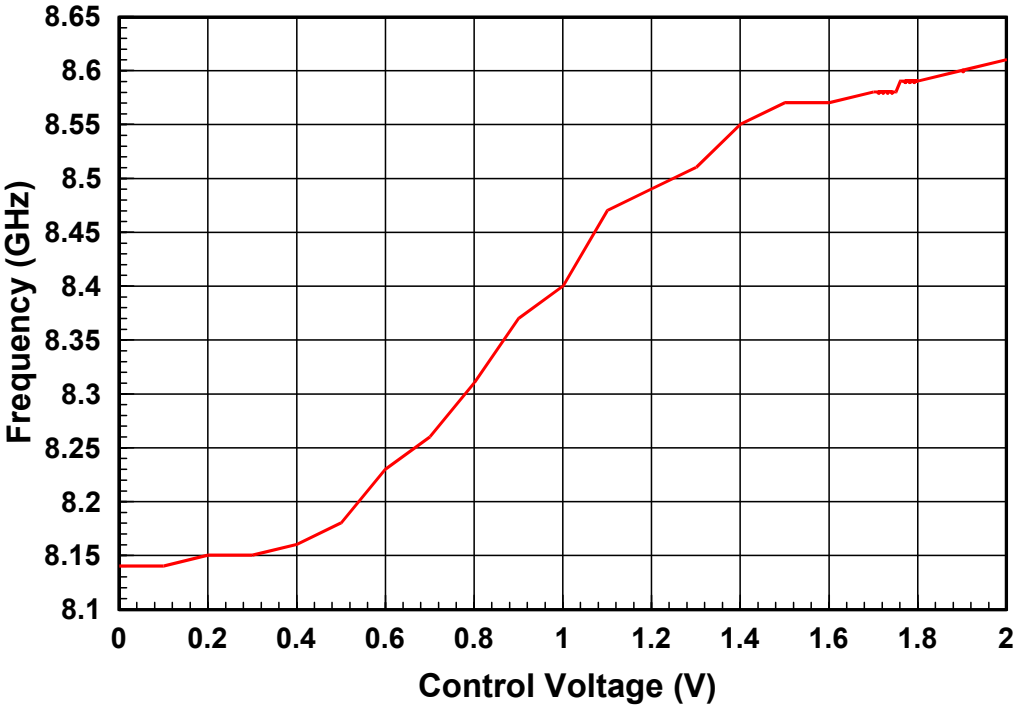


Fig. 2-20 The measured tuning range

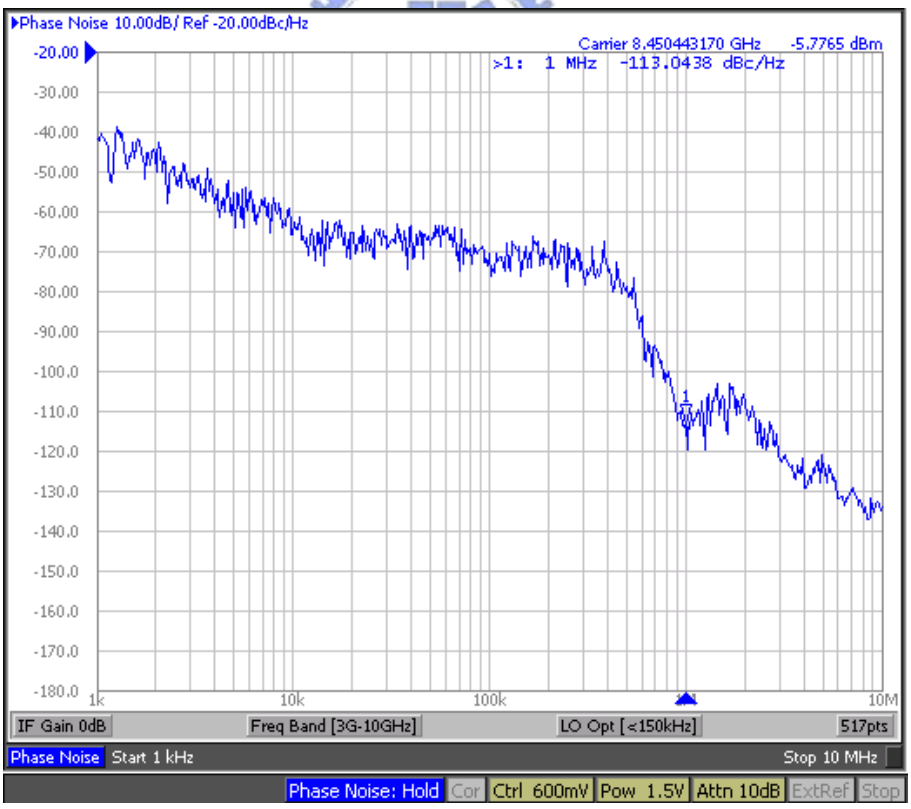


Fig. 2-21 The measure phase noise

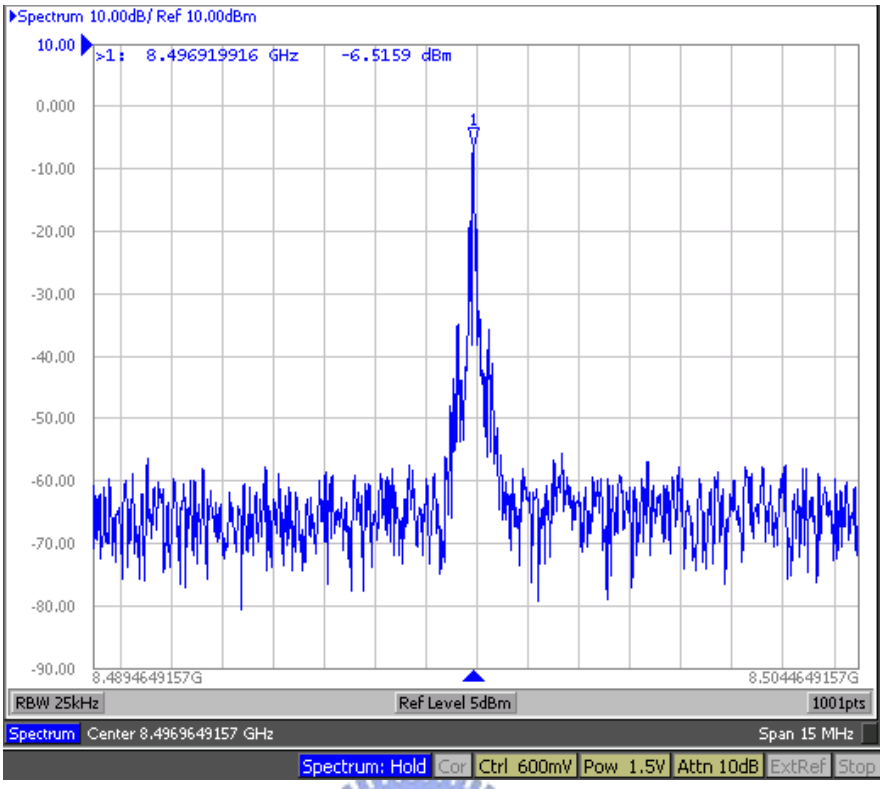


Fig. 2-22 The measure spectrum

Table 2-5 Performance summary of the TF-QVCO

Performance	Post-Simulation	Measurement
Supply Voltage	1.5V	
Tuning Range	8.9~9.7 GHz (9 %)	8.14~8.61 GHz
Phasenoise@1MHz	-114dBc/Hz	-113dBc/Hz
Power Consumption	22.4mW (VCO core 6.2mW)	21.1mW (VCO core 6.2mW)
Output Power	-3.2 dBm	-6.5 dBm
FOM	185.5	183.6

Table 2-6 Comparison of TF-QVCO

	This work	MWCL,2005 [4]	MWCL,2003 [16]
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS
Voltage	1.5V	1.8V	3V
Oscillation Frequency	8.4 GHz	11.22 GHz	8 GHz
Tuning Range	8.14~8.61 GHz	300MHz vtune from 1.6-2V	8.08~7.83GHz
	5.6%		3 %
Phase noise (dBc/Hz)	-113dBc/Hz	-109.4 @ 1MHz	-117 @ 1 MHz
Power Dissipation	6.2 mW	6.84 mW (vco core)	24 mW (vco core)
FOM	183.6	-181.8	-181.7

B. A Low-Power CMOS VCO with drain-source transformer feedback

The chip photograph is shown in Fig. 2-23.

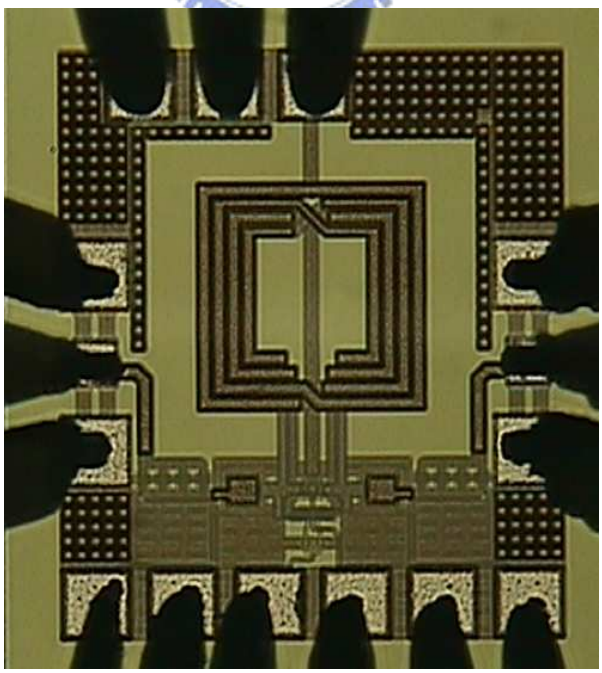


Fig. 2-23 Chip Photograph

According to Fig. 2-24 , the measured output frequency tuning range of the fabricated TFDSVCO is 290kHz ranging from 5.13 GHz to 5.42 GHz. Fig. 2-25 shows the phase noise of -114dBc/Hz at 1MHz offset when the frequency is 5.33GHz and the output spectrum is 1.62dBm as show in Fig. 2-26. The VCO core draws 1.2mA from 0.5V supply.

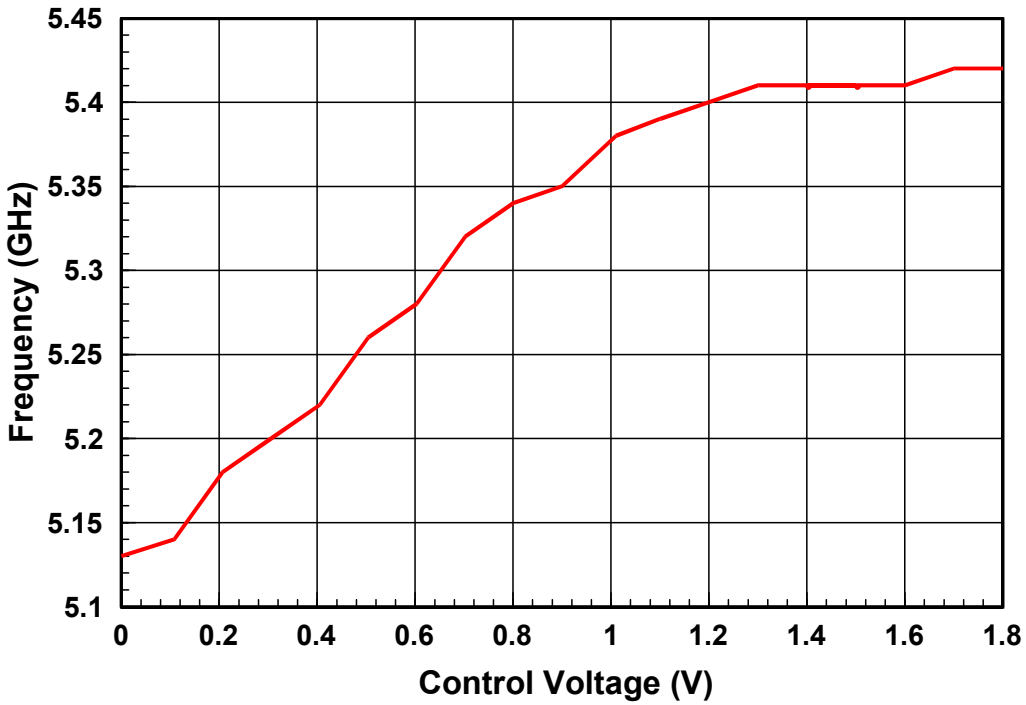


Fig. 2-24 The measured tuning range

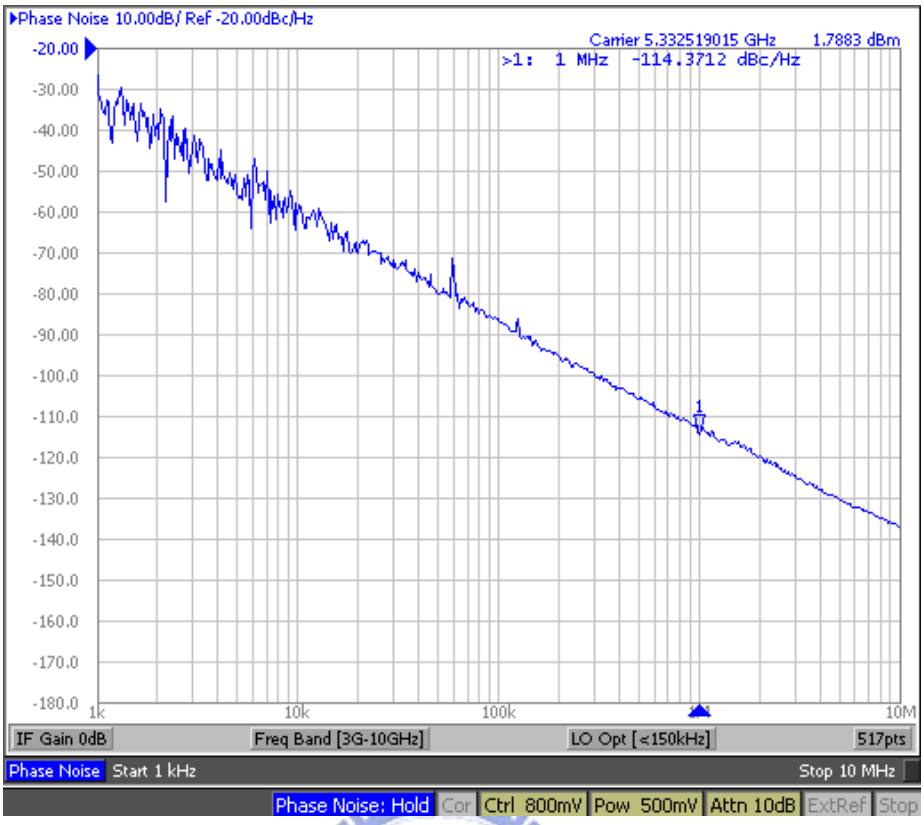


Fig. 2-25 The measure phase noise

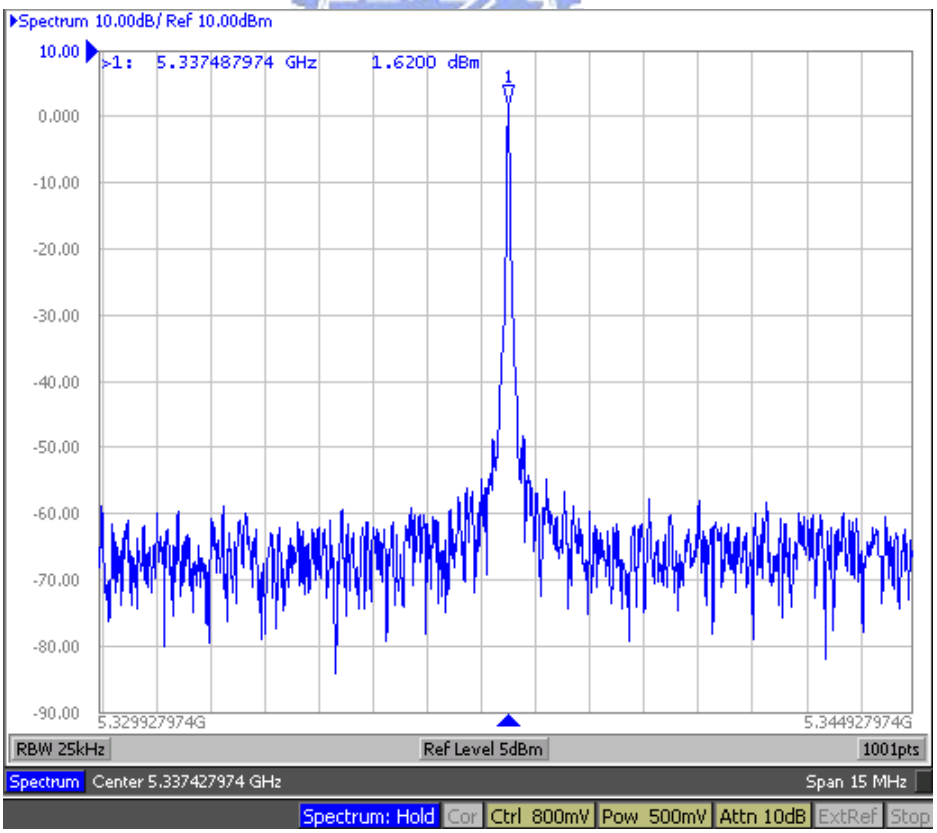


Fig. 2-26 The measure spectrum

Table 2-7 Performance summary of the TF-VCO

Performance	Post-Simulation	Measurement
Voltage	0.5V	0.5
Tuning Range	5.05~5.36GHz	5.13~5.42
Phase noise (dBc/Hz)	- 113@ 1 MHz	-114@1 MHz
Total Power Dissipation	0.6(vco core) +16.3mW(buffer)	0.6(vco core) +17mW(buffer)
FOM	192	193

Table 2-8 Comparison of TF-VCO

	This work (Measurement)	JSSCC, 2005 [5]	MTT, 2007 [14]
Technology	0.18um CMOS	0.18um CMOS	0.18um CMOS
Voltage	0.5V	0.5V	0.6V
Oscillation Frequency	5.25 GHz	3.8 GHz	5.6 GHz
Tuning Range	5.13~5.42 GHz	3.71~3.84 GHz	5.35 ~ 5.85 GHz
	5.5 %	8.4 %	8.1 %
Phase noise (dBc/Hz)	-114 @ 1 MHz	-119 @ 1 MHz	-118 @ 1 MHz
Total Power Dissipation	0.6 mW	0.57 mW	3 mW
FOM	-193	-193	-189

Chapter 3 Low Voltage Multi-Band VCO and its Frequency Divider

3.1 Introduction

Unfortunately, the inherently low transconductance of the MOSFETs at higher frequencies have impeded the evolution of low-power designs to RF front-ends. In addition to the power considerations, a reduced supply voltage is also an inevitable trend for CMOS designs as well. With the continuous shrinking in the transistor feature size, a proportional down-scaling of the supply is required to ensure the gate-oxide reliability [17].

The forecast of the supply voltage for CMOS circuits within the next decade [18] is shown in Fig. 3-1.

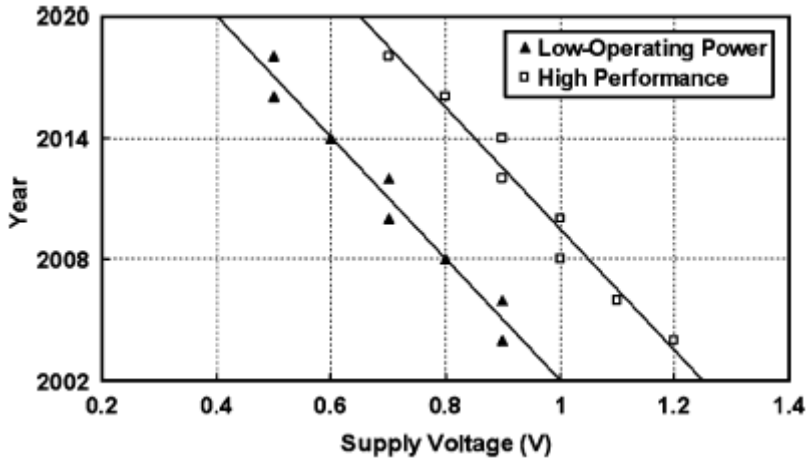
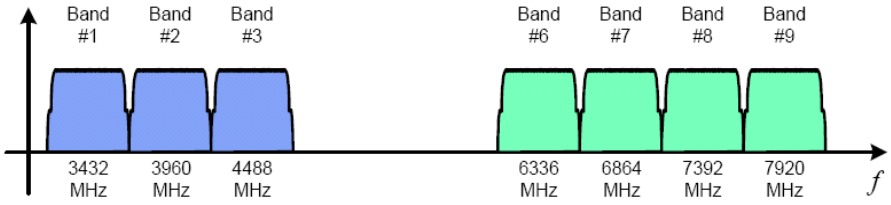


Fig. 3-1 Forecast of the CMOS supply voltage by ITRS [14]

3.2 Circuit Design Consideration



Frequency of operation for a Mode 2 device.

Fig. 3-2 Frequency allocation of MB-OFDM proposal.

In this work, Band 1, 2 and 6~9 are covered as shown in Fig. 3-2. Band Group 2 from 4752~5808 MHz causes interference with 802.11 a and Band Group 4,5 is reserved for future use. In order to meet such a specification, a VCO accompanied with a frequency divider is used to loosen the stringency, where the VCO provides carriers for Band 6~9 while the frequency divider is in charge of Band 1, 2. The multiplexer is also included to select where the output is from vco or divider. The architecture is shown in Fig. 3-3.

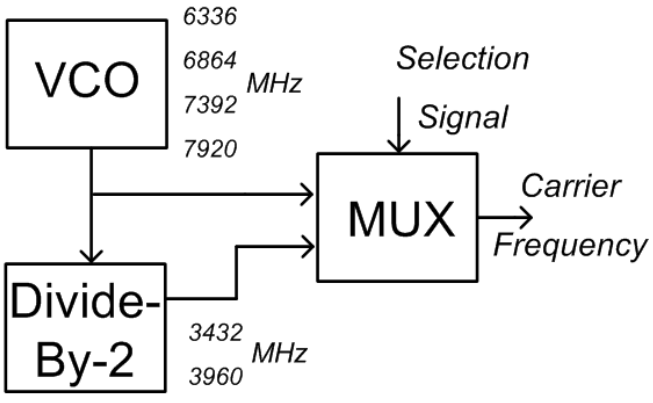


Fig. 3-3 Architecture of this circuit

3.2.1 Voltage-Controlled Oscillator

The schematic of the proposed VCO is shown Fig. 3-4. In order to reduce the required supply voltage and to eliminate additional noise contribution, the tail current transistor in a conventional cross-coupled VCO is replaced by on-chip inductors. For an enhanced voltage swing under a low supply voltage, the capacitive-feedback technique is employed [14]. Due to the use of the on-chip inductor and the feedback loop established by C_1 and C_2, the drain and source voltages can swing above the supply voltage and below the ground potential. Consequently, the output swing of the VCO is enhanced, leading to a superior close-in phase noise.

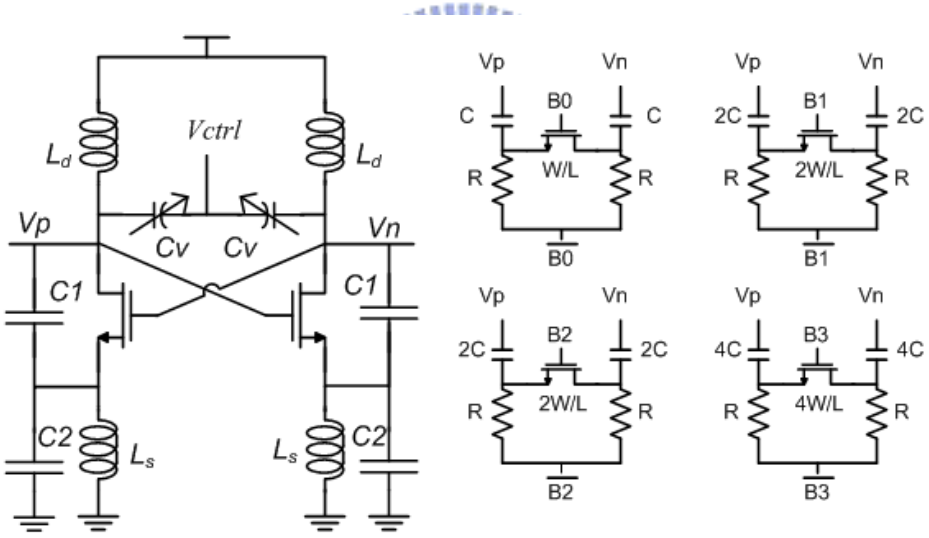


Fig. 3-4 Schematic of the proposed VCO with switched capacitor array

A. Startup Conditions

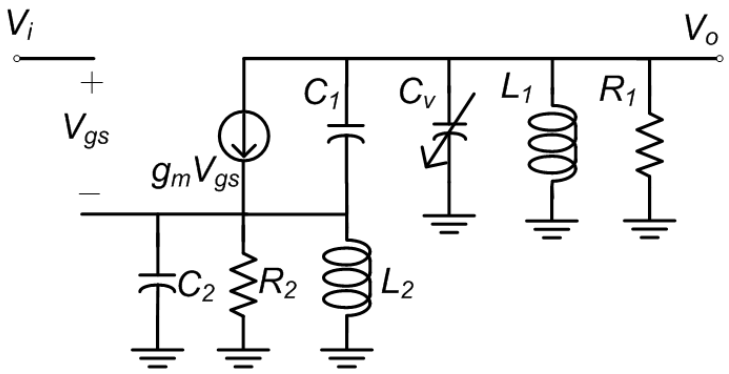


Fig. 3-5 Simplified half-circuit model of the proposed VCO

In order to derive the startup conditions and the oscillation frequency,the equivalent half-circuit of the VCO core is shown in Fig. 3-5, where R_1 and R_2 represent the losses of the on-chip inductors L_1 and L_2, respectively. In the equivalent circuit, the shunt resistance R_1 and R_2 can be estimated by

$$\begin{aligned} R_1 &= \omega^2 L_1^2 / R_{s1} \\ R_2 &= \omega^2 L_2^2 / R_{s2} \end{aligned} \tag{3-1}$$

where R_{s1} and R_{s2} are the equivalent series resistances of L_1 and L_2, respectively.

From the small-signal analysis, the transfer function between V_o and V_i is given by

$$\frac{V_o}{V_i} = \frac{-g_m\left(L_1L_2R_1R_2C_2s^2 + L_1L_2R_1s + L_1R_1R_2\right)s}{a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0} \tag{3-2}$$

where

$$\begin{aligned} a_0 &= R_1R_2 \\ a_1 &= L_1R_2 + L_2R_1 + g_mL_2R_1R_2 \\ a_2 &= L_1L_2\left(1 + g_mR_2\right) + R_1R_2\left(L_1C_1 + L_1C_v + L_2C_1 + L_2C_2\right) \\ &\approx R_1R_2\left(L_1C_1 + L_1C_v + L_2C_1 + L_2C_2\right) \\ a_3 &= L_1L_2\left[R_1C_1 + R_2C_1 + R_2C_2 + R_1R_2C_v\left(g_m + \frac{1}{R_2}\right)\right] \\ a_4 &= L_1L_2R_1R_2\left[C_1C_2 + C_v\left(C_1 + C_v\right)\right] \end{aligned}$$

The circuit oscillates if the loop gain is unity, which corresponds to a voltage gain V_o/V_i=-1 at the oscillation frequency ω_0

$$\frac{-jg_m\omega_0\left(-L_1L_2R_1R_2C_2\omega_0^2 + jL_1L_2R_1\omega_0 + L_1R_1R_2\right)}{a_4\omega_0^4 - ja_3\omega_0^3 - a_2\omega_0^2 + ja_1\omega_0 + a_0} = -1 \tag{3-3}$$

with proper arrangement, (3-3) yields

$$L_1L_2\left[C_1C_2+C_v\left(C_1+C_2\right)\right]\omega_0^4-\left[L_1\left(C_1+C_v\right)+L_2\left(C_1+C_2\right)-\frac{L_1L_2g_m}{R_2}\right]\omega_0^2+1=0 \quad (3\text{-}4)$$

and

$$\begin{aligned}\left[L_1L_2\left(R_1C_1+R_2C_1+R_2C_2+R_1C_v\right)-g_mL_1L_2R_1R_2\left(C_2-C_v\right)\right]\omega_0^3\\-\left[g_mR_1R_2\left(L_2-L_1\right)+R_1L_2+R_2L_1\right]\omega_0=0\end{aligned} \quad (3\text{-}5)$$

Provided $g_mL_1 << R_2\left(C_1+C_2\right)$ in typical design cases, (3-4) can be simplified as

$$L_1L_2\left[C_1C_2+C_v\left(C_1+C_2\right)\right]\omega_0^4-\left[L_1\left(C_1+C_v\right)+L_2\left(C_1+C_2\right)\right]\omega_0^2+1=0 \quad (3\text{-}6)$$

From (3-6), the oscillation frequency can be approximated by

$$\omega_0\approx\sqrt{\frac{L_1\left(C_1+C_v\right)+L_2\left(C_1+C_2\right)}{L_1L_2\left[C_1C_2+C_v\left(C_1+C_2\right)\right]}} \quad (3\text{-}7)$$

Based on (3-5) and (3-7), the required transconductance g_m to sustain the oscillation is given by

$$g_m=\frac{L_1L_2(R_1C_1+R_2C_1+R_2C_2+R_1C_v)\omega_0^2-L_1R_2-L_2R_1}{L_1L_2R_1R_2(C_2-C_v)\omega_0^2+R_1R_2(L_2-L_1)} \quad (3\text{-}8)$$

Equations (3-7) and (3-8) show the general form of oscillating frequency and transconductance, which could be simplified by selecting the ratio appropriately.

B. Output Voltage Swing

In the proposed VCO circuit, a capacitive feedback is formed by capacitors C_1 and C_2. Due to the in-phase relationship provided by the capacitive feedback and the use of on-chip inductors, the drain and source voltage can swing above the supply voltage and below the ground potential, as illustrated in Fig. 3-6(a). To evaluate the performance enhancement of this technique, the output voltage swing of the VCO is derived from the time-domain waveform of the drain current $I_1(t)$, as shown in Fig. 3-6(b).

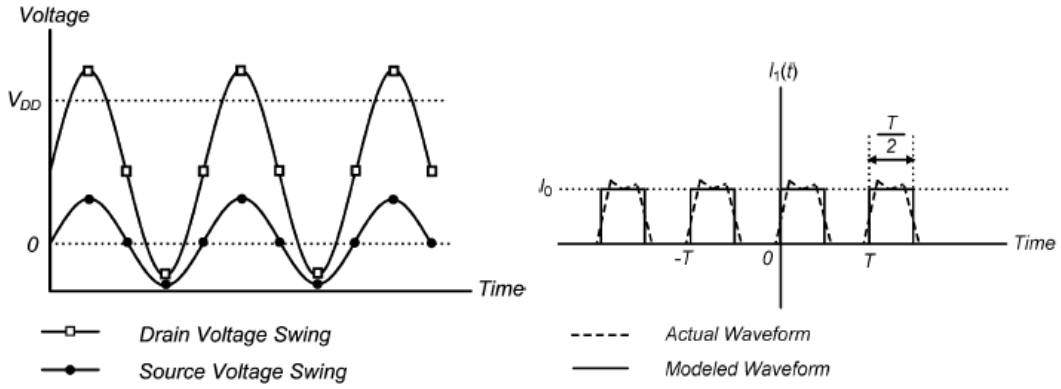


Fig. 3-6 (a) The drain and source voltage waveform due to capacitive feedback

(b) Acutal and modeld drain current waveform [14]

For simplicity, the periodic drain current is modeled by a square wave with a period of $T_0=2\pi/\omega_0$ and an amplitude of I_0. Note that, at the quiescent point, the transistors are biased at $V_{D1}=V_{D2}=V_{DD}$ and $V_{S1}=V_{S2}=0$. The maximum drain current occurs when the gate voltage V_{G1} reaches its peak value. Assuming that the amplitude of output oscillating signal is A, the gate voltages V_{G1} and V_{G2} are $(V_{DD}+A)$ and $(V_{DD}-A)$, respectively, while the source voltages V_{S1} and V_{S2} can be obtained by the voltage divider of C_1 and C_2. Thus, I_0 is approximated by the maximum drain current with the transistor operating in the nonsaturated region

$$I_0 \approx \mu_n C_{ox} \frac{W}{L}\left[(V_{DD}+A+nA-V_t)(V_{DD}-A+nA)-\frac{1}{2}(V_{DD}-A+nA)^2\right] \qquad (3\text{-}9)$$

where $n = C_1/(C_1+C_2)$ and Vt is the threshold voltage of the MOSFET.

From the Fourier series of $I_1(t)$, the fundamental current component is given by

$$I_1(t)\Big|_{fundamental} \approx \frac{2}{\pi} I_0 \sin(\omega_0 t) \qquad (3\text{-}10)$$

and the fundamental voltage amplitude is $A \approx \frac{2}{\pi} I_0 R_p$ (3-11)

where Rp is the load resistance. From (3-9) and (3-11), a simplified expression of the VCO output swing is given by $A \approx (1+C_1/C_2).V_{DD}$

C. Switched-Capacitor-Array

In order to achieve a wide frequency range while keeping a relatively low tuning sensitivity, the frequency tuning range is divided into 10 sub-bands by using a 4-bit binary weighted. For single ended switched capacitors, when a branch is turned ON it will contain two r_{ds0} in series going from one side of the differential circuit via ground to the other. This limits the achievable quality factor and degrades the phase noise. Therefore, the differential switched-tuning is used [19][20], the MOS switches are not directly connected to the ground, and instead they are connected both capacitors. This topology can avoid the substrate noise coupling into the tank and halve the number of the MOS switches. Therefore the on-resistance can be reduced and phase noise is improved. Furthermore, to achieve a high quality a wide transistor could be as wide and as short as possible, however the drain capacitance is proportional to the width of the transistor, that would reduce the tuning range and maximum oscillation frequency, leading to a compromise.

The inverter does not consume any static power, and a negligible amount of silicon area. Together with the resistors it makes sure that the transistor is OFF at all times in the OFF state and gets the maximum gate to source(and drain) voltage in the ON state.

3.2.2 Divider

Frequency dividers operating at high frequency are one of the key blocks in the RF circuits because dividers must function properly over the required bandwidth and provide enough output swing for the next stage. Three kinds of dividers are often used: digital CMOS logic, current-mode logic (CML), and injection-locked frequency dividers (ILFD) [21]. Digital CMOS logic is seldom used since full-scale swing is needed and the operating frequency is relatively low. Compared with CML, ILFD has

lower power consumption with larger area and narrower locking range. Due to very wide bandwidth of VCO, the CML is chosen in this work.

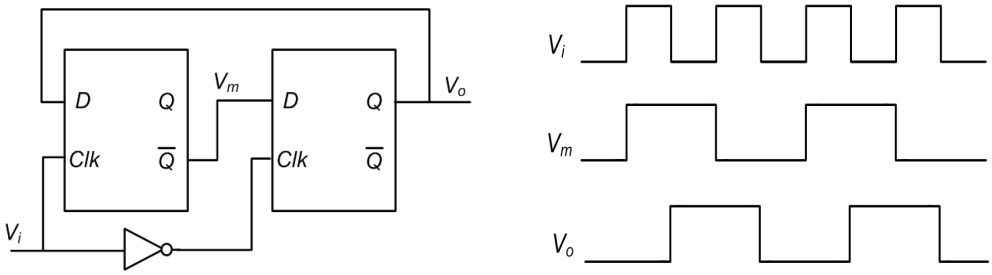


Fig. 3-7 Block diagram of the CML frequency dividers

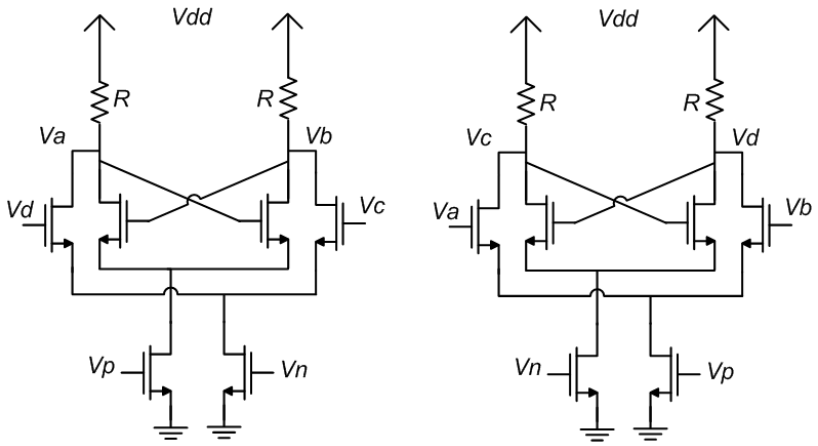


Fig. 3-8 Schematic of the CML frequency dividers

The block diagram of CML frequency dividers is shown is Fig.3-7. The master and slave D-FFs are clocked by complementary clocked signals and the differential outputs of LC-VCO in the previous section provide this kind of input signals. Consequently, the inverter in Fig.3-7 is implemented without adding any circuit. The frequency of both Vm and Vo is half the frequency of Vi. Meanwhile the phase difference between Vm and Vo is just 90 degree and quadreture outputs are obtained. In other words, CML is also a kind of quadrature signal generators owing to the characteristic of the output nodes.

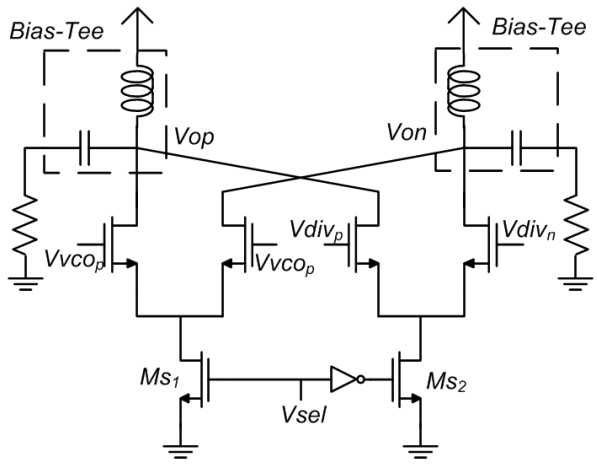
The D-FFs implemented in CML are composed of a clocked differential sensing amplifier pair and inversely clocked latching pair as shown in Fig. 3-8. The two D flip-flops are operate periodically and alternately between two modes. When the input

VCO signal is low, one of the D-FF is in the sensing mode, while the other D-FF is in the latching mode. In contrast with common CML circuits, the bias current source is eliminated increase the maximum operating frequency about 10% [22].

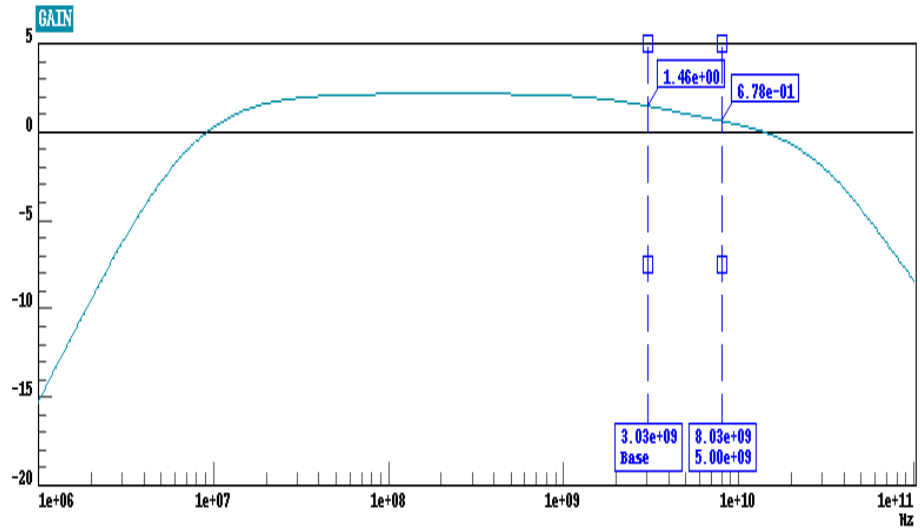
Only NMOS transistors are used in this circuit because the drain parasitic capacitance and power dissipation should be minimized. The trans-conductance of clock transistors has to be large and then the small input signals can drive them from the linear region to the saturation region. Therefore the sensitivity to the DC level of input signals is increased. Due to omitting the current source, the DC bias point of the circuit is determined by the size and Vgs-Vt of the clock transistors, the DC level of the input, and the value of the load resistance.

The load resistance is another key parameter since the dominant pole is decided by the load resistance and parasitic capacitance from transistors, interconnection, and next stage. To make this pole high enough, the R must be small, which inevitable leads to increased power consumption to set the DC output.

3.2.3 2-to-1 Multiplexer



(a)



(b)

Fig. 3-9 (a) Schematic of multiplexer

(b) Gain of the multiplexer vs. the input frequency

The 2-to 1 multiplexer is to decide that the output is generated from VCO or the Divider. Fig. 3-9 shows the schematic of the multiplexer. Again the current source is removed to relax the voltage headroom problem [23]. When V_{sel} is high, M_{S2} is off and the output is only from the VCO. On the other hand, when V_{sel} is low, M_{S1} is off and the output is only from the divider. Because the output frequency covers a wide range of spectrum, the gain must insensitive to the operating frequency. The load inductors and capacitors should be designed as large as possible to alleviate the impedance variation with the frequency. Therefore, the bias-tee is chosen as the load impedance. The inductor and capacitor in the bias-tee can be treated as infinitely large at the multi-GHz frequency. For this reason, the load impedance is approximately on R_L (50Ohm).

3.3 Chip Layout and Simulation Results

A signal generator is designed and simulated by Eldo RF simulator. The chip size is $0.95\times0.65mm^2$ including the pads and fabricated using TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. Fig. 3-10 shows the layout of this circuit, which is kept symmetry to equalize the amplitude of the differential outputs. The power consumption of each block is listed in Table 3-1.

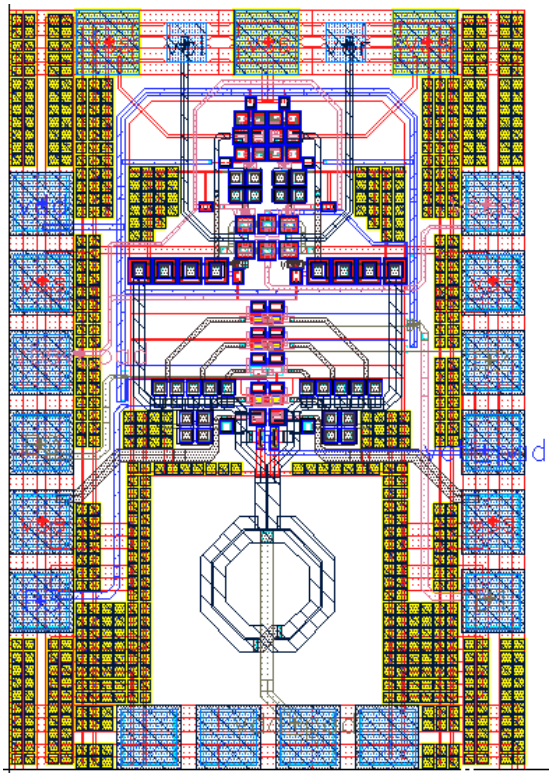


Fig. 3-10 The chip layout

Table 3-1 Power consumption of each block

	power	**current**
VCO	7.1 mW	7.9 mA
Divider	8.16 mW	4.5 mA
MUX	20.53 mW	11.4 mA
total	35.8 mW	21.06 mA

The simulation result shows that the tuning range is 6.05~8.14 GHz for the total 10 curves. Overlapping between curves is necessary to avoid the process variation and cover the entire band as shown in Fig. 3-11

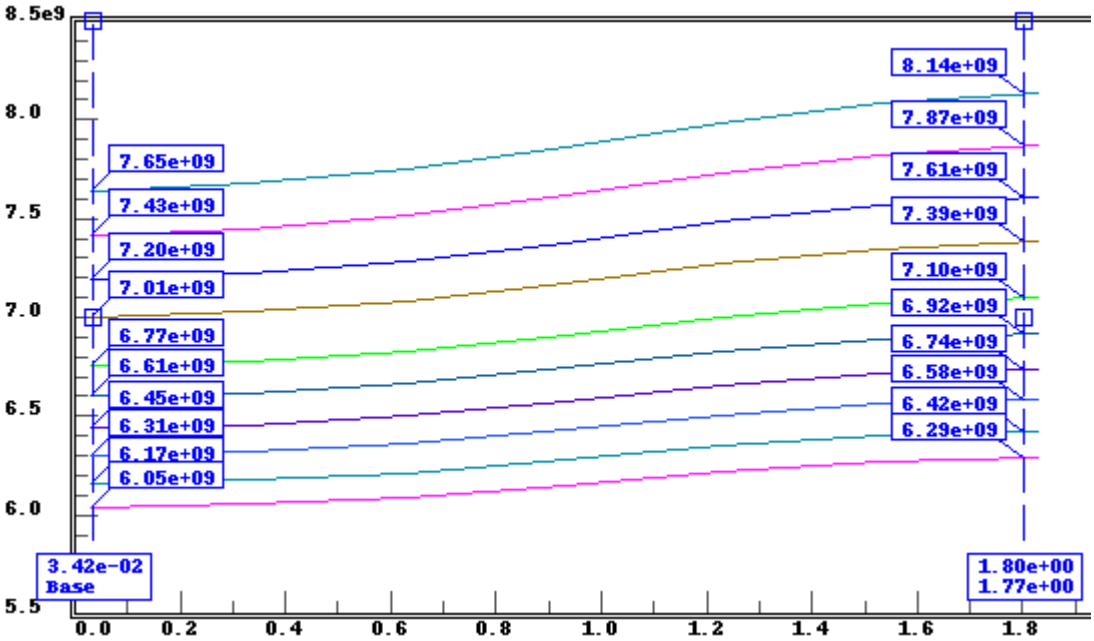


Fig. 3-11 Tuning range curves of different banks

In Fig. 3-12, the band switching is completed in about 0.61 nsec. In consequence, both of the periods are much shorter than the required time 9.5 nsec.

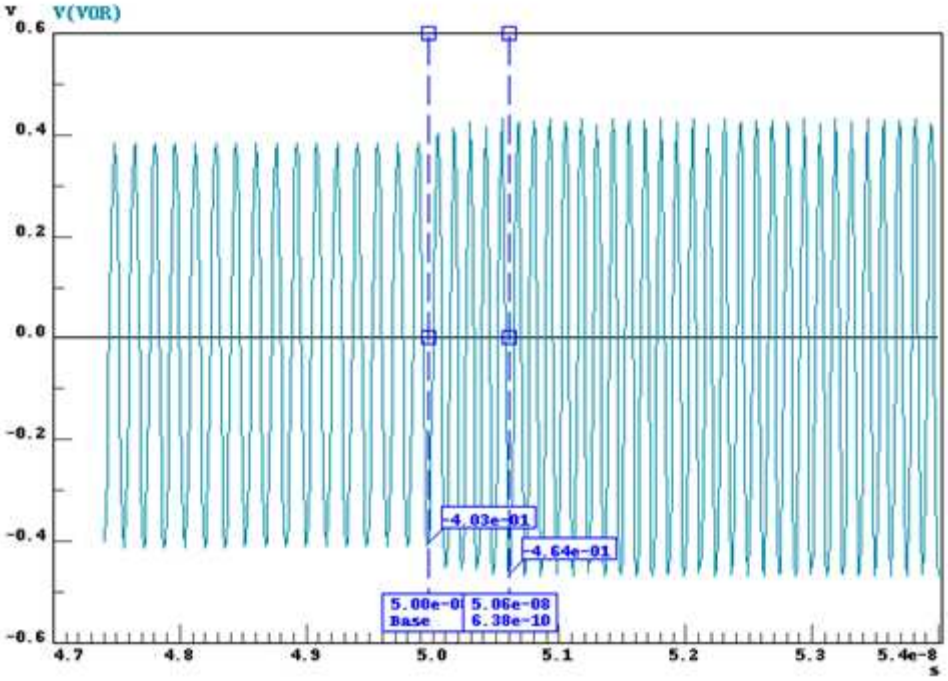


Fig. 3-12 Output waveform switching from bank (0,0,0,0) to (1,1,1,1)

When the digital input is (0,0,0,0) with the control voltage of 1V, the oscillation frequency is 7.920 GHz. The output swing is 0.95 V_{pp} (3.6dBm) and the phase noise is -110 dBc/Hz. Through the frequency divider, output frequency at 3.960 GHz is generated. These results are shown in Fig. 3-13 and Fig. 3-14

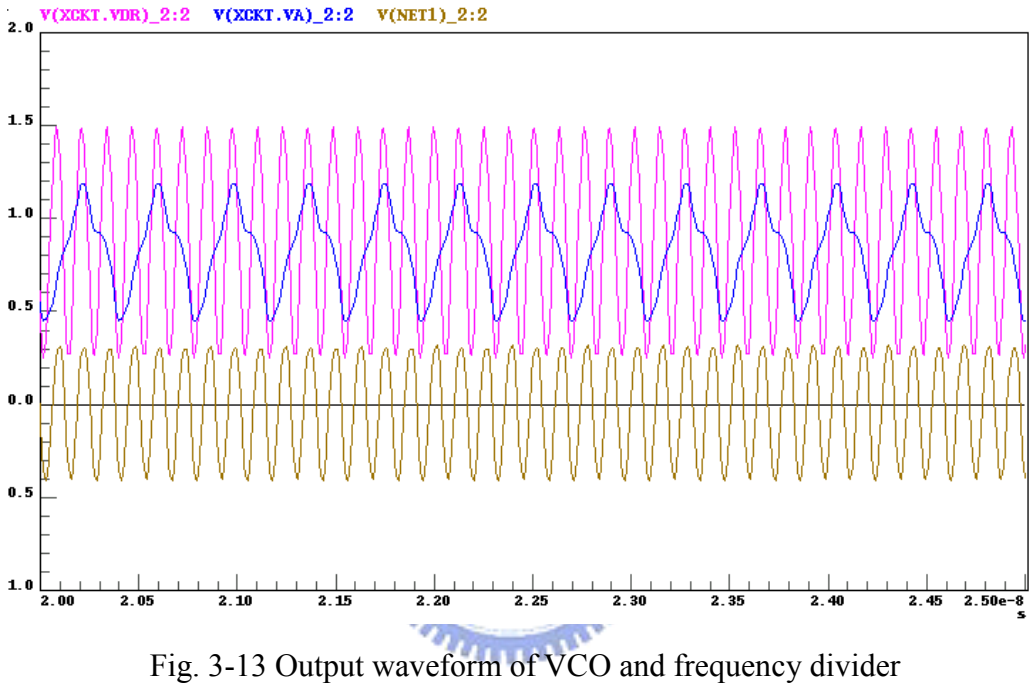


Fig. 3-13 Output waveform of VCO and frequency divider

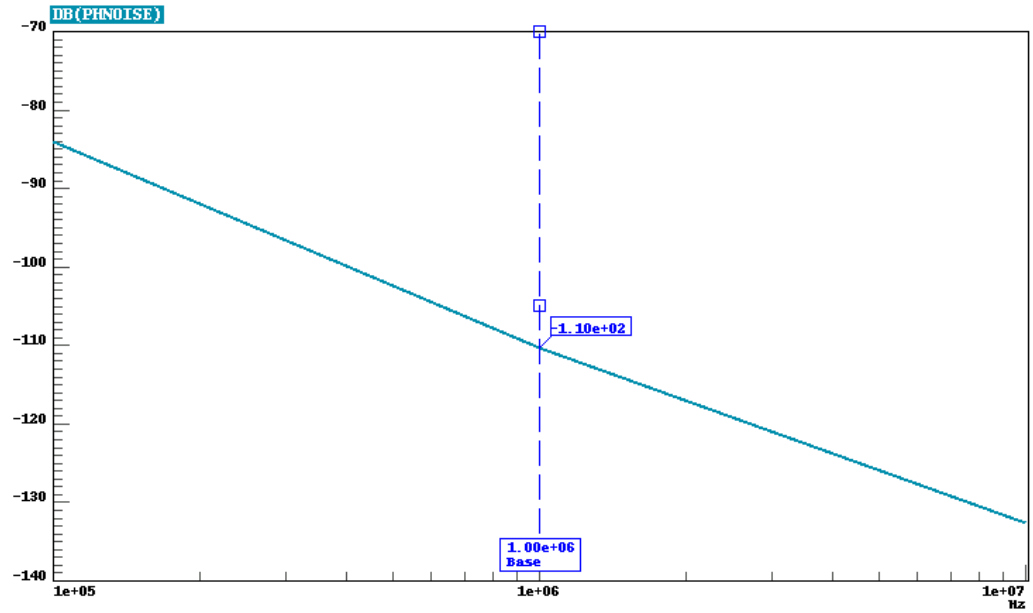


Fig. 3-14 Phase noise with oscillation at 7.920 GHz

When the digital input is (0,0,1,0) with the control voltage of 0.95V, the oscillation frequency is 7.392GHz. The output swing is 0.9 V_{pp} (3dBm) and the phase noise is -111 dBc/Hz. Through the frequency divider, output frequency at 3.692 GHz is generated. These results are shown in Fig. 3-15 and Fig. 3-16

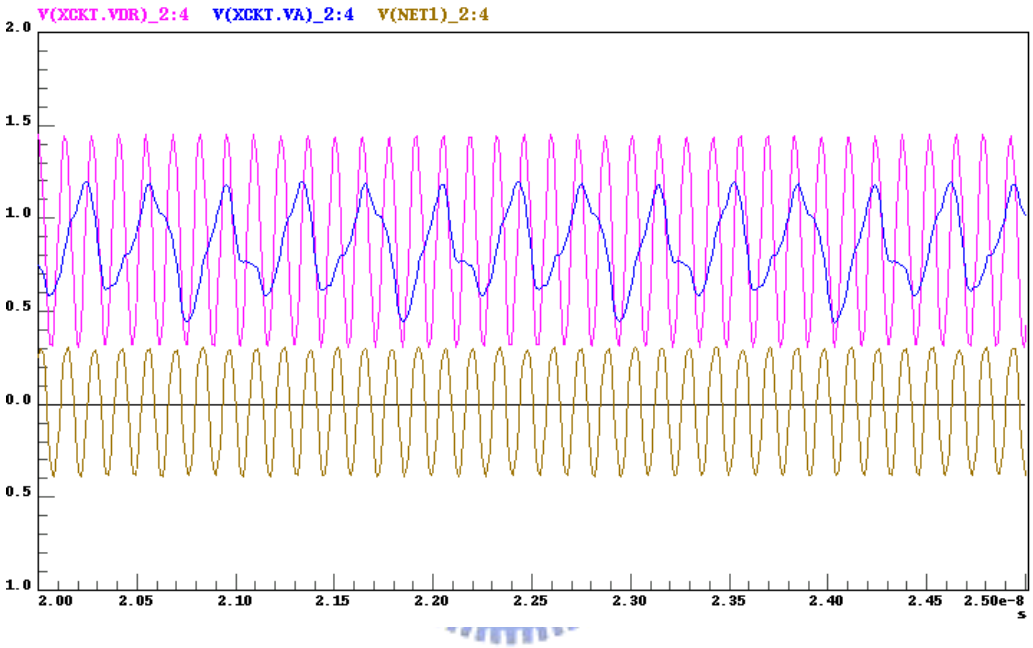


Fig. 3-15 Output waveform of VCO and frequency divider

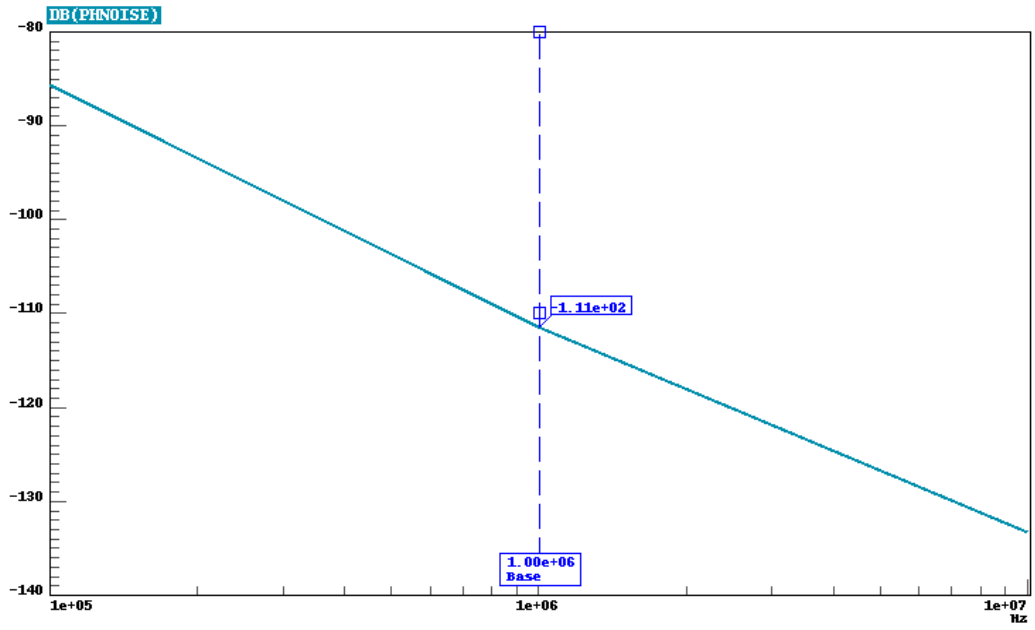


Fig. 3-16 Phase noise with oscillation at 7.392 GHz

When the digital input is (1,0,0,0) with the control voltage of 0.73V, the oscillation frequency is 6.864GHz. The output swing is 0.82 V_{pp} (1.8dBm) and the phase noise is -113 dBc/Hz. Through the frequency divider, output frequency at 3.692 GHz is generated. These results are shown in Fig. 3-17 and Fig. 3-18

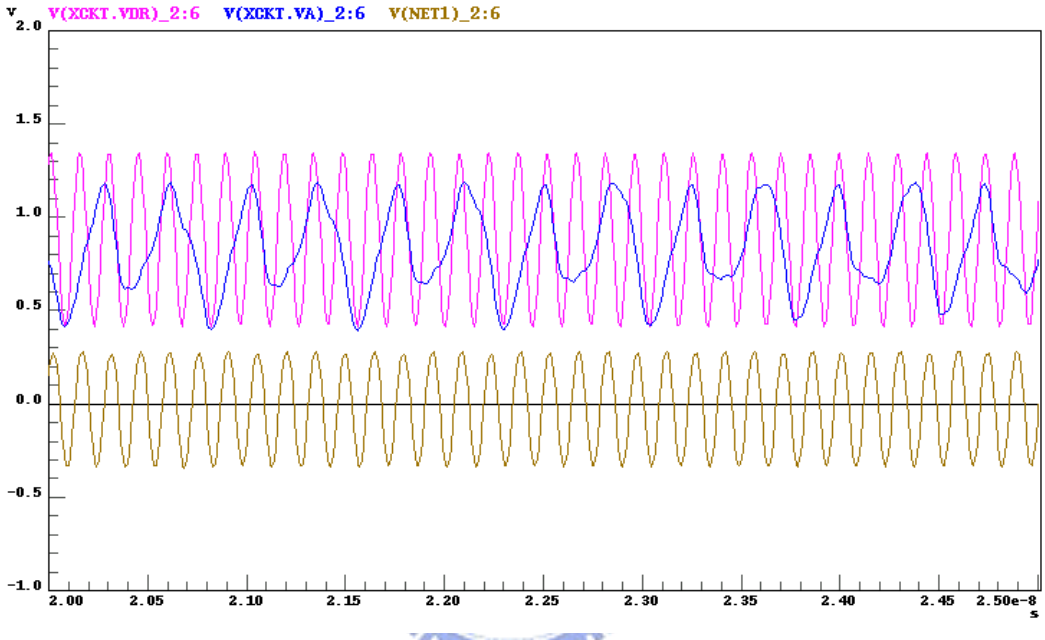


Fig. 3-17 Output waveform of VCO and frequency divider

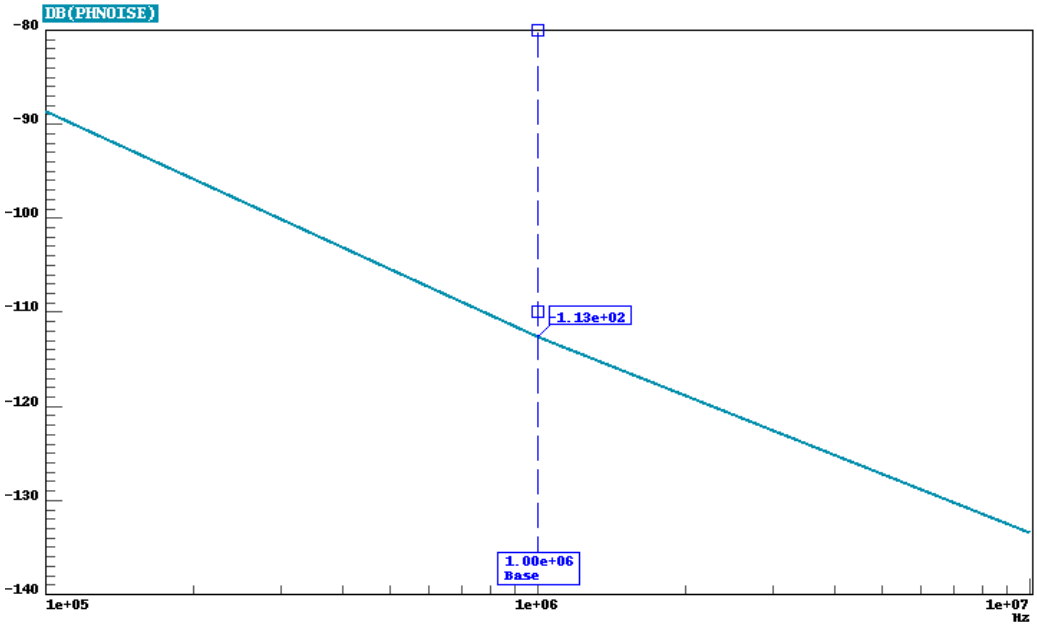


Fig. 3-18 Phase noise with oscillation at 6.864 GHz

When the digital input is (1,0,1,1) with the control voltage of 0.4V, the oscillation frequency is 6.336GHz. The output swing is 0.75 V_{pp} (0.2dBm) and the phase noise is -114 dBc/Hz. Through the frequency divider, output frequency at 3.692 GHz is generated. These results are shown in Fig. 3-19 and Fig. 3-20

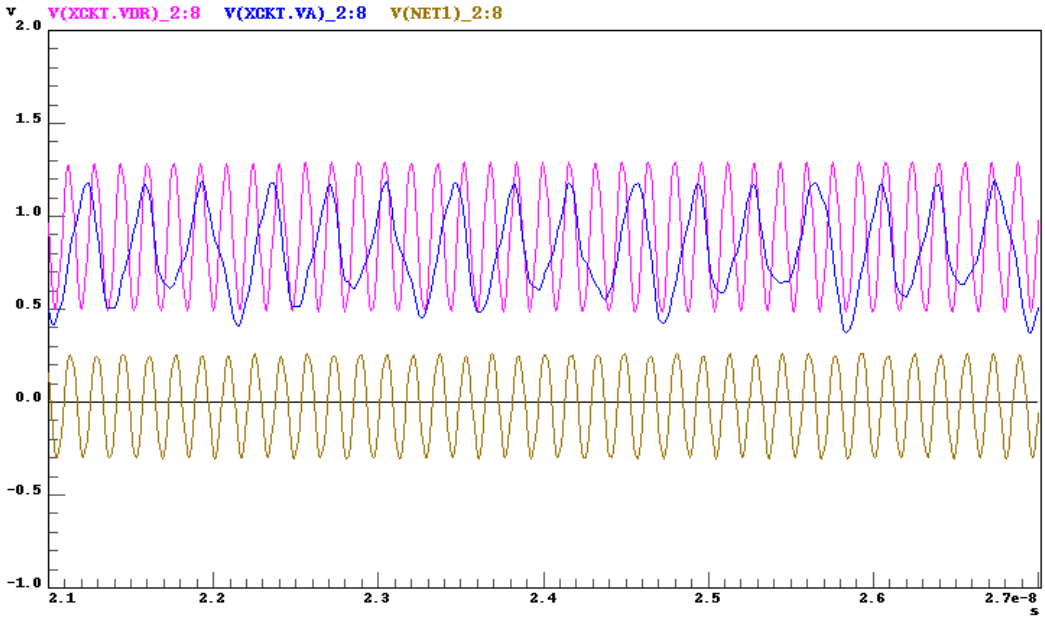


Fig. 3-19 Output waveform of VCO and frequency divider

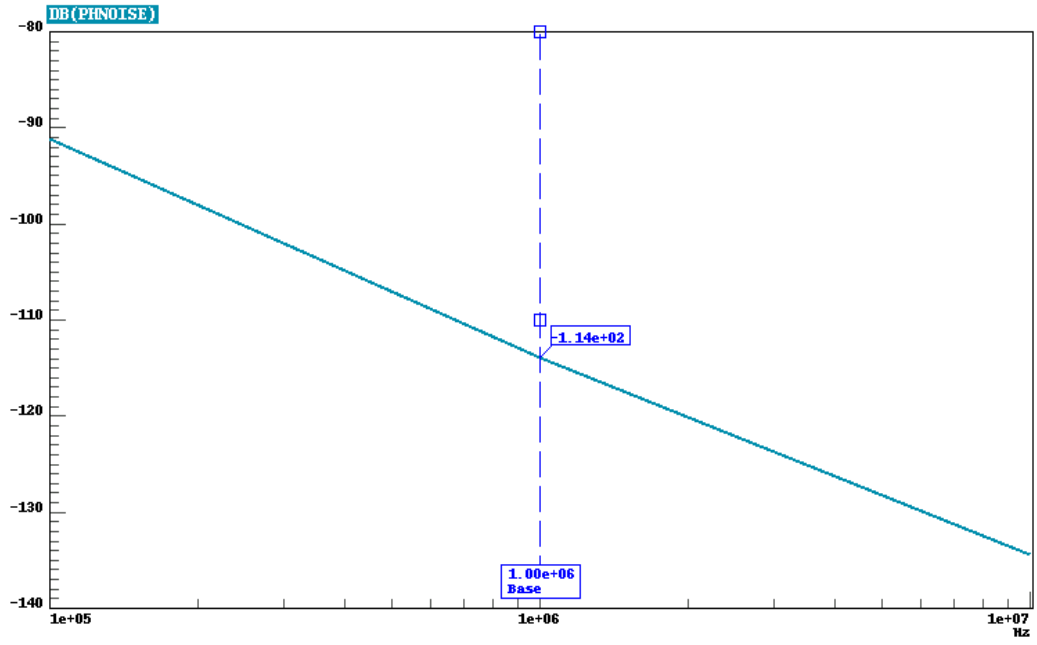


Fig. 3-20 Phase noise with oscillation at 6.336 GHz

Table 3-2 Summary performance of the carrier frequencies

Output Frequency	Voltage Swing	Phase noise @ 1MHz	FOM
6.336 GHz	$0.73V_{PP}$	-114 dBz/Hz	183
6.864 GHz	$0.82\ V_{PP}$	-113 dBz/Hz	182.8
7.392 GHz	$0.9\ V_{PP}$	-111 dBz/Hz	182.1
7.920 GHz	$0.95\ V_{PP}$	-110 dBz/Hz	181

Table 3-3 VCO tuning range and power dissipation for different corner

Corner	TT	FF	SS
Tuning Range (GHz)	6.05~8.14	6.36~8.32	5.75~7.99
Power Dissipation	35.8 mW	45.26mW	29.16mW

Table 3-4 VCO tuning range and power dissipation for different power supply

V_{DD}	0.9V	0.81V	0.99V
Tuning Range(GHz)	6.05~8.14	6.05~8.17	6.04~8.1
Power Dissipation	35.8mW	33.4mW	39.45mW

Table 3-5 VCO phase noise of the carrier frequency for different corner

Corner	TT	FF	SS
7.920GHz	-110	-109	-111
7.392GHz	-111	-110	-112
6.684GHz	-113	-110	-111
6.336GHz	-114	-113	-109

Table 3-6 VCO phase noise of the carrier frequency for different power supply

Corner	0.9V	0.81V	0.99V
7.920GHz	-110	-110	-111
7.392GHz	-111	-111	-112
6.684GHz	-113	-112	-113
6.336GHz	-114	-113	-114

3.4 Measurement results and Discussion

The multi-band controlled oscillator is designed for on-wafer testing. Therefore the arrangement of each pad must satisfy rules of CIC's (Chip Implementation Center's) probe station testing rules. The measurement equipments contain Agilent E5052A signal source analyzer, E4407B spectrum analyzer, and E3615A DC power supply. Also the whole chip photograph is shown in Fig. 3-21

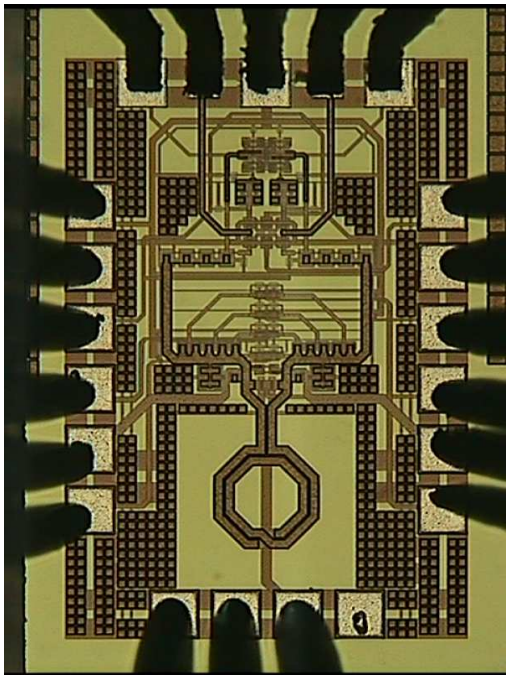


Fig. 3-21 Chip photograph

According to Fig. 3-22, the 10 tuning range curves cover each other and signal at GHz can be generated. Comparing with 6.05~8.14 GHz bandwidth in the simulation results, the total tuning range is a little shrunk. Because the gain of the VCO is little change in Table 3-7, the compressed tuning range is mainly from the overestimated capacitors in SCA.

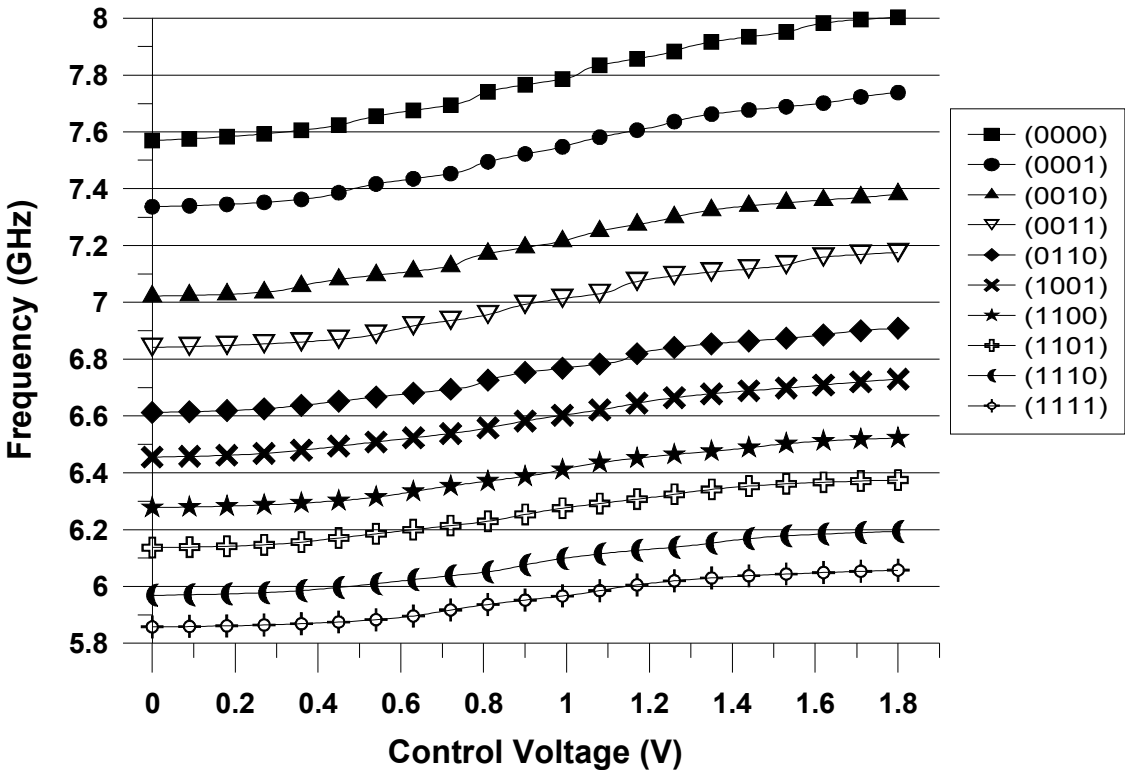
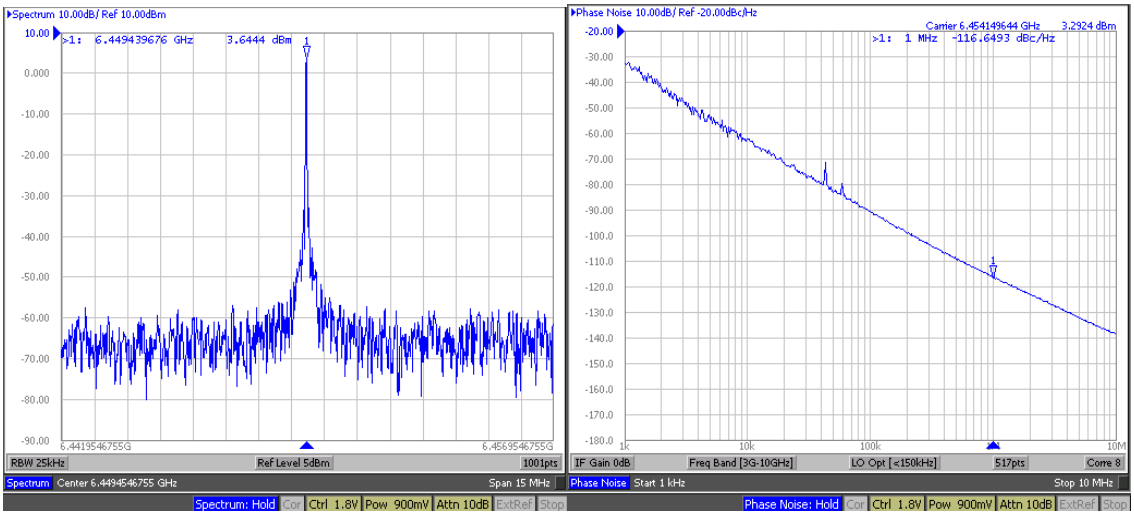


Fig. 3-22 Measured tuning range curves with different banks

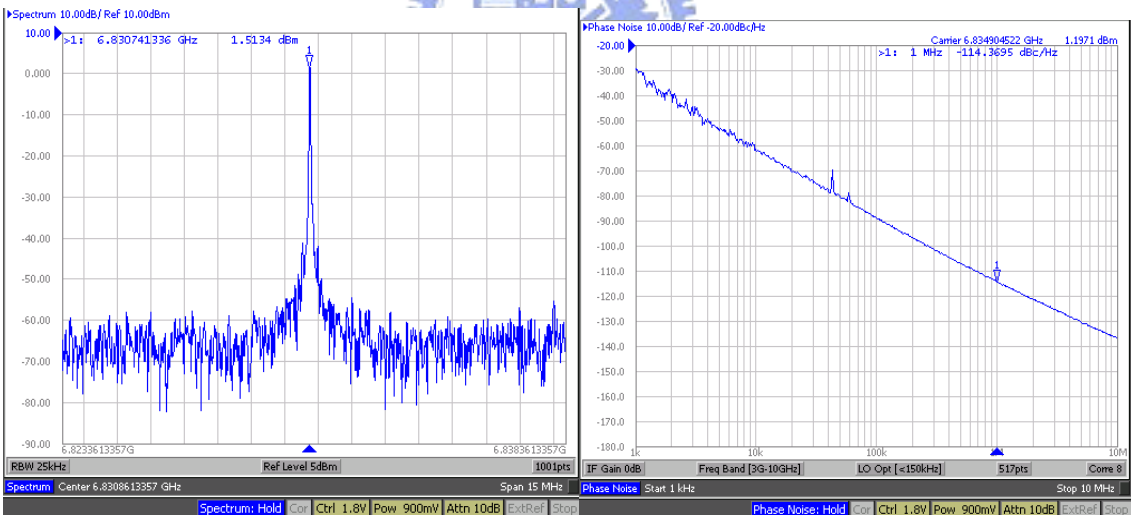
Table 3-7 K_{VCO} comparison between the simulation and measurement

	Simulation	**Measurement**
(0,0,0,0)	272.2 MHz/V	216.7 MHz/V
(0,0,0,1)	244.4 MHz/V	200 MHz/V
(0,0,1,0)	227.7 MHz/V	200 MHz/V
(0,0,1,1)	211.1 MHz/V	161 MHz/V
(1,0,0,0)	183.3 MHz/V	144.4MHz/V
(1,0,0,1)	177.7 MHz/V	138.8MHz/V
(1,1,0,0)	161.1 MHz/V	133.3MHz/V
(1,1,0,1)	150 MHz/V	130.1MHz/V
(1,1,1,0)	138.8 MHz/V	127.7MHz/V
(1,1,1,1)	127.7 MHz/V	116.6MHz/V

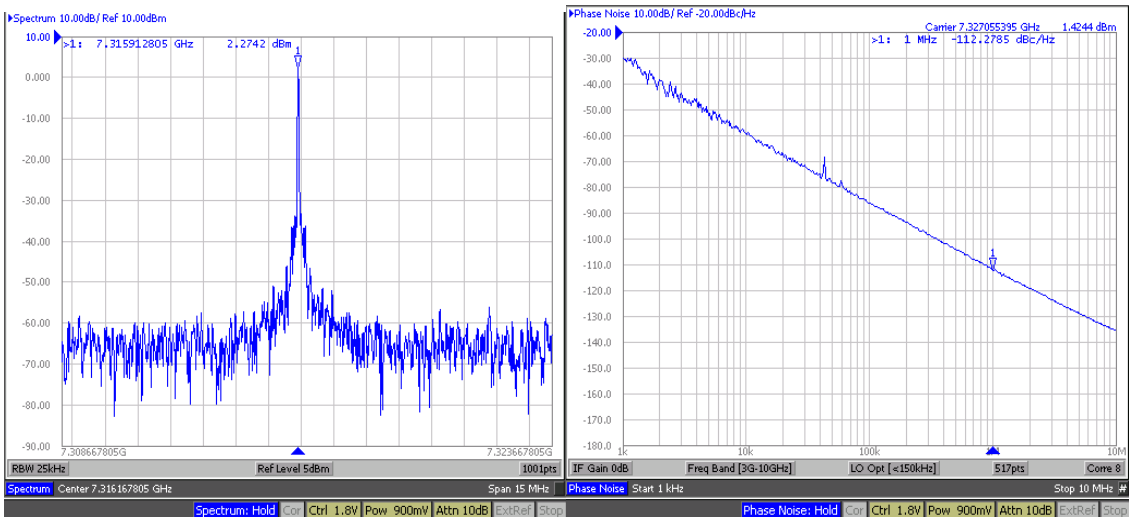
Following the tuning range, the output power and phase noise performance is measured in Fig. 3-23 and Table 3-8. The measure value of the phase noise is approximately equal to the simulated one.



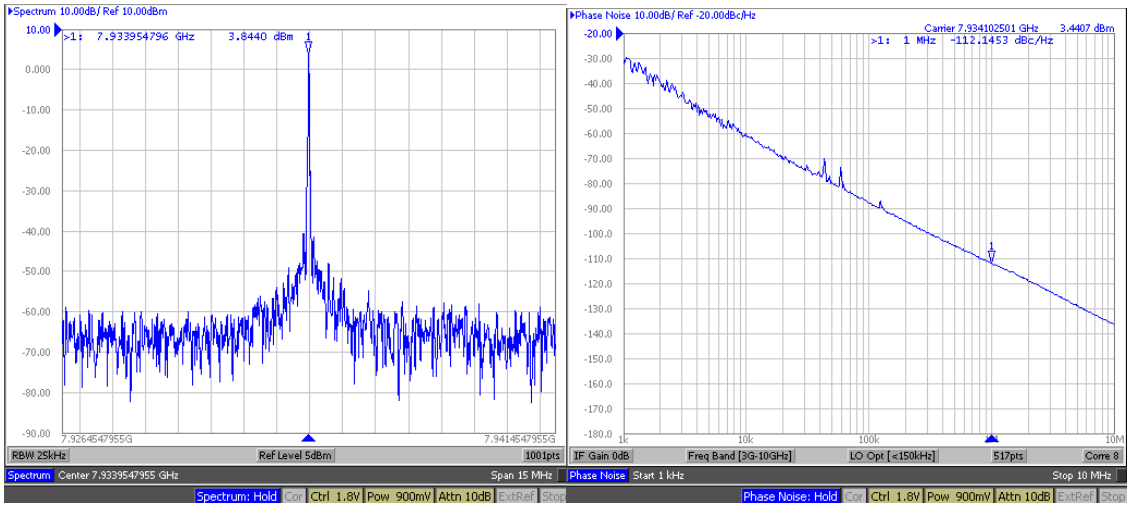
(a) 6.336GHz



(b) 6.864 GHz



(c) 7.392GHz



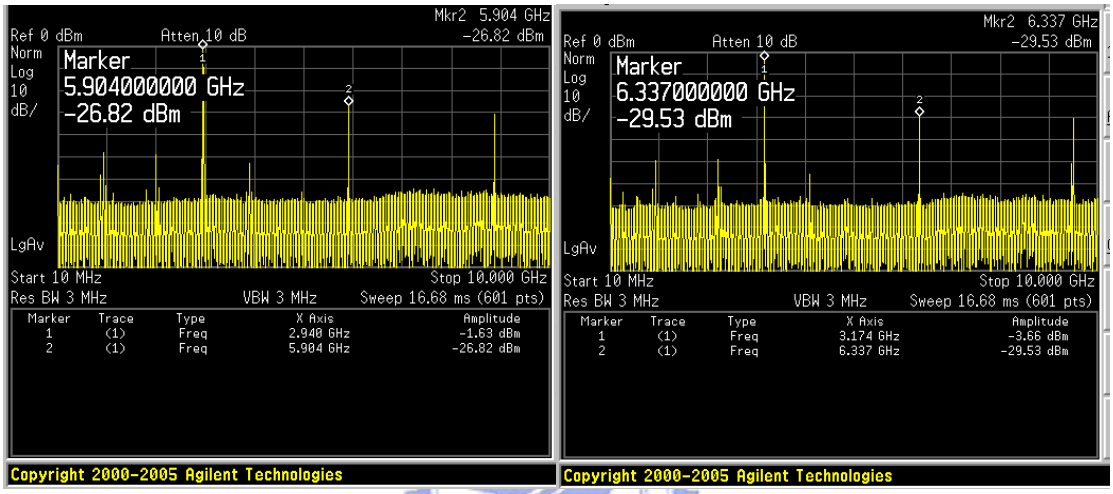
(d) 7.920GHz

Fig. 3-23 Measurement of output power and phase noise

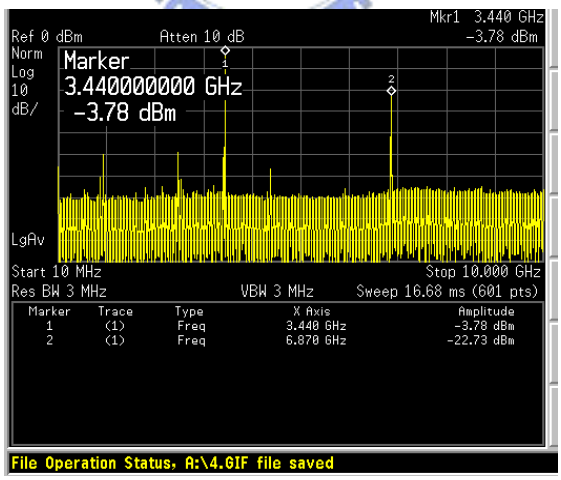
Table 3-8 Measurement of output power and phase noise performance

Output Frequency	Output Power	Phase noise @ 1MHz	FOM
6.336 GHz	3.64	-116 dBz/Hz	185
6.864 GHz	1.51	-114 dBz/Hz	184
7.392 GHz	2.27	-112 dBz/Hz	183
7.920 GHz	3.84	-112 dBz/Hz	183

Besides the VCO, the performance of the divider-by-2 circuit is measured in Fig. 3-24. The multiplexer suppresses the VCO signal about 20dB when the frequency divider is selected. But at 7.3GHz the divider doesn't work properly in Fig. 3-25. The reason is likely that the parasitic effect at the output nodes of the divider is not completely extracted and the behavior can't be accurately predicted in the post-simulation.



(a) (b)



(c)

Fig. 3-24 Output power of the carrier frequency at (a) 2.94 and (b) 3.174 GHz

(c) 3.440 GHz

As a result, the control voltage of VCO is tuned and the locking range of the frequency divider is up to 7.27GHz. The measurement is shown in Fig. 3-26. Finally, the power dissipation of each block in the measurement is very close to the result in the simulation.

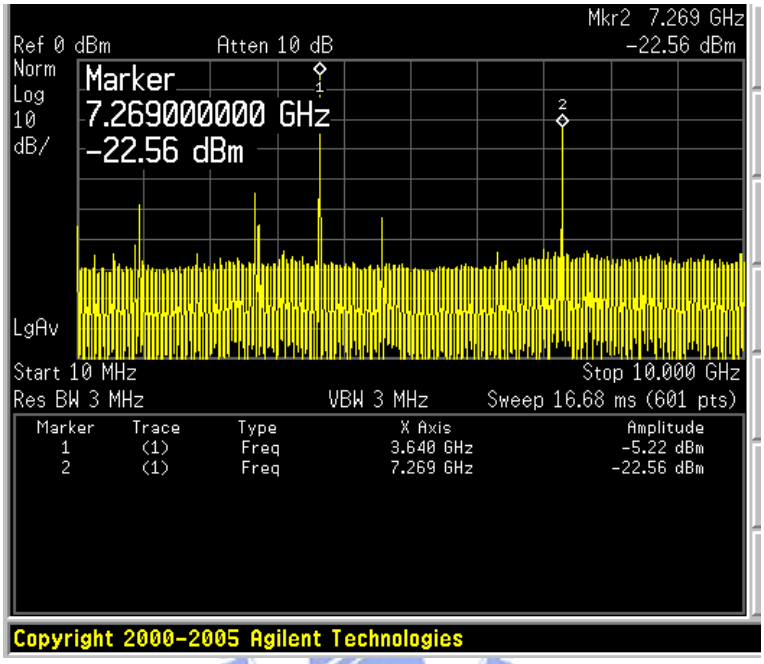


Fig. 3-26 Maximal frequency in the locking range of the divider

The performance in the measurement is close to the results in the simulation except that 3.96 GHz signal is not generated successfully. To improve this, the layout parasitic extraction by EM software has to be more detailed although this will take a longer time. Besides, the bias point of divider design should be checked and fine-tuned. The summary of this work is listed in Table 3-9. In addition, the comparison with other wideband VCOs is shown in Table 3-10. Through the calculation of the figure-of-merit (FOM), this work really achieves better performance.

Table 3-9 Performance summary of the multi-band VCO

Performance	Post-Simulation	Measurement
Supply Voltage	0.9V	
Tuning Range	6.05~8.14 GHz	5.85~7.93GHz
Phasenoise@1MHz	-110~-114dBc/Hz	-112~-116dBc/Hz
Power Consumption	35.8 mW	36.2
Output Power	2.2~4.5 dBm	1.51~3.84 dBm
FOM	181~183	183~185

Table 3-10 Comparison with the multi-band VCOs

	This work	ISCAS 2005 [25]	MWCL 2005 [24]
Technology	0.18 μ m CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Supply Voltage	0.9 V	1.5V	1.8V
Tuning range	5.85~7.93 GHz	3.5~5.3 GHz	5.5~6.7 GHz
Phase noise (dBc/Hz)	-116 @ 1 MHz	-115 @ 1 MHz	-114 @ 1 MHz
Power Dissipation	36.2 mW (7 mW in VCO core)	6 mW	5.8 mW
FOM	185	182	180

Chapter 4 Conclusion and Future Work

4.1 Conclusion

In chapter two, we discuss two kinds of VCO based on transformer：feedback to the Back-gate and the source. In order to achieve higher frequency operation, transformer is feedback to the back gate. The measured results reveal that the power consumption is 6.2mW for 1.5V supply voltage, the tuning rage is between 8.14~8.61 GHz, the phase noise is -113dBc/Hz@1MHz. Adopting transformer feedback from drain to source enables ultra-low power application. The measured results reveal that the tuning rage is between 5.13~5.42 GHz, the phase noise is -114dBc/Hz @1MHz, the power consumption is only 0.57mW under 0.5V supply voltage. In chapter three, for MB-OFDM UWB system, the VCO generates the carrier frequency for Band 6~9, the divider generate Band 1,2, and multiplexer select the signal from the VCO or Divider. The measured results reveal that the tuning rage is between 5.85~7.93 GHz, the phase noise is best -116dBc/Hz @1MHz, the total power consumption is 36.2mW.

Finally, we introduce an ultra-wide band low noise amplifier in the appendix. It uses the intrinsic capacitance of transistors to achieve the input matching and the complicated input matching network is replaced. The simulation result of UWB LNA demonstrates S11 < -10dB and S22 < -10dB from 3.1 to 10.6 GHz. The power gain (S21) is 15dB. The minimum noise figure is 4.2dB.

4.2 Future Work

From chapter 2, the X-band back gate TF-QVCO could be modified as shown in Fig. 4-1. We insert a resistor between the bias transistor as current source and the core circuit [6]. Low frequency bias noise is the dominant factor for the $1/f^3$ phase noise. The filtering resistance can isolate the bias transistor from the cross-coupled pair and less bias noise can be upconverted into the $1/f^3$ phase noise. As we increase the resistance, the $1/f^2$ phase noise performance will reach its optimum value and begin to degrade in the same way. This is because the thermal noise contribution overwhelms the phase noise reduction by the harmonic filtering. So there is a tradeoff between $1/f^2$ and $1/f^3$ phase noise performance as a function of the filtering resistance.

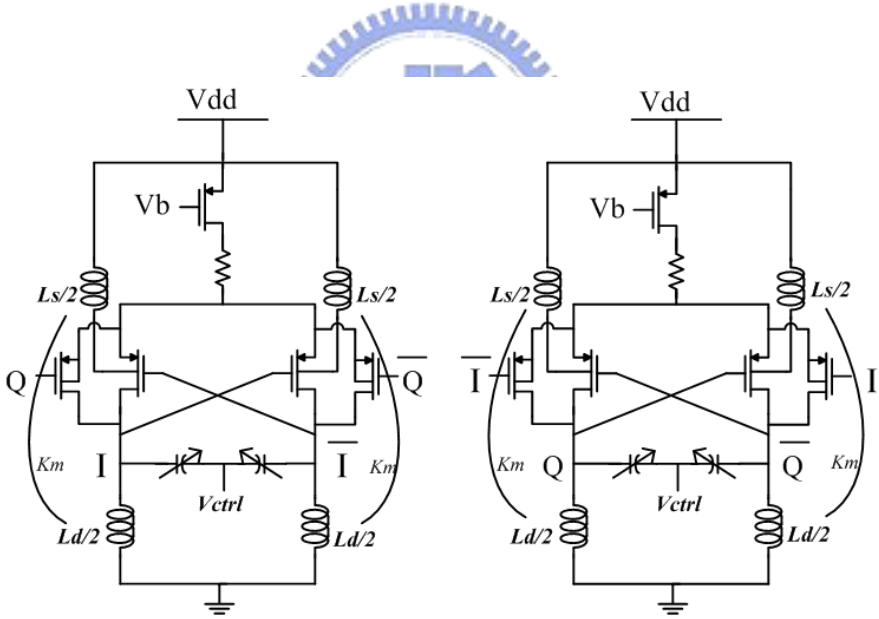


Fig. 4-1 Revised architecture of back gate TF-QVCO

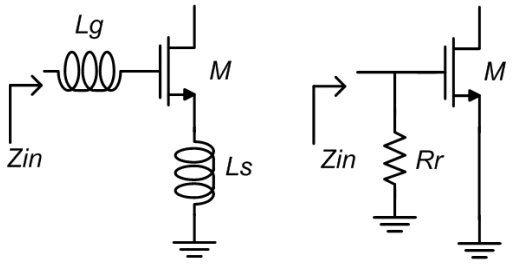
Appendix

CMOS Low-Noise Amplifier for UWB System

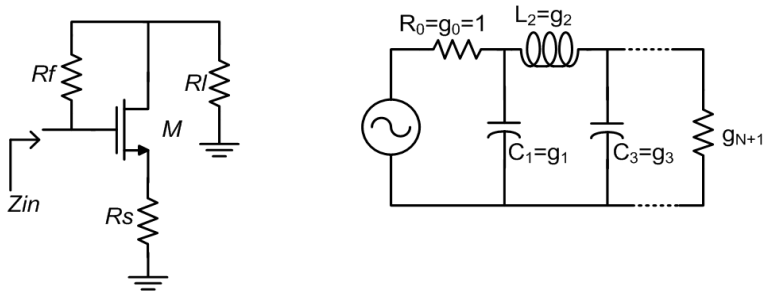
A.1 Introduction

A low-noise amplifier is the first stage in the receiver block of a communication system. For UWB applications, the criteria to judge its performances are slightly different from narrow system. Because transmitted power spreads over a wide range and is restricted to be less than -41.3 dBm per MHz, the requirement on linearity in UWB system is not such important as in narrow system. The important requirements for UWB applications are wide-band input impedance matching, low power consumption, low noise performance, and enough gain to suppress noise of the next stages.

Fig. A-1 shows the four basic 50 Ohm input matching techniques. However, these topologies have some drawbacks. The four input matching is only suit for narrow band amplifier [26][27][28][29][30].



(a) (b)



(c) (d)

Fig. A-1 Basic input matching topology. (a) Inductive source degeneration.(b) Direct resistor termination.(c) Shunt-series feedback.(d) Chebyshev band-pass filter

Fig. A-1 (a) is traditional source degeneration topology, because it only resonances at one frequency, it can't achieve wide-band 50 Ohm matching. It realizes only narrow band matching. Fig. A-1 (b) is the resistive termination matching, because of the loading effect, it will loss a lot of voltage if resistive termination matching is used. Fig. A-1 (c) is feedback method. It can achieve wideband input matching. But because of feedback mechanism, it can't achieve high gain to suppress noise of the next stages. Fig. A-1 (d) is LC 3'rd Chebyshev band-pass filter. It can perform good input matching, but it consumes large chip area because of using four inductors for input matching.

The noise performance of an LNA is directly dependent on its input matching. The wide-band input matching is intrinsically noisier than narrow-band counterparts as the noise performance can not be optimized for a specific frequency. Thus the designer has to be trade off between the input matching and noise.

- Distributed amplifiers [31]

  The Fig. A-2 shows a basic four-stage single-ended distributed amplifier.

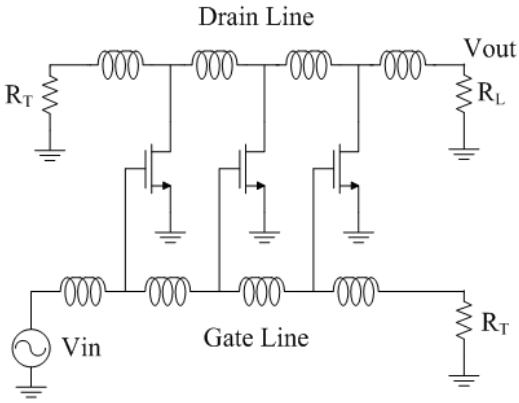


Fig. A-2 Basic four single-end distributed amplifier

The distributed amplifiers normally provide wide bandwidth characteristics but they consume large dc current due to the distribution of multiple amplifying stages, which make them unsuitable for low-power application. And the distributed amplifiers are not optimized for noise. This bring the challenge of finding a low-power topology that satisfies all the other design requirements, the most stringent one being the input match.

- Ultra-wideband low noise amplifier using LC-ladder filter input matching network [32][33]

Recently another topology of wideband LNA has been present. It expands the conventional narrow-band LNA using source degeneration by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a wider bandwidth. Fig. A-3 shows a typical narrowband cascode LNA topology and its small-signal equivalent circuit.

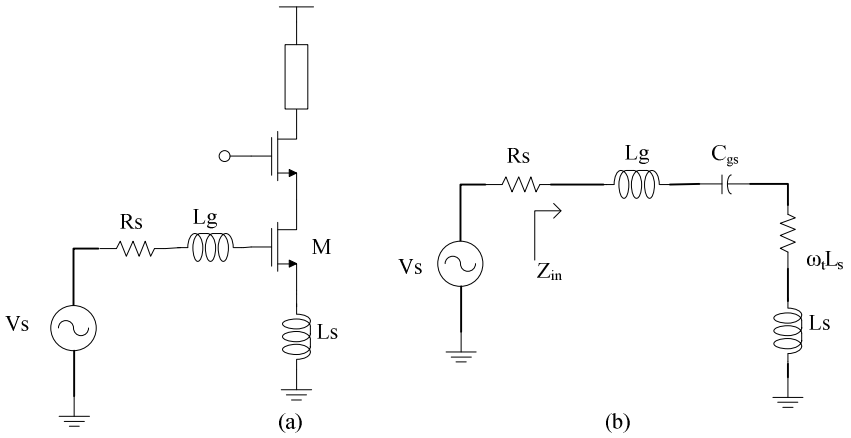


Fig. A-3 Narrowband LNA topology. (a) overall schematic. (b) Small-signal equivalent circuit at the input

The inductor L_s is added for simultaneous noise and input matching and L_g for the impedance matching between the source resistance R_s and the input of the narrowband LNA [14]. Fig. A-3(b) shows the equivalent small-signal circuit. Assume the gate-drain C_{gd} can be ignored, the impedance of the gate terminal is a series RLC circuit. The reactive part of the input impedance is resonated at the carrier frequency in narrowband design. The basic concept of the LC-ladder input matching is expanded from the input impedance of the narrowband which is a series RLC circuit. Consider a fourth-order bandpass ladder filter, shown as in Fig. A-4.

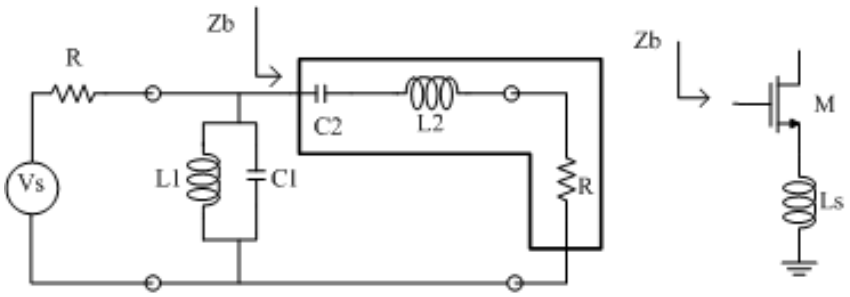


Fig. A-4 Fourth-order bandpass ladder filter used for impedance matching.

The right part of the bandpass filter looks similar to the equivalent circuit of the inductively degenerated transistor in Fig. A-3(b). Therefore, the bandpass filter can embed the inductively degenerated transistor and obtain the desire input impedance.

The LC-ladder filter input matching of wideband LNA has two significant drawbacks. Because the LC-ladder filter at the input mandates a number of reactive elements, which could lead to a larger chip area and noise figure degradation in the case of on-chip implementation.

- Ultra-wideband low noise amplifier using the common-gate as the first stage.[34]

In traditional narrow-band receiver the common-gate is not used widely due to its relatively lower gain and higher noise figure than a common-source amplifier. The actual configuration of common-gate stage is shown in Fig. A-5(a).

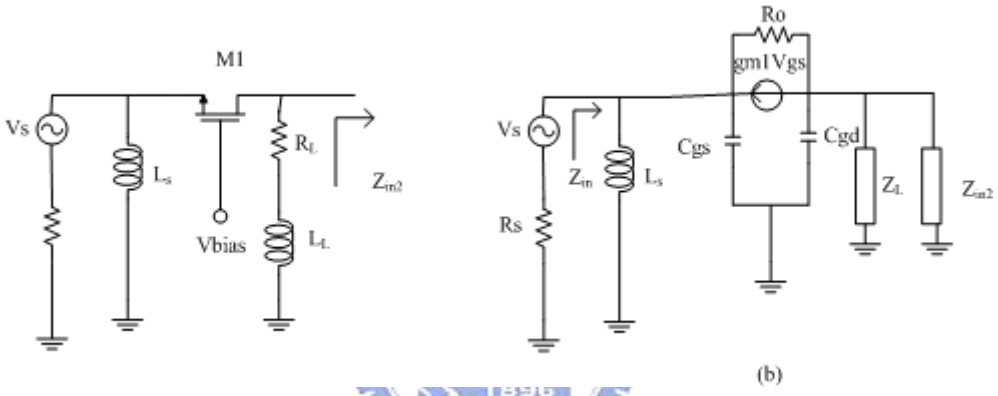


Fig. A-5 (a) Configuration of a common-gate input stage.

(b) The small-signal equivalent circuit.

From the Fig. A-5(b), we can derive the input impedance

$$Z_{in} = \frac{1}{g_{m1} + \frac{1}{Z_s(\omega)} + \frac{1 - g_{m1} Z_o(\omega)}{R_o + Z_o(\omega)}} \cong \frac{1}{g_{m1} - j\frac{1}{X_s(\omega)} + \frac{1 - jg_{m1} X_o(\omega)}{R_o + jX_o(\omega)}}$$

In below equation we assume that the $Z_s(\omega)$ and $Z_o(\omega)$ are both composed of high-Q inductors and capacitors and can be regarded as purely reactive within the frequency band of interest.

$$Z_s(\omega) = j\omega Ls // \frac{1}{j\omega C_{gs}} = jX_s(\omega), Z_o(\omega) = \frac{1}{j\omega C_{gd}} // Z_L // Z_{in2} = jX_o(\omega)$$

After some mathematical calculation

$$Z_{in} = \frac{1}{(g_{m1} - \frac{g_{m1}.X_o^{\ 2}(\omega) - R_o}{R_o^{\ 2} + X_o^{\ 2}(\omega)}) - j(\frac{1}{X_s(\omega)} + \frac{1 + g_{m1}R_o}{R_o^{\ 2} + X_o^{\ 2}(\omega)} \cdot X_o(\omega))}$$

Since $g_{m1}X_o^{\ 2}(\omega) << R_o^{\ 2} + X_o^{\ 2}(\omega)$,the real part in the denominator will remain relatively constant within the 3.1-10.6GHz UWB band. The imperfect matching of the common-gate stage throughout the band arise from the frequency dependent $Xs(\omega)$ that dominates the imaginary part in the denominator. To get a good matching over the wide band , the LC tank of $Xs(\omega)$ formed by Ls and C_{gs} should be selected such that they resonate at the center of the 3.1-10.6GHz, leaving only a 50Ω real input impedance. The noise figure of the common-gate input stage UWB LNA can be improved by increasing g_{m1} but it will degrade the input matching.

- Wideband matching using the transistor intrinsic gate-drain capacitor [35]

Recently a novel wideband input match has been present. It considers the gate-drain capacitor has significant effect on the circuit performance. The Fig. A-6 show a simple common source amplifier with source degeneration inductor and the drain loaded an equivalent capacitor and resistor from the next stage.

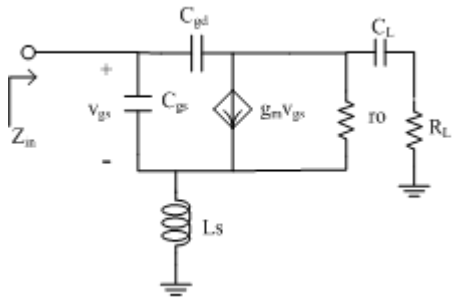


Fig. A-6 The small signal equivalent circuit of common-source with inductive source degeneration

The C_{gd} and r_o are neglected in conventional analysis of low noise amplifier. It is inaccurate numerically. If both C_{gd} and r_o are considered we will find that the input match at high frequency is depend on the resistive load and at low frequency is depend on the capacitive load. We can achieve wideband match without external input

match network. It also can achieve low noise match. Therefore, we will adopt this wideband matching method as a part of the proposed LNA.

A.2 Design Consideration

A.2.1 Wideband matching technique[35]

Consider a small signal equivalent circuit of a source degeneration low noise amplifier which is shown in Fig. A-7. C_L and R_L present the parasitic capacitance and resistance which is contributed from the next stage.

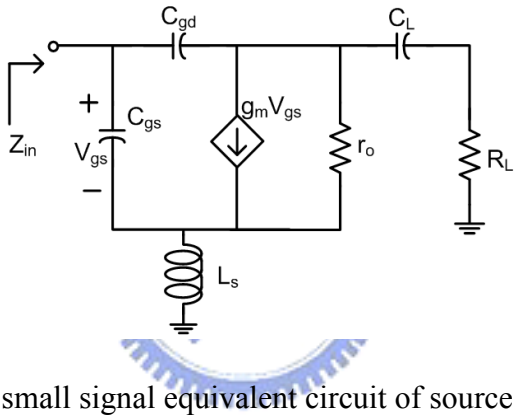


Fig. A-7 The small signal equivalent circuit of source degeneration

To derive the input impedance we consider that the load of the circuit is divided into two parts, one of which is only a resistor R_L which dominates at the high frequency and another is the capacitor C_L dominates at the low frequency. The circuit of resistive loading is shown in Fig. A-8

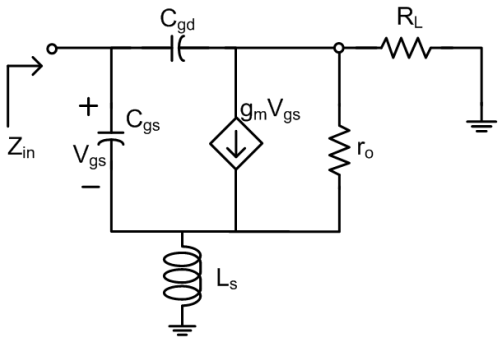


Fig. A-8 The equivalent small signal circuit of resistive loading

While we assume that $\omega L_s << \frac{1}{\omega C_{gs}}$ $\omega L_s << R_L$ we can find the input impedance $Z_{in} \approx (\frac{1}{j\omega C_{gs}} + \frac{L_s \gamma g_m}{C_{gs}})[1 + \frac{C_{gd}}{C_{gs}}(1 + \gamma g_m R_L)]^{-1}$, with $\gamma = \frac{r_o}{r_o + R_L + j\omega L_s}$. As frequency as high the input impedance will approach the 50Ω when the inductor Ls is designed properly. To derive the input impedance of the capacitive loading, which is shown in Fig. A-9, we divided this circuit into two branches and replace the current source by voltage source.

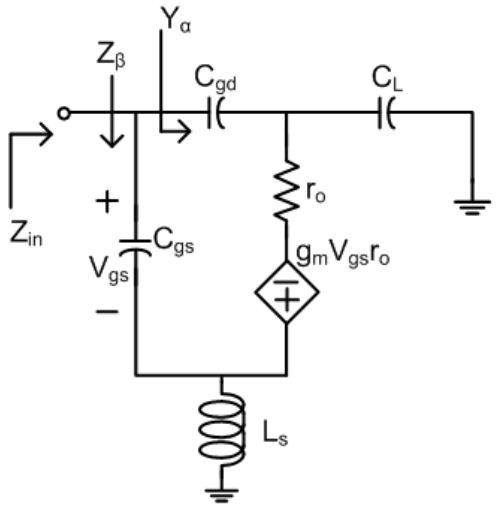


Fig. A-9 The equivalent small signal circuit of capacitive loading

One of the two branches is looking into the capacitor C_{gs} and another is looking into the capacitor C_{gd}. Y_α is the impedance looking into the C_{gd} and Z_β is the impedance looking into the C_{gs}. Assuming that the current flowing the capacitor C_{gd} and C_{gs} is smaller than the induced current $g_m V_{gs}$, the Y_α can be derived. Thus $Y_\alpha = j\omega C_{gd} + (R_\alpha + \frac{1}{j\omega C_\alpha} + j\omega L_\alpha)^{-1}$ and $Z_\beta = \frac{1}{j\omega C_{gs}} + (\frac{1}{R_\beta} + j\omega C_\beta + \frac{1}{j\omega L_\beta})^{-1}$

with $R_\alpha = \frac{C_L}{g_m C_{gd}}$, $C_\alpha = g_m r_o C_{gd}$, $L_\alpha = \frac{L_S C_L}{g_m r_o C_{gd}}(1 + g_m r_o)$

$$R_\beta = \frac{g_m L_s}{C_{gs}} \quad , C_\beta = \frac{C_{gs}}{g_m r_o} \quad , L_\beta = \frac{L_s g_m r_o C_L}{C_{gs}}$$

The input impedance of the capacitive loading circuit can be found out as follow

$Z_{in} = (Y_\alpha + \frac{1}{Z_\beta})^{-1}$. According to above the equations the input impedance can be rearranged as a simpler RLC circuit as shown in Fig.4-10

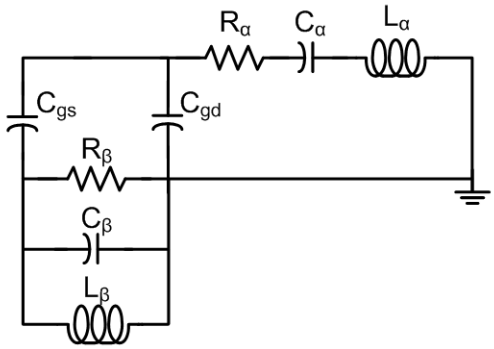


Fig. A-10 The equivalent circuit of input impedance

The C_{gd} branch is the critical branch that is a series component of RLC and its resonate frequency is $f_0 = \frac{1}{2\pi\sqrt{L_\alpha C_\alpha}} = \frac{1}{2\pi\sqrt{L_S C_L (1+g_m r_o)}}$. At the high frequency the resistive loading is matched and the capacitive loading is matched at the comparatively low frequency. Thus the composite $R_L C_L$ load circuit is matched over a wide bandwidth.

A.2.2 Ultra Wide-band Low-Noise Amplifier

Fig. A-11 shows a UWB LNA using transistor's intrinsic gate-drain capacitor to achieve input matching. In this design we add an inductor to the original $R_L C_L$ loading circuit, as shown in figure Fig. A-12.

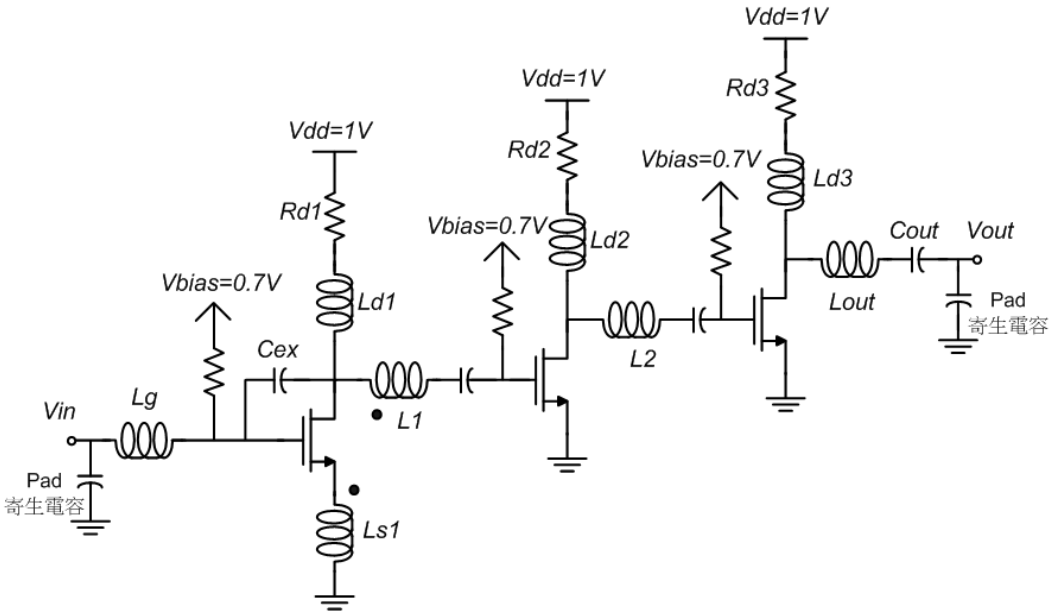


Fig. A-11 The schematic of the proposed UWB LNA

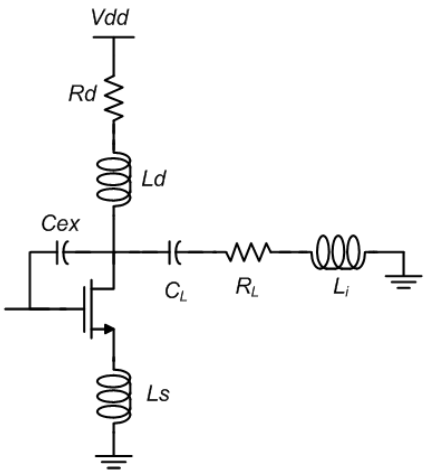
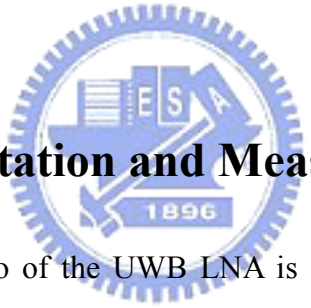


Fig. A-12 The equivalent circuit of first stage UWB LNA

In this circuit the external C_{ex} is added to increase the equivalent gat-drain capacitance, thus allowing a smaller transistor to get better input match but it effect the noise figure at lower frequency. The inductor L_i can improve the input matching.

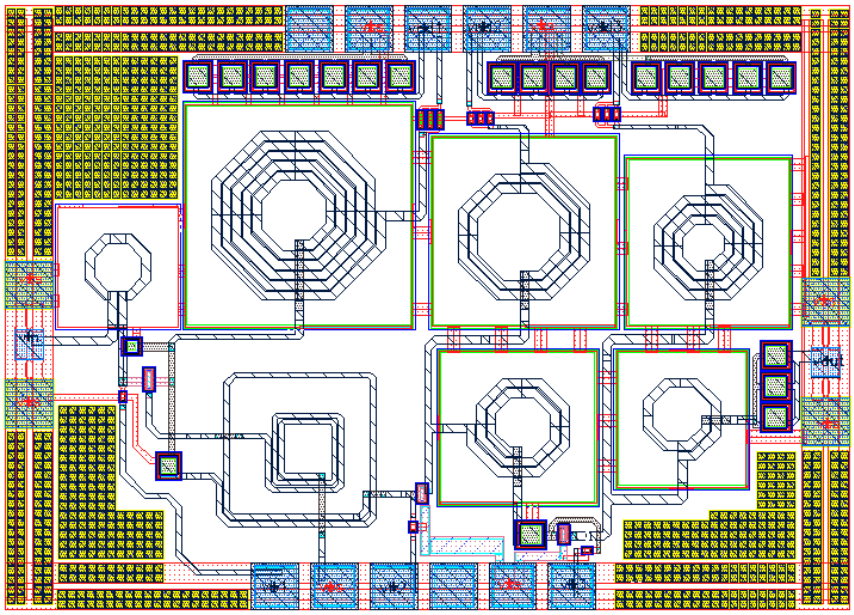
To improve the input match at lower frequency the gate inductor is added and it will influence the noise figure. Shunt-series-peaking is a bandwidth extension technique [36] which is used in this circuit to extend bandwidth by the inductor L_d, L_i and resistor R_d. To achieve a flat gain over whole frequency range we cascade three stages.

The concept of this design is that we design the first stage with a capacitive, resistive and inductive load to achieve the input return loss first. The transformer is added to improve the input return loss and flatter gain but it may make the circuit become a little unstable and it has to be design carefully. The value of capacitive load is approximated to the next input impedance of next stage. Due to the input impedance of the common source topology is the series resistance, capacitor and inductor it is suited to be the consequence stage. We use the common source topology to be the second and third stage. Then we replace the resistance by the common source stage with a capacitive, inductive and resistive load and fine tune all elements to get required specification. The three stages are response for different band of gain to maintain the flatter gain over whole wide band.

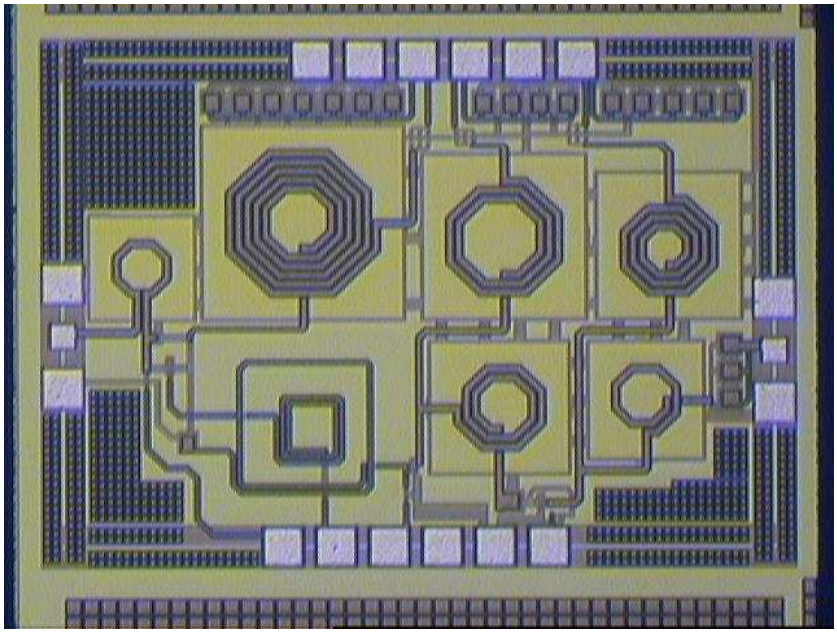


A.3 Chip implementation and Measured Results

The chip layout and photo of the UWB LNA is shown in Fig. A-13. The power supply (Vdd) is 1V. The 0.18μm (minimum) gate length was chosen to get the highest speed. The MIM (Metal-Insulator-Metal) capacitors without shield and hexagonal spiral inductors (the Q-value is below 18) are used in this work. Guard-rings are added with all elements to prevent substrate noise and interference. A shielded signal GSG pad structure is used in RF input and RF output to reduce the coupling noise from the noisy substrate. All interconnections between elements are taken as a 45° corner. The chip size is 1.418x1.013 mm^2. All connection wire are simulated by ADS momentum to extract parasitical effect.



(a)



(b)

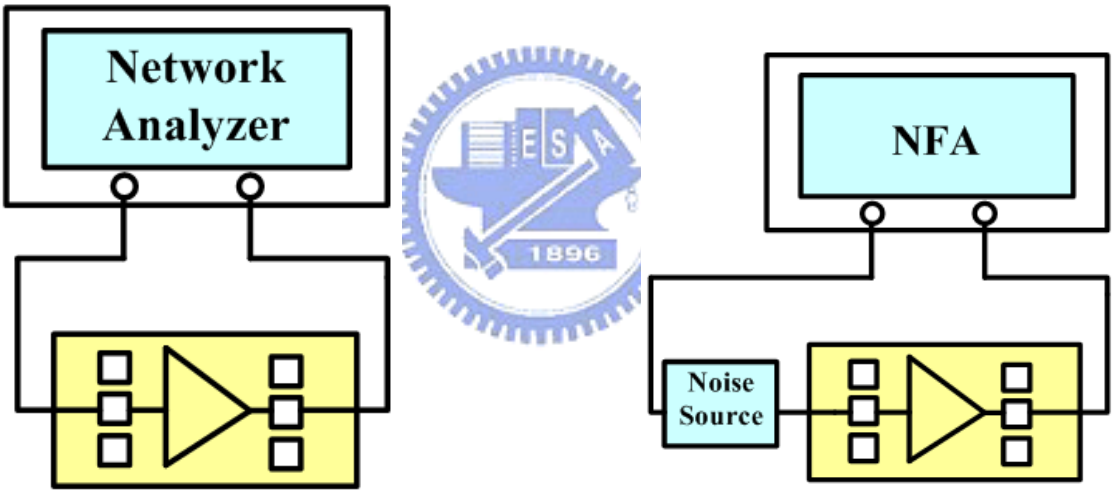
Fig. A-13(a) the chip layout (b) the chip photograph

The UWB LNA is designed for on-wafer measurement so the layout must satisfy the rules of CIC's (Chip Implementation Center's) probe station testing rules. The measurement equipments include a network analyzer (HP8510C), a noise analyzer (Agilent N8975A), a spectrum analyzer (Agilent E4407B), two signal generators, and several dc power supplies. Besides, this circuit needs two 6-pin DC PGPPGP probe and

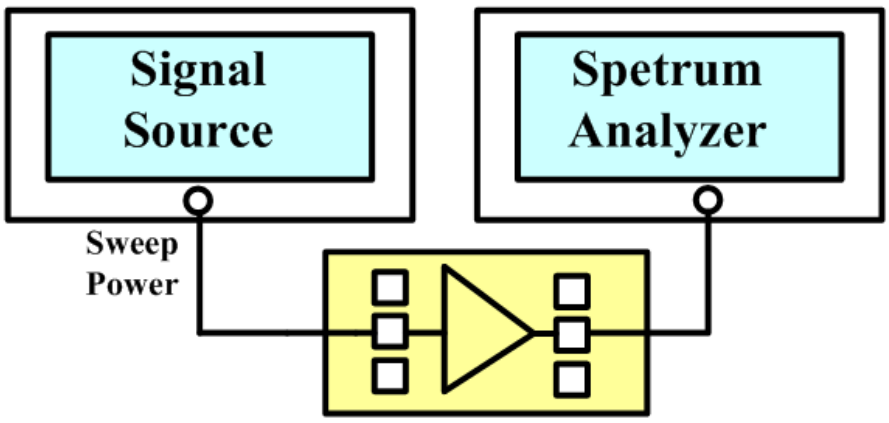
two RF GSG probes for on-wafer measurement. Fig. A-14 show the measurement setup for S-parameters, noise figure, 1dB compression point and third-order intercept point.

Angilent-8510C network analyzer

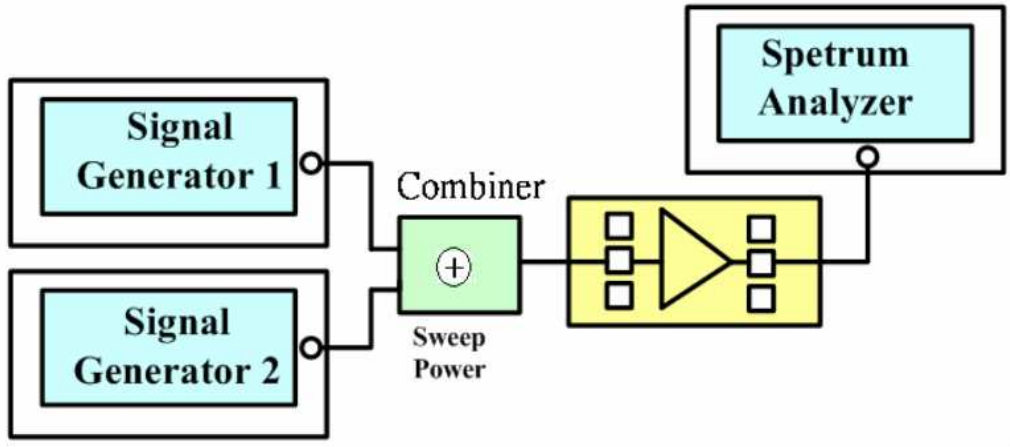
N 8975A Noise Analyzer



(a) (b)



(c)



(d)

Fig. A-14 Measurement setups for (a) S-parameter (b) noise figure (c) P1dB (d) IIP3

The S-parameter are shown in Fig. A-15(a)~(d), where the measured S11 < -8dB and S22 < -13 dB from 3.1 GHz to 10.6 GHz. The power gain (S21) is around 15dB from 3.1 to 8 GHz, except the point which produces peak value, the 3dB bandwidth is 2.9-9 GHz. The measured noise figure of 4.2-5.4 dB from 3.1 to 10.6 GHz has been presented as shown in Fig. A-16. The measured P_{1dB} are -17dBm at 3 GHz, and -13.5dBm at 9 GHz in Fig. A-17(a)~(c). The measured IIP3 are -7.5dBm at 3 GHz, and -5dBm at 9 GHz in Fig.A-17,A-18. Table A-1 summarizes the measured data of proposed wideband LNA. Table A-2 summarizes the comparison of proposed wideband LNA.

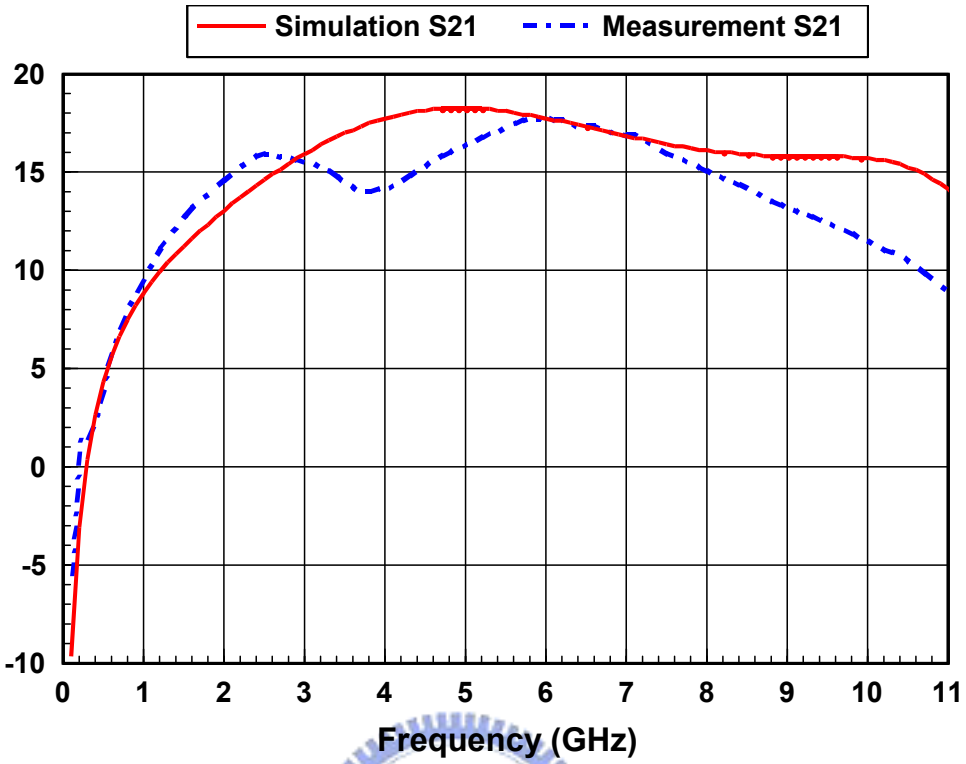


Fig. A-15 (a) Power gain vs. Frequency

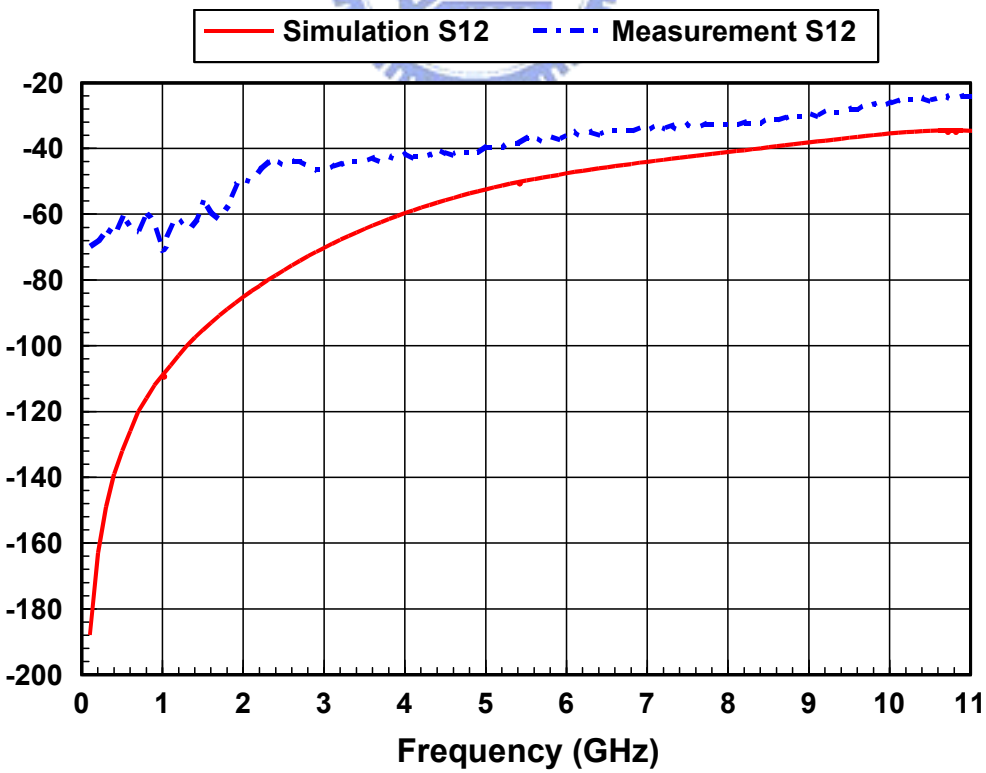


Fig. A-15 (b) Isolation vs. Frequency

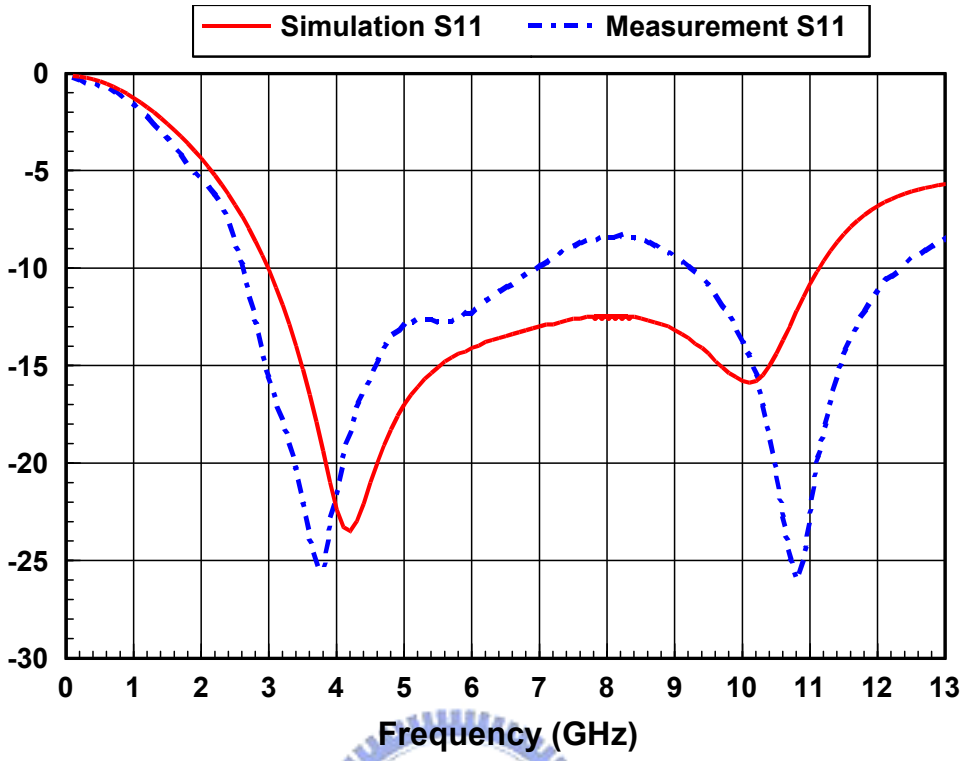


Fig. A-15 (c) Input return loss coefficient vs. Frequency

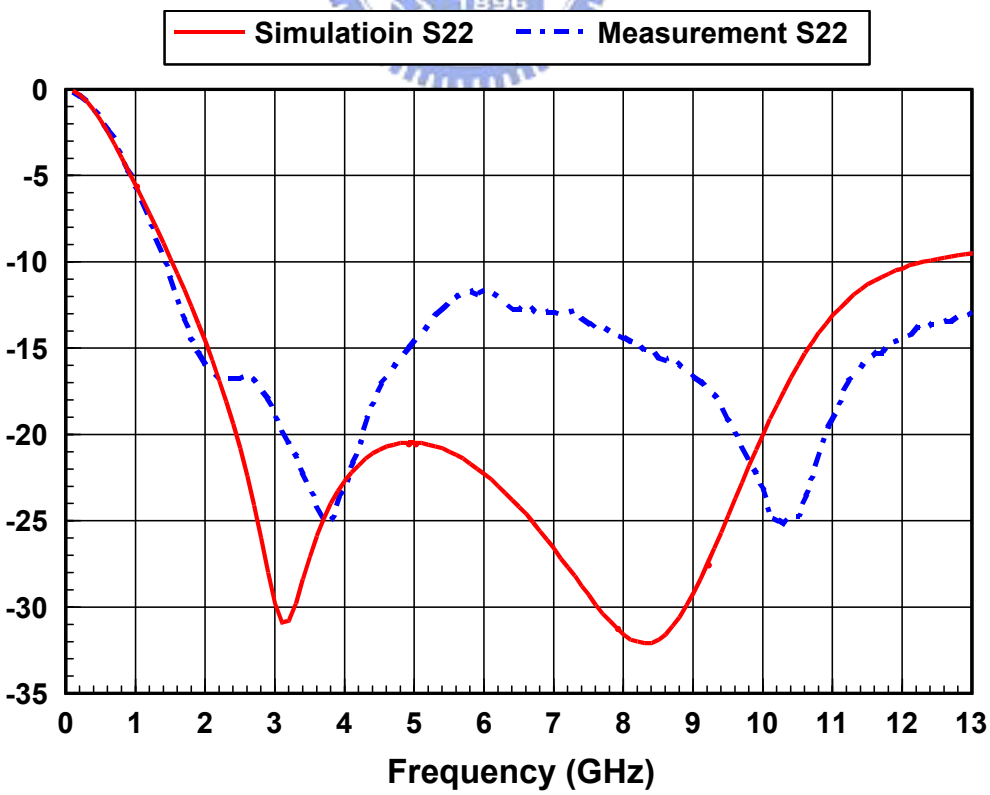


Fig. A-15 (d) Output return loss coefficient vs. Frequency

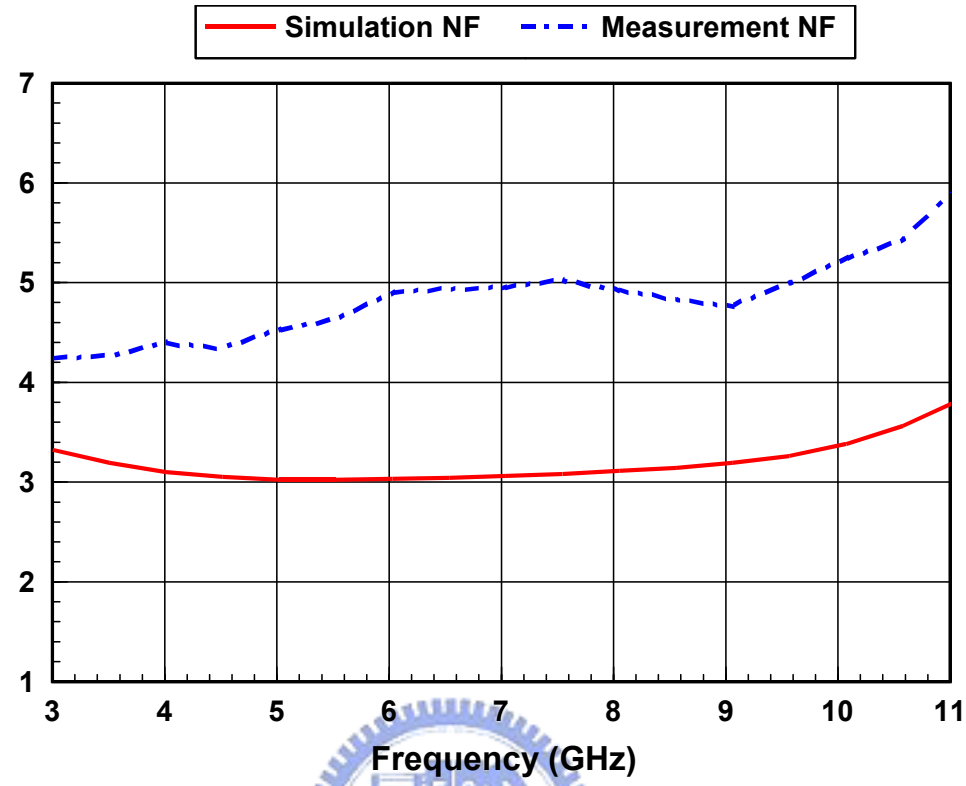


Fig. A-16 Noise Figure vs. Frequency

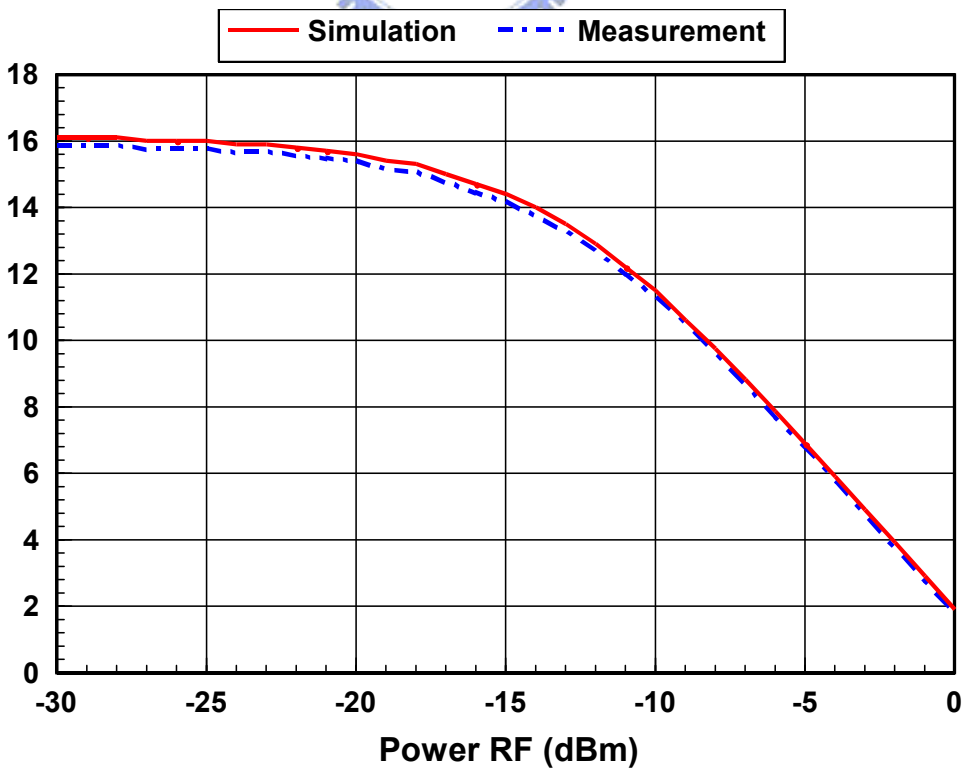


Fig. A-17 (a) P1db at 3 GHz

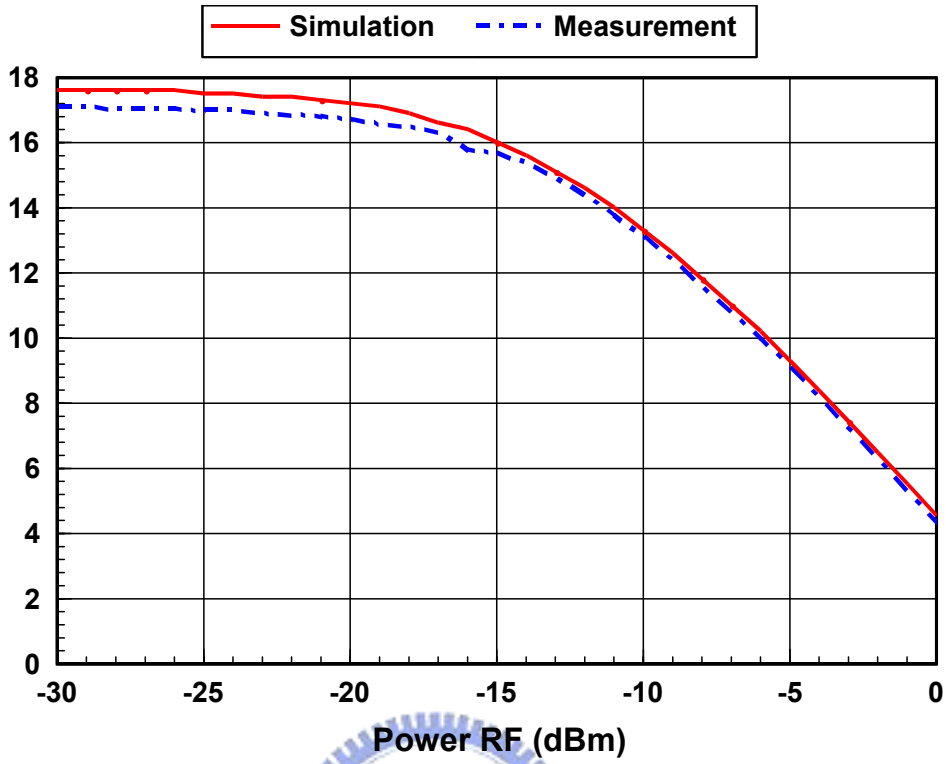


Fig. A-17 (b) P1db at 6 GHz

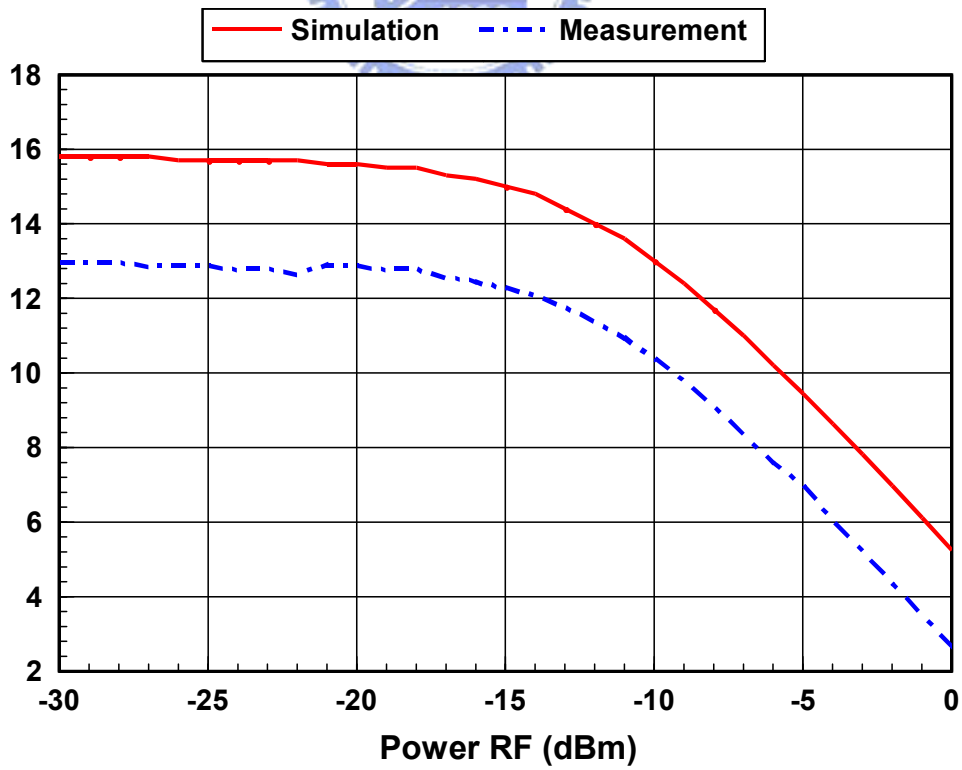


Fig. A-17(c) P1db at 9 GHz

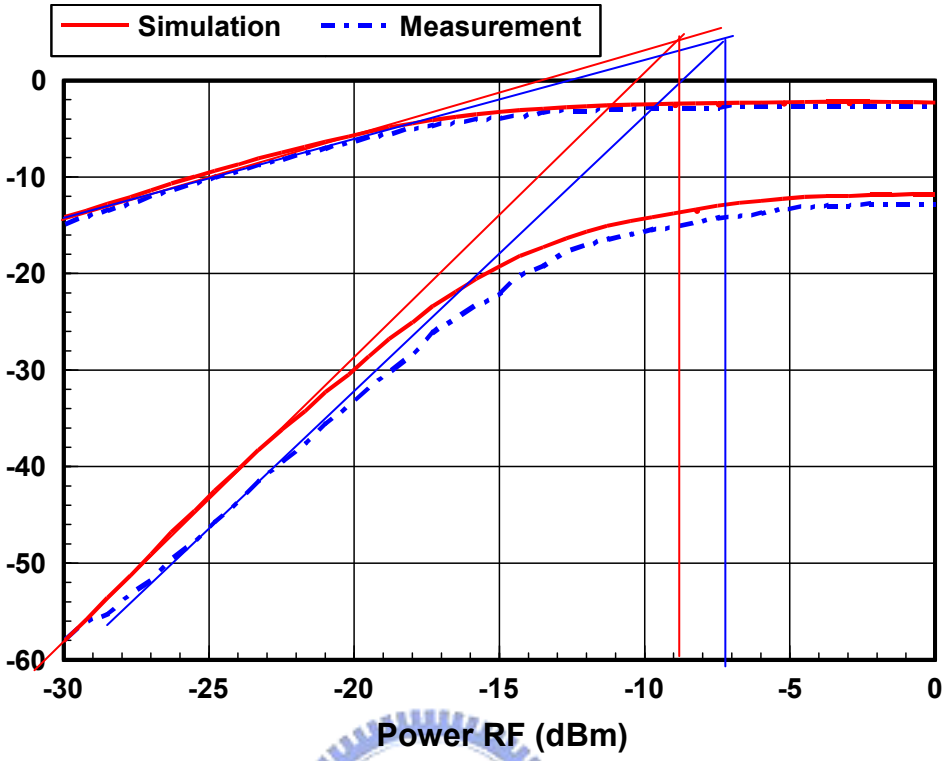


Fig. A-18 (a) IIP3 at 3GHz

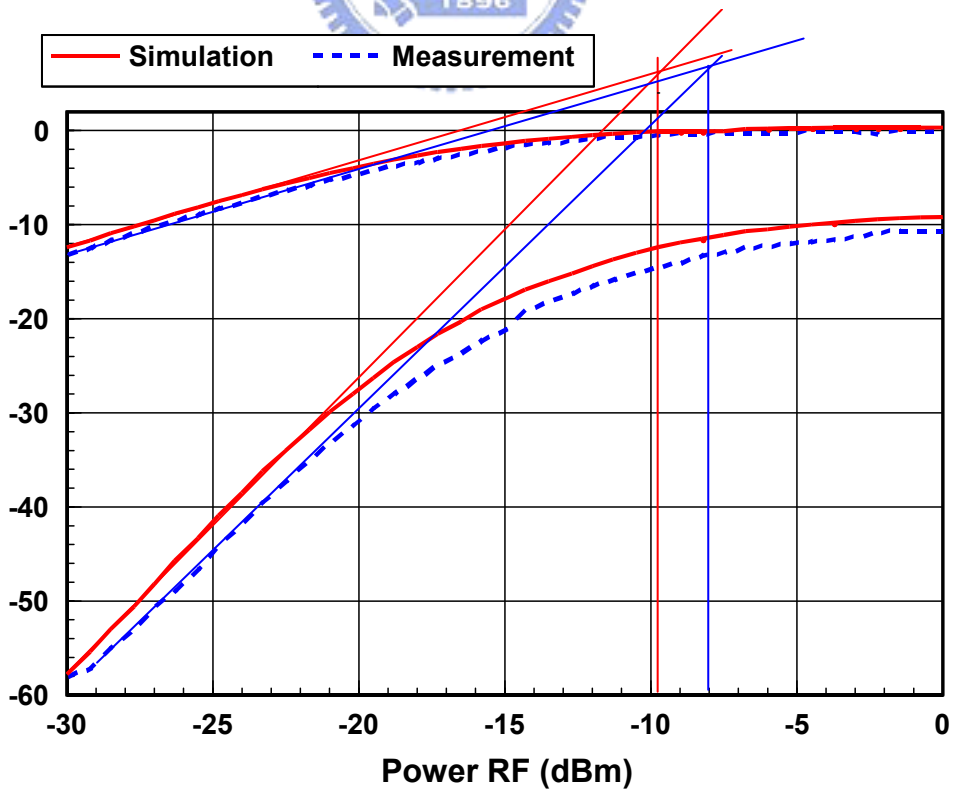


Fig. A-18 (b) IIP3 at 6GHz

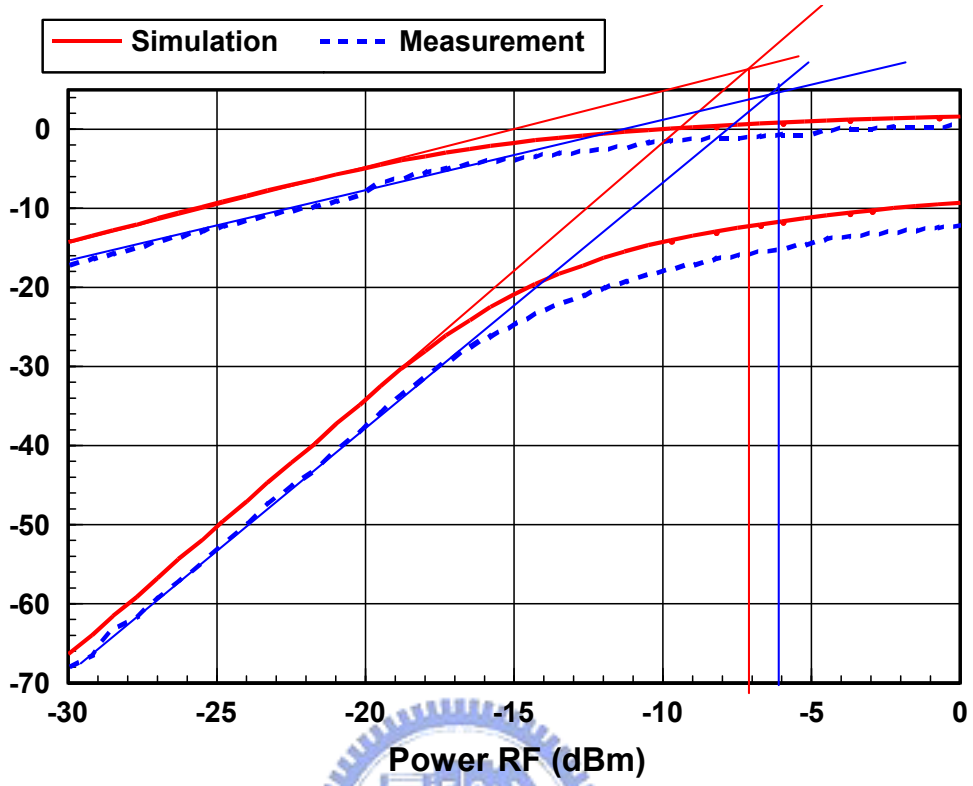


Fig. A-18 (c) IIP3 at 9GHz

Table A-1 Performance summary of Ultra-wideband LNA

Specification	**Measurement**			**Post Simulation**		
S11 (dB)	< -8			<-10		
S22 (dB)	< -10			<-10		
S21 (dB)	15 dB			16dB (flat gain)		
S12 (dB)	< -34			<-40		
Noise Figure (dB)	4.1~5.4			3.2~3.5		
P_{1dB} (dBm)	3 GHz	6 GHz	9 GHz	3GHz	6GHz	9GHz
	-17	-17	-13.5	-17.5	-18	-14.5
IIP3 (dBm)	-7.5	-11	-5	-9	-10	-7
Vdd (V)	1			1		
LNA Power (mW)	19.8			18.5		

Table A-2 The comparisons of this work and recent LNA papers.

	Tech.	BW (GHz)	S11 (dB)	S22 (db)	Flat Power Gain (dB)	NFmin (dB)	Vdd (V)	Power (mW)
This work	**0.18μm CMOS**	**3.1-10.6**	**<-8**	**<-10**	**15**	**4.5**	**1**	**19.8**
[29]	0.18μm CMOS	2-6.5	<-7.8	N/A	11.9	4.1	1.8	27
[16]	0.13μm CMOS	3.1-10.6	<-9.9	<-6.2	15.1	2.5	1.2	9
[11]	0.18μm CMOS	2.4-9.5	< -9.4	< -10	10.4	4	1.8	9
[15]	0.18μm CMOS	3.1-10.6	<-9	<-13	15.9-17.5	3.1-5.7	1.8	33.2
[17]	0.18μm CMOS	3.1-10.6	<-10	<-10	10.87-12.0	4.7	1.5	10.57

A.4 Discussion and Conclusions

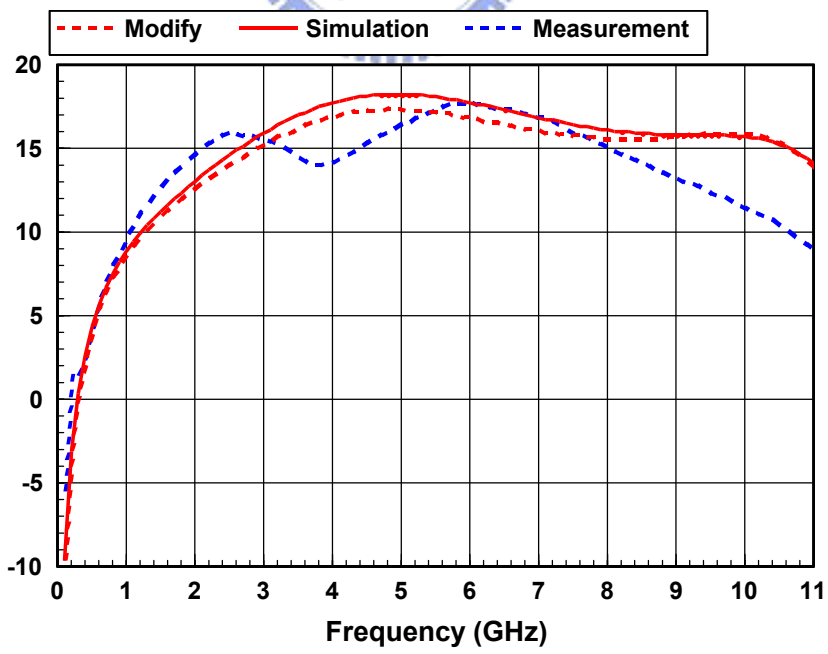


Fig. A-19 (a)The modified S21 simulation

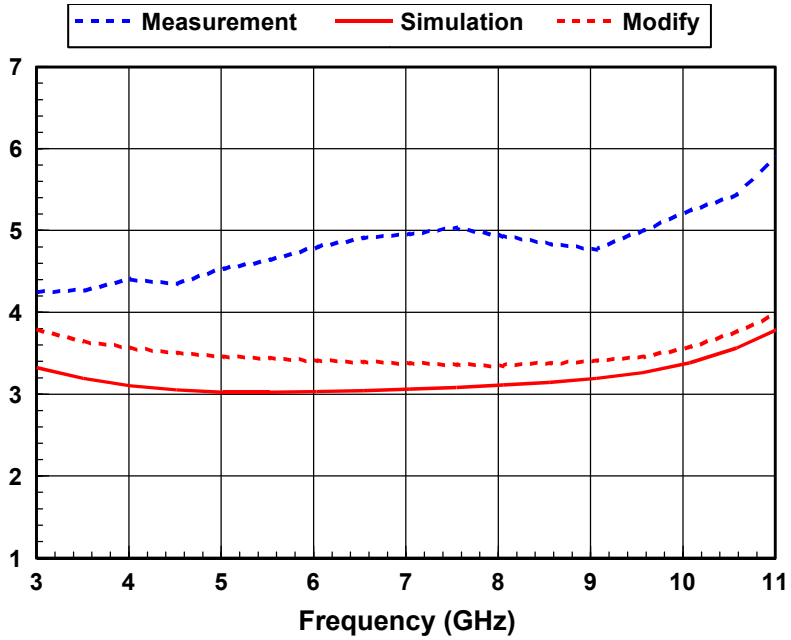


Fig. A-19 (b) The modified NF simulation

Fig. A-19 shows the modified of larger block post-simulation，which could approach the measurement a little. Besides, the S21 measurement result shows the first peak that occur at resonance shunt-peaking lower than expected, that might be due to transformer mutual coupling inductance. According to table 4-3, the phenomenon is like the condition of maximum bandwidth.

Table 4-3 Shunt-peaking summary [12].

Condition	$m=R^2C/L$	Normalized Bandwidth	Normalized peak frequency response
Maximum bandwidth	~1.41	~1.85	1.19
Max. flat frequency response	~2.41	~1.72	1
No shunt peaking	∞	1	1

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2. Yu-Shun Liao, *Yi-Shing Shen*, and Christina F. Jou,"Low Voltage Multi-Band Voltage-Controlled Oscillator for MB-OFDM UWB system", APMC, Dec, 2008 in Hong Kong.