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全積體化低電壓低功率之 CMOS
電壓控制振盪器設計

A Fully Integrated CMOS LC-VCO with
Low Voltage and Low Power

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A Fully Integrated CMOS LC-VCO with Low Voltage Low Power

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全積體化低功率低電壓之 CMOS 電壓控制振盪器設計

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摘要

在目前無線通訊技術系統快速發展之下，研發低成本、高效能、低功耗之無線射頻積體電路日益迫切。過去，因其在高頻的高效能之原因，射頻前端電路多採用矽鍺（Silicon Germanium；SiGe）BiCMOS為主流製程，然而隨著標準CMOS製程技術日趨成熟，目前採用此製程之比重已逐年提高，預計在2009年時，將約有40%的射頻收發機電路改採CMOS製程技術。由於CMOS製程早已導入基頻晶片多年，若是射頻電路也採用相同製程，將有助於晶片之整合，在成本降低、整合度提高之驅動下，將掀起無線通訊市場之另一波成長；另外，在手持行動裝置中，因射頻前端電路為最耗電之其中一部分，使得電源供應無法長效使用，尤其在輕薄短小之目標下，功耗問題往往限制了其應用發展，因此，研發更具成本效益的電路同時達到低功耗的目的，將是迫於解決的問題。本篇論文的研究焦點著重於降低電壓控制振盪器其供應電壓及功率消耗之設計，同時在低功耗程度維持一定的相位雜訊水準。利用傳統交叉對耦式的架構，以最少疊接級數中增加一對

NMOS平行於電感電容共振腔，其提供的寄生電容Cgs、Cgd與交叉對耦電晶體產生額外負電導，此負電導與等效電容可有效降低相位雜訊，另外，我們在此NMOS之基體端加上偏壓，此一步驟將與可變電容器產生共軛壓差，進而降低共模雜訊，同時，因此NMOS以閘極端連接共振腔，故不增加額外壓降及直流功耗，使在最少疊接級數中能將電壓完全供應給後級的交叉對耦電晶體，達到低電壓、低功耗目的。由量測結果(TSMC 0.18-μm 1P6M CMOS 製程)，在距離中心頻率1-MHz相位雜訊為-112.24dBc/Hz。此設計的供應電壓為0.51V，消耗功率為1 mW，其工作頻率為3.3GHz，晶片面積為0.61(μm)×0.76(μm)。

Fully Integrated CMOS LC-VCO with Low Voltage Low Power

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Abstract

As the advancement of wireless communication system growing rapidly. Development of radio frequency (RF) integrated circuits in low cost, high performance and low power consumption is more and more imminently. In the past, the RF front-end circuits are made by SiGe BiCMOS process technologies due to its high performance in high frequency. However, with the standard CMOS process technology getting proficient, RF front-end circuits made by CMOS process are more and more popular. As far as the actual applications are concerned, the RFICs are power-hungry devices which cause the battery life time could not be extended effectively. The problem of power consumption further restricts the applications in wireless electronic devices, especially in the demands of light, thin, short and small devices. Therefore, development of RFIC more efficient in cost and low power consumption is an emergent issue to solve. This thesis focuses on the design of low supply voltage and low power consumption and maintains comparable level of phase

noise simultaneously. Using a conventional NMOS cross-coupled LC-VCO architecture which has the least stages stacked in vertical could be reduced the supply voltage. By adding a proposed NMOS pair which paralleled the LC-tank, the parasitic capacitances Cgs, Cgd of the proposed NMOS pair generate an additional negative conductance, as a result, the phase noise can be degrade effectively in low power, low supply voltage operation level. Besides, the bodies of proposed NMOS pair are biased, which generate an opposite voltage drop as compared with varactors. As a result, the common mode noise is reduced. Eventually, the goals of low power consumption and low supply voltage can be achieve due to most of the supply voltage feed the cross-couple NMOS and the added NMOS pair take no voltage drop. The proposed low voltage, low power LC-VCO is implemented by TSMC 0.18-μm 1P6M CMOS process. With only 0.51 V bias, the power consumption of the proposed LC-VCO is 1 mW. The phase noise is -112.24 dBc/Hz from 1 MHz offset frequency at 3.3GHz and the chip size of 0.61 (μm) × 0.76 (μm).

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Chapter 1 *Introduction*

1.1 Background and Problems

In recent years, the development of several kinds of new communication technique is expected to provide high data rate, wide range and high speed communications in wireless area networks [1]. As the advancement of wireless communication system, transmission distance and data rate growing rapidly, the design of high performance radio frequency (RF) transceivers is an aspiration target.

At present, RF transceivers have been widely implemented by SiGe, GaAs or HBT processes due to the high performance at high frequency. However, the system cost will remain high because that those processes are not compatible with the silicon process and let along of a system on a chip (SOC) solution for the present time. Thus, the CMOS technology is an attractive process to meet the low cost requirement in RF transceivers.

Among function blocks of a RF transceiver as shown in Figure 1.1, the voltage controlled oscillator (VCO) is used to provide clean, stable, and precise carrier signals

for frequency translation in wireless transceivers. Because the purity (phase noise) of local signal which generated by the VCO will dominate the performance of the system, the design of high performance VCO is an urgent and momentous subject. In the design of VCOs, there are several common goals, such as low phase noise, low power consumption, low cost, satisfactory output power, and sufficient tuning range. Mostly, the low phase noise is a critical specification of VCOs for actual practice. As the shrinking of chip size and the growing demand of portable applications and power-efficient issues, the low voltage and low power design is another important target of VCOs. However, according to the well-known Leeson's model of phase noise [2], the phase noise and power consumption usually formed a key tradeoff in the circuit design of VCOs. Hence, how to design a VCO that satisfies the requirements described above is a challenging issue.

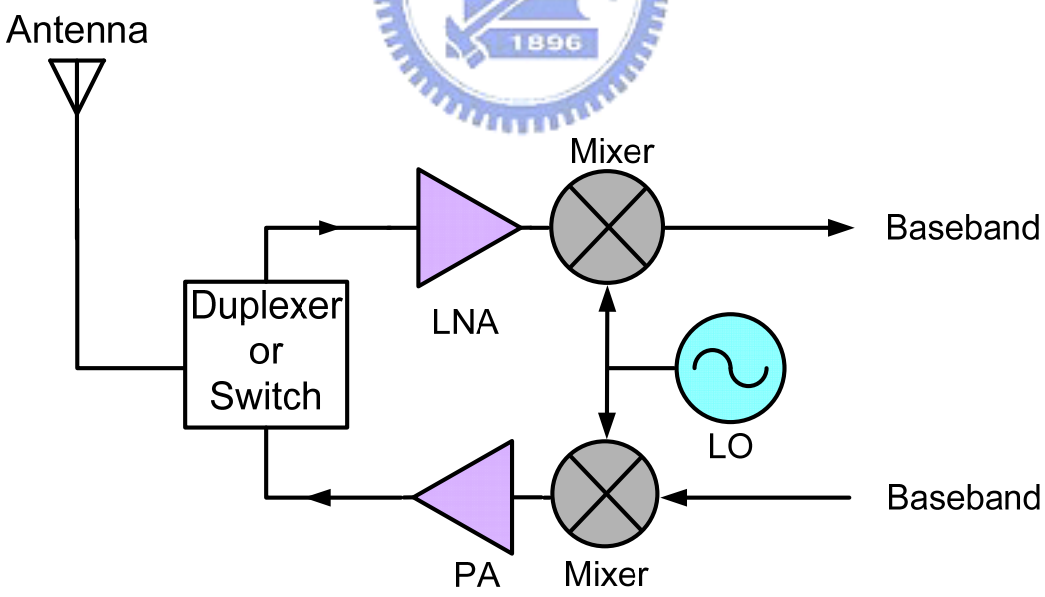


Figure 1.1 Block diagram of a typical RF front-end transceiver

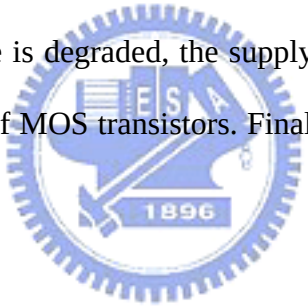
1.2 Related Works and Motivation

In nowadays, the digital and baseband circuits can be implemented in CMOS process. However, the analog and RF integrated circuits are still need the special processes to accomplish. In the RFICs, due to the crucial function in wireless transceivers and power-aware demand, the development of high performance, low power and low cost VCO is an urgent demand. For CMOS process, due to the substrate loss of bulk is avoidless in silicon based technology, the Q factor of on-chip inductors and capacitors have restricted improvement to the phase noise performance in a VCO [3]. In order to achieve low phase noise in a VCO, the complementary NMOS-PMOS cross-coupled pair architecture is employed to ease the phase noise for the reasons of the tank amplitude is twice that of NMOS or PMOS only topologies and the complementary one has more symmetry output waveform [4]. But the supply voltage can not be reduced due to the much more transistors are stacked in the topology. [5] uses a harmonic tuned (HT) method to suppress the harmonic frequency of the circuit by adding an external circuit. This method can reduce the phase noise effectively, but it also increases both the chip area and power consumption.

In low power topics, reducing supply voltage is an effective method, but mostly, the supply voltage is restricted by the threshold voltage of MOS transistors. Moreover, once the supply voltage is reduced, the signal amplitude of LC-tank will be limited in turn, further decreases the signal-to-noise ratio (SNR) and increases the phase noise of VCO. In [6-7], the current-reuse method may be an effective method to reduce the power consumption, but the phase noise performance is affected by the asymmetric structure. In conclusion, how to obtain a comparable phase noise effectively at the low power level becomes a bottleneck to design.

In this thesis, we propose a fully integrated, low voltage and low power 3.3

GHz LC-VCO by the negative conductance enhancement and common mode noise reduction methods in a conventional NMOS cross-coupled VCO. In the VCO design, achieving the goal of low power or low voltage may not be a difficulty. The real problem is the phase noise performance is considerably poor at low power level. On the other hand, the bottleneck is how to improve the phase noise of VCOs at low voltage or low power operation. The negative conductance enhancement method employs an NMOS pair paralleled the LC-tank, the parasitic capacitances of the NMOS pair will increase the negative conductance of the VCO. In the analysis of Q factor, the raise of negative conductance will degrade the phase noise effectively. The common mode noise reduction method uses the contrary placement of NMOS pair and varactors and then the VCO's gain can be reduced. Ultimately, the phase noise is reduced. Once the phase noise is degraded, the supply voltage can be reduced and is near to the threshold voltage of MOS transistors. Finally, the low power consumption can be achieved.



1.3 Thesis Organization

There are five chapters of the thesis. Chapter 2 deals with the basic concepts and parameters of VCOs. In chapter 3, some advanced popular VCO topologies are reviewed. In chapter 4, we proposed a design of low voltage and low power consumption CMOS LC VCO with the simulated and measured results. Chapter 5 conclusion is drawn.

Chapter 2 *Design Basics of CMOS VCO*

2.1 Fundamental Characteristics of LC VCO

In general, the VCO is a spontaneous circuit which starts up by inherent noise and retains a stable oscillation by positive feed back and negative resistance. The VCO is used as a local oscillator that generates a precise periodic waveform for frequency up and down translation in mixer. In the analysis of VCOs, the negative resistance model (one-port network) is widely used. As shown in Figure 2.1, the oscillator is treated as two parts that one is an active circuit part and the other is resonant circuit part.

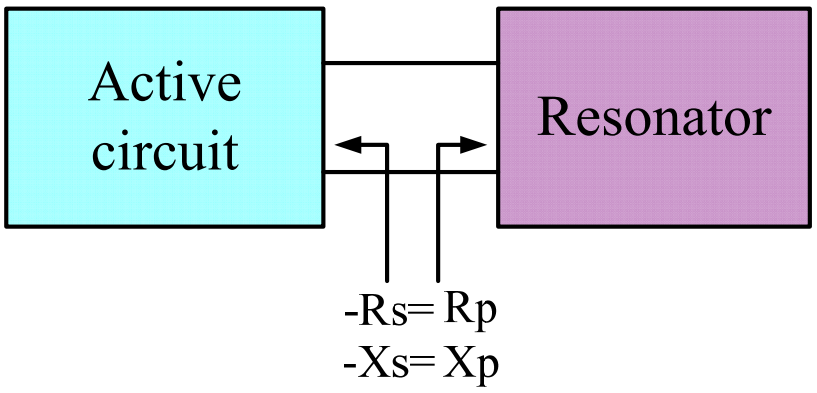


Figure 2.1 Negative resistance model of a VCO.

When the resonator or a LC-tank resonates at a target frequency, an existed loss, represented by an equivalent resistance Rp (mostly comes from the inductor), reduces the oscillated amplitude and results in operation stop. Therefore, the active circuit provides an equivalent negative resistance -Rs to compensate the energy loss. As shown in Figure 2.2, the negative resistance $-2/g_m$ needs to satisfy the condition that

$$2/g_m \geqq Rp \tag{2-1}$$

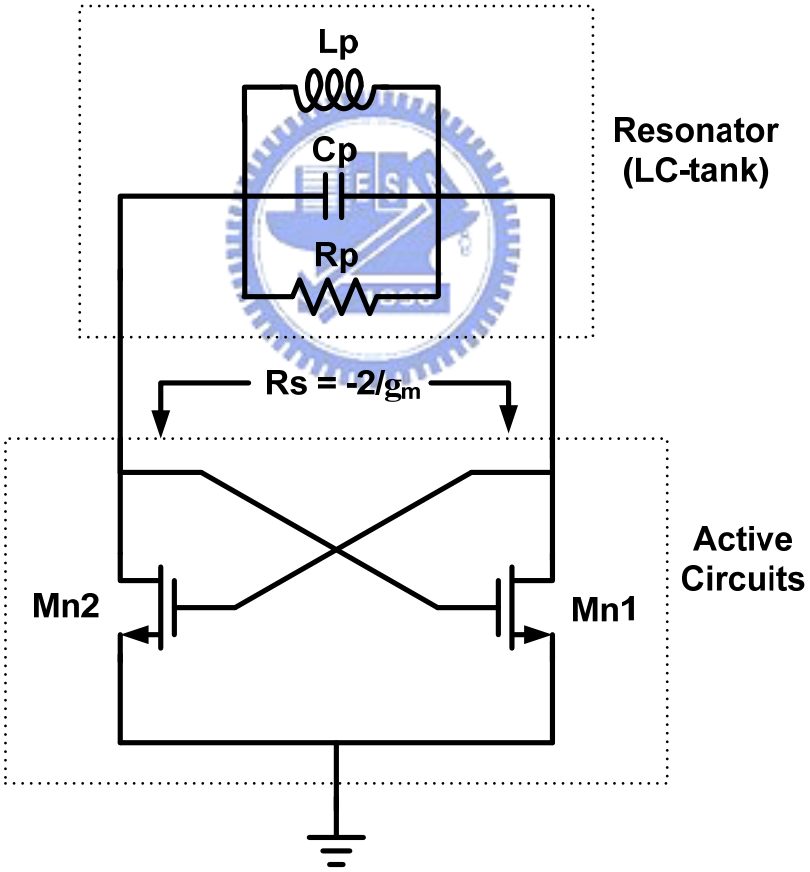


Figure 2.2 Negative resistance model of NMOS cross-coupled LC VCO

The feedback model (one-port network) is also a popular method and is widely used in the oscillator analysis. Figure 2.3 shows the block diagram of the feedback model. The transfer function of the output/input is given as

$$\frac{Xo(s)}{Xs(s)} = \frac{A(s)}{1 - A(s)H(s)} \tag{2-2}$$

where s is complex frequency. The oscillation will keep in certain amplitude if the open loop gain

$$Ao(s) = A(s)H(s) \tag{2-3}$$

with

$$\left|Ao(\omega_0)\right| = 1 \quad \& \quad \angle Ao(j\omega_0) = 0 \tag{2-4}$$

This is the so-called Barkhauen criterion, where ω_0 is the radian frequency of oscillation. The Barkhauen criterion of the feedback circuit is a necessary condition but not a sufficient condition. Actually, the loop gain was chosen to be at least two or three times.

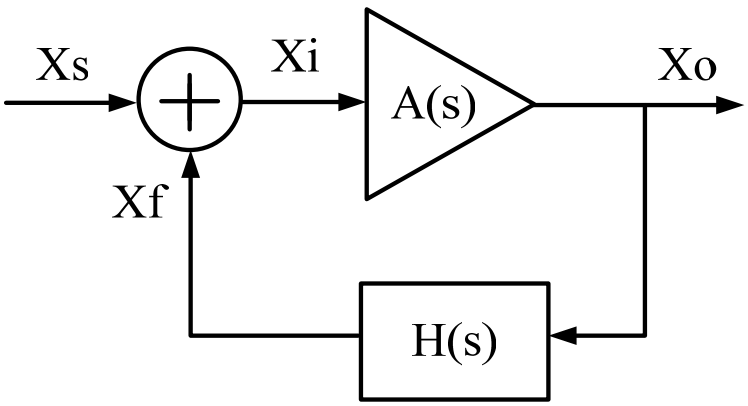


Figure 2.3 Feedback model of a VCO.

2.2 LC Tank

Figure 2.4 shows the series resonant circuit and the parallel resonant circuit with input impedance Zin given by, respectively,

$$Zin = R + j\omega L + \frac{1}{j\omega c} \quad \text{(series resonant circuit)} \tag{2-5a}$$

$$Zin = \frac{1}{1/R + 1/j\omega L + j\omega C} \quad \text{(parallel resonant circuit)} \tag{2-5b}$$

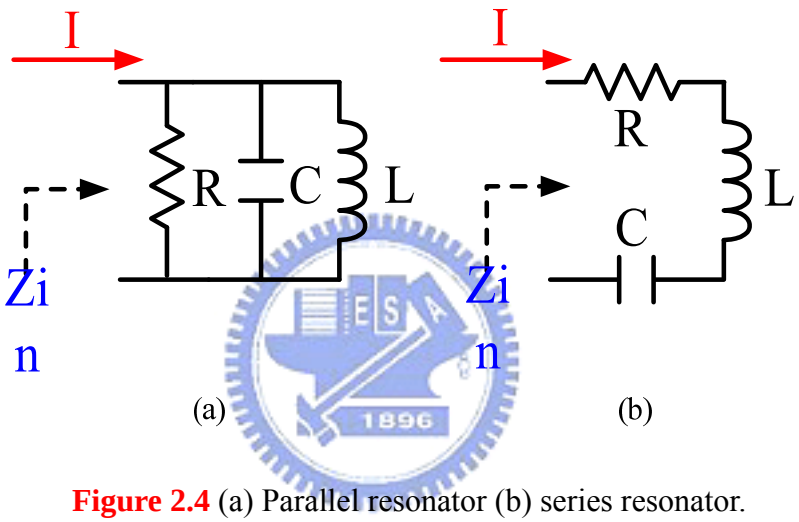


Figure 2.4 (a) Parallel resonator (b) series resonator.

The energy stored in the L and C are given by, respectively,

$$W_L = \frac{1}{4}L\left|I^2\right|, \quad W_C = \frac{1}{4}\frac{\left|I^2\right|}{\omega^2 C} \tag{2-6}$$

The resonance will occur when

$$W_L = W_C \tag{2-7}$$

The input impedance and oscillating frequency are

$$Zin = R \tag{2-8}$$

$$\omega = \omega_0 = \frac{1}{\sqrt{LC}} \tag{2-9}$$

From the analysis of LC-tank, the Q (quality) factor is given as

$$Q = \omega \frac{average\ enegy\ store}{average\ energy\ loss\ \ per\ cycle} \tag{2-10}$$

Therefore the Q factor of the resonant circuit is

$$Q = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RC} \quad \text{(series resonant circuit)} \tag{2-11a}$$

$$Q = \frac{R}{\omega_0 L} = \omega_0 RC \quad \text{(parallel resonant circuit)} \tag{2-11b}$$

2.3 Phase Noise

One of the most important characteristic of VCOs is phase noise which represents the purity and stability of the output signal of a VCO. The signal to noise ratio (SNR) is also affected by phase noise greatly in a transceiver. In light of ideal case, the output spectrum of an oscillator has only one impulse at the fundamental frequency as shown in Figure 2.5(a). In practice, however, the output spectrum of an oscillator is not so clear due to the spurious signals come from its harmonics or intermodulation products. Then the noise skirts which spread the fundamental output tone at oscillated frequency in a VCO, as shown in Figure 2.5(b).

An ideal sinusoidal wave form is defined as

$$V(t) = A\cos(\omega_0 t + \phi) \tag{2-12}$$

where A is the oscillated amplitude, ω_0 is oscillated frequency and ϕ is a random phase. The waveform function should be

$$V(t) = A(t) f(\omega_0 t + \phi(t)) \tag{2-13}$$

where the oscillated amplitude $A(t)$ and phase $\phi(t)$ are functions of time t, the function f has the period of 2π. The jitter can cause the amplitude fluctuation and phase fluctuation in a VCO. Mostly, the amplitude fluctuation can be neglected due to

the voltage limiter or nonlinearity effect of the circuits, but the phase fluctuation can not.

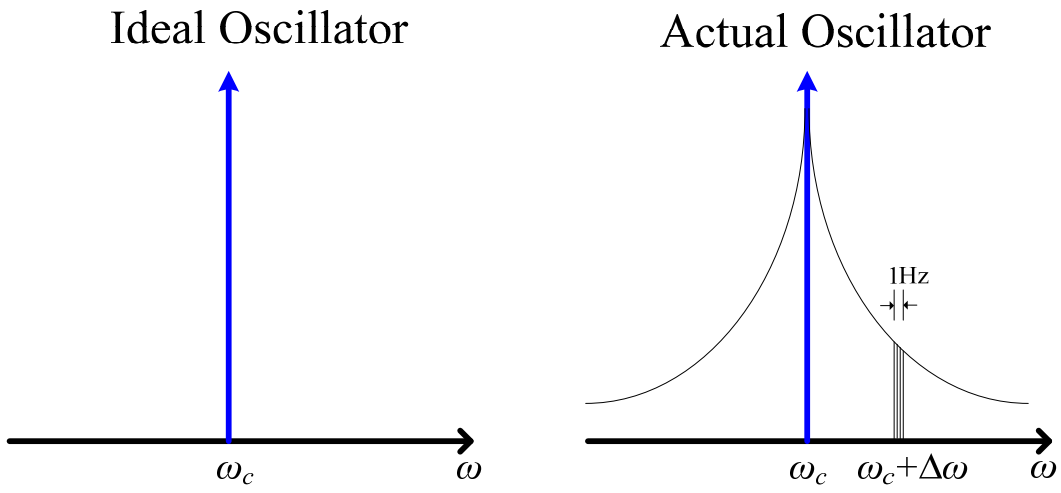


Figure 2.5 Output spectrum of ideal and realistic oscillators.

There are several methods to describe the frequency fluctuation of VCOs. Here, we briefly present some works about phase noise model, one is D. B. Leeson and the other is A. Hajimiri.

2.3.1 Leeson's Model

As the empirical method, the phase noise of signals is usually expressed in the description that relative to the carrier power per Hertz of bandwidth (dBc/Hz). The phase noise is typical expressed as [2]

$$L(\Delta\omega) = 10\log\left[\frac{P_{SSB,1Hz}(\omega_0+\Delta\omega)}{P_C}\right] \quad (dBc/Hz) \tag{2-14}$$

where $\Delta\omega$ is the offset frequency form the carrier frequency, $P_{SSB,1Hz}(\omega_0+\Delta\omega)$

represents the single sideband (SSB) power at a frequency offset of $\omega_0 + \Delta\omega$ from the carrier with a measurement bandwidth of 1Hz, and P_C is the carrier power, as shown in Figure 2.6.

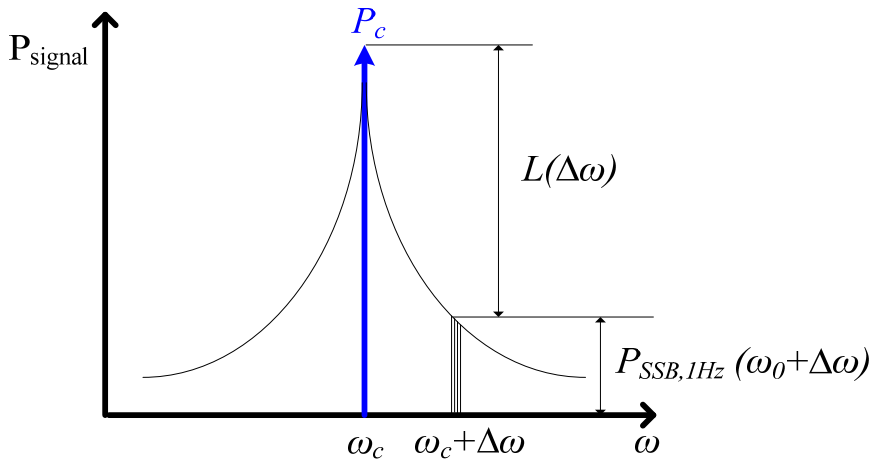


Figure 2.6 The diagram of the oscillator power spectrum around the fundamental.

In 1966, D. B. Leeson proposed a model to describe the phase noise, this model is expressed as [2],

$$L(\Delta\omega) = 10\log\left\{\frac{2FKT}{P_S}\cdot\left[1+\left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right]\cdot\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right\} \qquad (2\text{-}14)$$

where F is the excess noise factor, K is the Boltamann's constant, T is the absolute temperature, P_S is the average power consumption of resonator, ω_0 is the oscillator frequency, Q_L is the loaded Q, and $\Delta\omega_{1/f^3}$ is the corner frequency. Figure 2.6 does not express the actual shape of a SSB spectrum for a VCO, the actual SSB phase noise often approximate to the diagram shown in Figure 2.7, which shows the typical regions of phase noise of VCOs from the Lesson's phase noise model. According to Figure 2.7, the corner frequency $\Delta\omega_{1/f^3}$ of $1/f^3$ phase noise should be equaled to the corner frequency $\Delta\omega_{1/f}$ of $1/f$ phase noise of a device. However, after the

experimental steps, the $\Delta\omega_{1/f^3}$ is not equal to the $\Delta\omega_{1/f}$ in an actual oscillator. The $\Delta\omega_{1/f^3}$ is a kind of empirical result without any physics significance. The power spectral density of flicker noise of active devices (MOS) is proportional to $1/f$. This results in the $1/f^3$ region and closes the oscillated frequency.

From equation (2-14), increasing the Q factor of a LC-tank and P_S can improve phase noise effectively, but the Q factor and P_S are usually restricted by the poor-Q inductor in CMOS process and low power applications respectively.

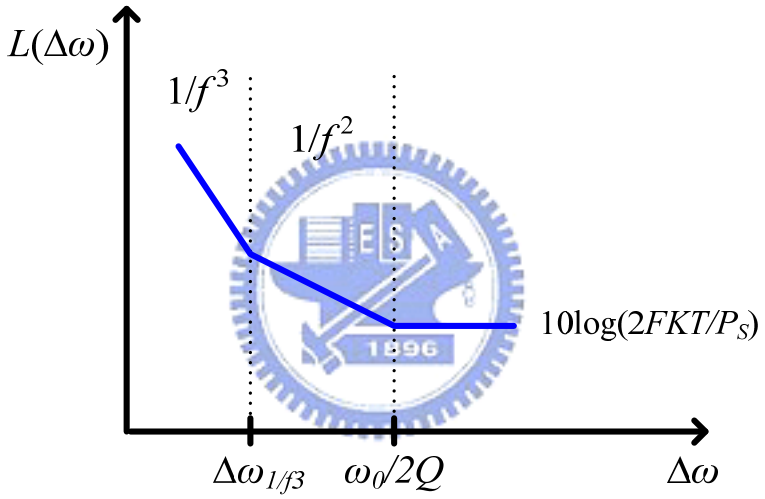


Figure 2.7 Phase noise curve of Lesson's model.

Leeson's phase noise model includes an empirical factor F in the description. Therefore it can not analyze the phase noise of a VCO precisely. A more accurate model is proposed by Hajimiri and T. Lee in 1998 [8].

2.3.2 Hajimiri Model

The Hajimiri model introduces impulse sensitivity function (ISF) to analyze the phase noise. This model can explain the mechanisms that how the flicker noise upconvert to phase noise in a VCO. An oscillator can be modeled as a system with n noise source inputs and two outputs that are the instantaneous amplitude $A(t)$ and excess phase $\Phi(t)$ of an oscillator. Noise inputs to the system are in the form of current sources injecting into circuit nodes and voltage sources in series with circuit branches. For each noise input source, both systems can be considered as single-input, single-output systems. Then the time and frequency-domain fluctuations of $A(t)$ and $\Phi(t)$ can be characterized as the two equivalent systems shown in Figure 2.8.

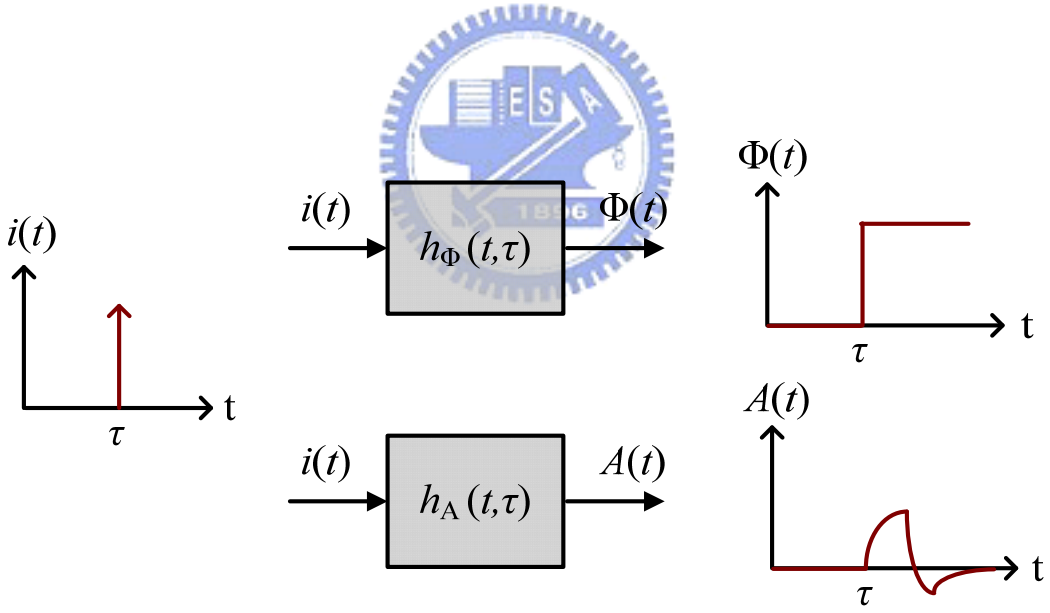


Figure 2.8 Phase and amplitude impulse response model.

A time varying impulse response can be written as [8]

$$h_{\Phi}(t,\tau)=\frac{\Gamma(\omega_0\tau)}{q_{\max}}u(t-\tau) \tag{2-15}$$

where q_{max} is the maximum charge displacement across the capacitor and $u(t)$ is the

unit step, τ is the time when the impulse is injected and $\Gamma(x)$ is the impulse sensitivity function (ISF). Using the relevant Fourier series, then the $\Gamma(\omega_0\tau)$ can be expanded as

$$\Gamma(\omega_0\tau) = \frac{C_0}{2} + \sum_{n=1}^{\infty} C_n \cos(n\omega_0\tau + \theta_n) \tag{2-16}$$

where the coefficients C_n are real and θ_n is the phase of nth harmonic of the ISF.

The phase noise depends on the time when the noise current is injected. In Figure 2.9 (a), the impulse at the zero crossing causes phase noise only and does not cause amplitude noise. As shown in Figure 2.9 (b), the impulse as the peak causes amplitude noise only. The amplitude of impulse response of phase depends on the time when the impulse is injected. The increment of amplitude is $\Delta V = \Delta Q/C$ and the timing of the zero crossings does not change. In this system, the phase displacement depends on that the impulse is applied, the system is time variant.

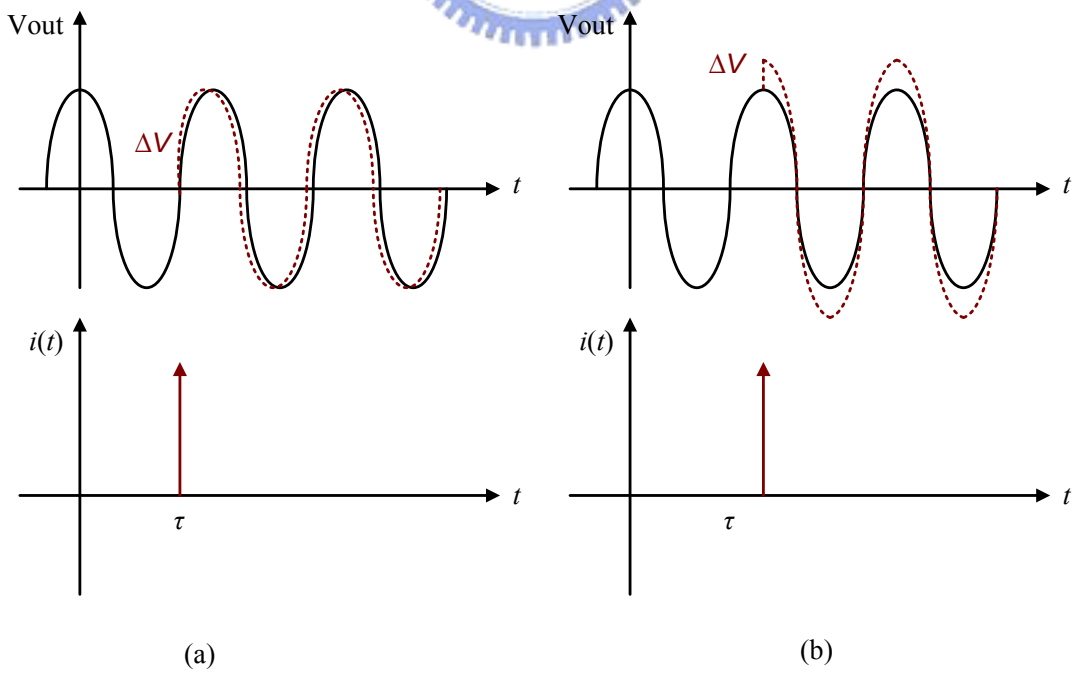


Figure 2.9 Waveforms for impulse excitation.

For a given impulse sensitivity function oscillator, the excess phase due to the noise current can be obtained

$$\Phi(t) = \int_{-\infty}^{\infty} h_{\Phi}(t,\tau) \cdot i(t)\, d\tau = \frac{1}{q_{\max}} \int_{-\infty}^{1} \Gamma(\omega_0 \tau) \cdot i(t)\, d\tau \qquad (2\text{-}17)$$

where the coefficients C_n are real and θ_n is the initial phase of nth harmonic of the ISF, $q_{max} = CV_{max}$, V_{max} is the largest amplitude of the VCO. If the oscillator take account of white noise $\overline{i_n^2}/\Delta f$, then the SSB phase noise is

$$L(\Delta\omega) \approx 10 \log \left(\frac{\overline{i_n^2}/\Delta f}{2q_{\max}^2} \cdot \frac{\Gamma_{rms}^2}{\Delta\omega^2} \right) \qquad (2\text{-}18)$$

and the SSB phase noise due to flicker noise is

$$L(\Delta\omega) \approx 10 \log \left(\frac{\overline{i_n^2}/\Delta f \, C_0^2}{8q_{\max}^2 \Delta\omega^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \right) \qquad (2\text{-}19)$$

To general belief, the phase noise *1/f*^{3} is identical to the flicker noise *1/f*. The equation (2-19) indicates that the *1/f*^{3} region can be reduced once the Fourier coefficient C_0 is diminished. On the other hand, the meaning of diminished C_0 is the more symmetrical output waveform is achieved in a VCO. The Hajimiri model provides the exhaustive analysis on phase noise. This model can help the designer to understand the noises from each source and how they affect the phase noise. Finally, the designer can suppress the phase noise in an efficient way.

Chapter 3 *Advanced Design of Related Works*

3.1 Basic CMOS LC VCO Topologies

Figure 3.1 (a)-(d) show the prototypes of conventional CMOS LC VCOs published in [2], [8-10]. Topologies in Figure 3.1 (a) with a tail current source and in Figure 3.1 (b)-(c) with top current sources have the advantage of less supply voltage due to less stages are stacked in vertical. Because they are not all control by the DC bias once the current sources are employed in Figure 3.1 (a)-(c), the VCOs could reduce the sensitivity of the proposed circuit gain versus the supply voltage effectively. But, it means that the more supply voltage may be needed. Furthermore, the current sources will down convert the noise around $2f_0$ by channel length modulation to the phase noise and degrades the phase noise.

Because of the flicker noise performance in PMOS is better than that in NMOS, the cross-coupled PMOS LC VCO were usually employed as the active circuit as shown in figure 3.1 (b). The difference between Figure 3.1 (a) and Figure 3.1 (c) is that the output DC level is close to supply voltage and close to ground respectively.

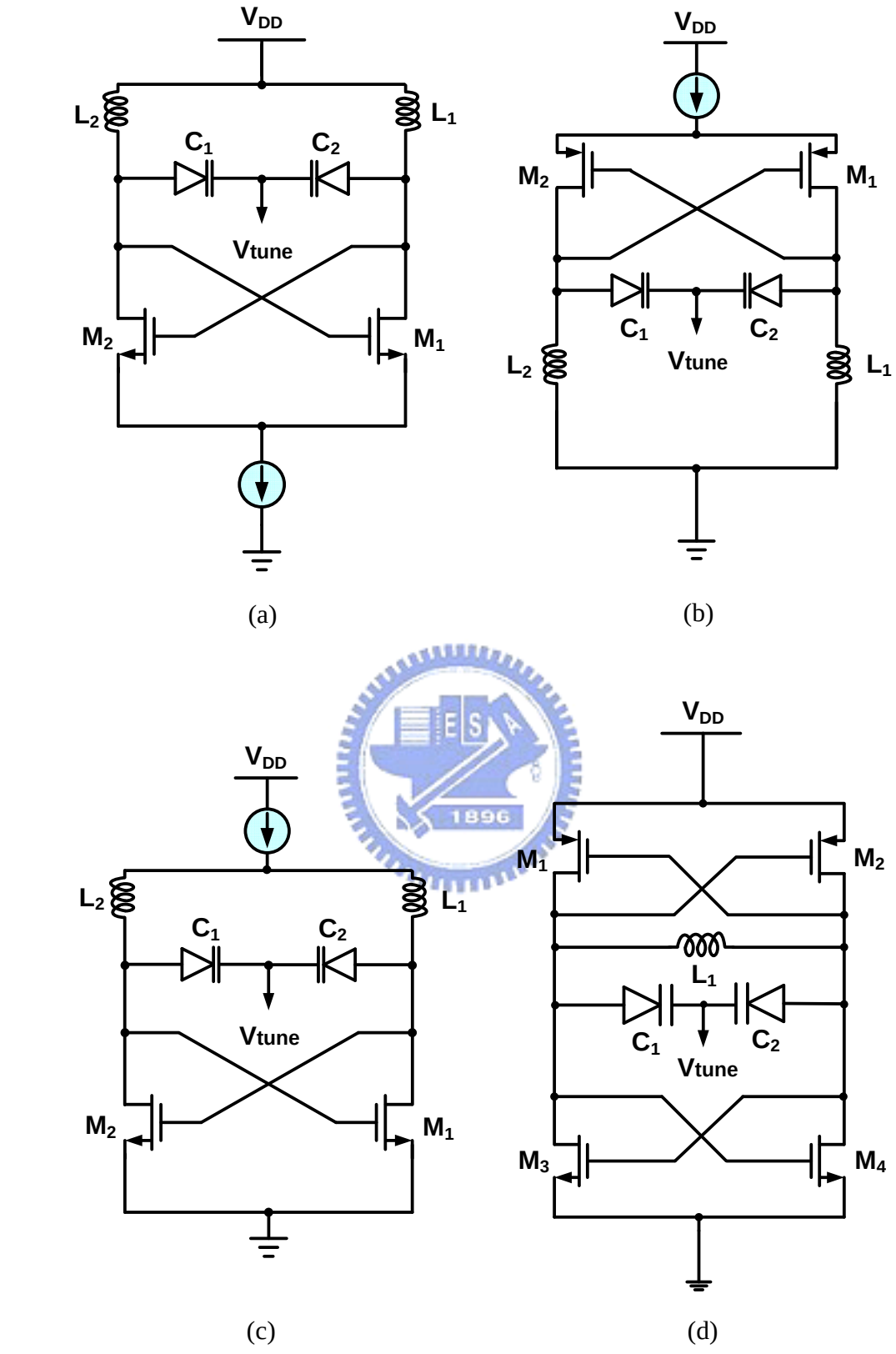


Figure 3.1 (a) NMOS cross-coupled LC VCO with a bottom current source. **(b)** PMOS cross-coupled LC VCO with a top current source. **(c)** NMOS cross-coupled LC VCO with a top current source. **(d)** Complementary cross-coupled LC VCO.

In Figure 3.1 (d), the complementary LC VCO not only has the more symmetric topology which could suppress the $1/f$ noise up-conversion by its symmetric waveforms but also generates the output waveforms which are twice of that in NMOS or PMOS only architectures, therefore the complementary architecture has the better phase noise performance. However, comparing to another topologies in Figure 3.1, the complementary one consumes more voltage headroom and the larger size of transistors are needed to get enough transconductance to loose the overdrive voltage at low voltage operation, which results the increase of parasitic capacitance and decrease of tuning range. The LC VCOs in Figure 3.1 (a-c) have the related larger voltage headroom, the wider tuning range and the smaller size of transistors to start the oscillation than that in Figure 3.1 (d). But the cost is that the $AM-FM$ conversion from the current source reducing the phase noise performance.

Figure 3.2 shows the LC VCO of two differential frequency tuning tanks [11-12]. Four varactors are used for frequency tuning instead of two varactors which are employed in conventional design. When using varactors with the contrary polarities, the common mode voltage for V+ and V- are cancelled out. The varactors in Figure 3.2 are accumulation mode MOS varactors [13]. Tuning of all LC-tank oscillators may be achieved by tuning its effective capacitance with an appropriate bias control voltage (V+ and V-). Since CMOS junction capacitors have relatively poor Q, it is advisable to use as much junction capacitance as necessary to achieve the desired tuning range.

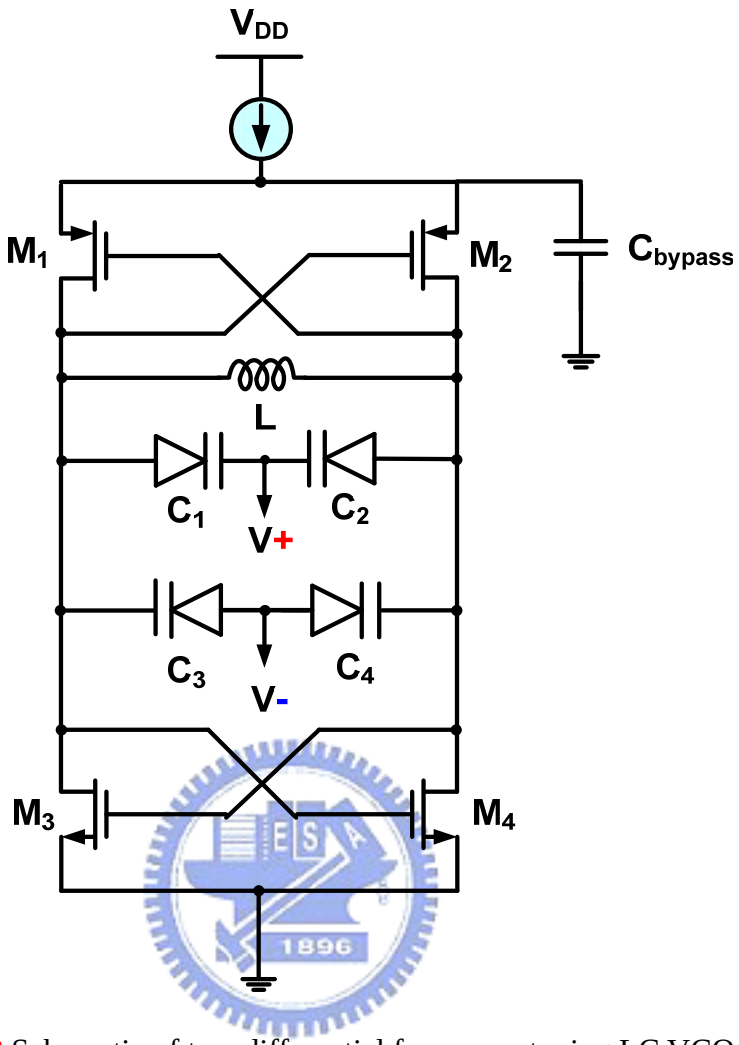


Figure 3.2 Schematic of two differential frequency tuning LC VCO.

3.2 Related CMOS LC VCO Issues

In the past research, effort to reduce phase noise has been published in several methods, one of that is to reduce phase noise of the LC-VCO by adding external circuits and enhancing the quality factor (Q) [14]. In this method, the tail current is made large when the oscillator output voltage reaches its peak value and when the sensitivity of the output phase to injected noise is the smallest; the tail current is made small during the zero crossings of the output voltage when the phase noise sensitivity is large. But, this method consumes more voltage headroom and power consumption

due to its tail current source. As shown in Figure 3.3 which proposes a harmonic tuned (HT) method that suppresses the harmonic frequency of the circuit by opening the fundamental and third frequencies and shortening the second harmonic by inserting L_2, L_3, C_3 and C_4 as a harmonic tuning network [5]. This method can reduce the phase noise effectively but the drawbacks are to increase the chip area and power consumption.

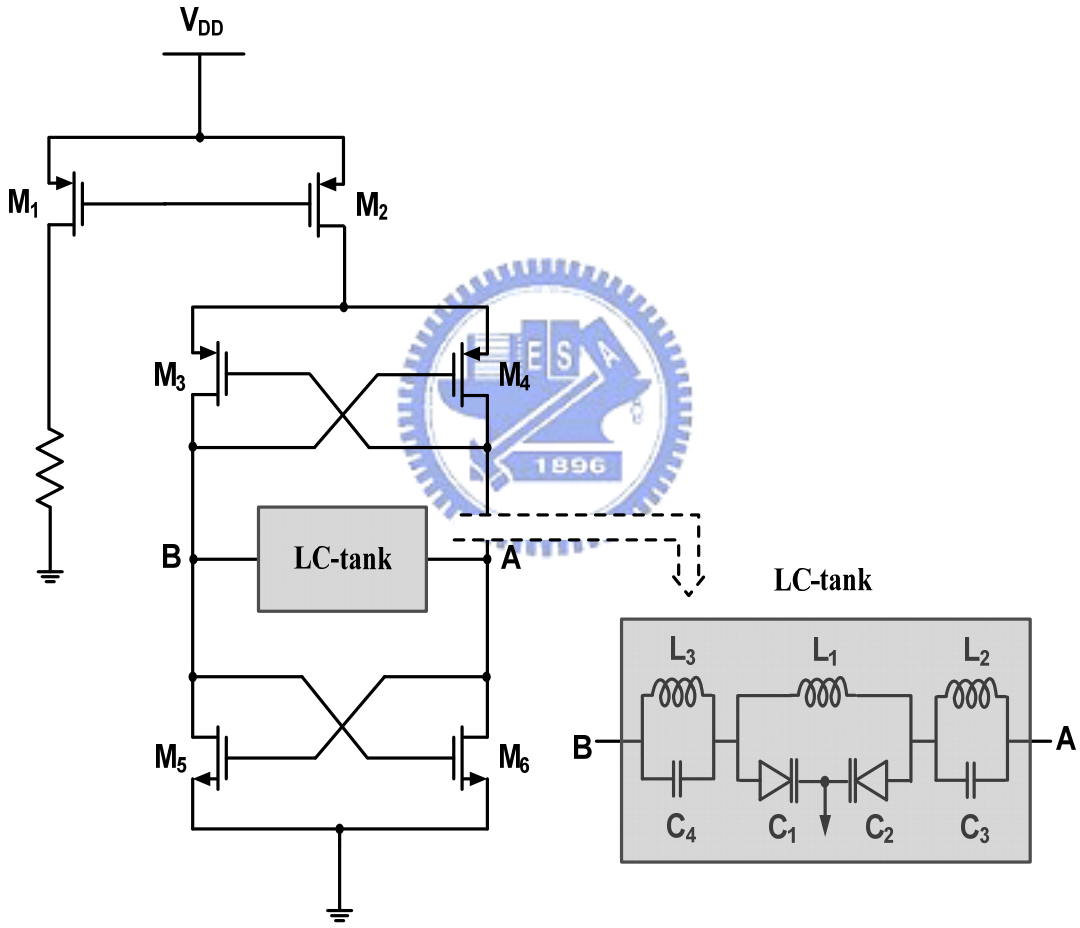


Figure 3.3 Schematic of simplified HT CMOS LC VCO

Figure 3.4 shows the full PMOS LC VCO with a top current source [15]. In most cases, the major noise contributor in VCOs is the channel noise form CMOS transistors [16]. In this condition, the use of PMOS is more attractive since the PMOS transistors have lower $1/f$ noise than that in NMOS transistors [3], [17]. Furthermore, the large capacitor C_E parallels the current source is needed because of the transistors of the differential pair might carry very little current for a fraction of the cycle. Thus, the duty cycle of the drain current waveform is reduced significantly. As a result, the drain current noise injection during the zero-crossing of the tank differential voltage can be reduced and the better phase noise performance is achieved. In addition, the C_E attenuates both the high-frequency noise components of the tail current and the voltage variations on the tail node. The improvement of voltage variations results in more symmetric waveforms and smaller harmonic distortion in VCO outputs.

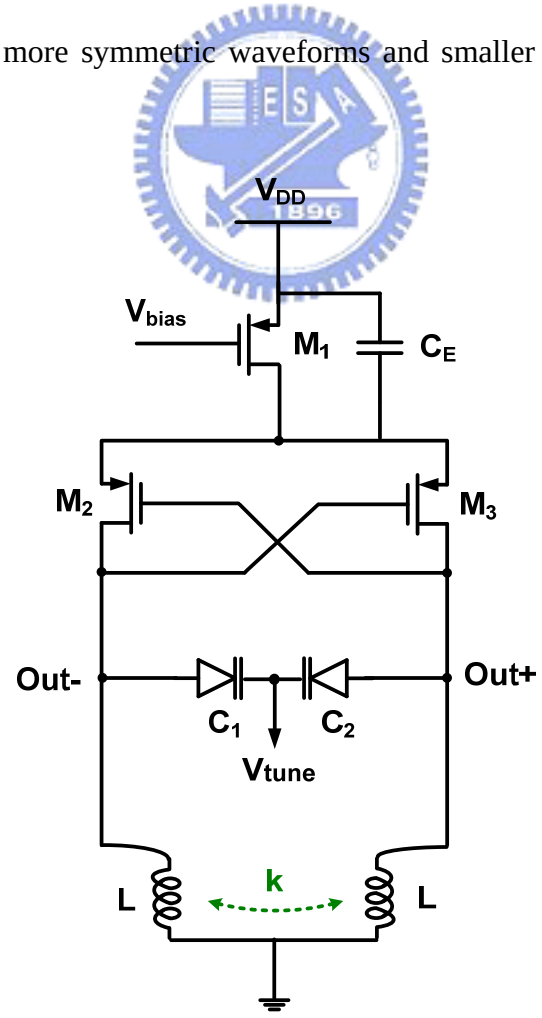


Figure 3.4 Full PMOS LC VCO

It is well known that the higher quality factor can be achieved by exciting an inductor differentially rather than single ended [18]. Therefore, as shown in Figure 3.4, the use of a symmetric center-tapped inductor not only has the more symmetric output waveforms of the LC-tank but also has the benefits of the coupling factor to increase the inductance value and can lead to save the chip area.

In the design of low power CMOS LC VCO, current-reused is a method in common use [6-7], [19]. Figure 3.5 shows the schematic of the current-reused CMOS LC VCO. The current-reused LC-VCO uses both NMOS and PMOS transistor in cross-coupled pair as a negative conductance generator to achieve low power consumption easily. The series stacking of NMOS and PMOS allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance. This topology is not only low power consumption but also low cost since it used only one inductor and two MOS transistors..

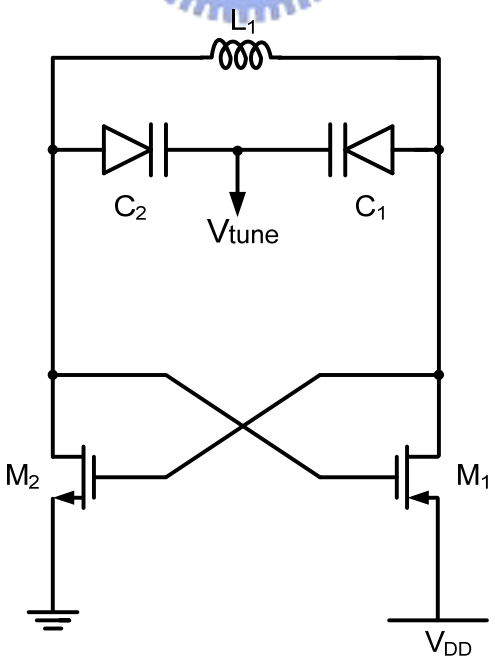


Figure 3.5 The current-reused LC VCO

Another method for a VCO to operate in low power consumption is the transformer feedback (TF) structure [20]. As shown in Figure 3.6, the drain and source voltages are decreased when the gate voltage is increased simultaneously. The reduction of the source voltage lowers the ground potential effectively and allows the drain voltage to sweep to a negative potential before the transistor gets into the linear region. As a result, the phase synchronization provides extra voltage headroom for the drain oscillation, the drain voltage could swing above the supply voltage and the source voltage could swing below the ground level. Furthermore, the drain and source signals oscillate in phase. Substantially, the oscillation amplitude is enhanced, and consequently, the supply voltage can be reduced for the same phase noise with lower power consumption. In Figure 3.6, the TF VCO uses a single transformer for the feedback across the drain and source terminals, which structure is similar to the Hartley design [21-23].

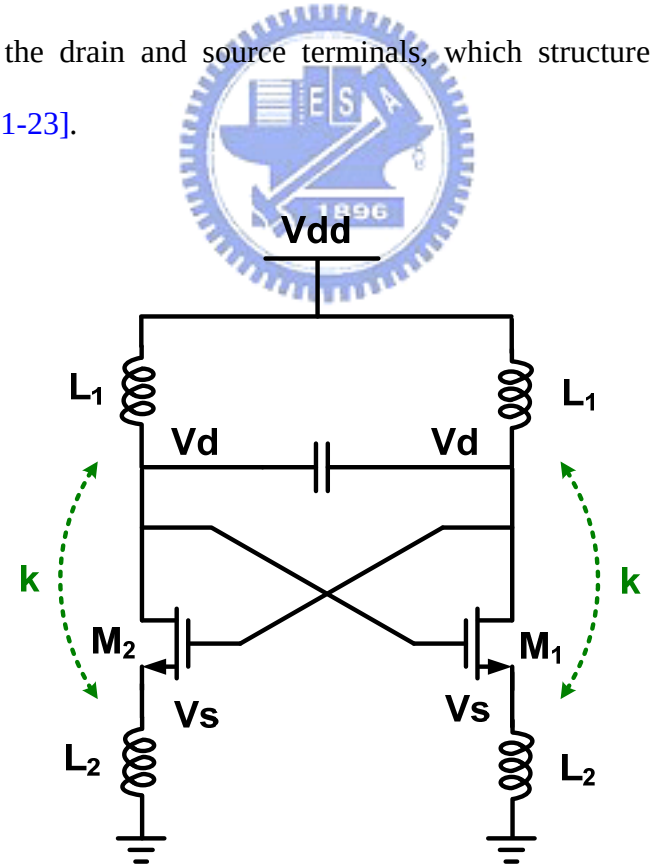


Figure 3.6 Transformer-feedback LC VCO

Chapter 4 *Design of a Fully Integrated Low Voltage Low Power CMOS LC VCO*

4.1 Introduction

As the modern CMOS process technology has been scaled down and the market trend moves toward a greater scale of integration gradually, the reduction of power consumption has become considerably important to portable devices in the applications of wireless communication system. As we can see in Table 4.1, weather the RF technology or the analog and mixed signal technologies, all the supply voltage are forced to reduce by the shrink of process technology [24].

In general, the most direct and efficient way to reduce power consumption in circuit design is to reduce the supply voltage. However, the supply voltage is relies on the threshold voltage chiefly. Once the supply voltage can be reduce, the MOS transistors may go into subthreshold regime, this result will bring about the decrease of reliability. Furthermore, unfortunately, the low supply voltage is usually limits the output signal amplitude, which leads to degrades the signal to noise ratio and deteriorates the phase noise performance in turn.

TABLE 4.1

ANALOG, MIXED SIGNAL, AND RF TECHNOLOGY ADVANCE TREND.

Year	***1997 250nm***	***1999 180nm***	***2001 150nm***	***2003 130nm***	***2006 100nm***	***2009 70nm***	***2012 50nm***
Supply voltage (V)	2.5-1.8	1.8-1.5	1.6-1.3	1.5-1.2	1.2-0.9	0.9-0.6	0.8-0.5
Frequency (GHz)	1.8-2.5	2.5-3.5	3.0-4.0	3.5-5.0	5.0-6.5	6.5-9.5	9.5-13

In this chapter, we propose the design of low voltage and low power consumption CMOS LC-VCO with negative conductance enhancement and common mode noise reduction method. The section 4.2 briefly describes the low voltage LC VCO topology that can operate with less voltage headroom compared to complementary LC VCO topology due to less transistors are stacked in vertical direction. In the section 4.3, the low voltage LC-VCO with negative conductance enhancement method and common mode noise rejection is proposed. Comparing to conventional LC VCO, the simulated results are illustrated in section 4.4. In section 4.5, the measured results are shown.

4.2 Low Voltage and Low Power LC VCO

In the design of LC VCO in low voltage operation, it mostly restricted by the threshold voltage of MOS transistors. However, as the advancement of CMOS process technology continue increasing, the threshold voltage of MOS transistors can be reduced to milivoltage level. It is a good deal for the design of low supply voltage LC VCOs. However according to the Leeson model of phase noise, we can see that there have two ways to improve the phase noise performance, one is to increase Q factor and another is to increase the average power in the LC-tank. Due to the serious loss of inductor in CMOS process technology, the first method mostly dominated by inductor which has the poor Q factor than varactors. The later method means that the more power consumption (or supply voltage) is needed. In the consideration of power-saving, this method is not efficient enough. Therefore, how to design a low voltage, low power consumption LC VCO and maintain comparable phase noise level is a difficult problem.

Figure 4.1 shows the conventional design of low supply voltage LC VCO. The LC-VCO consists of two deferential symmetrical inductors (L1 and L2), two accumulation-mode MOS varactors (C1 and C2) and a MIM capacitor (C3). The NMOS cross-coupled pair (M1 and M2) serves as the negative resistance to compensate for the energy losses from the LC-tank. The C3, L1 and L2 set the fix frequency while the C1 and C2 with the control voltage make the frequency tunable. The circuit has a symmetric topology to create symmetric output waveforms, which can reduce l/f noise up-conversion [25]. By the optimal design in the conventional LC VCO, we got the simulated results as shown in Figure 4.2 (a)-(b). In Figure 4.2 (a) the phase noise is -112.66 from 1MHz offset frequency at 3.4 GHz with 0.5V supply voltage and 0.54 mW power consumption. In Figure 4.2 (b) the tuning range

with 0 to 0.5 V control voltage is drawn.

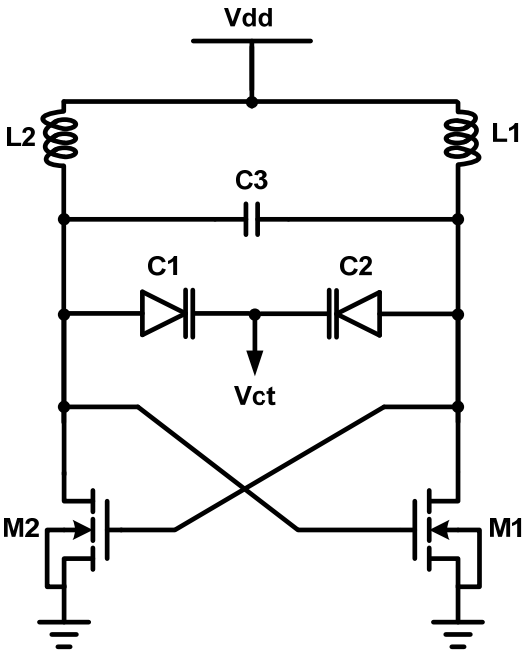


Figure 4.1 Conventional CMOS LC VCO with NMOS cross coupled pair.

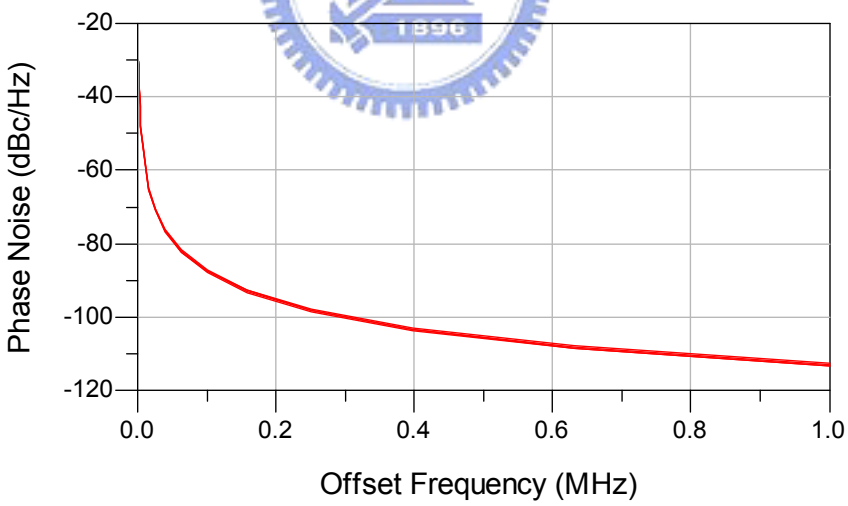


Figure 4.2 (a) The simulated phase noise of the conventional NMOS only LC VCO.

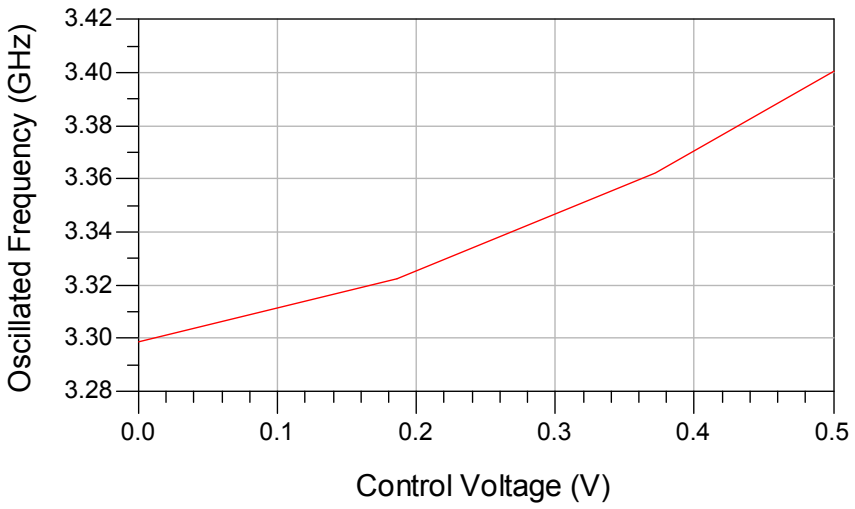


Figure 4.2 (b) The simulated tuning range of the conventional NMOS only LC VCO.

As we can see in Figure 4.2 (a), the low supply voltage can be achieved due to the less transistors are stacked. But the phase noise is usually not satisfied. Here, we proposed a negative conductance enhancement and common mode noise rejection method to improve the phase noise.

4.3 Design and Analysis of the Proposed LC VCO

4.3.1 Negative Conductance Enhancement

In the analysis of Q factor of a LC tank, the relation between conductance and Q factor is

$$Q = \frac{1}{G_P}\sqrt{\frac{C}{L}} \tag{4-1}$$

where the Gp is the conductance of a LC tank, the diagram of a LC tank with negative conductance is shown in Figure 4.3.

As the equation (4-1), we can obtain the result that Q factor will be increase when the G_P is decrease. Therefore, as shown in Figure 4.4, if we could add an additional negative conductance $-G_N$ to the LC tank, the total conductance G_{tot} will be degraded.

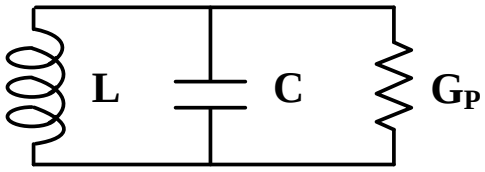


Figure 4.3 An LC tank with conductance.

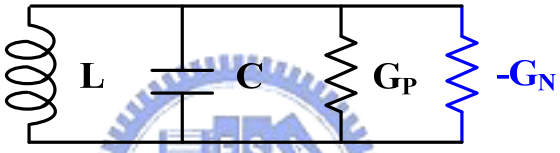


Figure 4.4 An LC tank with negative conductance.

According to [26], the negative conductance can be obtained from the topology in Figure 4.5, and the value of negative conductance is

$$G_N = \frac{\omega^2 C_{gs}(C_N + C_{gd})}{g_m} \tag{4-2}$$

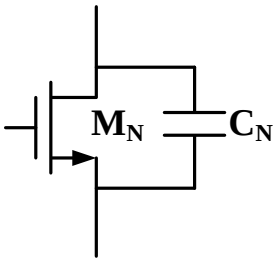


Figure 4.5 Negative conductance topology.

With the negative conductance is presented above, we now take this method into the proposed LC VCO to enhance the negative conductance. Figure 4.6 shows the proposed LC VCO with an NMOS pair, M3 and M4 that in parallel to conventional NMOS only cross-coupled LC VCO. For the demand of measurement, the M5 and M6 are served as buffer stages.

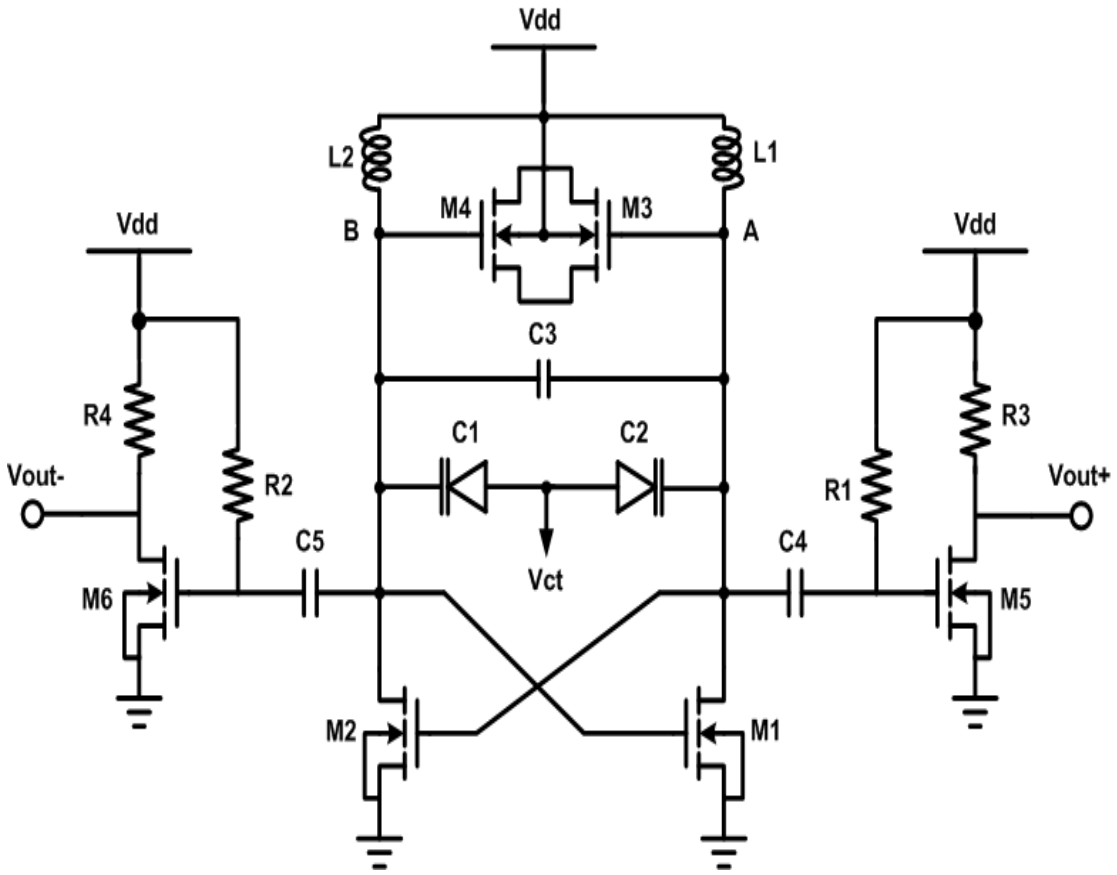


Figure 4.6 The proposed low voltage, low power consumption CMOS LC VCO.

Figure 4.7 shows the parasitic capacitances Cgs and Cgd of the proposed LC VCO. Due to the differential topology of the LC VCO, the equivalent circuit in Figure 4.7 can be equal to Figure 4.8. As shown in Figure 4.9, the parasitic capacitances C_{gs3}, C_{gd3} of M3, and C_{gs4}, C_{gd4} of M4 provide an additional negative conductance with M1 and M2. According to equation (4-2), the total negative conductance of the proposed LC VCO is

$$G_N = \frac{\omega^2 C_{gs1}\left[(C_{gd3}+C_{gs3})+C_{gd1}\right]}{g_{m1}} + \frac{\omega^2 C_{gs2}\left[(C_{gd4}+C_{gs4})+C_{gd2}\right]}{g_{m2}} \quad (4\text{-}3)$$

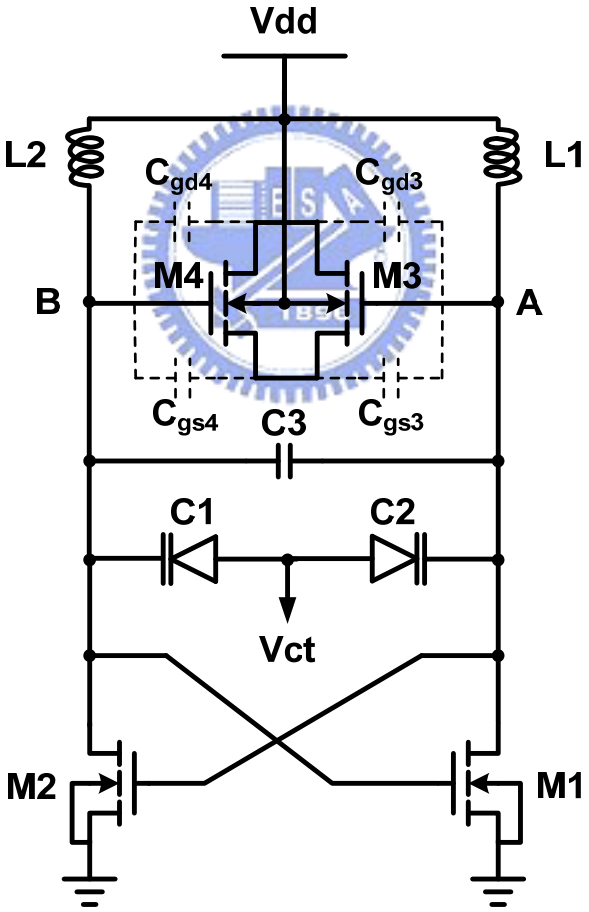


Figure 4.7 The proposed LC VCO with parasitic capacitances of M3 and M4.

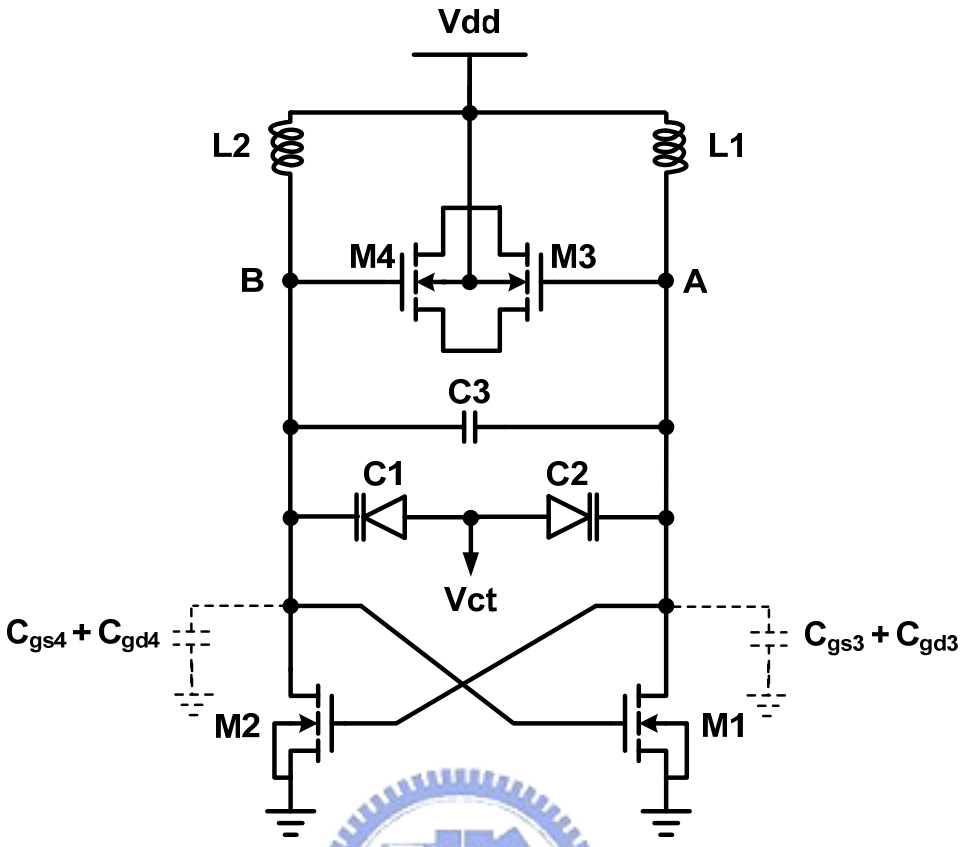


Figure 4.8 The parasitic capacitances of M3 and M4 of the proposed LC VCO.

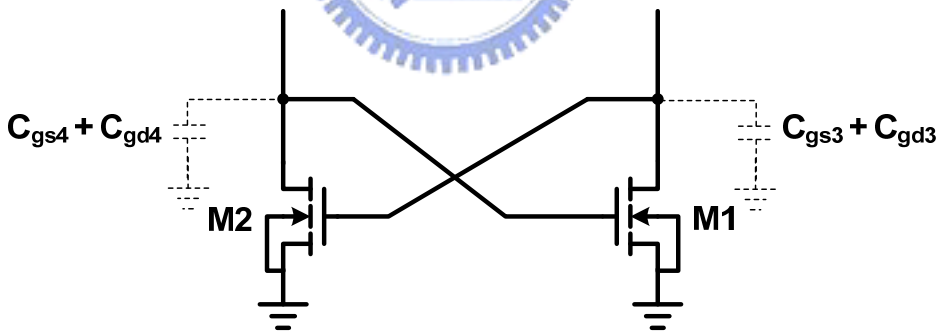


Figure 4.9 Negative conductance of the proposed LC VCO**.**

However, in order to avoid the cease of oscillation, the additional negative conductance should not be large than the conductance of LC tank.

4.3.2 Common Mode Noise Reduction

Common mode noise is an unwanted noise, which upconvert to the carrier frequency and result serious jitter and weak phase noise performance in LC VCOs. For this reason, we employ a common mode noise reduction method to suppress the common mode noise [11-12]. Figure 4.10 shows the common mode noise rejection of the proposed LC VCO.

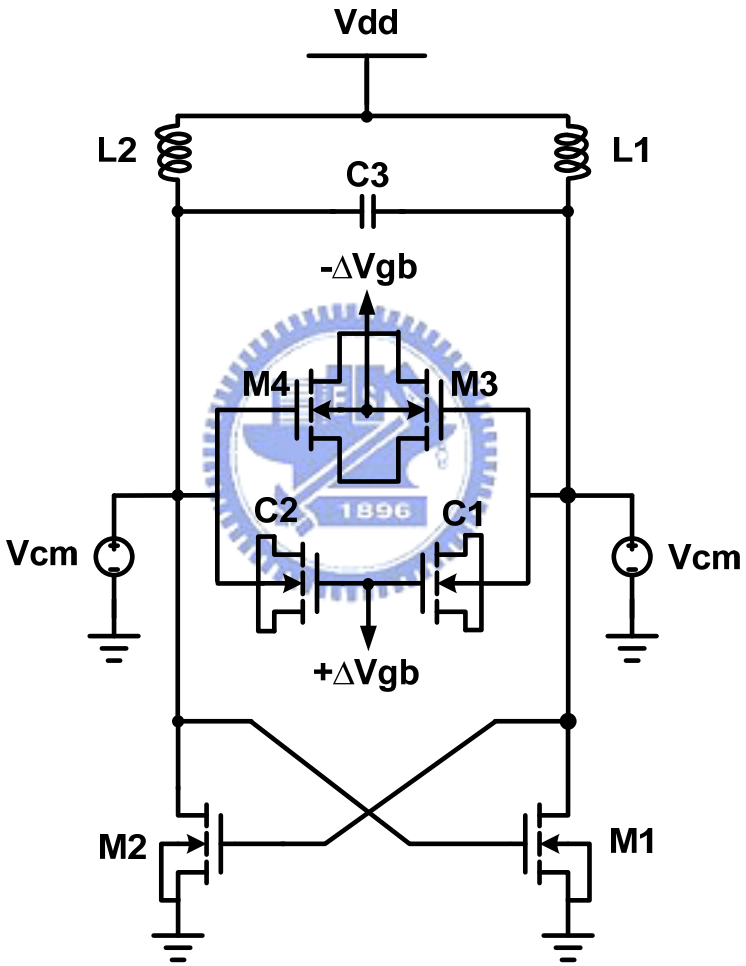


Figure 4.10 Common mode noise reduction of the proposed LC VCO diagram.

The common mode voltage Vcm is

$$Vcm \cong V_T + (\frac{I}{g_m}) \tag{4-4}$$

where I is the total current in the VCO, V_T and g_m are the threshold voltage and transconductance of the NMOS respectively. The -△Vgb and +△Vgb are the gate to bulk terminal voltage of the proposed NMOS pair (M3 and M4) and varactors (C1 and C2) respectively. In order to reduce the common mode noise, the symmetry of differential tuning is needed. According to mathematical analysis, the capacitances of NMOS pair and varactors can be shown as

$$C_N = C_0 + k_{v1}(-\Delta Vgb + Vncm) \tag{4-5a}$$

$$C_V = C_0 - k_{v2}(+\Delta Vgb + Vncm) \tag{4-5b}$$

Where C_0 is the zero bias capacitance, the $Vncm$ is common mode noise and the k_{v1} and k_{v2} are the capacitor gain of NMOS pair and varactors respectively. If the perfectly selection is achieved such that

$$k_{v1} = -k_{v2} \tag{4-6}$$

then the total capacitance C is

$$C = 2C_0 + 2kv\Delta Vgb \tag{4-7}$$

where $C=C_N+C_V$, △Vgb =+△Vgb –(-△Vgb). In equation (4-7), the common noise is canceled out. If not, the gain of the common mode noise is

$$\left|k_{v1} - k_{v2}\right| \tag{4-8}$$

As the common mode noise rejection has been explained above, the compared results between proposed LC VCO and conventional one is presented in next section.

4.4 Simulation Results

Figure 4.11 shows the simulated phase noise with different body bias of the NMOS pair. As we can see, the best phase noise is around 0.6 V.

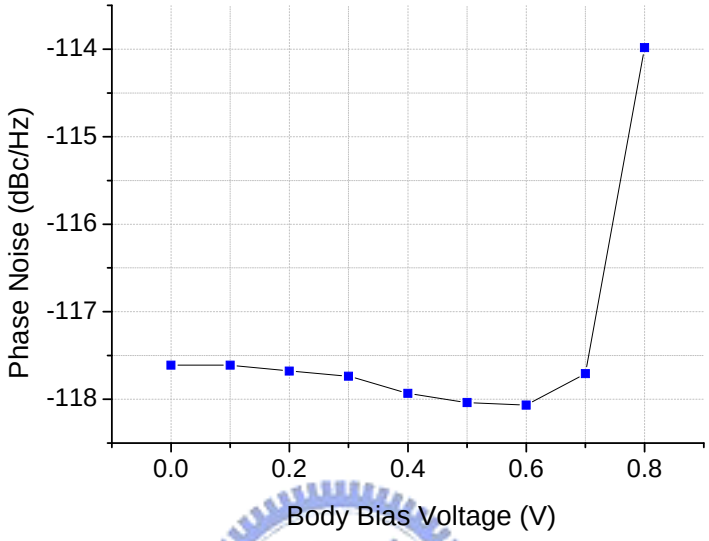


Figure 4.11 Simulated phase noise versus body bias.

As shown in Figure 4.12, the conventional and proposed LC VCOs are compared.

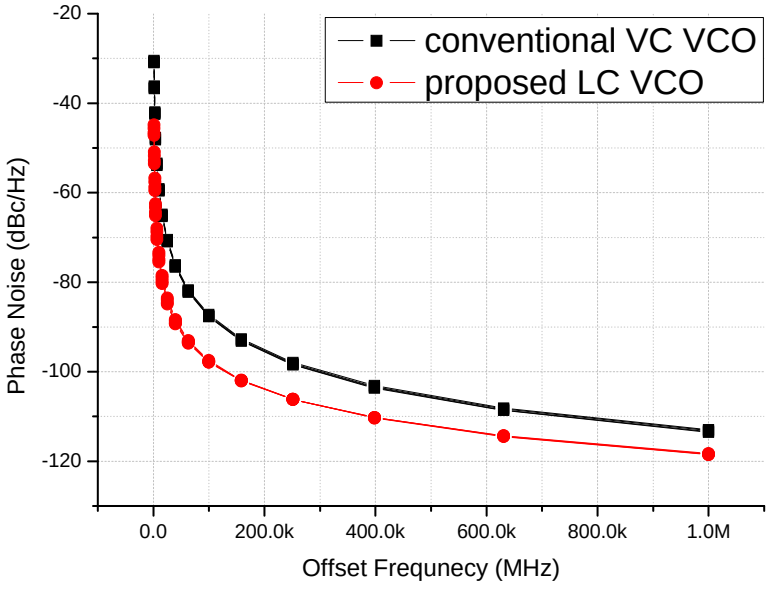


Figure 4.12 Compared phase noise of two LC VCOs.

In the proposed LC VCO, the phase noise is -118.32 dBc/Hz at 1 MHz offset from carrier frequency. The improvement between conventional and proposed LC VCOs is about 6 dBc/Hz at 1 MHz offset frequency. Another parameter Kvco is also improved as shown in Figure 4.13.

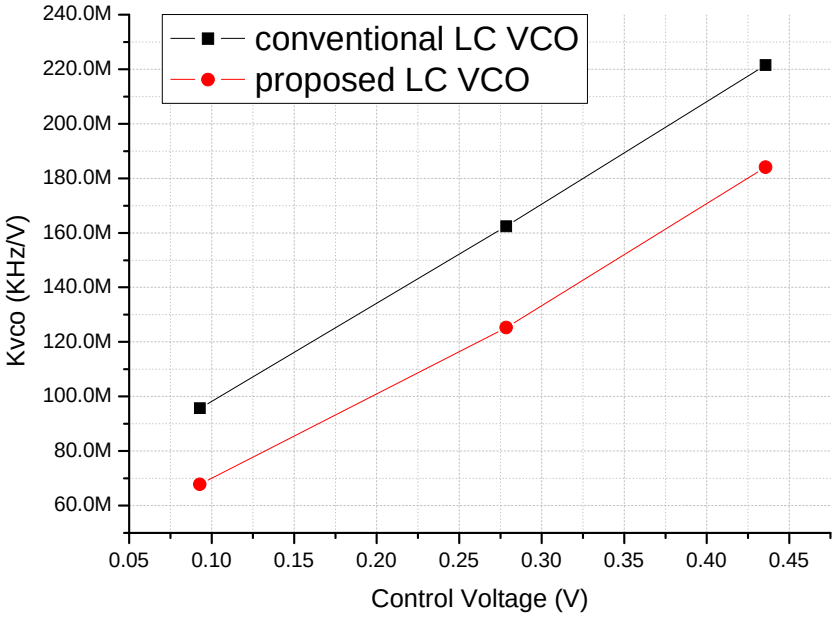


Figure 4.13 The compared result of Kvco.

As shown in equation (4-9), the figure of merit (FOM) is widely used to compare the VCO performance among the different designs

$$FOM = L(\Delta\omega) + 10 \times \log\left(\frac{P_{DC}}{1mW}\right) - 20 \times \log\left(\frac{\omega_0}{\Delta\omega}\right) \qquad (4\text{-}9)$$

where ω_0 is the oscillating frequency, $\Delta\omega$ is the offset frequency, $L\{\Delta\omega\}$ is the phase noise at $\Delta\omega$, P_{DC} is the DC power consumption of VCO in mW. The FOM of proposed VCO are evaluated and are equal to -192 dBc/Hz.

In addition, in order to match the simulated results, the pad-effect which is provided by national chip implementation center (CIC) as shown in Figure 4.14

should be take into consideration. In post simulation, we finished the EM simulation by Agilent advanced design system (ADS) Momentum design tool.

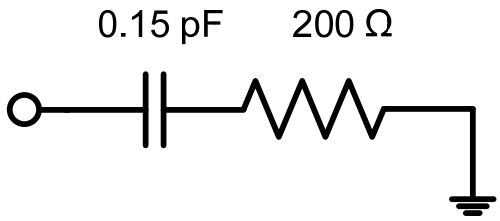


Figure 4.14 The equivalent model of pad-effect.

4.5 Measured Results

In this section, the measurement results of the proposed LC-VCO are presented. In Figure 4.15 and Figure 4.16, the chip layout and microphotograph of the proposed LC-VCO are shown, respectively. The LC-VCO is fabricated in TSMC 0.18-μm 1P6M CMOS process. Its chip area including pads is 0.61×0.76 mm^2.

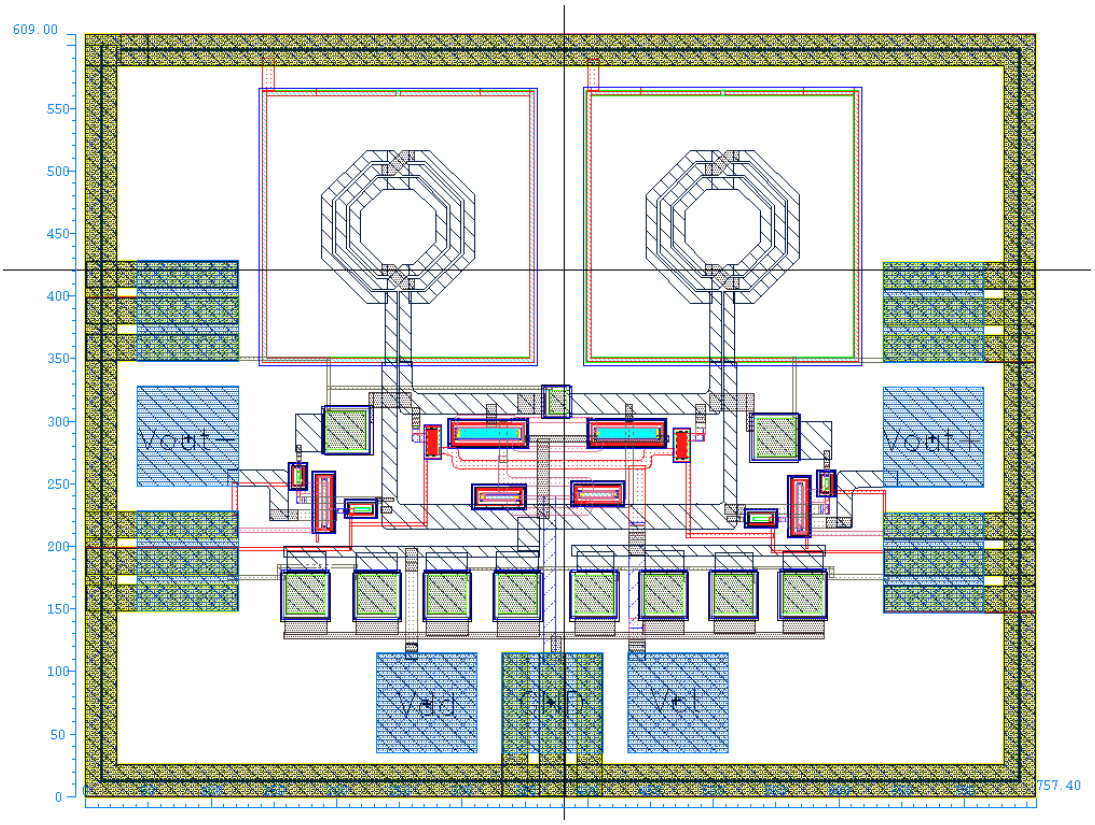


Figure 4.15 The chip layout of the proposed LC-VCO.

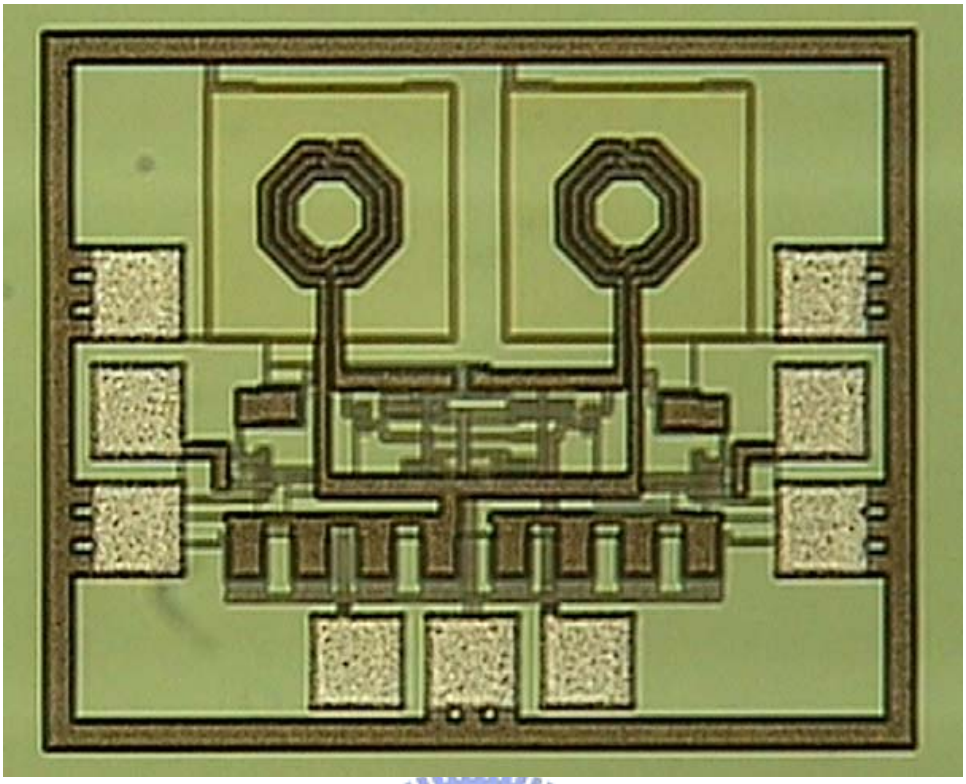


Figure 4.16 The Microphotograph of the proposed LC-VCO.

The LC-VCO chip was measured by on-wafer probe method. Figure 4.17 shows that the measured phase is -112.24 dBc/Hz with 0.51 V supply voltage. According to the measured current in Figure 4.18, the chip drew a total DC current is 2.05 mW. The power consumption which including buffer circuits of the LC VCO is 1.05 mW. Figure 4.19 shows the output spectrum. The measured VCO's gain is drawn in Figure 4.20. In table 4.2, the measured results are summarized and compared with related LC VCOs.

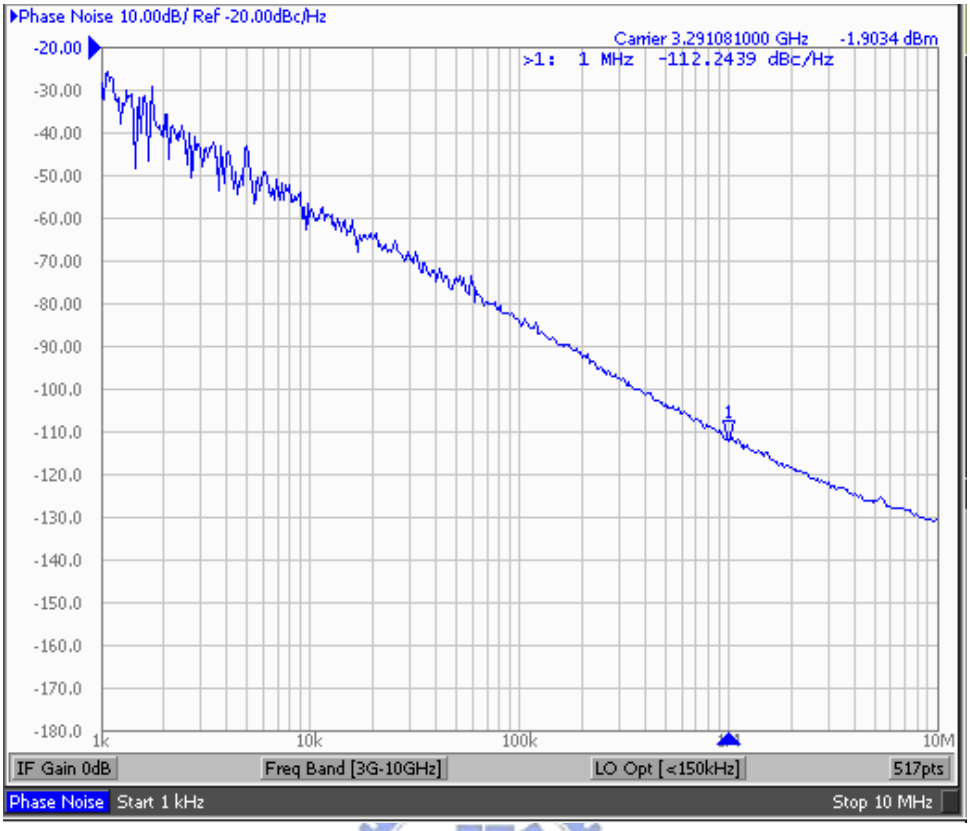


Fig. 4.17 Measured phase noise of the proposed LC VCO.

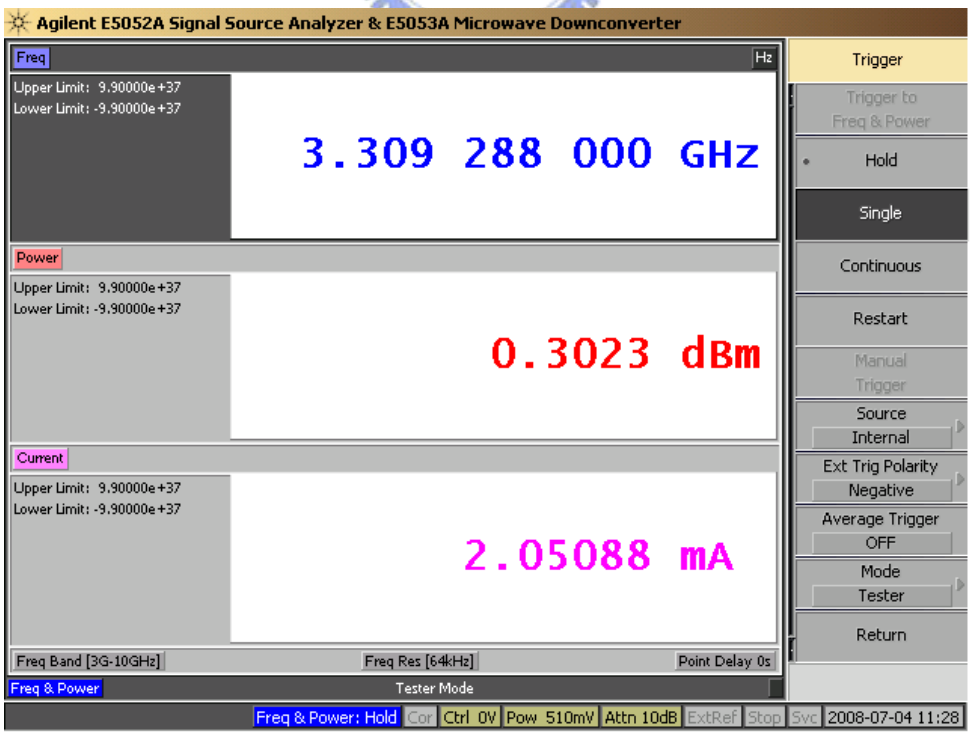


Fig. 4.18 Measured characteristics of the proposed LC VCO.

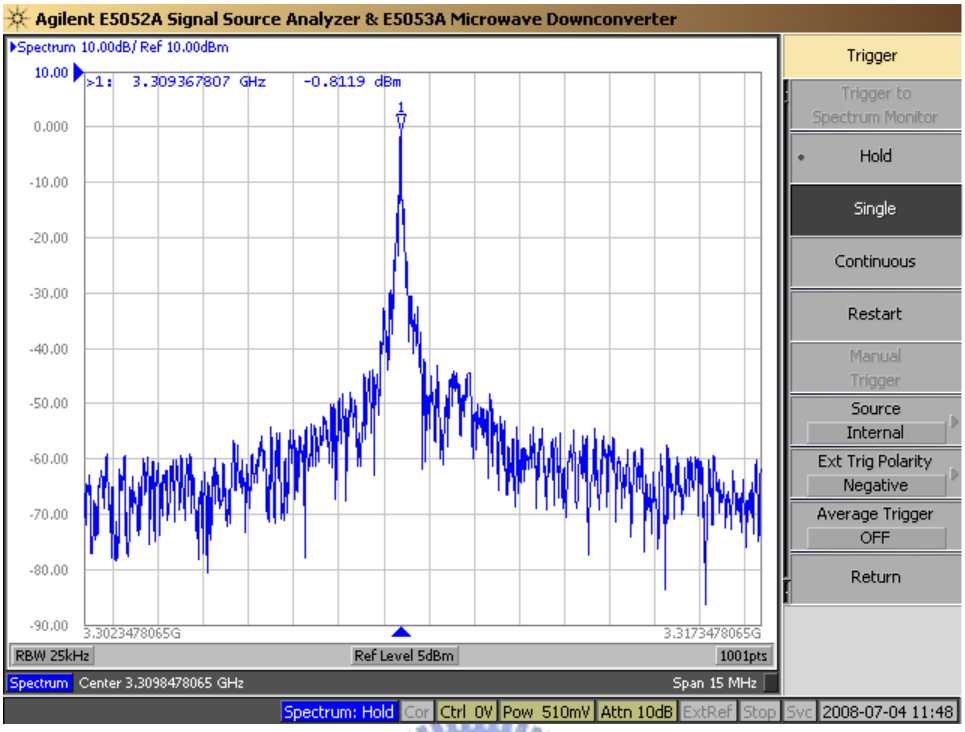


Fig. 4.19 Output spectrum of the proposed LC VCO.

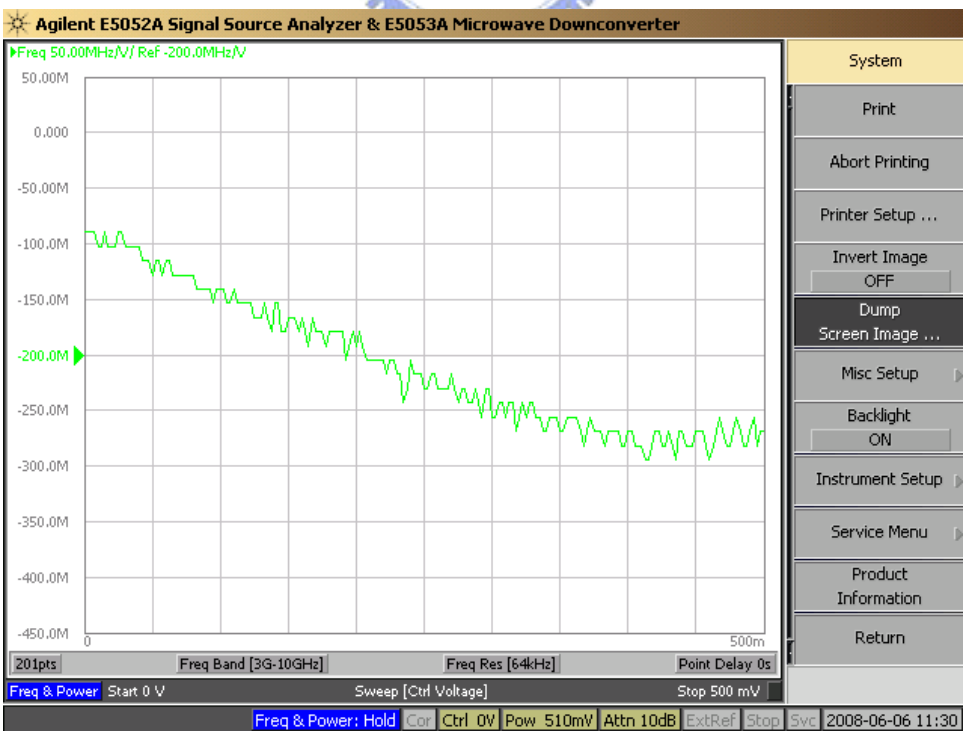


Fig. 4.20 The measured gain of the proposed LC VCO.

TABLE 4.2

COMPARED THE PROPOSED LC VCO WITH RECENTLY PUBLISHED LC VCOS

Ref.	Tech. (um)	f_o (GHz)	PN (dBc/Hz)	V_{DD} (V)	P_{DC} (mW)	FoM (dBc/Hz)
This work	0.18 CMOS	3.3	-112.2	0.51	1	-182.6
[27]	0.18 CMOS	2.2	-122	1.8	18.5	-176.2
[28]	0.18 CMOS	2.4	-113	0.75	4.5	-178.8
[29]	0.18 CMOS	2	-111.7	0.9	0.5	-180.7
[30]	0.18 CMOS	3.5	-108.5	1.2	4.5	-161.6

Chapter 5 *Conclusions*

A fully integrated, low voltage and low power CMOS LC-VCO with negative conductance enhancement and common mode noise reduction is proposed and implemented by TSMC 0.18-μm 1P6M CMOS process. The design uses the conventional NMOS only cross-coupled topology combined with an NMOS pair to improve the phase noise performance in low voltage operation. The proposed LC-VCO consumes 1 mW with 0.51 V supply voltage. The measured phase noise at 1 MHz offset frequency is -112.24 dBc/Hz at 3.3GHz. Although the supply voltage and power consumption are obviously improved, there is still a lot of space for noise reduction. Several extensive studies have been underway to further reduce the phase noise of LC-VCOs. In this field, it maybe worth our effort in the future works, such as low phase noise LC-VCOs.

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