國 立 交 通 大 學

電信工程學系

碩 士 論 文

一個低功率的權重前饋控制串聯式積分器架構之二階三角積分器設計與實現

Design and Implementation of a Low-Power CIFF Structure Second-Order Sigma-Delta Modulator

研究生：蘇品翰

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中　華　民　國　九　十　八　年　一　月

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摘要

隨著 VLSI 技術的演進，類比電路已經被實現在更低的提供電壓及更小的晶片面積。在各種低供電、低功率消耗的元件中，三角積分數位類比轉換器在音頻的可攜帶電子元件應用上的實現，是一種比起其他數位類比轉換器、在功率消耗上更有效率的一種實現方式。

本論文提出並經由台積電的 0.18 微米製程實現了一個低功率消耗的三角積分數位轉換器電路。經由將回路濾波器中的運算跨導放大器的規格做最佳化，一個電流最佳化的技術被提出。使用權重前饋控制串聯式積分器的調變器架構以及單級-A 類加上正回授的運算跨導放大器電路，本論文提出的三角積分類比數位轉換調變器的訊號雜訊比到達 63.4dB, 並且能處理直流到最高 16KHz 的訊號。使用一伏特的供應電壓、整個調變器的功率消耗只有 18 微瓦特。

Design and Implementation of a Low-Power CIFF Structure Second-Order Sigma-Delta Modulator

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Abstract

With the scaling down of VLSI technology, the analog circuit have implemented with a lower supply voltage and smaller chip area. Among the low-voltage low-power building blocks, the sigma-delta ADC provides a power-efficient way to implement an ADC for audio-band portable device applications.

This thesis presents the design and implementation of a low power sigma-delta modulator (SDM) with a standard 0.18-μm CMOS technology. A current optimization technique is proposed by making a specification optimization of the Operational Transconductance Amplifier (OTA) in loop filter. Using a chain of Integrators with weighted feed-forward summation (CIFF) structure and a single-stage class-A OTA with positive feedback, the proposed second-order SDM achieves a SNR of 63.4dB that be able to process the signal form DC to 16KHz.The power consumption is only 18 uW from a 1-V supply.

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其次，謝謝嘉儀、順華、江俊、信太及俊誼學長在研究上或是日常生活上對我的照顧；還要謝謝秉勳、凱迪、明君、春慧四位同學在我的課業及生活上的幫忙;平常在研究領域上的討論及切磋，讓我的基本觀念能夠更加的紮實。也謝謝是瑜、鎮宇、國哲、鼎國、燦傑、登政等學弟的支持與幫忙。最後還要特別謝謝大學同學士豪、奐箴、訓緯、建興、傑天、慶陽、善凡、詠峻、俊穎、士昌等人對我在類比電路設計領域的幫助。有了各位的陪伴，才能讓我在這兩年半的日子裡有這麼快樂且充實的研究生活。

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蘇品翰

January, 8, 2009 於新竹

Content

List of Tables

List of Figures

Chapter 1
Introduction

1.1 Motivation

With the scaling down of modern VLSI technology in recent years, the digital circuits have implemented with a complex and a higher clock rate, and it introduces more constraints for the analog circuits.

However, the decreased supply voltage restricts the signal swing in circuits and brings difficulties for analog circuit design. In low-voltage environments, the transistor characteristics degrade and some circuit techniques can no longer be used, thus the low-voltage design different from the traditional circuit design technique. Therefore, the design of low-voltage, low-power analog devices has become more and more important.

Among the low-voltage low-power building blocks, the audio-band battery-based operation system is highly desired by various applications, such as mp3 players, radio-frequency identification (RFID), biomedical electronics and digital hearing aid instrument.

In these devices, the analog-to-digital converters (ADCs) are widely used in various systems, because it is necessary to transfer nature analog signal to digital code.

Among different ADC topologies, the Sigma-Delta ADCs efficiently trade speed for accuracy, providing an efficient way to implement high-resolution ADCs without stringent matching requirements compared to other types of ADCs (ex: flash ADC, pipeline ADC). By over-sampling and noise shaping, the sigma-delta ADCs transfer most of the signal processing tasks to the digital domain. Therefore, for high-resolution ADCs, the sigma-delta ADCs are more power-effective and robust compared to other architectures.

Therefore, the design target of this thesis is to achieve a low-power audio band sigma-delta ADC design. The experimental SDM present here have been fabricated in a standard 0.18um CMOS technology, and provide a SNR of 63dB for audio band signal (16k) and only dissipates 18uW, it can be used in a low power portable audio devices.

1.2 Organization

In Chapter 2, the beginning is the overview of the analog-to-digital converters (ADC). After them, the quantization issues, oversampling and noise shaping are introduced. Then the performance metrics of sigma-delta modulators (SDM) end this chapter.

Chapter 3 describes the system level design considerations, including the analysis of the power issues of SDM, the topology selections and the limitations and non-ideal effects of the SDM.

Chapter 4 discusses the topics of sub-circuits that will be used to realize the proposed SDM circuit, which includes an OTA, a comparator, a clock generator, capacitors and switches. The pre-simulation and post-simulation results are given. The layout level design will be described in this sequence.

In Chapter 5, the testing environment is present, including the instruments and the testing circuits on printed circuit board (PCB).The experimental results for the SDM, which is fabricated in a 0.18um 1P6M 1.8V standard CMOS technology with MIM process will be summarized.

Chapter 2

SDM Fundamentals

This chapter begins with a brief overview of analog-digital converter (ADC). Following by the classification of ADC, the oversampling and noise shaping is introduced and considered and defined mathematically. The performance metrics of targeting ADC is than described in the end of this chapter.

2.1 A brief Introduction of ADC

The ADCs are fed a continuous-time analog signal to convert discrete-time digital signals. In order to perform the analog to digital conversion, two steps should be down. The first is the discretization of the continuous analog signal, which is called sampling. After sampling, the quantization step is followed by digitizing the amplitude of the discrete signal, as shown in Figure 2.1.

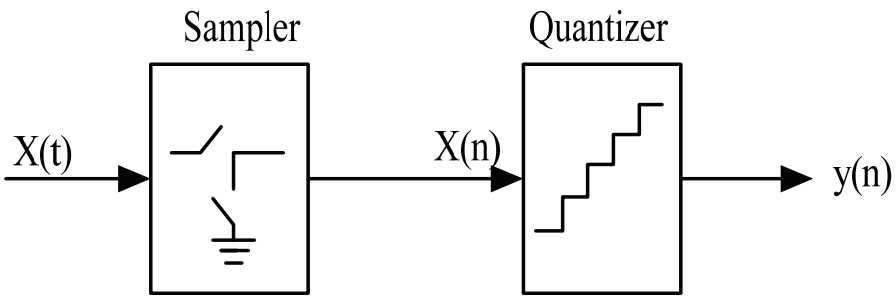

Figure 2.1 Block diagram of an ADC

For an ADC, there are two important parameters, input signal bandwidth and resolution, and different types of ADCs are developed according to different input signal bandwidth and resolution requirements as depicted in Table 2.1. Among the ADCs, the sigma-delta ADC is suitable to medium to high resolution applications in the audio frequency range.

Category	**Structure**
Low-to-Medium Speed High Accuracy	Integrating ADC Sigma-Delta ADC
Medium Speed , Medium Accuracy	Successive approximation ADC
High Speed Low-to-Medium Accuracy	Pipeline ADC Flash ADC

Table 2.1 various kinds of ADCs

Since the process of quantization is a classification process in amplitude, there is always an error in an ADC, and the quantization error e_q is smaller than the quantization step Δ of the ADC, as depicted in Figure 2.2.

$$-\frac{\Delta}{2} \le e_q \le \frac{\Delta}{2} \tag{2.1}$$

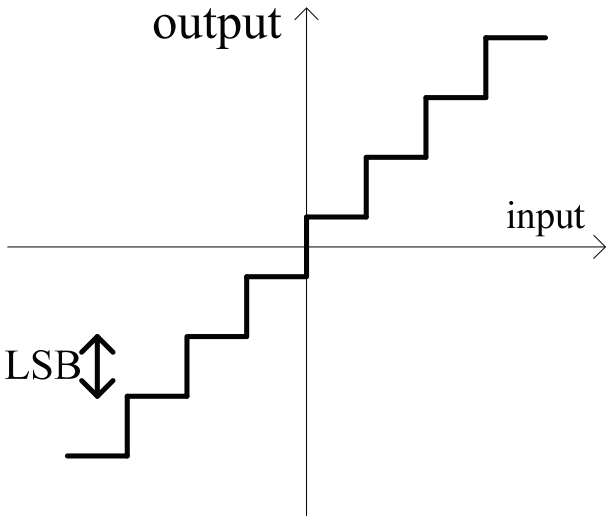

Figure 2.2 Transfer curve of ADCs

The quantization step Δ is called the least significant bit (LSB) of the ADC, where $\Delta = {V_{ref}}/{2^N}$. If we assume that the quantization noise is white noise, it is uniformly distributed between $\pm\frac{LSB}{2}$, as Figure 2.3:

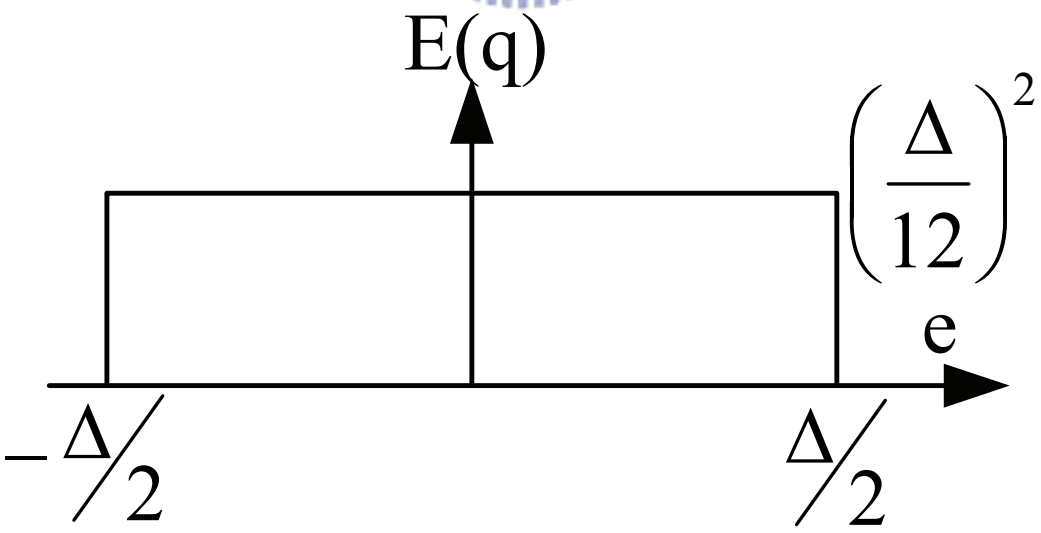

Figure 2.3 Power spectral density of quantization noise

Therefore, the power of the quantization error can be derived as:

$$P_e = \int_{-\infty}^{\infty} e^2 \rho(e_q) de = \frac{\Delta^2}{12} \tag{2.2}$$

For a sinusoidal input signal, its maximum peak value without clipping is $2^N \frac{\Delta}{2}$, where N is the bit number of the quantizer. Thus the sinusoidal signal power equals to:

$$P_{in} = \frac{1}{2}\left(\frac{2^N \Delta}{2}\right)^2 = \frac{2^{2N}\Delta^2}{8} \tag{2.3}$$

From the equation, if the quantization noise can be modeled as a noise source, we can calculate the signal-noise-ratio (SNR) of an ideal N-bit ADC:

$$SNR_{peak} = 10\log\left(\frac{P_{in}}{P_e}\right) = 10\log\left(\frac{\frac{\Delta^2 2^{2N}}{8}}{\frac{\Delta^2}{12}}\right) = 10\log\left(2^{2N}\right) + 10\log\left(\frac{3}{2}\right) = 6.02N + 1.76(dB) \tag{2.4}$$

It can be found that increase one bit resolution of the quantizer gives the SNR improvement of 6.02dB.

2.2 Oversampling and Noise Shaping

This section describes the principle and the theorem of the digital signal processing technique. We discuss oversampling first, which is followed by noise shaping.

2.2.1 Oversampling

For a signal bandwidth of f_B, the Nyquist rate is $2f_B$.A Nyquist ADC represent that the sampling frequency of the ADC is at Nyquist rate. Moreover, an ADC with the oversampling technique can also improve the SNR. Its sampling rate f_S is greater more times than the signal bandwidth $2f_B$, and the oversampling ratio is defined as $OSR = \frac{f_s}{2f_B}$, as Figure. 2.4, than the quantization power spectral density is reduced to:

$$P_e = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.5}$$

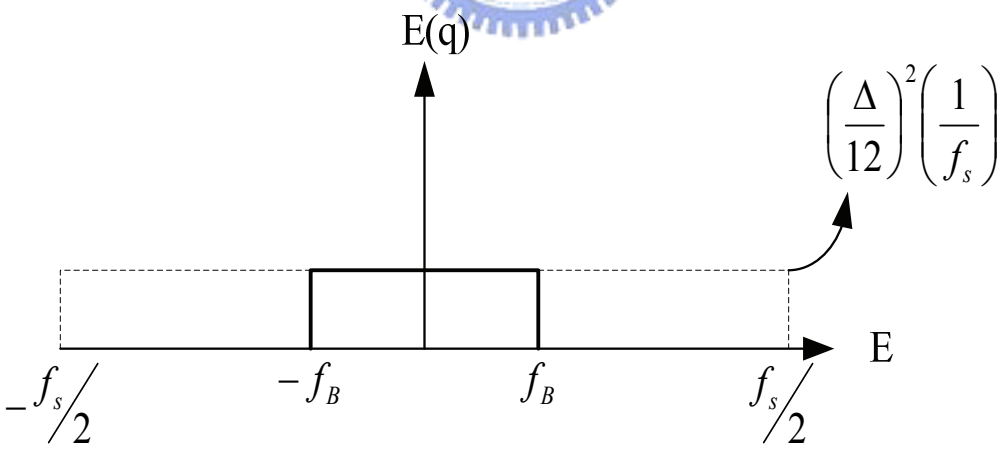

Figure 2.4 Quantization noise in an oversampled converter

Thus the peak SNR equals to:

$$SNR_{peak} = 10\log\left(\frac{P_{in}}{P_e}\right) = 6.02N + 1.76 + 10\log(OSR) \tag{2.6}$$

2.2.2 Noise Shaping

With oversampling technique, the SNR increase 0.5 bit if sampling frequency is doubling. In addition to use oversampling technique to improve the performance of ADCs, we can use noise shaping technique to further increase the SNR of the ADC, by applying a loop filter before the quantizer and introducing the feedback, a noise-shaping modulator is built and new noise transfer function is realized.

A basic Sigma-Delta modulator is shown in Figure 2.5, it contains a loop filter, a quantizer and a feedback loop. If we assume that the DAC feedback gain is unity, than we can express the output of the SDM is:

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2.7}$$

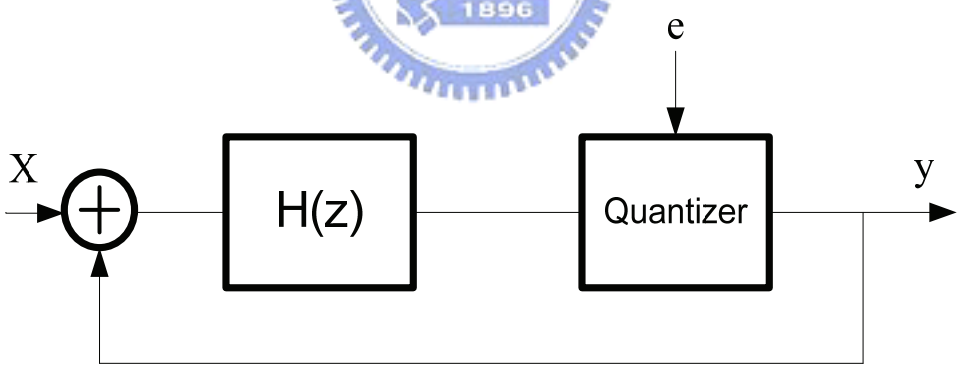

Figure 2.5 A linear model of the sigma-delta modulator

Where STF(z) represents the signal transfer function and NTF(z) represents the noise transfer function. And the STF(z) and NTF(z) can be calculated as:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} \tag{2.8}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{2.9}$$

With the large gain of H(z) at the frequency band, the STF(z) will approximate unity and the NTF(z) is going to approximate zero over the signal band. Thus the quantization noise is further attenuated than only by oversampling.

2.3 Performance Metrics

The performance metrics is shown at Figure 2.6 with a full scale sine wave to ADC, performed a Discrete Fourier Transform (DFT) to map into Fast Fourier Transform (FFT) spectrum. Some of the performance metrics are listed below, while the unit is "dB".

1. SFDR: the abbreviation of "spurious free dynamic range". Difference between the fundamental bin and the highest harmonic bin.

2. SNR: the abbreviation of "signal to noise ratio". Fundamental power divided by the power of the bins in the FFT other than DC, fundamental and first N harmonic bins.

3. SNDR: the abbreviation of "signal to noise and distortion ratio". Fundamental power divided by the power of the bins in the FFT other than DC and fundamental bins.

4. ENOB: the abbreviation of "effective number of bits", which is defined at Equation 2.10:

$$ENOB = \frac{SNDR - 1.76}{6.02}(dB) \tag{2.10}$$

5. DR: the abbreviation of "dynamic range". Effective input range when SNR remains positive.

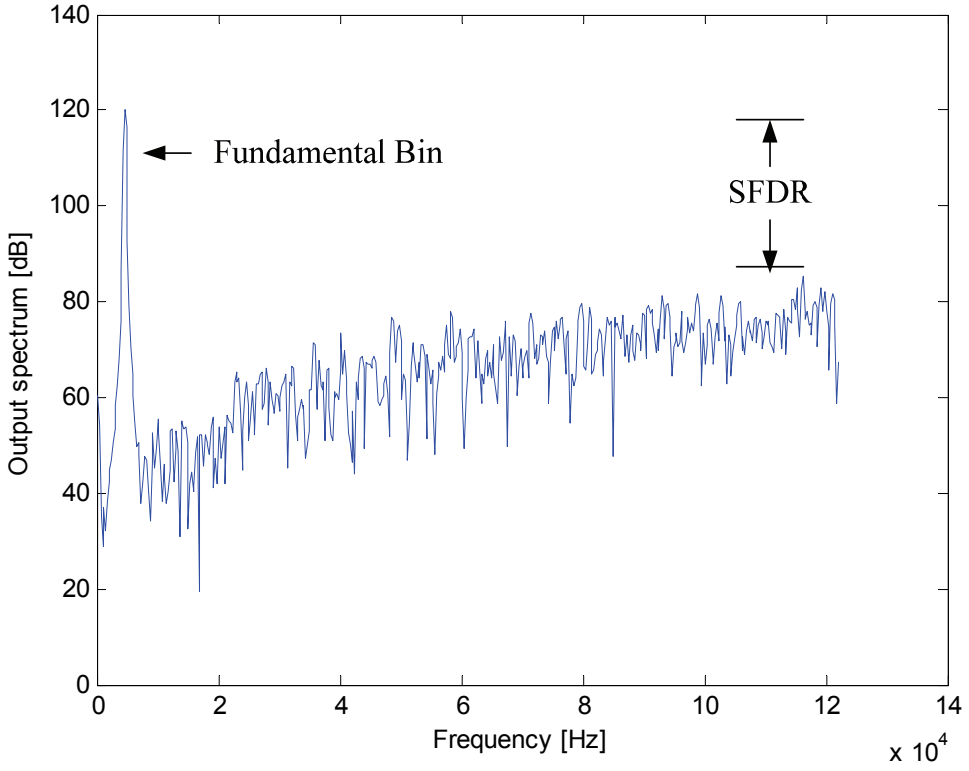

Figure 2.6 Performance metrics

Chapter 3

System Considerations

This chapter discusses actual SDM design considerations. We begin with reviewing previous researches then consider power issues in traditional SDM design, and the system parameter considerations are discussed in Section 3.2. Several non-idealities such as gain requirement, settling of OTA and capacitor sizing are discussed in the end of the chapter.

3.1 Power Issues in SDM

There are many researches about how to reduce the power of the sigma-delta modulator for audio band applications in recent years [2-9].

A switched-OPamp technique combined with a dc level shift has been proven to allow proper operation under low VDD conditions (0.7v),thus lower the power consumption[2]; A new fully differential CMOS class AB Operational Amplifier with a charge-pump is proposed [3]; And a load-compensated OTA with rail-to- rail output swing and gain enhancement is used in a 90nm technology [4]; And a 0.6v folded-cascode OTA topology is used in a 2-2 cascade delta-sigma ADC design with a resistor-based sampling technique[5]. A switched-current SDM is used for a bio-acquisition Microsystems with 0.8v power supply. And a Digital Hearing Aid

chip is proposed [7]; Then a ADC is designed and optimized for a CMOS image sensor[8]; Finally, a 4th order SDM is presented with a single stage class A OTA and positive feedback[9].

The comparisons of above researches are listed as Table 3.1:

	Technology	VDD	Signal BW(KHz)	OSR	Peak-SNR (dB)	Power
JSSC 2002[2]	0.18	0.7	8	64	67	80
ISCAS 2003[3]	0.18	0.9	10	100	74	38
JSSC 2004[4]	0.09	1	20	100	85	140
JSSC 2005[5]	0.35	0.6	24	64	77	1000
TCASI 2006[6]	0.18	0.8	5	64	50	180
JSSC 2006[7]	0.25	0.9	8	128	86	60
IMTC 2007[8]	0.18	1	25	1000	70	150
JSSC 2008[9]	0.13	0.9	20	50	83	60

Table 3.1 Summary of previous SDM papers

Among these researches, a part of them adopt some special analog circuits, such as switched-Opamp technique[2], switch-current topology[6] or resistor-based sampling technique[5] to reduce the power. Moreover, because that the power consumption of a SDM is most consumed at the OTA in loop filter, therefore some of them choose adaptive OTA topology to reduce power [3][4][7][8][9].

From above researches, we can observe that the former have a low supply voltage, but generally they often have larger chip area due to the use of extra component. Furthermore, using a low-power OTA in loop filter is an effective method to lower the power consumption of SDM because that the power consumption of a SDM is most consumed at the OTA in loop filter.

There are several specifications we must take care when designing an OTA (such as gain requirement, bandwidth, slew-rate, phase margin, output swing…etc) in Sigma-Delta A/D system conveniently. The specifications of the OTA in these researches are listed at Table 3.2. From the table, we can observe these specifications are followed by the "rule of thumbs" in traditional ADC design mostly. A lack of specification detail analysis is happened in these researches.

OP Architecture	Fs (MHz)	DC gain (dB)	UGBW (MHz)	SR (v/us)	Phase (°)	CL (pF)	Power (uW)
Switched-OP[2]	1	50	10	3.3	80	4	78/16
Class-AB OTA[3]	2	46	3.2	7	50	5	X
Gain-enhancement[4]	4	50	57	X	57	6	80
Folded-Cascode[5]	3	60	10	10	65	X	X
Two stage Class-AB[7]	2	78	7	X	55	3	X
Gain-boosted[8]	5	90	300	125	60	0.6	130
One stage positive feedback[9]	2	55	37	X	29	3	20

Table 3.2 Specification comparison of OTA

In fact, traditional design rules are not optimized according to low-power concern, so specifications optimization is needed in low-power demand SDM design. Therefore, we try to use a suitable OTA topology, and then we optimize the power

consumption by minimizing the total current consumption of OTA such as Figure 3.1 shows in this thesis. No special technology or extra analog devices is needed, thus the chip area and cost are also lower compared to previous researches.

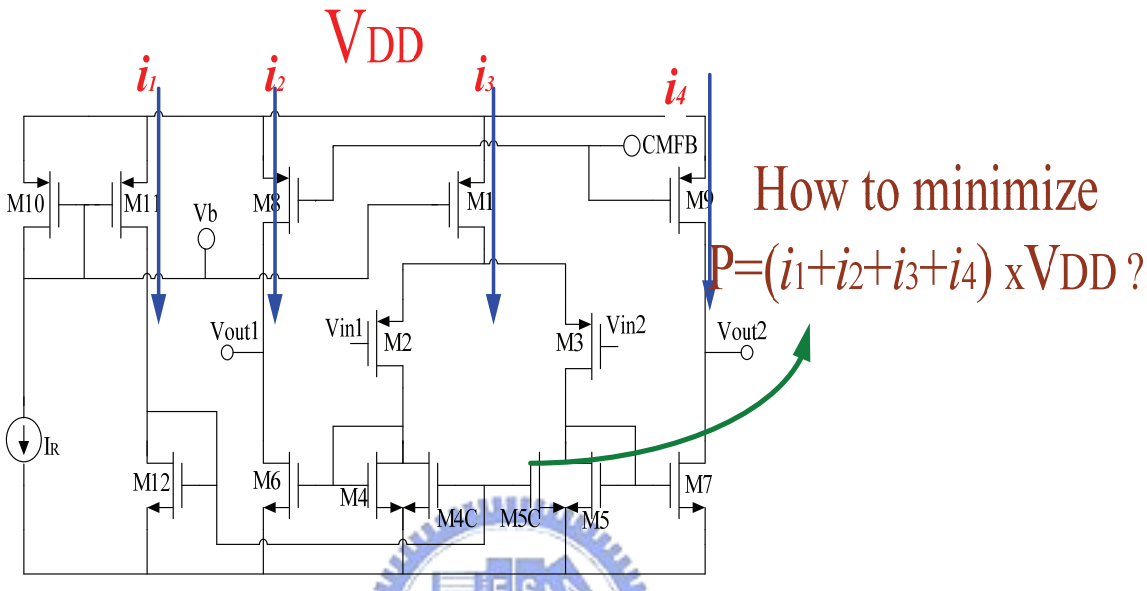

Figure 3.1 power consumption in an OTA

3.2 System Parameter Considerations

Our design goal is to achieve a lowest power consumption SDM while the target SNR (DR) is high enough for audio band portable electric devices applications. There are many trade-offs when designing a low-power SDM, thus three steps are followed in this section to determine the system parameters of the SDM, topology decision, architecture selection and coefficient decision, respectively.

3.2.1 Topology Decision

The first step to design a sigma-delta modulator is to determine the system level parameters based on the modulator specifications while the power consumption can be minimized. The power consumption formula:

$$Power = I \times V = f \times c \times \left(Vdd\right)^2 \tag{3.1}$$

Therefore, we must choose the supply voltage we used in this thesis. The basic principle is to reduce power, and in TSMC 0.18um technology, vtn+vtp～0.9v, so we choose supply voltage is one volt for some design.

The system-level parameters include oversampling ratio (OSR), the loop filter order (L), the number of the quantizer level (N).

First we decide N. Because the power consumption of the quantizer increases proportionally with N, and a multi-bit quantizer have more complicated DAC structure, thus will make whole circuit more complicated and consume more power, so for a low-power SDM design, the number of the quantizer should be minimized, so we choose N=1.

Second, because single-stage structure has more advantages on low-power design, for example simple analog circuit, good circuit mismatch characteristic, so single stage architecture is selected.

Therefore, for a target SNR, the oversampling ratio (OSR) can be made after deciding the loop filter order n:

$$SNR_{peak} = 10\log\left(\frac{P_{in}}{P_e}\right) = \frac{3}{2}\pi(2n+1)\left(\frac{OSR}{\pi}\right)^{2n+1} \quad (3.2)$$

A higher loop filler order n have more switches and integrators, lower sampling frequency, and higher order of n has more stability issue. So we have to make a trade-off between the order and the sampling frequency. If we compare different order N by simple estimation (suppose power consumption is proportional to sampling frequency), we can know that for loop filter order 2, 3, and 4, we can have similar power consumption as Table 3.3 shows.

Loop filter Order	**OSR for target SNR>60**	**Power Consumption (unit in uW)**				
		1st OP	2nd OP	3rd OP	4th OP	**Total**
1	256	160				**160**
2	64	40	20			**60**
3	48	30	15	15		**60**
4	36	22.5	11.5	11.5	11.5	**57**

Table 3.3 Power comparison of different loop filter order

Therefore, a second order architecture, 1-bit with OSR=64 is chosen because of the simplicity of the analog circuits, thus we can use simpler circuit to achieve the same target SNR.

3.2.2 Architecture Selection

The most general single stage topology in the SDM design is the CIFB architecture, and it is shown at Figure 3.2:

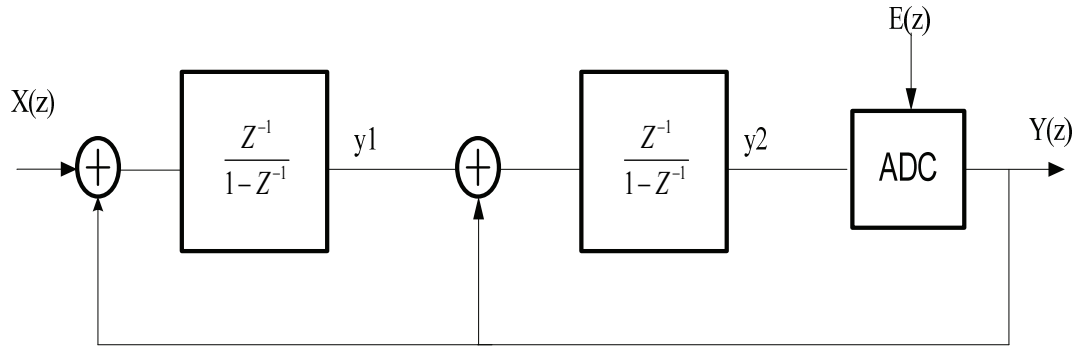

Figure 3.2 Chain of Integrators with distributed feedback(CIFB)

The input and output relation in CIFB topology can be expressed as:

$$Y(z) = Z^{-2}X(Z) + (1-Z^{-1})^2 E(Z) \tag{3.3}$$

Where the STF and NTF are given by

$$STF(z) = Z^{-2}, NTF(Z) = (1-Z^{-1})^2 \tag{3.4}$$

Where the output of integrator one and two are:

$$y1 = Z^{-1}(1-Z^{-1})X(Z) - Z^{-1}(1-Z^{-1})E(z) \tag{3.5}$$

$$y2 = Z^{-2}X(Z) - Z^{-1}(1-Z^{-1})E(z) \tag{3.6}$$

From the equations, we can know that the output signal of the integrators are the functions of input signal x(z), so if we want to have a full scale input signal x(z), than there will be a large output swing at y1(z) and y2(z),hence the power of the OPAMP will increased .

If the x(z) has a smaller input signal, than the target SNR of the modulator will be degraded. So this feature make the CIFB topology have some restriction for low-power design.

Because the nature restriction of the CIFB architecture, another architecture is chosen for low-power design [1], the CIFF architecture have some advantages, and its figure is shown at Figure 3.3:

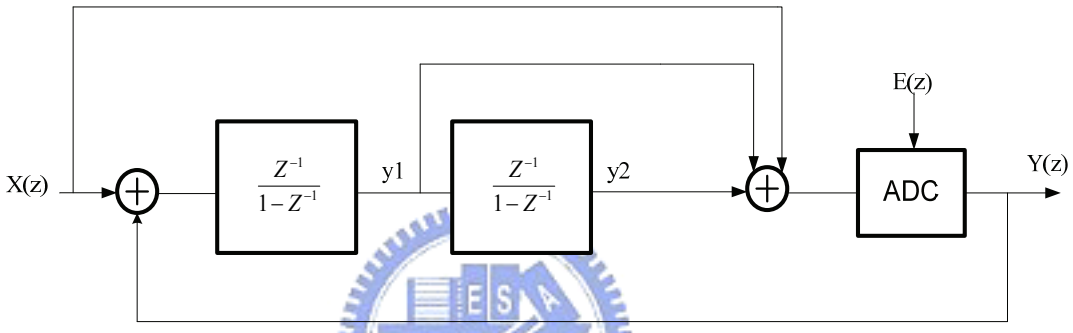

Figure 3.3 Chain of integrators with weighted feed-forward summation. (CIFF)

The input and output relation in CIFF topology can be expressed as:

$$Y(z) = Z^{-2}X(Z) + (1-Z^{-1})^2 E(Z) \tag{3.7}$$

Where the STF and NTF are given by:

$$STF(z) = 1, NTF(Z) = (1-Z^{-1})^2 \tag{3.8}$$

Where the output of integrator one and two are:

$$y1 = -Z^{-1}(1-Z^{-1})E(Z) \tag{3.9}$$

$$y2 = Z^{-2}E(Z) \tag{3.10}$$

From above equations, we observed that the output signals of two integrators y1 and y2 in CIFF structure are not contain the input signal x(z),which means that this loop filter process E(z) only, thus the output swing requirements of the loop filter will decrease ,it means that the slew-rate requirement is not critical when we design the OPAMPs in loop filter[3], so it is more suitable for low-power applications.

3.2.3 Coefficient Decision

In a general structure of CIFF sigma-delta modulator like Figure 3.4, the modulator contains five coefficients: two integrator gain (a1, a2) and three summation factor (b0, b1, b2):

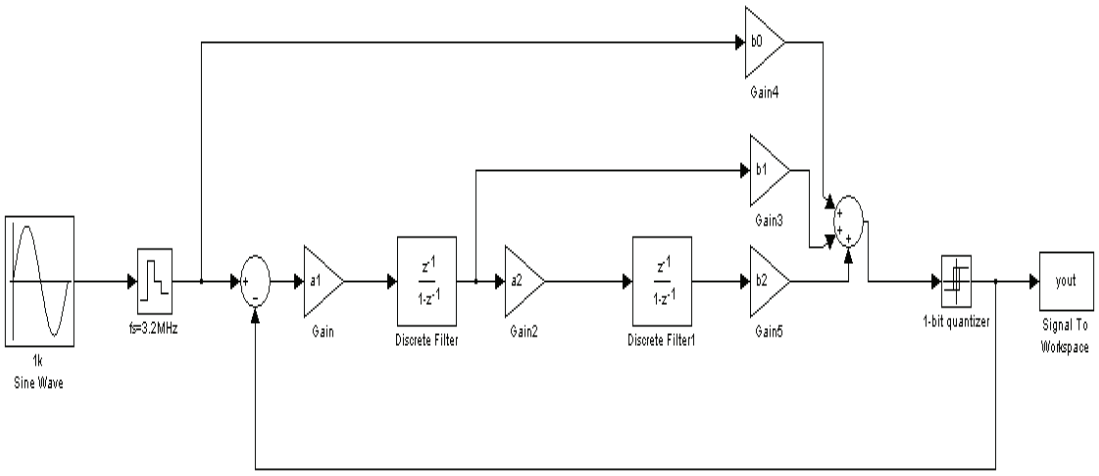

Figure 3.4 Simulink model of a 2nd-order CIFF SDM

From the Delta-Sigma Toolbox, give order=2, OSR=64, the noise transfer function (NTF) that have SNR(max):

$$NTF(Z) = \frac{(z-1)^2}{z^2 - 1.225z + 0.4415} \tag{3.11}$$

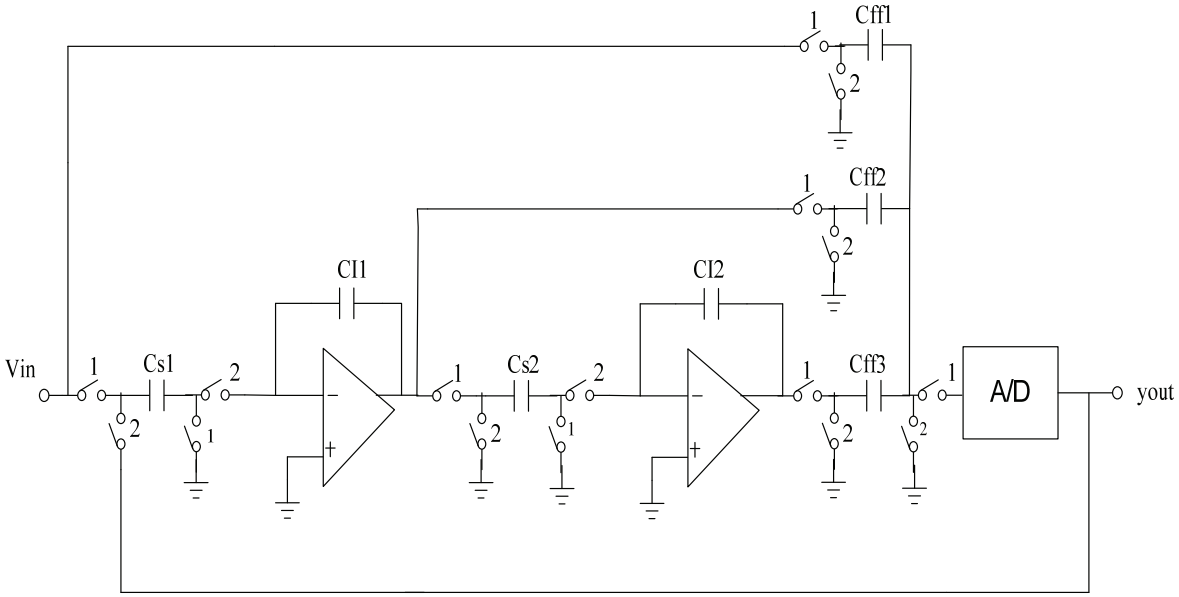

Figure 3.5 a second order CIFF SDM

And from calculation of the Figure 3.5,

$$y = x + \frac{(1-z^{-1})^2}{1+(a1b1-2)z^{-1}+(a1a2b2-a1b1+1)z^{-2}} \tag{3.12}$$

Therefore, $a1b1 = 0.775$ and $a1a2b2 = 0.2165$ must be met.

After deciding the transfer function of the SDM, we must decide which combination of (a1, a2, b1, b2, b3) we will use. Because our design target is to achieve low-power, and the most important feature of a low power SDM is that the signal swing at the loop filter output must be small.

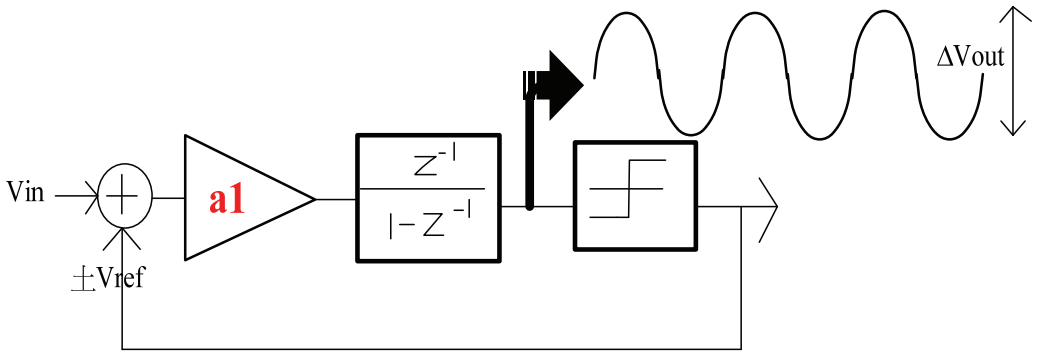

Figure 3.6 A general linear model of SDM

Figure 3.6 is a general case first-order SDM, we can know that when the coefficient a1 is larger, the output swing of the loop filter is larger ,then the power consumption is larger of the whole modulator; therefore, if we want to have a smaller signal swing, the a1 coefficient must be minimized.

However, if a1 is too small, the stability of the SDM will be degraded because the signal will overload, and the SNR will decrease, so we must make a trade-off between the coefficients.

In this work, we choose a1=0.25 and b1=3,combined above requirement, capacitor matching and the signal scaling issues, the coefficients of the second-order modulator is listed at Table 3.4:

Integrator Coefficients	Feed-Forward Coefficients
a1=0.25	b0=1
a2=1	b1=3
	b2=1

Table 3.4 Coefficient of proposed SDM

Under the coefficients, the modified NTF becomes:

$$NTF(Z)' = \frac{(z-1)^2}{z^2 - 1.25z + 0.5} \tag{3.13}$$

It cause a slightly change of the NTF pole and it will not degrade the SNR significantly.

The ideal Output spectrum of 8192-point FFT with 8k input signal is shown at Figure 3.7, the simulation result reveals that the SFDR exceed 78dB.

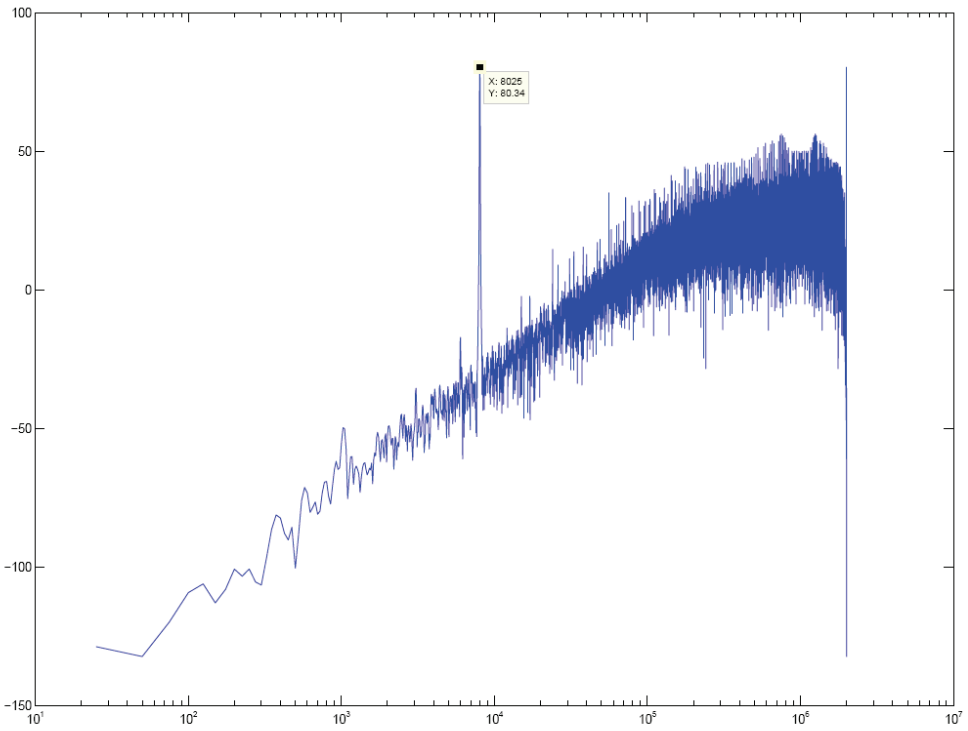

Fig.3.7 Ideal 8192 point FFT of proposed SDM architecture

3.3 Non-idealities Considerations

The above simulations show an ideal model of the second-order sigma-delta modulator. However, there are some non-ideal effects in analog circuit design and it is unavoidable, so we must evaluate the non-ideal effect to make our designs meet the desired margin.

3.3.1 Gain requirement

The transfer function of an ideal integrator:

$$H(z) = \frac{Z^{-1}}{1 - Z^{-1}} \tag{3.14}$$

However, the gain of OTA cannot be infinite in circuit design, when a finite gain is A in an OTA, the transfer function will become:

$$H(z) = \frac{Z^{-1}}{1 - (1 - \varepsilon)Z^{-1}} \tag{3.15}$$

Where $\varepsilon = \frac{1}{A} \cdot \frac{C_S}{C_I}$

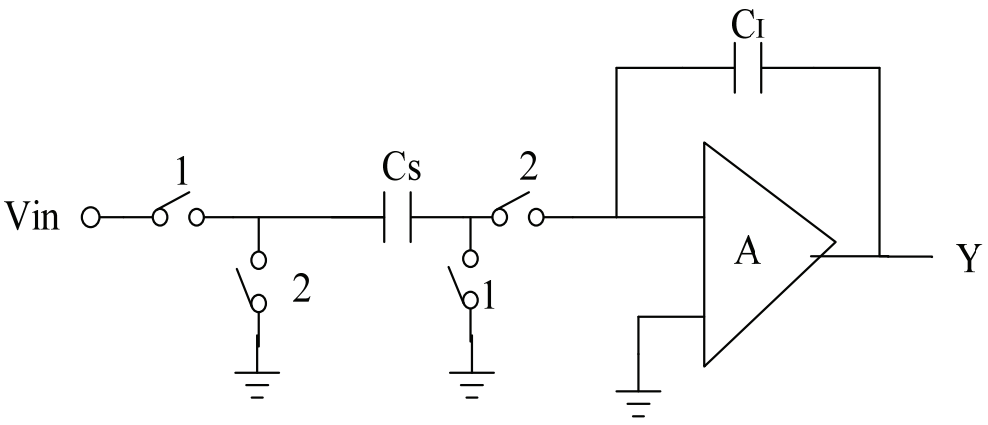

Figure 3.8 a switched-capacitance circuit in SDM

A finite gain of OTA means that the pole of the H(Z) will depart from unit circle, and when the distance of the zero exceed about $\frac{\pi}{OSR}\cdot\frac{C_{I1}}{C_{S1}}$, the noise attenuation of NTF begins to degrade, so the lower limit of A is about 40 dB[10].

3.3.2 Settling of the OTA

In a switched-capacitance circuit, the loop filter can be separately into two parts, namely the sampling period and the integration period, as shown at Figure 3.9:

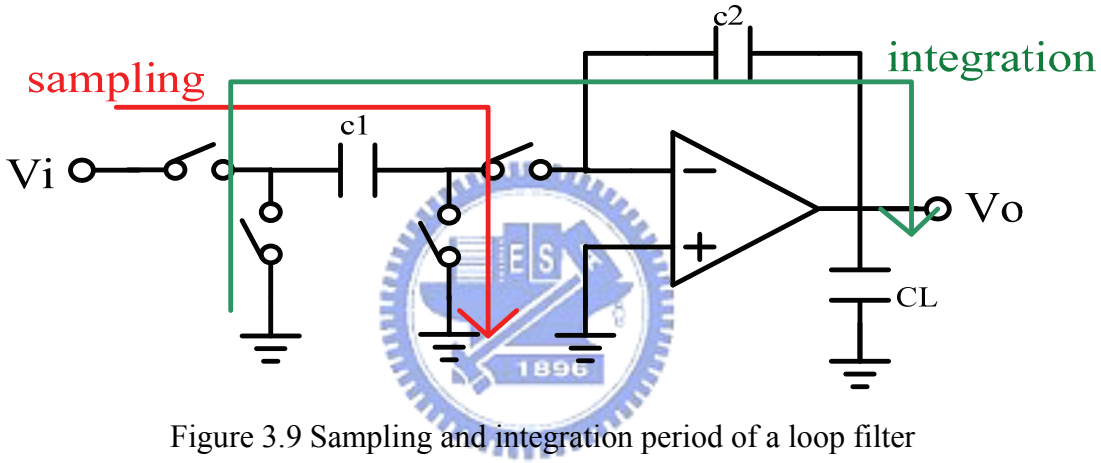

Figure 3.9 Sampling and integration period of a loop filter

When the loop filter is at integration period, the settling behavior of the OTA can be derived as the Figure 3.10. A slewing is happened when a large output change of the loop filter. When the differential input voltage is less than $\sqrt{2}V_{OV}$, the OTA enters linear settling region. Because of the speed limitation of the OTA, settling error will occur at the end of integration period as the Figure 3.10 shown, so we must take settling error into consideration when designing OTA.

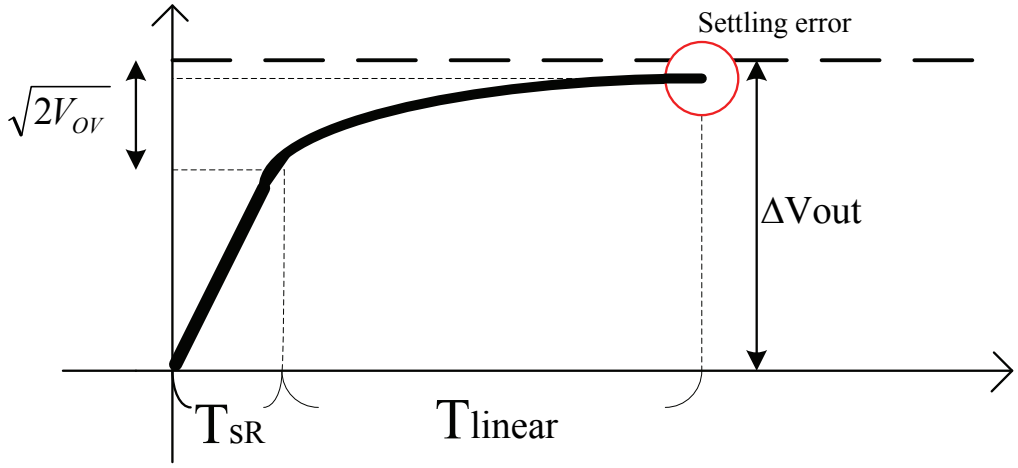

Figure 3.10 Settling behavior of OTA

3.3.3 Capacitor Sizing

The input-referred thermal noise of the integrator is:

$$V_n^2 = \frac{KT}{C_s}, \tag{3.16}$$

Where Cs is sampling capacitor of the integrator.

With an oversampling ratio of OSR, the in-band KT/C noise:

$$V_n'^2 = \frac{KT}{C_s \cdot (OSR)} \tag{3.17}$$

And if for a full scale input amplitude, the in-band noise power must be at least 85dB below the signal power:

$$V_n'^2 \le 10^{-8.5} \cdot \left(\frac{V_{DD}}{2}\right)^2 \cdot \frac{1}{2} \tag{3.18}$$

⇨
$$C_S > \frac{8KT \cdot (SNR\_peak)}{V_{DD}{}^2 \cdot (OSR)} \tag{3.19}$$

⇨ It can be calculated that Cs> 0.163pF

The simulation result of first sapling capacitor is shown at Figure 3.11, from the figure we choose C_{S1}=0.5pF for safety noise margin.

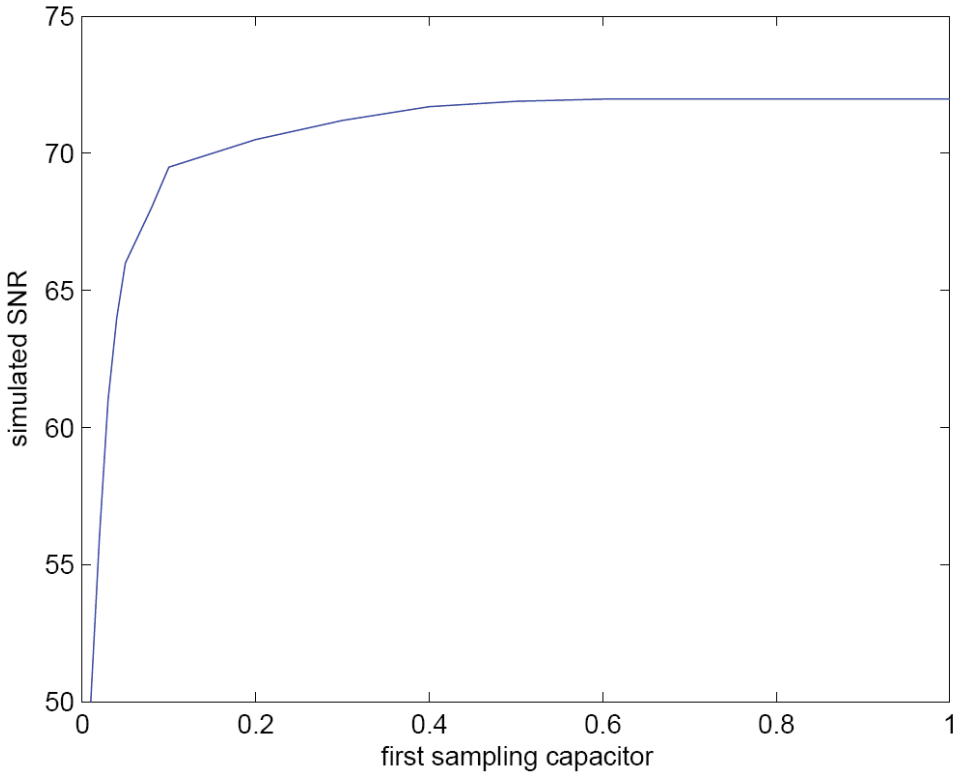

Figure 3.11 Simulation result of the first sampling capacitor

The KT/C noise at the input of the second integrator is shaped by the first-order noise shaping, so that Cs2 can be scaled down since its effect of thermal noise is fewer. In this SDM system, we choose C_{S2}=0.2pF.

Chapter 4
Circuit Implementation

The proposed sigma-delta modulator has been fabricated in TSMC 0.18um single-poly six-metal CMOS process. The circuitry is operating at a supply voltage of 1 volt. The sub-blocks which including OTA, comparator, clock generator and switched capacitor circuit in SDM are described in Section 4.1. In Section 4.2, the simulation results of sub-blocks and whole SDM are presented. In Section 4.3, the final layout design of proposed SDM is then described.

4.1 Transistor Level Design

After considering the system parameters and non-idealities of proposed SDM, the following is the circuit implementation. The sub-circuit of each component in this modulator is presented including OTA, 1-bit quantizer, clock generator, switched capacitor circuit, respectively.

4.1.1 Differential OTA in loop filter

The OTA in loop filter is the analog block which consumes the most power, and it also dominant the performance of the modulator, so it is the most critical building block that we must design it seriously.

In previous researches, a single stage OTA must used because it doesn't have to waste extra current in driving the compensated capacitance[4], and although the class-AB OTA is the most widely used OTA architecture when designing a low power SDM, it requires extra paths to drive the transistor of output stage[9]; Therefore, a single-stage class-A Amplifier with positive feedback to increase its gain is used in this design, as shown in Figure 4.1, We use PMOS as the input transistor because of two reasons:

(1)The input common mode voltage (ICM) is low than Vt

(2)The noise of PMOS input pair is smaller than NMOS

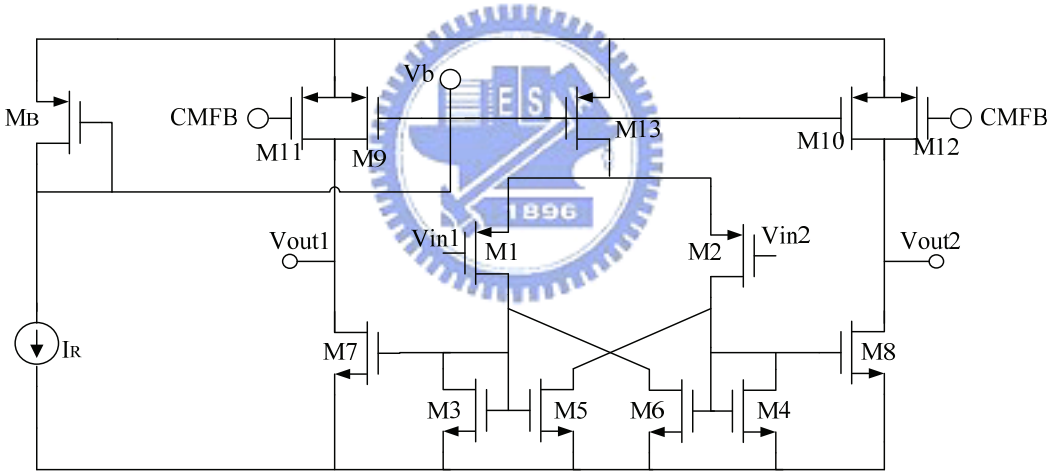

Figure 4.1 Single Stage Class-A OTA with positive feedback

An OTA in loop filter works at the integration period, and the settling behavior of the OTA can be divided into two parts, the slewing and the settling time. A slewing is happened when a large output change of the loop filter. When the differential input voltage is less than $\sqrt{2}V_{OV}$, the OTA enters linear settling region, with a 2MHz clock, the integration period is 250ns, so that:

$$T_{SR} + T_{settling} = 250ns \tag{4.1}$$

A trade-off between the slewing time and linear settling time means different settling behavior of the OTA. The proposed optimization technique is to find the optimization of slewing-settling trade-off as shown in Figure 4.2, thus the total current consumption of the OTA can be minimized, and the analysis is followed.

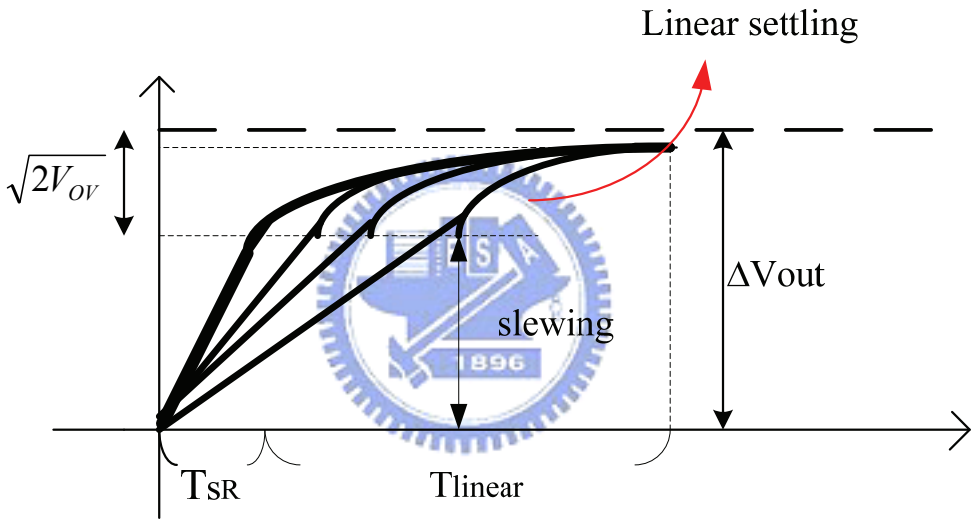

Figure 4.2 trade-off between slewing and linear settling

The slewing behavior is related to the current of output path:

$$2I_{out} = \frac{C_{load} \cdot \Delta V}{T_{SR}} \tag{4.2}$$

For a load capacitance of 2.5pf and a v=0.5, we can derive that:

$$I_{out} = \frac{4.49x10^{-13}}{T_{SR}} \tag{4.3}$$

The speed of the OTA settling is depend on its time constant, therefore , the unit gain bandwidth, therefore the input path current of the OTA, we set the linear settling period is larger than 10 time constant , thus the settling error is lower than 85dB.

Therefore,

$$T_{linear} \geq 10\tau \tag{4.4}$$

So, the unit-gain bandwidth:

$$GBW = \frac{1}{2\pi\tau} = \frac{1.59}{T_{linear}} \tag{4.5}$$

And, $GBW = \frac{g_{m1}}{2\pi C_L}\frac{B}{1-\alpha}$ for the input of the OTA,

$$\rightarrow \quad g_{m1} = GBW \cdot 2\pi \cdot C_{load}\frac{1-\alpha}{B} = \frac{2I_{in}}{V_{GS}-V_t} \tag{4.6}$$

$$\rightarrow \quad I_{in} = \frac{1.59}{T_{linear\ t}}\ (V_{GS}-V_t)2\pi \cdot C_{load}\frac{1-\alpha}{B} \tag{4.7}$$

For $V_{OV} = 0.1v, \alpha = 0.25, B = 4$, we can derive that:

$$I_{in} = \frac{0.78x10^{-13}}{T_{linear}} \tag{4.8}$$

From (3.16) and (3.21) we can know that the total current consumption of the OTA:

$$I_{total} = 2(I_{in} + I_{out}) = \frac{8.98x10^{-13}}{T_{SR}} + \frac{1.56x10^{-13}}{T_{linear}} = \frac{8.98x10^{-13}}{T_{SR}} + \frac{1.56x10^{-13}}{250 - T_{SR}} \tag{4.9}$$

Therefore, we can optimize the OTA to minimize the total current consumption of the OTA by plotting it as a function of the slewing time such as Figure 4.3:

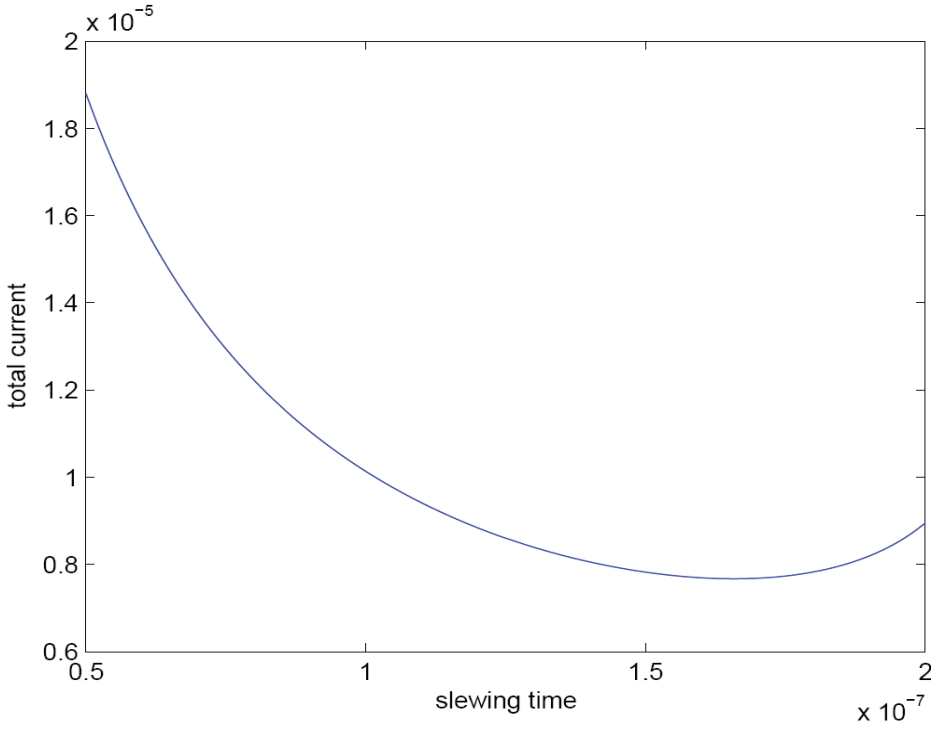

Figure 4.3 Slewing time versus total current of the OTA

From this figure, we know that the minimum current occurs at T_{SR}=160~170ns. However, when T_{SR}=170 ns is used, and we can calculate that:

$$I_{in} = \frac{0.78x10^{-13}}{T_{linear}} = 1.3uA \tag{4.10}$$

$$I_{out} = \frac{4.49x10^{-13}}{T_{SR}} = 2.56uA \tag{4.11}$$

Then the coefficient B of the OTA is about 3, which departs from our assumption, so we must decrease the T_{SR} so that the B is close to 4, we modify the slewing time so that T_{SR}=130ns as Figure 4.4 plots, therefore:

$$I_{out} = \frac{4.49x10^{-13}}{T_{SR}} = 3.45uA \tag{4.12}$$

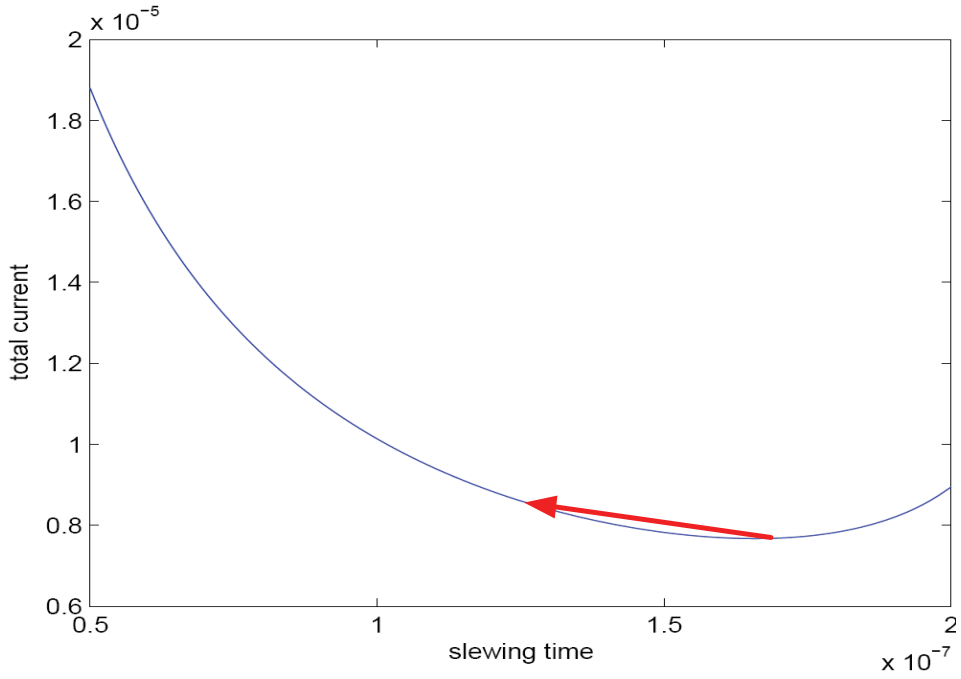

Figure 4.4 modification of the slewing time

Therefore, the current consumption of our calculation can be simplified as Figure 4.5:

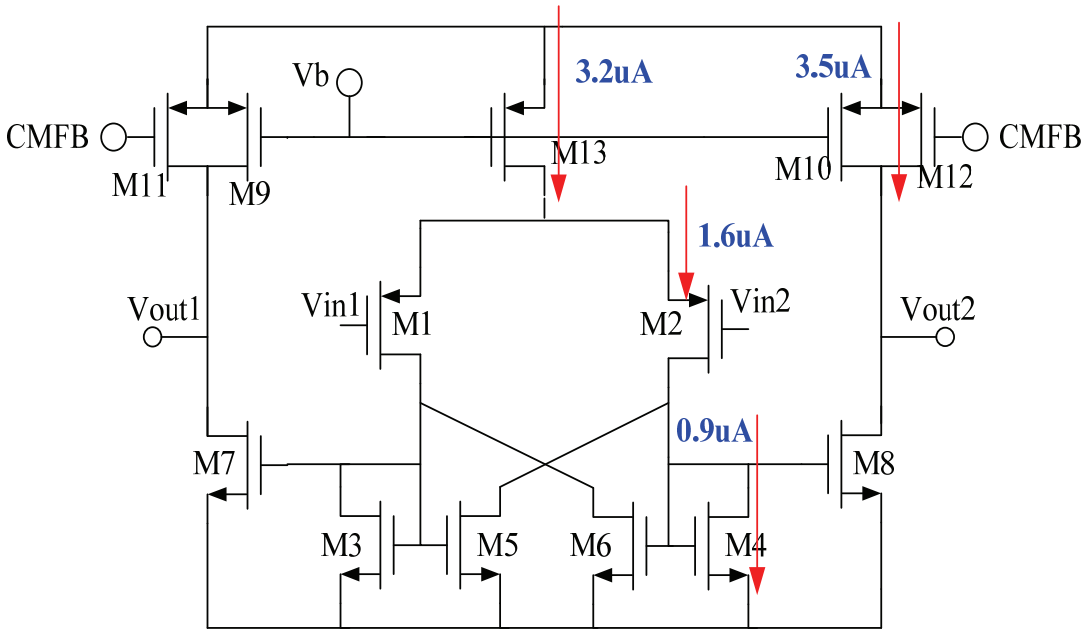

Figure 4.5 Current consumption of first OTA

The transistor size summary of the first OTA is shown at Table 4.1:

Transistor	W	L	M
M1,2	1	0.8	4
M3,4	0.6	0.8	1
M5,6	0.48	0.8	1
M7,8	0.6	0.8	4
M9,10	4.16	1.5	1
M11,12	4.16	1.5	3
M13	2	1.5	8

Table 4.1 Device ratio summary of first OTA

The decision of the size is based on the following principles:

(1) Tune M13 that the current of M13 as we want and the overdrive voltage= 100mv.

(2) Tune M1, M2 to meet the gm and Fu specification.

(3) Tune M3~M6 to adjust the second pole, and the positive feedback gain is 0.8 at the same time.

(4) Tune M7, M8 to meet the assumption that B=4 we used above.

(5) Tune M9~12 that the output stage has a output closed to 0.5Vdd, and the gain of the whole OP exceed 50dB.

A larger length of the transistor is used (0.8um) is because that the overdrive voltage, low current and corner consideration. In order to achieve a low-power and stable OTA, some area is trade for our requirement.

The design procedure of the second stage OTA is similar to the first one, except that B=4 we used in first OTA is adjust to B=2 in second stage due to the parasitic capacitance at the output of this OTA is smaller than the first OTA, thus the power consumption can be lowered as Figure 4.6 is shown:

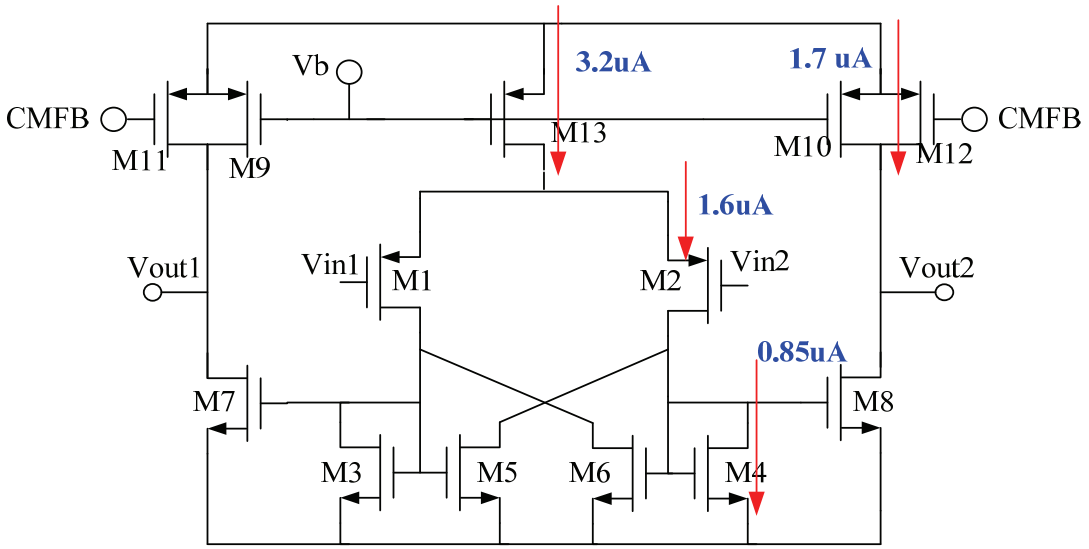

Figure 4.6 Current consumption of second OTA

The performance summary of the first OTA is listed at Table 4.2:

Specification	Result
Gain	61.9dB
Unit Gain Bandwidth	22.2MHz
Phase Margin	37°
Slew Rate	3.8 v/us
Settling Time Constant	12ns
Output Swing	800mv
Power Dissipation	10.14uW

Table 4.2 Summary of first OTA simulation results

The comparison of the two OTA for a 2.5pf loading capacitance is listed at Table 4.3, and the frequency response of the first OTA is shown at Figure 4.7:

	Gain(dB)	GBW	Total Power
OTA1	61.9dB	22.2MHz	10.14uW
OTA2	61.6dB	15.1MHz	6.67uW

Table 4.3 Performance comparison of the two OTA

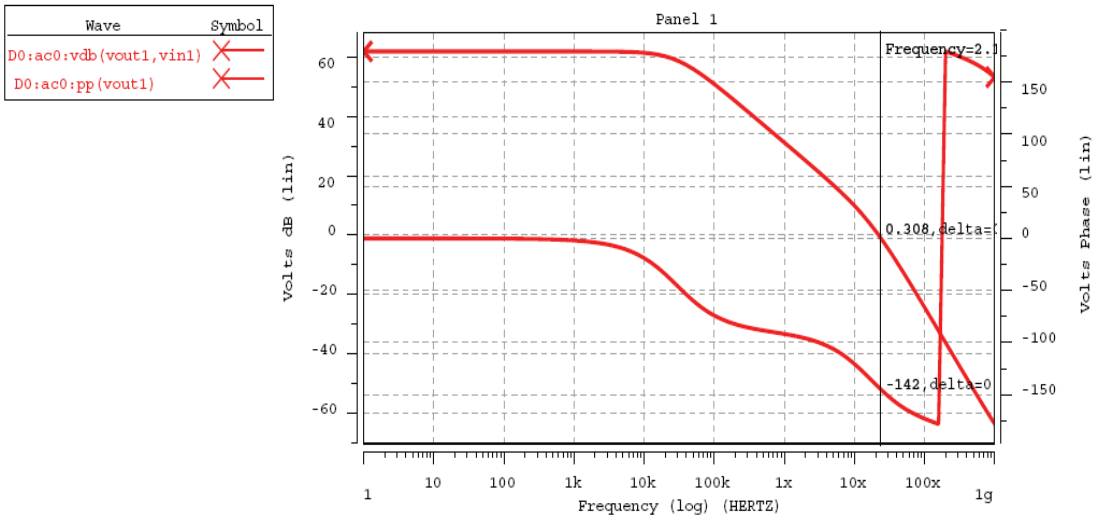

Figure 4.7 Frequency Response of first OTA

The comparison of the OTA before and after this current optimization technique is listed at Table 4.4. It shows that the total current consumption is form 14.5uA to 10.2 uA. It means at least 30.1% current reduction in OTA.

OP Architecture	Fs (MHz)	UGBW (MHz)	SR (v/us)	Iin	Iout	Power (uW)
Switched-OP[2]	1	10	3.3			78/16
Gain-enhancement[4]	4	57	X			80
One stage positive feedback[9]	2	37	X			20
Traditional specification (the same architecture)	2	**10**	**7**	0.8	6.45	**14.5**
Proposed optimize method		**22**	**3.8**	1.6	3.5	**10.14**

Table 4.4 Comparison before/after current optimization

Because of the differential architecture of the OTA, so we must have a CMFB circuit, thus a dynamic CMFB circuit like Figure 4.8 is used because it is the most power-efficient. In the CMFB circuit, Vcmo is set to 0.5v and only the switch connect to CMFB use CMOS switch, other switches is PMOS switch only.

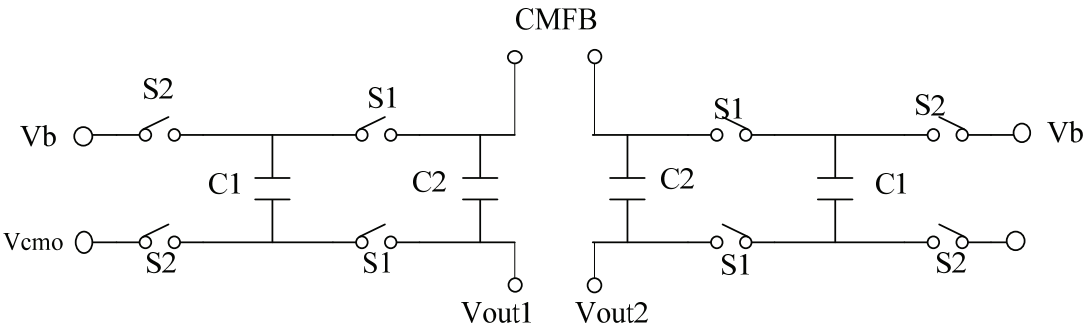

Figure 4.8 Dynamic CMFB circuit

The device ratio summary we used in CMFB circuit is listed at Table 4.4, and the transient response of the first OTA and CMFB circuit is shown below at Figure 4.9:

Transistor Type	W/L	Transistor Type	W/L
PMOS	2/0.6	NMOS	1/0.3
Capacitor	Value	Capacitor	Value
C1	0.1pf	C2	0.4pf

Table 4.5 CMFB circuit summary

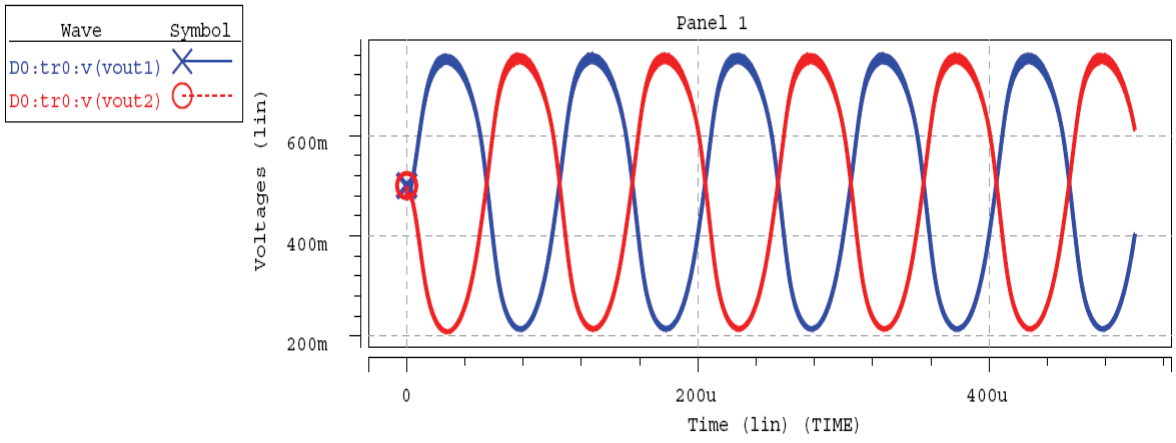

Figure 4.9 Transient Response of first OTA output

4.1.2 1-bit Quantizer

The 1-bit quantizer is realized with a comparator and a SR latch, shown at Figure 4.10. The comparator is a dynamic comparator to lower average power consumption, when CLK is high, the comparator compares the two input voltage, then the comparison result is followed by the SR latch behind the comparator.

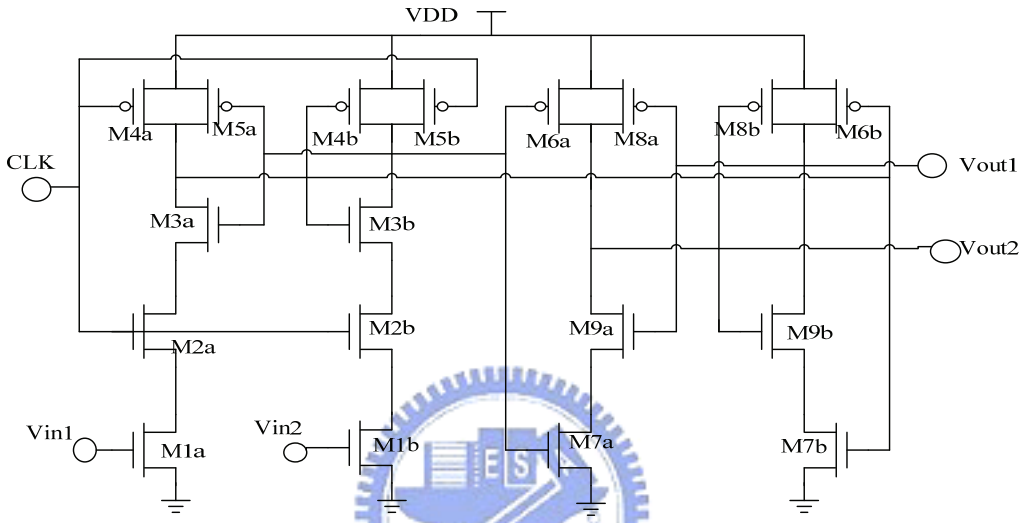

Figure 4.10 a power-efficient 1-bit quantizer

The simulation result of the 1-bit quantizer is shown at Figure 4.11, for a 16KHz input signal and a clock of 4MHz, the quantizer compare the input signal correctly. After the simulation result, the device ratio of the quantizer is listed at Table 4.6.

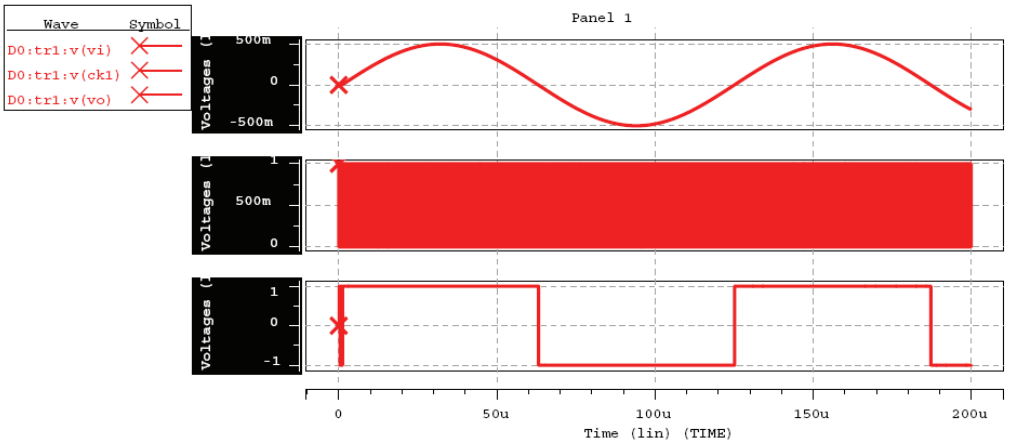

Figure 4.11 Simulation results of the 1-bit quantizer

	Width(um)	Length(um)	M
M1a,b	2.5	0.5	2
M2a,b~M5a,b	0.5	0.18	1
M6a,b	0.5	0.18	5
M7a,b	0.5	0.18	1
M8a,b	0.5	0.18	5
M9a,b	0.5	0.18	1

Table 4.6 Quantizer transistor size summary

4.1.3 Clock Generator

The on-chip clock generator is shown as Figure 4.12, an external clock input signal is buffered and then two non-overlapping clock phases are generated. To avoid the signal dependent charge injection, two delayed clocks, i.e., C1d and C2d, are also be generated.

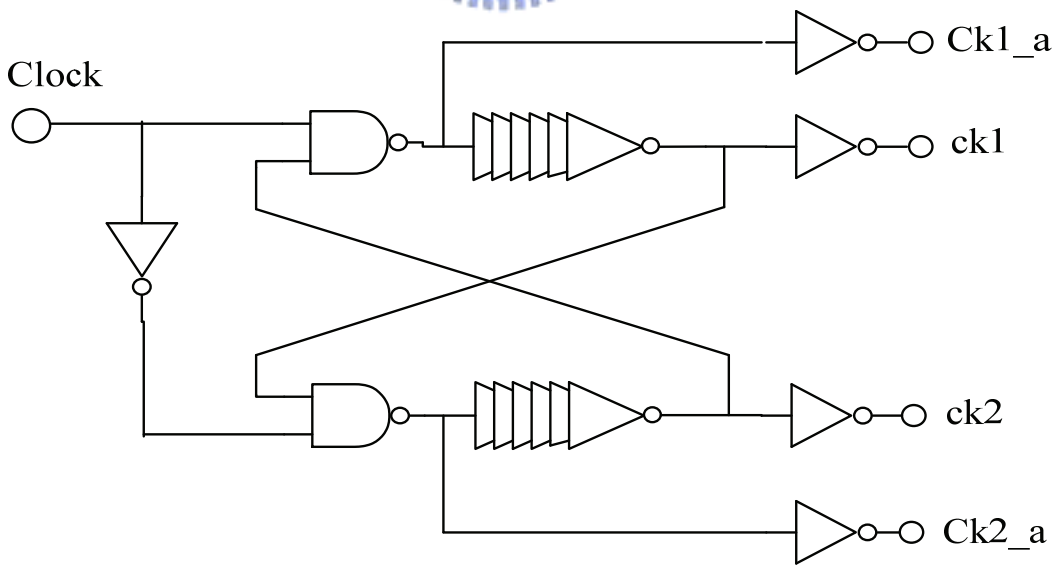

Figure 4.12 Clock generator circuit

The output of the clock generator are four different clock phases, the simulation results are shown at Figure 4.13, and Figure 4.14 shows that the phase one and two are non-overlapped each other.

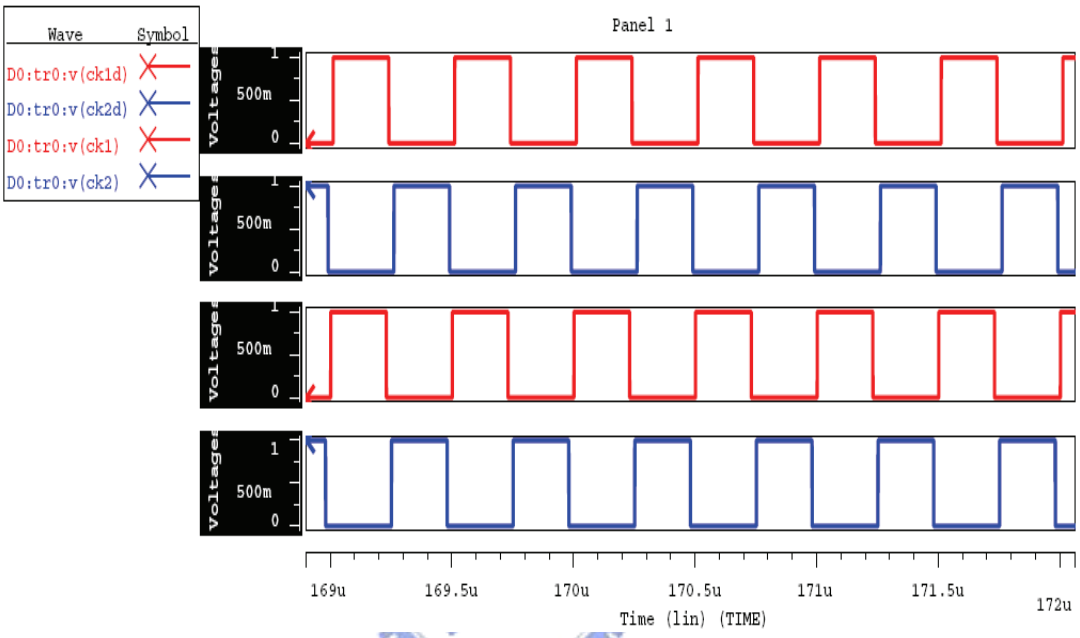

Figure 4.13 Output of the clock generator

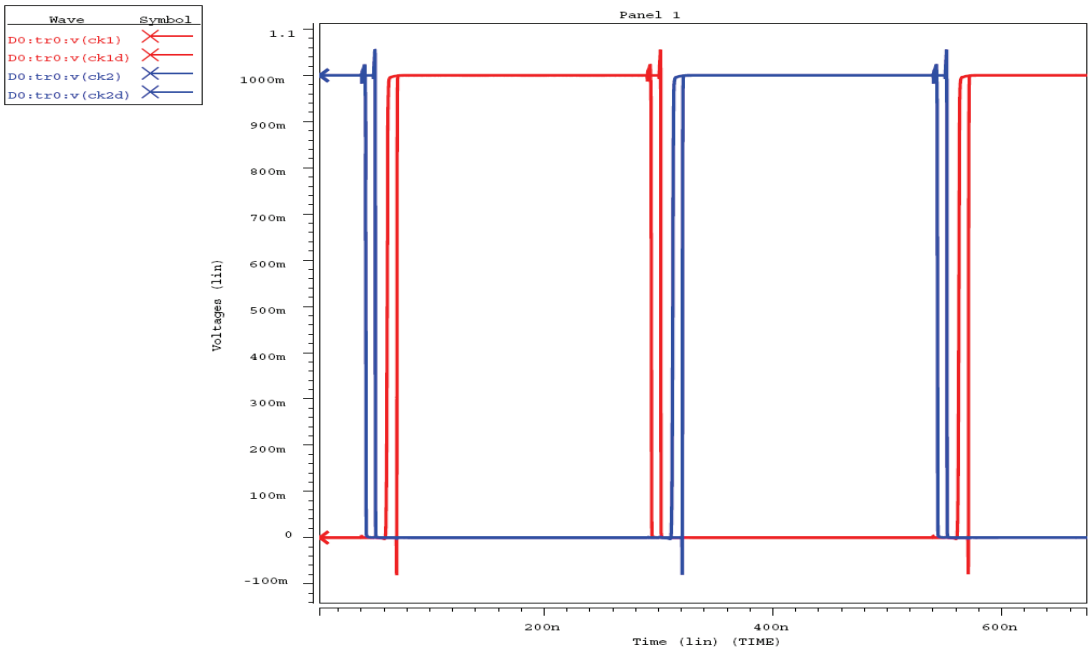

Figure 4.14 Four non-overlapping phases

4.1.4 Switches

The current of a MOS switch:

$$I_D = u_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{DS}\right)V_{DS} \tag{4.13}$$

Therefore, the turn-on resistance of the NMOS, PMOS and CMOS switches can be derived as:

$$R_{NMOS} = \frac{1}{u_n C_{OX} \frac{W}{L}(V_{DD} - V_{tn} - V_{in})} \tag{4.14}$$

$$R_{PMOS} = \frac{1}{u_n C_{OX} \frac{W}{L}(V_{in} - V_{tp} - V_{SS})} \tag{4.15}$$

$$R_{CMOS} = \frac{1}{u_n C_{OX} \frac{W}{L}(V_{DD} - V_{tn} - V_{in})} // \frac{1}{u_n C_{OX} \frac{W}{L}(V_{in} - V_{tp} - V_{SS})} \tag{4.16}$$

It is clearly that:

(1) Use NMOS switch as much as we can due to the area consideration.

(2) When the input signal of the MOS switch is large, us CMOS switch.

(3) Large ratio of W/L can lower the turn-on resistance of the switches, but have larger area and parasitic capacitance.

4.2 Modulator Design and Simulation

A second-order sigma-delta modulator with CIFF topology is done as Figure 4.15:

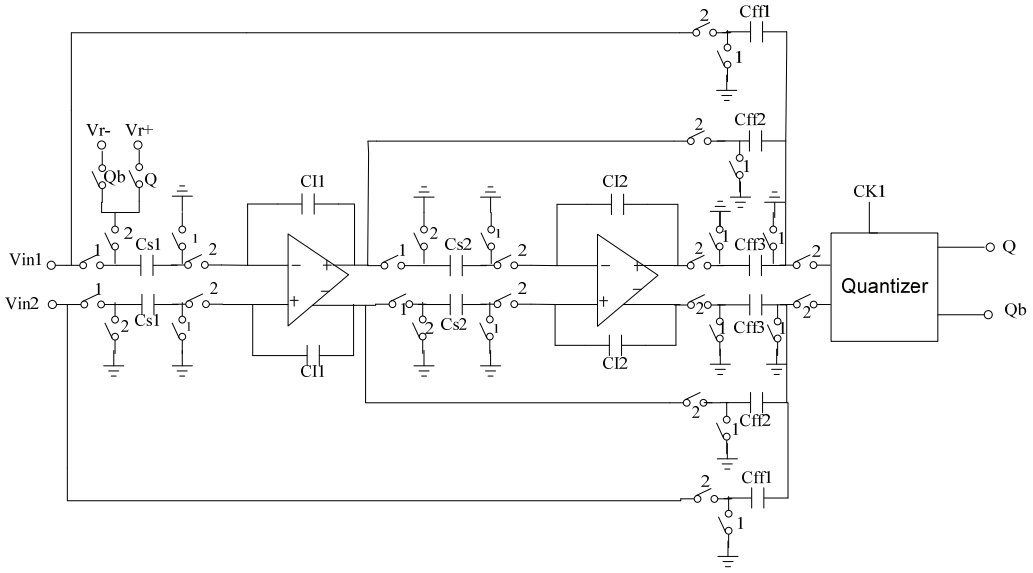

Figure 4.15 2nd order CIFF SDM

The Sigma-Delta modulator is implemented by fully differential input and output signal, the building blocks in this figure are done as we described in previous sections. With a 8k input signal and a -6dB full scale input amplitude, the simulated time-domain integrator output signal and the frequency-domain output spectrum can be observed by Figure 4.16 and Figure 4.17, respectively:

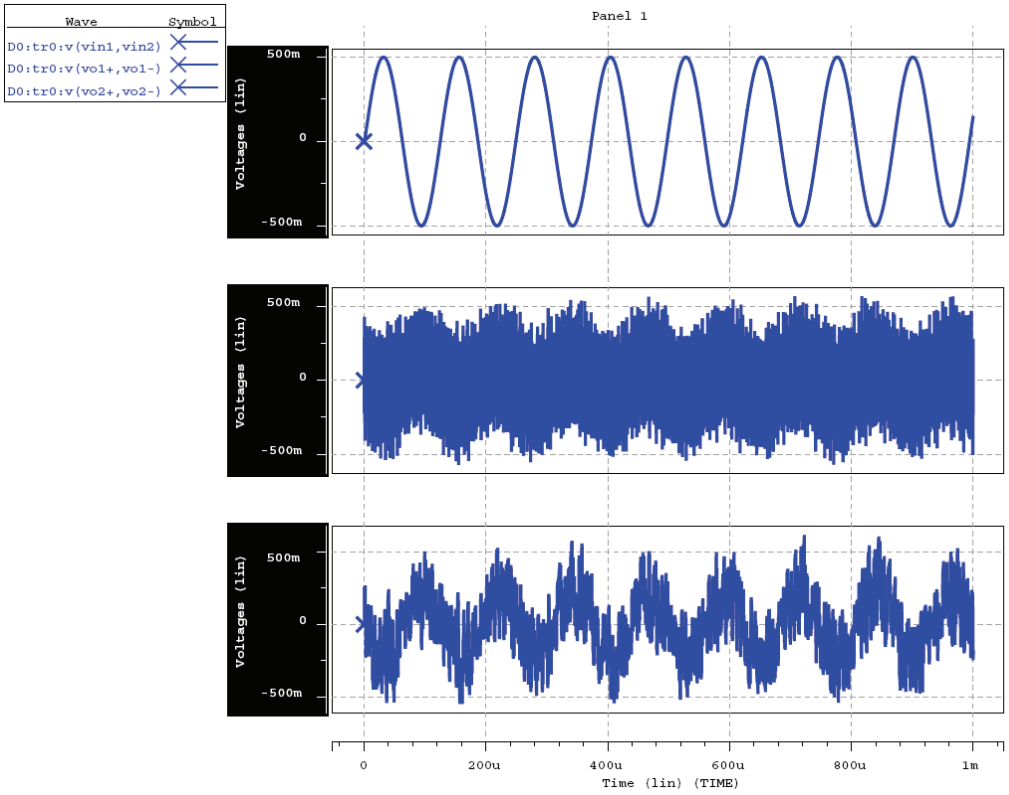

Figure 4.16 output signal of input and two integrator outputs

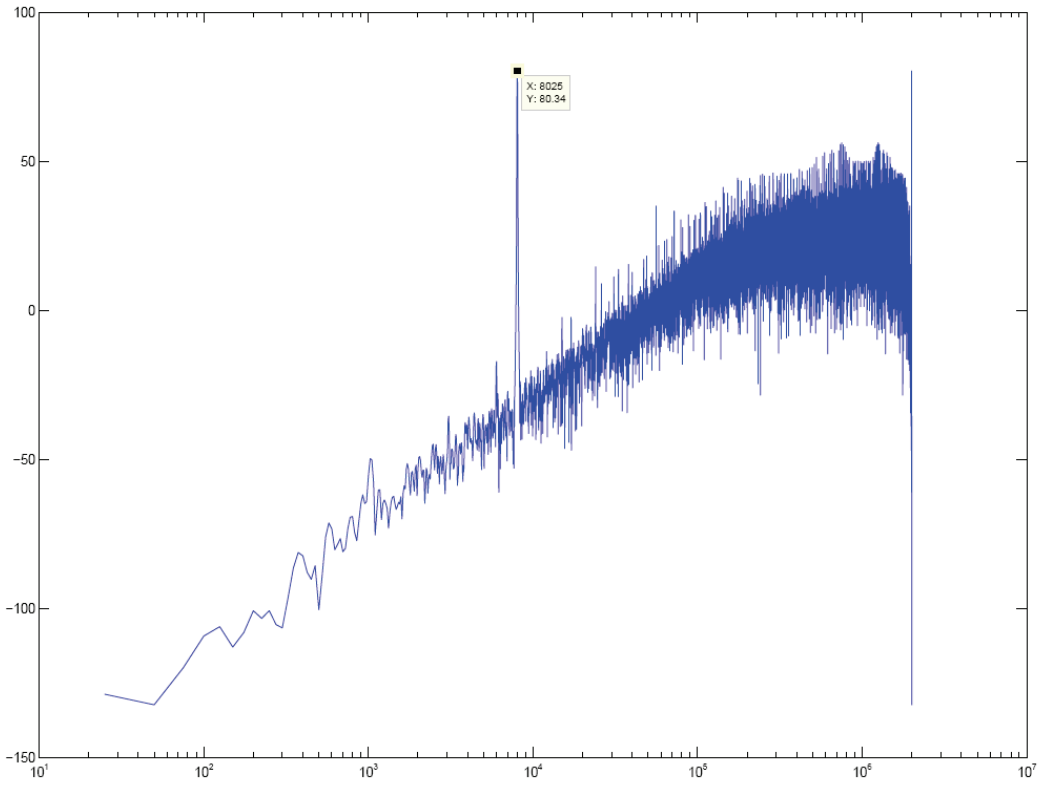

Figure 4.17 8192-point output FFT of the SDM

The FFT shows that the SNR=69.1, SNDR=68.4 and the SFDR=77.2dB, and the dynamic range (DR) is about 72dB as Figure 4.17 and Figure 4.18 shows.

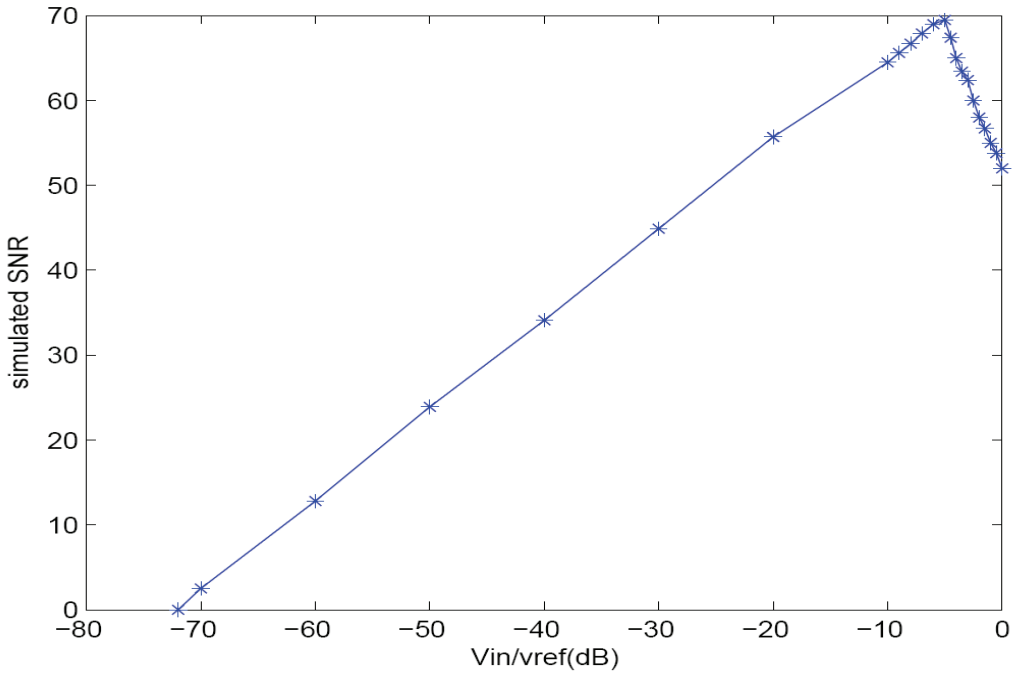

Figure 4.18 Dynamic range of the SDM

Beside this, because of the possibly process variation, we simulate the SNR results of four corners, the corner simulation results are summarized at Table 4.7.

Unit(dB)	TT	FF	SS	SF	FS
SNR	69.1	60.2	63.0	58.6	61.2
SNDR	68.4	56.9	61.1	56.6	60.3

Table 4.7 Comparison of the simulation results of four corners

4.3 Layout Level Design

A physical design in the context of integrated circuit is referred to as layout. Effects of parasitic components and mismatching will damage the performance of the chip, so layouts must be considered heavily in design process. Several principles of layout must be obeyed to minimize cross-talk, mismatches include (a) multi-finger transistors (b) symmetry (c) dummy cell (d) common centroid.

The diagram of layouts are shown at Figure 4.20, there are twenty-two I/O pads, including a pair of differential inputs, a pair of modulator outputs, a input clock, five reference voltages and eleven VDD/GND lines. The I/O pad description is listed at Table 4.7. This circuit is fabricated in a 0.18um 1P6M 1.8V standard CMOS technology with MIM process. The chip area is $0.665mm^2$ including ESD-protection I/O pads and $0.05mm^2$ for the core area.

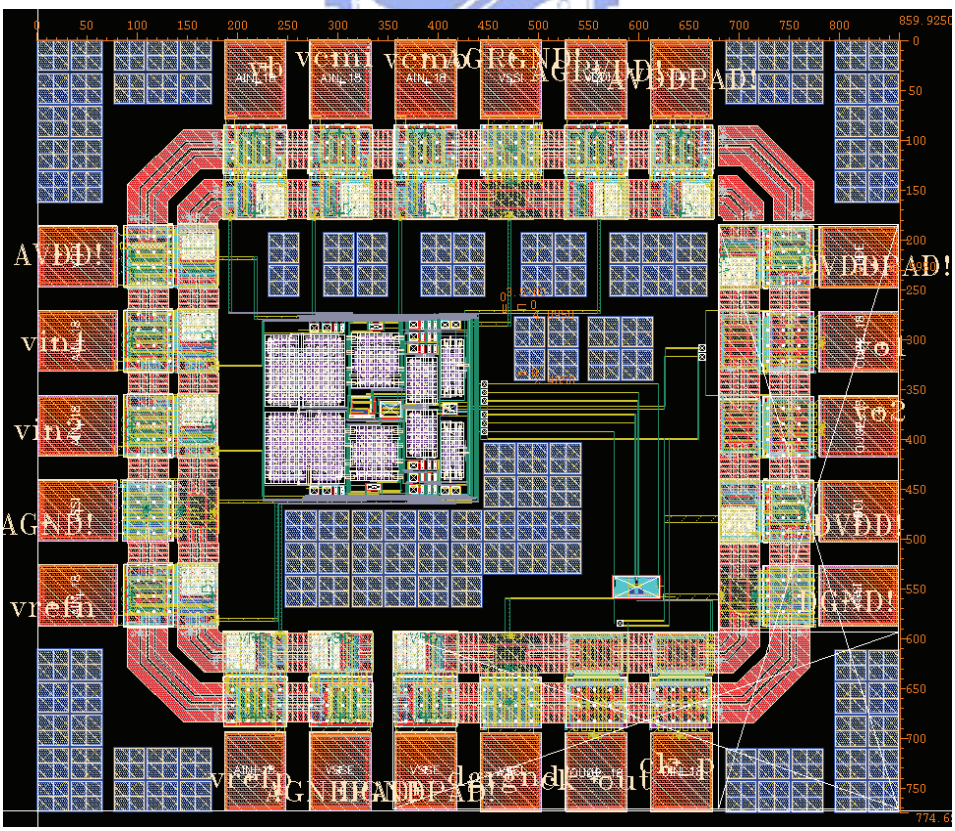

Figure 4.19 Diagram of the layout

The proposed chip is fabricated in a 0.18um 1P6M 1.8V standard CMOS technology with MIM process. And the package type is S/B type 24 pin, as shown in Figure 4.21 where the actual chip photograph is shown at Figure 4.22. The pin assignment is listed at Table 4.8.

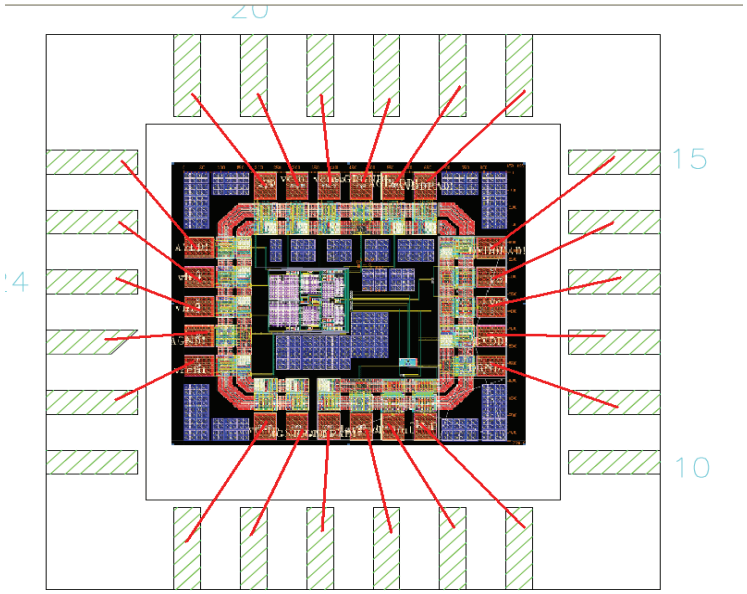

Figure 4.20 Diagram of the 24 pin DIP package

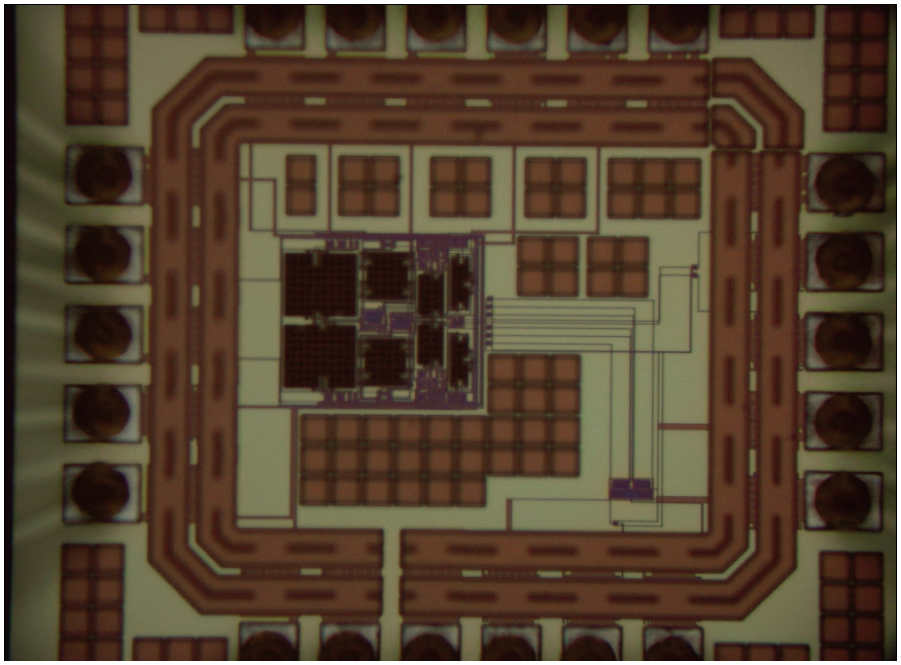

Figure 4.21 Die photograph

Pin	Name	Description
1	AGND	Analog circuit ground
2	vrefn	Reference voltage
3	NC	No connection
4	vrefp	Reference voltage
5	AGNDPAD	ESD PAD ground
6	DGNDPAD	ESD PAD ground
7	DGRGND	Digital circuit guard ring
8	Ck_out	input clock signal
9	Ck	Clock signal output
10	NC	No connection
11	DGND	Digital circuit ground
12	DVDD	Digital circuit VDD
13	Vo2	Differentail output signal
14	Vo1	Differentail output signal
15	DVDDPAD	ESD PAD Digital VDD
16	AVDDPAD	ESD PAD Analog VDD
17	AGRVDD	Analog circuit guard ring
18	AGRGND	Analog circuit guard ring
19	Vcmo	Reference voltage
20	Vcmi	Reference voltage
21	vb	Reference voltage
22	AVDD	Analog circuit VDD
23	Vin1	Differential input signal
24	Vin2	Differential input signal

Table 4.8 Pin Assignments

The 8192-point FFT of the post simulation result is shown as Figure 4.23 with an input frequency of 4k and the input amplitude is -6dB of full scale. This spectrum shows the SNR is 63.4dB while the SNDR is 58.7dB, and the comparison of pre-simulation and post-simulation is listed at Table 4.9.

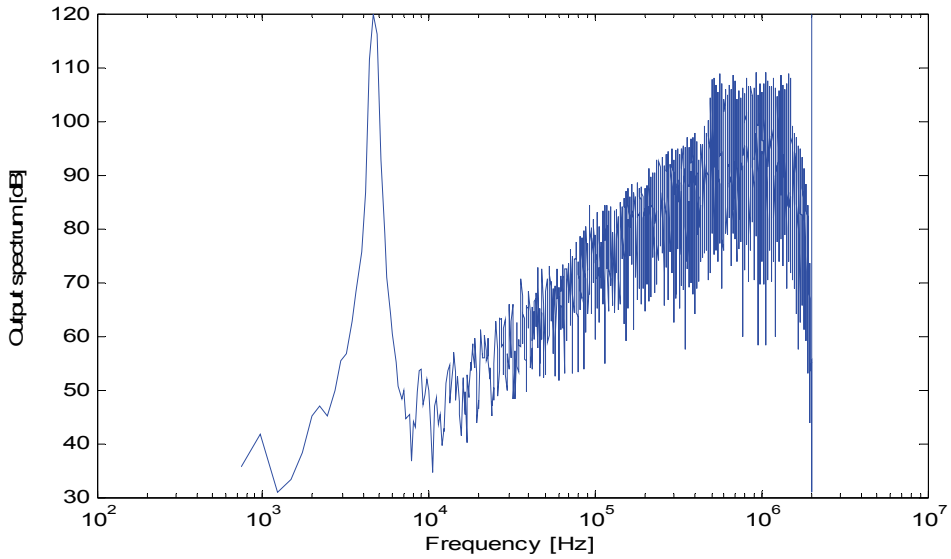

Figure 4.22 8192-point FFT of the post-simulation result

Unit(dB)	Pre-Simulation	***Post-Simulation***
SNR	69.1	***63.4***
SNDR	68.4	***58.7***

Table 4.9 Comparisons of pre & post simulation

Finally, the performance summary of the proposed SDM is listed at Table 4.10, the simulation result shows that the peak SNR is 63.4dB for a 16 KHz signal bandwidth and sampling frequency of 2MHz. With a 0.18um technology, the average power consumption is only 18uW.

Technology	**0.18um**
VDD	**1V**
Signal Bandwidth	**16KHz**
Sampling Frequency	**2MHz**
Peak SNR	**63.4dB**
Power Consumption	**18uW**
Layout Core Area Size	**240um x 210um**

Table 4.10 Summary of the proposed SDM

4.4 Comparison

The comparison of this work and previous researches are listed at Table 4.11 and Figure 4.24, in order to compare the design result, we define the figure-of-merit as:

$$FOM = SNR_{dB} + 10\log\left(\frac{BW}{P}\right)$$

	Tech	VDD	Signal BW(KHz)	OSR	PeakSNR (dB)	Active Area (mm^2)	Power	FOM
JSSC 2002[2]	0.18	0.7	8	64	67	0.082	80	147
ISCAS 2003[3]	0.18	0.9	10	100	74	0.27	38	158
JSSC 2005[5]	0.35	0.6	24	64	77	2.88	1000	151
TCASI 2006[6]	0.18	0.8	5	64	50	0.05	180	124
IMTC 2007[8]	0.18	1	25	1000	70		150	136
pre-layout simulation	**0.18**	**1**	**16**	**64**	**69.1**		**16.1**	**159.1**
post-layout simulation					**63.4**	**0.0504**	**18**	**152.9**

Table 4.11 Comparison of this work

The FOM comparison shows that the power consumption of proposed SDM is lowest compared to other researches while the FOM is still above average. The SNR versus power comparison is shown at Figure 4.24.

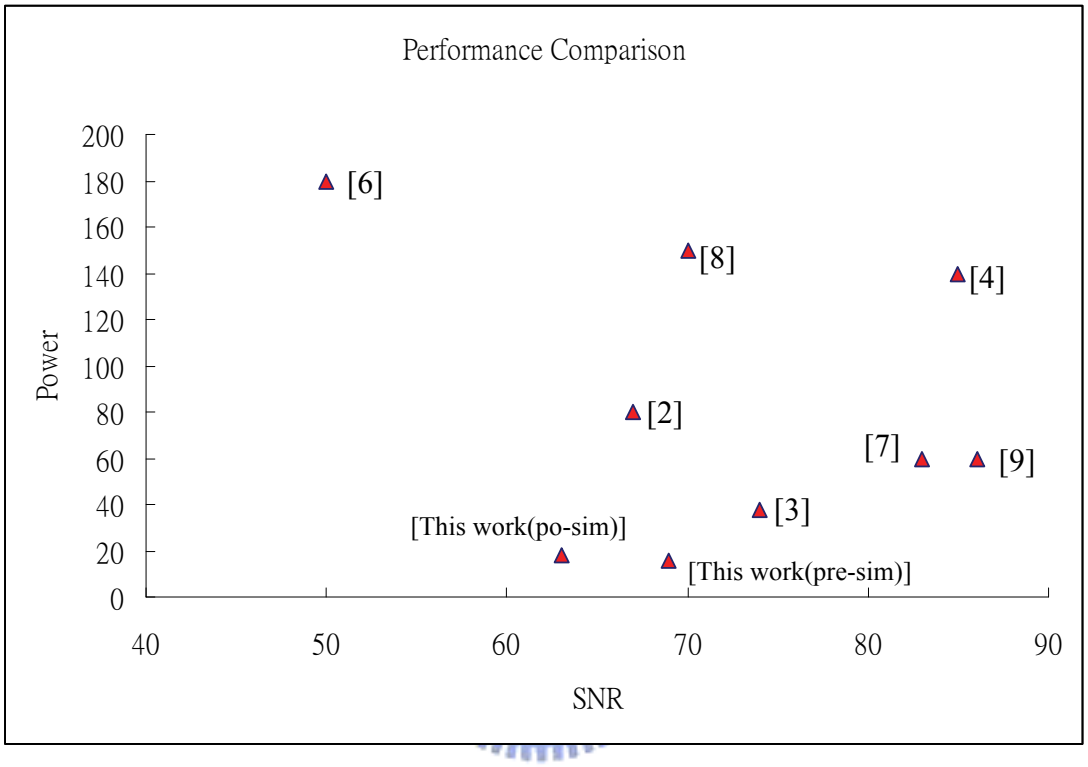

Figure 4.23 SNR versus power comparison comparisons

Chapter 5

Testing Setup and Measurement

A testing setup for fabricated chip is presented in this chapter. And a costumed designed printed circuit board (PCB) is designed and fabricated to integrate the targeting prototype chip in order to measure the performance metrics of proposed design. Following by the setup for measurement, the experimental results is presented and discussed. And the performance summary is summarized in the end of this chapter.

5.1 Testing Environment Setup

The testing environment setup is shown as Figure 5.1. It includes a printed circuit board (PCB**)** including a device under test (DUT) board, a logic analyzer (Agilent 16902A), an audio signal generator (Stanford Research DS360), a power supply (E3610A), a mixed-signal oscilloscope (Agilent 54641D) and a PC to analyze the output bit stream of proposed modulator.

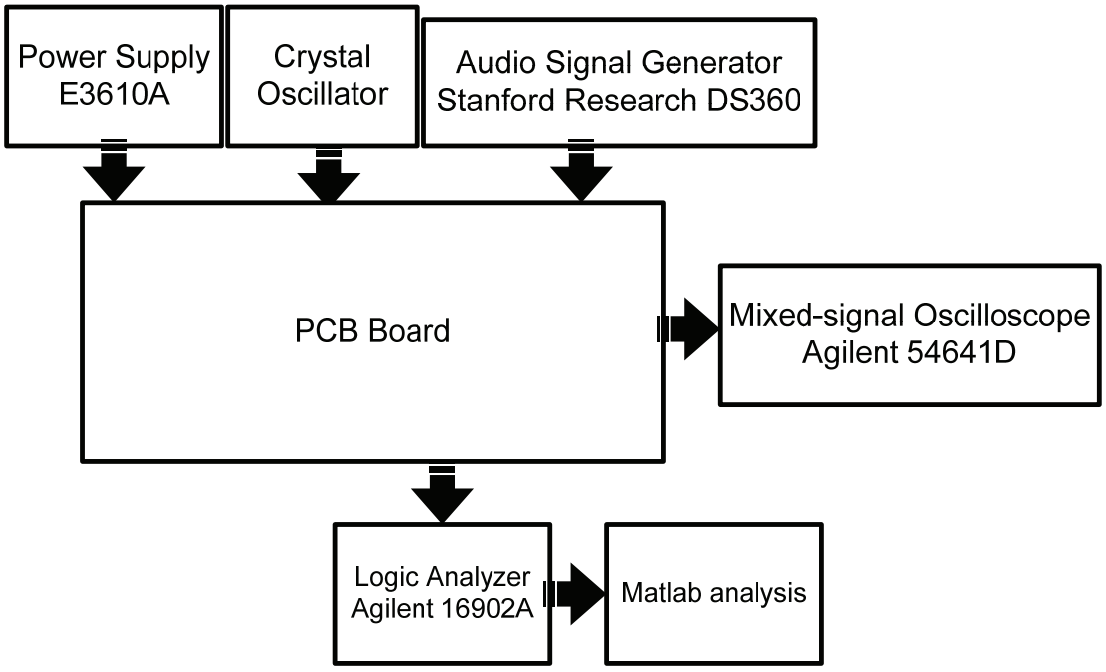

Figure5.1 experimental test chip

As shown in Figure 5.1, the input signal is generated by audio signal generator, and the digit output is fed to the logic analyzer, then load to PC for MATLAB simulation. A PCB board combines the clock generator (a crystal oscillator) and a device under test (DUT) to measure the chip. The photograph of the measurement environment is shown at Figure 5.2.

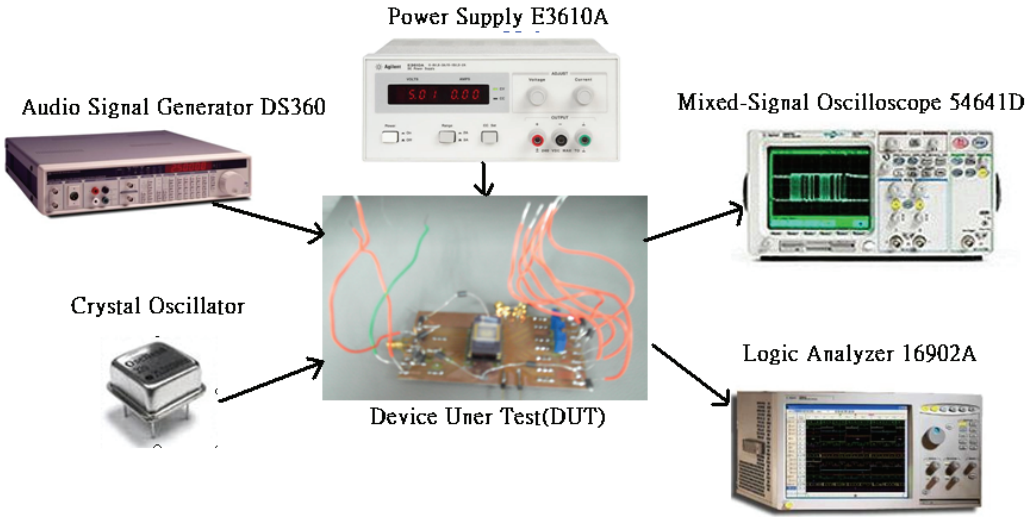

Figure 5.2 Photograph of the measurement environment

5.2 Measurement Result

The measurement result of proposed chip is failed. The probably reason is that the transistor size of the output buffer is too small to push the ESD PAD and the parasitic capacitance of the packages as Figure 5.3 shows.

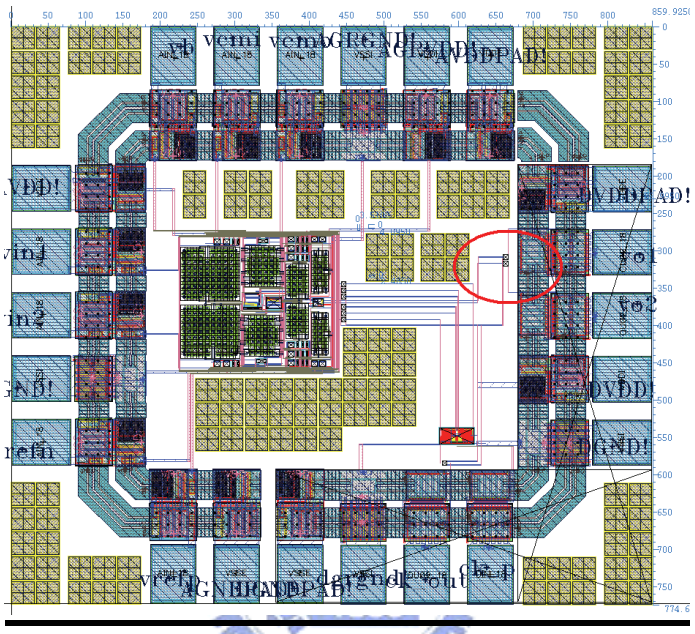

Figure 5.3 Probably problem of output buffers

Stage1	Stage 2
1um/0.18um	***4um/0.18um***

Table 5.1 Output buffer device ratio summary

Due to the problem of this layout, we modify the design as Figure 5.4, and it is modified by following principles:

1. ESD protection for analog input signals while the output pad is pure pad to reduce chip area and measuring core power of proposed SDM.
2. Wider metal for power lines.
3. Independent PAD for different supply voltage: AVDD, DVDD, IOVDD to measure the power respectively.
4. A larger output buffer of six stages is used, the device ratio is listed at Table 5.2.

Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6
1/0.18um	***3/0.18um***	***9/0.18um***	***27/0.18um***	***81/0.18um***	***243/0.18um***

Table 5.2 the modified output buffer device ratio summary

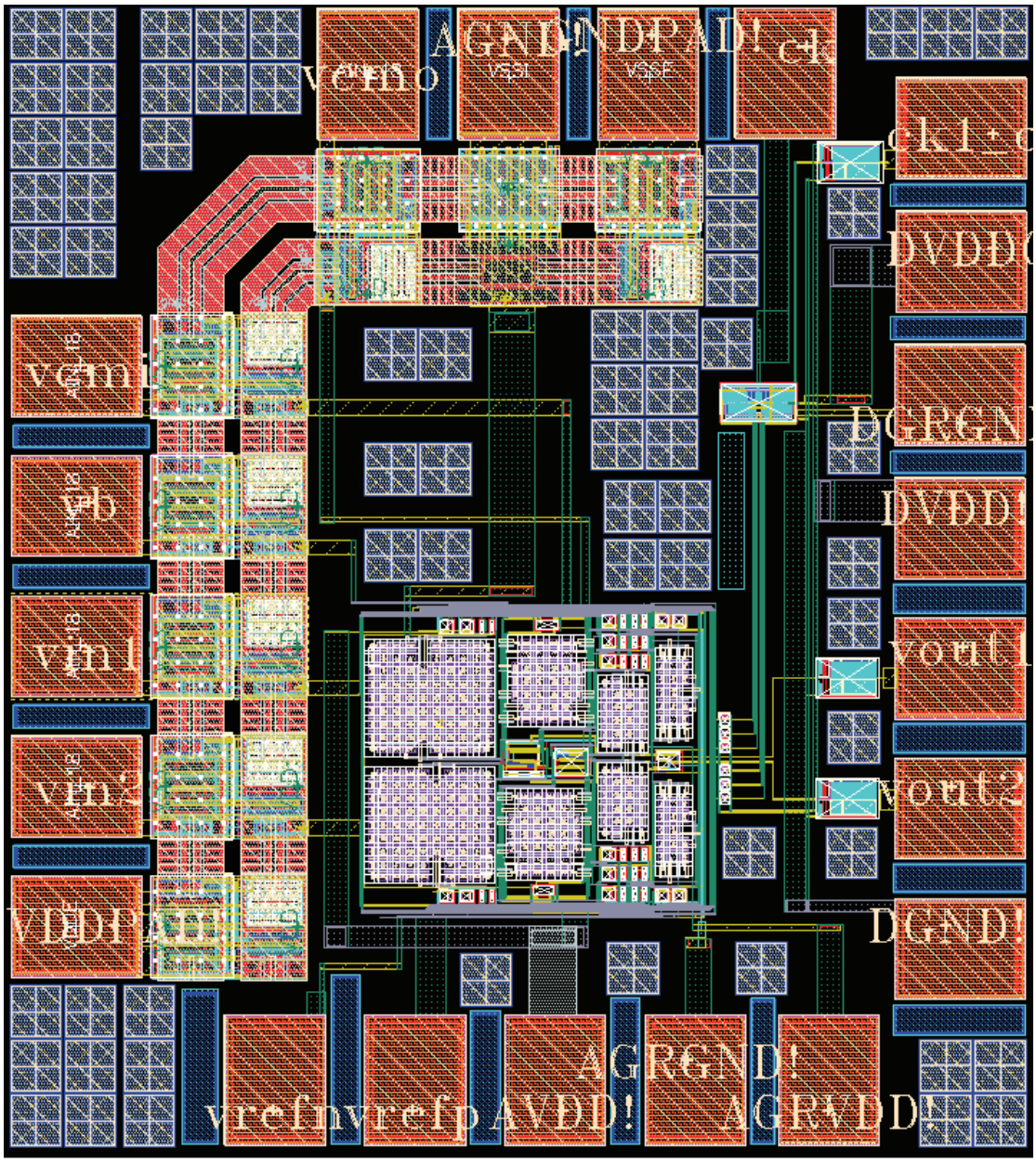

Figure 5.4 modified version of layout

We also take the measurement of the core power into considerations of the modified version of layout, we use three independent supply voltage pads for analog circuits (part A), clock generator circuit (part B) and output buffer (part C), respectively. The

simulation results of the power consumption for three parts are listed at Table 5.3, and the post layout simulation results are shown at Figure 5.5. The simulated result of SNR and SNDR are listed at Table 5.4.

	A	A+B	A+B+C
Power(uW)	14.3	18.0	25.4

Table 5.3 Power consumption for three parts circuits

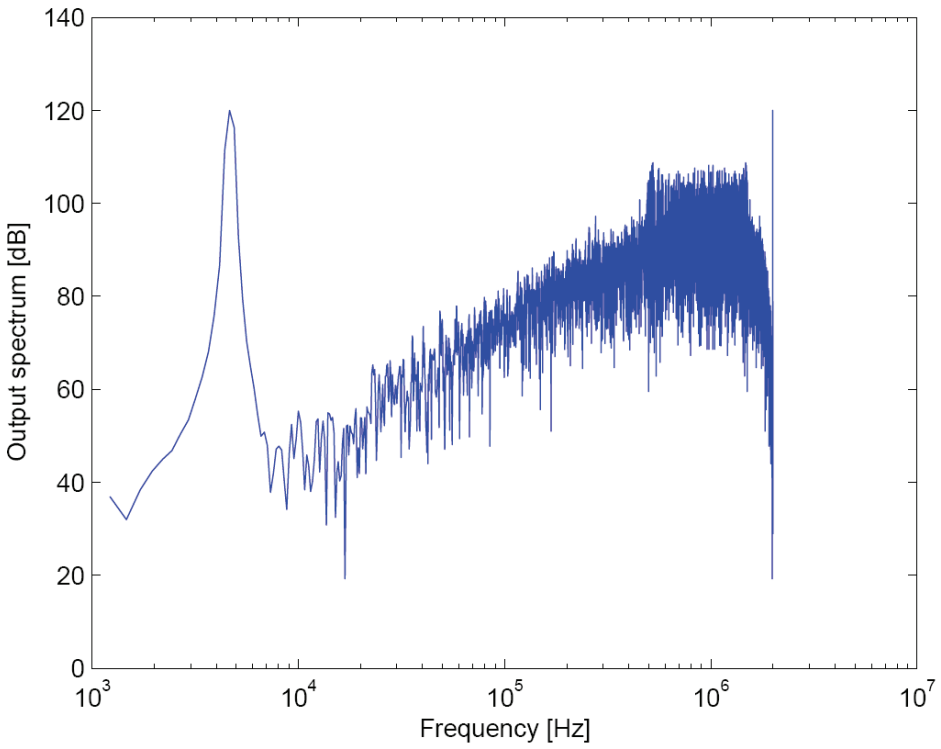

Figure 5.5 8192-point FFT of the modified layout

Unit(dB)	Pre-Simulation	***Post-Simulation***	***Modified layout***
SNR	69.1	***63.4***	***61.3***
SNDR	68.4	***58.7***	***57.9***

Table 5.4 Comparison of this modified layout

5.3 Summary

The circuit present in this thesis is implemented by design considerations described in Chapter 3 and circuit design implementation in Chapter 4.This work emphasized the complete design flow for low-power design and the current optimization of the OTA by discussing the slewing-settling trade-off of it.

The predicted resolution of the SDM is 11.2 bits (68.4dB), and the post-simulation result is 9.6 bits (58.7dB). It can be used in the audio electrical portable devices applications.

Chapter 6
Conclusions

This thesis describes the design and implementation of a low-power second-order sigma-delta modulator (SDM) with CIFF structure for audio-band applications. A single stage class-A positive feedback OTA with current optimization has been presented to lower the power of SDM.

Using 0.18um CMOS technology, this modulator achieves SNR of 63.4dB with 16KHz bandwidth. With a moderate target signal-noise-ratio (SNR), it is suitable for battery-based operation system, such as mp3 players, biomedical electronic and digital hearing aid instrument applications. The simulation results show that the power consumption is 18uW. It is the lowest compared to references [2]-[9].

The future work is to integrate the modified version from the problems of proposed SDM. A low-power measurement consideration is included in the modified SDM design consideration.

After this modified layout, a high resolution sigma-delta modulator can be done using the same method of optimizing the power of the OTA.

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