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Novel coexisted sol-gel derived poly-Si-oxide-nitride-oxide-silicon type memory

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The authors use a very simple sol-gel spin coating method at 900 °C and 1 min rapid thermal annealing to fabricate three different poly-Si-oxide-nitride-oxide-silicon-type flash memories. The memory windows estimated from the curve of drain current versus applied gate voltage are 3, 3.3, and 4 V for (i) HfO_2 thin film, (ii) hafnium silicate nanocrystal, and (iii) coexisted hafnium silicate and zirconium silicate nanocrystal memory, respectively. Together with the measurement from gate disturbance and drain disturbance on these fabricated devices, the coexisted nanocrystal devices exhibit better reliability than both the thin film type memory and single nanocrystal type memory. [DOI: 10.1116/1.2794327]

I. INTRODUCTION

Conventional flash memory devices use a floating gate structure and charge is stored in a polysilicon floating gate.[1] However, when the tunneling oxide is below 85 nm, a floating gate structure faces scaling issues.[2] The stored charge can leak due to defects in the tunneling oxide formed by repeated program/erase cycles. Therefore, discrete trap memory devices such as thin film poly-Si-oxide-nitride-oxide-silicon (SONOS) or nanocrystal-based memories are widely studied to replace the floating gate structure for semiconductor memory applications.[3–7] The charge trapping layer of traditional SONOS memory is silicon nitride (Si_3N_4). High-*K* materials such as HfO_2 or ZrO_2 thin films are considered as charge storage material to achieve the faster programing speed and better charge retention performance. SONOS high-*K* memory encounters the electron migration problem in the charge trapping layer,[5] and this effect will cause the charge loss and degrade the charge retention performance during memory operation. The nanocrystal memory can keep the trapped charge tightly to avoid the charge loss problem of SONOS memory and also achieve the advantages such as fast program/erase speed, low programing voltage, and good endurance.[8,9] Hence, the device reliability would be significantly enhanced.

Numerous technologies have been developed recently for the preparation of various high-*K* films. To prepare insulating thin films, atomic layer deposition (ALD), physical vapor deposition (PVD), and chemical vapor deposition (CVD) methods have all been used to prepare films for new technologies.[10–12] The sol-gel method is a very interesting simple preparing technique for ceramic films.[13] The sol-gel method can provide colloidal solvents or precursor compounds when metal halides are hydrolyzed under controlled conditions. In the sol-gel process, hydrolysis, condensation, and polymerization steps occur to form metal oxide networks. These reactions play significant roles in modifying the final material's properties. The most interesting feature of sol-gel processing is its ability to synthesize various types of materials that are known as "inorganic-organic hybrids." The film preparation with spin coating is a more simple method than ALD, PVD, or CVD due to its simpler operation, cheaper precursor, and lower tool price. In addition, the film can be fabricated in an atmospheric pressure system instead of a complex high vacuum system.

Regarding device reliability, there also arises a challenge as the flash memory is repeatedly programed and erased. The memory will be degraded as if the device suffers from the formation of a new defect during the applied voltage. In addition, the developed flash memory is designed as an array for regular operation. The continuous stressing on the device of interest may influence the performance of surrounding devices. Therefore, the flash memory also needs to check the gate disturbance and drain disturbance to ensure the fabrication reliability.[14]

In this article, we develop the sol-gel spin coating method and annealing technique to fabricate three SONOS-type flash memories: (i) 10 nm HfO_2 thin film, (ii) $HfSi_xO_y$ nanocrystal, and (iii) coexisted $HfSi_xO_y$ and $ZrSi_xO_y$. The performance of the drain current versus applied gate voltage, gate disturbance, and drain disturbance is conducted to evaluate the device reliability.

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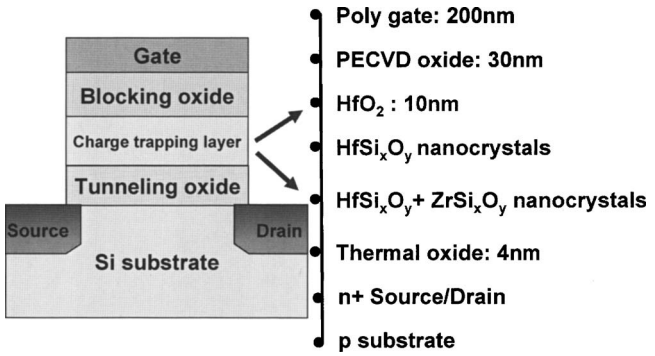

FIG. 1. Schematic diagram of the SONOS-type memory device structure with spin-coated sol-gel charge trapping layers.

II. EXPERIMENT

We separately prepared $HfCl_4$ (99.5%, Aldrich, St. Louis, MO), $ZrCl_4$ (99.5%, Aldrich, St. Louis, MO), and $SiCl_4$ (99.5%, Aldrich, St. Louis, MO) as precursors and dissolved into isopropanol (IPA, Fluka, water content $<0.1\%$) solvent to fabricate three sol-gel solutions for high-K films and nanocrystals. The first device with 10 nm HfO_2 thin film used the $HfCl_4$ sol-gel solution.[15] The second device used the coexisted $HfCl_4$ and $SiCl_4$ sol-gel solutions to prepare the initial thin film.[16] The film will be transferred into 5 nm $HfSi_xO_y$ nanocrystals in the subsequent annealing step. The third device was prepared by mixing the three sol-gel solutions of $HfCl_4$, $ZrCl_4$, and $SiCl_4$ to the initial thin film, and then transferred into coexisted 5 nm nanocrystals by the subsequent annealing.[17]

The structure of the fabricated devices is shown in Fig. 1. The fabrication of sol-gel spin coating nanocrystal memory is started with local oxidation of Si process on p-type (100) 150 mm silicon substrate. At the beginning, a 4 nm tunneling oxide was thermally grown at 925 °C in a furnace. The thin film was deposited by spin coating at 3000 rpm for 60 s at ambient temperature (25 °C). The spin coater used was TEL Clean Track model-MK8 (Japan). After spin coating, the wafer was rapid thermal annealed (RTA) at 900 °C for 60 s in O_2 ambient to form the memories with (i) HfO_2 layer, (ii) $HfSi_xO_y$ nanocrystal, and (iii) coexisted $HfSi_xO_y$ and $ZrSi_xO_y$ nanocrystals, respectively. The 30-nm-thick blocking oxide was deposited by low pressure chemical vapor deposition (LPCVD) tetra-ethyl-ortho-silicate (TEOS) followed by 200 nm poly-Si gate deposition. After the LPCVD TEOS deposition, the TEOS oxide is densified in N_2 ambient at 900 °C for 30 s. Finally, gate pattering, source/drain implant, and the rest of the subsequent complementary metal oxide semiconductor processes were used to fabricate this SONOS-type memory.

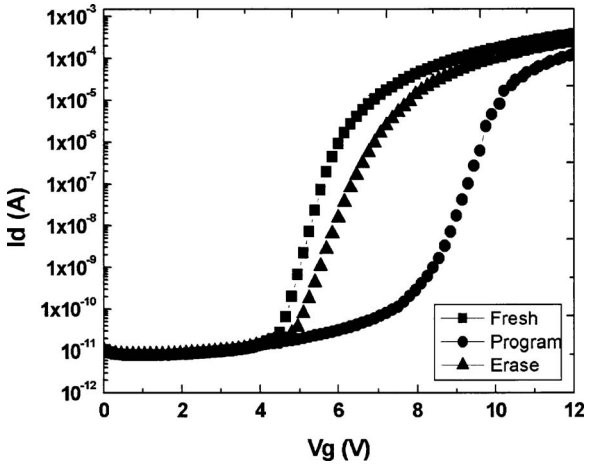

FIG. 3. I_d-V_g curve of SONOS-type memory from $HfSi_xO_y$ array nanocrystals fabrication.

III. RESULTS AND DISCUSSION

The drain current with respect to the applied gate voltage for the fabricated devices is demonstrated in Figs. 2–4. The HfO_2 thin film SONOS-type memory in Fig. 2 is measured by channel hot electron injection for programming and band to band tunneling induced hot hole injection for erasing. The

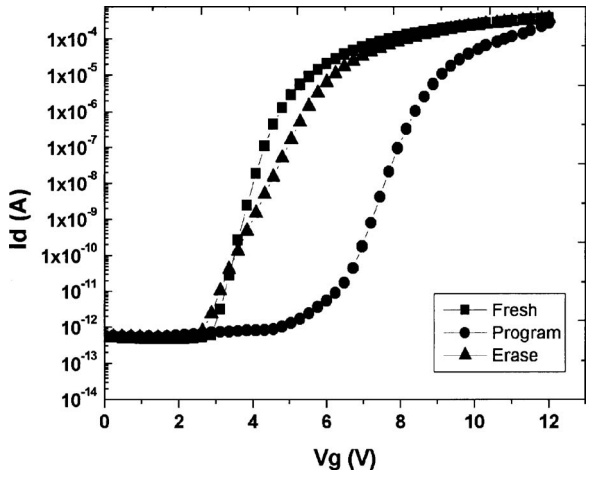

FIG. 2. I_d-V_g curve of SONOS-type memory from 10 nm HfO_2 thin film fabrication.

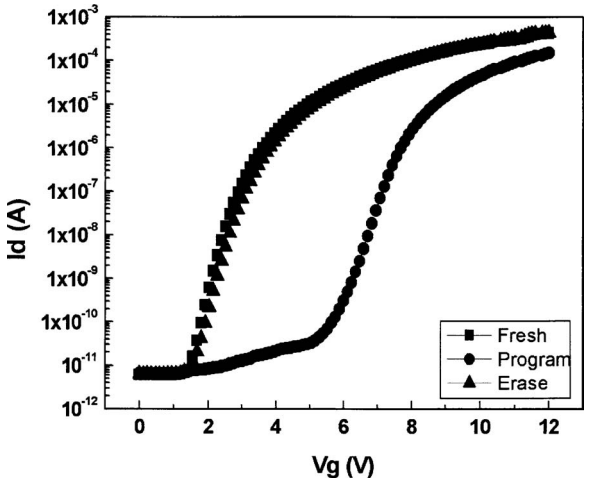

FIG. 4. I_d-V_g curve of SONOS-type memory from the coexisted $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals fabrication.

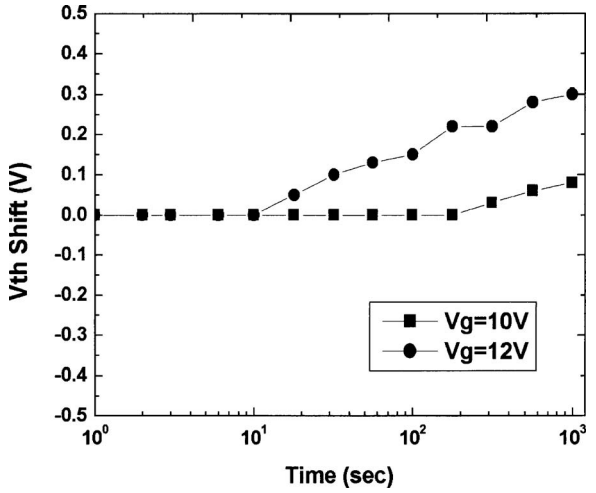

FIG. 5. Gate disturbance of memory fabricated by 10 nm HfO_2 thin film.

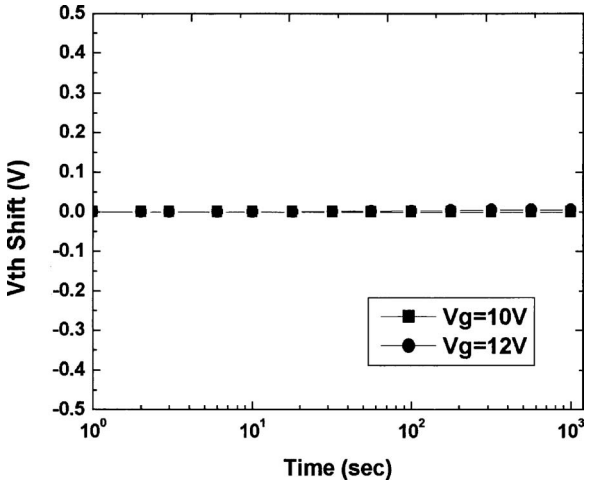

FIG. 6. Gate disturbance of memory fabricated by $HfSi_xO_y$ array nanocrystals.

programming condition is operated at V_g (gate voltage) $=15$ V and V_d (drain voltage) $=10$ V for 10 ms, while the erasing condition is operated at $V_g=-10$ V and $V_d=10$ V for 1 s. The memory window of this device is about 3 V at the drain current of 10^{-8} A. In the $HfSi_xO_y$ nanocrystal memory, the memory window from drain current versus gate voltage in Fig. 3 is estimated to 3.3 V at the drain current of 10^{-8} A. This observation suggests that the nanocrystal type memory operates better than the thin film SONOS-type memory. The nanocrystal memory can trap more charge carriers, and therefore exhibits the better memory window. This increased performance can promote the reliability of the memory.

Instead of the single type of nanocrystals in Fig. 3, the memory in Fig. 4 is fabricated with two types of nanocrystals (i.e., $HfSi_xO_y$ and $ZrSi_xO_y$). The memory window is about 4 V at the drain current of 10^{-8} A. This SONOS-type memory with coexisted nanocrystals has the largest V_{th} shift compared to the memories with HfO_2 film or $HfSi_xO_y$ nanocrystal due to more nanocrystals in the charge trapping layer. The observation from Figs. 3 and 4 suggests that the formation of nanocrystals for the memory's charge program/erase is an effective way of improving the device reliability.

The gate disturbance for the fabricated three devices is illustrated in Figs. 5–7. We measure the erased state for these devices and apply the $V_g=10$ or 12 V with the drain, source, and substrate grounded. In Fig. 5, the threshold voltage shift (V_{th}) for $V_g=10$ V remains constant for 1–200 s, and gradually increases for 200–1000 s. Interestingly, the device V_{th} shift for $V_g=12$ V is observed at 10 s and V_{th} shift $=0.3$ V at 1000 s. The HfO_2 thin film device is easily degraded during gate biasing. In the regular memory operation, the unstable V_{th} shift will induce the loss of data storage. On the contrary, the SONOS-type memories fabricated by nanocrystal processing have very stable V_{th} shift for gate stressing at 10 or 12 V in Figs. 6 and 7. This is because the nanocrystal is surrounded by SiO_2, and this increases the equivalent tunneling oxide thickness. When the tunneling oxide thickness is increased, the electrons in the substrate are less able to tunnel to the nanocrystal by Fowler-Nordheim tunneling operation.

The drain disturbance measurement for these devices is depicted in Figs. 8–10. We measured the erased state for these devices, and applied the $V_g=6$ V at various drain voltages of 3, 4, and 5 V, respectively. In Fig. 8 for the HfO_2 thin film memory, the curve for $V_d=3$ V remains constant at 1 to 1000 s. The increase of V_{th} shift is observed at 60 and 100 s for the drain voltages of 5 and 4 V, respectively. In Fig. 9 for the $HfSi_xO_y$ nanocrystal memory, the curves for drain voltages of 3 and 4 V also remain constant from 1 to 1000 s. The increase of V_{th} shift is only observed for 200 s for the drain voltages of 5 V.

The coexisted nanocrystals in Fig. 10 indicates that the V_{th} for all three drain stressing voltages is very stable. Hence, the coexisted hafnium silicate and zirconium silicate nanocrystal memory devices have better electrical performance than the HfO_2 thin film type or $HfSi_xO_y$ nanocrystal type. This phenomenon is also attributed to the surrounding effect of SiO_2 mentioned above. The equivalent tunneling oxide thickness is increased after nanocrystal formation. When the tunneling

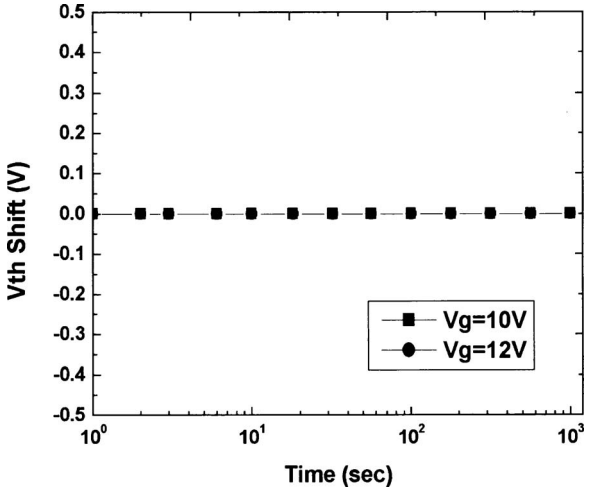

FIG. 7. Gate disturbance of memory fabricated by coexisted $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals.

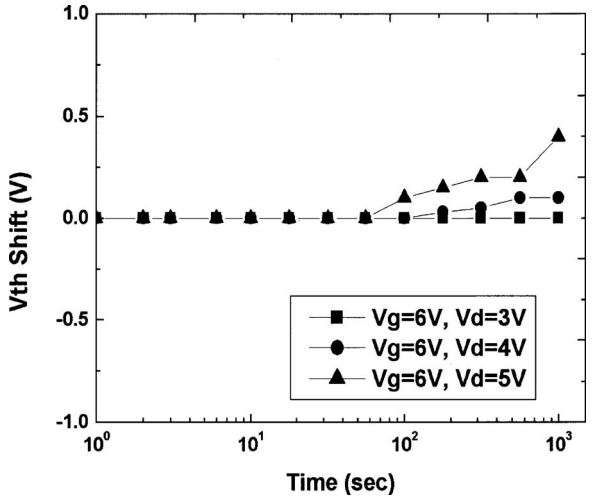

FIG. 8. Drain disturbance of memory fabricated by 10 nm HfO_2 thin film.

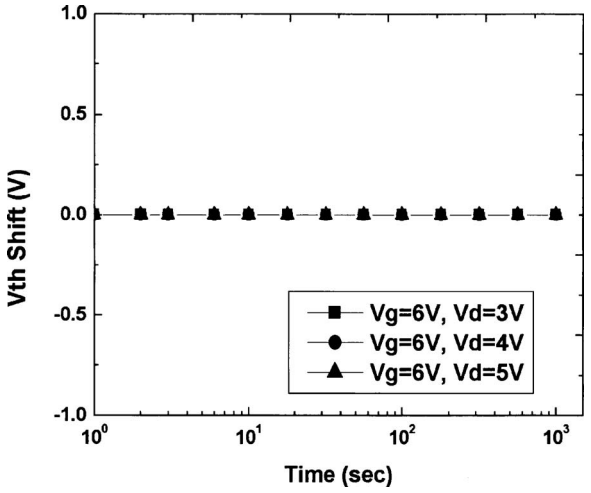

FIG. 10. Drain disturbance of memory fabricated by coexisted $HfSi_xO_y$ and $ZrSi_xO_y$ array nanocrystals.

oxide thickness is increased, the electrons in the substrate are less able to tunnel to and to be trapped in the nanocrystal. This observation also suggests that the formation of nanocrystals is an effective way of enhancing the device reliability. The coexisted hafnium silicate and zirconium silicate nanocrystal memory devices with higher density of nanocrystals demonstrate the best reliability.

IV. CONCLUSIONS

In this article, we use a sol-gel spin coating method to fabricate three types of flash memories from (i) HfO_2 thin film, (ii) hafnium silicate nanocrystal, and (iii) coexisted hafnium silicate and zirconium silicate nanocrystal memory. We have verified the device performance with drain current versus applied gate voltage, gate disturbance, and drain disturbance measurements. The quality of the coexisted hafnium silicate and zirconium silicate nanocrystals formed by the sol-gel spin coating method and RTA treatment exhibits better reliability in terms of broad memory window due to more trapping sites. In addition, the memory fabricated by the coexisted hafnium silicate and zirconium silicate nanocrystals has better gate and drain disturbance due to the contribution of surrounding SiO_2 to increase the equivalent tunneling oxide thickness.

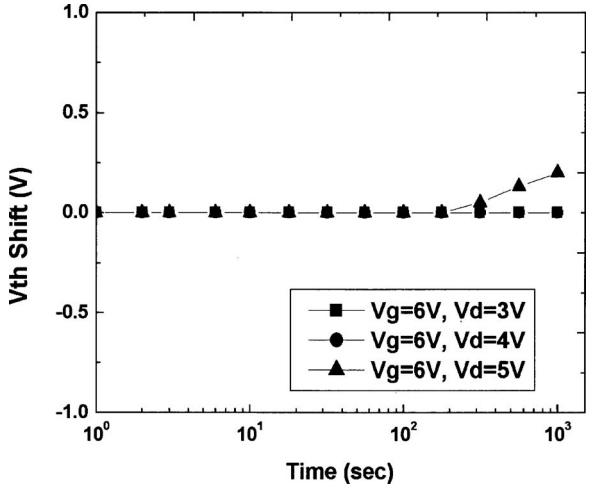

FIG. 9. Drain disturbance of memory fabricated by $HfSi_xO_y$ array nanocrystals.

ACKNOWLEDGMENTS

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