國立交通大學

顯示科技研究所

碩 士 論 文

低溫複晶矽薄膜電晶體的電容特性及模擬

Analysis and Simulation of Capacitance Characteristic in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

研 究 生：蘇旻君

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中華民國 九十七年八月

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摘要

近年來，低溫複晶矽薄膜電晶體已引起大量的研究，其應用相當廣泛。低溫複晶矽薄膜電晶體在面板技術的應用上，由於具有高遷移率，而有機會整合面板周邊電路，實現系統面板的目標。當低溫複晶矽薄膜電晶體應用為驅動電路時，交流信號將操作於閘極。因此低溫複晶矽薄膜電晶體對於元件在交流信號下的頻率響應就具有相當大的重要性。

在本篇論文中，使用準分子雷射製作低溫複晶矽薄膜電晶體，利用阻抗分析儀，量測電容－電壓和電容－頻率來研究準分子雷射製作的複晶矽薄膜電晶體。調變在不同準分子雷射能量密度下的複晶矽薄膜品質，觀察電容在不同的閘極偏壓下對頻率的變化。改變元件尺寸大小及製程步驟，來觀察元件特性的變化。由於複晶矽薄膜的品質不同，在複晶矽結晶顆粒較小的時候，可以利用先前研究的模型或是 RPI 模型，考慮膜內單一能階的缺陷，來解釋元件的電容特性。當複晶

矽的結晶顆粒逐漸增大，先前研究的模型或是 RPI 模型已經不能解釋 C-f 曲線呈現斜直線的現象，單一能階的缺陷已經不能解釋，應由連續能階的缺陷去解釋。利用 Seto 模型的觀念，考慮晶粒邊界的能障對載子的影響，成功地建立一個模擬來解釋 C-f 曲線關係。

Analysis and Simulation of Capacitance Characteristic in Low-Temperature Polycrystalline Silicon Thin-Film Transistors

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Abstract

In recent years, low temperature polycrystalline silicon thin-film transistors (poly-Si TFTs) have been investigated extensively for their wide applications. Poly-Si TFTs have been studied extensively for their application on system-on-panel (SOP) technology due to the high mobility. The low temperature poly-Si TFTs are operated under gate alternating current signal. Therefore, the studies of frequency response of low temperature poly-Si TFTs under gate alternating signal become very important.

In this thesis, the low temperature polycrystalline silicon TFTs fabricated by the excimer laser annealing (ELA). To research the characteristics of ELA poly-Si TFTs is analyzing the capacitance-voltage (C-V) and capacitance-frequency (C-f) by using impedance analyzer. Here, by adjusting different poly silicon crystalline film qualities due to different excimer laser energy densities, the variation of the measured capacitance under different gate biases is observed. We change the dimension of poly-Si TFTs and the fabrication process to observe the characteristic of devices. As

poly-Si grain is small, the capacitance characteristics of the poly-Si TFTs can be described by RPI model or the pre-studies which considering the mono-energetic (single energy level) of the trap. As the grain size becomes larger, RPI model or the pre-studies can not be applied to the case which C-f curve is sideling straight. The mono-energetic response is not able to fit experiment result, and we need to specify a continuous-distributed response time of the trap. Using the Seto's model, we consider the energy barrier of the grain boundary, and the influence of the carriers. We make a new simulation to express the C-f curve successfully.

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僅以這篇論文，獻給我的老師、好友與家人。

旻君

2008 夏 于新竹

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Chapter 1

Introduction

1-1 Introduction of polycrystalline silicon thin-film transistors

Polycrystalline silicon thin film transistors (poly-Si TFTs) have attracted more attention because of their widely applications on active matrix liquid crystal displays (AMLCDs) [1.1]-[1.4], organic light-emitting displays (OLEDs), three-dimensional (3D) integrated circuits [1.5]-[1.7] and memory devices such as dynamic random access memories (DRAM's) [1.8], static random access memories (SRAM's) [1.9], electrical programming read only memories (EPROM's) [1.10], electrical erasable programming read only memories (EEPROM's) [1.11], and charge coupled device (CCD). Undoubtedly, poly-Si TFT technology is the most promising approach.

Unlike amorphous silicon (a-Si) TFT's or organic TFTs, poly-Si TFT's have much higher carrier mobility which usually exceeds 100 $cm^2/V\text{-}sec$ by present mature technology. The superior carrier mobility is essential to integrate Poly-Si TFT's successfully and peripheral driving circuits [1.9] on the same panel to reduce the assembly complexity and cost. Furthermore, because of the higher mobility, the dimension of the poly-Si TFTs can be designed smaller to get larger aperture ratio in each pixel and higher turn-on current, which allows a higher panel resolution.

However, there are still some problems existed in Poly-Si TFT's. There are a lot of defects at the disordered grain boundaries of poly-Si films which degrade device performance severely. The performance of poly-Si TFTs is strongly influenced by grain boundary in the channel region. In order to make high performance poly-Si TFTs, low-temperature technology is required for the commercial flat-panel displays (FPD) on inexpensive glass substrate, whereas the maximum processing temperature needs to be kept below than 600 $^{\circ}C$ [1.12]. There are several techniques have been proposed and developed [1.12]-[1.14] to manufacture the LTPs film on glass or plastic substrate: solid phase crystallization (SPC), sequential lateral solidification (SLS), excimer laser crystallization (ELC), and metal-induced lateral crystallization (MILC). Because of the recrystallization, process will influence the quality of Poly-Si films and it will influence the device performance of Poly-Si TFT's spontaneously. Thus, the roughness and uniformity of poly-Si film are important issues that may degrade the electrical characteristics if the laser energy is not accurately controlled.

In conclusion, the main limitation of poly-Si TFTs is their instability for various kinds of applications, associated with the trap states. To overcome this inherent disadvantage of poly-Si films, many researches have been focused on modifying or eliminating these grain boundary traps. Hydrogenation is a method for reducing the trap density in poly-Si film [1.15]-[1.17]. As the number of trapped carriers decreases,

the potential barrier associated with the grain boundary also decreases and enhances the characteristics of poly-Si TFTs.

1-2 Introduction of Seto's model

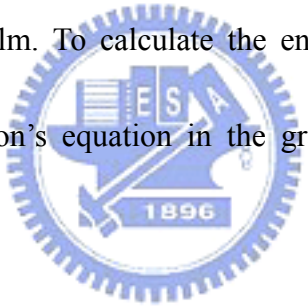
As previously mentioned, the poly-Si material contains some grain boundaries. The device characteristics of poly-Si TFTs are strongly influenced by the grain structure in poly-Si film. J.Y Seto proposed a new model for the electrical properties and the carrier transport in poly-Si TFTs [1.18]. The Seto's model is based on the following assumptions:

- Poly-Si film has small grain size,
- The single crystalline silicon energy band structure is assumed to be applicable inside the crystallites,
- Doping concentration in poly-Si is uniform,
- All the doping atoms are ionized,
- All the grains have the same size,
- The representation is mono-dimensional,
- The grain boundaries have no thickness,
- The defects are carrier traps that are located in grain boundaries.

  The trap concentration is defined per surface unit. The trap is assumed to be initially neutral and become charged by trapping carriers,

- The traps are acceptors in the n-type and donors in the p-type semiconductor.
- The trap energy level is unique and located more or less in the middle of the forbidden band.

In this model, it is assumed that the poly-Si material is composed of a linear chain of identical crystallite having a grain size L_G and the grain boundary trap density N_T, as Fig. The charge trapped at grain boundaries is compensated by oppositely charged depletion regions surrounding the grain boundaries. This model is based on the calculation of energy barrier at grain boundaries, which affects the transport f electrons in the film. To calculate the energy barrier, the simplest way consists of solving the Poisson's equation in the grain. We consider the different following parameters:



- X, extension of the space charge region,
- N_D, donor doping atom concentration,
- N_{TA}, acceptor like trap surface density at grain boundaries,
- ε_0, permittivity in vacuum,
- ε_s, semiconductor permittivity,
- L_G, size of the grain,
- V, the electrostatic potential,
- x, the position coordinate,

The distribution of the charges in the material is schematically described in Fig.1-2-1.

In the space charge region, $0<x<\frac{X}{2}$, $\frac{d^2V}{dx^2}=-\frac{qN_D}{\varepsilon_s\varepsilon_0}$ (1)

Out of the space charge region, $\frac{X}{2}<x<\frac{L_G}{2}$, $\frac{d^2V}{dx^2}=0$ (2)

At the border of the space charge region, the electric field is null: $[\frac{dV}{dx}]_{\frac{X}{2}}=0$

$0<x<\frac{X}{2}$: $\frac{dV}{dx}=-\frac{qN_D}{\varepsilon_s\varepsilon_0}x+const.=\frac{qN_D}{\varepsilon_s\varepsilon_0}(\frac{X}{2}-x)$, $V(x)=-\frac{qN_D}{2\varepsilon_s\varepsilon_0}(\frac{X}{2}-x)^2+V(\frac{X}{2})$

$\frac{X}{2}<x<\frac{L_G}{2}$: $V(x)=V(\frac{X}{2})$

And the energy barrier height (E_B) is defined as the energy difference between the positions $x=0$ and $x=\frac{X}{2}$,

$V_B=-[V(0)-V(\frac{X}{2})]=\frac{qN_D}{2\varepsilon_s\varepsilon_0}(\frac{X}{2})^2=\frac{qN_D}{8\varepsilon_s\varepsilon_0}X^2$ (3)

The value of X has to verify for the electrical neutrality of the global material, which means $XqN_D^+=N_{TA}^-$, N_{TA}^- is the ionized part of N_{TA}. The Seto's model defines a critical concentration (N_D^*), which corresponds to this limit:

$\frac{X}{2}=\frac{L_G}{2}$ $\rightarrow$ $X=L_G$ $\rightarrow$ $N_D^*=\frac{N_{TA}}{L_G}$ (4)

For a fixed trap density, if the effective doping concentration is higher than the critical concentration, the space charge extension is lower than the crystallite site.

$N_D>N_D^*$: $X=\frac{N_{TA}}{L_G}$ and $V_B=\frac{q}{8\varepsilon_s\varepsilon_0}\frac{N_{TA}^2}{N_D}$ (5)

$N_D<N_D^*$: $X=L_G$ and $V_B=\frac{qN_D}{8\varepsilon_s\varepsilon_0}L_G^2$ (6)

In poly-Si TFTs, the carrier density n induced by the gate voltage can be expressed as

$$n = \frac{C_{ox}(V_G - V_{th})}{qt_{ch}} \tag{7}$$

where t_{ch} is the thickness of the inversion layer.

1-3 Introduction of the RPI C-V model of the poly-Si TFT

In RPI AC models, the grain boundary and intra-grain trap states in poly-Si result the gate to source/drain capacitance ($C_{G\text{-}SD}$) of a TFT in a function of measurement frequency. Here, the source and drain terminals of an n channel TFT have been shorted to ground, and a small signal is applied to the gate of the device. For a signal frequency of 10 *kHz*, $C_{G\text{-}SD}$ increases from approximately zero to the gate oxide capacitance (*Cox*) as V_{GS} is increased. The frequency dispersion phenomenon can be comprehended by considering the transmission line model that is illustrated in Fig.1-2-1. A typical analysis of the effective circuit model forms complex impedance between the gate and source/drain terminals which depends on different frequencies. For single crystalline silicon transistors, the impedances are very small due to high mobility. Therefore the capacitance is almost independent of frequency.

In the RPI models, the small signal equivalent circuit model is shown in Fig.1-2-4 [1.19], where the gate resistors, r_{sx} and r_{dx}, are in series with the capacitances and approximate the distributed nature of the structure. For zero drain and source bias, the device is symmetric, $r_{sx} = r_{dx}$ and $C_{sx} = C_{dx}$. Based on a circuit analysis of Fig.1-2-4 where $r_{sx} = r_{dx}$ and $C_{sx} = C_{dx}$, the effect gate to source/drain

capacitance, $C_{G\text{-}SD}$, is given as a function of frequency, ω, by

$$C_{G-SD} = \frac{2C_{sx}}{(\omega r_{sx} C_{sx})^2 + 1} . \quad (8)$$

At very low frequency, r_{sx} and r_{dx} have little effect, and $C_{G\text{-}SD}$ approaches the frequency independent value of $2C_{sx}$. Accordingly, for zero drain bias, $C_{sx} = C_{dx}$ is given by $C_{sx} = \frac{C_{G-SD}'}{2} = \frac{1}{2} \times \frac{C_{ox} LW}{1 + 2\exp[\frac{-(V_{GS} - V_{th})}{\eta_c V_T}]}$. (9)

η_c is the capacitance ideality factor, V_T is the thermal voltage and the other symbols have their usual meanings.

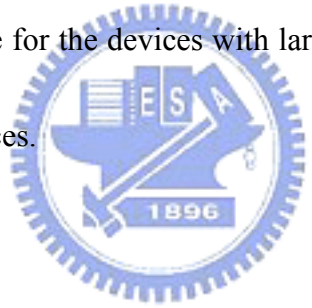
Besides, previous research also referred to later flow transmission line model [1.19][1.20], and introduced the influence of depletion capacitance (C_D). These statements indicated the variation of measured capacitances with different frequencies primarily arises from a frequency response associated with the later flow of carriers into and out of the channel from adjacent source and drain region.

However, the defects existed at the interface between gate oxide and poly-Si film, the grain boundary defects and the intra-grain defects are other factors to affect the device performance which are likely to respond to the small ac signal. Because of the response time of these defects, the measured capacitance is also a function of frequency in the depletion region. Therefore, the effect of trap capacitance (C_t) should be taken into account, where C_t is in parallel with C_D.

1-4 Motivation

The large area electronics or the flat-panel displays comprised of poly-Si TFTs are widely used all over the world. Most of the previous studies have focused on the analysis of the defect density within the energy band-gap, the dependence of mobility on different biases, film qualities, environment temperatures, and the extraction of effective parasitic resistance by drain current-voltage measurement.

In addition, in recent years, the fabrication technology of poly-Si TFTs have been improved a lot, and the poly-Si grain become larger. About the RPI model or the pre-studies are not appropriate for the devices with large grain, so we want to make a new simulation for these devices.



1-5 Thesis outline

This thesis is organized into the following manner.

In Chapter 1, the various kinds of applications, the advantages and the disadvantages of poly-Si TFTs, and several popular laser crystallization technologies are introduced in a brief overview of the poly-Si TFT technology. Then, Seto's model, RPI model of poly-Si TFTs and the other background studies are discussed briefly. Finally, the motivation of this work to study the capacitance modeling of poly-Si TFTs is expressed.

In Chapter 2, detailed fabrication processes of ELA poly-Si TFTs, and the instruments which we use to measure are introduced, respectively. The measuring conditions are described concisely.

In Chapter 3, the discussion is divided into two parts: First, the phenomena of the C-V curves are analyzed. Second, the phenomena of the C-f curves are analyzed.

In Chapter 4, the conclusion is given the analysis result of poly-Si TFTs.

Figure

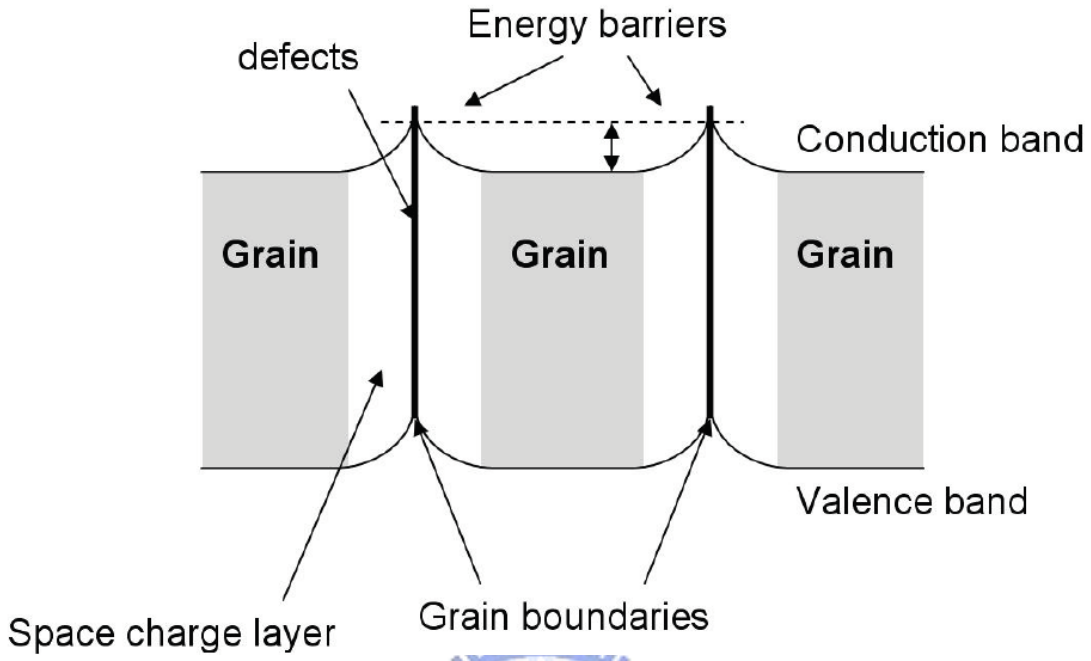


Fig.1-2-1 One-dimensional energy band diagram in polycrystalline material. The grain size is assumed to be constant. At grain boundaries, defects are electrically active.

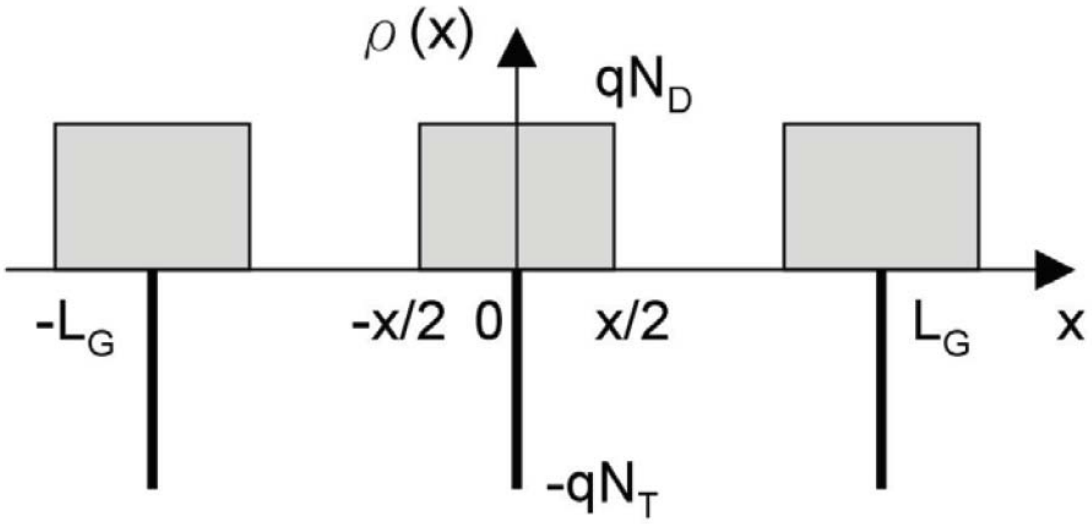


Fig.1-2-2 Simplified distribution of charges within the grain and at grain boundaries. At grain boundaries, the trap state density is defined per surface unit, while N_D is a doping volume concentration.

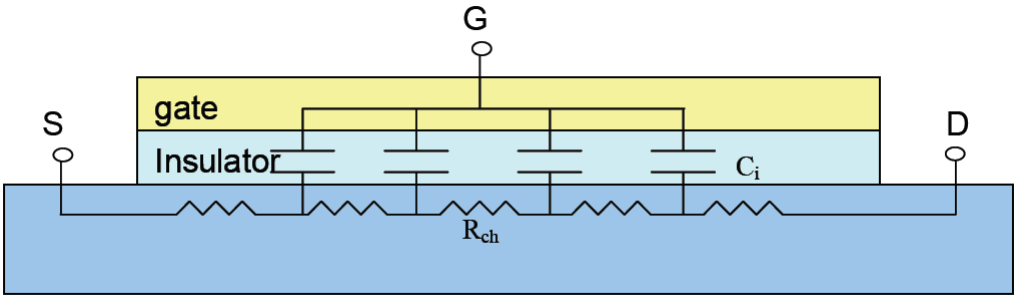


Fig.1-2-3 Transmission line model proposed by RPI.

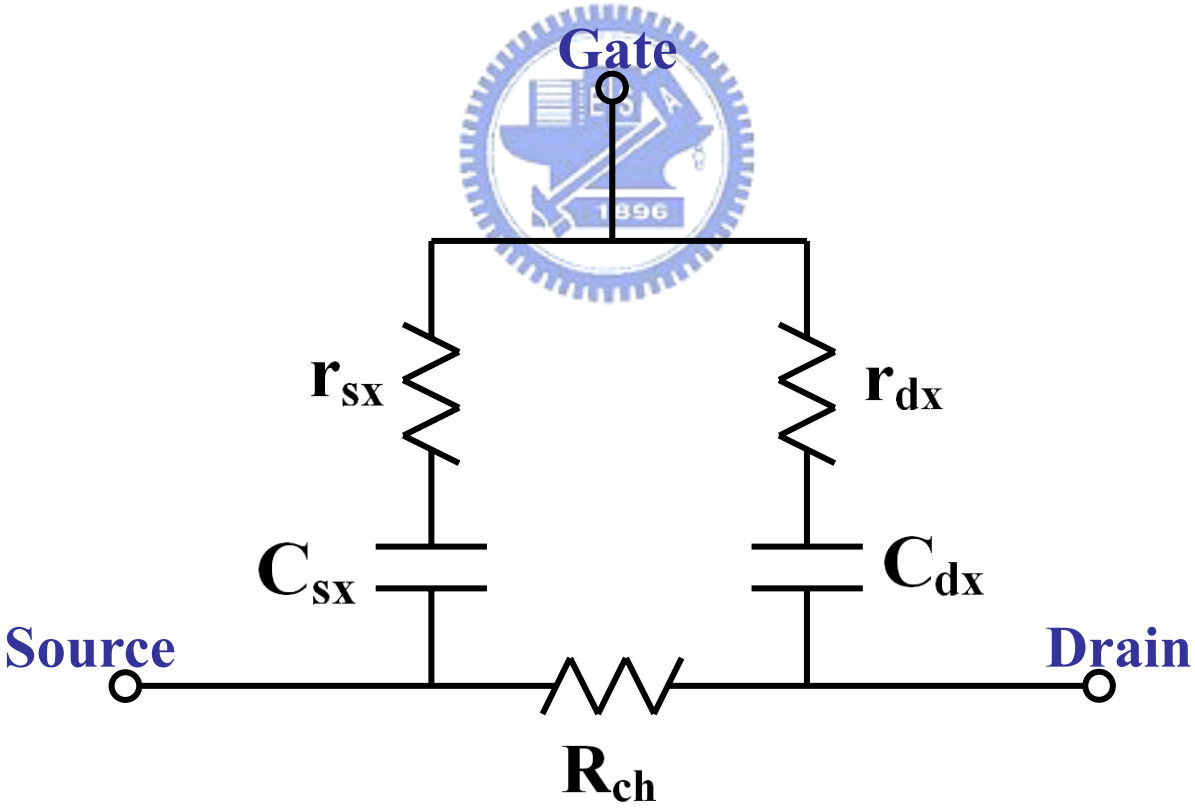


Fig.1-2-4 Equivalent circuit model for SPICE transient and small signal simulations

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Chapter 2

Experimental Procedures

2-1 Fabrication processes of LTPS poly-Si TFT

In this experiment, the typical top-gate, coplanar self-aligned poly-Si TFTs were fabricated on the glass substrates and crystallized by ELA recrystallization technology. The schematic cross sectional view of p-type ELA poly-Si TFT without lightly doped drain (LDD) structure are shown in Fig.2-1-1 and that of n-type ELA poly-Si TFT with LDD structure are shown in Fig.2-1-2. The device fabrication process is described below and shown in Fig.2-1-3.

First, the oxide buffer layer was deposited on the glass substrate to prevent the diffusion of the impurities existing in the glass substrate from the silicon layer. Then, the undoped 50-*nm*-thick amorphous-Si layer was deposited on the buffer layer. After that, amorphous-Si layer was recrystallized by ELA method with several different laser energies; here, the laser energy densities were 340 mJ/cm^2, 360 mJ/cm^2, and 380 mJ/cm^2, respectively. The recrystallized poly-Si layer was patterned into the active island with different dimensions. Afterward, the gate insulator layer was deposited. The gate insulator layer was combined with a 50-*nm*-thick oxide layer deposited on the poly-Si layer and a 20-*nm*-thick nitride layer deposited on the oxide layer. Next,

phosphorus ions were implanted to form the n^+ source/drain and n^- LDD regions; boron ions were implanted to form p^+ source/drain regions. These dopants were activated by thermal process. Finally, the metal layer was deposited and then patterned for the source/drain and gate regions as the metal pads.

The electrical characteristics of the 6, 600 μm channel width and 4, 6, 8, 10, 12, 15, 30, 600 μm channel length n-type poly-Si TFTs with different LDD lengths which varies from 0.75 to 1.25 μm were measured under various temperatures which varies from 90 K to 330 K to check the influence of the capacitance of poly-Si TFTs.

2-2 Instrument and measurement setup

2-2-1 Instrument

For I-V measurement:

- Microscope, Hot chuck, Probe station
- Semiconductor Parameter Analyzer (Agilent HP4156C) :

  Be used to measure the characteristic curve of Current-Voltage (I-V)
- Impedance Analyzer (Agilent HP4284A) :

  Be used to measure the characteristic curve of Capacitance-Voltage (C-V)
- Low-leakage Switch Mainframe (Agilent E5250)
- Software of measurement : ICS (Interactive Characterization Software)

For C-V and C-f measurement:

- Impedance / Gain Phase Analyzer (Agilent HP4194A)：

  Be used to measure the characteristic curve of Capacitance-Voltage (C-V), Capacitance-frequency (C-f, also called Admittance Spectroscopy), Transient Capacitance and Deep Level Transient Spectroscopy.

- Variable Temperature System：

  This system is the form of open cycle, decreasing temperature by using liquid nitrogen which can achieve to 80 K for the minimum value. The other way for decreasing temperature is to use liquid helium which can achieve to 20 K. The system including Cryogenic, auto-tuning temperature controller, vacuum pump motor, the cylinder of liquid nitrogen and vacuum chamber.

- Vacuum Chamber :

  There are one heater platform and three probe platforms in the vacuum chamber. This vacuum chamber was produced by CRYO, type CMP-1487.

All the measurement data of the research are done by using GPIB interface control card to control instruments and loading data, then using math software to analysis data and draw curves.

2-2-2 Set up instrument for the C-V and C-f measurement

In this experiment, the current-gate voltage (I_D-V_G) characteristic measurements of the devices were performed by HP4156. Besides, the capacitance-gate voltage (C-V) characteristic measurements of the devices were performed by HP4284 under different frequencies which range from 10 *kHz* to 1 *MHz*. In addition, to measure capacitance-frequency (C-f) is also used by HP4194 in different gate voltages that were biased at the depletion region, and the measured frequencies were from 10 *kHz* to 1 *MHz*.

Fig, shows three different connections for C-V characteristics measured [1], and Fig. shows the measured result. $C_{G\text{-}S,DF}$ is the gate-to-source capacitance with the drain electrode floating, and $C_{G\text{-}D,SF}$ is the gate-to-drain capacitance with the source electrode floating. $C_{G\text{-}SD}$ is the capacitance between the gate and the sour-drain connected together. In this experiment, we discussed the varied of $C_{G\text{-}SD}$.

Figure

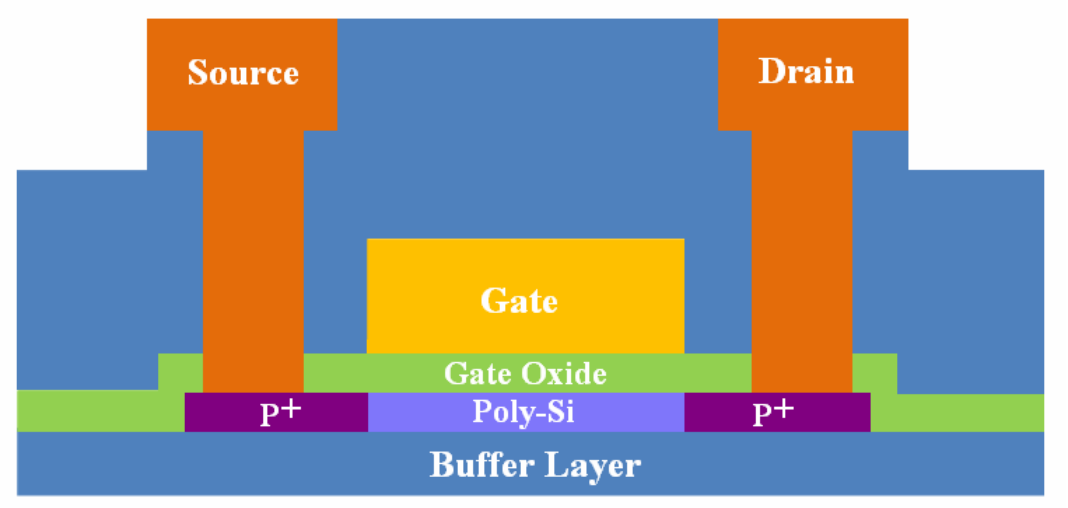


Fig.2-1-1 The schematic cross sectional view of p-type ELA poly-Si TFT without LDD structure.

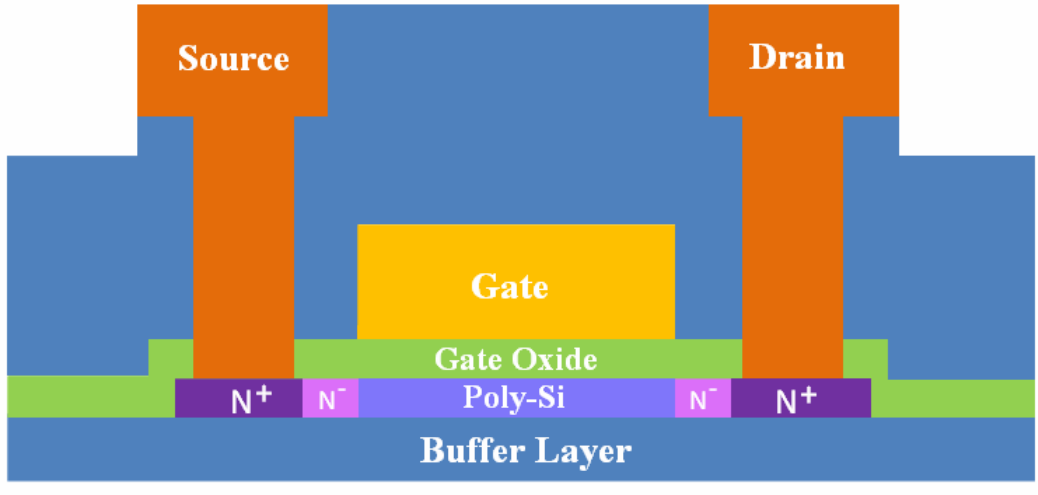


Fig.2-1-2 The schematic cross sectional view of n-type ELA poly-Si TFT with LDD structure.

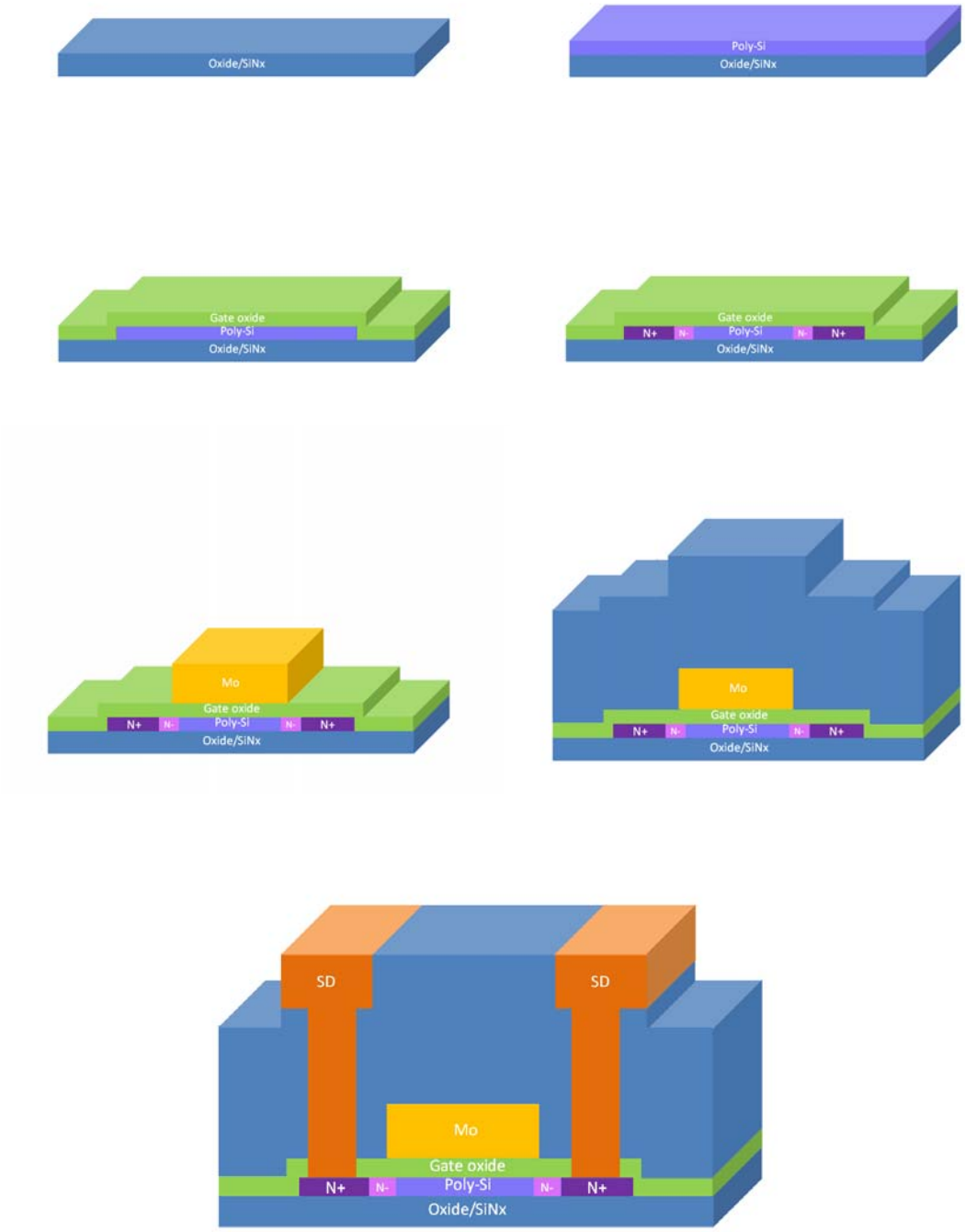


Fig.2-1-3 The device fabrication process of n-type TFT with LDD structure.

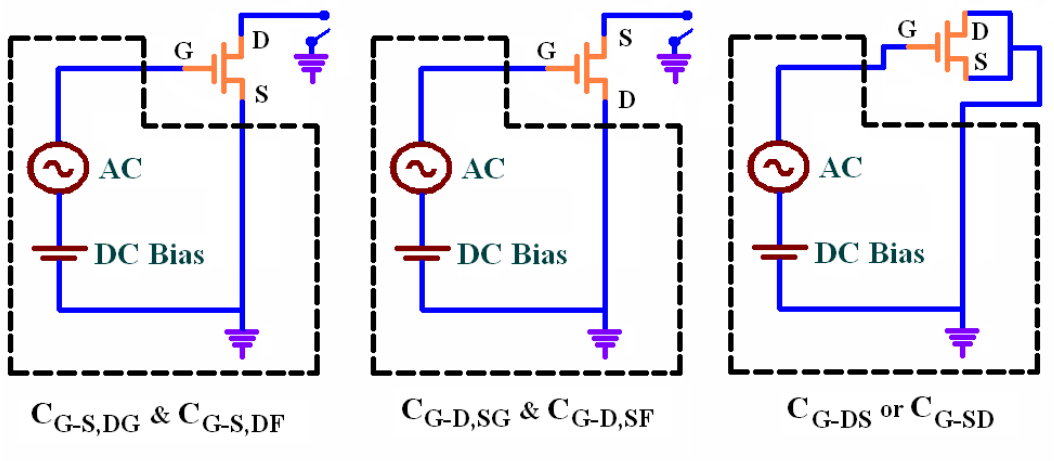


Fig.2-2-1 Circuit diagrams of C-V measurement. In $C_{G-S,DG}$ measurement, drain was connected to the ground terminal of the measuring instrument, but in $C_{G-S,DF}$ measurement, the drain electrode was floated. Similarly, $C_{G-D,SG}$ and $C_{G-D,SF}$. C_{G-DS} or C_{G-SD} is the capacitance between the gate and the source-drain connected together.

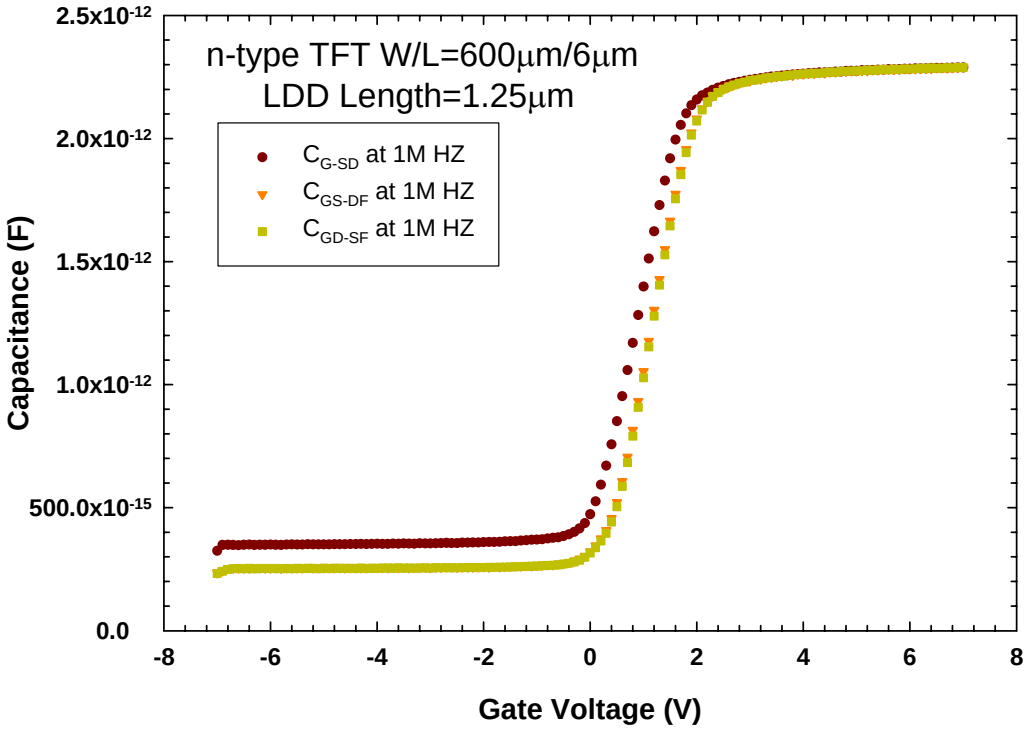


Fig.2-2-2 C_{G-SD}, C_{GS-DF} and C_{GD-SF} versus V_G characteristic of poly-Si TFTs with W/L=600*μm*/6*μm*, and LDD length=1.25*μm* at 1 *MHz*.

Reference

[2.1] Hyuk-Ryeol Park, Daewon Kwon, and J. David Cohen, “Electrode Interdependence and Hole Capacitance in Capacitance-Voltage Characteristics of Hydrogenated Amorphous Silicon Thin-Film Transistor”, Journal of Applied Physics, Vol.83, No.12, pp.8051-8058, June 1998

Chapter 3. Results and Discussions

3-1 The analysis of the C-V curve

3-1-1 Poly-Si TFTs with various channel length and LDD length

To confer the relation between the size of device and the capacitance characteristic of the poly-Si TFT, we measure the poly-Si TFTs with various channel length and LDD length. We observe that the measured C-V curve is shifted as the frequency increases in Fig.3-1-1(a) for the TFTs with small channel length, and the frequency dispersion phenomenon appears in depletion region as the frequency increases in fig.3-1-1(b) for the TFTs with large channel length. These devices in Fig.3-1-1 are ELA n-type poly-Si TFT, which channel width is 600μm and ELA laser energy is 380 mJ/cm^2. In Fig.3-1-1(a), the curves are shifted toward the positive gate voltage as the measured frequency increases from 10 *kHz* to 1 *MHz*, and the difference of the gate voltage is 0.7V. In the turn-off region and the turn-on region, the values of capacitance dose not change as the measured frequency increased. Capacitances in these two regions are independent with the measured frequency. In Fig.3-1-1(b), the curves appear the frequency dispersion phenomenon as the measured frequency increases from 1 *kHz* to 100 *kHz*. The measured frequency increase from 1 *kHz* to 10 *kHz*, and the curve is shifted toward the positive gate voltage. As the

measured frequency increases above 10 *kHz*, the values of capacitance start to decrease in the depletion region and the turn-on region. In the turn-off region, the value of capacitance dose not change as same as Fig.3-1-1(a). Capacitance in the turn-off region is independent with the measured frequency, and in the depletion region and the turn-on region are depend on the measured frequency. Compare to these two figures, the frequency dispersion is observed easily for the device with large channel length, and the curves starts to disperse at low measured frequency.

Fig.3-1-2 shows the C-V curves of n-type poly-Si TFT with various channel length. The channel width of these devices is 600μm, and the measured frequency is 10 *kHz*. The value of capacitance in the turn-off region dose not change as the measured frequency increases, but that in the depletion and the turn-on region are increase as the measured frequency increases. In the turn-on region, the value of capacitance increased from $1.36\times10^{-12}\,F$ to $1.02\times10^{-11}\,F$ with channel length increasing from 4 μm to 30 μm. The turn-on capacitance grows with the channel length. In the previous studies, B. J. SHEU addressed a simple capacitance method for determining the channel length of devices [3.1]. The capacitance method is based on the linear relationship between the intrinsic gate capacitance and the effective channel length. In this method, the intrinsic gate capacitance can be expressed as

$$C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}W(L-\Delta L).$$

To extract the value of capacitance in the turn-on region, the plot of capacitance versus channel length for poly-Si TFTs is shown in Fig.3-1-3. This curve is a straight line. The intercept of the straight line at the abscissa gives $\Delta L = 0.24\,\mu m$. The correlation coefficient for the straight line is better than 0.9998. Using W = 600 μm and the slope in Fig.3-1-3, gate-oxide thickness is determined to be 60.7 *nm*. This line is almost through the origin. This analytical result proves that the measured value of capacitance is the oxide capacitance of devices in turn-on region.

Fig.3-1-4 shows the C-V curves of n-type poly-Si TFT with various LDD length. The channel width (W) is 600 μm, the channel length (L) is 6 μm and the measured frequency is 10 *kHz*. The values of capacitance are not variable with LDD length increasing from 0.25 μm to 3.00 μm in the turn-off region, the depletion region, and the turn-on region. To extract the value of capacitance in turn-on region, the plot of capacitance versus LDD length for poly-Si TFTs is shown in Fig.3-1-5. This curve is a horizontal straight line, and the values of capacitance are almost the same, $2\times10^{-12}\,F$. This analytical result proves that the value of LDD length dose not influence the measured value of capacitance.

3-1-2 Poly-Si TFTs with the fabrication process, GI-clean step

Observing the measured result of capacitance can describe the change of the film with various fabrication processes. Fig.3-1-6 shows the C-V curve of the devices with

or without the fabrication process, GI-clean. These characteristic of device in Fig.3-1-6(a) is about p-type poly-Si TFT and in Fig.3-1-6(b) is about n-type poly-Si TFT. The W/L of the poly-Si TFT is 600μm/6μm, and the measured frequency is from 10 *kHz* to 1 *MHz*. The red curves stand for the device with doing GE-clean step, and the blue curves stand for the device without doing GI-clean step. This fabrication step, GI-clean, is to clean the surface of poly-Si layer before depositing the dielectric oxide layer on the poly-Si layer. In previous studies of C–V measurements [3.2], the fixed charges in the gate oxide of TFTs are not affected by a small applied signal, whereas the trap states in the band-gap respond to the applied frequency. If the *C–V* curve of the TFTs was slightly stretched out with increasing frequency, which may be attributed to an increase of the interface trap states. If the *C–V* curve of the TFTs was significantly shifted with increasing frequency, which may be attributed to an increase of trap states at the grain boundary. In these figures, the red curves are shifted toward the negative gate voltage, 3 V about p-type TFT and 4 V about n-type TFT. There is no stretched phenomenon in comparing the red curves to the blue curves. This analytical result proves that the flat-band of both type devices shift to negative side after GI-clean which indicates that GI-clean only increases positive trap states.

3-1-3 C-V measurement with various osc level

C-V curve is measured by DC signal added AC signal gate voltage, and the osc level is the height of the step gate voltage. With various osc level, the measured range of the gate voltage are different. With large osc level, the measured range is large, and the measured result of the capacitance is a comprehensive result of the poly-Si film. With small osc level, the measured range is small, and the measured result of the capacitance is a detailed result of the poly-Si film. Fig.3-1-7 shows the C-V curves of n-type poly-Si TFT with various osc level. The W/L of the poly-Si TFT is 600μm/6μm, LDD Length is 0.75 μm, and the measured frequency is 10 kHz. The range of osc level is from 0.1 V to 1.0 V. In the turn-off region or the turn-on region, the value of capacitance does not change with various osc level. In depletion region, the variation of capacitance is obviously different with various osc level. The red curve is measured by osc level 0.1V, and it increases more sharp as the gate voltage increases. As increasing the osc level, the curve becomes to increase gradually slowly. By osc level 1.0V, the curve is blue, and it increases most slowly as the gate voltage increased. The curves with various osc level are crossed in the depletion region, and this phenomenon shows in this figure. At small gate voltage of the depletion region, the value of measured capacitance at 1.0 V osc level is larger than at 0.1 V osc1evel. As the gate voltage increasing, the curves of capacitance measuring at various osc level

come closer and closer. Then, they approach the same value at certain gate voltage. At large gate voltage of the depletion region, the value of measured capacitance at 1.0 V osc level is smaller than at 0.1V osc1evel.

Fig.3-1-8 shows the schematic of the moving Fermi level on the Electron density of state-energy curve. The square wave represents the AC signal gate voltage. The large amplitude of square wave stands for the large osc level, and the small amplitude of square wave stands for the small osc level. At small gate voltage of the depletion region, in Fig.3-1-8(a), the Fermi level is located at deep state. The low levels of the small and the large osc level are both near the states below the Fermi level, but the high level of the large osc level is more near the states above the Fermi level than that of the small osc. level. The high level of the osc level dominates at small gate voltage of the depletion region, and the large osc level can measure much more. The value of measured capacitance by using the large osc level is larger than that by using the small osc level. At the large gate voltage of the depletion region, in Fig.3-1-8(b), the Fermi level is located at tail state. The high levels of the small and the large osc level are both near the states above the Fermi level, but the low level of the small osc level is more near the states below the Fermi level than that of large osc. level. The low level of the osc level dominates at large gate voltage, and the small osc level can measure much more. The value of measured capacitance by using the small osc level

is larger than that by using the large osc level. Using this description can explain the phenomenon in Fig.3-1-7.

3-2 The analysis of the C-f curve

3-2-1 Poly-Si TFTs with various laser energy

To confer the relation between the grain size of the poly-Si film and the capacitance characteristic of the poly-Si TFT, we measure the poly-Si TFTs with various grain sizes. Fig.3-2-1 is the C-V curves of ELA n-type poly-Si TFT with various ELA laser energy densities. The W/L of these devices is 600μm/6μm, and the measured frequency is from 10 *kHz* to 1 *MHz*. The ELA laser energy densities of Fig.3-2-1(a), Fig.3-2-1(b), and Fig.3-2-1(c) are 380 mJ/cm^2, 360 mJ/cm^2, and 340 mJ/cm^2, respectively. The device performance is shown in these three figures. The shifted phenomenon of poly-Si TFT as the measured frequency increased is the most serious about the ELA poly-Si TFTs with 340 mJ/cm^2 laser energy density. The excellent performance is the ELA poly-Si TFTs with 380 mJ/cm^2 laser energy density. The frequency dispersion phenomenon in the depletion region becomes more seriously which is discussed in the previous studies.

Fig.3-2-2 shows the C-f curves of p-type poly-Si TFT with various eximer laser energy densities. The W/L of the poly-Si TFT is 600μm/6μm, and the measured frequency is from 10 *kHz* to 1 *MHz*. Table.1 lists the relationship between the laser

energy density and the average grain size. The poly-Si film with different laser energy density, the grain size of the poly-Si film is different. The laser energy is higher, the grain size will grow larger. In this figure, the red, green, and blue curves are the C-f characteristic of the ELA poly-Si TFTs with 380 mJ/cm^2, 360 mJ/cm^2, and 340 mJ/cm^2 laser energy density, respectively. The red curve is like a sloping straight line, but the other two curves decay seriously, especially the blue curve. More pronounced frequency dispersion is observed in the characteristic of the device with smaller grain size.

3-2-2 A new simulation method for C-f curve

Fig.3-2-3 shows the C-f curves for various kinds of devices. The device in Fig.3-2-3(a) is α-Si MIS, and the W/L of this device is 500μm/1000μm. Another device in Fig.3-2-3(b) is α-Si TFT, and the W/L of this device is 600μm/4.5μm. The other device in Fig.3-2-3(c) is poly-Si TFT with 380mJ/cm^2 laser energy density, and the device of W/L is 600μm/6μm. In Fig.3-2-3(a) and Fig.3-2-3(b), the C-f curves decay seriously as frequency increases. This similar phenomenon in Fig.3-2-2 is the green and blue curves. In Fig.3-2-3(c), the c-f curves are like sloping straight line as like the red curve in Fig.3-2-2. To compare Fig.3-2-2 and Fig.3-2-3, the speed of the C-f curve decay is due to the size of the grain. When the grain is small, the C-f curve decays fast, like the green and blue curve in Fig.3-2-2. Otherwise, the grain is large,

and the C-f curve decays slowly, like the red curve in Fig.3-2-2.

In Fig.3-2-4, the measured curves are simulated by using RPI model. This device is ELA n-type poly-Si TFT with 380mJ/cm^2 laser energy density. The red curves are simulated by using

$$C_{G-SD} = \frac{2C_{sx}}{(\omega r_{sx} C_{sx})^2 + 1} \tag{10}$$

and

$$C_{sx} = \frac{C_{G-SD}'}{2} = \frac{1}{2} \times \frac{C_{ox} LW}{1 + 2\exp[\frac{-(V_{GS} - V_{th})}{\eta_c V_T}]} \tag{11}$$

, these two equations of RPI model, and the blue curves are measured. These curves are not similar. The red curve decays suddenly at high frequency, but the blue curve is a sloping straight line to decay when the measured frequency increases. From this analytical result, the RPI model is not appropriate for the poly-Si TFTs with larger grain.

A new simulation of C-f is considered the Seto's model, and the simulated steps are shown in Fig.3-2-5. First, to calculate the energy barrier of grain is used by Seto's model. In the case, $N_D < N_D^*$: $X = L_G$, the potential variation in the crystallite is expressed by the following: $V_{B(x)} = -\frac{qN_D}{2\varepsilon_s \varepsilon_0}(\frac{L_G}{2} - x)^2$

In the other case, $N_D > N_D^*$: $X = \frac{N_{TA}}{L_G}$, the expressions of the potential in the two regions are shown as follows:

$$0 < x < \frac{X}{2}, \quad V_{B(x)} = -\frac{qN_D}{2\varepsilon_s \varepsilon_0}\left(\frac{N_{TA}}{2N_D} - x\right)^2$$

$$\frac{X}{2} < x < \frac{L_G}{2}, \quad V_{B(x)} = 0$$

Fig.3-2-6 shows the curve of the energy band with various gate voltages. Second, this numerical simulation is used the transient carrier emission from deep level traps in poly-Si TFTs. e_n is the emission rate [3.3][3.4], defined by

$$e_n = \gamma \sigma_n \nu_n n_i \exp\left(\frac{E_F - E_i}{kT}\right). \tag{12}$$

Using Eq.(12) and Fig.3-2-6, this simulation is putting the value of the energy band into Eq.(12) to get the relationship to the position of the emission rate, and compare the value of emission and the measured frequency.

Final, this step of new simulation is shown in Fig.3-2-7. The red region in this figure represents the activation region for a single grain. When the measured frequency is smaller the emission rate of all the carriers, all the carriers can be measured, in Fig.3-2-7(b). As the measured frequency increases, the partial carriers can not be measured due to their emission time are smaller then the measured frequency. The red activation region becomes small like Fig.3-2-7(c), Fig.3-2-7(d), and Fig.3-2-7(e). The ratio of the effective activation region (%) is equal to the activation region over the total region. Table.2 lists the parameter values of this new C-f simulation and this simulated result is shown in Fig.3-2-8. The curves for small grain size are calculated by using this new simulation in Fig.3-2-8(a) and for large

grain size are in Fig.3-2-8(b). The curves decay suddenly at high frequency in Fig.3-2-8(a), and this phenomenon is similar with the measured curve. The curves are like sloping straight line and decay slowly in Fig.3-2-8(a), and this phenomenon is also similar with the measured curves. Fig.3-2-9(a) is the measured curves and the simulated curves for small grain size, and Fig.3-2-9(b) is for large grain size. The simulation of the C-f curve is presented and shown to validate the experimental measurement. Finally, this new C-f simulation is appropriate for the poly-Si TFTs with larger grain.

Nomenclature

C_{ox} Gate oxide capacitance [F/cm^2]

E_a Activation energy [eV]

E_F Fermi level [eV]

I_D Drain current [A]

L Channel length [cm]

k Boltzmann constant [J/K]

N_A Acceptor concentration [cm^{-3}]

N_D Induce charge concentration [cm^{-3}]

N^* Critical carrier concentration [cm^{-3}]

n_i Intrinsic concentration [cm^{-3}]

q Elementary charge [1.6x10^{-19} coul.]

T Absolute temperature [K]

t_{ox} Gate oxide thickness [cm]

t_{si} Silicon film thickness [cm]

V_G Gate voltage [V]

$V(x)$ Potential at grain-boundary depletion region [V]

W Channel width [cm]

x coordinate perpendicular to the channel [cm]

ε_{ox} Oxide permittivity

ε_{Si} silicon permittivity

σ_n electron capture cross-section

ν_n the thermal velocity of electron

Table

Table.1

The relationship between laser energy density and average grain size which is defined SEM images after secco etching.

	Ec	Ec-20	Ec-40
Laser energy density (mJ/cm^2)	**380**	**360**	**340**
Average grain size (μm)	**0.60**	**0.25**	**0.15**

Table.2

The parameter values of the new C-f simulation for the W/L=600*μm*/6*μm* n-type poly-Si TFT with 1.25*μm* LDD length.

$W\ [cm]$	6.0×10^{-2}	$C_{ox}\ \ [F/cm^2]$	6.2×10^{-8}
$L\ [cm]$	6.0×10^{-4}	ε_{Si}	3.9
$t_{Si}\ \ [cm]$	6.0×10^{-6}	ε_{ox}	11.9
$N_{TA}\ [cm^{-3}]$	1.0×10^{12}	$\varepsilon_0\ \ [F/cm]$	8.85×10^{-14}
$n_i\ [cm^{-3}]$	9.65×10^{9}	$K\ [J/K]$	8.63×10^{-5}
σ_n	1.0×10^{-16}	$T\ [K]$	300
ν_n	2.3×10^{7}	$q\ [C]$	1.6×10^{-19}

$L_G\ [cm]$					
0.15			0.60		
$V_G\ [V]$	$N_D\ [cm^{-3}]$	γ	$V_G\ [V]$	$N_D\ [cm^{-3}]$	γ
0.8	5.16×10^{16}	50	0.2	1.29×10^{16}	0.003
1.0	6.45×10^{16}	50	0.8	5.16×10^{16}	0.003
2.0	1.10×10^{17}	50	2.0	1.10×10^{17}	0.003

Figure

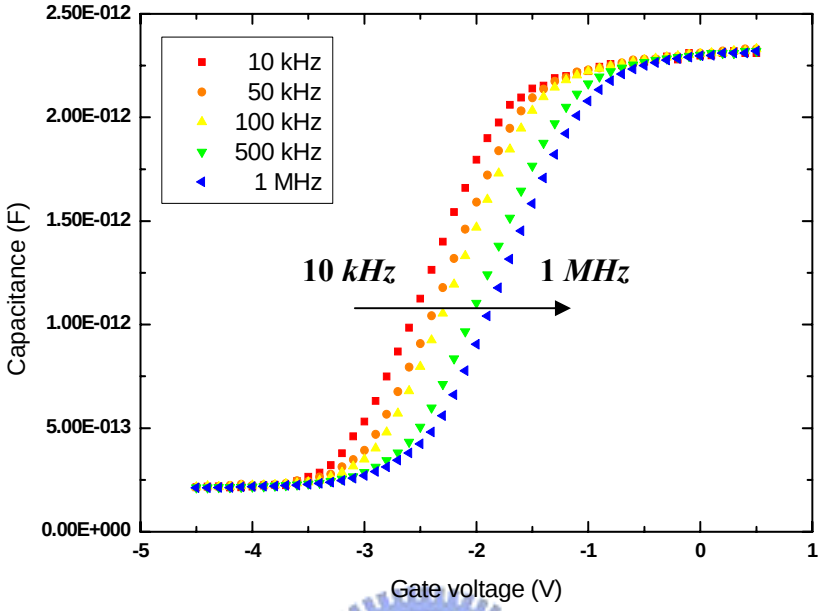


Fig.3-1-1(a) C-V curves of ELA n-type poly-Si TFT, W/L=600*μm*/6*μm*, frequency is from 10 *kHz* to 1 *MHz*, and ELA laser energy is 380 *mJ/cm²*.

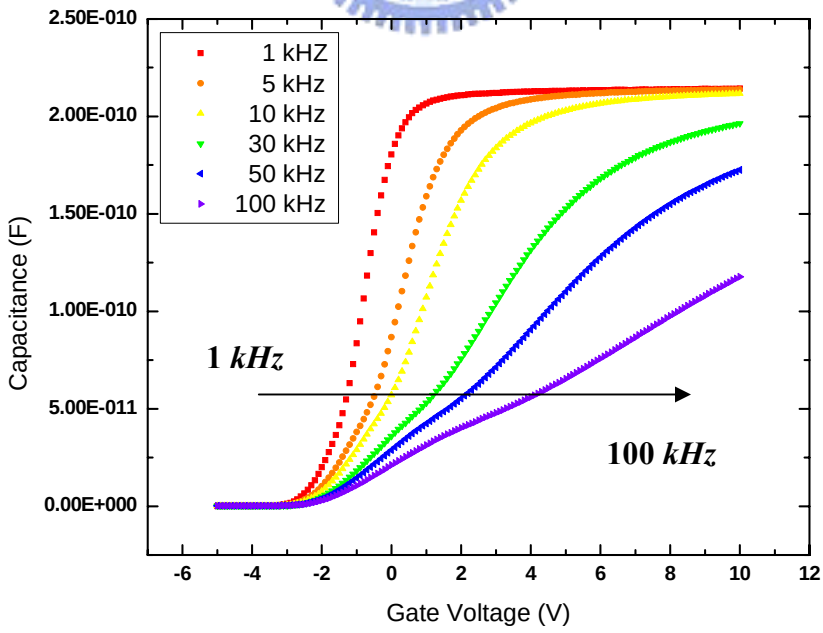


Fig.3-1-1(b) C-V curves of ELA n-type poly-Si TFT, W/L=600*μm*/600*μm*, frequency is from 1 *kHz* to 100 *kHz*, and ELA laser energy is 380 *mJ/cm²*.

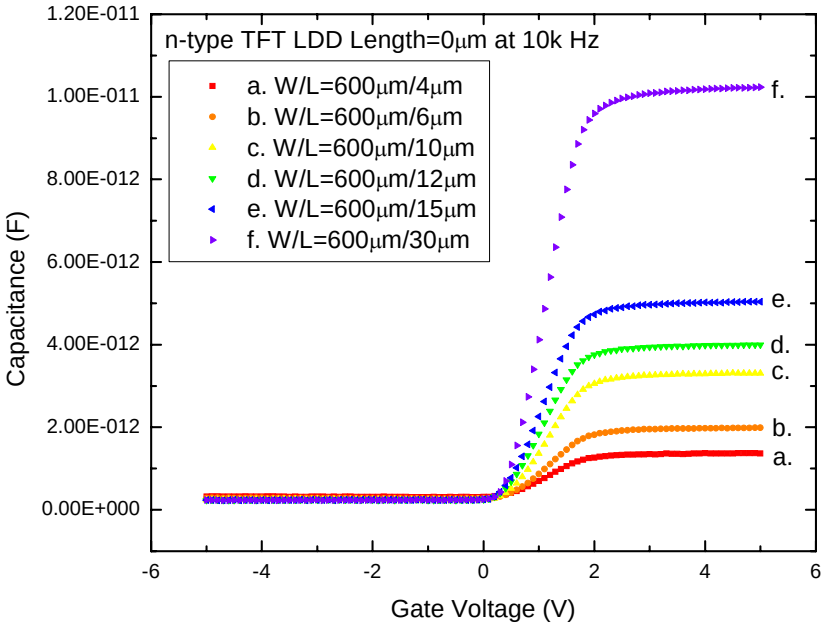


Fig.3-1-2 C-V curves of ELA n-type poly-Si TFT with various channel length at 10 *kHz*.

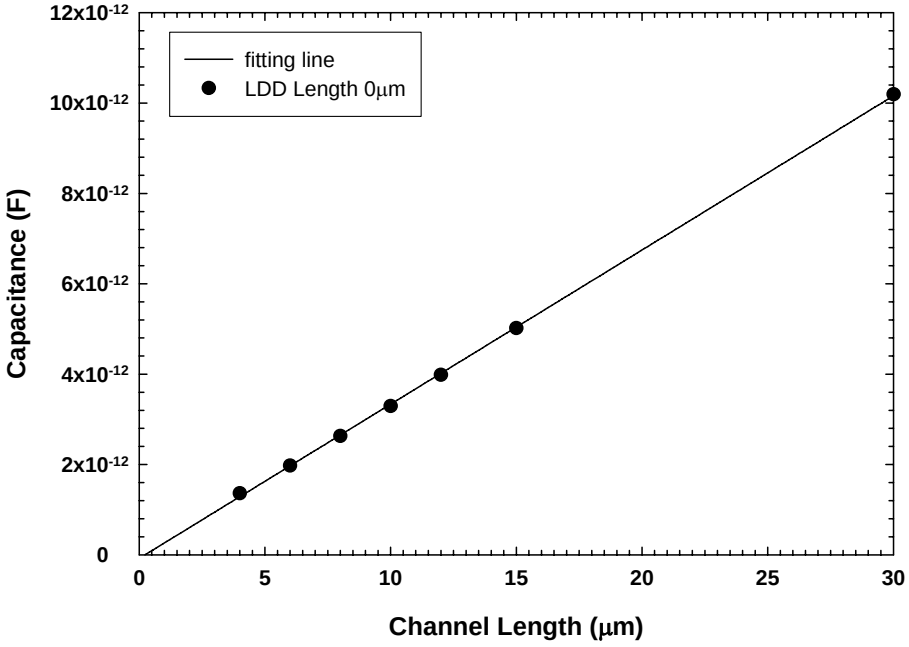


Fig.3-1-3 Capacitance-channel length curve of ELA n-type poly-Si TFT at large gate voltage.

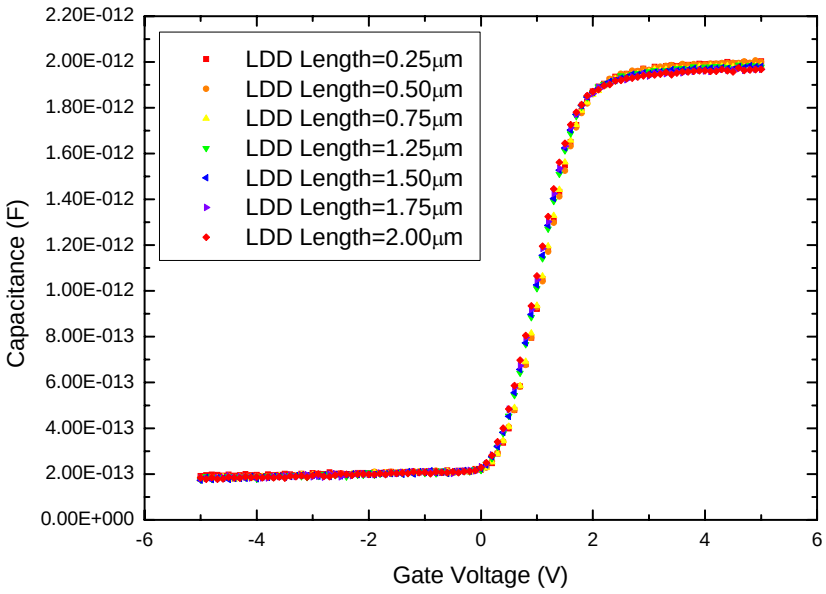


Fig.3-1-4 C-V curves of ELA n-type poly-Si TFT with various LDD length at 10 *kHz*.

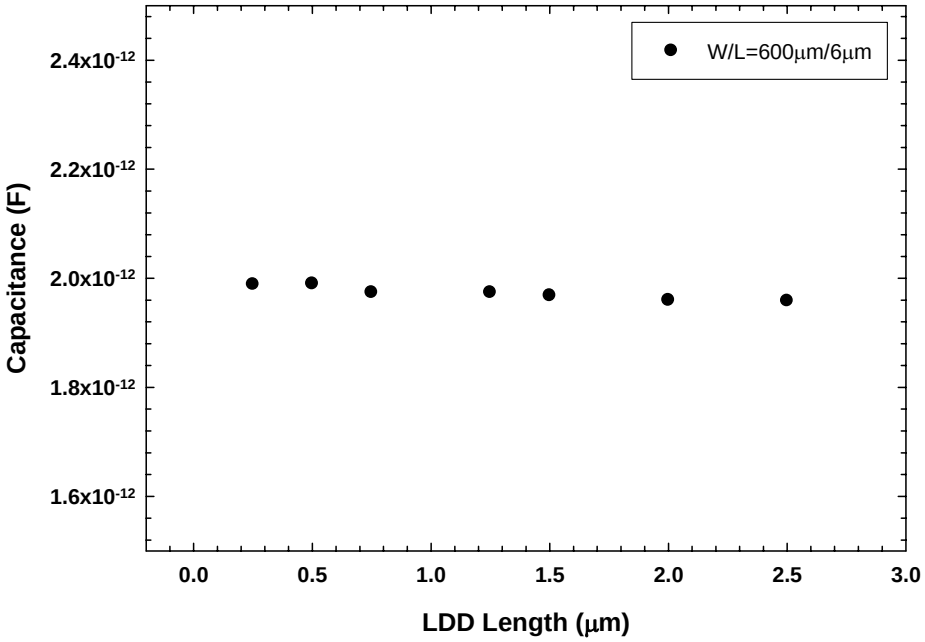


Fig.3-1-5 Capacitance-LDD length curve of ELA n-type poly-Si TFT at large gate voltage.

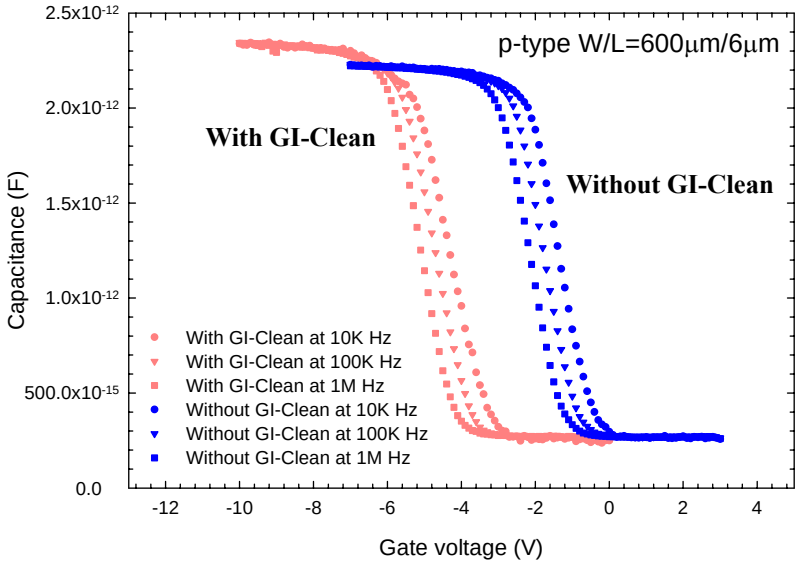


Fig.3-1-6(a) C-V curves of ELA p-type poly-Si TFT, W/L=600*μm*/6*μm*, and frequency from 10 *kHz* to 1 *MHz*. The red curves stand for the device with doing GI-clean process. The blue curves stand for the device without doing GI-clean process.

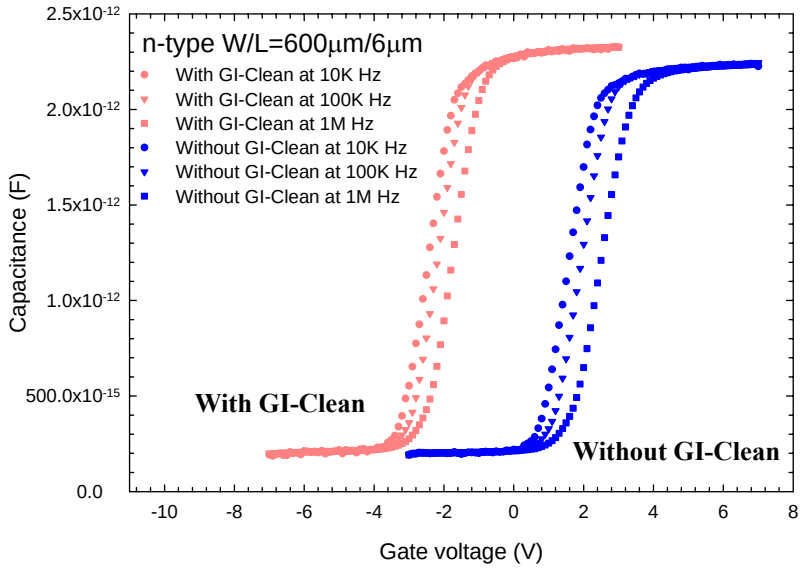


Fig.3-1-6(b) C-V curves of ELA n-type poly-Si TFT, W/L=600*μm*/6*μm*, LDD length=0.75*μm*, and frequency from 10 *kHz* to 1 *MHz*. The red curves stand for the device with doing GI-clean process. The blue curves stand for the device without doing GI-clean process.

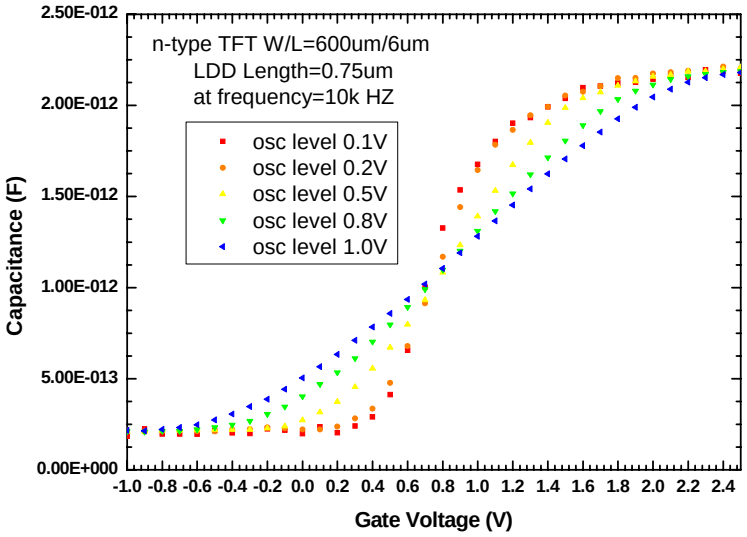


Fig.3-1-7 C-V curves of ELA n-type poly-Si TFT with various osc level at 10 *kHz*.

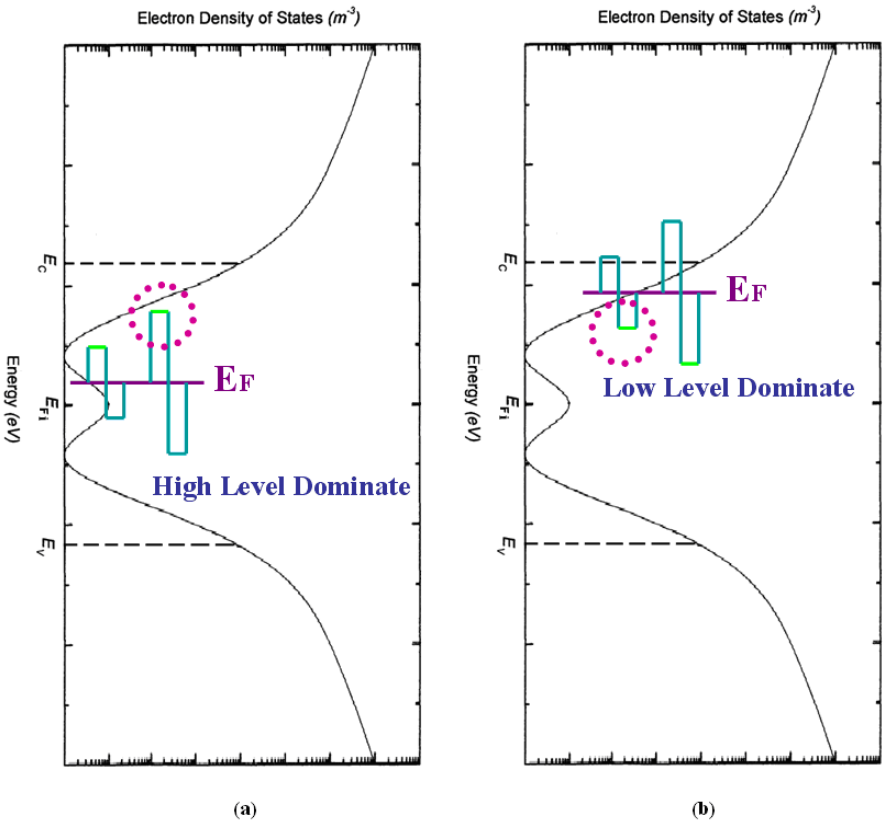
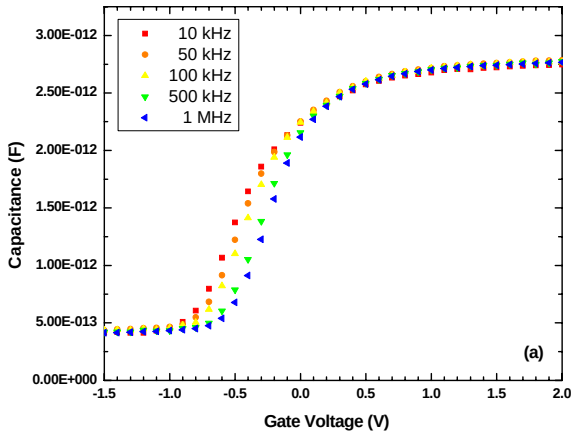
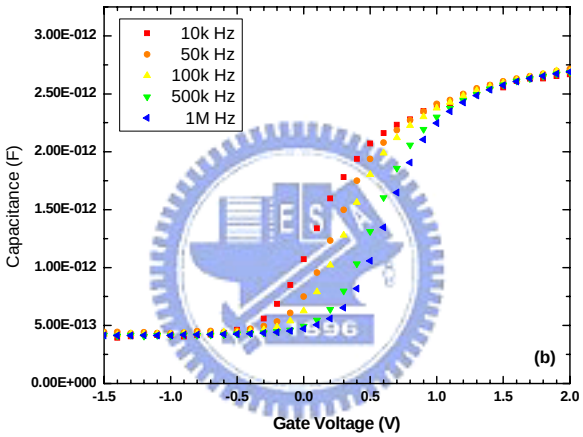


Fig.3-1-8 The schematic of the moving Fermi level on the electron density of state-energy curve. (a) at small gate voltage (b) at large gate voltage





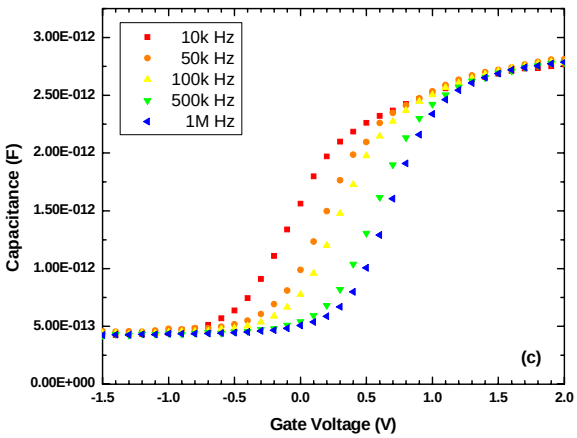


Fig.3-2-1 C-V curves of ELA n-type poly-Si TFT, W/L=600*μm*/6*μm*, frequency is from 10 *kHz* to 1 *MHz*, and ELA laser energy is (a) 380 *mJ/cm*^{2}, (b) 360 *mJ/cm*^{2},

and (c) 340 *mJ/cm²*.

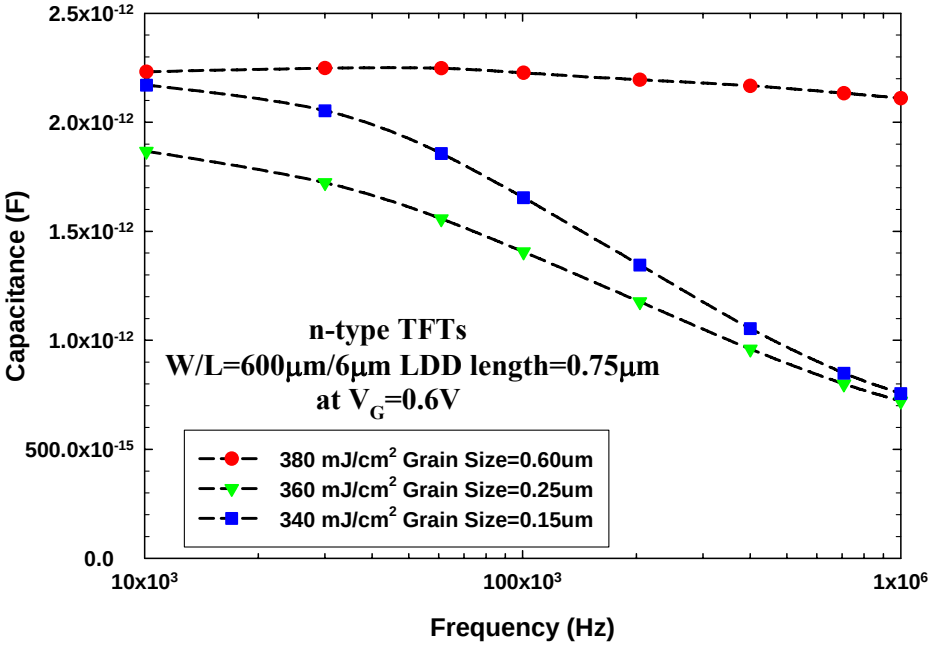


Fig.3-2-2 C-f curves of ELA p-type poly-Si TFT, W/L=600*μm*/6*μm*, with various eximer laser energy.

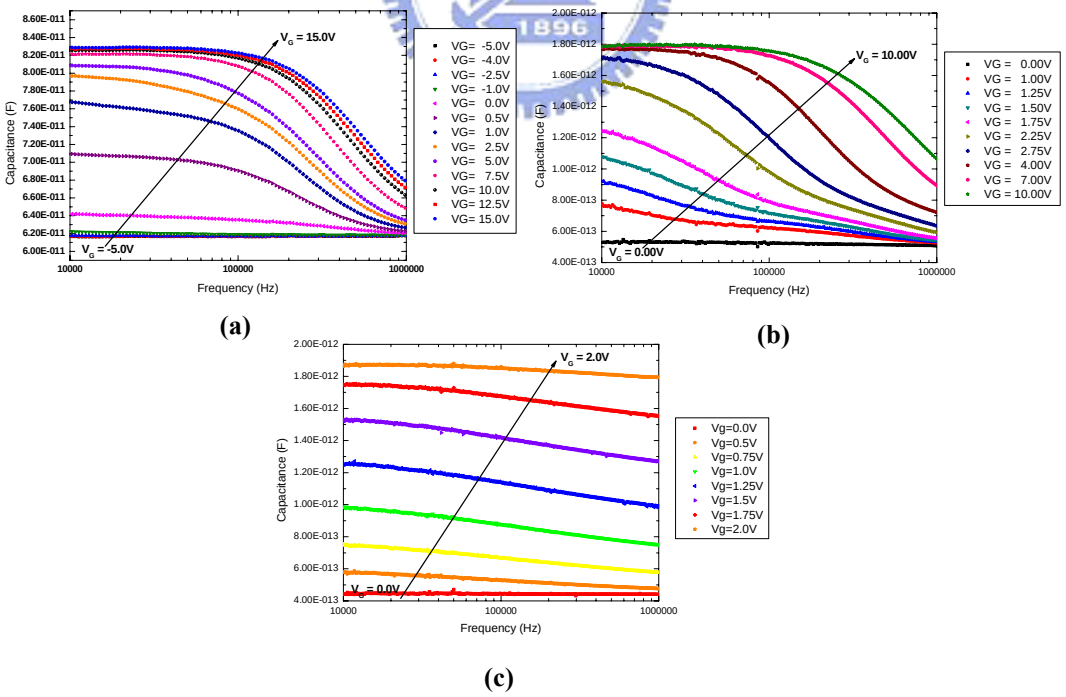


Fig.3-2-3 C-f curves of various kind of TFT. (a) α-Si MIS, W/L=500*μm*/1000*μm*. (b) α-Si TFT, W/L=600*μm*/4.5*μm*. (c) poly-Si TFT, W/L=600*μm*/6*μm*, with laser

energy density=380*mJ/cm*^{2}.

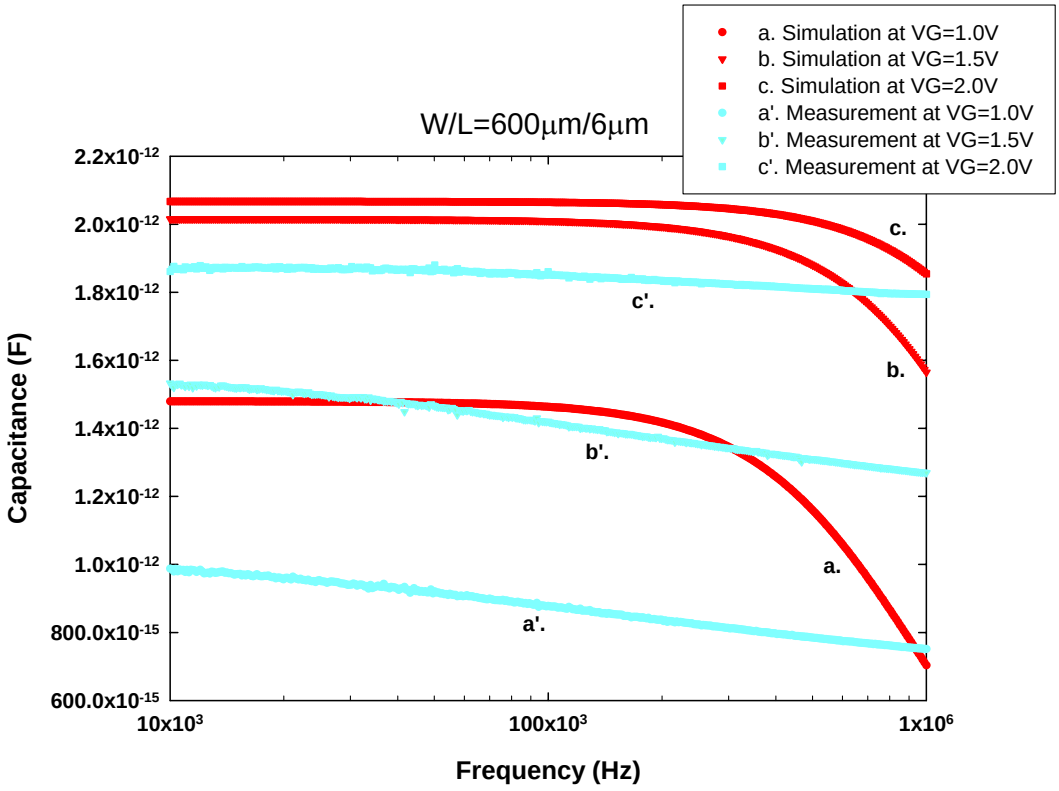


Fig.3-2-4 The curves are simulated by using the RPI model. The device is ELA n-type poly-Si TFT with laser energy density, 380*mJ/cm*^{2}.

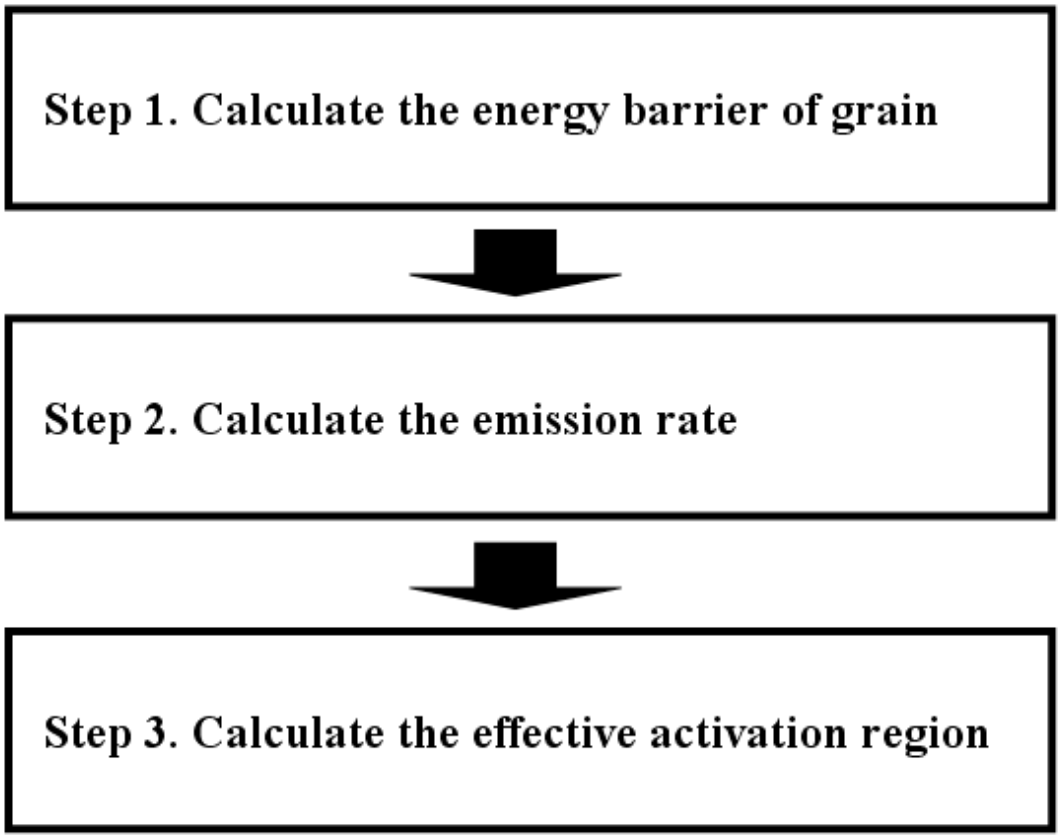
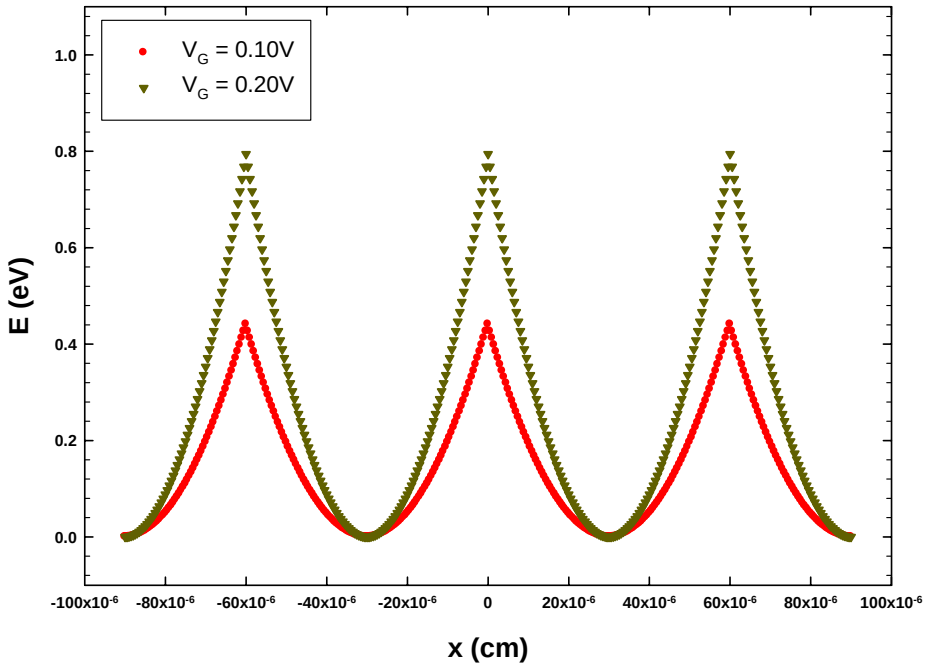
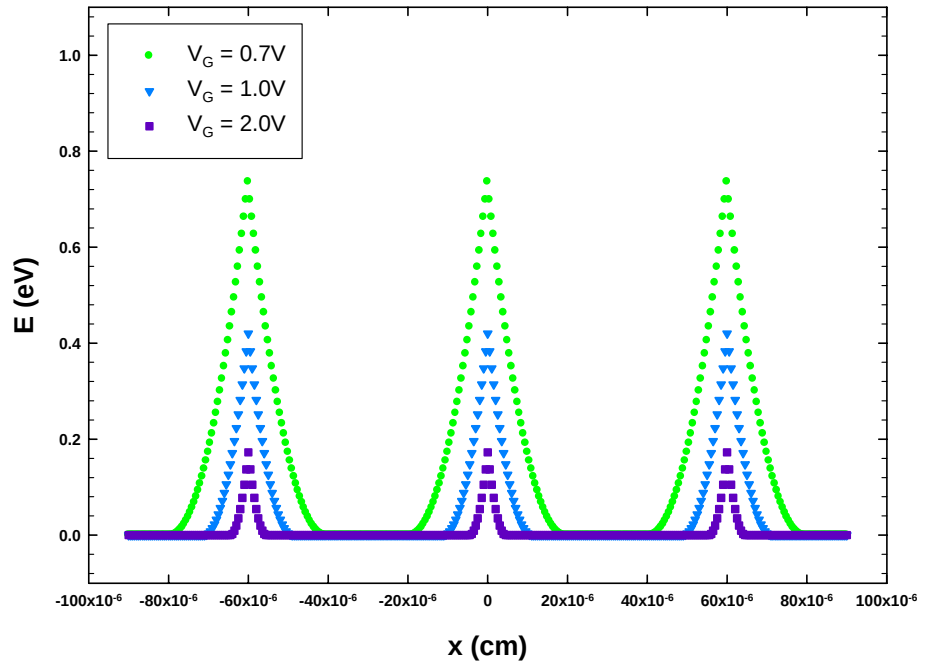


Fig.3-2-5 The schematic for the steps of this new simulation



(a) The case of $N_D < N_D^*$



(b) The case of $N_D > N_D^*$

Fig.3-2-6 The curve of the energy band with various gate voltages for grain size of 600 *nm*.

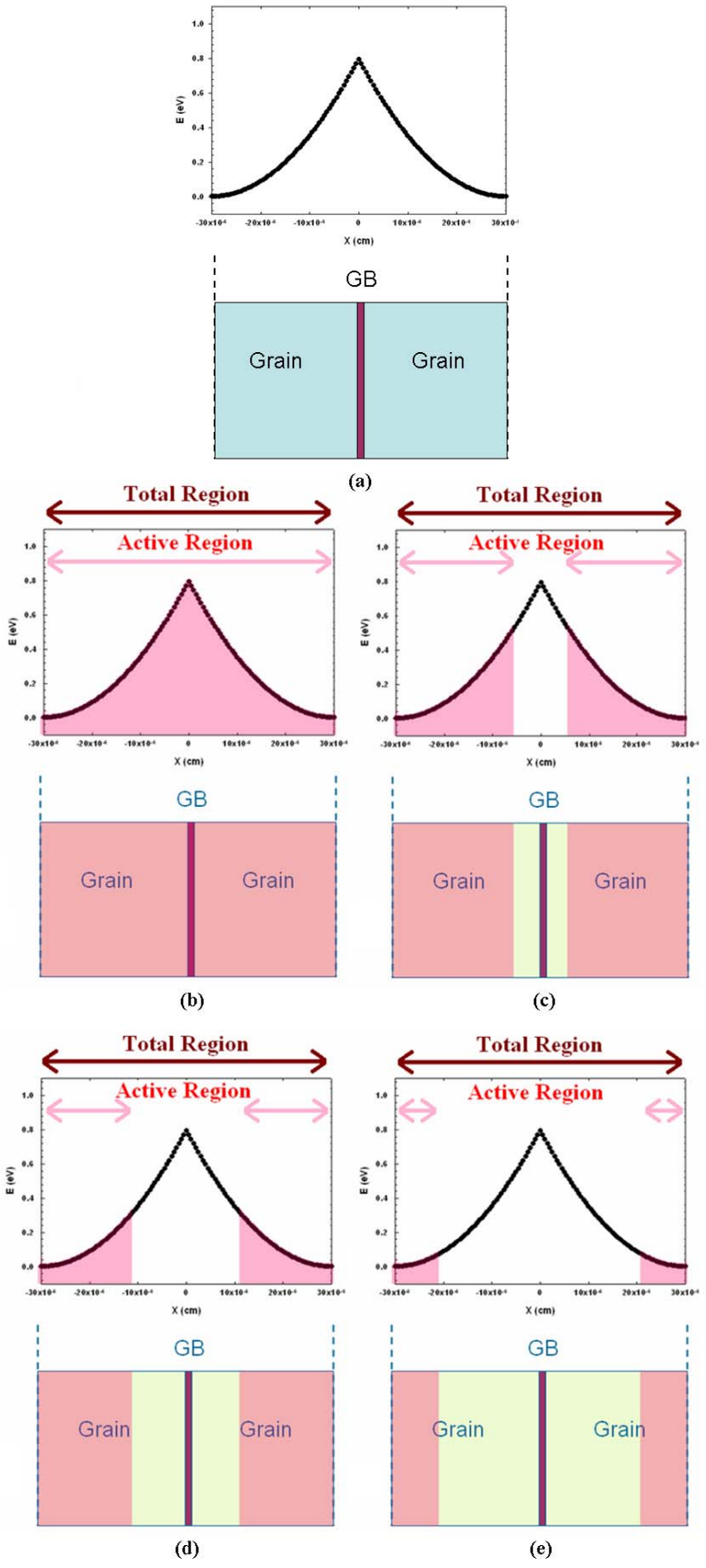


Fig.3-2-7 The schematic for the third step of this new simulation.

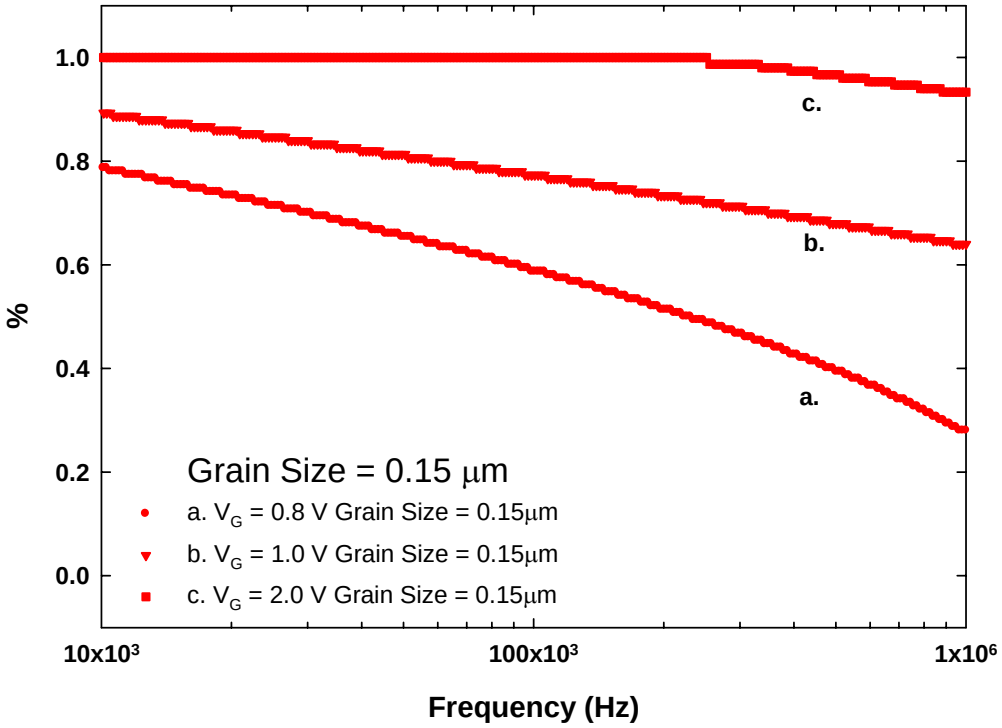


Fig.3-2-8(a) The curves are calculated by using this new simulation for small grain.

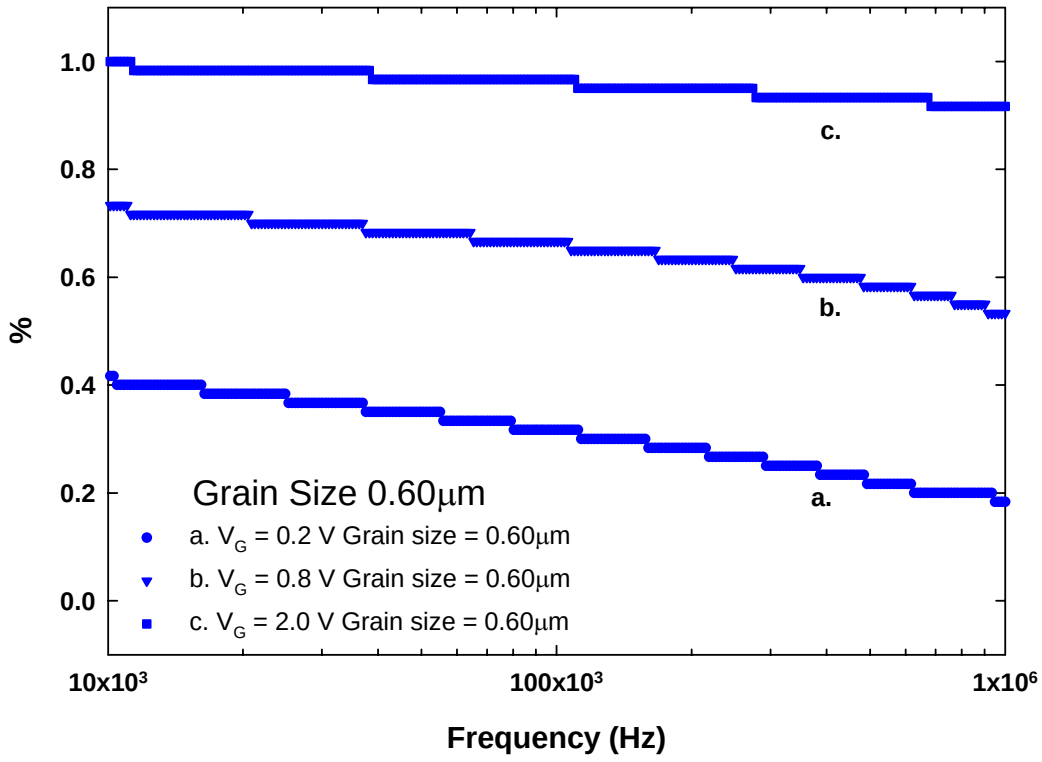


Fig.3-2-8(b) The curves are calculated by using this new simulation for large grain.

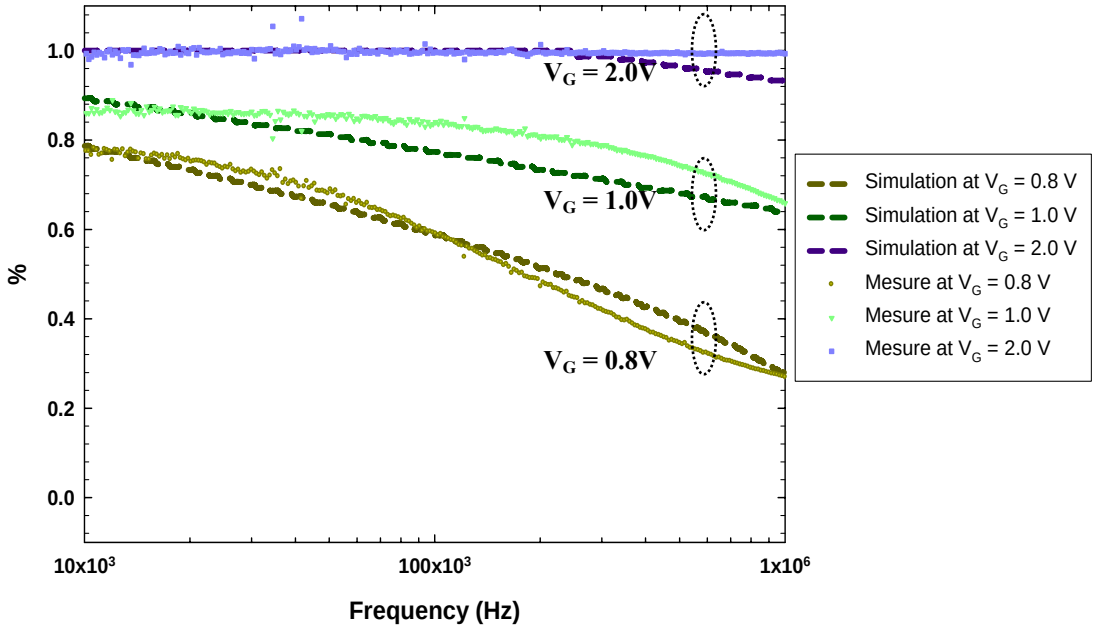


Fig.3-2-9(a) The measured curves and the simulated curves for small grain size.

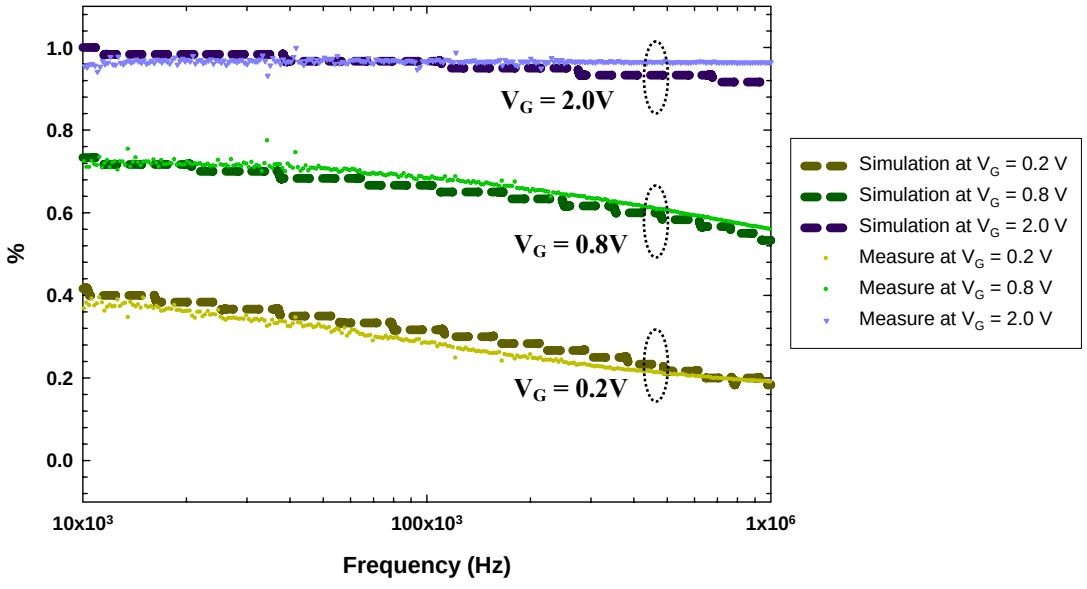


Fig.3-2-9(b) The measured curves and the simulated curves for large grain size.

Reference

[3.1] B. J. SHEU, student member, and P. K. KO, member, “A Capacitance Method to Determine Channel Lengths for Conventional and LDD MOSFET’s”, Electron Device Letters, Vol.EDL-5, No.11, November 1984

[3.2] Kook Chul Moon, Jae-Hoon Lee, and Min-Koo Han, “The Study of Hot-Carrier Stress on Poly-Si TFT Employing *C–V* Measurement”, IEEE Transactions on Electron on Devices, Vol.52, No.4, April 2005

[3.3] G.. A. Armstrong, J.R. Ayres, and S. D. Brotherton, “Numerical Simulation of Transient Emission from Deep Level Traps in Polysilicon Thin Film Transistors”, Solid-State Electronics, Vol.41, No.6, pp.835-844, January 1997

[3.4] J. G Simmons and L. S. Wei, , “Theory of transient emission current in MOS devices and the direct determination interface trap parameters”, Solid-State Electronics, Vol.17, Issue 2, pp.117-124, February, 1974

Chapter 4

Conclusion

In this thesis, the poly-Si TFTs were fabricated by excimer laser annealing recrystallization technology and the measurement work was done for the poly-Si TFTs of the same channel, various channel length and LDD length at AC small gate bias under the same environment temperature.

We studied new simulation of capacitance-frequency measurement and the classical characteristic of poly-Si TFTs. We assure the measured capacitance in turn-on region is only the oxide capacitance by varying the scale of devices. The change fabrication of devices will influence the characteristic of devices. Measuring C-V and observing the variation of characteristic curve can identify how the devices make changes after doing the varied fabrication. By this method, we can derive the better fabrication process for device.

In our experiment, we measure C-V curve by using various osc level. The value of osc level influences the measurement. Using the large value, the height of AC step signal is large, and the sweep range of gate voltage is large. We can obtain the rough of the characteristic of device in this measured result. Using the small value, we can obtain more details of the devices.

In the past, the grain size if the poly-Si film is small. The characteristic of this device can simulate by using RPI model appropriately. When the poly-Si TFT technology is improving, the grain size becomes much larger. The pronounced frequency dispersion of poly-Si TFT is not serious, and the RPI model or the pre-studies is not appropriate for the poly-Si TFTs when the grain size of device is larger. In our study, we use a new simulated method for the poly-Si TFTs with large grain or small grain. There are grain boundaries in the poly-Si material, and these grain boundaries act as energy barriers that the carriers have to come. The grain boundaries are crucial. We consider the emission time of the carrier for poly-Si TFTs. In this analysis result, the simulation and the measurement are appropriate for the characteristic of this device.