Chapter 1

Introduction

1.1 Background

1.1.1 Memory Device

In 1967, *D. Kahng* and *S. M. Sze* invented the first floating-gate (FG) nonvolatile semiconductor memory in *Bell Lab.* [1]. Owing to the improvement of the leakage current and power consumption, the nonvolatile semiconductor memory devices play an important role in memory applications because of its low-voltage and low-power features for portable commercial devices.

Very recently, *organic semiconductor devices* such as light-emitting diodes, photovoltaic cells and transistors have aroused noticeable applications due to the admirable advantages of low-cost manufacture, high mechanical flexibility, and particular characters of the chemical structures [2, 3, 4, 5]. So far a lot of research has been made to focus organic electronics devices on universal and excellent memorial devices comprising fast, new, inexpensive, non-volatile methods to store information and have astounding retention and endurance properties. Many researchers study organic thin-film materials for the nonvolatile memory (NVM) applications and attempt to accomplish on the glass or plastic substrate [6,7,8]. In order to design novel memory devices by using organic and polymeric materials, several groups develop advanced techniques to create organic memories. For example, a high performance organic electrical bistable device (OBD) exhibits the phenomena to precisely control conductivity behavior of a positive/negative voltage pulse for switching

(write/erase) application with triple-layer structure composed of an organic/metal/organic, interposed between an anode and a cathode [9]. A superior ferroelectric memory made of metal/ferroelectric/semiconductor field-effect transistor (MFSFET) is applied for saving electrical power and decreasing the size of the memory cell that can be achieved higher memory effect with two metal-organic insulators by using metal-organic chemical vapor deposition（MOCVD) [10]. Referred to memory effect, the hysteresis mechanisms about the shifts of threshold voltage are extensively discussed and associated with gate dielectric summarized well by *Katz et al* [11]. Additionally, the hysteresis effect is also explained by charge trapping stored in the localized states and influenced by the measurement condition. On the other hand, *Street et al*. propose bipolaron mechanism with diverse modification layer for a model of bias-stress effect and use a good material subject to the charge trapping effect, resulting in a shift of threshold voltage when repeated twice [12,13]. In the case of organic memory based on pentacene-based field-effect transistor on SiO_2, *Baeg et al.* demonstrate the use of a polymeric gate electret and the method of programming/erasing behavior to control conspicuous shifts of the threshold voltage, enhance good transistor properties, and obtain large memory windows [14]. Moreover, metal nanoparticle layers as significant charge-storage elements show remarkable non-volatile and rewrite memory behavior; and further, it is made to improve the performance of nanocrystal memory by replacing SiO_2 with high dielectric constant (*k*) materials, especially embedded with germanium (Ge) nanocrystals [15, 16].

Materials such as high-permittivity (high-*k*) dielectrics, e.g. Ta_2O_5, HfO_2, and Al_2O_3, have been explored to replace silicon dioxide or silicon nitride in the polycrystalline silicon- or metal-oxide-nitride-silicon (SONOS or MONOS, respectively) for application in electrically erasable and programmable read only memory (EEPROM) device improve the programming and retention prosperities. Among high-*k* materials, hafnium-silicate dielectric

was frequently known to be a promising candidate for trapping material as a result of its dual-phase property and the process compatibility with the conventional complementary metal-oxide semiconductor (CMOS) process [17]. In particular, electrical properties of MOSNOS structure for an advanced memory application are demonstrated with high-*k* dielectric stacks, which combine the benefits of good trapping capability of hafnium silicate and low operation voltage of HfAlO [18]. Therefore, it is a suitable material for memory application as a trapping layer caused by defect-induced structural disorder. More importantly, hafnium silicate can yield lower leakage current than other Hf-based dielectrics with the same equivalent oxide thickness (EOT) because of its large band gap and heavier electron effective mass [19].

1.1.2 Statement of Inorganic Dielectric Materials for OTFTs

In current-generation inorganic integrated circuit technologies, SiO_2 grown in situ on doped silicon wafers is the most widely used gate insulator despite its relatively low **dielectric constant** (***k*** = 3.9) and substantial tunneling currents when very thin films are employed [20]. So far limitations have been compensated by device engineering and the outstanding carrier mobility of (poly) crystalline inorganic semiconductors, which enable to low voltage operation. In the field, the driving force for high-*k* insulators is the need to increase TFT density on integrated circuits when preserving good insulator properties [21]. The use of appropriate high-*k* materials would afford greater surface charge densities at the TFT semiconductor-dielectric interface from greater polymer thickness with low leakage current compared to lo-*k* dielectric. By taking the place of low dielectric constant (*k*), parts of charge carriers enough to fill entire traps is caused from the field effect at smaller gate

bias when using higher dielectric materials. Table1.1 exhibits important metrics and related statistics for high dielectric, including thickness (d), dielectric constant (k), device mobility (μ), and on-off ratio (I_{on}/I_{off}). With respect to a prototype material of p-type charge transport, *Dimitrakopolous et al*. are the first to use high-k oxides to reduce OTFT operating voltages and provide an insight into the gate-bias dependence on the field-effect mobility in pentacene-based OTFTs [22]. By using sputtered amorphous barium zirconate titanate (BZT, k = 17.3), barium strontium titanate (BST, k = 16), and Si_3N_4 (k = 6.2) film as the gate dielectric, the performance OTFTs such as the field effect mobility more than 0.3 $cm^2V^{-1}sec^{-1}$ and the current modulation of 10^5 are conspicuously enhanced at operating voltage as low as only 5 volts.

However, one of the challenges for high-k integration is the generation of high leakage current in utilization of OTFTs contributed by high charge-carrier concentration. Another disadvantage of high-k gate dielectric is the shift of threshold voltage instability during operating process and generic disorder caused by the high dipolar disorder at the interface that induce carrier localization and reduce mobile carrier [23]. That is, the hysteresis is blamed on trapping of charge carriers in these traps. In general, traps are related to impurities, disorders of amorphous structure with in the inorganic layer, and diverse defects of the crystalline structure of polymer films, involving point defects, grain boundaries, and dislocations. On the other hand, the morphology and grain structure of the polymer film usually are affected by the kind of substrate so it is a critical reason to consider that the polymer films with different morphology, density of structural defects, hence different substrate surface could impact on the concentration of traps.

Table1.1 Summary of the inorganic material for high dielectric [23].

Dielectric	Method [®]	D [nm]	*k*	Semi-conductor	μ [$cm^2V^{-1}s^{-1}$]	I_{on}/I_{off}	Year
BZT	sputt.	122	17.3	pentacene	0.32	10^5	1999
BST			16	pentacene	0.4–0.5		
Si_3N_4			6.2	pentacene	0.6		
Ta_2O_5	anodize	70	23	DH–5T FPcCu	~0.03 ~0.02		2000
Ta_2O_5	e-beam	100	21	P3HT	~0.2		2002
Al_2O_{3+x}	sputt.	270	7	pentacene	0.14	10^6	2003
Al_2O_3	anodize	120		PTAA	$3x10^{-5}$		2003
Ta_2O_5	anodize	86	24	pentacene	0.24	10^4	2003
Ta_2O_5	sputt.			PcCu	0.01		2003
SiO_x / SiN_x	PECVD			pentacene	0.2–0.4	~10^8	2003
TiO_2	sputt.	97	41	P3HT	$5x10^{-3}$	10^2	2004
Al_2O_3		93	8.4	P3HT	$6x10^{-3}$	10^2	
Al_2O_3	anodize	7	9–11	P3HT pentacene	$1.2x10^{-3}$ 0.06–0.1		2004
Ta_2O_5-air	sputt.		25–1	Rubrene	1.5–2.0		2004
GdO_3	IBDA	90	7.4	pentacene	0.1	10^3	2004
TiO_2+PαMs	anodize	8+10		pentacene	0.8	10^4	2005

[®]: Dielectric deposition method. Abbreviations: sputt., sputtering; anodize, PECVD, plasma-enhanced chemical vapor deposition; IBDA.

1.2 Objective and Motivation

In order to enhance device performance, many reports use the appropriate high-*k* materials to increase charge carrier densities for organic semiconductor transport. In this nonvolatile paper, organic memory with a high mobility, low operation voltage, lasting memorial effect using hafnium silicate as a gate dielectric (dielectric constant, $k = 7.14$) will be demonstrated.

General speaking, the memory effect is regard as a critical issue in OTFTs operation for other circuit applications. However, the purpose of this study is to emphasize the enhancement of memory behavior with modification polymer layer on hafnium-silicate substrate due to its intrinsic structure and chemical property.

Furthermore, the influence of photoexcited species on pentacene is the most important element for the reversible and rewrite effect. To verify reliable relationships between photoinduced relaxation and pentacene absorption, we investigate the rate of released charge at a single wavelength to interpret the experimental data. The following shows four topics :

Topic 1. Material analysis (The structure of hafnium-silicate dielectric):

- Transmission electron microscope (TEM).
- Electron diffraction pattern (EDP).
- X-ray photoelectron spectroscopy (XPS).

Topic 2. Memory effect

- Storage in the dark for one week, three weeks, one month, two months, and four months respectively.

Topic 3. Electrical characteristics

- Device performance.
- Endurance property.
- Retention ability.

Topic 4. Light–induced recovery and optical measurement

- Illumination under optical wavelengths (light frequencies) ranging from 450 nm to 670 nm.
- Three critical elements of optical experiment:

  - Control of light power intensity.
  - Calculation of photon flux density.
  - Influence of irradiation time.

- The relation between pentacene-absorption of organic semiconductor and lightinduced charge transfer.

1.3 Organization of The Thesis

This thesis is mainly composed of five chapters. The contents in each chapter are described as follows.

In this chapter, *introduction* includes background, motivation, and organization of this thesis. In particular, the concepts of high-dielectric materials are illustrated further.

In Chapter two, *principle* is consisting of the operation mechanism, device parameters, and conduction mechanism of organic thin–film transistor. Further, the transport models in the organic semiconductor are presented in detail.

Chapter three gives a description of our device fabrication process, measurement system.

Chapter four is the most important in this paper. The structure of hafnium-silicate materials will be analyzed by TEM, XPS, and EDP. The electrical characteristics of non-volatile memory device will be obtained from the capacitance (*C*)–voltage (*V*) and transfer characteristic curves. Besides, the related operation mechanism of retention ability, endurance property, memory effect, and negative/positive gate bias are explained. At the same time, the memory device with PαMs-modified layer on hafnium-silicate dielectric is mainly discussed compared with untreated device. More importantly, we stress the influence of photoexcited effect on our pentacene-based OTFTs and thereby investigate the relation between the photon number flux and the pentacene absorption.

Chapter five is the final summary of our work. In conclusions, we simply point out the experiment results and suggestions for pentacene-based memory applications.

Chapter 2

Principle

2.1 Organic Thin Film Transistors [24]

2.1.1 Operation Mechanism of Organic Thin–Film Transistors

Fig. 2.1 reveals an OTFT device configuration that we used for memory application in this study. The polycrystalline pentacene was employed to demonstrate p-type field-effect and the typical current (I)–voltage (V) measurement exhibits charge transport behavior. In our case, holes are considered the majority carrier. Thus, from the plot of drain-to-source voltage (V_{ds}) vs. gate-to-source voltage (V_{gs}), the field effect mobility and then device parameters are extracted.

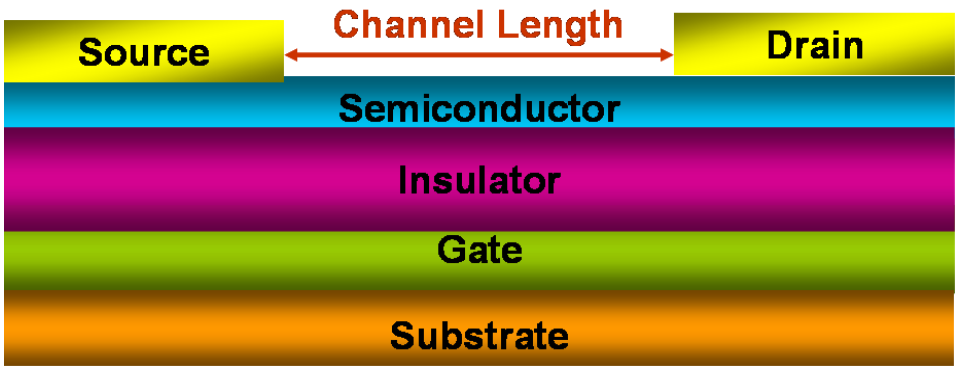


Fig. 2.1 An OTFT device configuration: the top-contact structure with the sequence deposition of organic polymeric layer and source/drain electrodes onto the gate insulator.

When the gate electrode is biased at positive voltage and the source electrode is grounded, the operation is in the "depletion mode", which means that charge carriers in the channel exist in the high channel resistance (turn-off state, I_{off}). On the other hand, while a negative V_{gs} is biased on gate electrode, an electric field is induced and a high concentration of the positive charges flow at the semiconductor/insulator interface, resulting in the "accumulation regime". In this regime, charge carriers are accumulated in the channel from the source to drain electrodes, resulting in a low channel resistance (turn-on state, I_{on}).

2.1.2 Equation

At low V_{ds}, with $-V_{ds} << -(V_{ds} - V_{th})$, I_{ds} increases linearly along V_{ds}, which is defined the "*linear regime*", and is expressed by the following equation:

$$I_{ds(linear)} = \frac{WC_i\mu}{L}\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds} \quad \textbf{(2.1)}$$

where L, W, C_i, V_{th}, and μ are the channel length, the capacitance per unit area of the insulator, the threshold voltage, and the field effect mobility, respectively. Besides, this equation can be used to calculate the trans-conductance (g_m) in the linear regime.

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}}\bigg|_{Vds=constant} = \frac{WC_i}{L}\mu V_{ds} \quad \textbf{(2.2)}$$

For $-V_{ds} > -(V_{gs} - V_{th})$, I_{ds} becomes saturated at a lager V_{ds} because of the pitch-off in the accumulation layer. Similarly, the mobility value (μ) can be calculated by the slope of the plot of $\sqrt{|I_{ds}|}$ versus V_{gs} in the saturation regime and the modeled equation is shown:

$$\sqrt{I_{ds(sat)}} = \sqrt{\frac{WC_i}{2L}}\mu\left(V_{gs} - V_{th}\right) \quad \textbf{(2.3)}$$

2.1.3 Device Parameters

In general, the typical measurements with respect to field effect mobility can directly express and calculate the performance of the device and carrier-transport abilities of the organic/polymeric materials. Besides, other device parameters such as threshold voltage (V_{th}), the ratio of the drain current I_{ds} (I_{on}/I_{off}) in the high current resistance over in the low current resistance, and subthreshold swing (*S.S*) are explicitly analyzed. A standard plot of the measurement of transfer characteristic contains a semilogarithmic plot of I_{ds} versus V_{gs} and a plot of $\sqrt{|I_{ds}|}$ versus V_{gs}, expressed in Fig. 2.2.

The threshold voltage (V_{th}) is defined as the onset voltage while the electrical conduction is formed in the channel. From equation (2.3), V_{th} represents the x-intercept of $|I_{ds}|^{1/2} - V_{gs}$ plot in the "saturation regime". The on/off current ratio (I_{on}/I_{off}) shows the ratio of the current when the device is turned on ($V_{gs} \neq 0$) and when the device is in the off state ($V_{gs} = 0$):

$$\frac{I_{on}}{I_{off}} = \frac{\mu C_i V_{gs}}{2\mu_r q N_A t} \qquad \textbf{(2.4)}$$

where μ_r is the device mobility, N_A the carrier concentration in the off state, t the device film thickness, and q the electron charge.

Furthermore, the sub-threshold swing (*S. S.*) in equation (2.5) reveals the speed of turn-on/turn-off switch during the process of operating device. Note that these important analyses of experiential parameters are depicted in Fig. 2.2.

$$S.S. = \frac{\partial V_{gs}}{\partial(\log I_{ds})} \qquad \textbf{(2.5)}$$

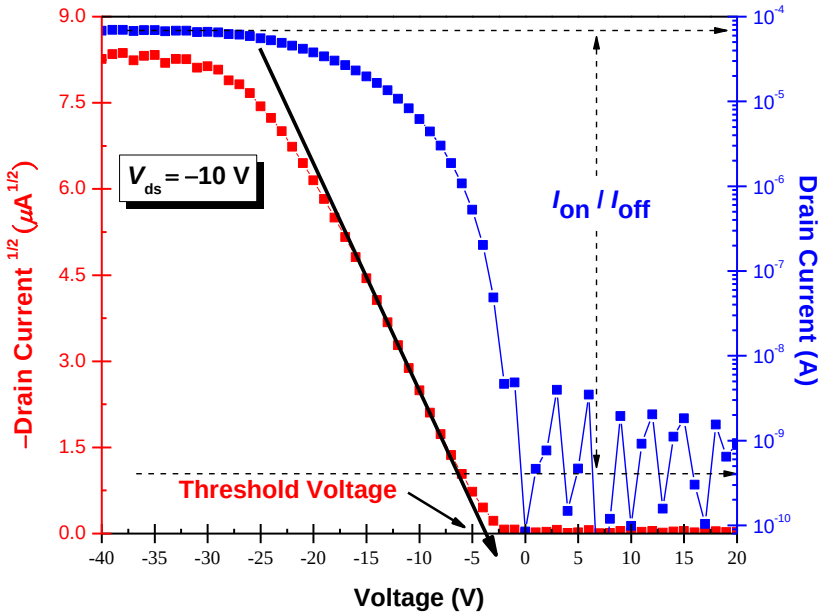


Fig. 2.2 A semilogarithmic plot of I_{ds} versus V_{gs} (right y-axis) and a plot of $|I_{ds}|^{1/2}$ versus V_{gs} (left axis) at a fixed drain voltage of –10 V.

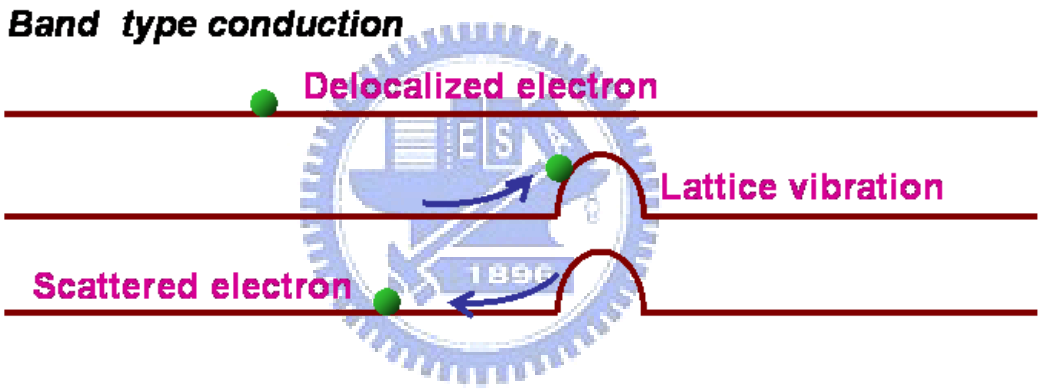
2.2 Conduction Mechanism in the Organic Semiconductor [25]

As a rule, it is expressed by the straight line or band-like description corresponding charge transport in a perfect crystal and a free charge is considered as the delocalized carrier (Fig. 2.3(a)). There are always lattice vibrations in Fig. 2.3(b) destroying the crystal symmetry and forming scattered electrons with these phonons, which resists the charge carrier transport. The mobility for band like transport decreases with increasing temperature, meaning that the acutely vibration of lattice limits the transportation of carriers motion. However, the carrier is localized due to defect, structure disorder or self-localization, e.g. in hopping transport system. On the subject of polarons, the lattice vibrations are essential

condition for a carrier that moves from one site to another. For hopping transport, the mobility usually increases with increasing temperature.

The study of disordered lattice is quite significant in material analysis and physical application. In fact, many materials are not perfect and have some defects which cause to disorder-related effects. Therefore, there exist local distributions of site-energies, such as disordered alloys and amorphous materials.

(a)



(b)

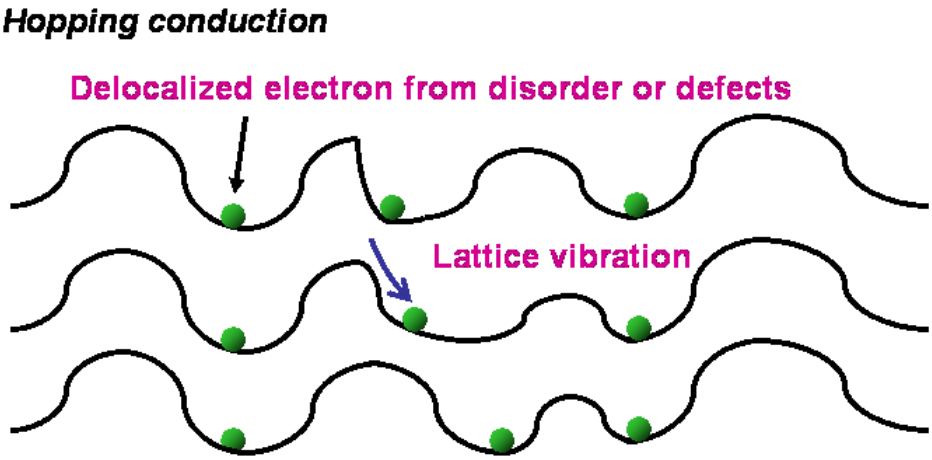


Fig. 2.3 Charge transport mechanisms in solids. (a) Band-type conduction. (b) Hopping conduction. Both band transport and hopping transport are adapted from reference.

2.3 The Transport Models

2.3.1 Multiple Trapping and Release (MTR) Model

For the polycrystalline organic semiconductors, the temperature-related charge transport can be interpreted by MTR model [26]. Because defects (dangling bounds and grain boundaries in the amorphous material or polycrystalline devices) act as usually charge traps, the MRT model assumes there localized levels in the energy gap as sketched in Fig.2.4. The organic semiconductor film consists of crystallites, which are separated from each other by grain boundaries. While charges move in middle of the crystallites, the carriers can move in delocalized bands, although in the grain boundaries, they turn into the traps in localized states. However, it is not clearly to distinguish hopping transport from multiple trapping and release, mentioned the relation between temperature and the carrier motilities. The drift mobility, μ_D, is given by:

$$\mu_D = \mu_0 \alpha \exp\left(\frac{-E_t}{kT}\right) \quad \textbf{(2.6)}$$

where, μ_0, E_t, and α are the mobility at the band edge, the energy of the trap state, the ratio between the effective density of states at the transport band edge and the density of traps.

From the pervious literature, the multiple trapping and release (MTR) model, this is widely used in the behavior of a–Si: H TFT, seems to explain well the observed characteristics [27]. The model has been also successfully used in the past to describe the operation of α–6T (α-sexithiophene) and DH6T (α–ω–dihexylsexithiophene) device characteristics [28]. According to this model, a large concentration of traps exists in the forbidden gap above the valence band edge.

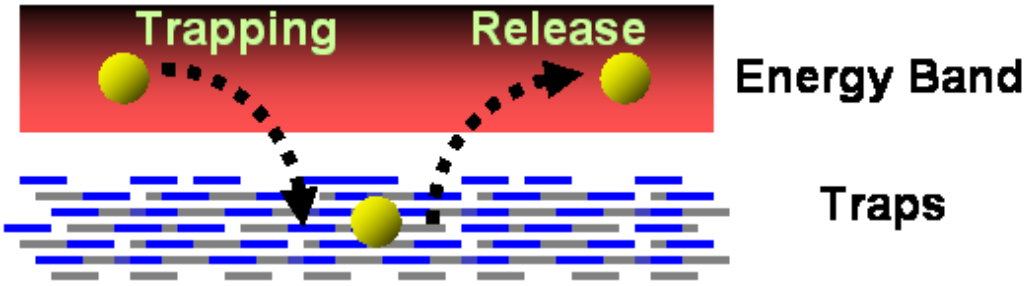


Fig. 2.4 In the MTR model, a narrow band narrow contains a high concentration of trap levels.

The trapping and release of charge carriers in the localized state lead to a thermally activated behavior of the device mobility. At the low gate bias, most of the holes injected in the semiconductor are trapped into the localized state. The deepest traps are filled first and carriers can be released thermally. While increasing the negative gate bias, the Fermi level approaches the valence band edge and more traps are filled. At an approximately high voltage, all traps state are filled and subsequently injected carriers move with the microscopic mobility associated with carriers in the valence band or highest occupied molecular orbital, HOMO.

2.3.2 The Polaron Model [29]

Polaron effects for charge transport are discussed in organic materials extensively. The basis concept of polaron connects with quasi-particle or the disorder-induced localization of charges, implying that a localized charge carrier is coupled to local polarization or vibrations and/or rotations of the molecules. In other words, the strong electron-phonon coupling brings about localized state of charge carriers. An excess charge carrier on a conjugated polymer chain can minimize its energy because of the local lattice

distortion. This composite object consisting of charge (e.g. electron) and a reformed lattice, or phonon cloud, is called a polaron. As electron-phonon or phonon-phonon interaction impacts on the local distortion of the lattice and the associated energy levels must split off forming HOMO and LUMO levels.

As for bipolaron in the organic chemistry, it is a molecule or part of a macromolecular chain containing two positive charges in a conjugated polymer. These charges can be located in the center of the chain or at its terminuses. While two polarons become close together, they decrease their energy to attain the lowest energy or stable state by sharing the same distortions, which can lead to an effective attraction between the polarons. However, the interaction is adequately large that the great attraction causes a bound bipolaron. Simply, bipolaron is formed with a bound pair of two polarons and can be accounted a negative energy state which recovers the bound state from the unpaired polaron state by an apparent relaxation of the polymer backbone. The formation of the hole pairs or bipolaron, $(hh)_{BP}$ and reverse dissociation is described by the following reactions and kinetics:

$$h + h \leftrightarrow (hh)_{BP} \tag{2.7}$$

$$\frac{dN_h}{dt} = -kN_h(t)^2 + bN_{BP}(t) \tag{2.8}$$

$$N_{b0} = N_h(t) + 2N_{BP}(t) \tag{2.9}$$

where N_h and N_{BP} are the hole and bipolaron concentration, respectively. Both k and b are temperature-dependent constants, which represent the rate of corresponding parameters. The value of N_h is obtained by measuring as a function of time at a constant V_{gs}. and oppositely as a function of V_{gs} at the fixed time [30].

2.3.3 Hopping Charge Carrier Transport

In disorder materials, the charge transport can be described using the hopping mechanism while the mobility depends on both temperature and gate voltage. The jump motion of particles in a lattice with site-energy disorder is a typically model to describe hopping transport in organic semiconductors. The hopping effect mainly takes place around the Fermi level. Besides, many models of the carrier hopping expand the concepts, depending on the rate of carrier jumps as described by Miller and Abrahams expression [31]. In this model, the rate υ of a tunneling carrier jumps over the distance r between an occupied site of the energy E_s and an adjacent unoccupied site of the energy E_t. The probability of tunneling carrier, υ, which can indicate in term of hopping parameter, u, as:

$$\upsilon = \upsilon_0 \exp(-u) \tag{2.10}$$

$$u = 2\gamma \cdot r + \frac{E_t - E_s}{k_B T} \cdot \eta(E_t - E_s) \tag{2.11}$$

where υ_0, γ, η are the attempt-to-jump frequency, the inverse localization radius, and the unity-step function, respectively. T represents temperature, and k_B is the Boltzmann constant. Moreover, this model points out that the hopping rate decreases at low temperatures, supposing that the electron-lattice coupling is very weak.

As the Miller-Abrahams opinion is used to polymeric materials, this concept is capable of applying to semiconductor and has convincing argument, even at high temperature. Based on the energetic and structural disorder of the hopping system, it can be favorable to hop over a longer distance with low activation energy (energy difference between E_t and E_s sites) than over a shorter distance with higher activation energy. This extension from the Miller-Abrahams model is called variable range hopping [32]. Besides, *Horowitz et al.* develop a model to describe hopping transport around the Fermi level in an exponential

density of states [33]. They indicate that the analytic treatment of hopping model is related with a similar model, where charge carriers are thermally activated to a transport level.

In point of some amorphous materials, *Bassler et al.* propose that the effective zero-field activation energy, E_{a0}, of the device mobility in a unstable hopping system with a Gaussian density-of-state (DOS) distribution can be expressed by the calculation of in disorder and polaron effects. The following equation:

$$E_{a0} = E_a^{(p)} + E_a^d = \frac{E_p}{2} + \frac{4}{9}\frac{\sigma^2}{kT} \qquad \textbf{(2.12)}$$

where $E_a^{(p)}$, $E_a^{(d)}$, and σ, are the polaronic contribution, disorder contribution, the width of the density of state (DOS) distribution, respectively. In organic materials, $E_a^{(p)}$ is almost determined by short-ranged relaxations, hardly to be affected from long-ranged disorder, and can be considered as a well-defined material parameter, hence they are regarded as the polaron effect on trap-controlled and hopping charge transport of polarons in the disordered materials.

Chapter 3

Experimental

3.1 Device Fabrication

3.1.1 Preparation of Substrates

In this study, a 90 nm-thick hafnium (Hf) silicate was deposited as the gate dielectric by metal-organic chemical vapor deposition (MOCVD) using an AIXTRON Tricent system under a wafer temperature of 500 ℃. The substrates consisting of heavily n^{++}-doped (0.001 Ω cm) (100) silicon wafer and Hf-silicate dielectric were used for pentacene devices.

To remove organic contaminants, the substrates were rinsed in de-ionized (DI) water for 5 minutes, dipped in $H_2SO_4 + H_2O_2$ (H_2SO_4: H_2O_2 = 3:1, 80 ℃) solution for 20 minutes, and then rinsed in DI water for 10 minutes. Finally, the cleaned substrates were blew by dry nitrogen (N_2) gas and dried in an oven at 120 ℃ overnight. The brief description and graphical procedure were expressed in Fig. 3.1.

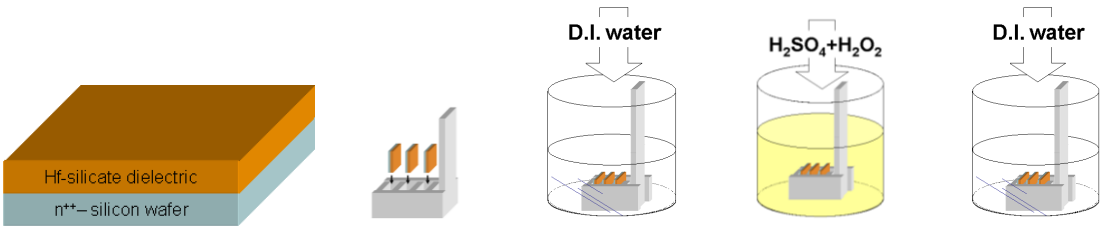


Fig. 3.1 The procedure of substrate cleaning. According to the statement and method, the surface of hafnium-silicate was cleaned.

3.1.2 Polymer Modification and Surface Treatment

It was known that dielectrics compatible with large area fabrication were explored to facilitate low cost electronics and charge transport. The morphology and the structural properties between the insulator and organic interface influenced the deposition condition on different inorganic dielectric. Therefore, surface treatment played a significant role in determining the electronic properties and was correlated with the impact of the dielectric on the device parameter of the mobility, threshold voltage, on/off ratio, subthreshold voltage swing (*S.S*), accompanying the improvement of the hole/electron mobility.

To improve the device performance of polycrystalline pentacene OTFTs, surface treatment of Hf-silicate dielectric was accomplished prior to the deposition of organic layer. That is, the films of pentacene and gate dielectric were separated by coating a thin layer of **p**oly-**α**-**m**ethyl**s**tyrene (PαMs; number-average weight $M_n = 4000$, glass-transition temperature $T_g = 76$/C) which served as the polymeric gate dielectric. Its chemical structure was sketched in Fig. 3.2. During the process of experiment, polymer was spin-coated from a 0.5 wt% solution in toluene in the air, to a 30-nm thickness and the post-annealing treatment was carried out at 100 ℃ for 1 hour to remove residual solvent entirely. In terms of film thickness and capacitance (*C*)–voltage (*V*) measurement, the capacitance per unit area and *k* value of Hf-silicate dielectric with PαMs treatment were calculated to be of 41.5 nF/cm^2 and 5.62, respectively.

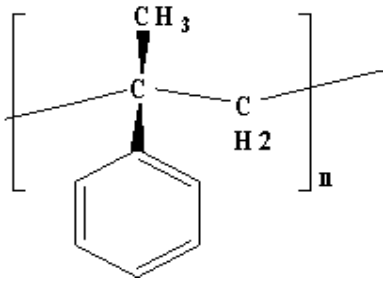


Fig. 3.2 The chemical formula of poly-α-methylstyrene (PαMS). The surface of Hf-silicate dielectric modified with PαMS by spin-coating from toluene.

3.1.3 Pentacene Growth

Among the molecular semiconductor, pentacene ($C_{12}H_{14}$) has been demonstrated as the one with highest hole and electron mobility. This material exhibits strong tendency to form highly ordered films. In our case, the growth of pentacene was deposited in the chamber via vacuum sublimation by thermal evaporation. Pentacene (97+% FLUKA Chemical Co., without further purification) was used as-received. During the deposition procedure of this active layer, a quartz oscillator and a shutter were used to control the deposition rate and reduce the influence of unstable vapor flux, respectively. On the other hand, the substrate was attached to the shadow mask to restrict the deposited area, reducing leakage current effectively. A 60-nm thick pentacene layer was thermally deposited in a vacuum evaporator as a channel with pressures below $6x10^{-6}$ Torr and the rate of deposition was controlled at 0.5 Å sec^{-1}. When finishing the growth of pentacene thin film, the substrate temperature was placed in the chamber to cool down for 10 minutes.

3.1.4 Source/Drain Electrode Deposition

After forming the active layer, gold (Au) metal through the patterned shadow mask was sequentially evaporated to construct the drain/source electrodes and the film thickness was ca. 35 nm. Besides, the deposition rate and pressure were maintained at 2.0–2.5 Å sec^{-1} and $3x10^{-6}$ Torr, respectively. Similarly, the completed devices were placed in the chamber to cool down for 20 minutes. The device had a channel length (L) and width (W) of 100 μm and 2 mm. A cross-section view of top-contact device structure is shown in Fig. 3.3.

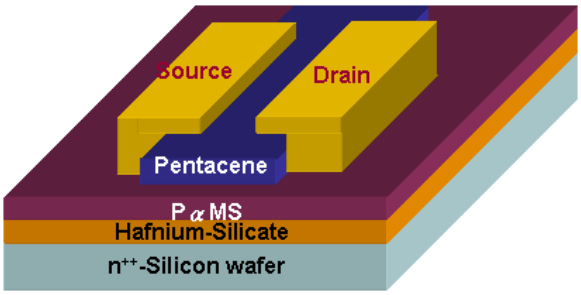


Fig. 3.3 An Schematic of the memory device with Hf-silicate dielectric on highly n-doped silicon wafer. The drain and source contacts were realized by evaporated gold.

3.2 Device Measurement System

3.2.1 Material Analysis

In our study, the Hf-silicate structure was mainly measured by the high resolution transmission electron microscopy (HRTEM) to examine plan-view images, surface morphology, and crystal structure. The physical thickness of Hf-silicate film and stack formation with TEM sample can be also observed by TEM cross-sectional graph. To explore TEM micrograph, this information about crystal structure by electron diffraction pattern (EDP) was understood. Furthermore, the X-ray Photoelectron Spectroscopy (XPS) technique was applied to understand the binding energy and crystallization characteristics.

3.2.2 Semiconductor Characterization System

The frequency (1 kHz) capacitance (C)–voltage (V) characteristics were measured by Agilent 4284A LCR meter. Besides, the sweeping bias conditions for our memory windows were investigated.

The electrical characteristics of our memory devices were measured with a Keithley 4200–SCS semiconductor parameter analyzer in the ambient air and in the dark. In the transfer characteristics measurement, the shift transfer curve operating in the saturation regime (drain-to-source V_{ds} = −10 V) was swept from gate-to-source V_{gs} = 20 V to −40 V. We performed various voltage stresses to observe charge carrier transfer dependence of memory windows. As for bias-stress measurement, the bias was stressed on the gate electrode at a fixed drain-to-source voltage in the dark or under illumination. After being stressed by bias

voltage, the number of trapped charges can be calculated.

At the same time, the device with modifying polymer layer was compared to untreated device and the conduction mechanism based on Hf-silicate dielectric can be explained. Details of operation method of our memory device were discussed in experimental results in Chapter 4.

3.2.3 Light-induced Installation and Method

An Oriel high-power supply of mercury (Hg)-arc lamp (200 W–500 W) was used as the light source and a monochromator was also used to isolate narrow portions of a light spectrum. With regard to light-induced installation, the motorized monochromator system orders gratings and slits light assembly separately. By connecting Oriel software and optical instruments through general purpose interface bus (GPIB) card in the computer, we were able to choose the particular channels of the monochromator and detector that controlled light wavelength and power meter. The semiconductor characterization system and light-induced installation were depicted in the Fig. 3.4

3.2.4 Experimental Instrument and Materials

Concerning to the detail information of the inorganic/organic materials and instruments, the following Table 3.1 exhibited the type for the specification clearly.

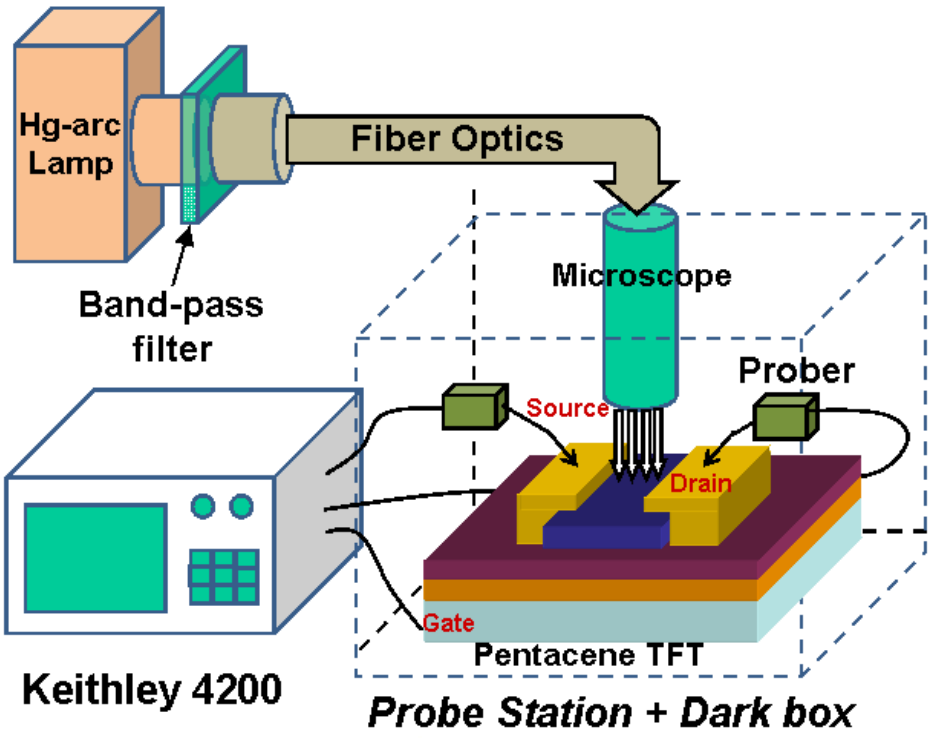


Fig. 3.4 Sketches of semiconductor characterization system and light-induced Installation.

Table 3.1 Chemicals and Instruments.

Name	Type
Poly(α-methylstyrene)	Sigma–Aldrich
Pentacene	Fluka
Spin Coater	Chemat Technology, KW-4A
Thermal Coater	ULVAC, CRTM-6000
Semiconductor Parameter Analyzer	Keithley–4200
LCR Meter	Agilent HP4156C
Power Supply	Mercury Arc Lamp (200 W–500 W)
Detector	Silicon photodiode
Monochromator	Oriel 74000

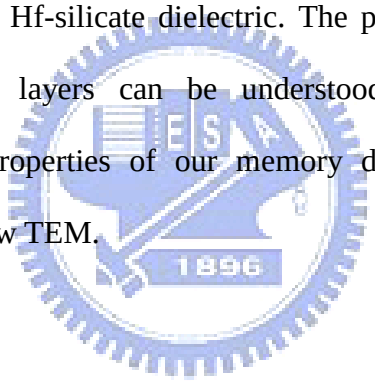
Chapter 4

Results and Discussions

4.1 Material Analysis of Hafnium-silicate Dielectric

4.1.1 Transmission Electron Microscope (TEM)

High resolution transmission electron microscopy (HRTEM) was used to examine the crystallographic structure of Hf-silicate dielectric. The physical thickness of the dielectric film and multi-component layers can be understood from the TEM cross-section. Additionally, architecture properties of our memory device were characterized by the powerful method of plan-view TEM.



- ***Cross-section***

In Fig. 4.1, we can clearly observe the cross-sectional view of TEM micrograph. Among these, platinum (Pt) strip was deposited as a protective layer to suffer the top surface from the ion-beam induced damage and unwanted milling during TEM sample preparation. Gold (Au) with good conductivity was used for preventing charge accumulation in insulator surface. The dielectric film with about 90-nm thick by metal-oxide chemical vapor deposition (MOCVD) was measured on n^{++}-doped silicon wafer.

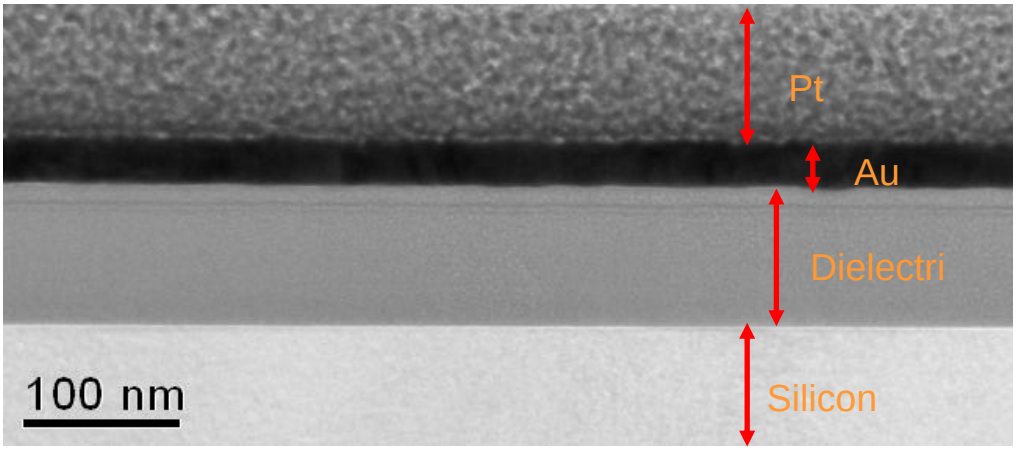


Fig. 4.1 TEM cross-section image from top to bottom is composed of platinum, aurum, dielectric (hafnium silicate), and n^{++}-doped silicon wafer.

➢ ***Plan-view***

In the literature, high-*k* materials had critical problems, including defects in the material which can lead to undesired charge transport through the dielectric and trapping-induced instabilities [34]. It was known that hafnium silicate was a satisfied material for memory behavior because of its chemical structure. Interfacial reactions and fractal formation were investigated by TEM plan-view observations. Furthermore, we focused the analysis of TEM plan-view on hafnium silicate near the interface of Au and dielectric, and thereby examined the reason of charge trapping which caused to the memory effect.

The material structure of dielectric film was analyzed that its phase separation was proved by TEM, shown in Fig. 4.2. The TEM microstructure in the film was composed of two chemical phase of nano-crystalline HfO_2 (dark) and amorphous silicate (bright), respectively (according to the result of XPS analysis). In fact, the defects of dangling bounds

or grain boundaries in the amorphous and polycrystalline devices acted as traps for the charge carriers. A memory device of hafnium silicate forming the phase-separated structure in our experiment can be regard as a significant element and impacted on charge trapping effect under the electrical filed. There was evident that Hf-silicate dielectric as a trapping layer was suitable for memory application [21, 22]. Therefore, the hysteresis phenomenon or memory effect had a dependency on trapping mechanism originating from the use of structural material.

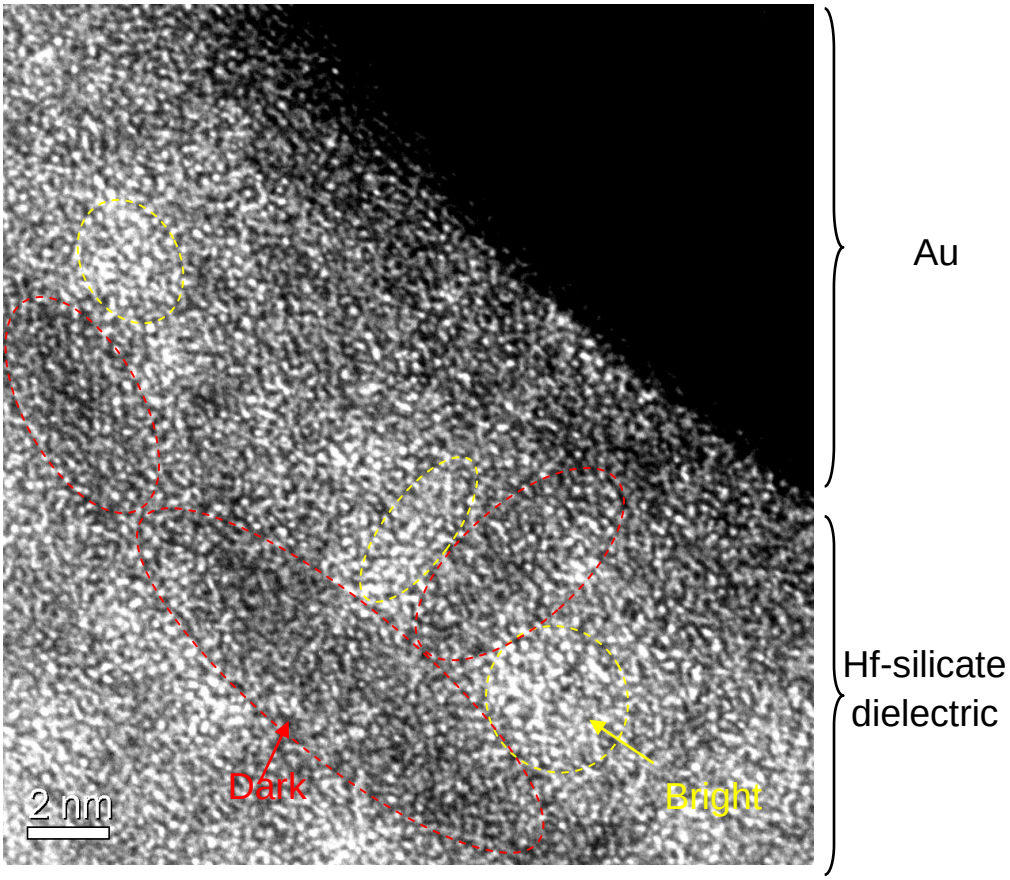


Figure 4.2 TEM plan view on silicate silicon film.

4.1.2 Electron Diffraction Pattern (EDP)

High-energy electron diffraction was most frequently applied to physical science and chemical analysis to study the crystal structure of solids. In particular, this experimental data was usually performed in TEM technology. To analyze the TEM micrograph by the measurement of electron diffraction pattern, information about the crystal structure was attained approximately. Fig. 4.3 exhibited electron diffraction pattern of the sample, which was a distribution of nano-crystalline HfO_2 in the dark region.

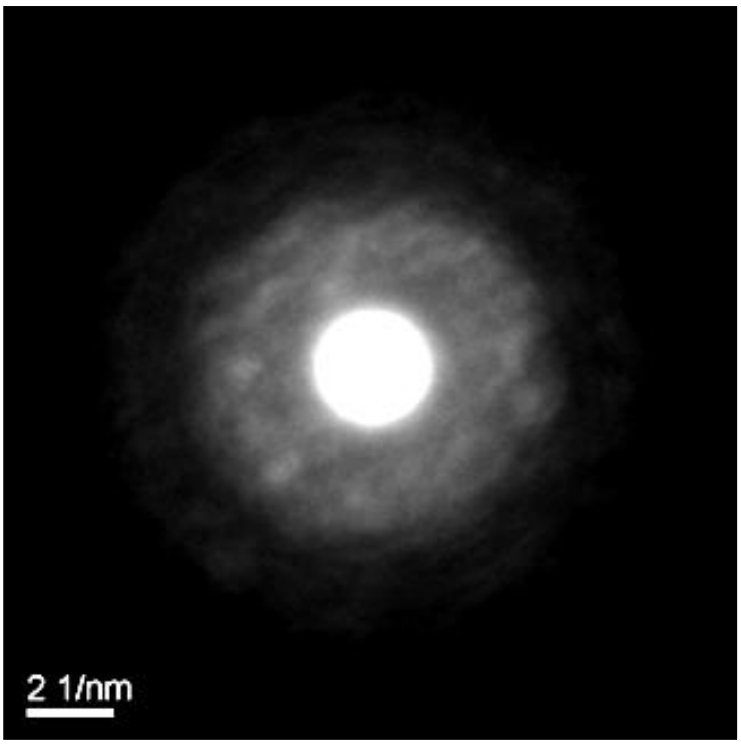


Figure 4.3 Diffraction pattern of Hf-silicate film.

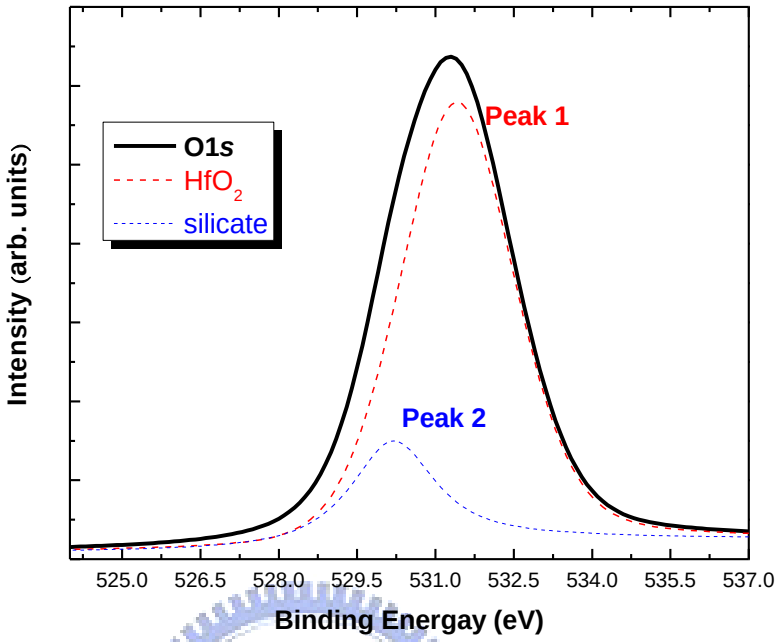
4.1.3 X-ray Photoelectron Spectroscopy (XPS)

Chemical composition of the prepared samples was verified by high-resolution X-ray photoelectron spectroscopy (XPS) measurement. The XPS peak fitting software program of XPSPEAK41 software can be able to combine different peaks of binding energy and analyze XPS data effectively. Generally speaking, all peaks were assigned 80% Gaussian and 20% Lorentzian character unless otherwise sated.

In Fig. 4.4, fitting of the XPS data was accomplished by XPSPEAK41 software and the binding energy component in the O 1*s* XPS showed slight silicate and HfO_2-rich crystal. According to XPS measurement, this spectrum authentically found out the atomic interaction and bounding element of hafnium silicate. On the basis of those spectra and database of XPS, the result indicated that one (peak 1) at 531.4 eV stood for the binding energy originating from hafnium and oxygen (Hf–O) bond. The other (peak 2) at 530.2 eV was interatomic binding between silicon and oxygen (Si–O) bond. The TEM picture (Fig. 4.2) and XPS result (Fig. 4.4(a)) clearly revealed hafnium oxide crystal and amorphous silicate which represented the darkness and brightness in TEM microstructure, respectively. Besides, Hf 4*f* XPS in Fig. 4.4 (b) revealed the binding energy at 17.9 eV (peak 3) and 19.7 eV (peak 4) originating from Hf–O bond. However, since there was not found in the appearance of Hf–Si bond with a binding energy of 14.6 eV in Hf 4*f* spectrum, we indicated that the interface between amorphous and crystalline was free of Hf-based silicide.

The surface stoichiometry of Hf-silicate film was studied by means of X-ray photoelectron spectroscopy (XPS). Based on the material analysis of hafnium silicate, the observation from the result of this work can reliably discern the material composition and crystal structures which significantly influence on the electrical measurement.

(a)



(b)

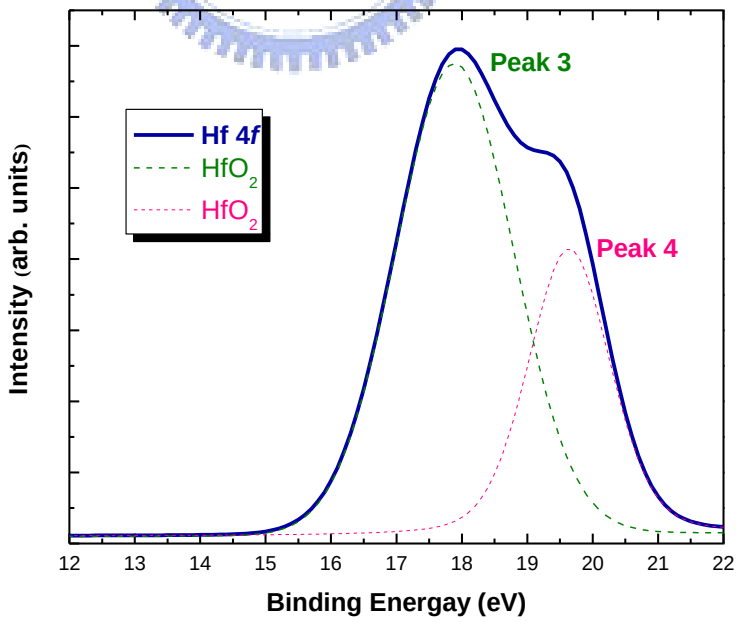


Fig. 4.4 Fitting results of XPS spectra on hafnium-silicate dielectric. (a) O 1*s* spectrum. (b) Hf 4*f* spectrum.

4.2 Electrical Characteristics on Hafnium-silicate Dielectric

4.2.1 Capacitance (*C*)–Voltage (*V*) Measurement

Capacitance (*C*)–voltage (*V*) characteristics were measured at the room temperature by Agilent 4284A LCR meter. During this experimental process, the operation frequency and alternating current (AC) signal level were set to maintain at 1 kHz and 25mV, respectively. Analysis of *C*-*V* curve used **m**etal-**p**entacene- **i**nsulator (Hf-silicate)-**s**ilicon (MPIS) structure as a function of the bias voltage. The memory effect or hysteresis phenomenon of this MIPS device was defined to be the flat-band voltage (V_{FB}) shift, always called "memory window". In Fig. 4.5, a counterclockwise hysteresis loop with a memory window was obtained from pentacene-based OTFTs on Hf-silicate dielectric when the bias voltage varied from a positive voltage to a negative voltage and then backed to the initial positive voltage (V_{gs}) with different voltage range.

Under the influence of a negative voltage for MIPS memory device, holes were easily injected into the pentacene layer from top Au electrode forming an abundance of holes carrier in pentacene film. Because the highest occupied molecular orbital (HOMO) of pentacene was close to the work function of Au, pentacene/Au was ohmic contact. The injection of holes, then, was promoted from pentacene into Hf-silicate dielectric and caused to hole trapping effect. The result in Fig. 4.5 was represented that there was little or mostly negligible memory window when the upward and downward scans were swept from gate voltage of 10V to −10 V. In contrast, a hysteresis window of capacitance curve with 18 V was measured from gate voltage of 40V to −40 V, thus indicating a lot of more holes trapping into insulator bulk and/or the interface with pentacene film. The hysteresis enlarged

by increasing the scan range and a very large hysteresis was achieved. As a result, the rise of voltage range conspicuously revealed hole trapping effect and had a larger memory window.

Besides, another critical influence of capacitance upon hole trapping densities was the different scan rate (or voltage step). Measurements of the capacitance versus bias voltage were shown at a frequency of 1 kHz for the different sweep rates of bias voltage swept from 20 V to −40 V. The adopted scan rates were 0.1, 0.5, 1.0, and 2.0 $Vsec^{-1}$ and similar hysteresis observations for memory window were obtained. As expected for gate dielectric with mobile charge carriers, hysteresis loops were evident by plots of the capacitance versus voltage bias for MPIS structure, as shown in Fig. 4.6. The hysteresis phenomena observed in the capacitance of the MPIS sample enlarged when decreasing the sweep rate of the bias voltage. The slowest scan of 0.1 $Vsec^{-1}$ displayed the largest hysteresis loop and it was expressed that switching speed of the residual dipoles in our dielectric layer was not high enough to entirely follow the high scan rate.

These observations exhibited the possibilities that the origins of memory characteristics were due to the presence of traps or defects. Altogether, a significant dependence of the hysteresis on the scan range and scan rate of gate bias were observed in our OTFTs with larger range V_{gs} scans or slower rate V_{gs} scans, producing a good deal of accumulated holes trapping and larger hysteresis.

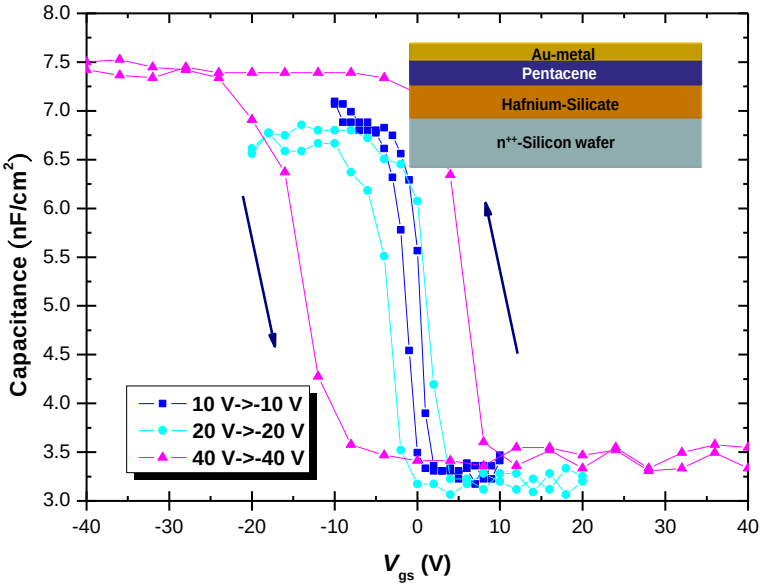


Fig. 4.5 Double sweeping *C-V* characteristics at at 1 kHz for different gate bias sweeps. (The inset shows schematically the device geometry: a cross-section graph of *C–V* measurement with the metal-pentacene-insulator–silicon structure, MPIS).

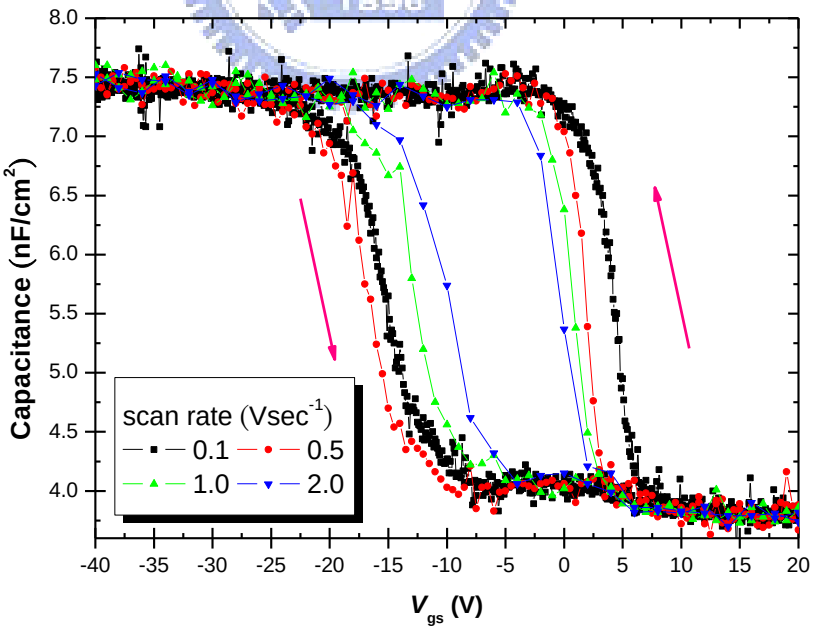


Fig. 4.6 Plots of *C-V* curve were measured from 20 to –40 V. The scan rates for MPIS device were 0.1, 0.5, 1.0, and 2.0 Vsec^{-1}.

4.2.2 Transfer Characteristics of Non-volatile Memory Device

In order to grasp the physical properties of the hafnium-silicate material, the characteristic curve was measured in the dark. The shifted transfer curve was swept from gate-to-source voltages V_{gs} = 20 to −40 V at 1 Volt step in the saturation regime (drain-to-source V_{ds} = −10 V) as illustrated in Fig. 4.7.

Concerning each set of experiment data, the second measurement was made under the same condition as the first measurement. The data showed repeated measurement of the transfer characteristic of pentacene-based OTFT, revealing unchanged carrier mobility (μ_{TFT}) and subthreshold slope (*S.S*) via the pulsed data. During the measurement of transfer charactristic, one manifestation of charge trapping within organic or/and the organic/polymer interface was a progressive shift of the threshold voltage (V_{th}) toward negative direction during successive bias swep on the gate electode.

In order to enhance the performance and improve electrical characteristics of pentacene-based memory device, PαMs-modified film was spin-coated onto the gate dielectric layer and arised the drain current densities. The results between Fig. 4.8 indicated that the satisfied OTFT behavior with modifying poly-α-methylstyrene (PαMs) polymeric layer did not drgrade the performance of the memory devices. In terms of the characterization equation (2.3), the μ_{TFT}, I_{on}/I_{off} ratio, and *S.S* obviously improved from 0.04 $cm^2V^{-1}sec^{-1}$ to 0.3 $cm^2V^{-1}sec^{-1}$, 10^4 to 10^6, and 3.8 to 1.07 V/decade compared with the vaules of untreated device, respectively.

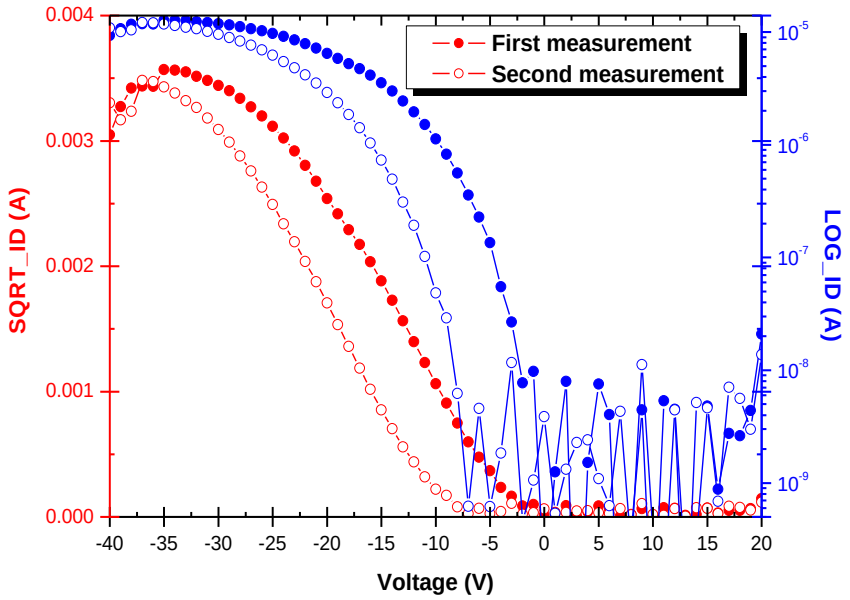


Fig. 4.7 Example of V_{th} shift upon sequential transfer curve measurement of pentacene-based OTFTs on an untread Hf-silicate surface (Pure device). The gate bias sweep direction was from positive to negative.

At the same time, a larger V_{th} shift of PαMs-treated device was more suitable for the application of memory device. The V_{th} was extracted by the intercept with V_{gs} axis (x-axis) of the maximum slope line from the I_{ds} versus V_{gs} at a drain voltage V_{ds} of −10 V. Regarding pronounced memory effects for PαMs-treated OFTFs, the additoinal PαMs polymer device had a larger shift of V_{th} of about 12 V; nevertheless, the pure device without modified layer on Hf-silicate surface was no significant observation about V_{th} shift of 7 V under the same gate bias conditions. From atomic force microscope (AFM) on pentance films (Fig.4.9 (a) and (b)), the morphology (Fig. 4.9 (b)) evidently showed that lager grain sizes and deeper grain boundaries improved the electricl performance and increasesd the probability of hole trapping in the semiconductor during charge transport process,

respectively. Besides, the number of trapped charges, Δn, can be determined from:

$$\Delta n = \frac{\Delta V_{th}}{e} C_i \qquad \textbf{(4.1)}$$

where e, ΔV_{th}, and C_i are the element charge, the shift of V_{th}, and the capacitance of the gate dielectric, respectively. Using the related equation (4.1), the trapped charges transferred from pentacene to PαMs, Δn, was calculated to be of order ca. 1.26×10^{12} cm^{-2}.

As a rule, memory effect for *p*-channel OTFT was mainly indentified the hysteresis mechanisms that included charge storage in the dielectric, slow polarization of gate dielectric, and hole trapping in the semiconductor. In our case, the reason for choice of treating device with PαMs was its weak dipolar polarization, symmetrical chemical structure, and the minimum influence of polarity effect, which can be slowly reoriented by an applied electric field [35]. On the other hand, it was proven that the memory effects did not originate from the dipole groups/molecules and rigid chains in polarized polymers, but mainly depended on the intrinsic structure of Hf-silicate dielectric resulting in charge trapping or hysteresis effect.

Further, the performance of PαMs-treated device was focused electrical bias sweeps on the analysis of charge-carrier concentration compared with the first and second measurement. The maximum slope lines of I_{ds} versus V_{gs} were estimated in Fig. 4.10. In the repeated measurement, Fig. 4.10 (a) showed that slope1 and slope2 of the transfer characteristics were the same value, respectively. So does Fig. 4.10 (b). It meant that carrier mobility and subthreshold slope of pentacene-based OTFTs scarcely changed via the pulsed measurement. Repeated sweep operations were done to ascertain that the shifts of V_{th} were trapping of charge in pre-existing traps, without creation of additional new traps during the operating process [38].

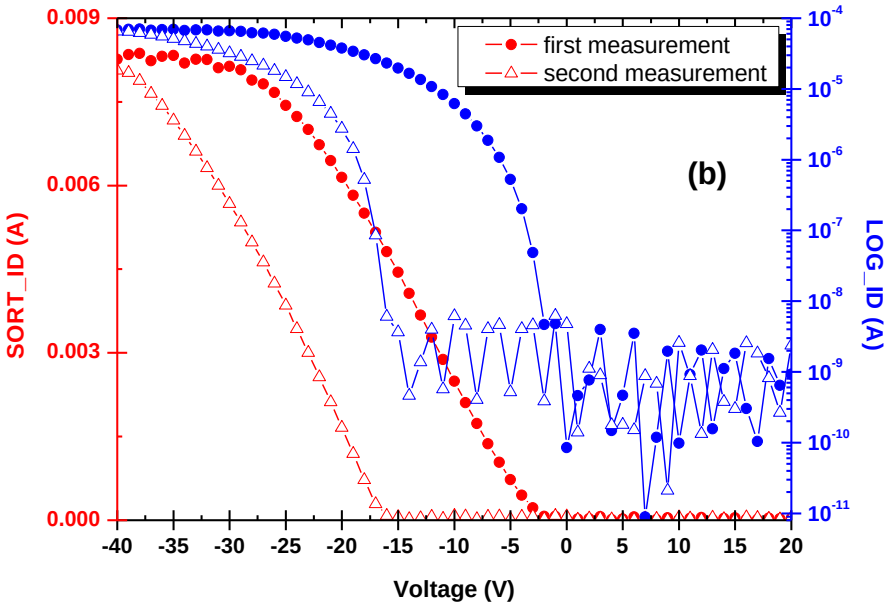
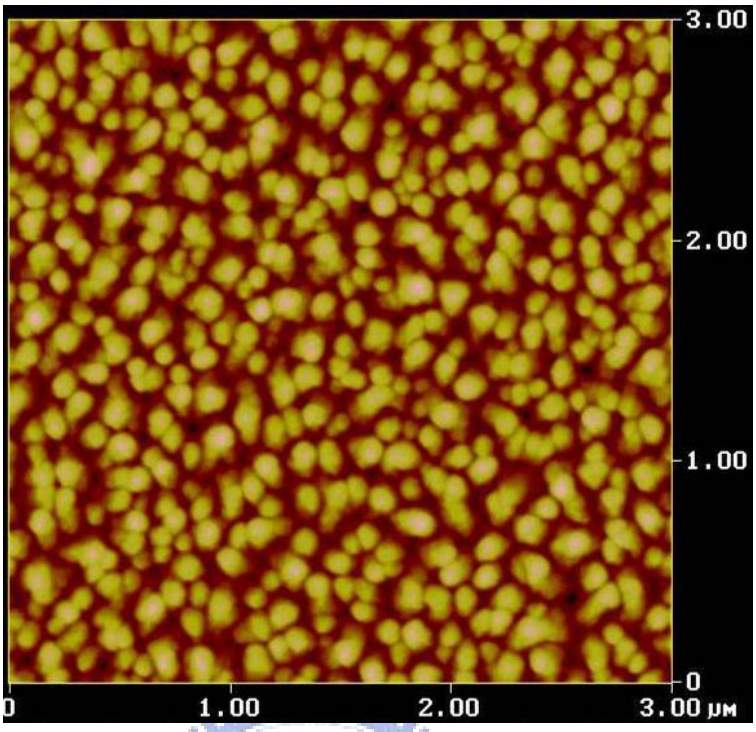


Fig. 4.8 Example of V_{th} shift of transfer characteristics with PαMS-modified layer on Hf-silicate dielectric was measured at the same scan condition compared to pure device.

(a)



(b)

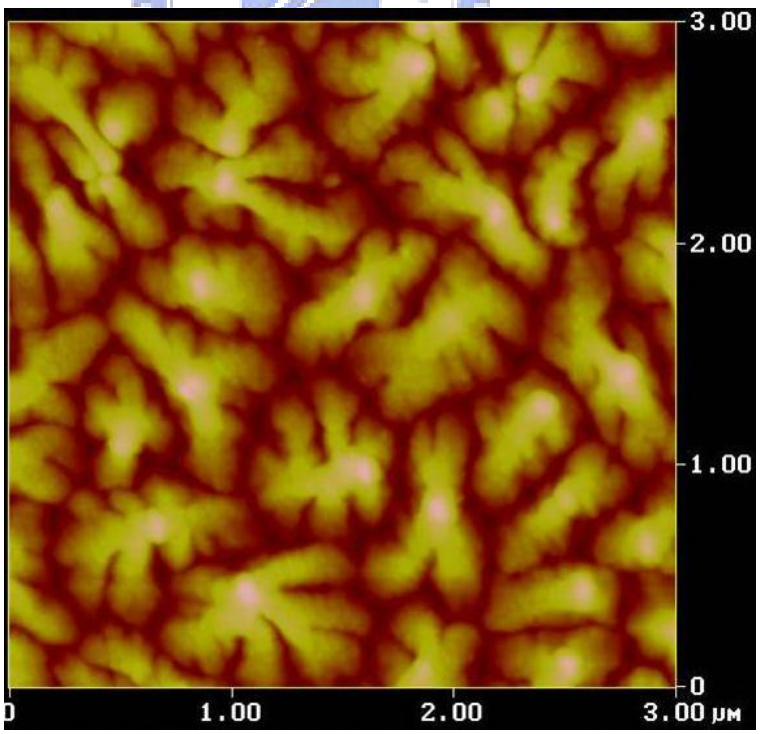
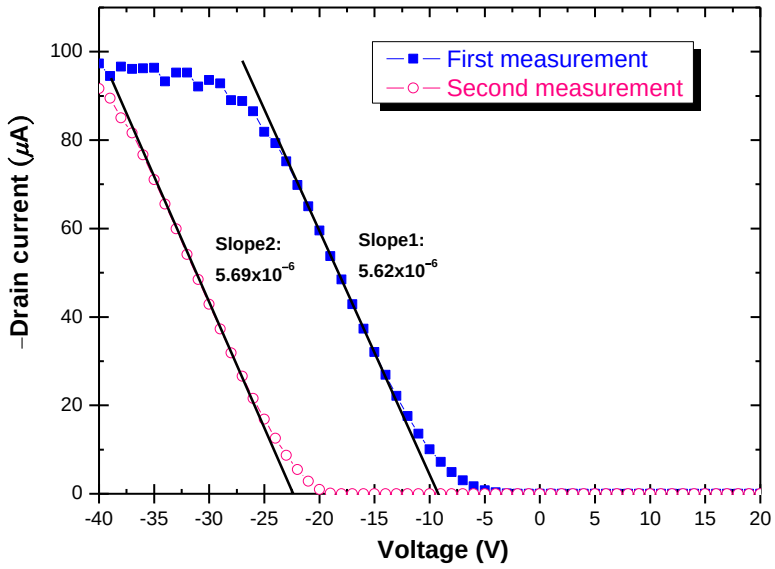


Fig. 4.9 AFM on pentacene film. (a) Pure device. (b) PαMs-modified device.

(a)



(b)

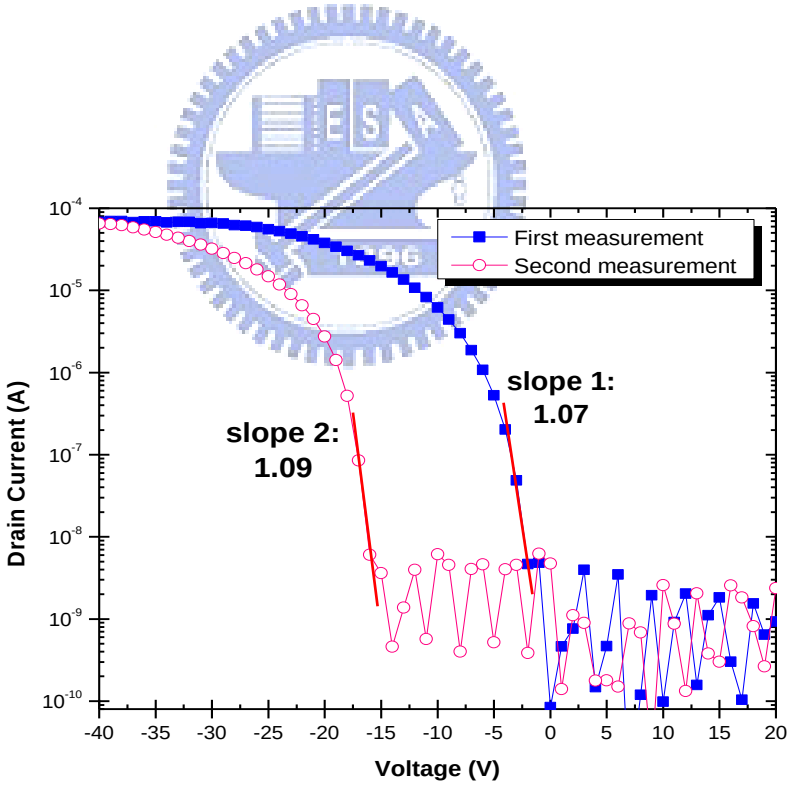


Fig. 4.10 The repeated transfer characteristics of pentacene-based OTFTs. The slope1 and slope2 stood for the maximum slope lines of I_{ds} versus V_{gs} drain at the first measurement and the second measurement, respectively. (a) Linear. (b) Semilogarithmic.

4.3 Retention Ability and Endurance Property

In general, charge-carrier transfer and trapping of organic semiconductor were obviously influenced by numerous parameters, namely, gate bias, stress time, arcitecture, etc. Memory effects in our memory device originated from switching behavior of the shifts of V_{th} with the mechanism of retention and endurance capacity.

In the view of charge retention behavior, the logarithmic longer time (t) decay of the drain current (I_{ds}) for both untreated and PαMs-modified device based on Hf-silicate substrate were measured at $V_{gs} = -10$ V and $V_{ds} = -10$ V **(*to read*)** at persistent stress time of ca. 1hr in a time of interval of 1 sec. As for the DC stress, we regarded as on-current state or high conductivity before applying high gate bias and then obtained off-current state or low conductivity **(*to read*)** after switching on the device at $V_{gs} = -30$ V and $V_{ds} = -10$ V for 1 min **(*to write*)**. The two states of non-volatile memory device differed in conductivity of several orders in the magnitude. In particular, the modified data (PαMs-treated device) showed excellent retention properties of the on and off ratio (I_{on}/I_{off}) of our memory OTFT to be of 1.2×10^5 (Fig. 4.12) better than the magnitude of 1.7×10^2 for the pure deivce (Fig. 4.11).

There was a notable difference on the memory effect of a pentacene OTFT between pure and PαMs-treated device on Hf-silicate surface. By constrast, pure device had no significant memory behavior of long-term charge retention, endurance performance, and data storage. Regarding the exprimential result with PaMs polymer layer, it was asserted that the enhancement of charge carrier densities effectively promoted to maintain decent memory stability, kept the off-current state well, and improved the electrical endurance characterization in spite of the measurement after the prolonged gate bias stress.

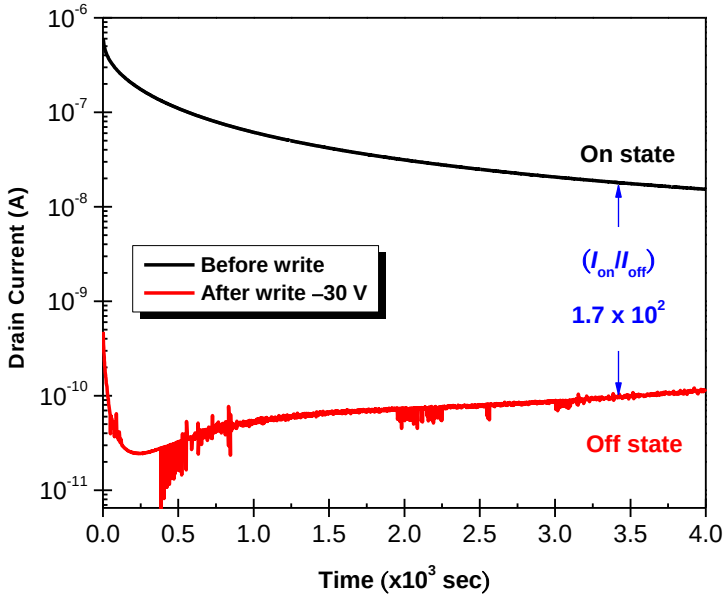


Fig. 4.11 Time dependence of the drain current of a pentacene memory TFT on Hf-silicate substrate was measured to read at $V_{ds} = -10$ V and $V_{gs} = -10$ V in a time interval of 1 sec.

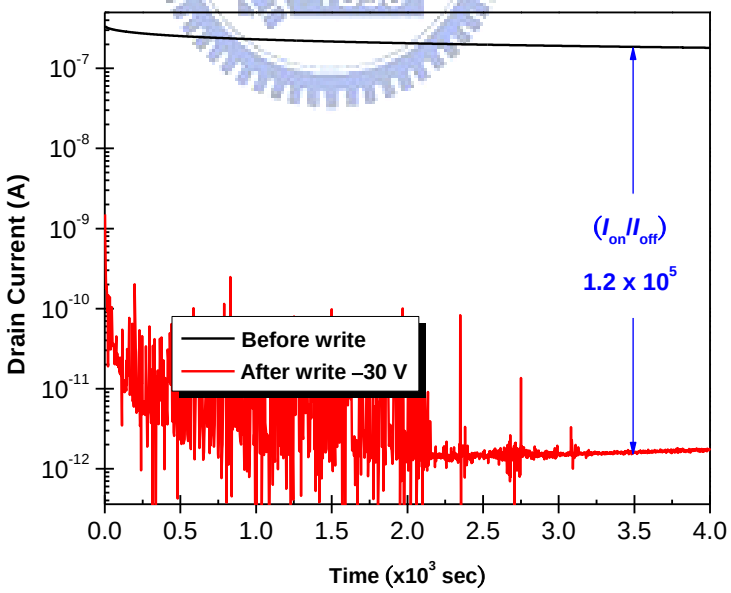


Fig. 4.12 Time dependence of the drain current of a pentacene memory TFT with PaMs-treated layer on the Hf-silicate sustrate was measured to read at $V_{ds} = -10$ V and $V_{gs} = -10$ V in a time interval of 1 sec.

The above results of the PαMs-modified device (Fig. 4.11) obviously had good endurance and long retention properities; and further, it was discussed at the different stress time. In order to verify the impact of hole trapping and current densities from changing stress condition, the time evolution of drain current was measured (to read) for the long-term measurement.

During DC stress, the off-state currents for our memory device with PαMs-modified substrate were obtained after the stress times for 1 sec and 10 sec at V_{gs} = –40 V and V_{ds} = –10 V (to write) as illustrated in Fig. 4.13. With V_{ds} held at –10 V, the hole traps were filled (trapped holes) when biased at high V_{gs} stress of –40 V, and subsequently few emptying at low gate bias of V_{gs} = –10 V, resulting in low-equilibrium mobile hole concentration in the conductance channel. Using the different stress time, on/off current ratio, current retention, and charge trapping effect were observed clearly. At gate bias of –10 V, on/off ratio of the stress time for 1 sec and 10 sec were $6x10^3$ and $1x10^6$, respectively. As expected, more trapped holes injected to the organic and/or organic/polymer interface with the longer stress time at the same bias on the gate electrode. At the start, both off-sate curves of 1 sec and 10 sec in this experimental data showed the same off-current state; nevertheless, the drain current versus stress time of them in this experimental result differed from the magnitude to be of two orders for the protracted time to approximately 1 hr.

More importantly, it was noteworthy that this retention properties and memory effects from a longer stress time led to more hole trapping, significantly influenced the endurance of our memory device, and then gained better endurance or data retention properties in the persistent time.

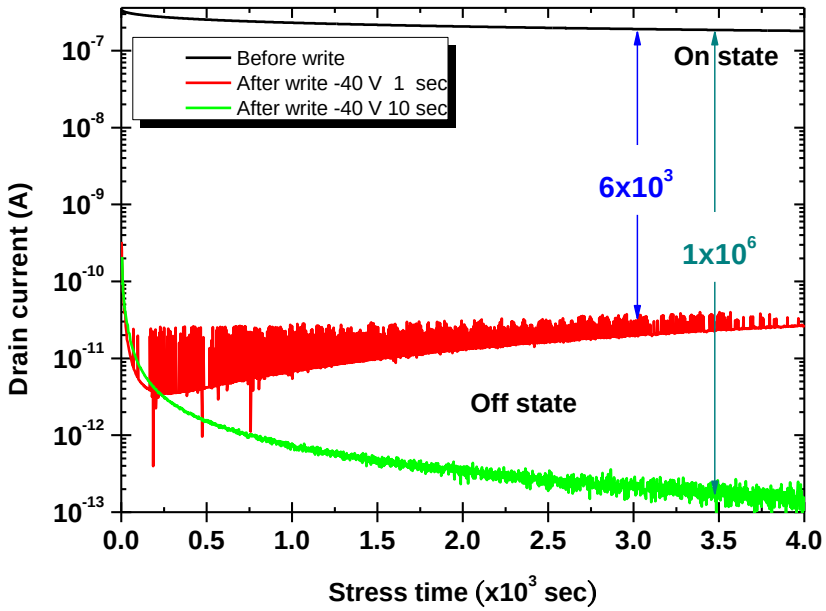


Fig. 4.13 The drain current versus stress time of pentacene-based OTFTs with PαMs-modified layer at V_{gs} = –10 V and V_{ds} = – 10 V. The DC stress curve was measured under various stress times at V_{gs} = –40 V and V_{ds} = – 10 V.

4.4 Memory Effect—PαMs-modified Device

In fact, an ideal memory device was qualified to the great property such as information storage. It should be understood that the memory effect for the observation about trapped hole and these devices avoiding light exposure and placing in ambient air were measured again after nine days, three weeks, one month, tow months, and four months respectively.

As shown in Fig. 4.14, it indicated that these recovered to the original states because of releasing parts of hole carriers from shallow traps at the interface between organic and

polymer layers. On the other hand, it was possible that a number of hole carriers holding in the deeper state in bulk dielectric led to maintain memory stability in despite of four months later. However, the absorbed water vapor in the ambient air increased with exposure time and degrades the OTFT performance with increasing the absorbed contents. In light of subthreshold swing and mobility of our memory device, the values of them slight varied initially, and then decayed evidently one month later.

It was known that the influence of trapping-detrapping process for charge transport on memory behavior was important. Thus, there was quite favorable for the application to non-volatile memory device due to hole traps, hysteresis effects, and shifts of V_{th}. In our work, the electrical characteristic showed an astounding memory behavior indeed.

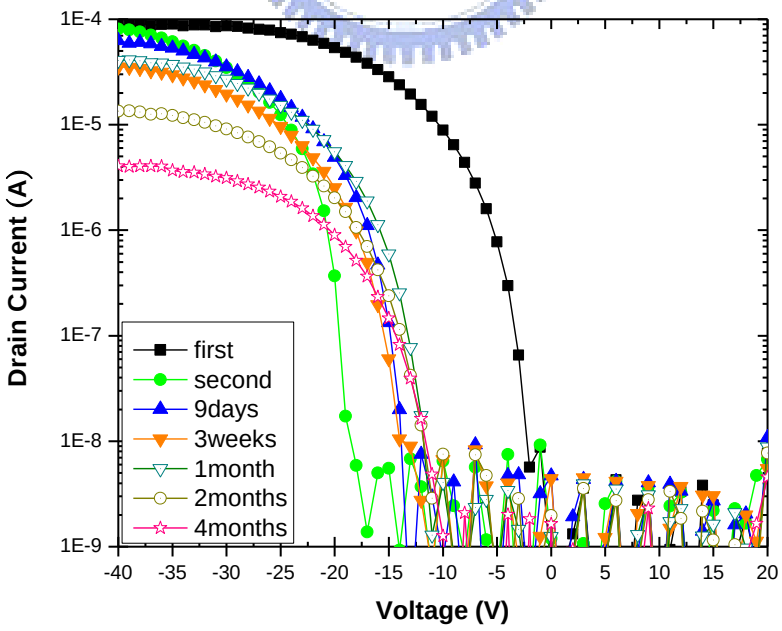


Fig.4.14 The observations of memory effect after nine days, three weeks, one month, tow months, and four months respectively.

4.5 Gate Bias Stress—PαMs-modified Device

4.5.1 Negative voltage

If the donor (hole traps) caused the hysteresis in the observed loop direction, this extracted field-effect mobility must be dependent on the magnitude of the gate voltage. The time dependence of V_{th} shift was clearly expressed by different bias stress on the gate electrode while keeping the source and drain terminals are grounded. After turning off gate bias, the shift of V_{th} was measured under the curve of current (I_{ds})–voltage (V_{gs}) characteristic at fixed $V_{ds} = -10$ V condition (to read). Through I_{ds}–V_{gs} measurement, the characteristics of bias-stress were able to monitor charge trapping effectively. In substance, a shift of V_{th} for this OTFT memory device was sensitive for hole trapping near the polymer/organic semiconductor interface at appropriate conditions. By controlling the value of gate bias and stress time, it was useful to examine a different range of memory window. As depicted in Fig. 4.15, measured shifts of V_{th} of pentacene OTFTs based on Hf-silicate substrate were stressed under gate voltage bias of –5 V, –10 V, –20 V, –30 V, and –40 V for the stress time of 10 sec, 60 sec, 180 sec, and 300 sec.

The data revealed that there was more pronounced shift of V_{th} or memory behavior when longer time and higher gate bias was stressed. With the rise of gate voltage, a progressive shift of V_{th} towards negative direction was likely to more charge trapping at the organic/polymer interface and/or in the organic. Particularly, a high gate bias at $V_{gs} = -40$ V was stressed; the bias-induced negative V_{th} shift was extremely conspicuous and then brought about a large memory window. No matter how long the time was stressed at low gate bias of $V_{gs} = -5$ V, the transfer characteristic curve was almost no negative shift of V_{th}.

Owing to the density of charge carrier was bare under low gate bias, this charge-trapping effect in our memory devices was not enough to cause the influence upon memory windows.

As analyzed above, the charge -trapping and -transfer effect for our memory device was extracted from a negative bias. Besides, Hf-silicate dielectrics impacted on the concentration of traps and corresponded to the memory behavior. In light of multiple trapping and release (MTR) model, at the low gate bias most of the holes (positive space charge) injected in the semiconductor were trapped into the localized state [27]. While increasing the negative gate bias, the Fermi level approached the valence band edge and more traps were filled. This model came from localized levels in the levels of the energy gap due to the defects acting as traps for the charge carriers.

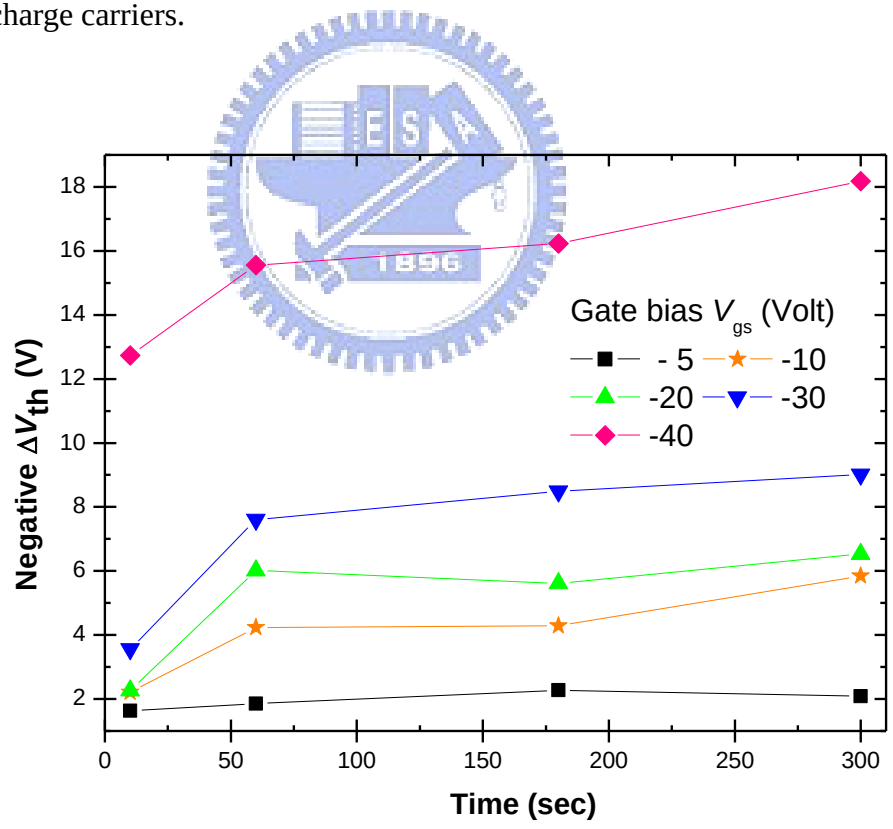


Fig. 4.15 The time dependence of measured shift of the subthreshold voltage of pentacene-based OTFTs on the hafnium-silicate substrate is stressed under different gate voltage bias at fixed V_{ds} = –10 V.

4.5.2 Positive voltage

The shift of threshold voltage and recovery kinetics under bias stress was also studied. In this memory device based on substrate with Hf-silicate dielectric, we accounted for the reversible method from the point of view of energy transfer to realize the operating mechanism at the same experimental condition to read.

Compared with negative bias (Fig. 4.15), a positive voltage bias (transverse electrical voltage field) stressed in the dark had merely no reversed shift of V_{th} despite at high gate bias. Fig. 4.16 showed that our memory device had the existence of potential barrier for charge carrier transfer and no accumulated charge in the depletion region (pentacene is a hole conductor) to explicate the absence of release effect. Using white light during the process of gate bias, the sample was illuminated for 10sec and 60 sec. A reversible shift of V_{th} and transfer characteristics curve was released especially for the stress time of 60 sec. After turning off a gate voltage with illumination, the transfer characteristics curve of pentacene-based OTFFs was measured (to read). This shift of reversible V_{th} of each curve was recorded and calculated from the second measurement for repeated scans. It was an indication that the subthreshold swing, the slope of I_{ds} versus V_{gs} (tranconductance) and, hence, the device mobility, was significantly enhanced, which represented the influence of reserved voltage under white light on the source/drain contact resistance and potential barrier.

Although the exact mechanism for the physics of photoinduced charge transfer in our OTFT memory device was not well understood yet, we proposed that the charge transfer and release model of energy barrier by photoinduced generation of light exposure facilitated the charge carrier transport between organic and polymeric layer. While the illumination with

5.5 mW/cm^2 was incident into pentacene-based OTFTs, light absorption in pentacene caused to the generation of charge carriers at the highest occupied molecular orbit (HOMO) and lowest unoccupied molecular orbit (LUMO) levels. The light-excited effect generated excess exciton formation (i.e., a bound electron-hole pair), photoinjection, dissociation, and free-carrier transfer in the film of pentacene. Therefore, the higher concentration of accumulated and mobile hole carriers caused to more drain current in the conductance channel. On the other hand, it was likely for some portions of the enhancement of charge carrier densities that detrapping of hole carrier stored shallowly in localized state in the organic (bulk or interface) was promoted because of lowering energy-barrier by the illumination of white light. As a result, these reasons for transfer and release of hole carriers were attributed by lower energy barrier and photoinduced recovery of the illumination effect.

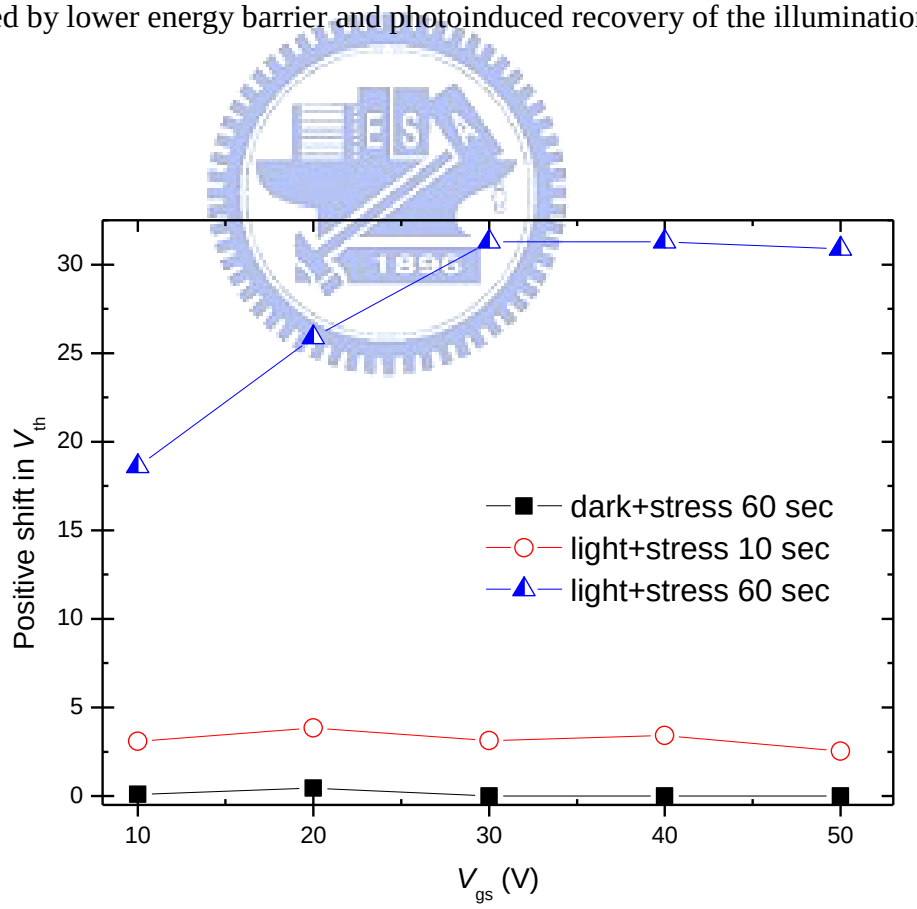


Fig. 4.16 Positive gate bias was stressed to memory device in the dark or light exposure during the process of gate bias stress.

4.6 Light-induced Recovery—PαMs-modified Device

4.6.1 Illumination with White Light

According to the above result by a useful method for light exposure, there was an essential element of this work to apply our non-volatile memory device that emphasized the strong influence of the effects of the illumination and the diagram of physical explanation was depicted schematically in Fig. 4.17. The cycle of stress and recovery by illumination was applied to the memory effects of pentacene-based OTFTs based on Hf-silicate substrate. This rewrite mechanism was supported by the experimental data obtained from the relaxation of photoexcited carriers. The following were four basic photocarrier generation processes of photoexcited species in solid organic polymers that can contribute to the enhancement of the carrier density in the conduction channel of the device [36]:

(1) exciton formation and subsequent diffusion to a dissociation site (electric field, defect, surface state, or impurity induced) into free carriers;

(2) direct, band-to-band excitation of electrons;

(3) photoinjection of carriers from the metal source/drain electrodes into the polymer;

(4) detrapping of carriers trapped in localized gap states in the polymer.

In order to explore the impact of light-induced effect, the device only subjected to light exposure without gate bias released at room temperature. For this case of our device, the carrier-generation process was through the main route from detrapping of carriers and exciton formation. As soon as exciton diffused and dissociated into electrons and holes, these charge carriers transport were influenced by the electric field from the applied the magnitude of V_{gs} and V_{ds}. As expressed in Fig. 4.18, this result of illumination measurement confirmed

that six min of illumination with 5.5 mW/cm^2 almost restored our device of V_{th} shift toward positive (reversible) direction and recover the curve in the initial state at the fixed V_{ds} of −10 V (to read). The photogenerated holes were collected at drain electrode. Furthermore, it was strongly believed that the charge transport mechanism of organic memory device was understood while storing in the dark or exposing under the light illumination.

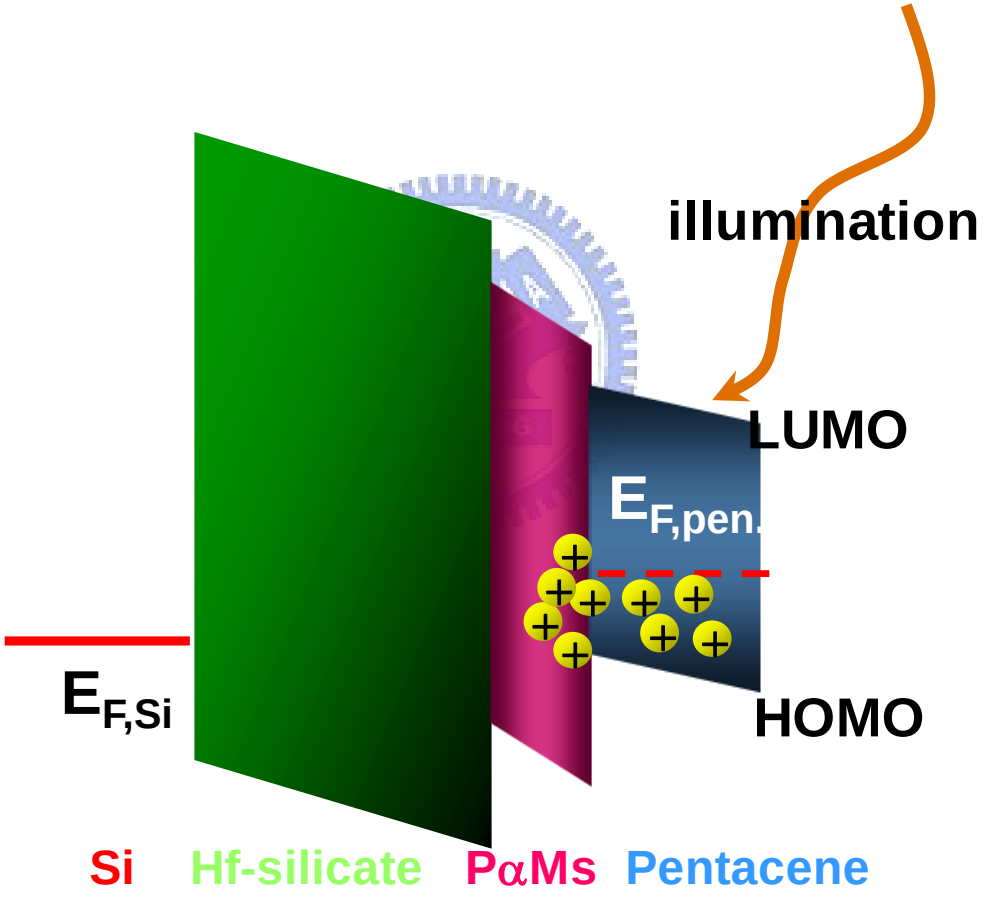


Fig. 4.17 Diagram of photoexcitation process for charge transport in the p-type channel.

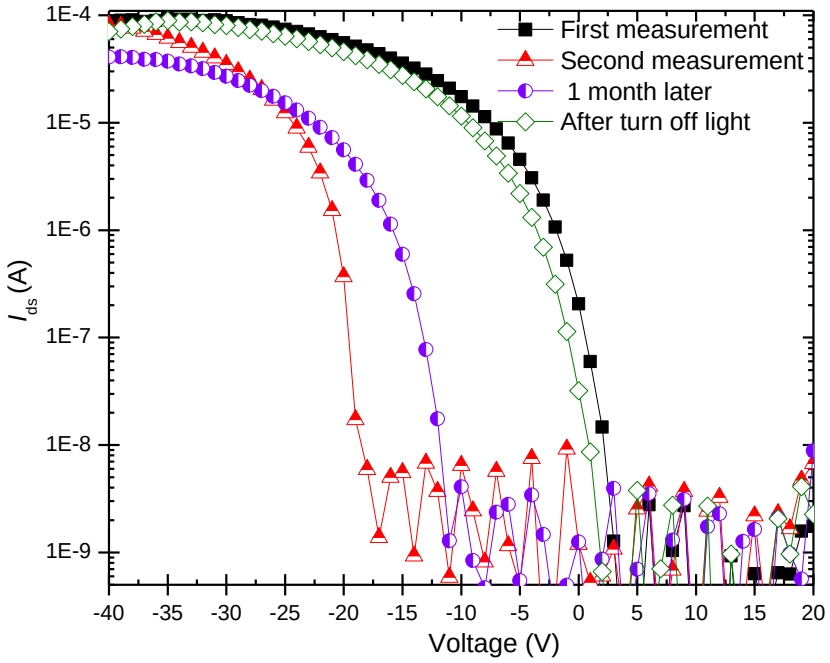


Fig. 4.18 The transfer characteristics of pentacene memory device at $V_{ds} = -10$ V were measured the first curve (filled squares), the second curve (half-up triangles) in the dark, and then again after turning off the white light for six min (open diamonds) or storing in the dark for one month (half-left circles).

4.6.2 Selective Absorption of Pentacene Film—PαMs-modified Device

To characterize the spectral response of pentacene, we discussed photoindued charge transfer and relaxation of mobile holes generation in the organic thin film transistor. As to this experiment under the illumination to pentacene film, measurements were made of the rate of recovery by illuminating OTFTs at different wavelengths and for the same exposure times. It was noteworthy that the speed of released charge of relaxation of the accumulated

and trapped charge depended on the kind of organic material.

In our study, light intensity was measured at the OTFTs location with a calibrated silicon photodiode. The fixed photon flux (Φ) at the wavelength (λ) was calculated as:

$$\Phi = \frac{P}{h\nu} \tag{4.2}$$

where h, P and ν are the Planck's constant, power intensity per unit second and light frequency, respectively [37]. Photons with wavelength ranging from 450 to 670 nm with the fixed flux of $1\text{x}10^{14}$ photons/cm^2 sec was incident into pentancene-based OTFTs and the illuminated time was 5 min. Light absorption in pentacene led to generation of charge carriers at the HOMO and LUMO levels. After the illumination, the characteristic curve was measured at the constant V_{ds} of −10 V. Given the same irradiated flux condition under the specific wavelength to organic memory device, the released charge was directly proportional to the absorption characteristics of pentacene. As shown in Fig. 4.19, this graph can be considered to be a combination of two multiple plots for one X-variable and double-different species of Y-variables. The plot for one X-axis was wavelength ranging from 425 to 700 nm. For double Y-axes, one (right Y-axis) was the absorption spectrum on a quartz substrate obtained from the polymer UV-Visible spectroscopy was measured by Perkin Elmer Lambda 650 and its strong absorption peak in pentacene was mainly at the wavelengths of 650–670 nm. The other (left Y-axis) was the released charge, Δn, shown by the reversible shift of V_{th} and equation (4.1).

This experimental result revealed that the absorption spectrum for pentancene energy band has no significant release phenomenon at the distribution of medium- and short-wavelength, but reacted very sensitive to the light illumination in the red region. The recovery rate was related to the absorption spectrum of organic materials the absorption

spectra of pentacene which abounded in charge carrier densities of hole-electron pairs that dissociated and increased the concentration of mobile holes of photoexcited species directly generated in the pentacene channel layer. Oppositely, it may be relatively more contribution at shorter wavelength radiation that the diffusion of photonexcited species were originated from the detrpped charge near the polymer/organic interface due to the lower directly absorption by the photoinjection process in the channel conductance of pentacene.

In this paper, an optical experiment for pentacene was carried out that selective material-absorbed distribution of the non-memory device with large concentration of hole transport (majority charge carrier) in the channel region compare to the influence from the bulk under photoexcitation. This evidence, therefore, obviously suggested that lager absorption ability and more the recovery rate of released charge for pentacene film at the particular wavelength was not only used effectively to form a high performance device with non-volatile and rewrite memory characteristics, but also take a reliable high-photosensitivity of pentacene to the application for organic thin film transistor and flat panel display.

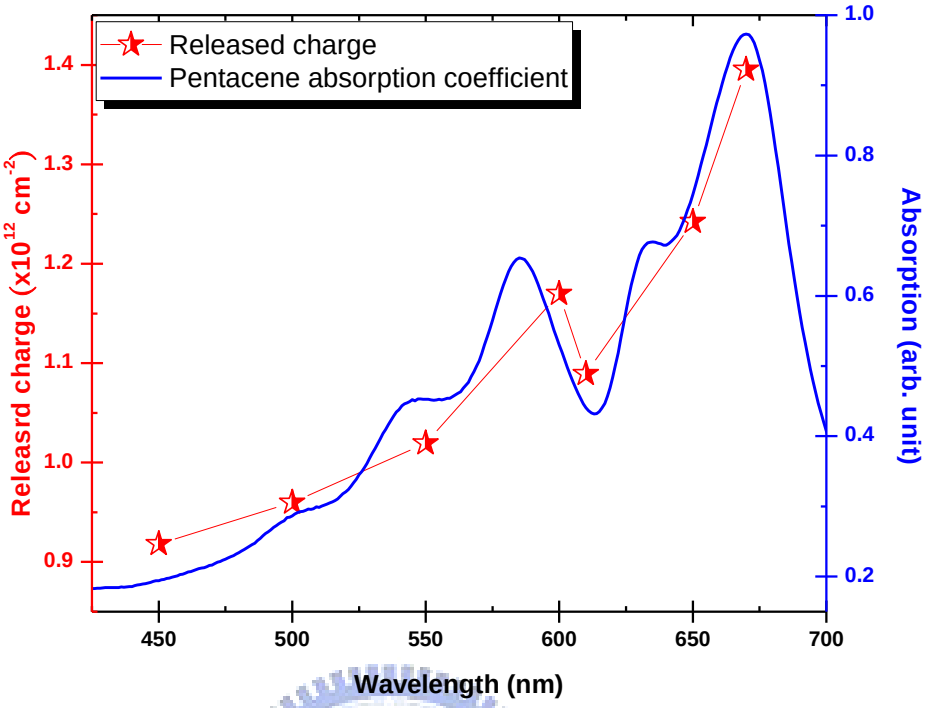


Fig. 4.19 The absorption spectrum for pentacene film (right Y-axis) and the photo-induced relaxation of released charge (left Y-axis) for PαMs-modified device in the fixed flux with the different wavelength.

4.6.3 Different intensity of illumination

The relaxation reaction was affected by the several parameters, such as the type of semiconductor, light intensity, irradiation wavelength, and exposure time, etc. The absorption spectrum for pentancene mainly appeared the absorbed peak in the distribution of red light. Therefore, we chose wavelength of the light irradiation respectively for 650 nm and 670 nm to investigate the released charge in a pentacene-based memory device as a function of

absorbed photo flux by controlling various illumination intensity and times.

It can be seen in Table 4.1 and Table 4.2 that the data of photon flux was distinctly calculated and obtained by equation (4.2) from the illuminated intensity of 28.5 μW, 50 μW, 71.4 μW, 114.3 μW, 100 μW, 142.8 μW and the irradiated time for 60 sec, 150 sec, 180 sec, 300 sec. As expressed in Fig. 4.20, result for the illumination experiment showed rather insensitive to both the insulator bulk and the organic/polymer interface, but was conspicuously related to the absorbed property of organic semiconductor material. As to the graphical analysis, the released charge depended approximately linear trend on the logarithmic increase of absorbed photon flux from light generation.

During the process of the photoinduced charge transfer, pentacene organic thin-film needed to absorb a higher order photon numbers and generated a constant amount of photoinduced charge transfer. As for our case, the difference between photon flux absorbed by polymer film and relaxation dynamics of charge carriers was approximately two orders of the magnitude. It was responsible for the difference of them that the photoexcited numbers of hole carriers were not completely absorbed by pentacene film.

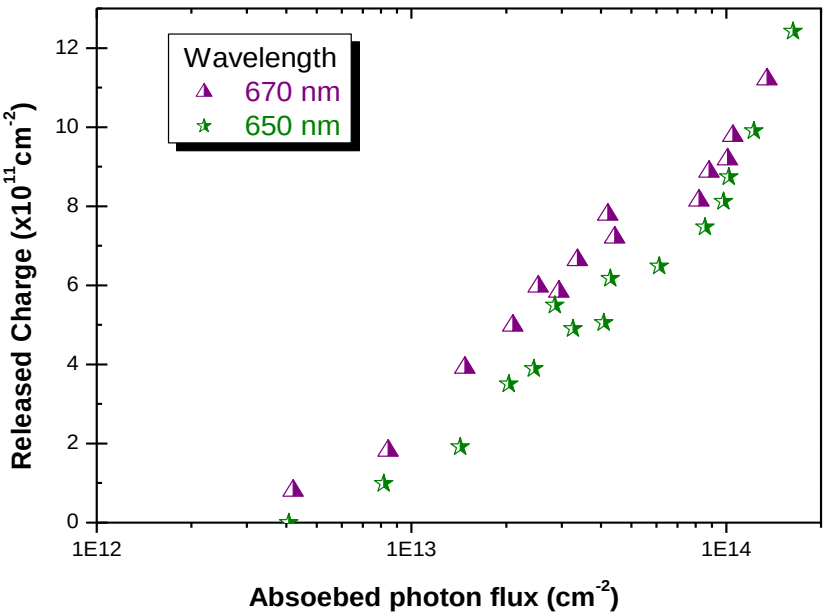


Fig. 4.20 Released charge in a pentacene TFT as absorbed photon flux in the dark was indicated at the particular wavelengths for 650 nm and 670 nm.

Table 4.1 The photon flux was calculated at particular exposure time and illumination intensity, at the irradiation wavelength of 670 nm.

670 nm (cm^{-2})	28.5 μW			71.4 μW			114.3 μW		
Illuminated Time (sec)	60	180	300	60	180	300	60	180	300
Flux (x 10^{13} cm^{-2})	0.84	2.53	2.9	2.1	6.3	10.51	3.36	10.1	16.83

670 nm (cm^{-2})	50 μW		100 μW		142.8 μW	
Illuminated Time (sec)	60	180	60	180	60	150
Flux (x10^{13} cm^{-2})	1.48	4.43	2.93	8.81	4.20	10.51

Table 4.2 The photon flux was calculated at particular exposure time and illumination intensity, at the irradiation wavelength of 650 nm.

650 nm (cm^{-2})	28.5 μW			71.4 μW			114.3 μW		
Illuminated time (sec)	60	180	300	60	180	300	60	180	300
Flux (x 10^{13} cm^{-2})	0.1	2.44	4.08	2.04	6.12	10.20	3.26	9.79	16.32

650 nm ($cm^{-2)}$	50 μW		100 μW		142.8 μW	
Illuminated Time (sec)	60	180	60	180	60	150
Flux (x 10^{13} cm^{-2})	1.42	4.28	2.85	8.57	4.08	10.20

Chapter 5

Conclusions

From the experimental process point of view, a satisfied memory device with PαMs-modified layer based on hafnium-silicate dielectric was the great advantage of rewrite ability and excellent enduring stability as well as its performance such as a high mobility, a large memory window, an obvious shift of V_{th}, and satisfied memory effect. Besides, hafnium silicate had an essential contribution to memory effect or charge trapping in this study. Due to its chemical structure with defects consisting of amorphous and crystalline phases, pre-existing traps resulted in charge carrier trapping effect during the transport process.

Using the *C-V* measurement, a significant dependence on the larger range V_{gs} scans or slower rate V_{gs} scans was observed. The electrical characteristics of bias-stress depending on the value of gate bias with different stress time controlled the magnitude of memory widow. On the other hand, the reversible and rewrite mechanism of non-volatile memory transistor were supported by the relaxation of photoexcited carriers. In our case, the strong influence of the illumination effects on the type of semiconductor was one of the most significant studies. There was evident that lager absorption ability at the particular wavelength (in the red region) led to a fast recovery rate of released charge for pentacene film, that is, the released charge was directly proportional to the absorption characteristics of pentacene. What is more, the released charge depended approximately linear trend on the logarithmic increase of absorbed photon flux from light generation.

In summary, these phenomena of our memory device on Hf-silicate dielectric with memory properties, a reliable high-photosensitivity of pentacene, relaxation of the illumination effect can pave the way for the applications of low-power consumption, flexible, lightweight, large-area, low-cost, data-storage, and rewrite device.

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