A Coupled-Simulation-and-Optimization Approach to Nanodevice Fabrication With Minimization of Electrical Characteristics Fluctuation

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***Abstract*—In this paper, a simulation-based optimization methodology for nanoscale complementary metal–oxide-semiconductor (CMOS) device fabrication is advanced. Fluctuation of electrical characteristics is simultaneously considered and minimized in the optimization procedure. Integration of device and process simulation is implemented to evaluate device performances, where the hybrid intelligent approach enables us to extract optimal recipes which are subject to targeted device specification. Production of CMOS devices now enters the technology node of 65 nm; therefore, random-dopant-induced characteristic fluctuation should be minimized when a set of fabrication parameters is suggested. Verification of the optimization methodology is tested and performed for the 65-nm CMOS device. Compared with realistic fabricated and measured data, this approach can achieve the device characteristics; e.g., for the explored 65-nm n-type MOS field effect transistor, the on-state current $>$0.35 mA/μm, the off-state current $<$ 1.5e $-$ 11 A/μm, and the threshold voltage $=$ 0.43 V. Meanwhile, it reduces the threshold voltage fluctuation ($\sigma_{\mathrm{vth}} \sim$ 0.017 V). This approach provides an alternative to accelerate the tuning of process parameters and benefits manufacturing of nanoscale CMOS devices.**

***Index Terms*—Characteristics fluctuation, complementary metal–oxide-semiconductor (CMOS) fabrication, device simulation, modeling, nanodevices, optimization, process recipe, process simulation, simulation, technology computer-aided (TCAD) design.**

I. Introduction

To pursue high-performance complementary metal–oxide–semiconductor (CMOS) devices for circuit designs, semiconductor manufacturing companies and foundries have to fabricate devices with different specifications. For example, logic, analog, and memory designs may require high threshold voltage, high speed, and low-power devices. Process and device engineers experimentally split the process conditions, such as channel and source/drain implantations, and fabricate test samples in developing the required process modules. This empirical approach directs the engineer to realistic devices. However, as dimensions of metal–oxide-semiconductor field effect transistors (MOSFETs) enter the sub-65-nm era [1]–[5], proper use of computer simulation-and-optimization-aided manufacturing techniques can reduce the number of test runs. Diverse simulation and optimization methods including statistical schemes have been reported in optimal fabrication of CMOS devices [3], [6]–[13], [19], [21]–[25]. The conventional methods use design of experiments (DOE) and external simulations to generate the response surface model (RSM) and then analyze the statistical variation of process parameters to perform optimization of manufacturing process; these methods have their advantages [7]–[10], [23]. Fluctuation of electrical characteristics is evident in sub-65-nm technology [12]–[15], [21], [22]. Therefore, it will be a crucial investigation if the random-dopant-induced characteristics fluctuation can be simultaneously minimized in the solution procedure of the simulation-based optimization methodology.

In this paper, we implement a technology computer-aided design (TCAD) simulation-based optimization methodology for nanoscale CMOS device fabrication. The TCAD simulation integrates two-dimensional (2-D) process simulation and device simulation. Threshold voltage fluctuations resulting from process variation effects and random dopant-induced effects should be taken into consideration and minimized in the optimization process. Here, we focus on the latter. The 2-D TCAD simulation is sequentially performed to evaluate device performance using the hybrid intelligent approach [17]–[20] which enables us to extract optimal recipes subject to designed device specifications. The hybrid optimization is mainly based on evolutionary computational techniques, numerical optimization methods, and expertise knowledge. The process simulation focuses on device structure and doping profile simulation. Next, the density-gradient-based drift-diffusion model is solved for device simulation [16], [26]–[28]. Finally, a quantum correction model is solved by perturbation and monotone iterative methods to estimate the random dopant-induced fluctuations [11], [12], [21], [22]. The developed prototype environment not only can integrate in-house developed simulation programs, but also provides a flexible interface to well-known TCAD software. Verification of the proposed computational methodology is performed on 65-nm CMOS devices. For a 65-nm n-type MOSFET, the on-state current $>$0.35 mA/μm, the off-state current $<$ 1.5e $-$ 11 A/μm, the threshold voltage $=$ 0.43 V, and

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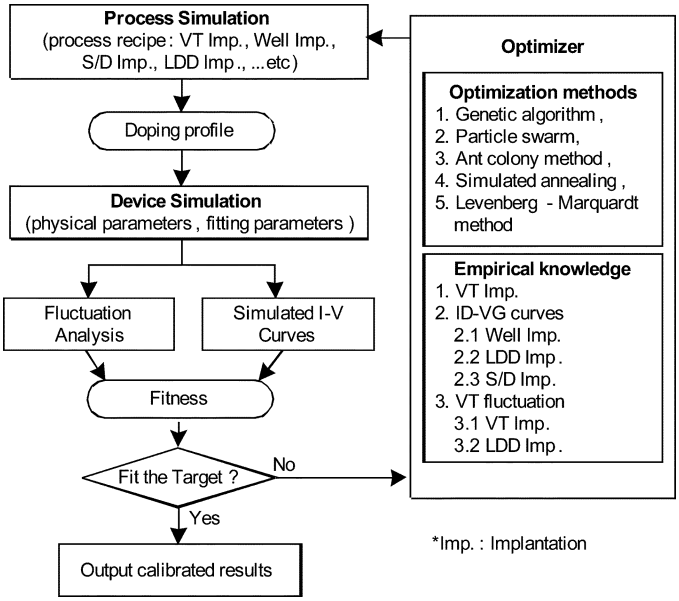

Fig. 1. Working flow of implement methodology for reverse modeling problem in tuning fabrication parameters.

the threshold voltage fluctuation $\sigma_{\rm vth} \sim 0.017$ V are adopted as targets to be achieved. Optimized recipes are automatically suggested then compared with realistic fabricated and measured data until results meet the device performance within a specified tolerance.

This paper is organized as follows. In Section II, we briefly describe the proposed coupled simulation-optimization methodology and architecture of the implemented prototype. In Section III, the experimental and theoretical calculated results are reported to show the robustness of the method. Finally, we draw conclusions and suggest future work.

II. Simulation-Optimization Methodology

As shown in Fig. 1, a flowchart of the simulation-based optimization methodology illustrates the sequence of process and device simulations [1], [2], [11], [16], [24]–[28], fluctuation analysis [12], [13], [21], [22], and a hybrid optimization kernel [17]–[20]. For a given device specification, such as the on- and off-state currents and the threshold voltage, the simulator searches out a set of optimal settings to fit the prescribed target and then estimates the variation of the threshold voltage accordingly. Starting from an initial process recipe, we apply 2-D process simulation to generate the corresponding device structure and doping profile. Together with device parameters and physical models, they are used in the 2-D device simulation to obtain the preliminary results. If we include the random-dopant-induced characteristics fluctuation, we pass the physical results to perform the fluctuation analysis by solving the quantum correction model with perturbation and monotone iterative methods. At the same time, we calculate the error between the simulated result and the target to get the fitness (or the cost function). When the stopping tolerance is met, the solution procedure is terminated and the final results are output. Otherwise, the hybrid optimization is enabled to do the evolutionary searching process with respect to several specified constraints. The refined fabrication conditions as well as the physical model parameters are then used as inputs to the process simulation and device simulation is repeated. The iteration between the TCAD simulation and optimization is terminated when the simulated device's specification and the correspondingly computed tolerance of characteristic fluctuation meet the target. We note that to automatically search for the optimal recipes for device fabrication, the problem is now treated as a reverse modeling problem, which is a multidimensional minimization problem. It minimizes the errors between the specified (or measured) physical (and electrical) characteristics and the simulated results. The dimension of the optimization problem depends upon how many parameters are to be optimized; in general, it is about 30 process and device parameters. For ultra-small devices, 3-D simulation should be considered to account for the geometry effect.

The developed evolutionary system for the semiconductor device fabrication contains two independent parts, the evolutionary core kernel and the external simulation programs, shown in Fig. 1. The former part mainly uses evolutionary algorithms, such as the genetic algorithm and the particle swarm method incorporated with other numerical optimization techniques [19]. The external programs consist of the codes for device simulation and process simulation which can be replaced with any existing TCAD software. During the iterative procedure, the optimizer computes the fitness score for each setting (i.e., the process recipe) through a fitness function. The fitness function measures the error between simulated and target characteristics and the fluctuation of threshold voltage. The fitness function used in this paper is

$$\text{fitness} \equiv \text{weight}_{\rm ID}\left(\frac{\log(I_D)-\log\left(I_D^{\rm target}\right)}{\log(I_D^{\rm target})}\right) + \text{weight}_{\sigma\rm vth}\left(\frac{\sigma_{\rm vth}}{V_T}\right) \quad (1)$$

where I_D means the simulated data, the $I_D^{\rm target}$ is the specified target to be achieved, and $\sigma_{\rm vth}$ is the fluctuation of the threshold voltage (V_T). $\text{weight}_{\rm ID}$ and $\text{weight}_{\sigma\rm vth}$ are the weighted value for the I-V curves and $\sigma_{\rm vth}$, respectively. In our paper, we set $\text{weight}_{\rm ID} = \text{weight}_{\sigma\rm vth} = 1$, which means that the device performance and the fluctuation of the threshold voltage have the same weight. However, it can be adjusted according to different design purposes. To retrieve the simulated physical characteristics including I-V curves, the optimizer sends the setting to be evaluated to the external process and device simulation programs, and the external programs perform the simulations and generate the I-V curves. Physical-based empirical knowledge embedded in the evolutionary core kernel defines the relationship of the parameters and the device characteristics. According to engineering observation, parameters to be optimized are grouped into two categories, one is process related and the other is device related. The former part plays the important role of determining a device's preliminary characteristics. The I-V curves are physically divided into the linear, the off-state, and the saturation regions. We first optimize process-related parameters by minimizing errors between simulation and target in the linear and off-state regions. To achieve error minimization, parameters relating to implantations of $\rm V_T$, well, lightly doped

drain (LDD), and source/drain are first computed simultaneously, allowing an accurate threshold voltage to be obtained. In the evolutionary part of the procedure, parameters coupled to band-to-band tunneling and saturation velocity are taken into consideration [16], [29]–[31]. Otherwise, parameters may possess unreasonable physical meanings, and then the optimization becomes meaningless. By minimizing errors in the saturation and off-state regions, device-related parameters are optimized with respect to the mobility model, band-to-band tunneling model, and saturation velocity [16], [29]–[31]. To reduce the fluctuation of the threshold voltage, we focus on $\mathrm{V_T}$ and LDD implantations. Finally, if necessary, the linear, off-state, and saturation regions are simultaneously optimized one more time. The optimization is terminated when errors are minimized for all I-V curves. We note that the device performance, in particular, for $\mathrm{V_T}$ and the linear region of I-V curves, is significantly dominated by process-related parameters. Therefore, we put emphasis on the linear region and then the saturation region of I-V curves in the optimization procedure. During the optimization procedure, once a larger error within a certain region of I-V curves is observed, an empirical rule is employed to destroy the evolution, which may result in different mutation and is useful in the iteration loop of simulation and optimization.

For device-related parameters, the mobility models used in the device simulation, according to Mathiessen's rule [16], consist of the following three parts. 1) The surface contribution due to acoustic phonon scattering

$$\mu_{\mathrm{surf\_aps}} = \frac{B}{E} + \frac{C(N_i/N_0)^{\lambda}}{E^{1/3}(T/T_0)^{K}} \tag{2}$$

where $N_i = N_A + N_D, T_0 = 300\,\mathrm{K}$ and E is the transverse electric field normal to the interface of semiconductor and insulator. 2) The contribution attributed to surface roughness scattering

$$\mu_{\mathrm{surf\_aps}} = \left(\frac{(E/E_{\mathrm{ref}})^{\Xi}}{\delta} + \frac{E^3}{\eta}\right)^{-1} \tag{3}$$

where

$$\Xi = A + \frac{\alpha \cdot (n+p)N^{v}_{\mathrm{ref}}}{(N_i + N_1)} \tag{4}$$

and E_{ref} is a reference electric field, N_{ref} is a reference doping concentration. 3) The bulk mobility

$$\mu_{\mathrm{bulk}} = \mu_L \left(\frac{T}{T_0}\right)^{-\zeta} \tag{5}$$

where μ_L is the mobility due to bulk phonon scattering and T is lattice temperature. For the saturation velocity, we use

$$V_{\mathrm{sat}} = V_{\mathrm{sat0}} \left(\frac{T}{T_0}\right)^{V_{\mathrm{sat1}}}. \tag{6}$$

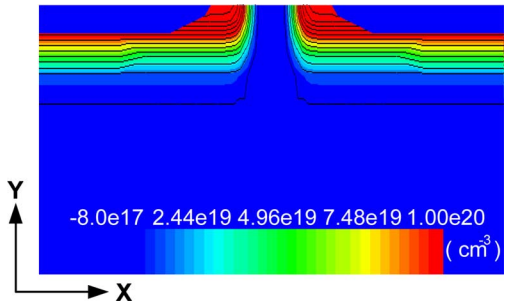

Fig. 2. Initial doping profile for explored 65-nm N-MOSFET.

Details of the mobility models and coefficients are described in [16], [29], and [30]. For the band-to-band tunneling, we used the model reported in [31]. Generally, the number of parameters to be optimized depends upon the device parameters selected in the TCAD simulation and the process-related parameters that directly affect the device structure and doping profile. From empirical knowledge, we especially investigate the parameters for $\mathrm{V_T}$, LDD, and well implantations due to their significance in the threshold voltage and the linear region of the I-V curves. Moreover, the $\mathrm{V_T}$ and LDD implantations are crucial when considering the random-dopant-induced characteristics fluctuation. We also adjust the mobility and saturation velocity parameters in the device simulation for fine-tuning the I-V curves. This study is mainly based upon our recent work on a unified optimization framework (UOF), where the developed open-source project UOF is available in the public domain [32]–[34].

III. Results and Discussion

In this section, the optimized parameters for on-target fabrication of the 65-nm CMOS devices will be investigated. For the sake of simplicity, we focus on the results of the 65-nm N-MOSFET. The device characteristics and the fluctuation tolerance of the threshold voltage are summarized in column 2 of Table I. In this investigation, the on- and off-state currents, the threshold voltage as well as the device's fluctuation tolerance have been optimized simultaneously. With these four physical constraints, the coupled simulation and optimization methodology was self-consistently performed with the specified fitness function. The initial doping profile used in the optimization procedure is shown in Fig. 2. The simulated doping of the optimized device, both with and without the reduction of the threshold voltage fluctuation, are shown in Fig. 3(a) and (b), respectively. Fig. 4 shows a 1-D section in the center of the device channel of the 2-D doping profile distributions shown in Figs. 2 and 3. It can be observed that the minimization of the threshold voltage fluctuation (dotted line) results in a lower doping level compared with the optimization without consideration (dashed line). This optimization automatically achieved the target parameters and confirms the studies reported in [13], [21], and [22]. Fig. 5 shows the horizontal doping profile 2 nm below the channel surface between the source and drain. Together with the results, shown in Fig. 4, the higher doping level along the channel for the device, when the threshold voltage fluctuations were also optimized, maintains the same device characteristics as the one where dopant fluctuations were not considered.

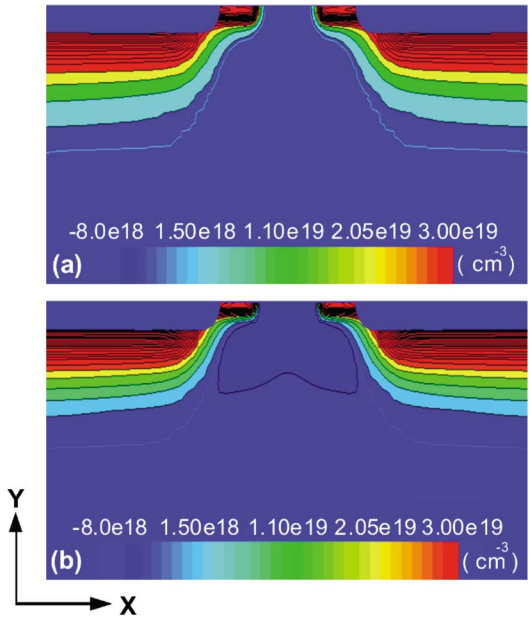

Fig. 3. Optimized 65-nm N-MOSFET doping profile for device (a) without and (b) with considering minimization of threshold voltage fluctuation.

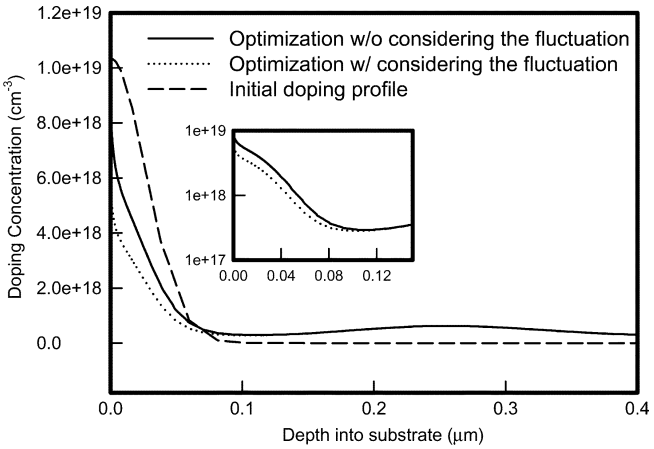

Fig. 4. Optimized doping profiles from channel surface deep into substrate. The 1-section is located at center of device channel ($x = 0$).

The results of the optimized 65-nm N-MOSFET are summarized in Table I. If the threshold voltage fluctuation minimization is not be activated in the optimization, there is a 6.7% threshold voltage fluctuation, which significantly shifts the process away from the design window (3.89%). The band profiles for the devices in the on- and off-states are shown in Figs. 6(a) and 7(a) for both of the optimization cases. The optimization without minimization of the threshold voltage fluctuation has a little bit lower band edge than its counterpart due to a higher doping level [Figs. 6(a) and 7(a)]. Figs. 6(b) and 7(b) once again show the horizontal profile along channel for both optimization cases. For the optimization without minimization of fluctuation, both the on- and off-state bands (2 nm below the channel surface) are lower than that the optimization minimizing the fluctuations. Both the specified target and the optimized results are shown in Fig. 8. The results with and without considering the threshold voltage fluctuation are very close to the specified target. Nevertheless, the strategy of including the reduction of threshold voltage fluctuation successfully reduced

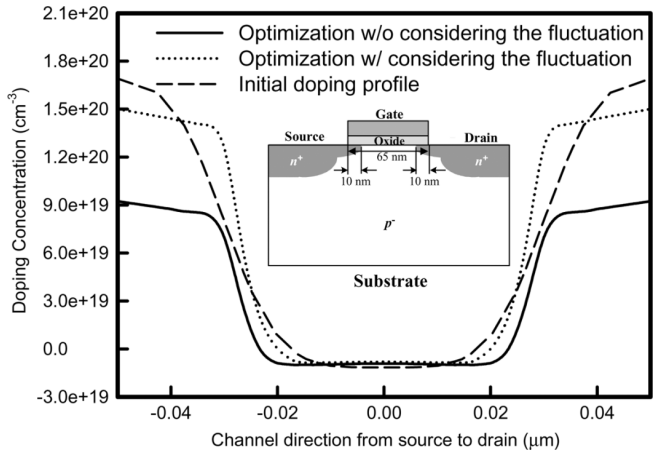

Fig. 5. Doping profile from source to drain along channel direction 2 nm below interface between gate oxide and silicon substrate. Inset of figure shows structure of optimized 65-nm N-MOSFET.

TABLE I
COMPARISON LIST OF ACHIEVED RESULTS WITH RESPECT TO TWO DIFFERENT EXTRACTIONS. TARGET SPECIFICATION IS ADOPTED FROM REALISTIC FABRICATED AND MEASURED DATA

	Target to be achieved	Result without σ_{vth} reduction	Result with σ_{vth} reduction
Ion (mA/μm)	> 0.35	0.35	0.39
Ioff (A/μm)	< 1.5e-11	1.05e-11	1.13e-11
V_{th} (V)	~0.436	0.442	0.432
σ_{vth} (V)	~0.017	0.03	0.014
σ_{vth}/V_{th} (%)	3.89	6.78	3.24

the threshold voltage fluctuation and is shown in Table I. A list of the process recipe and device parameters used for simulation, and the extracted parameters, with and without fluctuation reduction, are summarized in Table II. It can be noted that there is a major difference between the core V_T implantation and the result with and without σ_{Vth} reduction. To verify the efficiency of the proposed method, three examinations are performed on our PC-based Linux cluster system with 16 CPUs [24], [25]. The fitness score versus the number of evolutionary generations is shown in Fig. 9. For the given target, it shows that the methodology with simultaneously considering the parameters of the process and device physics provides better computational efficiency.

IV. CONCLUSION

A coupled TCAD-simulation-based optimization algorithm has been implemented and applied to fabrication optimization of the 65-nm CMOS devices. Fluctuations in the solution procedure are induced, which enables us to search out the optimum recipe for minimization of the threshold voltage fluctuation. Reducing the doping level in the device channel suppresses the threshold voltage fluctuation; but, it also modifies the device performance. This difficulty is one of the important issues in developing reliable fabrication technique in semiconductor foundries. In this example, both the threshold voltage implant and LDD implant are automatically optimized at the same time. Our investigation shows that to meet the goal discussed in Table I of Section III, the LDD dopant should be increased in the source and drain, and the concentration of the threshold

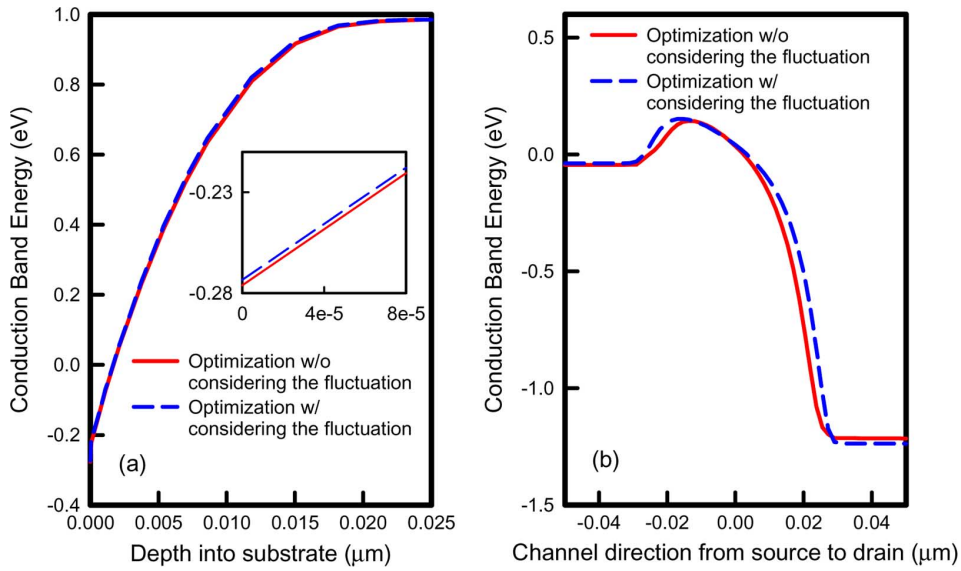

Fig. 6. Plots of band profile for optimization with and without considering threshold voltage fluctuation under on-state. (a) Surface to the substrate. (b) Along channel direction from source to the drain, which is about 2 nm below channel surface.

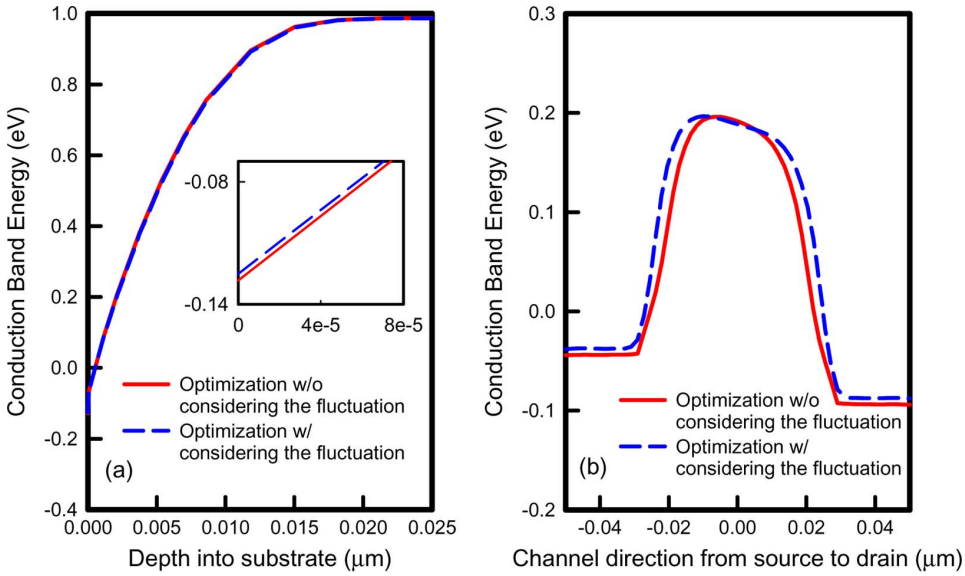

Fig. 7. Plots of band profile for optimization with and without considering threshold voltage fluctuation under off-state. (a) Surface to substrate. (b) Channel direction from source to drain which is about 2 nm below channel surface.

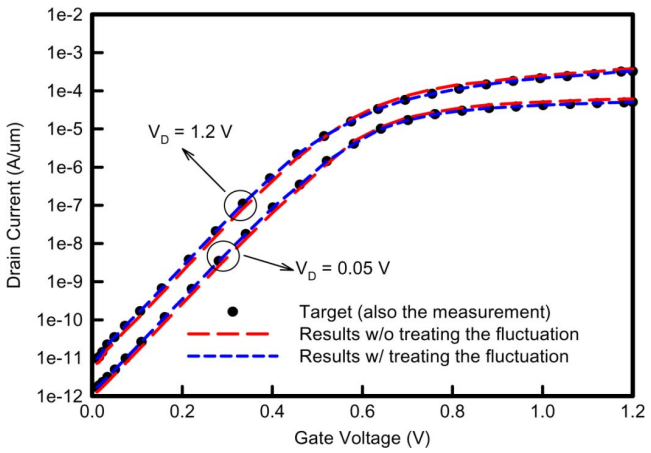

Fig. 8. Achieved accuracy of extracted I-V curves for explored 65-nm N-MOSFET.

TABLE II
LIST OF PROCESS RECIPE AND DEVICE PARAMETERS FOR DEVICE OPTIMIZATION W/ AND W/O CONSIDERING FLUCTUATION REDUCTION

Parameters	Parameters Range	Result w/o σ_{vth} reduction	Result w/ σ_{vth} reduction
Core V_T implantation	Energy: 20~80 KeV	58	24
	Dose: 1e12~2e13 cm^{-2}	2.7e12	1.3e13
N-LDD implantation	Energy: 10~50 KeV	28	29
	Dose: 1e13~5e13 cm^{-2}	3.1e13	3.8e13
P-WELL implantation	Energy: 200~400 KeV	250	250
	Dose: 1e13~4e13 cm^{-2}	2.4e13	2.4e13
Mobility model	B: 2e7~8e7 cm/s	3.5e7	3.41e7
	C: 100~500 $cm^{5/3}/(V^{2/3}S)$	160	170
Velocity saturation	V_{sat0}: 1e6~1e8 cm/s	9e6	9e6
	V_{sat1}: 0.5~1.0	0.81	0.82

voltage implant should be reduced at the channel surface. We believe that this approach provides an alternative to accelerate the tuning of process parameters and benefits fabrication of high

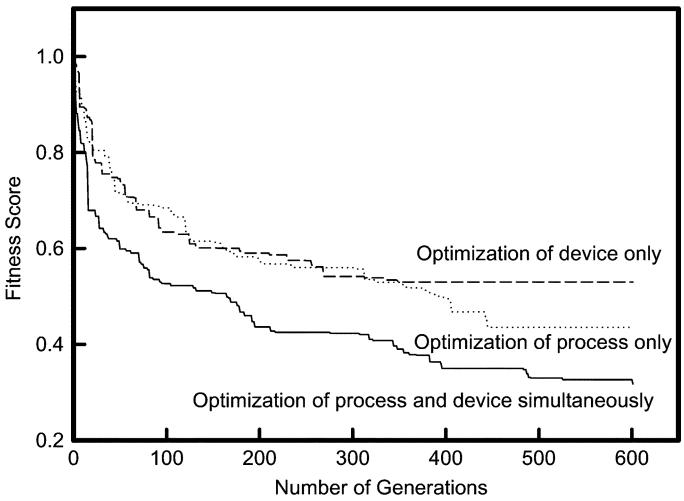

Fig. 9. Performance comparisons among three different evolutionary strategies. There are totally 31 process and device parameters to be optimized in the case of 2-D process and device simulations. Total time is about 70 h on PC-based Linux cluster with 16 CPUs.

performance device for sub-65-nm technologies, in particular, for the semiconductor foundry industry.

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