國立交通大學

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碩士論文

溶膠凝膠金屬氧化物薄膜電晶體之研究

Investigation on Sol-Gel Derived Metal Oxide Semiconductor Thin Film Transistors

研究生：郭豫杰 **Yu-Chieh Kuo**

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摘要

透明電子元件是新一世代光電元件中重要的技術。Zinc oxide (ZnO)，一種透明半導體材料，近年來廣泛被探討研究。它擁有大於可見光能量的能隙，在可見光區域幾乎透明；可以被製作在軟性基板上，並做成大面積且製作成本低廉。含摻雜物之氧化鋅材料，如二元的 ZTO、IZO，三元的 IGZO 都有相關研究製作出特性良好的元件。

本論文中探討之鋯摻雜氧化鋅材料(ZrZnO)使用溶膠凝膠(sol-gel)的方式來製造，以醋酸鋅為主要材料，水當作水解劑，先合成熔膠；再將此溶膠加入異丙醇當中攪拌並升溫到 60℃，溶膠中粒子鍵結成網狀的分子態稱為凝膠。

鋯摻雜氧化鋅(ZrZnO)薄膜旋塗沉積後(spin-coated)，搭配不同的熱處理條件，並且藉由不同氣氛下的二次退火來改善薄膜的品質，藉此降低元件對光的反應，進而改善薄膜電晶體的特性。我們還將本論文中提出之方法運用至它種氧化物半導體亦得到明顯效果，將會做一系列討論。此外，元件操作於不同環境下的穩定性表現也是我們探討的重點，在照光環境、不同氧分壓環境、和閘極偏壓操作下探討元件表現。在本論文中，我們使用 I-V 量測裝置(4156)來探討鋯摻雜氧化鋅薄膜電晶體的電性趨勢。

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Abstract

Transparent oxide semiconductors are nowadays a crucial technology for the next generation of optoelectronic devices. Oxide-based semiconductors have recently been proposed as active channel. Zinc Oxide (ZnO), a transparent conducting material, has been studied in recent years. As a wide band gap semiconductor, it is transparent to visible wavelengths, and the ability to fabricate good quality films over large areas with low cost, and compatible with flexible substrates.

Zr doped ZnO (ZrZnO) was sol-gel derived and thin film transistors (TFTs) were fabricated by spin-on deposition. The process of spin-on deposition provides a more efficient way for depositing devices and low cost.

After spin-on deposition, we improve the ZrZnO TFT characteristics by post-annealing treatment under different ambience, and we also replace ZrZnO by other transparent metal oxide semiconductors to obtain better device performances. Besides, devices operation under various conditions is a crucial point of electrical stability. The electrical characteristics were measured by the I-V measurement system.

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郭豫杰 2008 年 6 月

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Chapter 1 Introduction

1.1 General Background

Transparent electronics are nowadays an emerging technology for the next generation of optoelectronic devices. The fundamental device that enables the realization of transparent circuits is a transparent transistor. The possibility to perform transparent transistors is by using oxide semiconductor. They are widely used in a variety of applications (e.g. antistatic coatings, touch display panels, solar cells, optical displays, and sensors).

Transparent oxide semiconductor based thin film transistors have been proposed, using as active channel layer. They can broadly divided into two categories, single component systems, such as zinc oxide (ZnO), tin oxide, and multicomponent systems including zinc indium oxide (IZO), zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO). Although the control of the multicomponent oxides can be more difficult there are several advantages. The choice of alloys can be used to tailor the band gap. In the case of ZnO, which forms polycrystalline phases very easily even at room temperature , the additional of an element such as indium will inhibit the nucleation of polycrystalline grains. The remarkable feature of these materials is the mobility remains nearly unchanged even as the atomic disorder is increased in polycrystalline and amorphous forms. In addition, ZnO films have been deposited using many methods of deposition techniques. These include various sputtering techniques [1.1, 1.2], chemical vapor deposition (CVD) [1.3], molecular beam epitaxy (MBE) [1.4], pulsed laser deposition (PLD) [1.5], sol-gel [1.6, 1.7], and more.

Recently, high-performance thin-film transistors (TFTs) based on new materials have been investigated to achieve the features of larger diagonal size, greater transparency, more pixels, and lighter weight for high resolution electronic display devices [1.8, 1.9]. The most commonly used material for the active channel layer are amorphous a-Si:H and polycrystalline silicon poly-Si. However, there are a lot of drawbacks associated with both of these materials. While poly-Si devices have a high mobility 50cm^{2}V^{-1}S^{-1}, the thermal budget needed for their production makes them somewhat incompatible with flexible substrates based on polymers. In addition, poly-Si can be difficult to fabricate over large areas. Conversely, a-Si:H is readily used in large area flat panel displays but demonstrates a shortcoming, such as reduced pixel brightness due to opaque a-Si material.

The ZnO-based TFTs have been intensively studied due to their larger deposition area, non-toxicity, and high transparency as well as their compatibility with glass and plastic substrates, low-temperature processing, and simple wet chemical etching [1.10, 1.11]. These advantages of ZnO thin films have driven research efforts to develop high performance ZnO TFTs to overcome shortcomings of conventional a-Si TFTs.

The mixed oxide of Zn and Zr are very rarely studied and might be interesting from the point of view of application. With this understanding, we have fabricated sol-gel derived Zr doped zinc oxide based thin film transistors (ZrZnO TFTs). It is an attractive technique for obtaining thin films and has the advantages of ability to fabricate good quality films over large areas with low cost, and compatible with flexible substrates.

1.2 Motivation

ZnO is an n-type, wide band gap semiconductor with various applications, such as varistors, acoustic wave devices, and light emitting diodes. ZnO has a hexagonal wurtzite structure as shown in ***Fig1-1***, has a variety of optical and electrical properties depending on deposition condition. The lattice constants are a=3.24 Å and c=5.19 Å.

Generally speaking, ZnO based TFTs are usually deposited by sputter (e.g. DC sputter and RF sputter) or atomic layer deposition (ALD) or pulsed laser deposition (PLD). However, these deposition systems all need vacuum systems, will get much higher cost. In this study, we use sol-gel derived mixed oxide solution and spin-on deposition at room pressure, which is attracted attention due to its simplicity, low cost and advantages for large area deposition.

In undoped zinc oxide the n-type conductivity is due to deviations from stoichiometry. The free charge carriers result from shallow donor levels associated with oxygen vacancies and interstitial zinc [1.12], although interstitial oxygen and zinc deficiencies may also be present and produce acceptor states [1.13]. Regardless of the deposition method, all undoped ZnO conducting films have unstable electric properties in the long term. This stability is related to the change in surface conductance of ZnO films under oxygen chemisorptions and desorption [1.14]. The electrical properties of ZnO films strongly depend on the deposition method, thermal treatment and oxygen chemisorptions.

In this thesis, we studied the device properties of TFTs with sol-gel derived ZrZnO thin film, which act as an active channel layer deposited by spin-on method. Studies will be undertaken to interpret the growth mechanism of films, crystallographic structure, and electrical properties of the devices. We change manufacturing processes to find the best condition, for example: take the samples annealed under different ambiences, or deposit different numbers of layers. Besides, other transparent oxide semiconductors are deposited as active layers to fabricate TFTs, such as ZnO, ZTO and IZO. At last, we investigate devices working under various conditions, such as with light illuminated, under various oxygen pressures, and apply gate bias stress to test electrical stability of devices.

Chapter 2 Experimental Procedures

Table2-1 shows experiment flow path in my experiment. There were few papers about this deposition method for depositing ZrZnO film for TFTs utility. Because of the innovation of sol-gel derived solution, we have to reference lots of surveys on other treatment methods.

The sol-gel derived $Zr_xZn_{1-x}O$ was fabricated by the following steps: the sol-gel precursors were synthesized by the mixing of zinc Acetate $(Zn(CH_3COO)_2.2H_2O)$ and zirconium isopropoxide $(Zr((CH_3)_2CHO)_2)$ dissolved in 2-methoxyethanol and mono- ethanolamine (MEA), and the solution was stirring at 60 for 30 minutes. The nominal x value for $Zr_xZn_{1-x}O$ is 0.03, as shown in ***Table2-2***.

2.1 Fabrication of Thin Film Transistors

In this study, ZrZnO TFTs were fabricated on glass substrate coated with a 1000 Å sputtered MoW, which acts as gate electrodes for our TFT structure, and 3000 Å PECVD silicon nitride are deposited to be the gate insulator. Indium tin oxide (ITO) was deposited for the source and drain electrodes. TFTs which were fabricated for this study are bottom-gate structures with the ZrZnO active channel layer deposited at room temperature and room pressure by spin-on deposition. The rotation rate of the spin coater is 400rpm/15 seconds for step 1 and 2000rpm/20 seconds for step 2. After the ZrZnO film deposition, samples were taken to the hot plate for baking. The temperature was held at 50℃ for 5 minutes, then heated up to 300℃ and baked for 10 minutes. After baked thin films, they were crystallized at 350℃ for 1 hour in the furnace to improve the film quality. The device structure was shown in ***Fig2-1***. The active channel was patterned using standard photolithography and wet etching.

There are many scientific or technical literatures which report HCl and HNO_3 can etch ZrZnO film, however, we find the etching rate is too fast to avoid lateral etching. We use CH_3COOH as buffer solution to reduce the etching rate. We mix HCl, HNO_3, CH_3COOH, and de-ionized water with the optimal volume rate. Finally, we fabricate the device with "Standard Manufacturing Processes".

The bottom-gate structure devices were fabricated by the Taiwan TFT LCD Association (TTLA). The ZrZnO thin film was fabricated by spin coater in the National Nano Device Laboratories (NDL).

2.2 Experimental Procedures

The transfer characteristics [log (I_{DS}) - V_{GS}] of ZrZnO TFT fabricated by the "Standard Manufacturing Processes" are shown in ***Fig2-2***. We can see the device is normally-on and independent of gate bias and on current is about 10^{-6}A. ***Fig2-3*** shows the transfer characteristics of devices which were placed for 2 weeks, we observe that electric properties varied with time, and devices changed from depletion mode to enhanced mode. We need to understand the mechanism and find the method to solve it.

We consider that devices are placed in environment will suffer ambience effect, such as air. As we want to eliminate these behaviors and obtain proper characteristics immediately, we add one more step annealing process and try to solve it. Thus, we define the first annealing step as “***Curing***” and the second one as “***Annealing***” to avoid being confused, and we also define the baking step as “***Baking***”.

2.2.1 Various Ambience and Treatment Time

In this section, we discuss the ambience and time of heat treatment. ***Table2-3*** shows experimental flow of various ambience and treatment time in my experiment. First of all, we fabricate devices under various annealing ambience, such as oxygen, nitrogen, and vacuum. In order to compare performances resulting from the annealing step under various ambience and time, we fix the curing process at 350℃ for 1 hour under oxygen ambience in atmospheric anneal furnace but only change the annealing conditions. The ambience flow of oxygen and nitrogen are 10L, and the treatment time change from 10 minutes to 60 minutes. The annealing temperature are always fixed at 350℃. Atmospheric anneal furnace is used for oxygen and nitrogen ambience conditions, and backend vacuum annealing furnace for vacuum.

2.2.2 Various Film Deposition Conditions of Active Layer

In this section, we discuss the film deposition with various conditions. ***Table2-4*** and ***Table2-5*** show the various film deposition conditions of active channel layer in my experiment. We divide the deposition conditions into three parts: **numbers of active layers, period of baking time, and HMDS coating between dielectric and active layer interface**. Devices fabricated by optimal curing and annealing conditions still don't have large on currents. From pre study, we know devices with double active layers have better electrical properties. Thus, after first ZrZnO film deposition, we repeat the same spin-on process and coat another layer on the first one. Each layer is baked at 300℃ for 60 minutes. However, after ZrZnO deposition, we apply only one curing process under oxygen and one annealing process under nitrogen. N&K measurement system is used to fit the thickness of ZrZnO films.

The first step is used to adjust the period of baking times. The films are baked on the hot plate for three different times: 10, 30, and 60 minutes. In general, on current will be increased through better crystallization; therefore, we extend the baking time to obtain better quality of films.

In order to have a good interface between the insulator and active layer, we coat HMDS on the interface between insulator and active layer to reduce interface defects, and obtain better subthresold swing (S.S). HMDS is a purified hexamethyldisilazane with the chemical formula $[(CH_3)_2Si]_2NH$. The product is used to augment the adhesion of photoresist on silicon and SiO_2 surfaces. We compare electrical characteristics of devices with or without HMDS coating.

Generally speaking, the physical characteristics of semiconductors are easily modified by the crystallite size and boundary effects. We compare the devices that were only deposited single active layer and baked for 60 minutes. By this experiment, the effect of double layer can be observed.

2.2.3 Various Treatment on Devices

Table 2-6 shows the experimental flow of various RTA treatment and passivation process in my experiment. Rapid Thermal Annealing (RTA) can enhance the conductivity of the film, and further to improve device performances. Therefore, application of RTA under two different ambiences is placed between curing process and annealing one. The first RTA is under Ar ambience, the second one is under NH_3 ambience. The pressure is at 10mtorr and rate of gas flow are 20sccm, and the process temperature is at 350℃ for 2 minutes. All treatment conditions are the same except ambiences.

Besides, thin film transistors usually need the passivation layer to protect active channel layer from humidity, gas, and other factors from circumstance. Silicon oxide (SiO_x), silicon nitride (SiN_x) and PC403 are deposited to passivate the device. SiO_x and SiN_x are deposited by DC sputter. PC403 is coated by spin-on deposition, and the spin condition is 800rpm/18 seconds, followed by the exposure to UV light and post-bake at 220℃ for 1 hour.

2.2.4 Other Transparent Oxide Semiconductor TFTs

We now understand the optimal manufacturing processes of ZrZnO TFTs, however, devices performances are not good enough to compete with a-si TFTs. Fortunately, there are still many kinds of sol-gel derived materials. We replace the ZrZnO active channel layers by these materials, such as zinc oxide (ZnO), zinc tin oxide (ZTO), zinc indium oxide (IZO), and compare the electrical properties. ZrZnO and ZnO TFTs fabricating conditions are: double layers, with HMDS coating, baking for 60 minutes, curing for 60 minutes under oxygen, and annealing for 60minutes under nitrogen. ZTO and IZO TFTs fabricating conditions are: one layer, baking for 60 minutes, curing for 60 minutes under oxygen and annealing for 10 minutes under nitrogen or oxygen. We compare performances of each material and use material analysis to explain results.

Chapter 3 Effect of Various Experimental Conditions

3.1 Theories Review

3.1.1 Surface Conductivity and Photoconductivity

In general, a semiconductor adsorbs light with energy higher than the band gap energy, electron-hole pairs are generated according to Eq.(3-1),

$$hv \rightarrow h^{+} + e^{-} \qquad (3\text{-}1)$$

effectively result in the increase of electrical conduction which may be a fundamental, solid-state processes for photoconduction of conventional semiconductors. The electrons and holes generated by light illumination rapidly vanish after turning off the light. Therefore, the photoresponse rise in conductivity upon light illumination and the decay after close the light are expected to be very rapid.

For the last two decades it has been well known that the photoresponse of n-type metal oxide semiconductors such as titanium and zinc oxides shows a slow conduction decay process, as opposed to the rapid solid-state process, which is controlled by surface effects such as **gas adsorption and desorption** [3.1, 3.2]. In the dark environment, oxygen molecules adsorb on the oxide surface as negatively charged ions by capturing free electrons of the n-type oxide semiconductor, as described by Eq.(3-2),

$$O_2(g) + e \rightarrow O_2^{-}(ad) \tag{3-2}$$

Therefore, create a depletion layer with low conductivity near the surface. When light with energy higher than the fundamental band gap of the semiconductor illuminates, holes which are produced by light adsorption near the surface migrate to the surface along the potential slope created by band bending and discharge the negatively charged adsorbed oxygen ions.

$$h^{+} + O_2^{-}(ad) \rightarrow O_2(g) \tag{3-3}$$

Electrons produced at the same time by the light destruct the depletion layer, and increasing the conductivity [3.3]. Thus the photoresponse of oxide semiconductors includes adsorption Eq. (3-2) and photodesorption of oxygen on the surface Eq.(3-3) in addition to the very rapid change in conductivity by photogenerated hole-electron pairs and their extinction, which is, in other words, the solid-state process Eq.(3-1). Consequently, the decay of photoconduction is strongly dependent on the ambient gas conditions, being slow in vacuum or an insert gas atmosphere such as nitrogen, but fast in air [3.4].

Collins and Thomas further proposed that an electron enriched-type space-charge layer is formed by the photolysis of the zinc oxide (single crystal) surface. The holes from hole-electron pairs generated by light adsorption discharge surface lattice oxygen ions leaving an excess of zinc (interstitial) near the surface, according to Eq.(3-4).

$$Zn^{2+}(c) + O^{2-}(c) + 2hv \rightarrow 1/2O_2(g) + Zn_{i.} \tag{3-4}$$

Ionization of interstitial zinc by Eq.(3-5) supply free carrier electrons.

$$Zn_i \rightarrow Zn^{+} + e^{-} \qquad (3\text{-}5)$$

It is very interesting to investigate the photoconductive properties of thin films of n-type oxide semiconductors, because it can be assumed that they have some special photoelectrical properties due to the higher ratio of their surface atoms compared to bulk materials.

3.1.2 Physisorption and Chemisorption

There are two major classifications of adsorption shown in ***Table3-1***: physisorption (weak bonding, heat of adsorption is less than about 6 kcal mol^{-1}**)** and chemisorption (strong bonding, heat of adsorption is usually greater than about 15 kcal mol^{-1}). ***Fig3-1*** is the Lennard-Jones representation of physisorption and chemisorption. The Lennard-Jones model is a simple way to visualize the development of the activation energy ΔE_A of chemisorption. This is the energy that must be supplied to a molecule before it will chemisorb. In ***Fig3-1***, consider a molecule approaching the solid, with the total energy zero as indicated in curve a (the physisorption curve). It is not necessary to provide the total energy of dissociating the molecule before it can chemisorb; a lesser energy ΔE_A suffices when the molecule is near the surface, where in the Lennard-Jones model the curves for physisorption and chemisorption intersect. Thus the rate of adsorption (assuming modest coverage) is

$$\frac{d\theta}{dt} = \kappa_{ads} \exp\left(\frac{-\Delta E_A}{\kappa T}\right) \qquad (3\text{-}6)$$

where θ is the fraction of available surface sites covered. Equation (3-6) represents the rate for the normal case where ΔE_A is provided thermally. In this case, by Eq.(3-6), at very low temperature chemisorption cannot realistically occur.

In principle during physisorption and chemisorption of an adsorbate (the adsorbing species), there is no movement of the atoms of the adsorbent (the solid) from their normal lattice position. In practice, especially with chemisorption, there is movement and relocation of the surface atoms. One can view incipient formation of a new phase as the point where the surface atoms of the adsorbent change their bond structure, breaking bonds to the solid and replacing them with bonds to the adsorbate. It will not dwell on new phase development - the processes are hard to define quantitatively in practical cases, although with the new surface spectroscopies such as LEED (low-energy electron diffraction) the progress from simple adsorption to a new surface phase can be followed. It will instead concentrate on the description of adsorption, emphasizing the form most basic to gas sensors-*ionosorption,* adsorption as a surface state, where charge is transferred from the conduction or valence bands to ionize the adsorbate, but where local bonding of the adsorbate to one or a few atoms of the solid can be ignored.

The dependence of the rate of physisorption and chemi- sorption on the pressure of the species in the gas phase can be complicated; there are many expressions, both analytical and empirical, describing the dependence. In most of the discussion to follow we will assume the simple Henry's law, namely that the rate is proportional to the pressure. This law applies reasonably well at low coverage of the surface, but is inadequate as one approaches a monolayer.

3.2 Analysis of Experimental Results

3.2.1 Effect of Various Ambience and Treatment Time

In ***Fig2-2***, ***Fig2-3***, the standard TFTs work in depletion mode and change electrical properties with time. Thus, we apply annealing under oxygen ambience with different time to solve the problem. ***Fig3-2*** shows the transfer characteristics of annealing under oxygen ambience with different time (V_D=21V). The devices with different annealing time show the different behaviors. From the result, we understand devices with short annealing time will exhibit obvious on-off characteristics but small on currents. In contrast, long annealing time makes the thin film too conductive to turn off. However, time dependent electrical characteristics are not eliminated through annealing under oxygen ambience. ***Fig3-3*** shows the time dependent electrical properties of 60 minutes annealing, the on current decreases slightly but the off current decreases by five orders of magnitude several days later. The time dependent behaviors also happen to other annealing time of 10 and 30 minutes. From the result, we should apply heat treatment under other ambient environments.

Fig3-4 shows the I_D-V_G transfer characteristics of annealing in vacuum with different time (V_D=21V), the devices are all normally-on and the on current decreases while heat treatment time increasing, but the time dependent behaviors still don’t eliminate after vacuum annealing, as shown in ***Fig3-5***. The device with annealing time of 10 minutes changes from normally-on state to switching characteristics several days later, but on current is too small to apply in the panel. These results also happen to other treatment time devices.

Finally, we try to apply nitrogen into annealing processes to see if nitrogen can prevent the time dependent behaviors. ***Fig3-6*** shows the I_D-V_G transfer characteristics of the devices with annealing of different time (V_D=21V). From this figure, we know that the devices with 10 minutes treatment have best characteristics. The on current decreases while time increasing, but the most important thing is to solve the time dependent behaviors. Fortunately, the devices annealed under nitrogen ambience do not change with time and fix the current-voltage curves even after two weeks, as shown in ***Fig3-7***. The devices are now time independent after the annealing under nitrogen.

The mechanism of the time-dependent behaviors is attributed to the **oxygen adsorption,** mentioned at **section3.1**. A previous study reported that the chemisorbed O_2 molecules on ZrZnO TFTs undergo partial charge transfer (forming depletion layers below the active surface) and that the threshold voltage (Vt) systematically moves in the positive direction [3.5]. This is mainly due to conductivity changes caused by surface band bending, induced by O_2 molecule adsorption. It is known that surface defects of metal oxides, such as oxygen vacancies, function as adsorption sites. O_2 molecules adsorbed at these sites act as electron acceptors to form O^{2-} at room temperature. These chemisorbed O^{2-} ions deplete the surface electron-states and consequently reduce the channel conductivity. Devices without annealing or annealing in vacuum show the switch properties several days later because of the slow rate of oxygen adsorption, so electrical characteristics are time dependent.

In ***Fig3-2***, we also take annealing step for 10 minutes under oxygen ambience and fabricate the device with proper switching properties. From this experiment, we know that devices annealed under nitrogen or oxygen ambience can show switching properties immediately. The reason is that by introducing the annealing step, whether oxygen or nitrogen, the method can sweep out the chemical absorbed oxygen, fix the grain boundary defect and reduce the adsorption sites; therefore, conductivity of bulk decrease so gate can effectively control the switching properties., and TFTs will show switching properties without long waiting time [3.6].

However, transfer characteristics of ZrZnO TFTs annealed under oxygen ambience are time-dependent, that means the oxygen supplied by annealing step still react with oxygen in environment. The reason is that oxygen annealing supply oxygen atoms into the film, so chemical adsorption oxygen still exist in the film which caused devices are time dependent. As a result, nitrogen is decided to be annealing environment.

3.2.2 Effect of Various Film Deposition Conditions of Active Layer

Fig3-8 (V_D=21V) shows the transfer characteristics of devices with different baking time, and all these devices have two layers of ZrZnO film as active layers. Devices with 30 minutes baking time only have a little higher current than with 10 minutes baking time. However, devices with 60 minutes baking time show largest on current and best swing, and the threshold voltage makes a positive shift. The characteristics of device have been much improved through longer baking step. From results of electrical properties, we assume that film quality will be increased through longer baking time; therefore, larger on current and better swing can be obtained.

After we adjust baking time, we try to improve the interface between active channel layer and dielectric, which is very important to influence device performances. The electrical properties that we discussed above suffer Drain Induced Barrier Lowering effect (DIBL), which means the threshold voltage will be influenced by the drain bias, and the subthresold currents make a parallel shift to the negative side with drain bias increasing, as shown in ***Fig3-9***. Therefore, we deposit HMDS on the interface to reduce defects and enhance device performances.

From this section, we understand longer baking time will obtain better device performance. Here we apply HMDS to the various baking time experiment. From ***Fig3-8***, devices without HMDS show little differences between 10 and 30 minutes baking time, but devices with 60 minutes show the best electrical properties. However, with HMDS coating, devices with various baking time show almost the same performances and electrical properties, as shown in ***Fig3-10***. The result means through HMDS coating, device performances can be improved to the same level. Then we compare the devices performances with or without HMDS of various baking time, as shown in ***Fig3-11***, ***Fig3-12***, and ***Fig3-13*** which represent 10, 30, and 60 minutes. There is a positive shift about 20V and lager on current after HMDS coating in the first two graphs, but there are almost no differences in the last one, which means HMDS can effectively reduce the interface defects and obtain better swing. However, we can still get the same result from longer baking time, even without HMDS coating. ***Fig3-14*** shows the mobility changing ratio

(μ/μ_0) with various baking time, the maximum ratio is at baking for 10 minutes. Finally, we decide the manufacturing processes should have baking time of 60 minutes and with HMDS coating for interface improvement.

As we adjust the baking time of active ZrZnO films from 10 to 60 minutes, we fabricate devices which are deposited only single active layer, and the baking time is 60 minutes. We use N&K analysis system to measure film thickness, the thickness of one layer is about 500 Å and double layers are about 900 Å. ***Fig3-15*** shows the transfer characteristics of different active layers ZrZnO TFTs. The devices with two actives layers have larger on current and better S.S. and on-off ratio. Devices that are only deposited single active layer show smaller on current and worse swing than double layers, and characteristics are also worse than devices that were only baked for 10minutes. The longer baking time caused smaller on current in single layer case. The phenomenon proves that the improvement of electrical characteristics is caused by second layer deposition. However, annealing time of two active layers TFTs requires 60 minutes because short annealing time is not long enough to sweep out the chemical absorbed oxygen, fix the grain boundary defect and reduce the adsorption sites; thus, we can’t get the proper electrical behaviors immediately.

3.2.3 Effect of Various Treatment on Devices

We apply rapid thermal annealing will enhance the performances and increase the grain size of semiconductors. ***Fig3-16*** shows the transfer characteristics of devices annealed under NH_3 ambience, and ***Fig3-17*** shows the condition under Ar ambience. Although the initial properties of devices are poor, after application of RTA, the transfer characteristics made a negative shift let on-state current increase, but off-state current also increase heavily in the Ar case. This phenomenon results from more oxygen vacancies were created during RTA process, so devices can't be turned off. Therefore, we add one more annealing step under nitrogen ambience after RTA treatment, devices show much better switching properties after whole post treatment, such as: large on current, small threshold voltage and higher mobility. As a result, the continual heat treatment improves device performances effectively.

Devices usually need passivation layers to prevent themselves from humidity or other factors from environment. Silicon oxide, silicon nitride, and PC403 are used to be passivation layers of our devices. The transfer characteristics of the devices with SiOx passivated are shown in ***Fig3-18***. The devices do not have good switching properties after the SiOx deposited, and the off-state current is so large that the on-off ration is only about 10^2. The same situations also happen in the SiNx deposition, as shown in ***Fig3-19***. Therefore, we replace the SiOx, SiNx by PC403 which is coated by the spin-on deposition. Unfortunately, as shown in ***Fig3-20***, the devices still show bad switching properties and large off-state current.

All of them show the large off-state current as the device work in the off-state. When the device is working on off-state, the currents are too large to ignore, we attempt to find the path where currents passed through. We measure the devices with gate floating and only apply the drain voltage. The measured current is as the same order as the off-state leakage current, so we understand the leakage current passed through passivation layer. The fact that passivated devices show larger on current can be explained by oxygen adsorption theory again. Because when devices are capped by passivation layer, it have been sent to the vacuum chamber and given plasma treatment. Plasma damaged the back surface of thin film; therefore, lots of oxygen vacancies were created and the conductivity increased. Besides, devices that were capped with passivated prevent oxygen molecules to adsorb on the surface, so less $\boldsymbol{O^{2-}}$ will adsorb on the back channel to deplete the bulk. Consequently, we should research new material to passivate our devices without plasma or heat treatment.

3.2.4 Other Transparent Oxide Semiconductor TFTs

We apply the optimal conditions to fabricate TFTs with different active layer materials, such as ZnO, ZTO and IZO. They both are transparent oxide semiconductors and sol-gel derived materials. Here we compare three kinds of devices. ***Fig3-21*** shows the transfer characteristics I_D-V_G of ZrZnO TFTs and ***Fig3-22*** shows the I_D-V_D of ZrZnO TFTs. The current dropping effect was shown in I_D-V_D curve that means too large resistance in the depletion region. In addition, DIBL effects were eliminated after HMDS coating. ***Fig3-23*** shows the transfer characteristics I_D-V_G of ZnO TFTs and ***Fig3-24*** shows the I_D-V_D of ZnO TFTs. Devices show good saturation currents and on-sate current is at the same order as ZrZnO TFTS. ***Fig3-25*** shows the transfer characteristics I_D-V_G of ZTO TFTs and ***Fig3-26*** shows the I_D-V_D of ZTO TFTs. The current crowding effects are showed in ID-VD curves, that means large contact resistance between S/D metal and ZTO active layer.

Besides ZnO and ZTO application, we also replace ZrZnO by IZO, devices fabricated by it show excellent electrical characteristics than other materials. ***Fig3-27*** shows the transfer characteristics I_D-V_G and ***Fig3-28*** shows the I_D-V_D of IZO TFTs. Compare with ZrZnO TFT, IZO and ZTO TFT have larger on-state currents and better subthreshold swing. IZO TFTs show the best performance over other three kinds of devices. From I_D-V_G, on-off ration is about 10^7 and threshold voltage is only about 0.9V. I_D-V_D shows good saturation current which means fully depletion of channel. The characteristics of IZO TFT is as good as the traditional a-Si TFT. After considering the power consumption issue, we decide the ZrZnO active layer material should be replaced by IZO. ***Table3-5*** shows the device parameters of different TFTs fabricated by ZrZnO, ZnO, IZO, and traditional a-Si TFT [3.7].

Chapter 4　Study on Electrical Stability

In this chapter, we discuss some factors which affect performances of oxide semiconductor based devices, such as light illumination and ambient pressure, which were widely researched in recent years. We find some explanations from papers and verified them by results. Besides, we use gate bias stress to discuss the stability of devices to know degradation of devices under long time operation.

4.1　Influence of Light Illumination

Generally speaking, we measure devices in the dark environment (in the black box) and under room pressure. ***Table4-1*** shows the experiment flow of devices under light illumination. We find the devices fabricated by the standard manufacturing processes should be placed in the box for few minutes even few hours to get stable electrical performances. Besides, when devices are illuminated by light, the transfer characteristics turn to normally-on and show large off currents immediately, we should keep them in the dark for 15 minutes but they still don't recover to initial states, as shown in ***Fig4-1***.

However, devices fabricated with annealing step under nitrogen ambience show the proper characteristics in short time when placed in the dark, as shown in ***Fig4-2***. When light illuminate on devices, off current increases from 10^{-12} to 10^{-8}A, that means devices can't be turned off. But the most important of all, devices quickly return to the initial states after light illumination. The recovering time decrease from an hour to few minutes. These behaviors let the devices become much easily to measure.

The phenomenon indicates that light illumination caused electrical behaviors still are related to “oxygen adsorption and desorption”. When light illuminates devices, electron-hole pairs are generated by photo energy, and holes are captured by the O^{2-} near the surface and oxygen molecules desorbed [4.1]. The excess electrons increase the free carrier concentration and on-state and off-state currents increase immediately. ***Fig4-3*** shows the physical model of oxygen effect on the conductance of ZnO film and the interaction with light [4.2, 4.3].

Without the light illumination, the electrical characteristics recover to its initial states slowly. As we mentioned before, this is mainly due to conductivity changes caused by surface band bending, induced by O_2 molecule adsorption. It is known that surface defects of metal oxides, such as oxygen vacancies, function as adsorption sites. O_2 molecules adsorbed at these sites act as electron acceptors to form O^{2-} at room temperature. These chemisorbed O^{2-} ions deplete the surface electron states and consequently reduce the channel conductivity [4.4]; therefore, the standard devices need more time to complete the adsorption behaviors, so the photo response speed is very slow.

From the explanation in **section3.1**, we know that annealing step can sweep out the chemical absorbed oxygen, fix the grain boundary defect and reduce the adsorption sites, thus the devices with annealing under nitrogen ambience will return to the initial state quickly even after light illumination.

4.2 Influence of Oxygen Pressure

Since we frequently mention the oxygen effect to our devices, we compare devices performances under room pressure and in vacuum environment. By observing the behaviors under different conditions, we can verify the theory of oxygen adsorption. ***Table4-2*** shows the experiment flow of devices measured under different oxygen pressure. First, we put devices into vacuum chamber and pumped down to 10^{-2}torr and measure devices under room temperature in the dark. After transfer characteristics under room pressure were been saved, oxygen flow into systems and pressure was set at 1, 10, 100, 760torr. We measure the same device at each pressure condition.

Fig4-4 shows the transfer characteristics of ZTO TFTs measured under different oxygen pressure. The current-voltage curve has a shift to positive gate voltage direction while increasing oxygen pressure. This phenomenon has already been discussed from other researches [4.5].The device used in this paper is IGZO TFT. The author suggested that the increase in oxygen partial pressure reduces the number of carriers in the channel, resulting in higher gate voltages to be required to turn on devices, as shown in ***Fig4-5***. It also can be explained by the theory we mentioned early. At 760torr, oxygen molecules are sufficiently supplied by the environment, thus the oxygen adsorption reacts very quickly to deplete the surface region, the conductivity decreases and need higher voltage to turn on. However, when devices are placed in vacuum, such as 1, 10torr, the amount of oxygen molecules are not enough to sufficiently occupy oxygen vacancies, so the conductivity doesn’t increase too much. Therefore, the I_D-V_G curve has a negative shift so devices obtain larger currents. From the result, oxygen pressure surely influences devices properties.

Since me mentioned light illumination will desorb chemisorbed oxygen molecules, we suppose transfer characteristics will be similar while measure with light under different pressure. ***Fig4-6*** shows transfer characteristics of ZTO TFTs measured with light illumination under different oxygen pressure. Current-voltage curves do not show the same characteristics between each oxygen pressure, but devices which are measured under 760torr still have a shift to positive Vg direction. This fact illustrates that there is a relationship between properties of thin film and oxygen pressure, and it suggest that the device passivation should be deposited in vacuum to assure the real property of film. As a result, there is still a narrow gap between different electrical curves measured under different oxygen pressure. The experiment proves again that light illumination can desorb chemisorbed oxygen and devices performances are influenced by oxygen molecules.

4.3 Influence of Bias Stress

The stability of TFTs under bias stress is of crucial importance for their exploitation. The application of a prolonged bias stress result in a threshold voltage shift in a-Si TFTs [4.6]. Given the potential of ZrZnO, in this section we investigate the effect on device characteristics of the prolonged application of gate bias to the devices under room pressure and in vacuum. ***Table4-3*** shows the experiment flow of devices measured under gate bias stress.

The stress condition are: $\mathbf{V_G = Vt + 20V}$, $\mathbf{V_D = 0V}$, and we measure devices at 100 / 300 / 600 / 1000 seconds , the total stress time are 1000 seconds. After 1000 seconds stress, devices take a period of relaxation of 1000 seconds. ***Fig4-7*** shows the transfer characteristics I_D-V_G of ZrZnO TFTs for different stress time under room pressure. The application of positive bias stress result in the displacement of the transfer characteristic in the positive direction, but has no effect on the subthreshold behavior. After stress experiment, the devices spontaneously recover their initial state after a period of relaxation of 1000 seconds.

It has been reported that a positive shift of the threshold voltage under positive gate bias stress is the evidence that **charge trapping** is the dominant instability mechanism [4.7]. However, in order for a device to recover to its initial state once charge is injected into the insulator bulk after a period of stress, some form of bias thermal annealing is required. Similarly, thermal annealing is usually necessary to remove any defects that may have been created during stressing. The recovery behaviors that we observed under atmosphere are the same as the author did [4.6]. As we mentioned above, oxygen molecules influence device performances; therefore, we would like to apply gate bias stress in vacuum to compare the results. We suppose that devices will recover to initial state in vacuum as room pressure case. But this phenomenon is not observed when devices are placed in vacuum. ***Fig4-8*** shows the I_D-V_G of ZrZnO TFTs placed for different stress time in vacuum. The transfer curve still has a shift to positive V_G direction after bias stress; however, devices will not recover their initial state after a period of relaxation of 1000 seconds, which is different to room pressure case. As a result, we realize that recovery behaviors are related to oxygen molecules and pressure.

According to the different behaviors, we suppose that degradation of electrical characteristics not only caused by gate bias stress but also affected by oxygen adsorption. When gate bias stress was applied under room pressure, excess electrons were generated and reacted with oxygen molecules; therefore, lots of chemisorbed O^{2-} adsorbed on the surface and depleted the bulk to make devices degraded, thus transfer characteristics are displaced in the positive direction and swing is unchanged. After bias stress; however, without induction by the positive gate voltage, these excess chemisorbed O^{2-} will desorb from the surface so devices recover to its initial state. On the other hand, when devices are stressed in vacuum, because there are not enough oxygen molecules to form chemisorbed O^{2-}; therefore, excess electrons will be trapped into insulator or at the interface between channel and insulator, but the former behaviors need thermal energy or negative gate bias to remove the injected charges, devices can't recover to its initial state after a period of relaxation.

In conclusion, gate bias stress generates excess carriers in the channel. Under atmosphere, chemisorbed O^{2-} is the dominant factor that caused shift of the I-V curves, thus the transfer characteristics will recover. In vacuum, excess electrons are trapped into the insulator or on the interface between insulator and channel, thus devices can't recover resulting from charges trapped into the insulator.

Chapter 5 Conclusions

We have developed an optimized deposition condition for sol-gel ZrZnO semiconductor film and succeeded to fabricate a ZrZnO-based transparent thin film transistor with bottom-gate structure. The optimal conditions for depositing the ZrZnO film by spin coater are at room temperature and deposit two layers, each layer is baked on the hotplate at 300°C for 60 minutes. After film deposition, devices are taken one curing step under oxygen ambience at 350°C for 60 minutes. With the development of wet etchants, active regions can be patterned accurately. We solve the time dependent behaviors of devices and light illumination effect by adding post annealing treatment under nitrogen ambience at 350°C to complete device fabrication. Besides, the oxygen adsorption theory successfully explained the mechanisms of light illumination effect and oxygen pressure effect. ZnO, ZTO and IZO are also discussed to replace the active channel layer in this thesis. Devices with IZO active layer have the best performance, which can compete with traditional a-si TFTs. We also make some measurements to test electrical stability of devices, such as light illumination, oxygen pressure, and bias stress. At last, we successfully demonstrated sol-gel derived ZnO and ZrZnO and IZO based TFTs on glass substrate by spin-on deposition at low temperature. For large area flat-panel display fabrication in the future, the chemical solution deposition process provides a low cost and more efficient way for depositing devices than vacuum deposition techniques.

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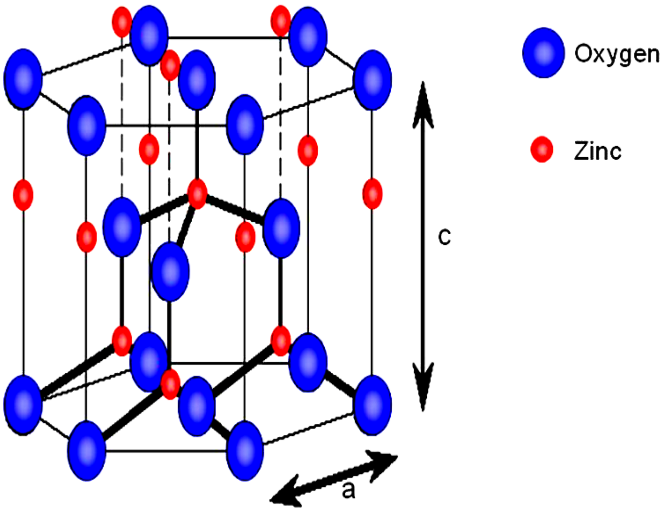

Fig1-1 The wurtzite lattice structure of zinc oxide: small circles represent zinc atoms, the large circles are oxygen atoms.

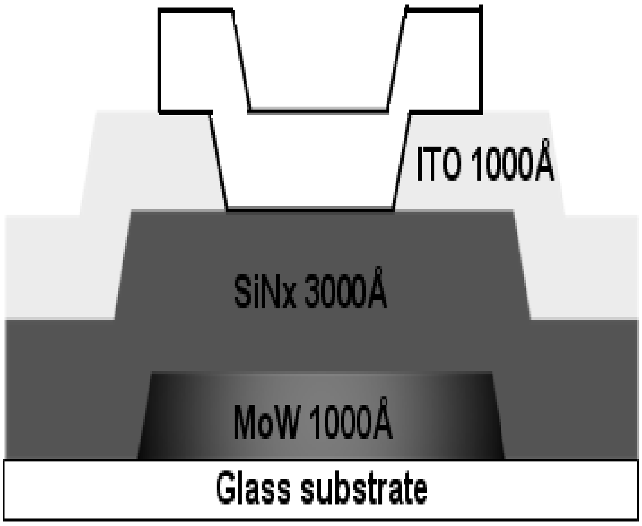

Fig2-1 The device structure of thin film transistor

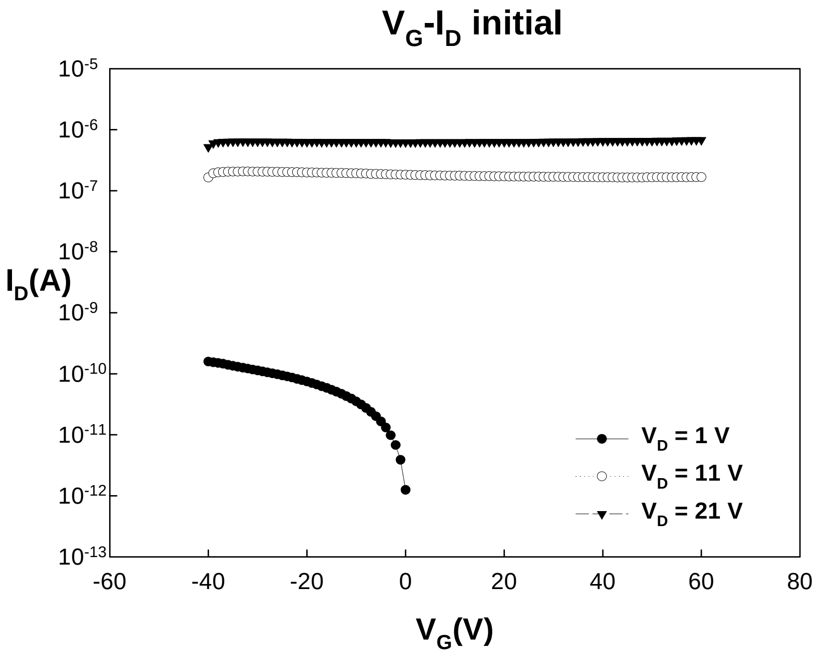

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Fig2-2 Transfer characteristics of ZrZnO TFTs that are fabricated by "Standard Manufacturing Processes"

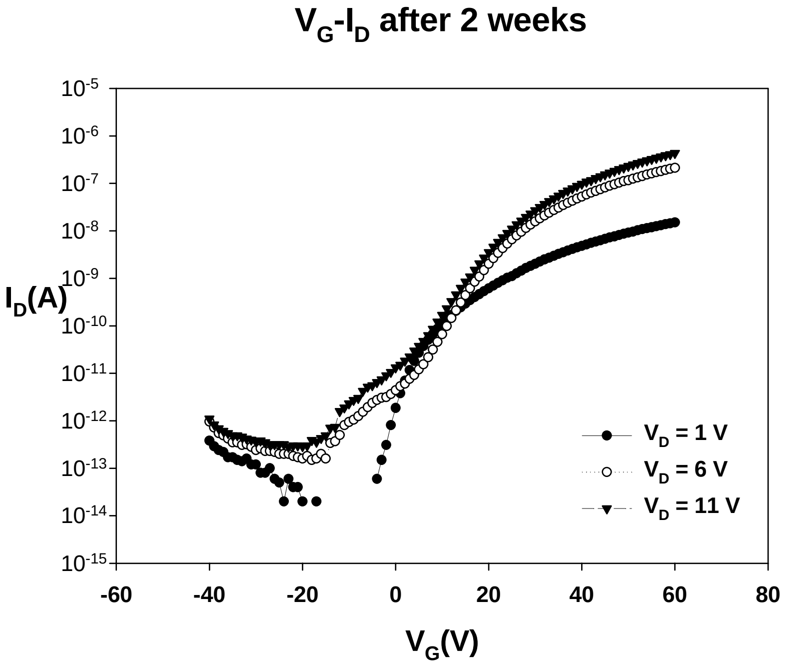


Fig2-3 Time dependent transfer characteristics of ZrZnO TFTs that are fabricated by "Standard Manufacturing Processes"

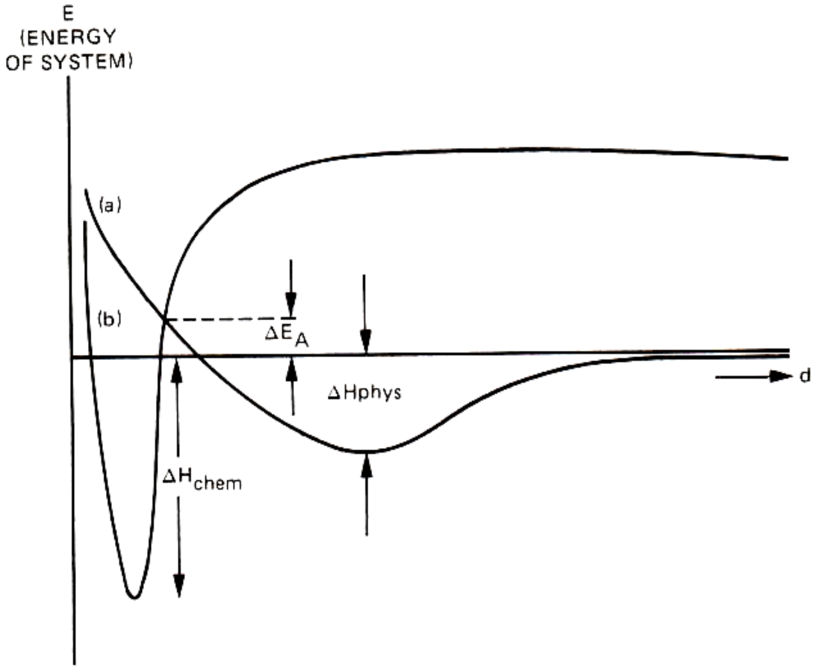


Fig3-1 Lennard-Jones Model of physisorption and chemisorption; (a) phtsisorption of a molecule, (b) chemisorption, where at d=∞, enough energy has been introduced to dissociate the molecule

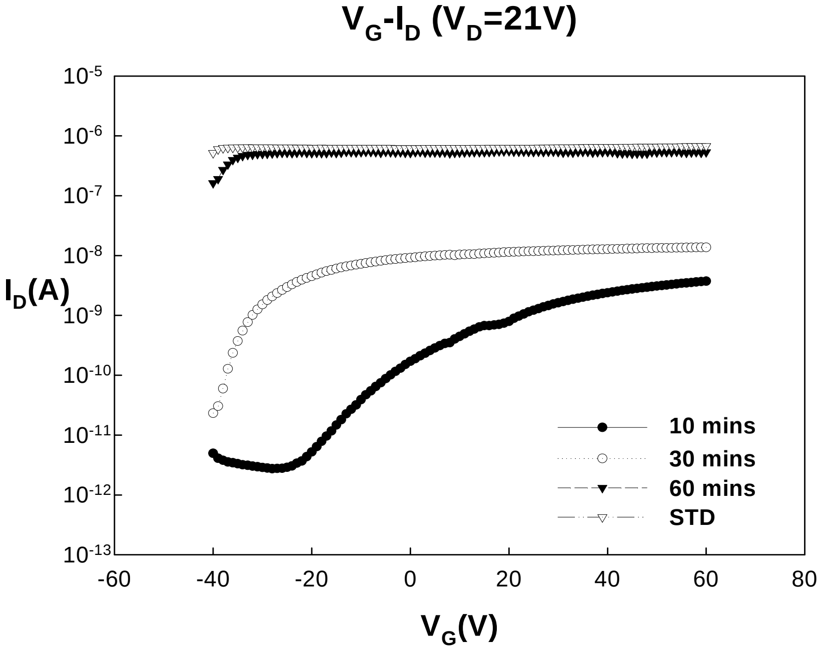


Fig3-2 Transfer characteristics of ZrZnO TFTs that are annealed under oxygen ambience with various time

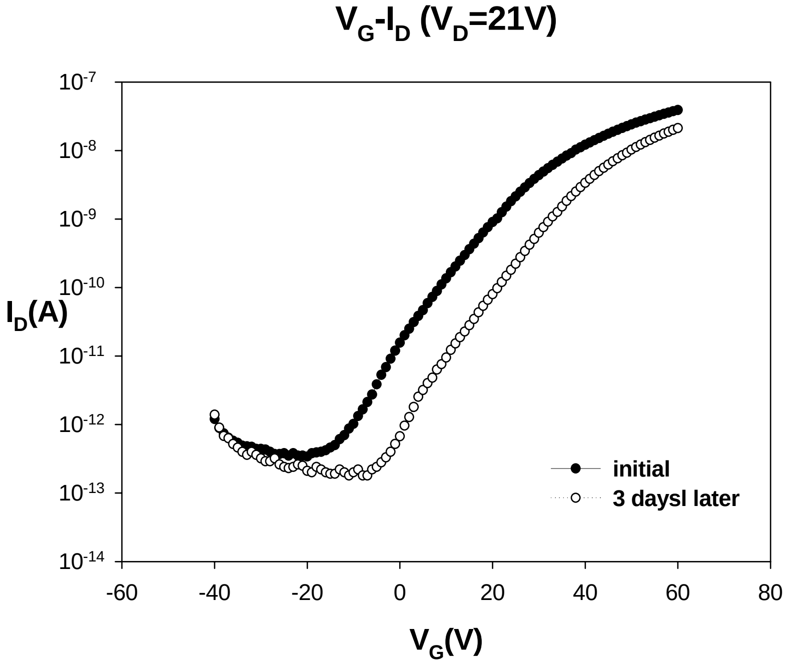


Fig3-3 Time dependent transfer characteristics of ZrZnO TFTs that are annealed under oxygen ambience for 60 minutes

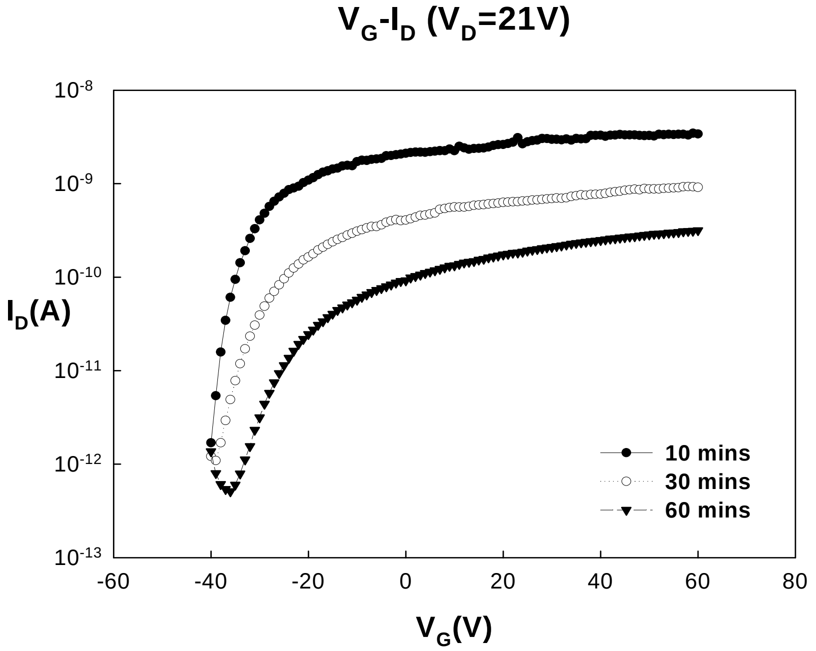


Fig3-4 Transfer characteristics of ZrZnO TFTs that are annealed in vacuum with various time

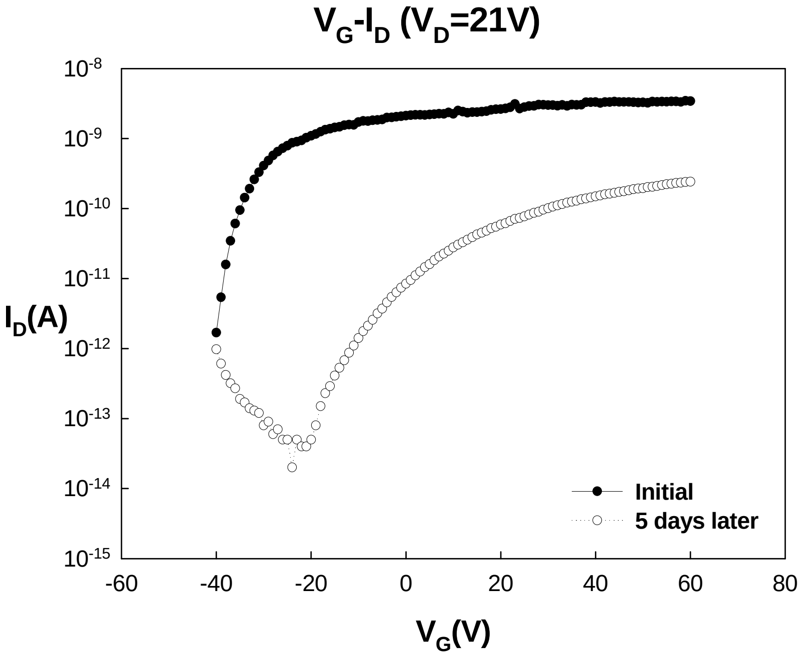


Fig3-5 Time dependent transfer characteristics of ZrZnO TFTs that are annealed in vacuum for 10minutes

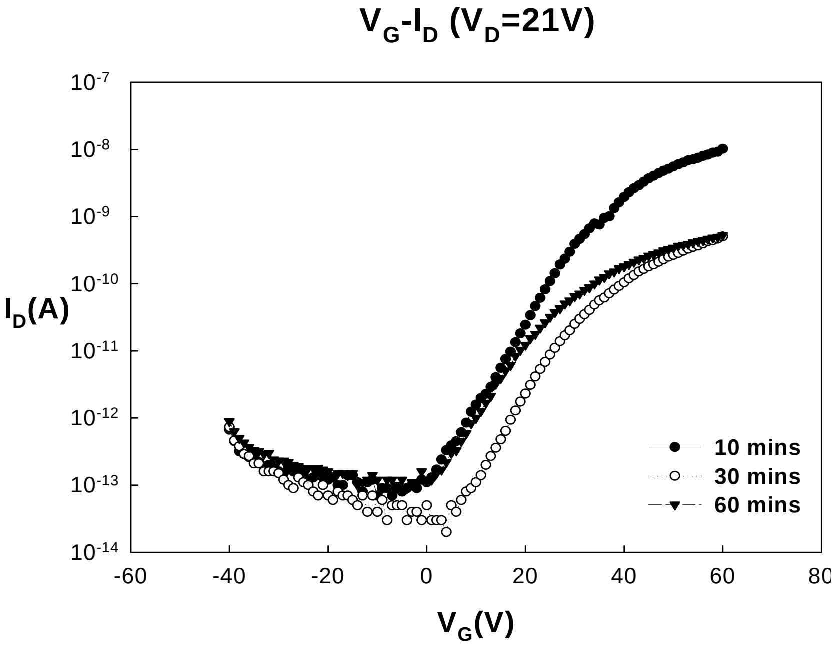


Fig3-6 Transfer characteristics of ZrZnO TFTs that are annealed under nitrogen ambience with various time

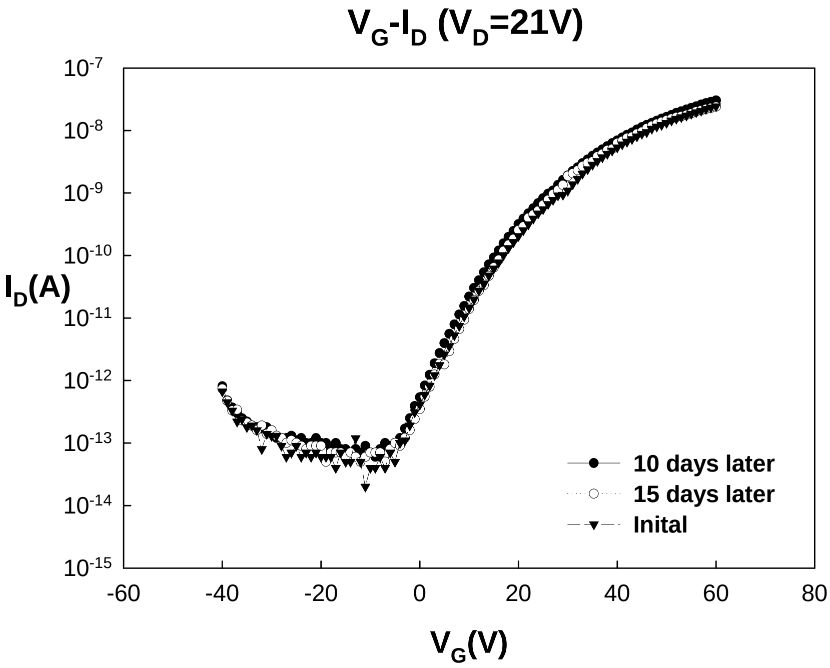


Fig3-7 Time independent transfer characteristics of ZrZnO TFTs that are annealed under nitrogen ambience for 10 minutes

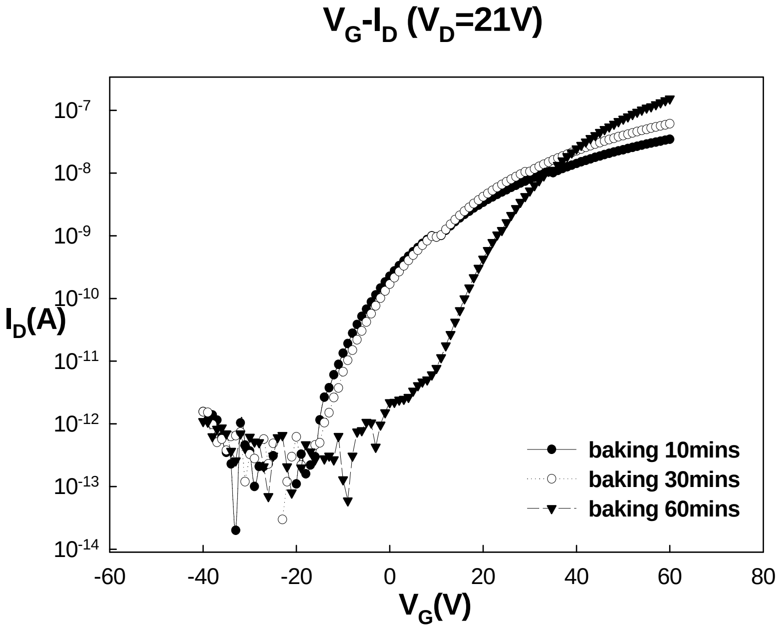


Fig3-8 Transfer characteristics of ZrZnO TFTs with various baking time

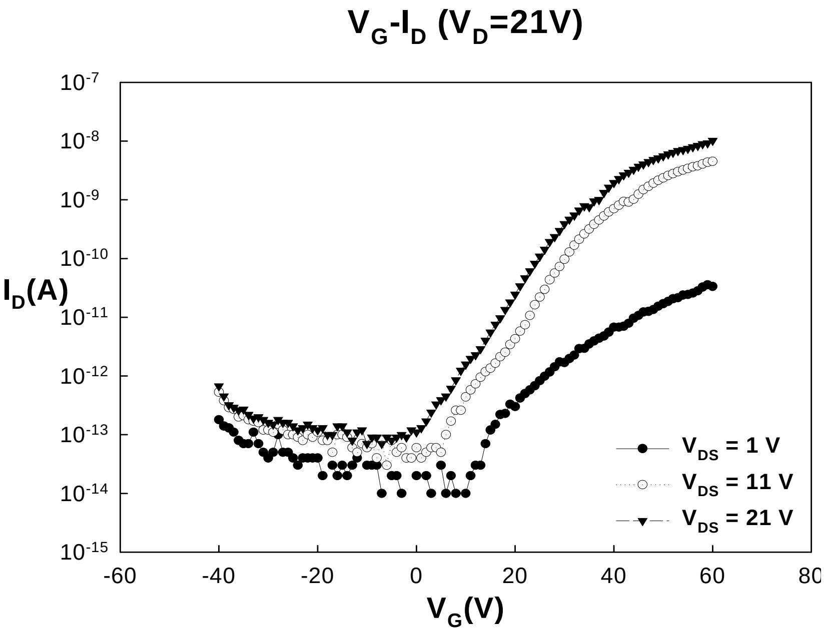


Fig3-9 Transfer characteristics of ZrZnO TFTs which suffer seriously Drain Induced Barrier Lowering effect (DIBL)

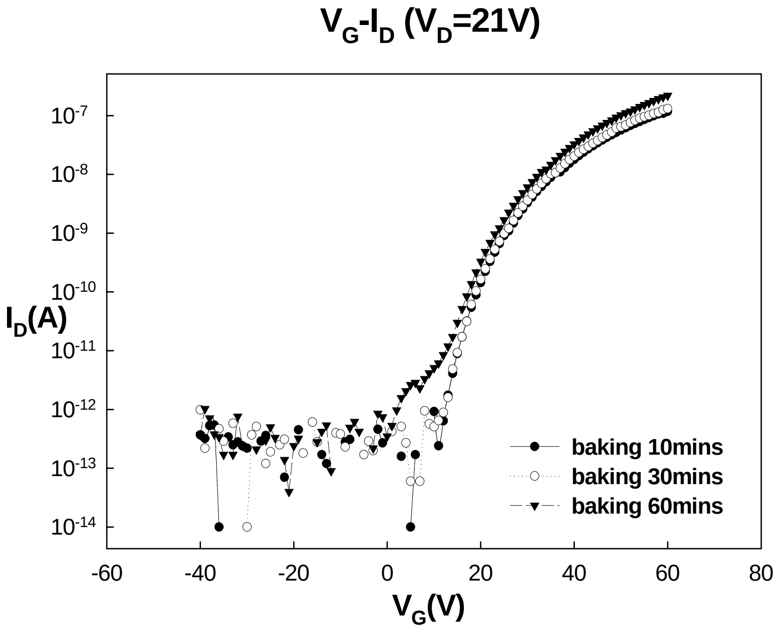
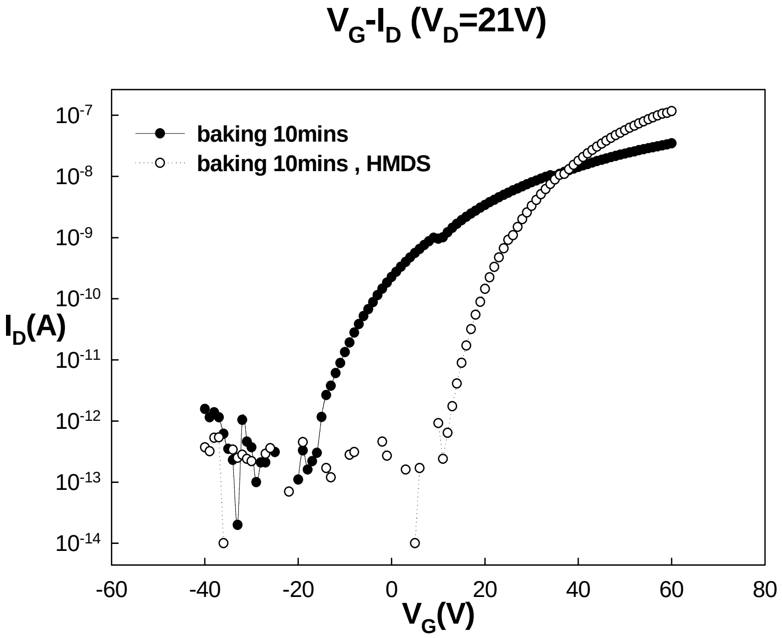
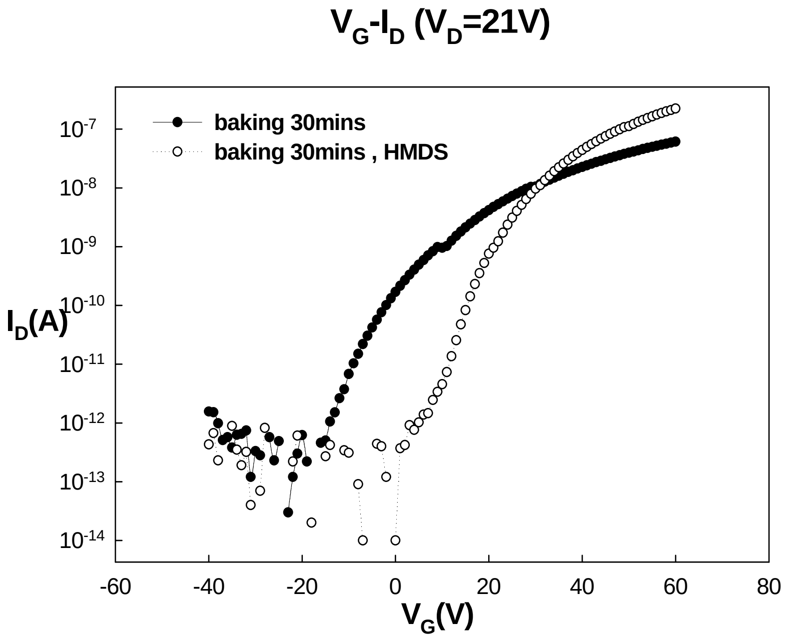


Fig3-10 Transfer characteristics of ZrZnO TFTs with HMDS coating baked for various time



<u>Fig3-11</u> Transfer characteristics of ZrZnO TFTs that are baked for 10 minutes with or without HMDS coating



<u>Fig3-12</u> Transfer characteristics of ZrZnO TFTs that are baked for 30 minutes with or without HMDS coating

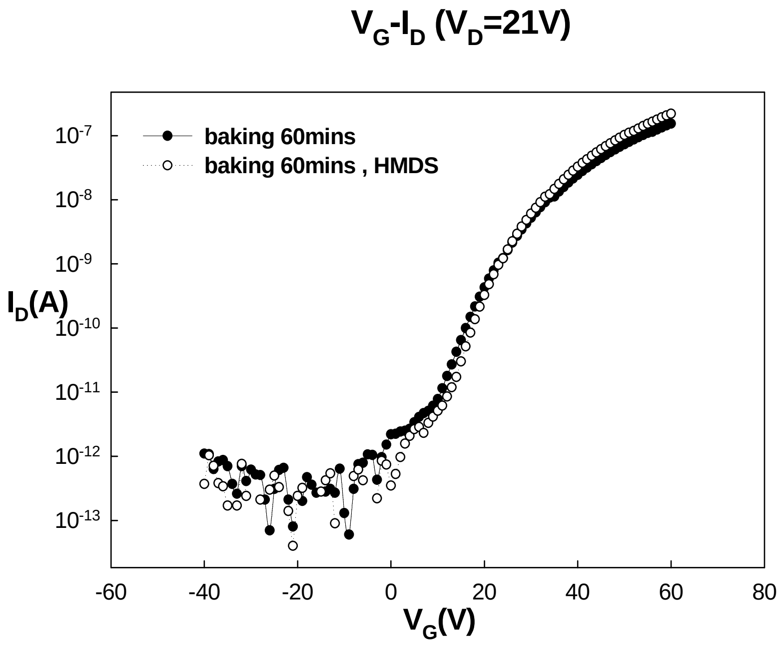


Fig3-13 Transfer characteristics of ZrZnO TFTs that are baked for 60 minutes with or without HMDS coating

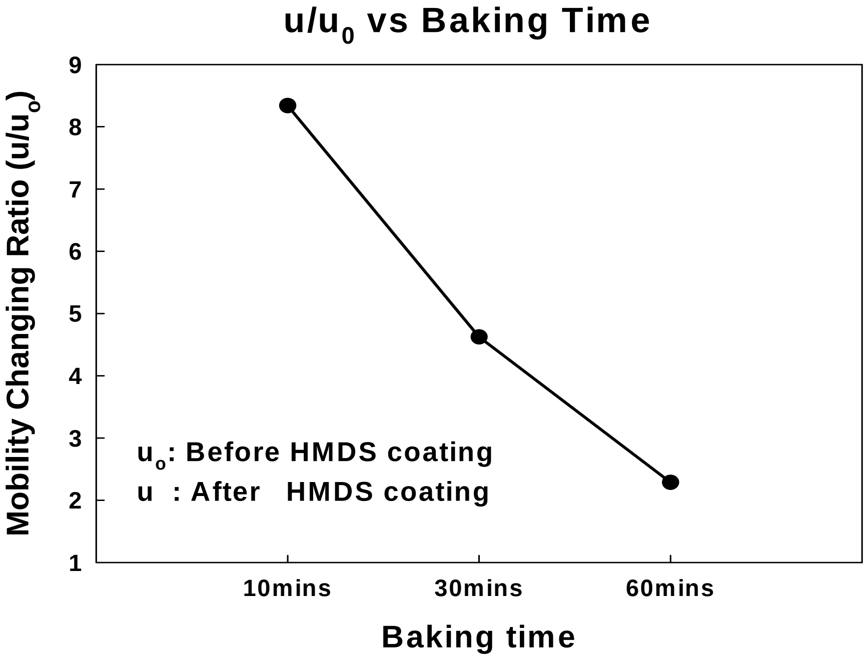


Fig3-14 Mobility changing ratio with various baking time

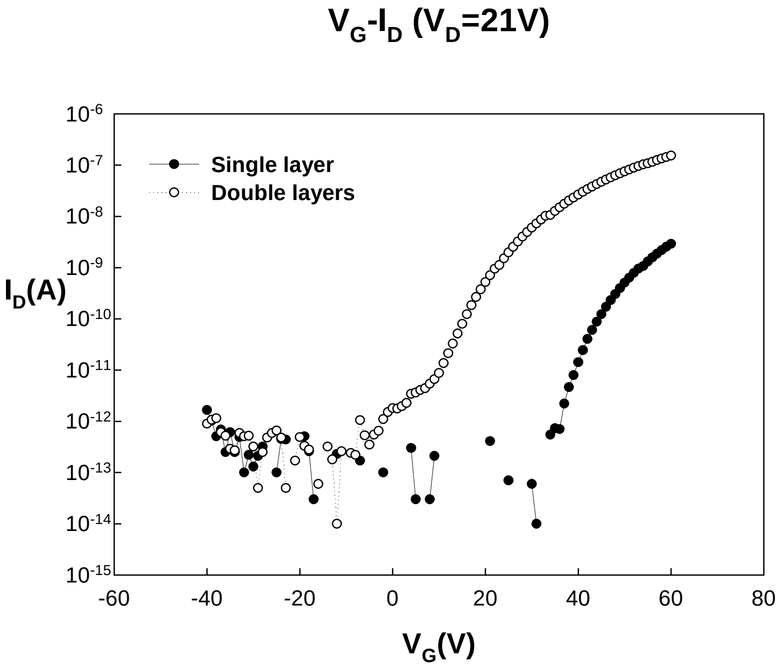


Fig3-15 Transfer characteristics of ZrZnO TFTs with different numbers of active layers

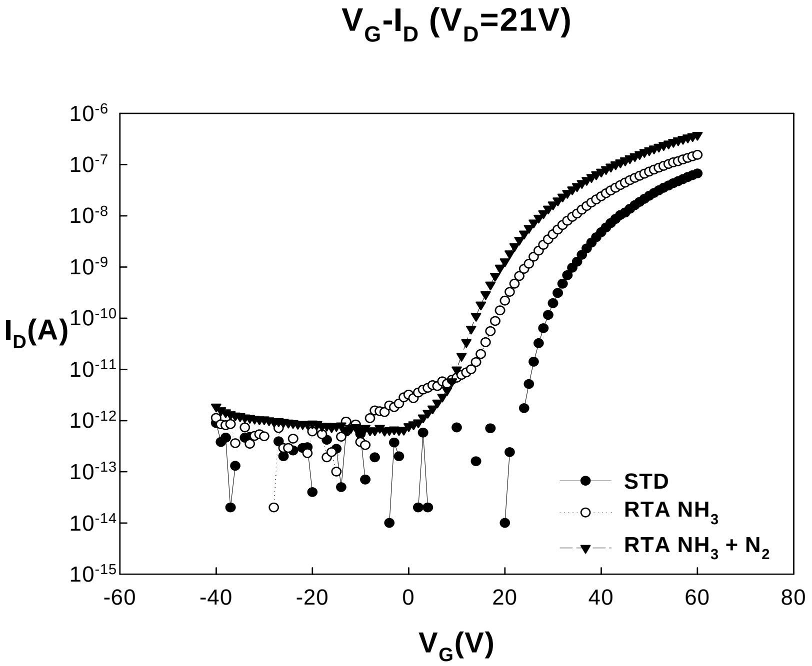


Fig3-16 Transfer characteristics of ZrZnO TFTs that are treated with RTA under NH3 ambience

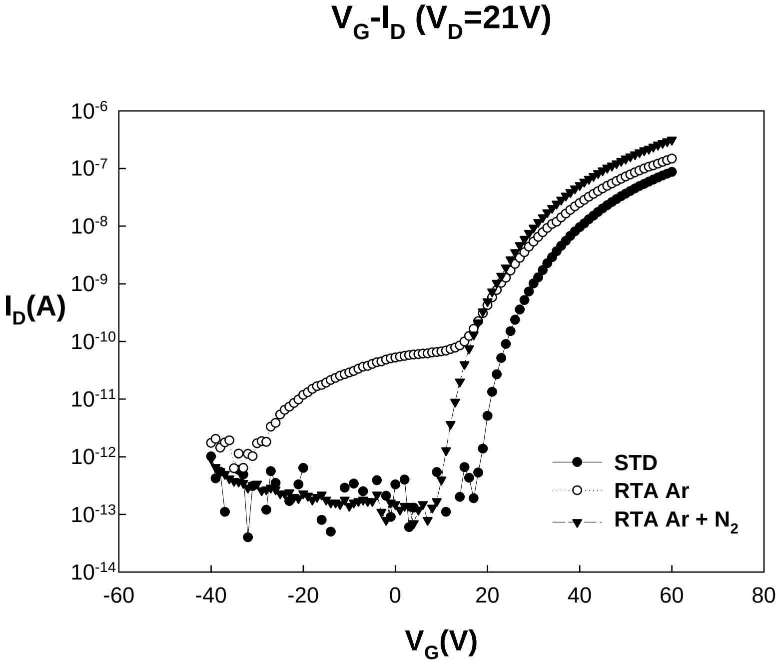


Fig3-17 Transfer characteristics of ZrZnO TFTs that are treated with RTA under Ar ambience

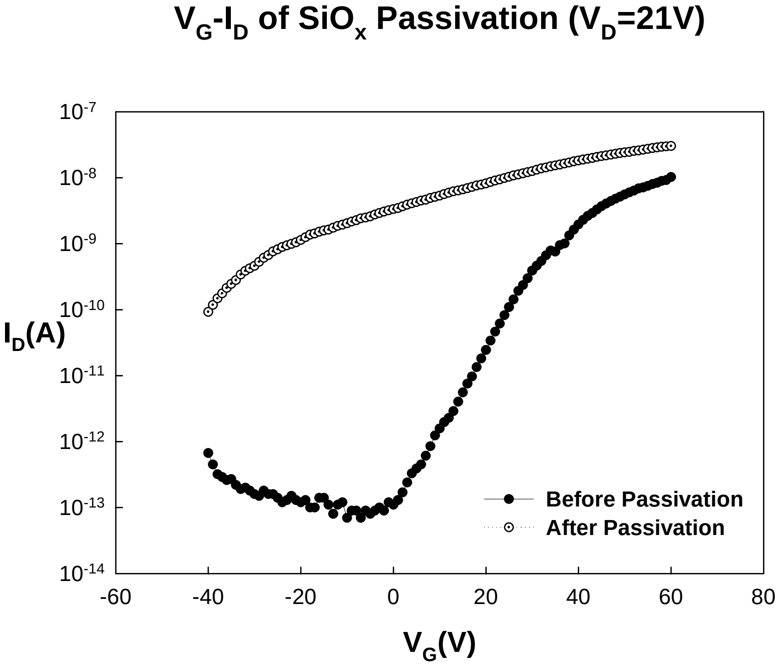


Fig3-18 Transfer characteristics of ZrZnO TFTs before and after SiOx passivation

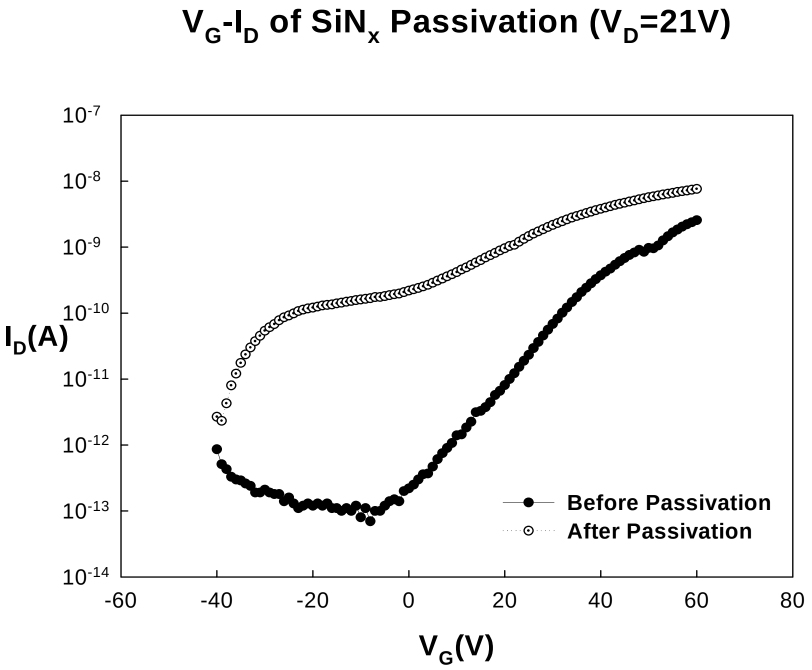


Fig3-19 Transfer characteristics of ZrZnO TFTs before and after SiNx passivation

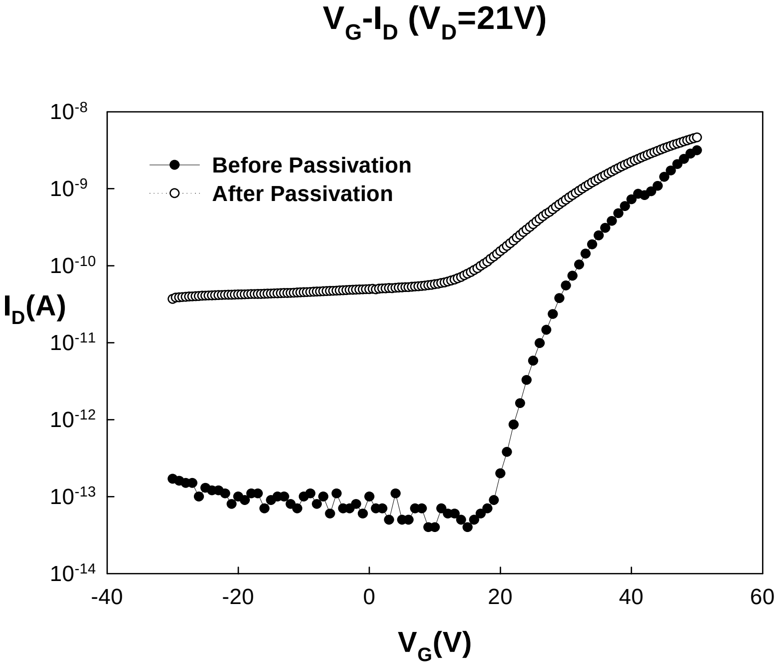


Fig3-20 Transfer characteristics of ZrZnO TFTs before and after PC403 passivation

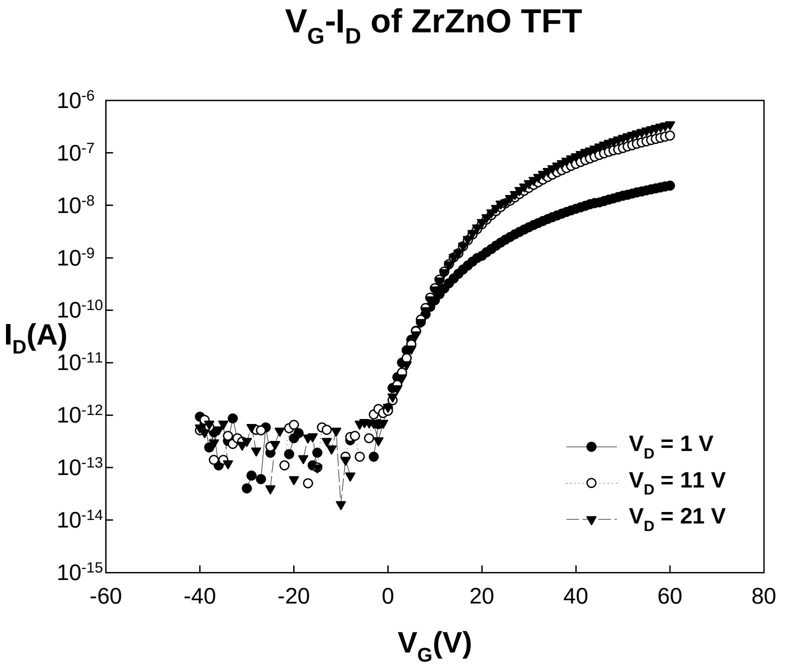


Fig3-21 Transfer characteristics of ZrZnO TFTs that are fabricated by the optimal conditions

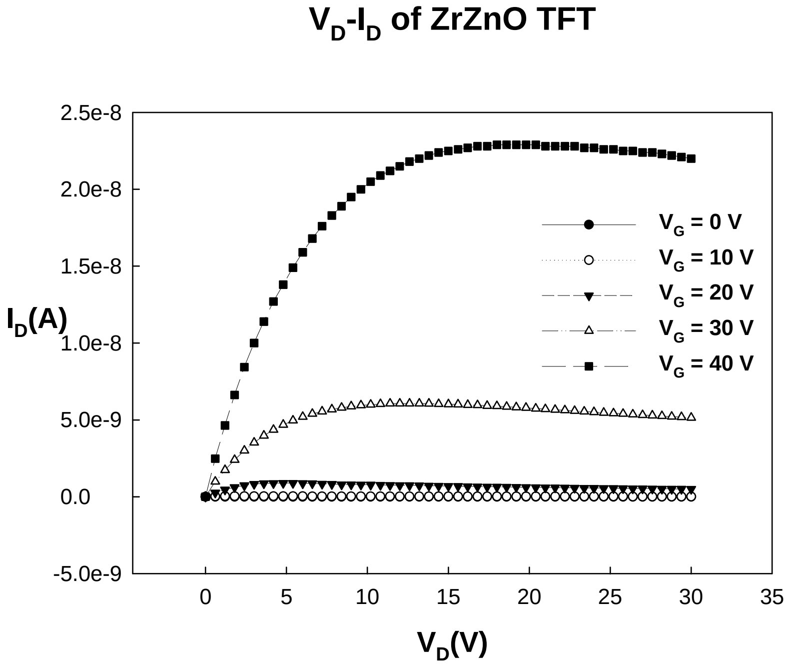


Fig3-22 I_D-V_D of ZrZnO TFTs that are fabricated by the optimal conditions

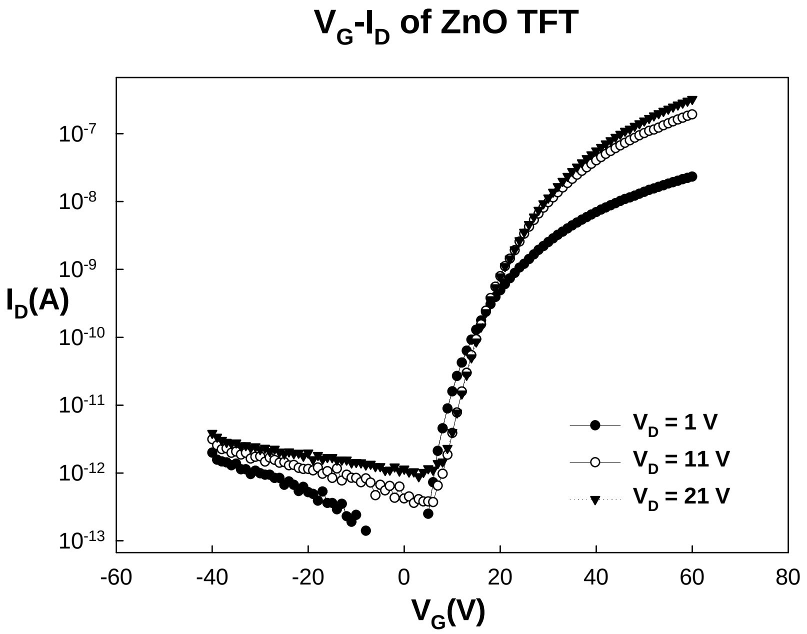


Fig3-23 Transfer characteristics of ZnO TFTs that are fabricated by the optimal conditions acquired from ZrZnO TFTs

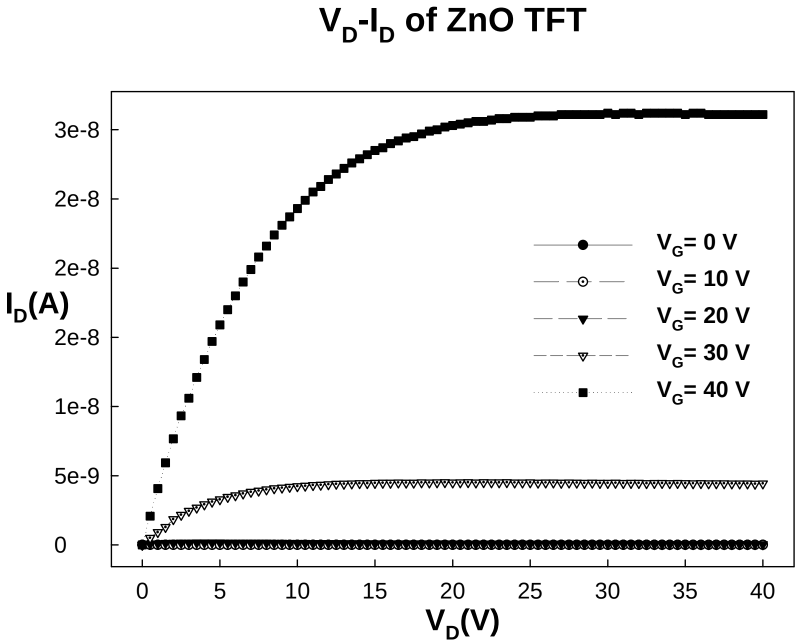


Fig3-24 I_D-V_D of ZnO TFTs that are fabricated by the optimal conditions acquired from ZrZnO TFTs

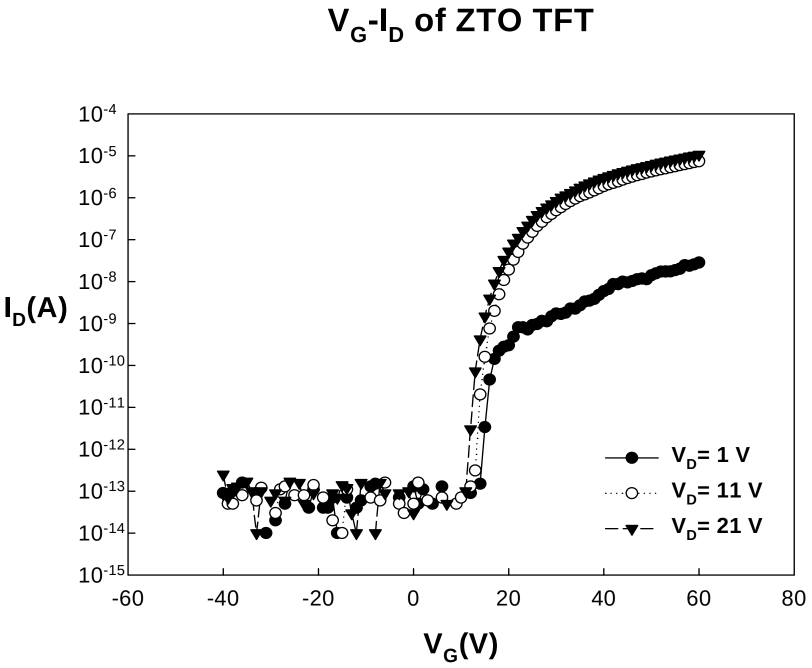


Fig3-25 Transfer characteristics of ZTO TFTs

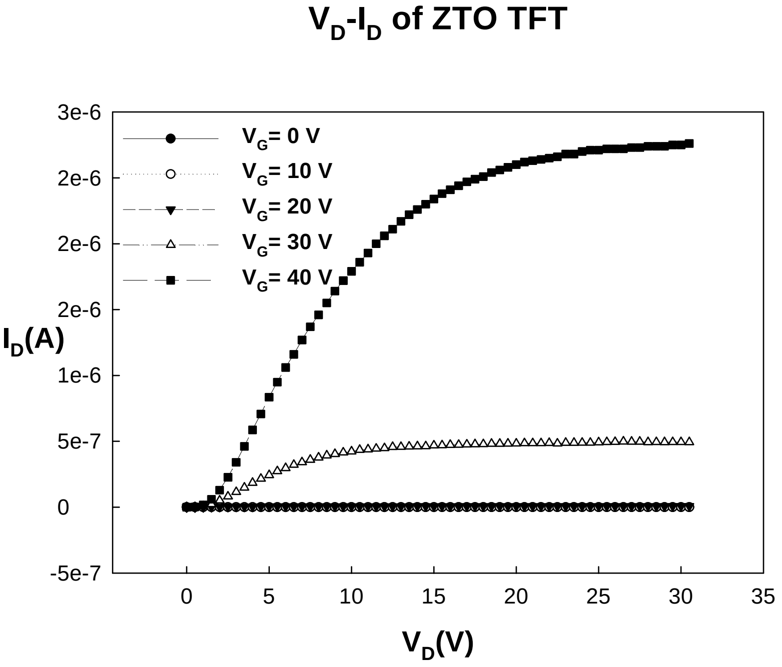


Fig3-26 I_D-V_D of ZTO TFTs

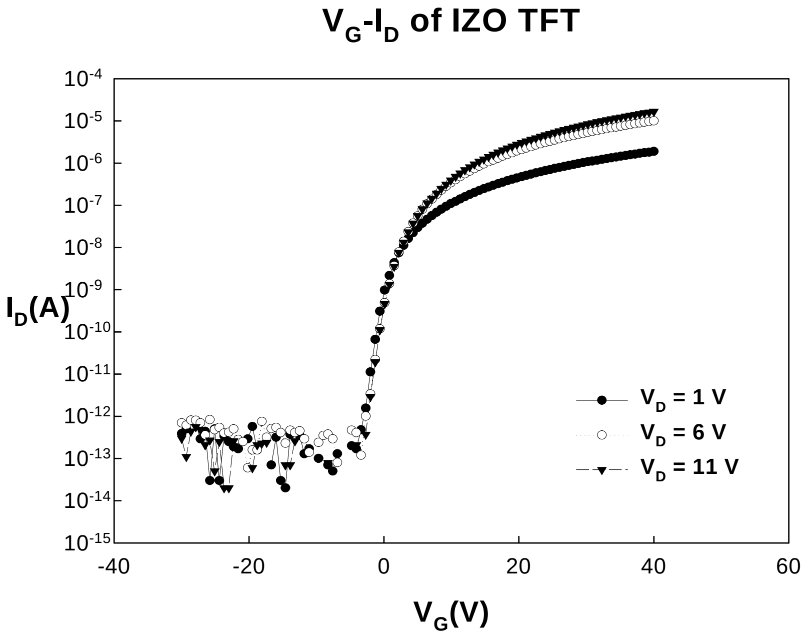


Fig3-27 Transfer characteristics of IZO TFTs

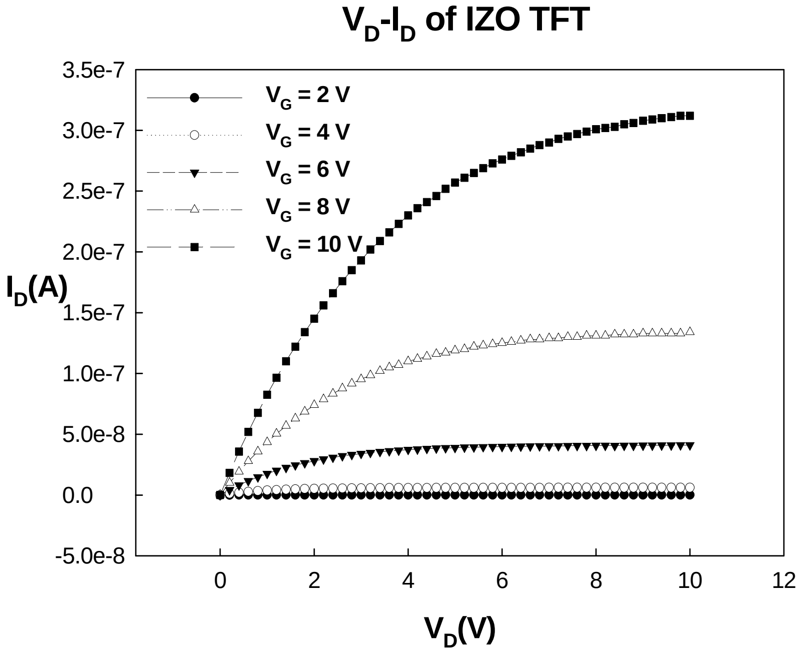


Fig3-28 I_D-V_D of ZTO TFTs

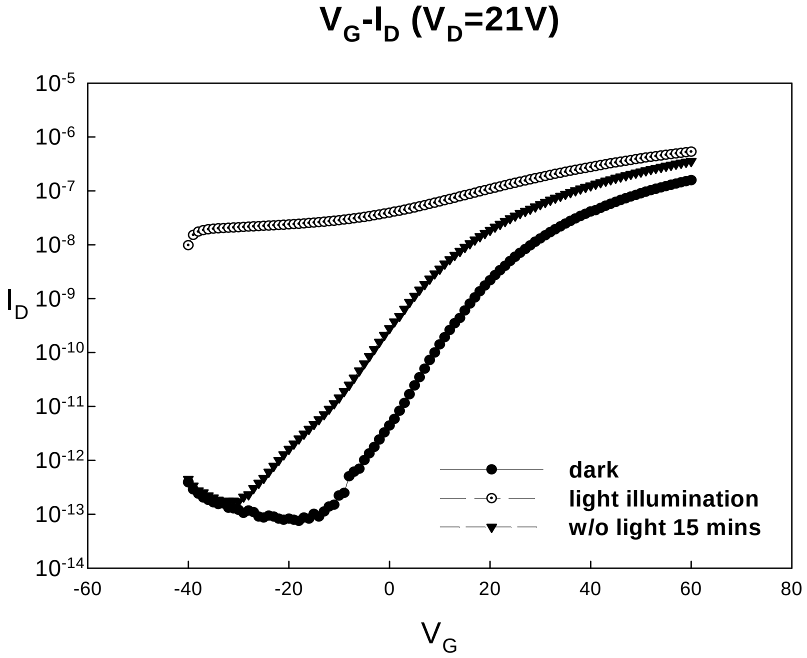


Fig4-1 Transfer characteristics of ZrZnO TFTs with light illumination and hold for 15 minute in dark environment

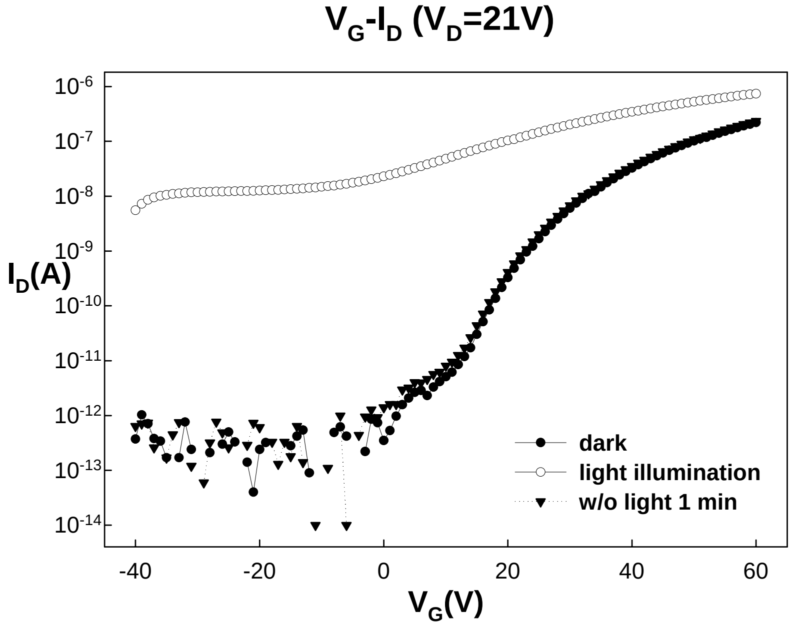


Fig4-2 Transfer characteristics of ZrZnO TFTs that are annealed under nitrogen with light illumination and hold for 1 minute in dark environment

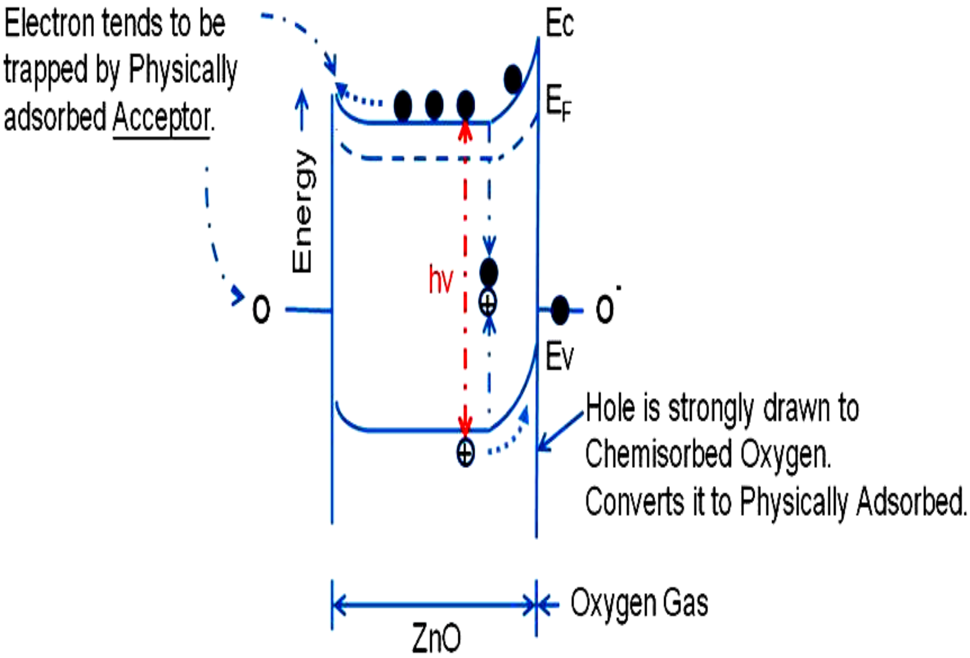


Fig4-3 Physical model of oxygen effect on the conductance of ZnO film and the interaction with light

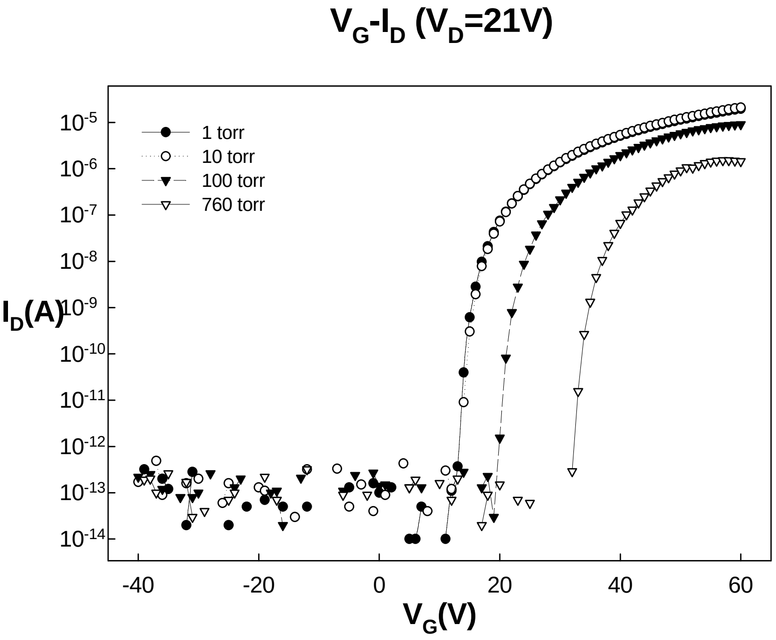


Fig4-4 Transfer characteristics of ZTO TFTs that are measured under different oxygen pressure

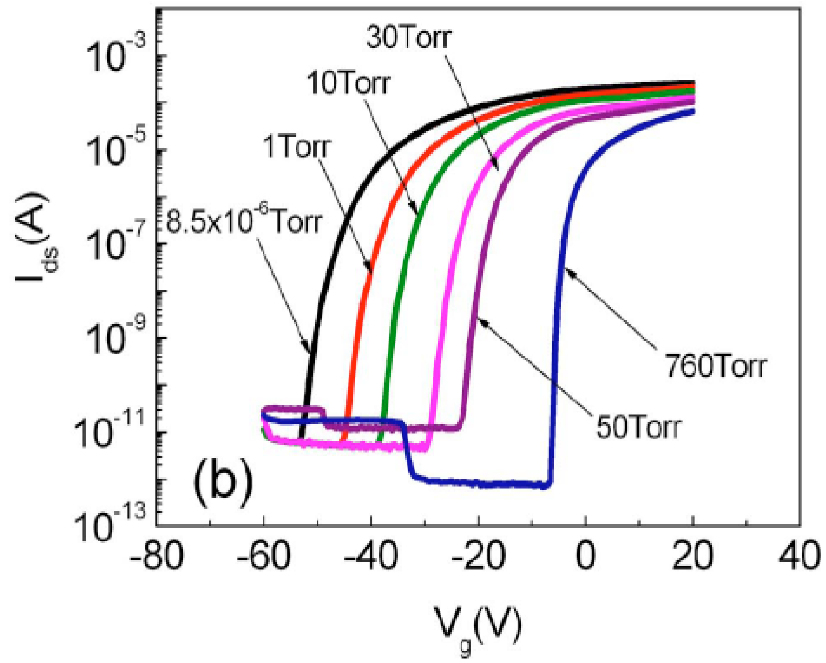


Fig4-5 Transfer characteristics of IGZO TFTs that are measured under different oxygen pressure

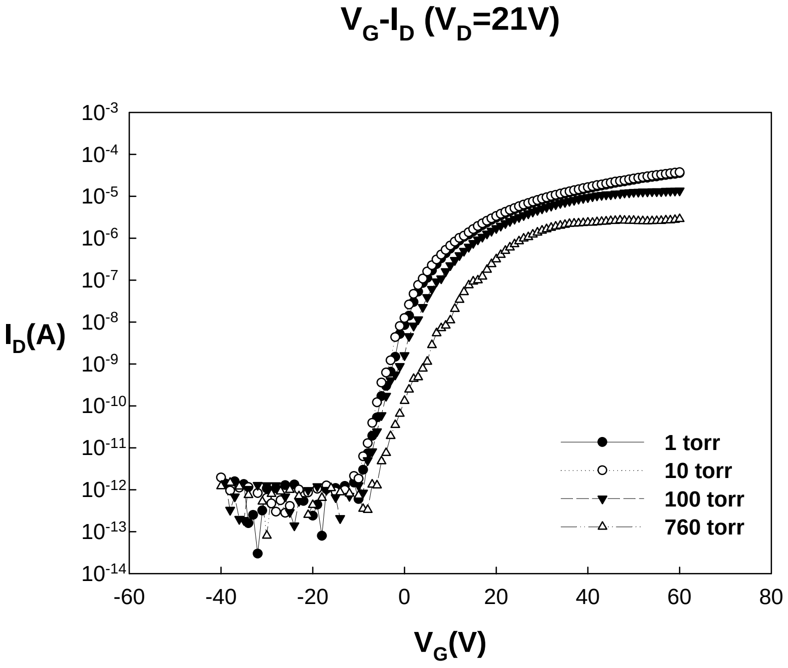


Fig4-6 Transfer characteristics of ZTO TFTs with light illumination that are measured under different oxygen pressure

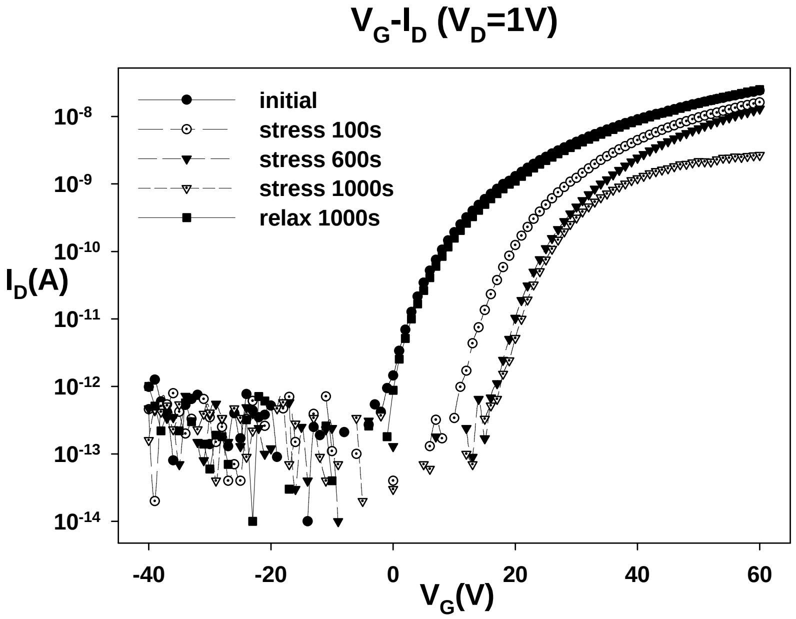


Fig4-7 Transfer characteristics of ZrZnO TFTs under gate bias stress for 1000s and after relax for 1000s at room pressure

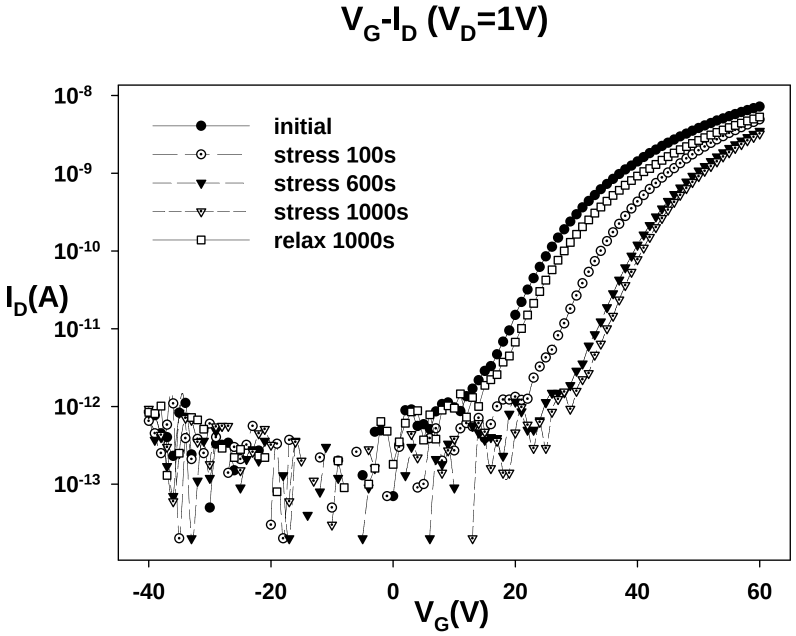


Fig4-8 Transfer characteristics of ZrZnO TFTs under gate bias stress for 1000s and after relax for 1000s in vacuum

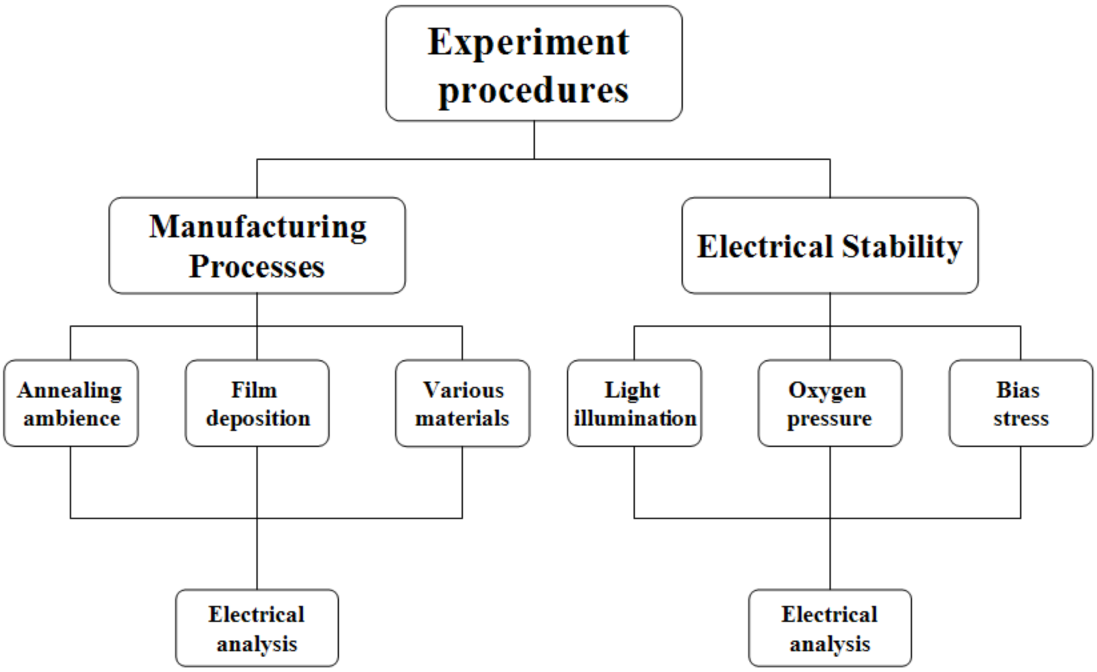


Table2-1 Experiment flow of in this experiment

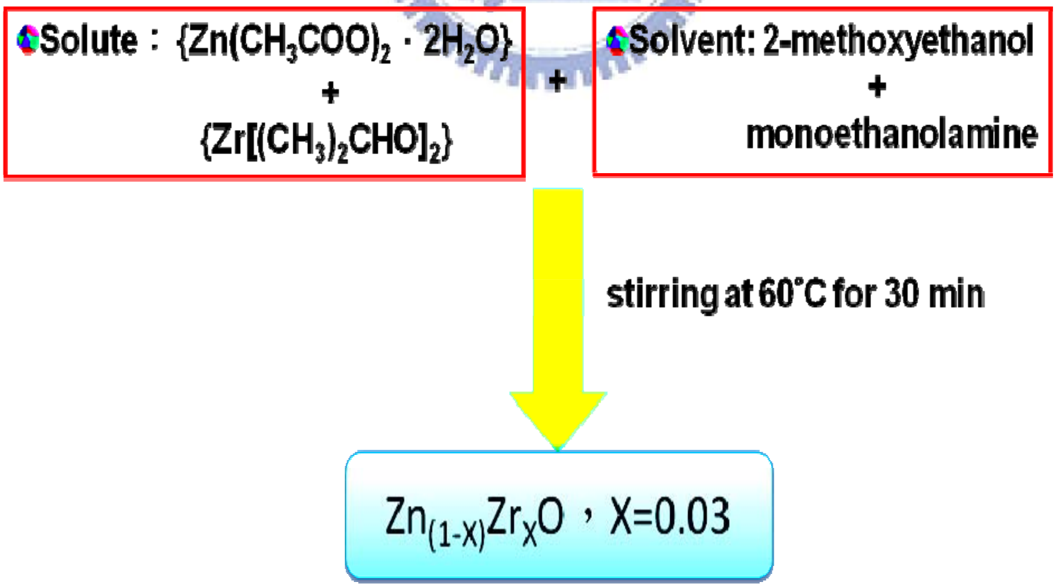


Table2-2 Experiment flow of sol-gel precursor preparation

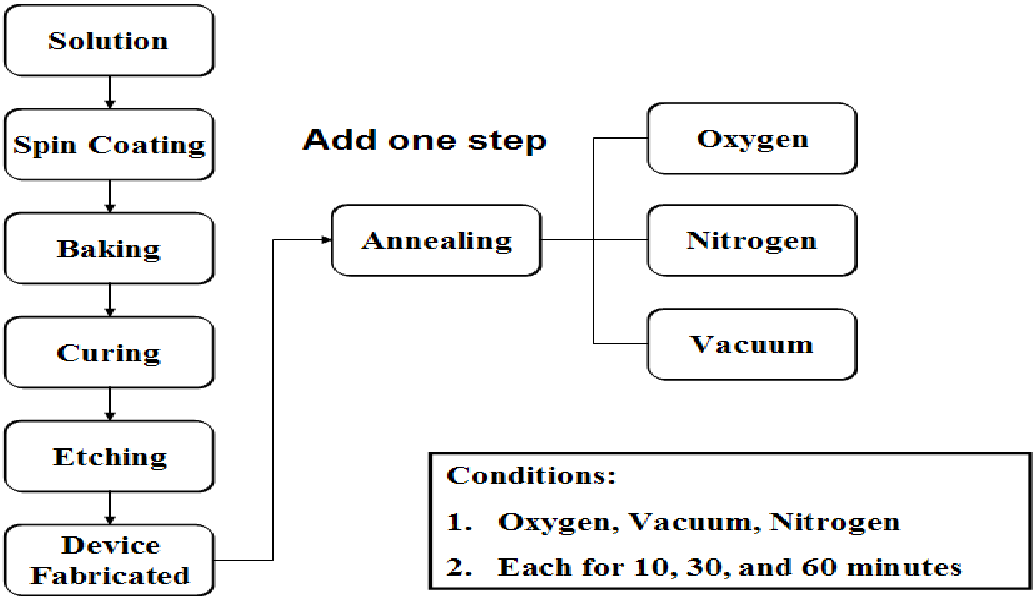


Table2-3 Experiment flow of various ambience and treatment time

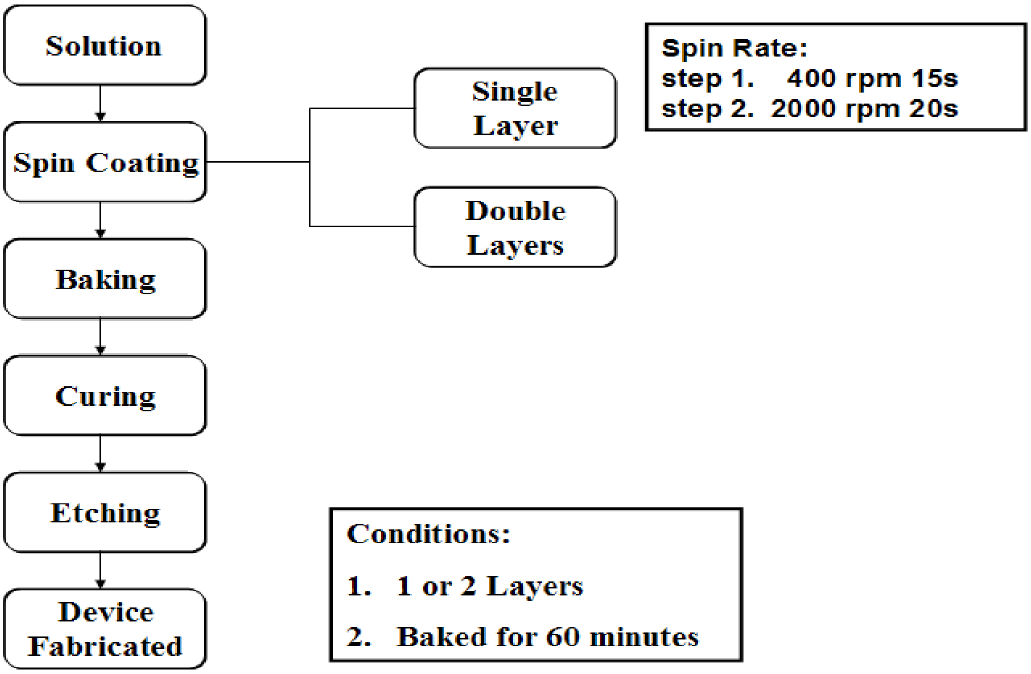


Table2-4 Experiment flow of various numbers of active channel layer

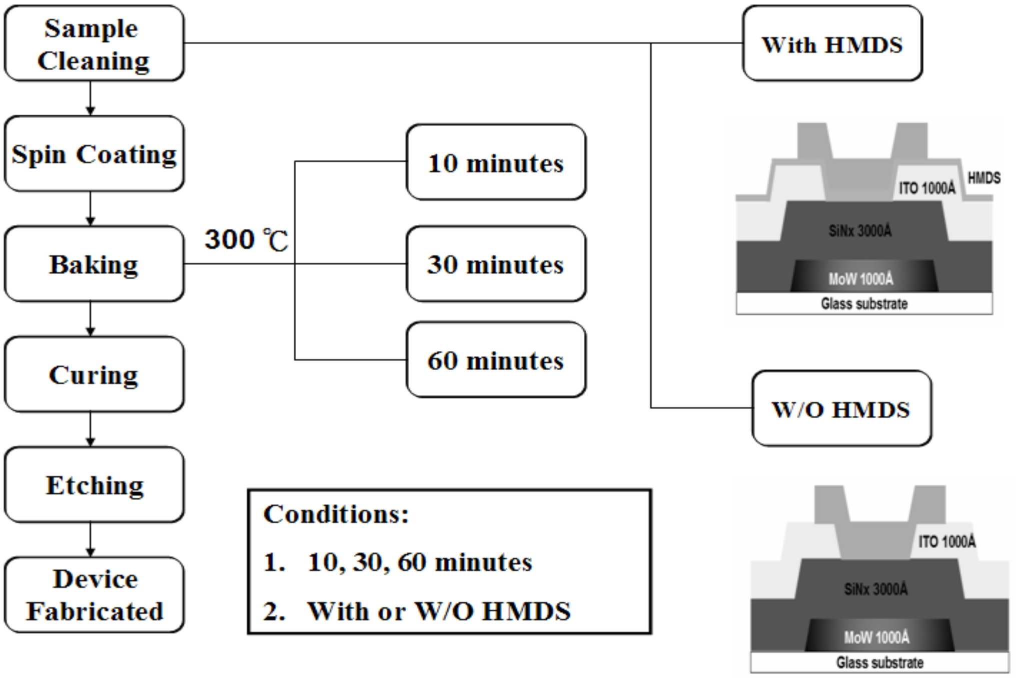


Table2-5 Experiment flow of various baking time and with or w/o HMDS coating

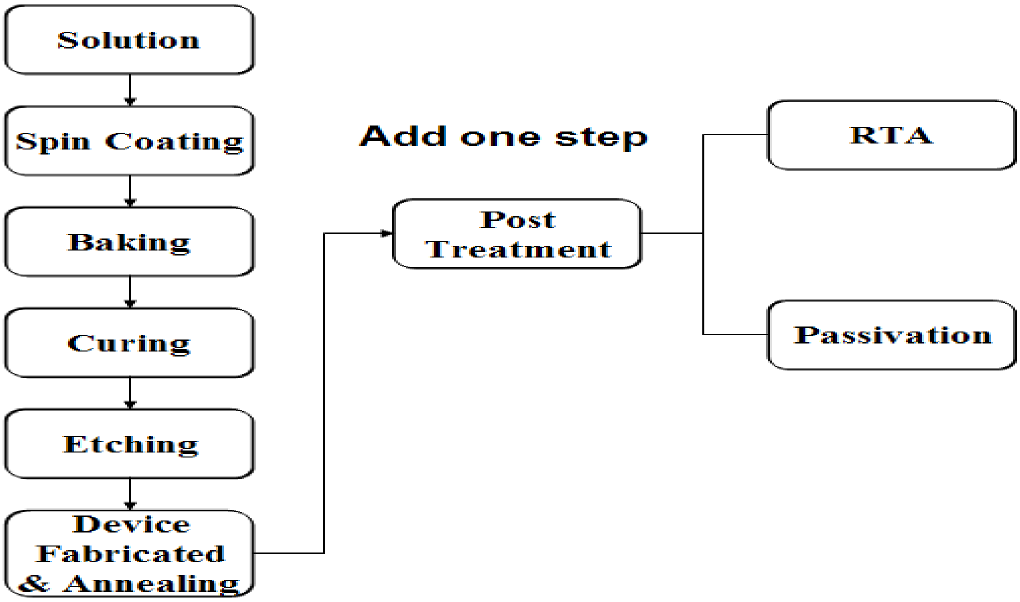
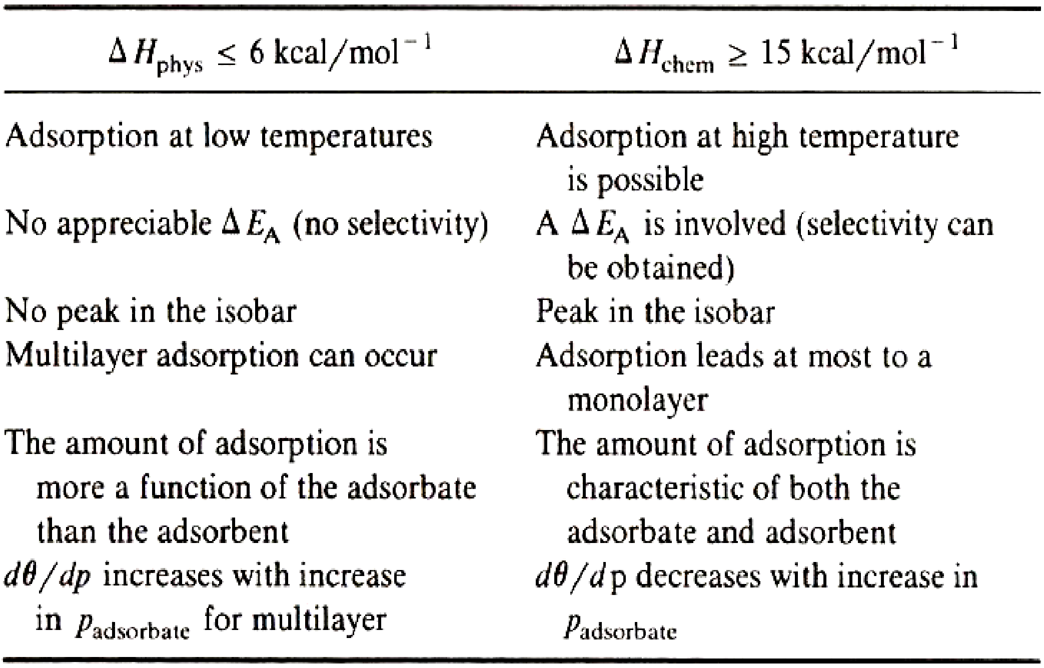
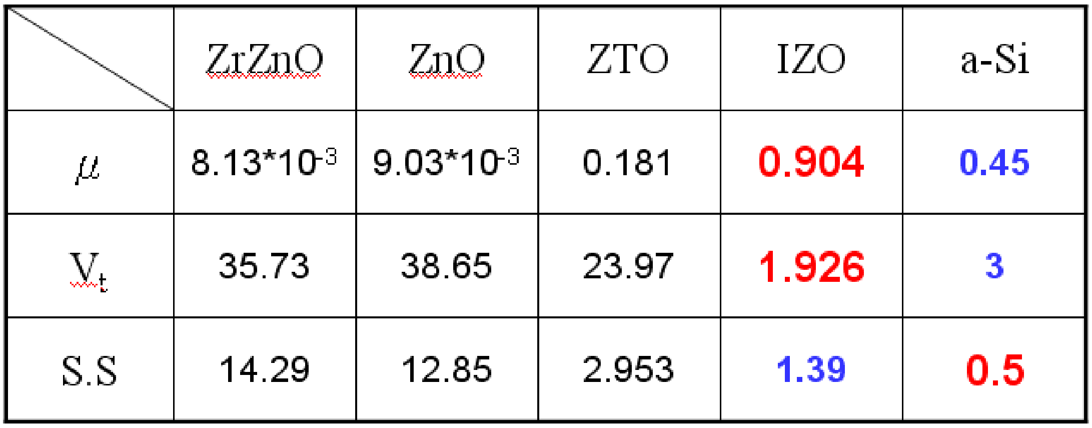


Table2-6 Experiment flow of various RTA and passivation processes



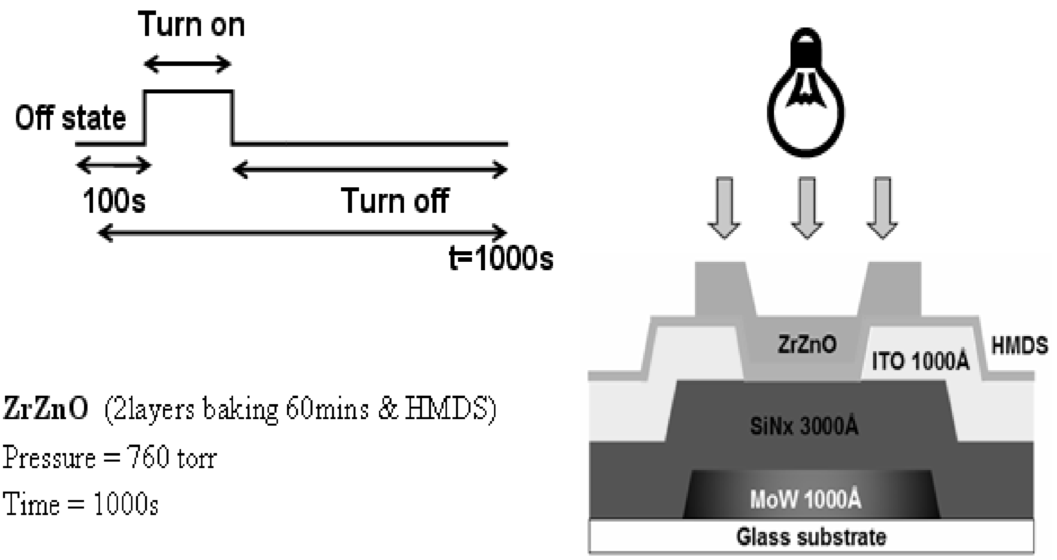
$\Delta H_{phys} \leq 6$ kcal/mol^{-1}	$\Delta H_{chem} \geq 15$ kcal/mol^{-1}
Adsorption at low temperatures	Adsorption at high temperature is possible
No appreciable ΔE_A (no selectivity)	A ΔE_A is involved (selectivity can be obtained)
No peak in the isobar	Peak in the isobar
Multilayer adsorption can occur	Adsorption leads at most to a monolayer
The amount of adsorption is more a function of the adsorbate than the adsorbent	The amount of adsorption is characteristic of both the adsorbate and adsorbent
$d\theta/dp$ increases with increase in $p_{adsorbate}$ for multilayer	$d\theta/dp$ decreases with increase in $p_{adsorbate}$

Table3-1 The characteristics of physisorption and chemisorption



	ZrZnO	ZnO	ZTO	IZO	a-Si
μ	$8.13*10^{-3}$	$9.03*10^{-3}$	0.181	0.904	0.45
V_t	35.73	38.65	23.97	1.926	3
S.S	14.29	12.85	2.953	1.39	0.5

Table3-2 The electrical parameters of various TFTs



ZrZnO (2layers baking 60mins & HMDS)
Pressure = 760 torr
Time = 1000s

Table4-1 Experiment flow of devices under light illumination

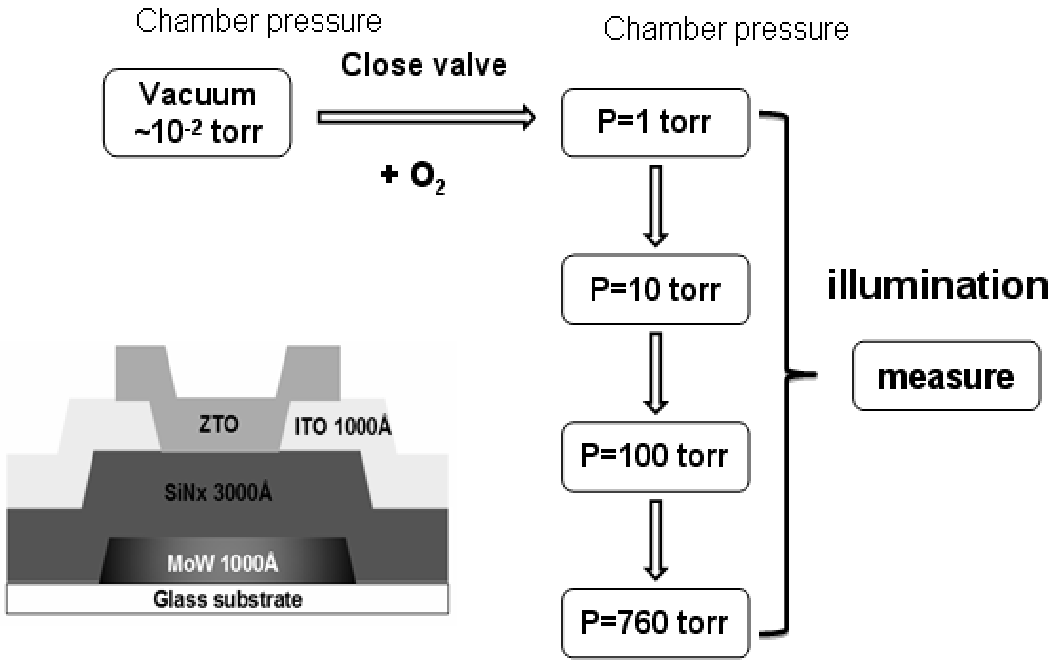
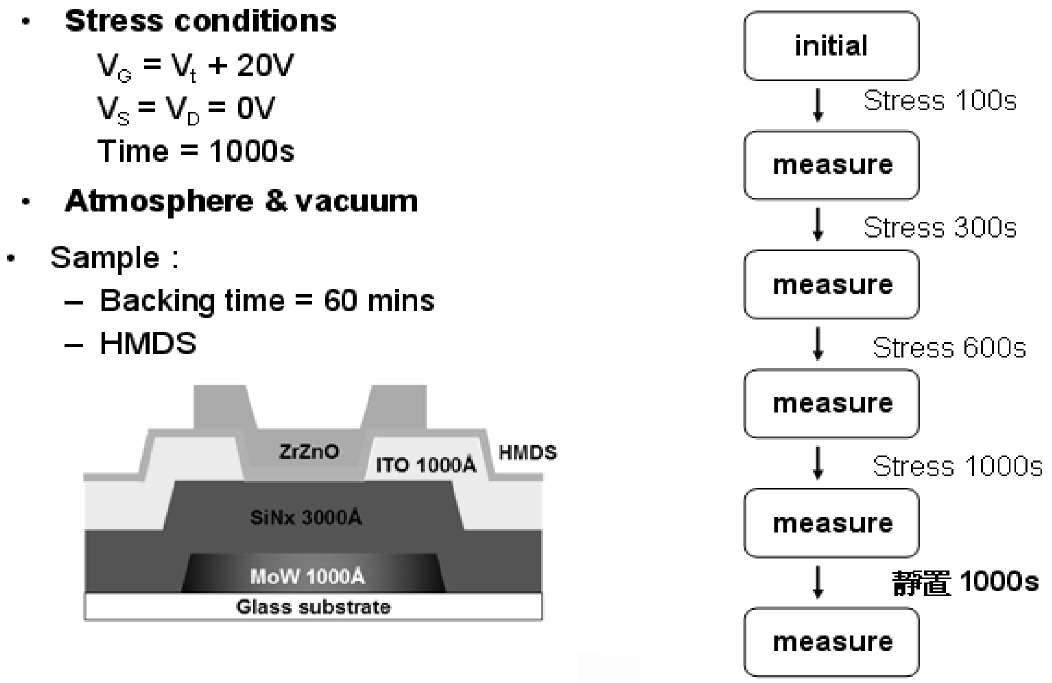


Table4-2 Experiment flow of devices measured under different oxygen

pressure



- **Stress conditions**
  $V_G = V_t + 20V$
  $V_S = V_D = 0V$
  Time = 1000s
- **Atmosphere & vacuum**
- Sample :
  - Backing time = 60 mins
  - HMDS

Table4-3 Experiment flow of devices measured under gate bias stress

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碩士論文題目:

溶膠凝膠金屬氧化物薄膜電晶體之研究

Investigation on Sol-Gel Derived Metal Oxide Semiconductor Thin Film Transistors