國立交通大學

光電工程學系顯示科技研究所碩士班

碩士論文

可撓式非晶矽薄膜電晶體之
可靠度探討與電性分析

Study on Reliability Analysis for
Flexible Amorphous Silicon Thin-Film Transistor

研 究 生 ： 蔡尚祐　　Shang-Yao Tsai

指導教授 ： 劉柏村 博士　　Dr. Po-Tsun Liu

中 華 民 國　九十七 年 六 月

可撓式非晶矽薄膜電晶體之

可靠度探討與電性分析

Study on Reliability Analysis for

Flexible Amorphous Silicon Thin-Film Transistor

研 究 生：蔡尚祐　　Student：Shang-Yao Tsai

指導教授：劉柏村 博士　　Advisor：Dr. Po-Tsun Liu

國 立 交 通 大 學

顯 示 科 技 研 究 所

碩 士 論 文

A Thesis

Submitted to Department of Photonics and Display Institute

College of Electrical and Computer Engineering

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master

in

Photonics

June 2008

Hsinchu, Taiwan, Republic of China

中 華 民 國 九十七 年 六 月

可撓式非晶矽薄膜電晶體之

可靠度探討與電性分析

研究生: 蔡尚祐　　指導教授: 劉柏村博士

國立交通大學

光電工程學系顯示科技研究所

中文摘要

可撓式主動式矩陣顯示器(Flexible active-matrix display)技術近年來已逐漸成為全球面板業界的發展主力，因為其輕薄、可撓性、和耐壓等諸多性質，使得一些可攜帶式電子產品，如電子書(e-book)、電子報紙(e-paper)、個人數位助理(PDA)等應用有了突破性的發展。為了提升可撓式顯示器的製程技術，了解薄膜電晶體處於應力彎曲狀態下的電性表現改變是不可或缺的研究關鍵。在本研究中，我們首先在一個利用不鏽鋼薄片基板處於190℃低溫下製程的可撓式非晶矽薄膜電晶體(amorphous-Si TFT)元件，探討了元件在受到拉伸(tensile)或壓縮(compressive)應力時電性上以及可靠度方面的改變。研究結果顯示，非晶矽薄膜電晶體第一次受到應力撓曲時會有相較於之後進行多次撓曲測試之下最明顯且無法回復的劣化情形發生，尤其是壓縮應力的施加會有最嚴重的影響，不管是基本電性表

現還是在可靠度上都有相當一致的結果。我們也做了處於撓曲狀態下寄生電阻與活化能的參數萃取分析，證明了應力撓曲所造成的劣化效應與寄生電阻無關以及從活化能的改變上進一步地解釋了電子遷移率和臨界電壓的劣化情形。這些對於元件在受到應力撓曲下的量測分析結果，對於將來在製造可撓式電子產品的設計考量上有了明顯的助益。

其次，在一般業界的非晶矽薄膜電晶體製程中，在完整的電晶體主結構完成後會作氮化矽(SiNx)保護層的覆蓋動作以及300~350℃的退火處理，我們依據此標準製程並將退火溫度修正為適用於軟性基板的溫度。結果顯示，我們在低於200℃之下所作的氮化矽覆蓋步驟以及退火處理，同樣成功地改善元件在撓曲下的特性表現。此方法可應用於改善不同軟性基板元件，如塑膠、有機高分子等不耐高溫製程之材料。

Study on Reliability Analysis for Flexible Amorphous Silicon Thin-Film Transistor

Student : Shang-Yao Tsai Advisor : Dr. Po-Tsun Liu

National Chiao-Tung University

Department of Photonics and Display Institute

Abstract

The application of flexible active-matrix display has become most promising technology in the whole wide world display industry recent years. Due to the properties such as light-weighted, flexible, and durable, there are some remarkable advances in portable electronic products like e-book, e-paper, and personal digital assistant (PDA). It is necessary to understand the effect of the mechanical strain applied on the TFT device in order to promote the flexible display panels manufacturing technology. In this thesis, we investigate the electrical performance and reliability under tensile and compressive strain by using an a-Si TFT fabricated on the stainless steel foils at 190℃ PEVCD. The result of the analysis shows there is the most obvious and irrecoverable degradation for the first-time bending stress test, especially under the compressive strain. We have

consistent experimental results both on electrical performance and reliability. We also prove the degrading mechanism is independent of the effect of parasitical resistance and explain the change of the threshold voltage and mobility by activation energy extraction under mechanical strain. From these measuring analysis while the TFT device is bent, there will be a great benefit to the design and fabrication of flexible displays.

In addition, there is a standard a-Si TFT fabrication in industry which is the silicon nitride passivating and post-annealing process under 300 ~ 350℃. We try to follow this process and especially modify the processing temperature to the lower value, which is adapted to flexible substrates. Successfully, we improve both the electrical performance and reliability by the nitride capping and post-annealing process below 200℃. This method is believed to apply to other flexible substrates such as plastics or organic polymers, which couldn't withstand high temperature processing as general a-Si TFT fabrication.

Acknowledgements

兩年的碩士班生活轉眼間即將步入了尾聲，在這個人生中光輝而燦爛的舞台上，首先，我要感謝我的指導教授 劉柏村博士；無論是在求學還是生活上，老師都給予了我最無私的指導與關懷。總是能在學生需要幫助時提供適時的建議與精確的判斷，使總是象徵冰冷的實驗室充滿了無限的溫暖。在此，對老師致上最深的敬意。

接著我要感謝一德學長，從碩一開始的實驗訓練到碩二的論文指導，辛苦的帶領我朝著正確的研究方向前進，在我需要解答疑惑時毫不吝嗇的伸出援手，如果沒有你的幫助，這篇論文將不會這麼順利地完成。同時也感謝實驗室中一起成長的好夥伴:立煒、豫杰、阿貴、繼聖、巍方、逸立、威廷、超帥。兩年以來的互相扶持與鼓勵，陪伴我度過了每一刻的研究生涯。一起相約打球、聚餐或出遊的歡樂時光也將是珍貴而不可取代的美好回憶。還有優秀的學弟們:立峯、虛胖、維哲、智昱，你們的加入使實驗室注入了新的活力，相信接下來實驗室會因為你們而持續發光發熱。

最後我想感謝的是我最親愛的家人，不管是在我情緒低潮或是挫折的時刻，都能以最關懷的態度支持我，讓我能夠繼續堅定地朝著理想而前進。我把這篇論文獻給我的家人，沒有你們，它將不會完成。

尚祐 2008.06.14

Contents

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter1

Introduction

1-1. General Background

Overview of flat-panel displays, liquid-crystal displays (LCDs) have become the most common system in many commercial applications for recent years in the age of high technology.

For computer monitors, the choice is easy, with LCDs having won the market, but for TV the several technologies are still competing. LCD technology clearly has many advantages for the IT (Information Technology) world. Computers are the channel through which the technology emerged; it was adapted to other applications. The pixels can be made very small thanks to the lithographic process used, which is taken from the semiconductor industry. The LCD computer monitors are now a serious alternative to the bulky CRT monitors, and the LCDs are also found in almost all portable applications. Meanwhile, production of OLED (Organic Light-Emitting Diode) displays is starting up, though it is rather slow at the moment.

Contrast performance remains below that of CRT and plasma, but that's not really a problem. The real problem has to do with the depth of the blacks. As we've seen, the pixels of an LCD panel are actually light valves, and they're not perfect ones—they leak light. So even when the switch is completely off—corresponding to a subpixel that should be black—an appreciable amount of light gets through. This is naturally an area where plasma and CRT have a big advantage over LCD: with those

technologies, black really means no light at all.

With the rapid development of consuming electronics, electronic paper, personal digital assistant (PDA), global positioning system (GPS), pen-size rollable papers and portable electronic device etc. are rapidly growing interest in recent years [1.1]. Therefore, we believe that the technology of flexible TFTs will lead us to a totally new page in the history of human being.

Thin-film transistors including an active layer of amorphous silicon or polycrystalline silicon have been widely employed as the pixel-driving elements of a liquid crystal display. Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) is an mature technology nowadays and widely used as switching device in active matrix liquid crystal displays (AMLCDs).The major advantages that makes this technology been widely used are its good electronic properties such as high photoconductivity, and the ability to achieve low cost fabrication at low temperatures. For the reason of making flexible displays possible, the requirements for thin, light, portable and even flexible substrates for display system become so necessary. However, the different fabrication process requirement, electrical performance, and the product protection between flexible flat-panel displays and traditional flat-panel displays will be the greatest challenge in the future.

1-2. Overview of Flexible a-Si:H TFT

The basic physics of the a pixel can be understood by reference to Fig. 1-1, where we schematically illustrate the band-bending and the occupancy of the electronic states with a simple density of states diagram [1.2]. Essentially the localized states in the amorphous silicon can be divided into two types, tail states and deep states [1.3-1.4]. The tail states are the Si conduction band states broadened and localized by the disorder to form a "tail" of localized states just below the conduction band mobility edge. The deep states originate from defects in the amorphous silicon network. These are thought to mostly consist of Si dangling bonds, which have a wide range of energies because of the variations in local environments. At zero gate volts the energy bands are close to the flat-band condition. For positive gate volts, less than the threshold voltage, the energy bands bend downward and the Fermi level moves through the deep states, which are then occupied. At the same time, some space charge is located in the band-tail states, but the occupancy of these states is low, since they are well above the Fermi level and so the total space charge is dominated by the deep states. The increase in source-drain current is due to the small fraction of the band-tail electrons above the conduction band mobility edge. The space charge in the deep states increases in proportion to the increase in gate voltage, but the current increases exponentially, as the band-bending increases. If the density of deep states between the Fermi level and the tail states were constant, then the pre-threshold slope in the logarithmic transfer characteristic would be roughly inversely proportional to the square root of the density of states. Above the threshold voltage, the space charge in the band-tail states

exceeds the space charge in the deep states, even though the Fermi level is still below the tail states. Now, both the total space charge and the source drain current increase linearly with the applied gate voltage and we have a well defined field-effect mobility. The mobility is thermally activated with an activation energy given by the width of the tail states, not by E_C - E_F. The transfer characteristics can be modeled from the density of states or, conversely, the density of states can be determined from an analysis of the transfer characteristic by solving Poisson's equation for the space-charge region [1.5-1.7]. Fig. 1-2 shows the field-effect density of states for undoped amorphous silicon, which is consistent with the characteristics of transistors made in laboratory. The Fermi level is near a region where the density of states is decreasing, which leads to a strong statistical shift [1.8]

Generally speaking, there are two main choices for substrates of the flexible TFT, which include metal foil and plastic. Since the flexible substrate represents the fundamental starting component for display, flexible substrates arguably face the greatest challenges in terms of compatibility with all of the other necessary display layers that need to be integrated onto them. Temperature is the most critical factor for polyimide substrate which can only tolerate below 200℃ [1.9-1.11]. A number of issues are discussed such as process temperature limitations as a function of polymer type, optical properties, thermal properties, and surface smoothness properties.

Some studies claimed the successful fabrication of TFTs device on polyimide substrates [1.12-1.13], but such materials suffered from

appearing yellow in optical transmission and the permeability to water. Therefore, these make polyimide substrates not suitable for display application. These fundamental requirements for such flexible substrates include chemical stability, unbreakable, insensitivity to environment and low coefficient of thermal expansion (comparable to that of the material in conventional TFT structure). Besides polyimide substrate, thin stainless steel foil substrates are also candidates where substrate flexibility are required, while steel foil material have better chemical and can be suitable for the full temperature range of TFT fabrication without changing the conventional TFT fabrication.

1-3. Reviews on DC Bias Stress

In order to make a-Si TFTs suitable for advanced circuits, besides the improvement of performance of a-Si TFTs, the improvement of reliability is also significant. Consequently, reliability testing and analysis of reliability mechanisms become more and more necessary.

The most important instability in a-Si TFTs is the shift of threshold voltage caused by a prolonged application of gate bias stress. The threshold voltage shift will limit the use of the devices in some demanding applications and has been reasonably heeded. Many reports indicate that there are two sources degrading the transfer characteristics of a-Si TFTs: charge trapping and defect state creation [1.14-1.15]. The defect state creation associates with the breaking of Si-Si weak bonds in the a-Si layer and at the a-Si/SiNx interface as well as increasing the density of defect states [1.16]. The charge trapping relates to trap sites in the silicon nitride gate insulator. Generally, the defect state creation in the fast state is dominant at lower electric fields, and in contrast, the charge trapping in the slow state is dominant at higher electric fields.

For defect state creation, while the device is stressed by gate voltage, it will produce additional deep states in the a-Si layer. Afterward we apply a positive voltage, which makes band-bending and electrons accumulated at the a-Si/SiNx interface, on gate. When Fermi level moves up, we will need larger gate voltage to provide additional electrons for filling acceptor-like states (So that the threshold voltage shows the right shift). In contrast, applying a negative voltage makes holes accumulated at the interface. When Fermi level moves down, we will need more negative voltage to fill donor-like states with additional holes (So that the

threshold voltage shows the left shift). The quantity of threshold voltage shift is dependent on the induced acceptor-like states or donor-like states after the gate voltage bias stress.

For charge trapping, if we apply a prolonged positive gate voltage stress on devices, it will cause the negative charges being trapped in the nitride layer. In consequence, we need provide additional positive gate voltage in order to counterweigh the effect of negative charges trapping in the silicon nitride if the device is operated under positive gate voltage (So that the threshold voltage shows the right shift). However, when the device is operated under negative gate voltage, the trapping negative charges are equal to providing a negative gate voltage first. In this case the device will turn on earlier (So that the threshold voltage shows the right shift). Of course that we will have a reverse result if applying a prolonged negative gate voltage stress in the beginning.

Powell first noticed the distinction between defect state creation and charge trapping in 1987 by experimenting with ambipolar TFTs. He determined that state creation is characterized by a power law time dependence and affected by temperature. On the other hand, charge trapping has a logarithmic time dependence and is independent of temperature.

1-4. Motivation

As the mention in Introduction, different electrical performance between flexible flat-panel displays and traditional flat-panel displays will be one of the most important issues.

However, as for flexible application, device on panel must sustain certain bending strain. It could be figured that the deformation of devices will cause an influence on the internal structures in TFTs, extending to change the electrical performance and stability at the same time. There are many studies discussing about the relationship between strain stress and TFTs performance [1.17-1.19]. Their results indicate the strain stress can strongly affect threshold voltage, subthreshold slope and mobility. But seldom studies has discussed stress release problem. In this thesis, a-Si:H TFTs fabricated on steel foil substrate are used to investigate the situation while the devices were under or after mechanical strain stress. The metastability effect of the uniaxial mechanical bending and strain stress release on hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) fabricated on flexible steel foil have been also studied by applying DC bias stress on gate electrode. Only if we could make some predictions for the trend of TFT electrical performance under mechanical strain precisely, we could finally apply our flexible TFTs to realistic display applications.

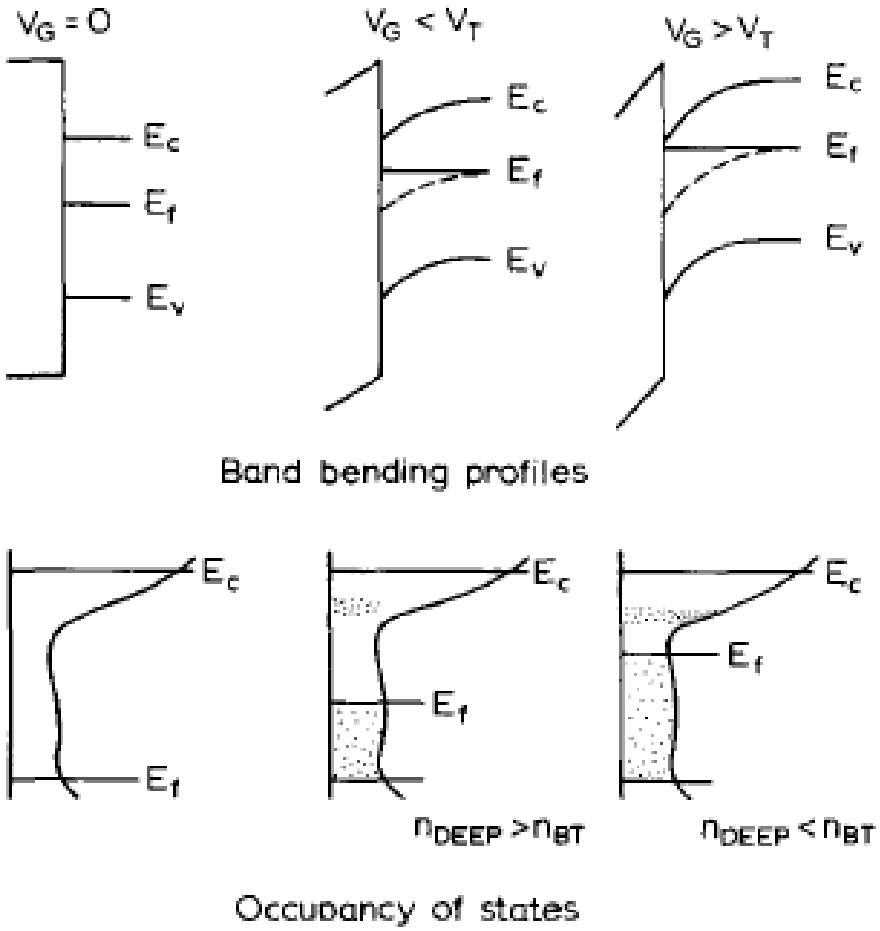


Fig. 1-1

Schematic illustration of the basic operation of an a-Si TFT, showing the energy band-bending (top) and the occupancy of the localized states; n_{deep} is the number of electrons in deep states and n_{BT}. Is the number of electrons in tail states.

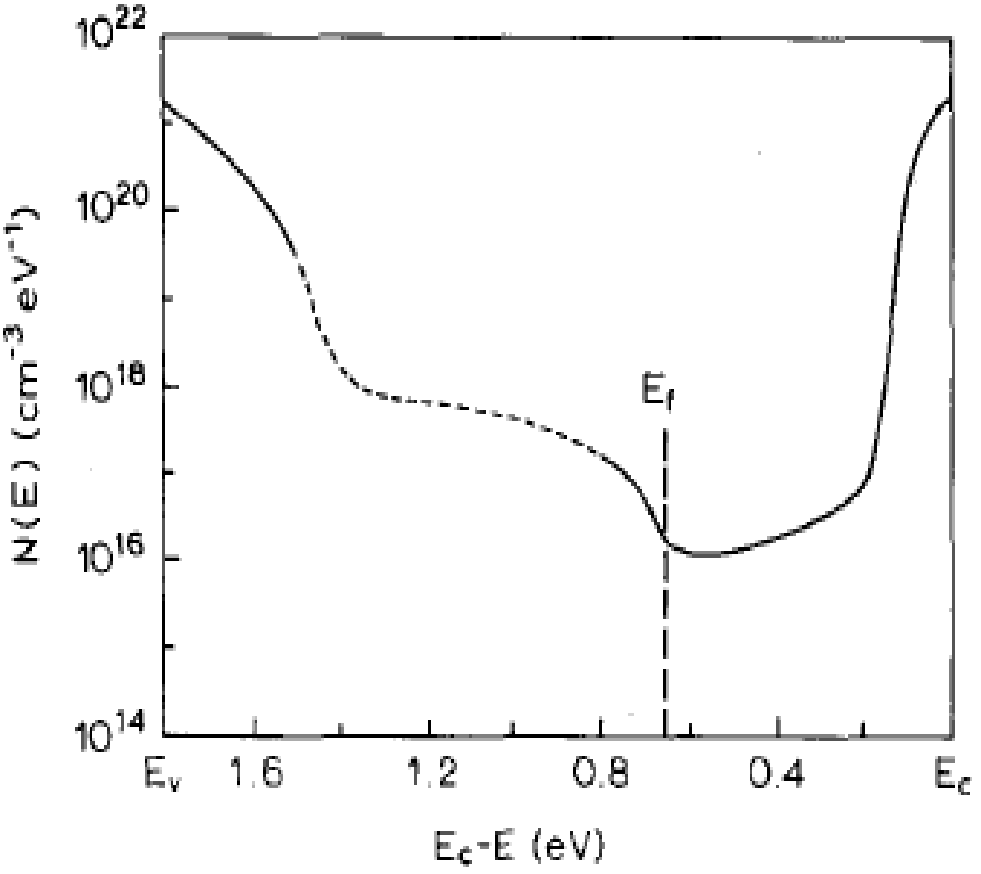


Fig. 1-2
The field-effect density of states.

Chapter 2

Experiments and Measurements

2-1. Procedures of Fabricating a-Si:H TFTs on Metal Foils

Our TFT device was chose as inverted staggered structure with back channel etching method on a 50um thick stainless steel foil substrate as shown in Fig 2-1. At beginning, the stainless steel foil substrates were polished with a combination of mechanical and chemical processes to reduce the surface roughness to a limit. Then, a 10nm planarization SiN:H layer was passivated on the steel foil to serves as a barrier against solvents and acids during the following TFT process. After the chromium (Cr) gate electrode was deposited and patterned on the substrate, the tri-layer comprised of 300 nm thick a-SiN:H layer, 200 nm thick a-Si:H layer and 50 nm thick n+ a-Si:H were consequently deposited by plasma enhanced vapor chemical deposition (PEVCD). All process temperature was controlled below 190℃ for the reason that several other polymers can withstand the temperature of 190℃ and therefore a 190℃ TFT technology can be used on other flexible substrates. After islanding the active region, the source and drain electrodes were deposited and formed for TFTs. Finally the n+ a-Si:H layer in the channel region would be etched off using the source/drain pattern as a mask. The channel length of TFTs ranged from 3 to 16 um, and the width ranged from 24um to 50um.

2-2. Extraction of Device Electrical Parameters

The methods of the typical electrical parameter extraction will be introduced in the following contents, including threshold voltage, sub-threshold swing and effective mobility.

Threshold Voltage (V_{TH})

To determine the threshold voltage in this thesis, we use the constant current method, which is adopted in most studies of a-Si TFTs. The threshold voltage is defined as the gate voltage which yields a normalized drain current (i.e. the current without the influence of channel length and width). In linear region measurement the normalized drain current 1nA and in saturation region 10nA were chosen for our flexible a-Si TFTs.

Sub-threshold swing (SS)

The method of determining SS is defined as the amount of gate voltage to increase and/or decrease drain current by one order of magnitude. The following expression for SS is given by

$$SS = \frac{\partial V_g}{\partial(\log I_d)} \tag{2-1}$$

As well-known, sub-threshold swing is a measure of the efficacy of gate potential to modulate drain current. From the equation above, we could clearly estimate that for a small value of SS, it means a small change in the input bias voltage can modulate the output current considerably. Therefore, SS is an indicator for determining whether this

TFT is a good transistor as a switch or not.

Effective Mobility (μ)

Mobility is another important electrical parameter for any types of TFT devices. The value of typical high quality a-Si material suitable for use in a TFT is about 1 $cm^2V^{-1}s^{-1}$.

For the linear region, we start extracting the parameter of mobility from the basic TFT drain current equation given by

$$I_D = \mu C_{ox} \frac{W}{L}[(V_G - V_t)V_D - \frac{1}{2}V_D{}^2] \quad (2\text{-}2)$$

, and we continuously define gm as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu}{L}V_D \quad (2\text{-}3)$$

Finally a maximum value of gm is chosen, and we could successfully extract mobility as

$$\mu = \frac{g_{m(\max)}L}{WC_{ox}V_D} \quad (2\text{-}4)$$

Similarly, we get mobility in the saturation region as

$$\mu = \frac{L}{WC_{ox}}(\frac{\partial\sqrt{I_D}}{\partial V_G})^2 \quad (2\text{-}5)$$

For all measurements, we performed the extracting parameter using HP 4156 semiconductor analyzer on the devices.

2-3. Measurement of Mechanical Strain on a-Si:H TFTs

For flexible display application, display panels are required to suffer certain degree of bending. Bending operation will induce strain in the electronic circuits and make influence on TFT device characteristics. Additionally, the DC operation on a-Si TFT has been extensively studied, but not for flexible display applications in which the real operation mode is under the mechanical strain. We found that the TFT device will suffer an obviously irreversible degrading effect from the applying strain at the first time, and become more stable under different strain status after multi-strain process. Also we investigate the influence of capping a silicon nitride passivating layer on our flexible a-Si TFT device.

2-3-1 Cylindrical Bending for the First Time

Before the device is under mechanical strain, a series of electrical parameters, such as V_{TH}、SS、and mobility, has been extracted in order to act as a compared data for the following strain tests. We set a fixed V_G-I_D measurement recipe for all this thesis as following, V_G swept from -25V to +35V, V_D had steps from 1V to 13V and V_S is grounded.

The cylindrical bending mold in our first part experiment was set to a positive R_p (tensile) and negative R_n (compressive) with the radius of 10 mm which could apply a large and effective strain on our sample. TFT sample was stock on the mold and the stain stress prolonged to the direction parallel to the source-drain channel current path (Fig. 2.2). After the electrical performance was measured, the TFT sample was released

from the bending condition and re-flattened to flat condition. We repeated this flat-bending-reflatten process for several times and measure the change of electrical performance on every experiment step.

The DC gate bias stress condition was set to V_G = +40V, while source and drain electrodes are connected to ground from 0 second to 10^4 seconds. The sample was stressed under initial flat plane, bending on mold and re-flatten back to plane at room temperature (25℃). While the sample was stock on mold (under cylindrical bending), we also changed the measurement condition to 50℃

2-3-2 Gate DC Bias Stress under Multi-Strain Status

In realistic living application, because the flexible TFT must be operated under repeatable mechanical strain, the second part of our experiments is to investigate the electrical performance under multi-strain status after first-time bending.

After the TFT sample was strained through many times and turn to a more stable condition compared to first-time bending effect, our TFT sample was stock on different bending radius from R_p= 50mm to 10mm, R_n = -50mm to -10mm, and the stain stress also prolonged to the direction parallel to the source-drain channel current path. Additionally, we measure in 5 different temperature, as 25℃、50℃、75℃、100℃、125℃ respectively, in order to extract the activation energy.

The same as the first part, the DC gate bias stress condition was set to V_G = +40V, while source and drain electrodes are connected to ground from 0 second to 10^4 seconds.

2-3-3 Nitride Layer Capping on Device

Before the TFT device is applied to display panel circuit in practice, there is usually a passivating layer for preventing it from ion contamination and humidity. Therefore, the effect of passivating layer on TFT device, even under mechanical strain after passivation, should be an important issue which we couldn't ignore.

2-3-3.1 Procedures of Silicon Nitride Passivation

In the a-Si TFT industry recent years, silicon nitride film (SiNx) plays a key role for TFT passivation. For standard a-Si TFT fabrication, the process temperatures lie between 300 and 350℃ and so does the temperature with SiNx deposited by PEVCD. For this reason, we try to investigate the influence on SiNx passivation on our flexible a-Si TFT,

As mentioned in Procedures of Fabricating a-Si TFTs on Metal Foils, we reduced the fabrication temperature to 190℃ for certain reasons. Therefore, we also deposited SiNx films on top of our TFT device as the passivation by PEVCD 190℃. The DC gate bias stress condition was also set to V_G = +40V, while source and drain electrodes are connected to ground from 0 second to 10^4 seconds, before and after SiNx capping in order to analyze the reliability between different conditions.

2-3-3.2 Post Annealing Process

Thermal treatment is one of some well-known processes which may possibly improve the electrical performance of a-Si TFT. The post annealing process after TFT device passivated is also a conventional

process for standard fabrication in industry. 300~350℃ 60 minutes annealing under Nitrogen atmosphere is the most common method for post thermal treatment as we know. But for our 190℃ SiNx deposition temperature, we considered that such high temperature as 300℃ would cause unpredictable damage to our low-temperature a-Si TFT samples. So that the set of 190℃ 60min annealing was chosen. After annealing process we take the same gate voltage DC bias stress test as well.

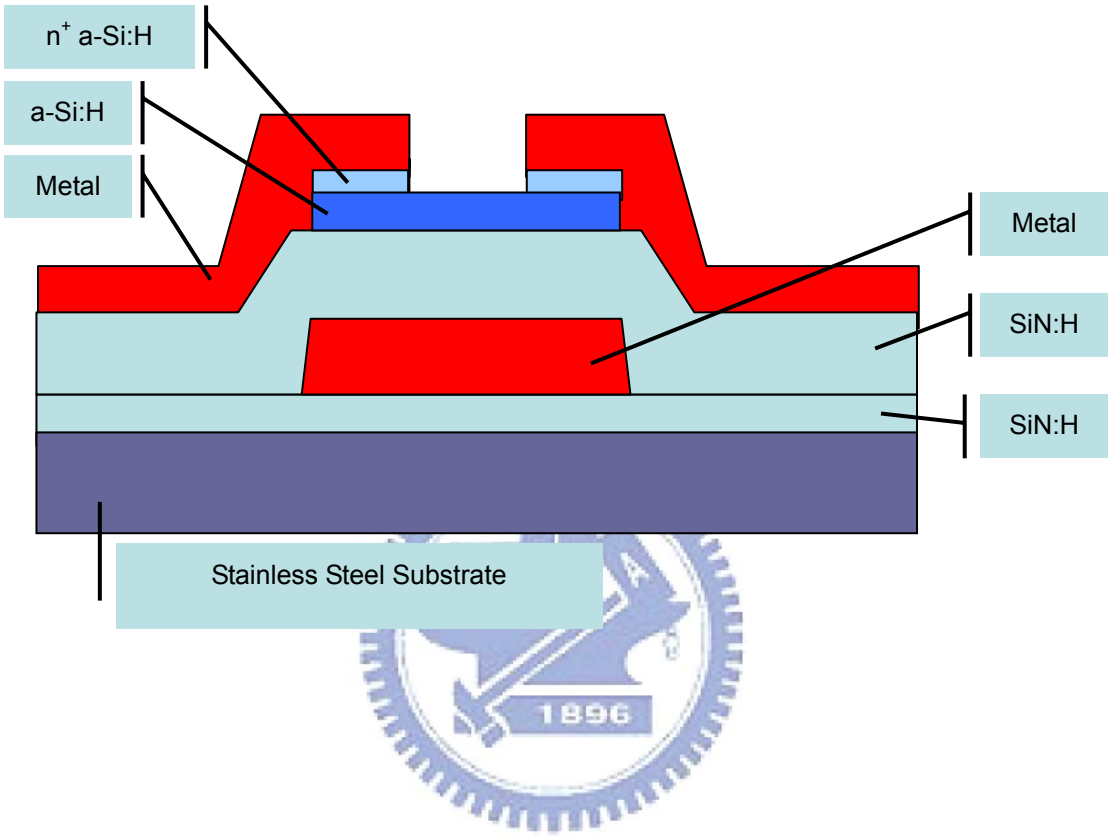


Fig. 2-1.

Cross section view of our TFT device, which was chose as inverted staggered structure with back channel etching method on a 50um thick stainless steel foil substrate

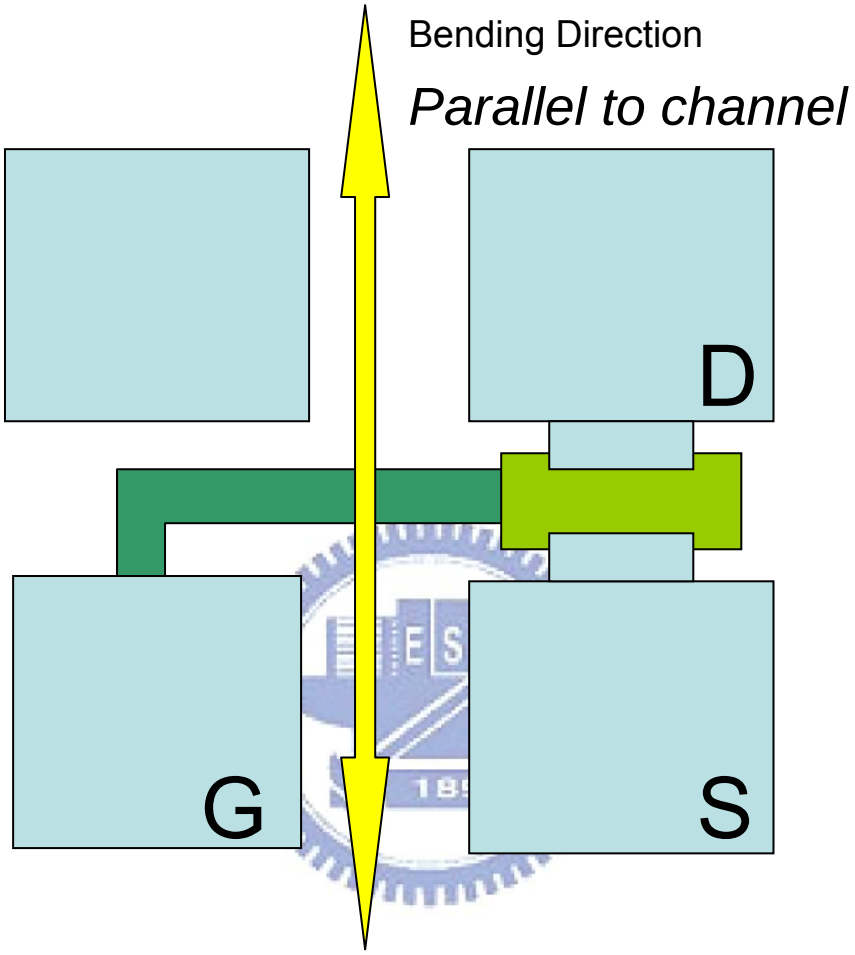


Fig. 2-2.

The arrow denotes the bending direction parallel with the TFT source-drain current path.

Chapter 3

Result and Discussion

3-1. Electrical Performance under Different Mechanical Strain

As mentioned before, we found that the first-time mechanical strain will induce a irreversible degrading effect on flexible a-Si TFT sample. The following contents will focus on the first-time bending effect first.

In realistic living application, because the flexible TFT must be operated under repeatable mechanical strain, the second part of our experiments is to investigate the electrical performance under multi-strain status after first-time bending.

3-1-1. Bending processes on flexible a-Si:H TFTs

Fig.3-1. shows the V_G-I_D transfer curves of the flexible a-Si TFTs before the first-time bending. The channel size is 24um in width and 16um in length. The off current is ~5 x 10^{-13} A , the on-off current ratio > 10^7, the threshold voltage ~6 V, and the subthreshold slope ~0.76 V/decade. The electron linear mobility, calculated from the transfer characteristic for drain-to-source voltage V_{DS} = 1 V, is ~0.55 cm^2/Vs.

Inward cylindrical bending produces compression, by definition negative, and outward bending tension, positive. By repeating the flat-bending-reflatten process for several times, we get a TFT threshold voltage degradation diagram Fig.3-2. The error bar in Fig.3-2 represents the data range because we have more than one experiment data showing this kind of trend and the solid points are the average values of all data

collection. From this figure, we could obviously find that the threshold voltage shifted most seriously when our device was under mechanical strain for the first time, and didn't recover to the initial performance for a period of time (We had transfer characteristics measured after 72 hours later and showed it still couldn't get back to the initial performance).

In compression of first-time bending effect, our initial flexible a-Si TFT sample were bent to two kinds of bending method, tensile strain R_p = 10mm and compressive stress R_n = 10mm. Fig.3-3. shows the transfer characteristics with V_D = 13V respectively. We first applied tensile strain and observed a slight increase in the threshold voltage, and then found there was more seriously shift in threshold voltage when applied compressive strain. We will have more detailed discussion about these phenomenons in the following section.

Fig. 3-4, Fig. 3-5, Fig 3-6 shows the relative mobility, threshold voltage, and sub-threshold swing as a function of strain extracting from the same TFT device after the sample is bent time after time. To compare the data from the bending and stretching experiments, we calculate the strain **ε** under bending from the formula [3.1] given by

$$\varepsilon = \frac{d_f + d_s}{2R} \frac{(1 + 2\eta + \chi\eta^2)}{(1+\eta)(1+\chi\eta)} \qquad (3\text{-}1)$$

, with $\eta = d_f / d_s$ and $\chi = Y_f / Y_s$, here $d_f = 2.5$ and d_s = 50um are film and substrate thicknesses, respectively. Y_f = 200 GPa and Y_s = 20GPa are Young's modulus of film and substrate, respectively.

Fig.3-4 depicts the relative mobility μ/μ_0 as a function of strain when TFTs is operated under V_D=13V and channel size is 24um/16um, whereμ is the mobility under different imposed strains andμ_0 is the initial

mobility (Flat condition). It shows that the mobility will have a decreasing trend both under tensile strain and compressive strain. Obviously the compressive strain stress will cause more serious decrease on mobility than the tensile one [3.2].

Fig. 3-5 shows the relative threshold voltage V_{TH}/V_{TH0}, where V_{TH} is the threshold voltage at a given strain and V_{TH0} is the initial threshold voltage. The greatest increasing ratio of V_{TH} shift is almost 17% when the flexible a-Si TFT is under compressive strain of ~ -0.00187 (R = -50mm). Similar to the phenomenon observed in mobility change, we could find the V_{TH} degradation existing in both tensile and compressive strain. We will discuss these degrading effects under mechanical strain in the next section 3-1-3.

Fig. 3-6 indicates the relative sub-threshold swing SS/SS_0, where SS is the sub-threshold swing at a given strain and SS_0 is the initial swing. While there is a clear trend in μ/μ_0 and V_{TH}/V_{TH0} as a function of strain, the spread in SS/SS_0 seems more disorderly. Roughly, the value SS will increase with the applied strain, but we draw this conclusion with reservations as some previous reports [3.2].

3-1-2. Analysis of Parasitical Resistance Extraction

Form previous reports, the parasitical resistance might be one factor of change on a-Si TFT transfer characteristics. However, the effect of the parasitical resistance, under mechanical strain has not been precisely discussed yet.

The total resistance for the ON resistance, R_{total}, extracted from the V_D-I_D curves, is consisted of channel resistance R_{ch} and parasitical

resistance R_p. The parasitical resistance is estimated by the following equations:

$$R_{total} = R_{ch} + R_p \tag{3.1}$$

, and then

$$R_{ch} = \frac{L}{W \mu Ci(V_G - V_T)} \tag{3-2}$$

$$R_p = R_{p0} + \frac{L_0}{W \mu C_i(V_G - V_{T)}} \tag{3-3}$$

, where R_{p0} is the intrinsic parasitical resistance independent of electric fields and $L+L_0$ is defined as effective channel length. From linear region drain current equation, we could get

$$I_D = \frac{W}{L} \mu C_i(V_G - V_T)V_D \tag{3-4}$$

$$\frac{\partial I_D}{\partial V_D} = R_{total}^{-1} \tag{3-5}$$

If under the same VG, there are two different channel length sizes, A and B respectively. And

$$\begin{aligned} R_{total}A &= R_p + AK \\ R_{total}B &= R_p + BK \end{aligned} \tag{3-6}$$

K is a constant parameter which represents the R_{ch} except channel length factor. From the equation above, we can erase this unknown value of K and get R_p value when $R_{total}A$ and $R_{total}B$ are extracted by V_D-I_D curves. For comparison, we calculated the Rp from two conditions, initial flat and compressive radii of 10mm, to investigate the influence of parasitical

resistance under mechanical strain. The first step of extracting R_p is shown in Fig.3-7. Clearly there is no great change for R_p when the sample is under mechanical strain.

Having estimated the total R_p, we proceed to find the intrinsic R_{p0} which is independent of gate voltage. As can be seen from Eqn.(3-1), (3-2), (3-3), the measured resistance for the TFT is linear function of L. Therefore, based on the method used bt Terada and Muta [3.3], and Chern at al. [3.4], a plot of $R_{on}W$ as a function of channel length L for different values of V_G maybe used to extract L_0. Fig.3-8. illustrates this for TFT remaining flat and under mechanical strain. As can seen, the curves for different applied voltages have an intercept point with x-axis coordinates (L_0). It should be noticed that there is an identical value of L_0 between flat condition and strain condition.

Summarizing all the results above, we make a conclusion that the degradation mechanism of threshold voltage under mechanical strain is independent of parasitical resistance.

3-1-3. Analysis of Activation Energy Extraction

As mentioned in introduction, the localized states in the amorphous silicon can be divided into two types, tail states and deep states as the Fig. 3-9. The tail states are the Si conduction band states broadened and localized by the disorder to form a “tail” of localized states just below the conduction band mobility edge. The deep states originate from defects in the amorphous silicon network. These are thought to mostly consist of Si dangling bonds, which have a wide range of energies because of the variations in local environments.

By changing the measuring temperature [3.5-3.6], we have extracted the activation energy under R_p = 10mm and R_n = -10mm to investigate the degradation phenomenon. Fig. 3-10 shows the activation energy (E_A) as a function of V_G in three conditions. The thick solid line indicates the V_{TH} for this TFT device. We divide the total E_A illustration into three regions: V_G above V_{TH}, V_G between zero point and V_{TH}, V_G below zero point.

The region for V_G above V_{TH} relates to the "ON "state for a-Si TFT and the acceptor-like tail state, which is the dominant region for the mobility. Firstly, as shown in Fig.3-10 the E_A of the a-Si TFT in this region under tensile and compressive strain are both larger than the flattened condition. Additionally, the compressive strain status has the largest E_A. These trends indicate that there are larger densities of states (DOS) in acceptor-like tail state when sample is under mechanical strain. Therefore, the mobility decreases as the results we measured before in Fig. 3-4.

The region relating to V_G between zero point and V_{TH} represents the forward sub-threshold region, where the deep state in acceptor-like states. For V_G below zero point, TFTs operated region start from reverse sub-threshold region to the well known Poole-Frenkel region, both relate to deep states in donor-like states. However, the deep level states dominate the mechanism of threshold voltage and the density of states has a positive correlation to activation energy. From our E_A plot Fig. 3-10, we find both regions mentioned above showing that there is lower E_A under mechanical strain.

If we focus on the decreased E_A value for strained conditions

specifically, we can find the region for $V_G < 0$ has the greater E_A decreasing value than the region between 0 to V_{TH}. If we transfer E_A to DOS parameter, we will obtain a result just as Fig. 3-11. The solid line represents the initial state for flatten status while the dotted line represents the condition under mechanical strain. Clearly E_i will shift left when applied strain on flexible a-Si TFT. Therefore, there is larger range between E_C to E_i, which means more charges needed to fit in the deep states, and so the threshold voltage will increase. Again the E_A analysis supports the conclusion we made for threshold voltage degradation under mechanical strain before.

3-1-4. Reliability Investigations of Gate DC Bias Stress

The gate-bias voltage was set to 40V to keep the TFT channel forming in the a-Si layer. The drain and source terminals remain grounded during all the reliability tests.

For most of the reliability researching papers, the metastability of threshold voltage is what people always focus on. Fig. 3-12 shows the Vth shift curves of the TFTs of the flexible a-Si TFT before and after 10000 seconds of gate voltage 40V DC stress with different status including flat、tensile (compressive) strain at room temperature、tensile (compressive) strain at 50℃、and reflatten conditions. It is observed that threshold voltage serious depends on the applied mechanical strain. When the TFT sample is under no matter outward (tensile) or inward (compressive) bending, there is much more degradation of V_{TH} shift than flat condition. For the reflatten condition curve it could tell us that the

sample didn't recover to the initial status. This result verifies the conclusion we made in section 3-1-1 again.

From the previous sections, the most important instability mechanisms for a-Si TFTs under prolonged gate stress are charge trapping and defect creation. Usually the degradation behavior is identified as the combination of both effects, but one mechanism mainly dominates. From Fig. 3-13, we can observe the obvious power-law time dependence of positive V_{TH} shift. This phenomenon shows the first step that we predict the defect states creation is the dominant instability mechanism of our gate DC bias stress experiment. As mentioned before, the defect state creation is strongly affected by the temperature. From Fig 3-13, clearly the variation of V_{TH} curve shifts much more seriously when the temperature is 50℃ than 25℃ under mechanical strain. The second step for identification of instability mechanism is done. We could now make a conclusion that the dominant instability mechanism under mechanical strain for the flexible a-Si TFT is defect state creation during our gate voltage DC bias stress experiment.

From the theory of defect pool model [3.7], the rate of defect creation is a function of the barrier to defect formation, the number of carriers in the tail states, and the density of the weak bond sites. It has also been proven that the higher gate bias, the more serious the degradation in a-Si TFTs.

Such metastability of $\triangle V_{TH}$ could be refer to the deformation of disorder in a-Si:H cause by strain stress and the formation of creation of dangling bonds in acceptor-like level in our flexible samples. This kind of effect on the disorder of a-Si:H interior structure is permanent, that's why

the re-flatten result was so similar to bending one.

After the first-time bending reliability analysis, we now proceed to investigate the reliability for different strain status. The radii of cylindrical bending we use for V_G stress tests are R_p = 10mm, 30mm, and 50mm, R_n = -10mm, -30mm, and -50mm. Fig. 3-14 and Fig. 3-15 show the threshold voltage shift under compressive strain (R_n) and tensile strain (R_p) respectively. First, there is an obvious trend that the degradation of threshold voltage is more serious under larger strain whether compression or tension. This result also accords with the prediction we made in first-time bending test. And then from Fig. 3-14 and Fig. 3-15, we can find that there is an instant threshold voltage shift when Rn = -50mm strain is applied. Comparing with Rp = 50mm, it seems no such large threshold voltage degradation. We make a conclusion that the compression will cause more degree of interior disorder than tension again via reliability investigation.

3-2. Influence of Nitride Layer Capping on TFTs

The following contents include all the results of electrical performance analysis and reliability tests for the effect of capping silicon nitride (SiNx) passivation under 190℃ PECVD.

3-2-1. Effect of Passivation on flexible a-Si:H TFTs

Fig. 3-16 showed comparison of the I_D-V_G figure operated under V_D = 10V of the flexible TFTs with and without passivating layer, and pre-annealing and the post-annealing. Clearly 190℃ SiNx passivatng process will improve our flexible a-Si TFT as well as the traditional high temperature passivating process. The mobility increased from 0.31 to 0.33 cm^2/Vs, V_{TH} shifted from 9.5 to 7.3 volts, and SS decrease from 1.76 to 1.55 V/decade. From the result, we conjecture that hydrogen will have a passivating effect on dangling bonds and decrease the density of defect states during depositing SiNx layer process.

3-2-2. Reliability Comparison of TFTs under Strain

In order to investigate the reliability issue of passivating nitride at 190℃ on flexible a-Si TFT under mechanical as well, we make a comparison with and without capping nitride by using V_G= +40V DC bias stress.

Fig. 3-17 and Fig. 3-18 show the V_{TH} shift under R_p = 10mm and R_n = -10mm strain status respectively. As Fig. and Fig. illustrate, no matter when the sample is under compression or tension, the V_{TH} degradation

have an obvious improvement after 190℃ SiNx capping process. Combining the results of 3-2-1 and 3-2-2, we successfully affirm that capping SiNx at 190℃ has the same effect for improving a-Si TFT device characteristics as industrial 300~350 ℃ SiNx deposition temperature.

3-2-3. Post-Annealing Effect on Passivated a-Si:H TFTs

As mention before, we try to follow the same post-annealing process as the standard a-Si TFT fabrication in industry but reduce the annealing temperature to 190℃ in order to match our low temperature flexible a-Si TFT fabrication.

From Fig. 3-16 again, we can observe the additional improved transfer curve after 190℃ thermal annealing for 60 minutes. Comparing with the sample only passivated, the mobility increased from 0.33 to 0.35 cm^2/Vs, V_{TH} shifted from 7.3 to 6.6 volts, and SS decrease from 1.55 to 1.51. The behavior of the electrical performance of flexible a-Si TFTs after post-annealing treatment is similar to the effect of thermal enhanced diffusion (TED). With the thermal effect, the hydrogen will diffuse into the active layer for mending the dangling bonds and defect states, and improve the electrical performance.

Fig. 3-19 shows the threshold voltage shift under three different conditions, including flat, tensile, and compressive status comparing the sample with and without post-annealing process. It clearly indicates the reliability improving again after 190℃ annealing in atmospheric anneal

furnace 60 minutes. The results of reliability tests also support our argument for hydrogen diffusion under thermal influence.

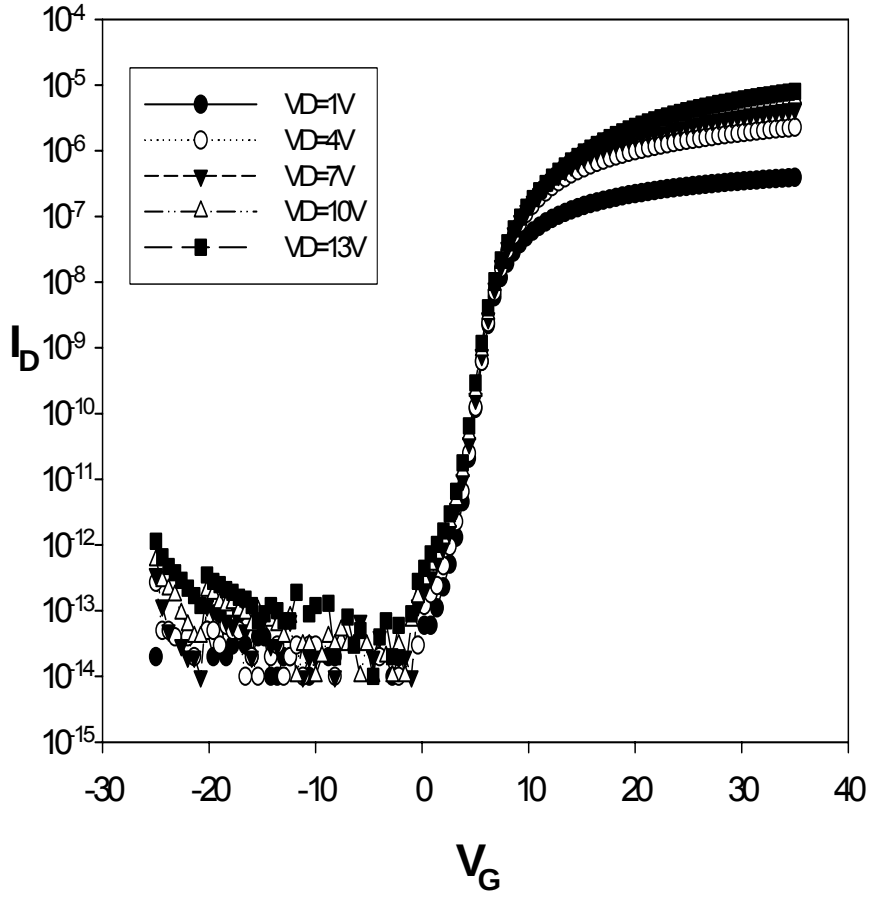


Fig. 3-1

The basic transfer curves of a flexible a-Si TFT on stainless steel foil, showing the 5 different V_D operated condition.

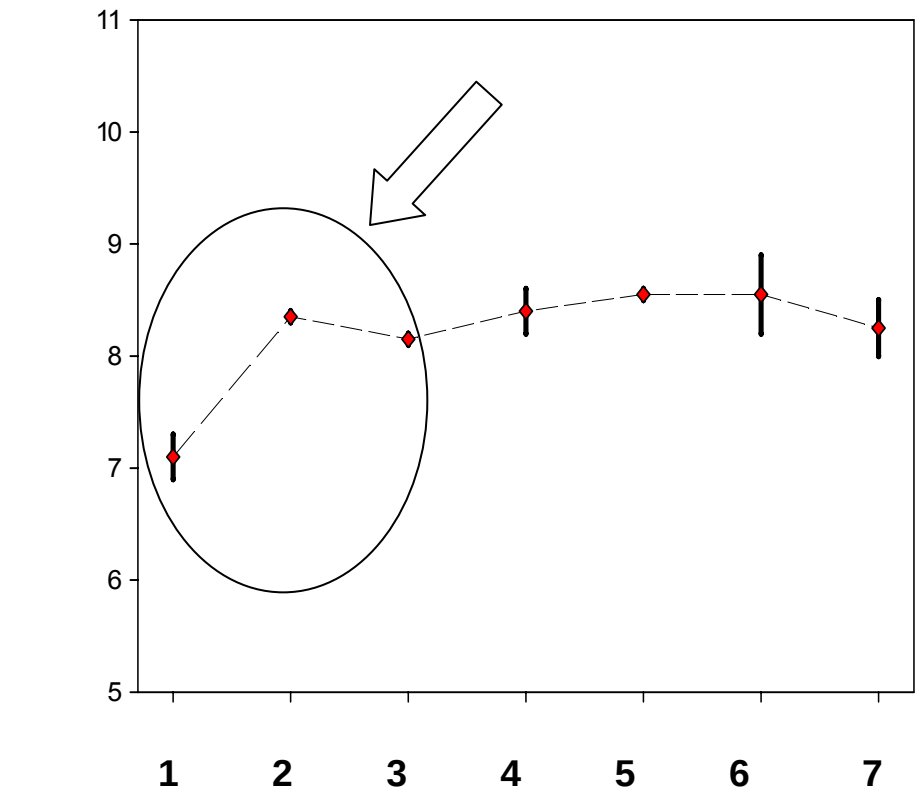


Fig. 3-2

The diagram shows the threshold voltage shift caused by repeating Flat-Bending-Reflatten process. (1:Initial status, 2:1st tensile strain, 3:1st reflatten, 4:2nd tensile strain, 5:2nd reflatten, 6:3rd tensile strain, 7:3rd reflatten). We can easily observe the most serious Vth shift from the first time bending.

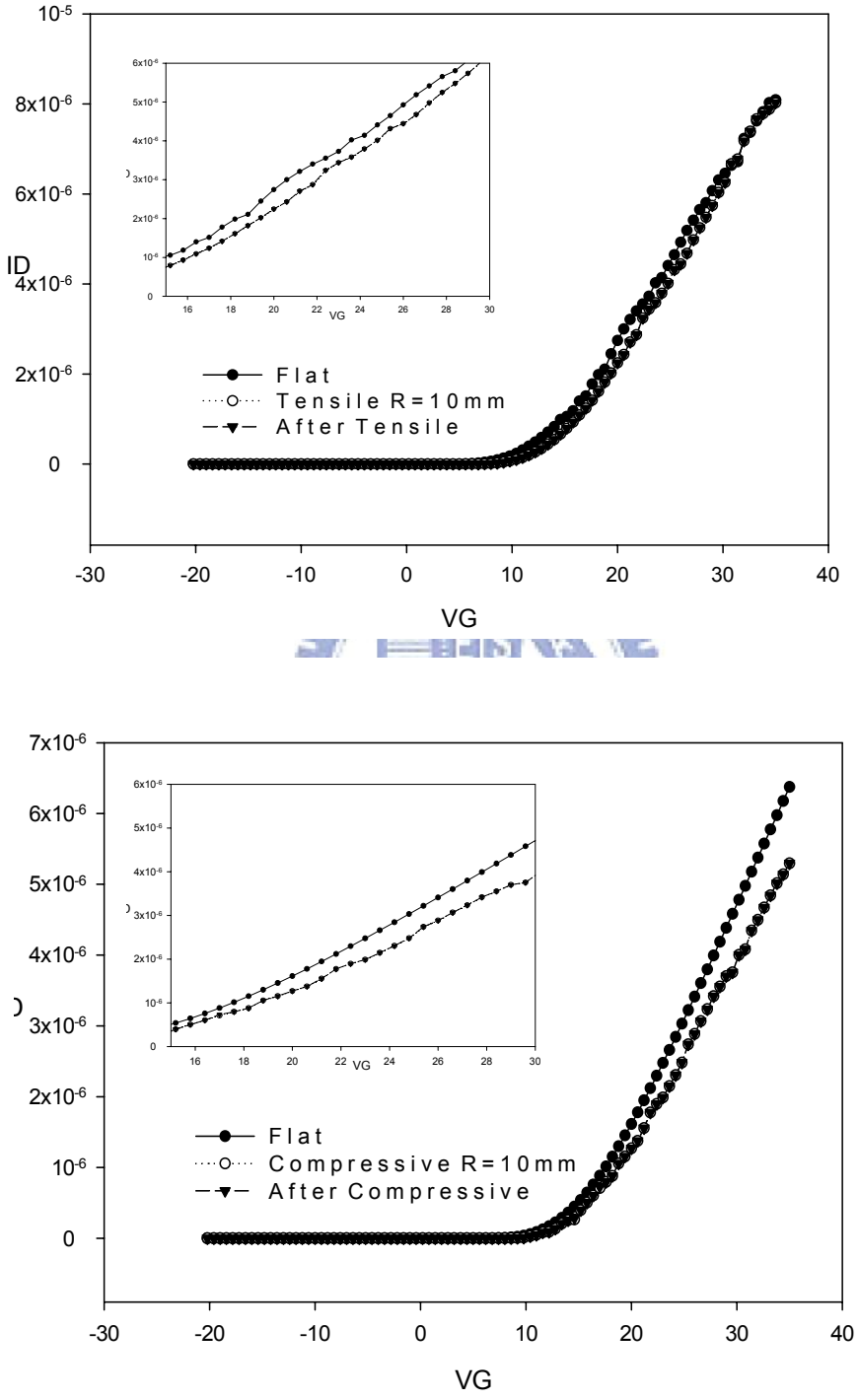


Fig. 3-3

Transfer characteristics for flexible a-Si TFTs strained under tensile radius of 10mm and compressive radius of 10mm.

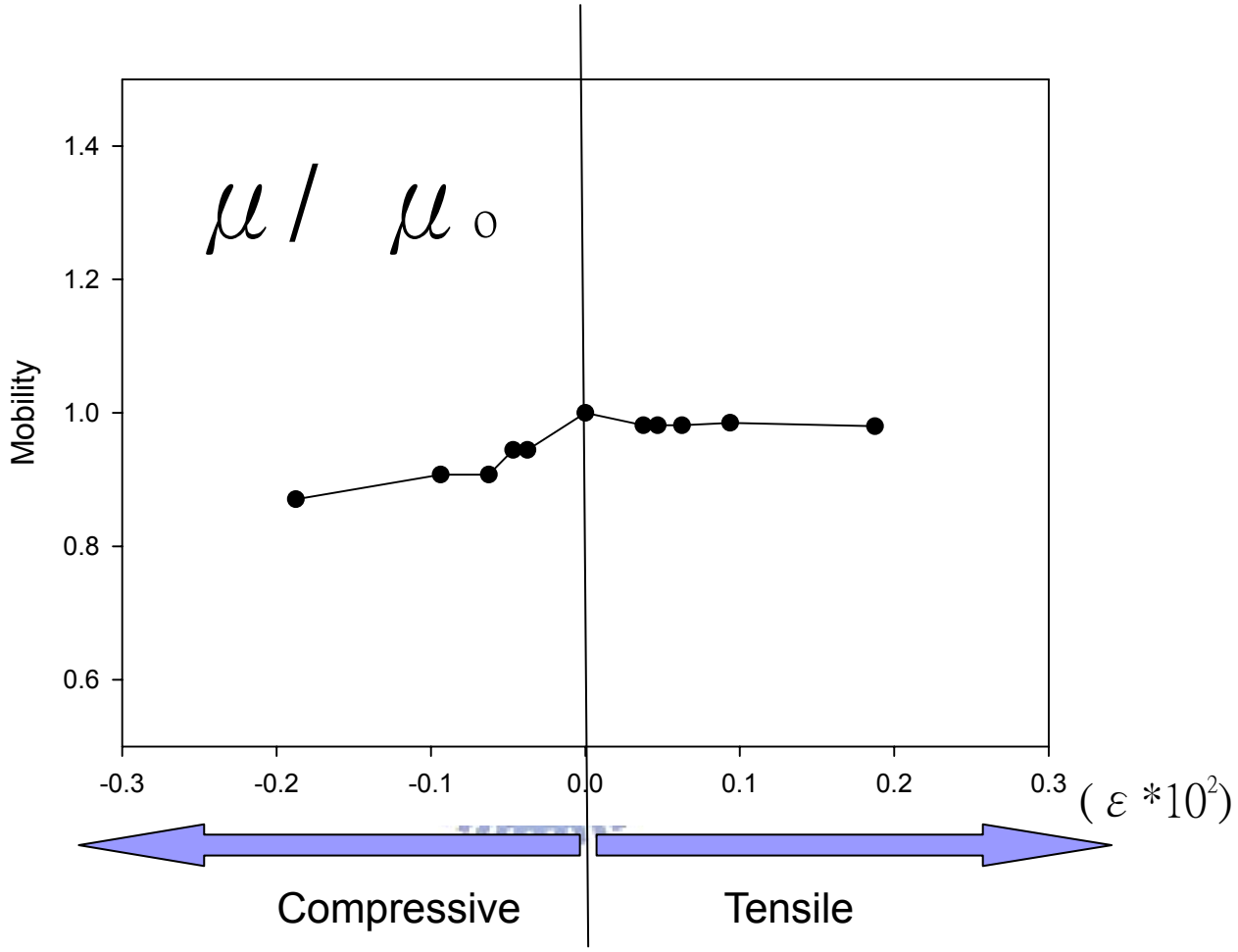


Fig. 3-4

The relative mobility as a function of strain.

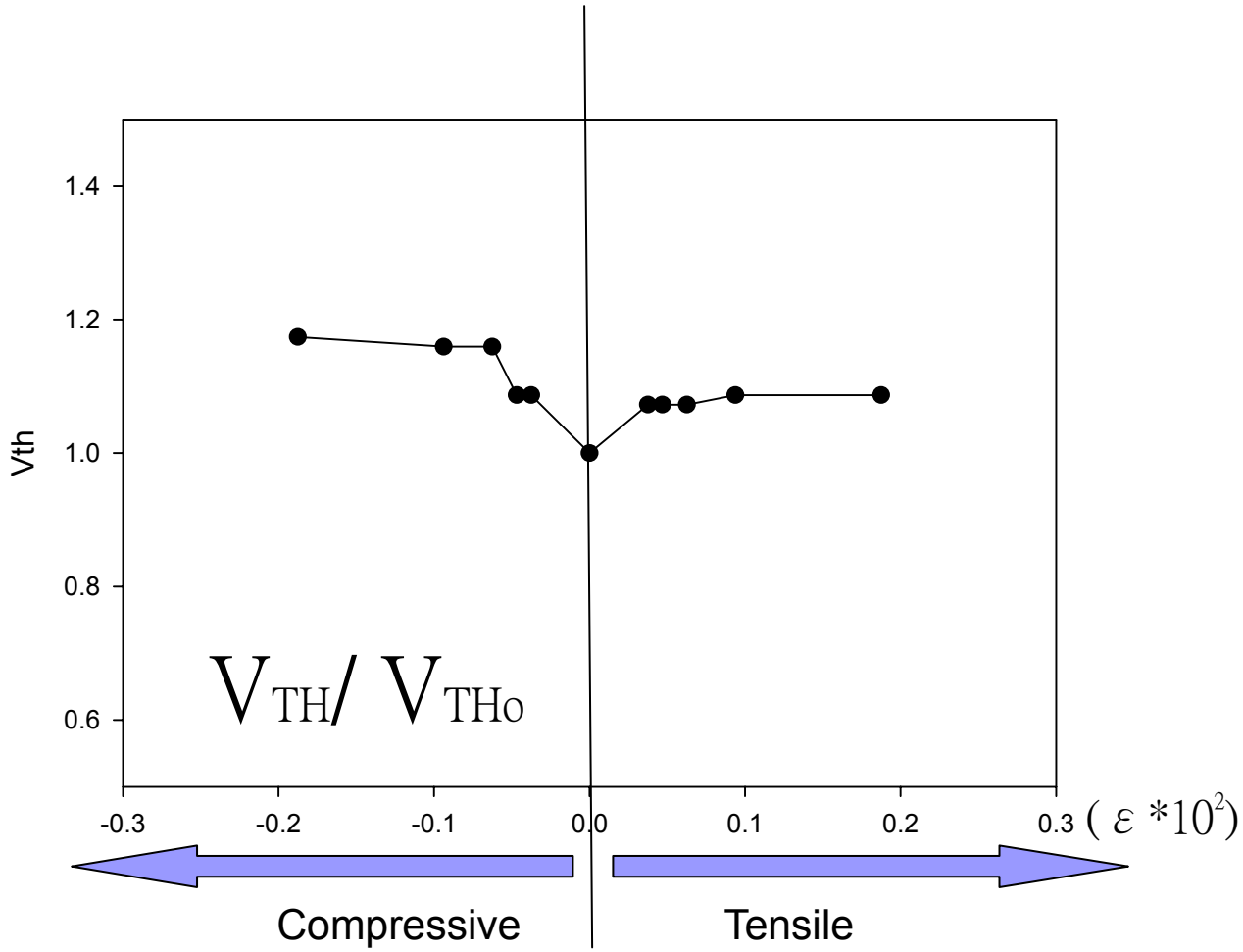


Fig. 3-5

The relative threshold voltage as a function of strain.

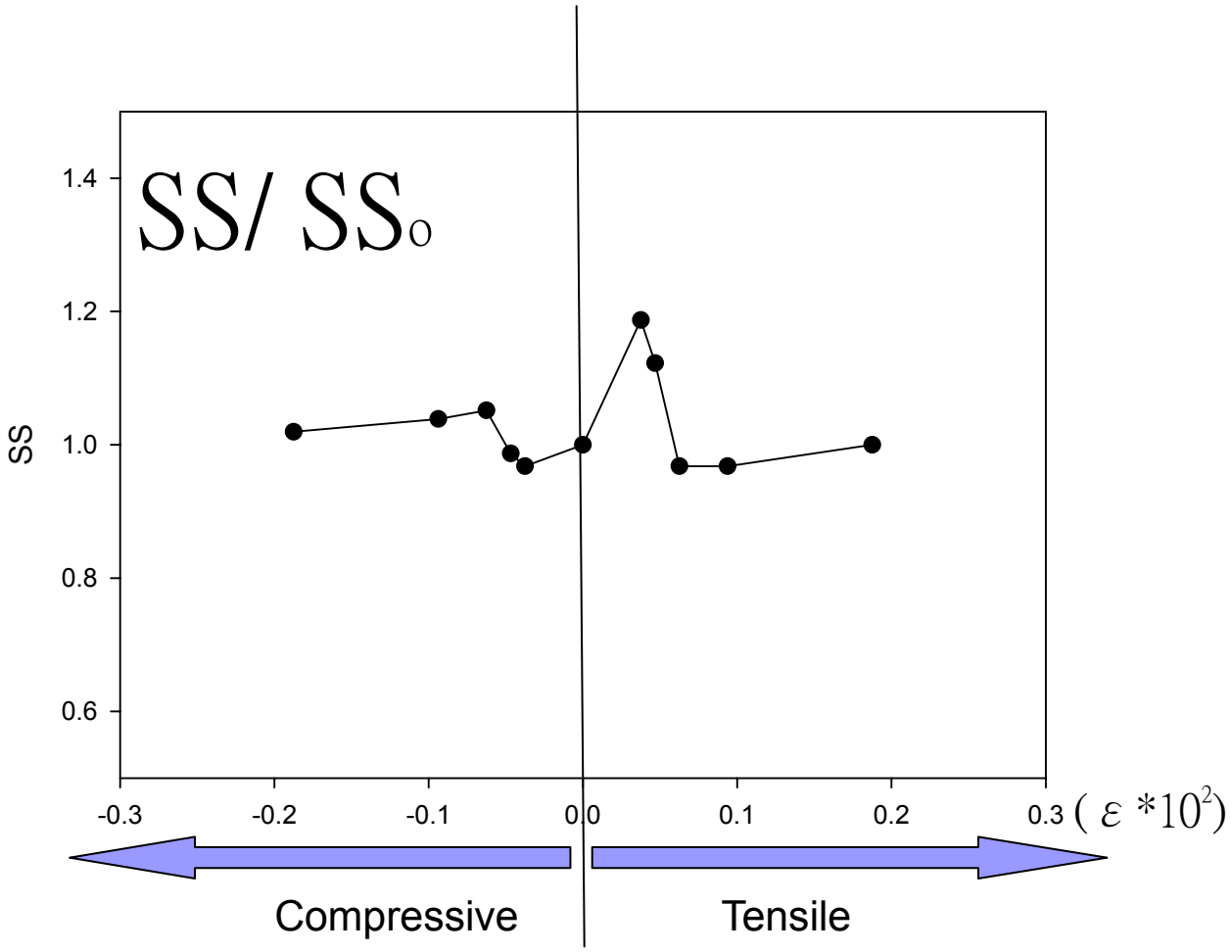


Fig. 3-6

The relative sub-threshold swing as a function of strain.

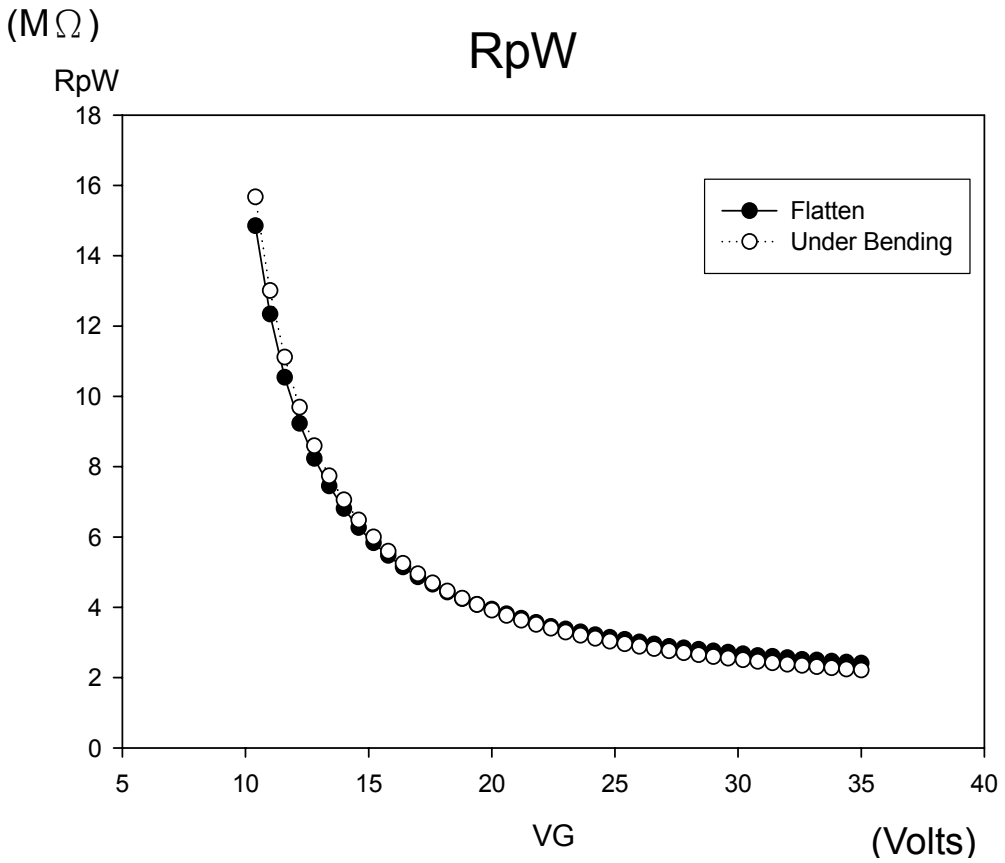


Fig. 3-7

The parasitical resistance under two conditions shows as a function of gate voltage. The two curves almost matching indicates that there is no great change for R_p under mechanical strain.

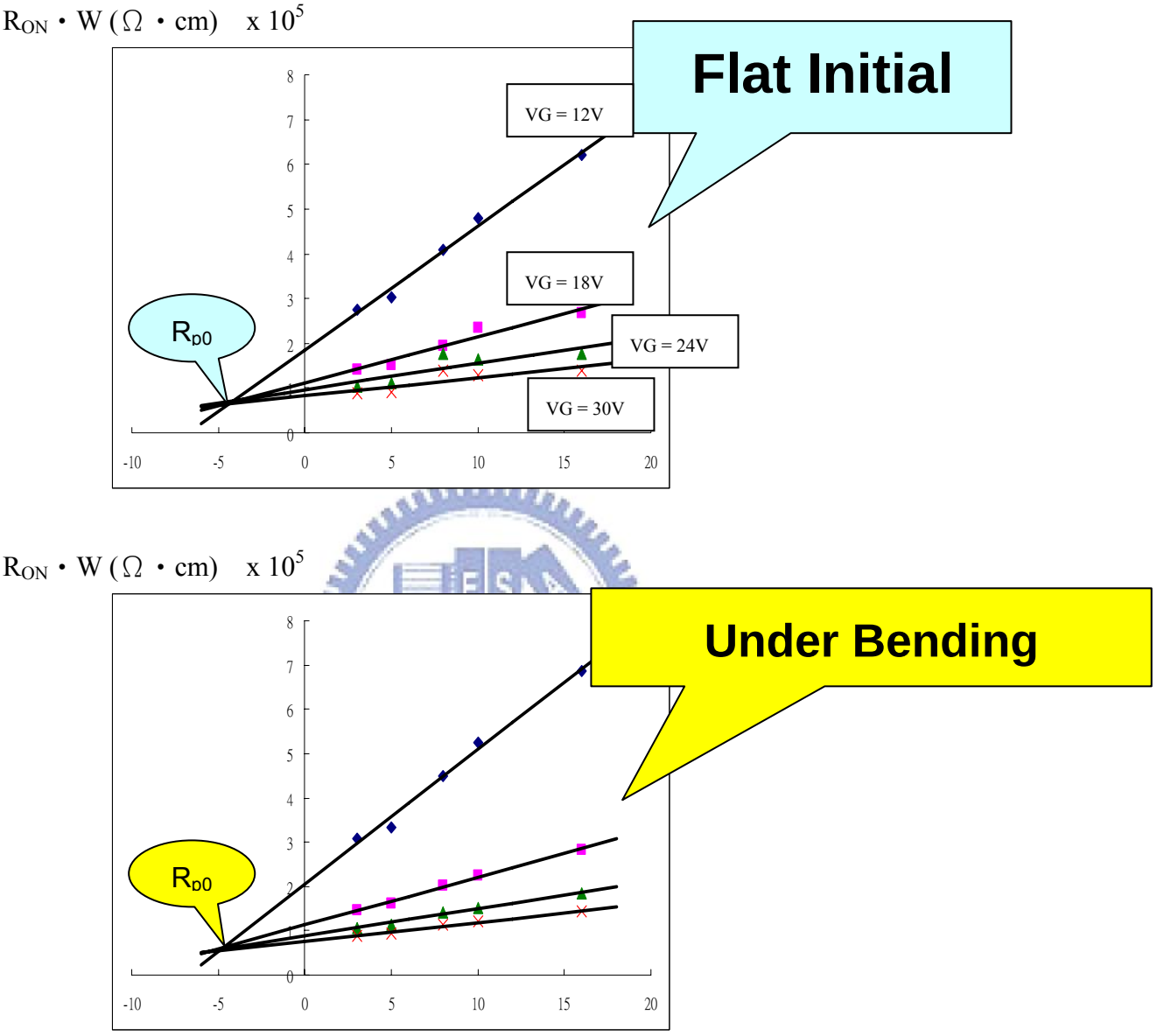


Fig. 3-8.

$R_{on}W$ of flexible TFTs as a function of L under two different status. It should be noticed that the L_0 value is the same between flat condition and strain condition.

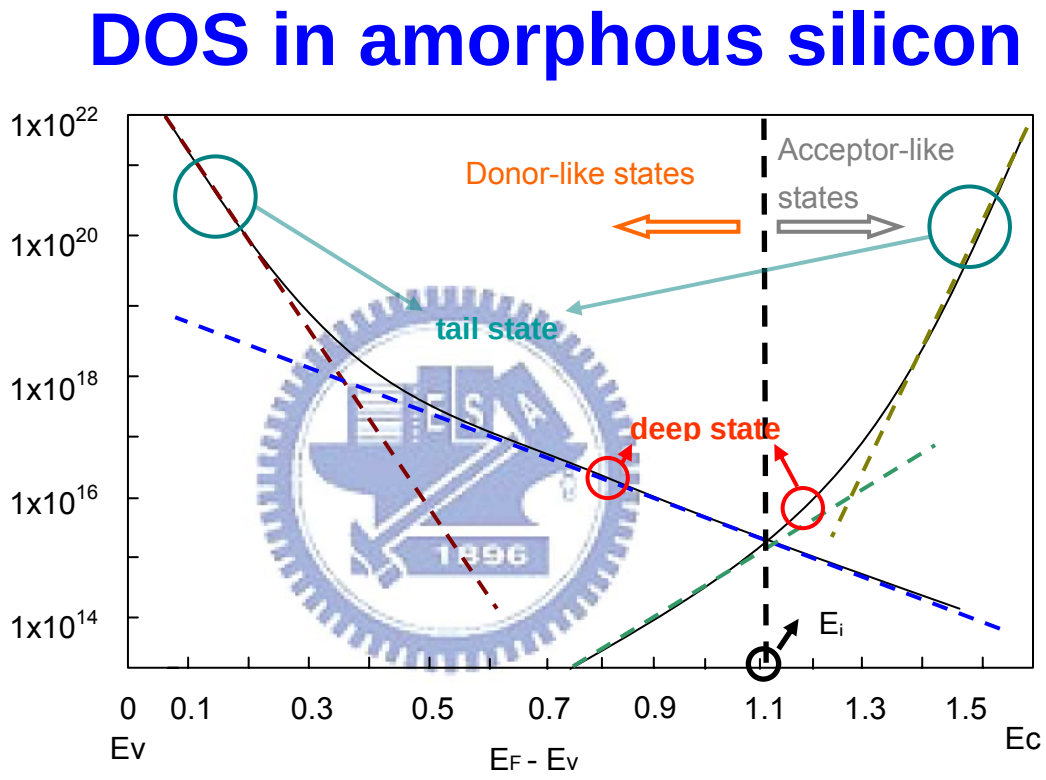


Fig. 3-9

Illustration of the density of states (DOS) in intrinsic a-Si.

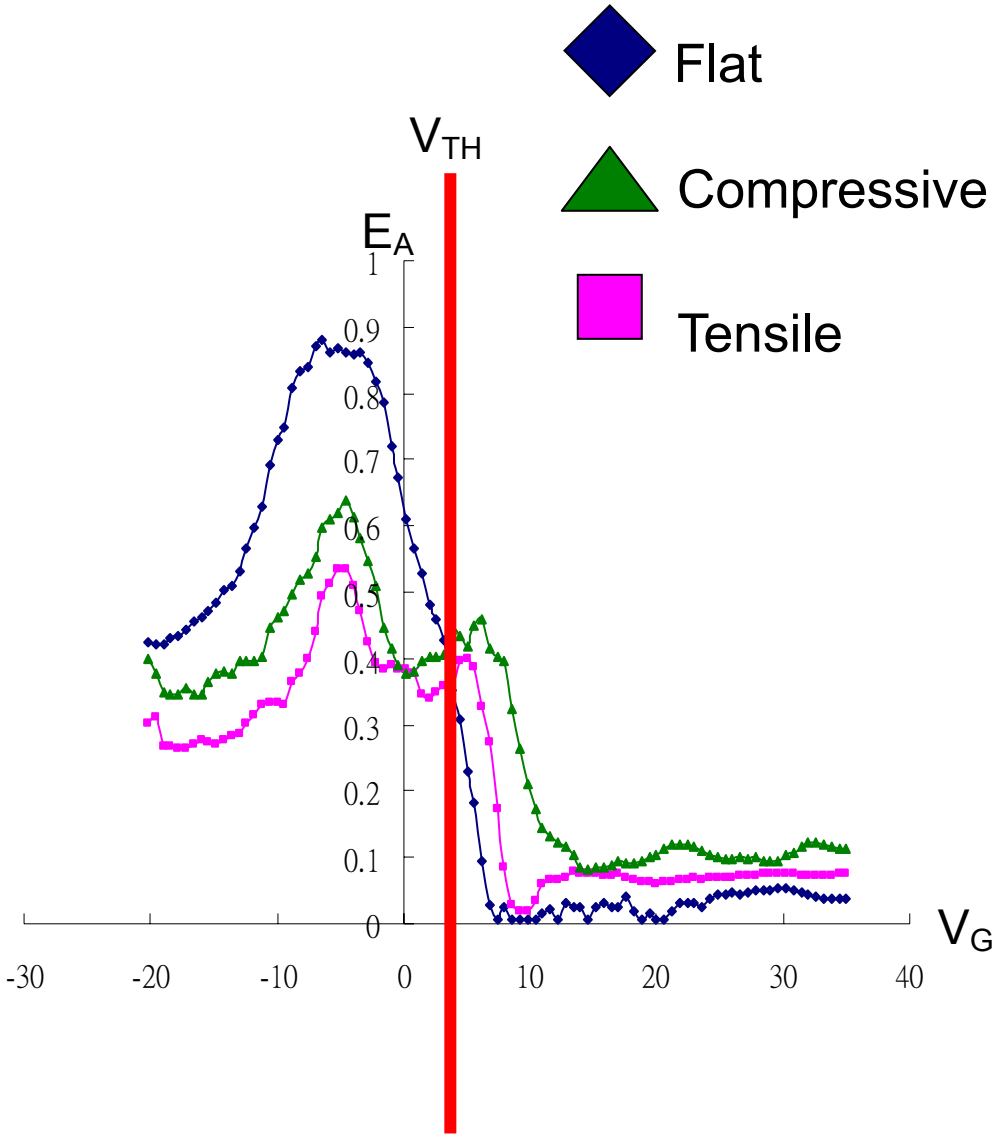


Fig. 3-10

The activation energy (E_A) as a function of V_G in three conditions including flat, compressive, and tensile status.

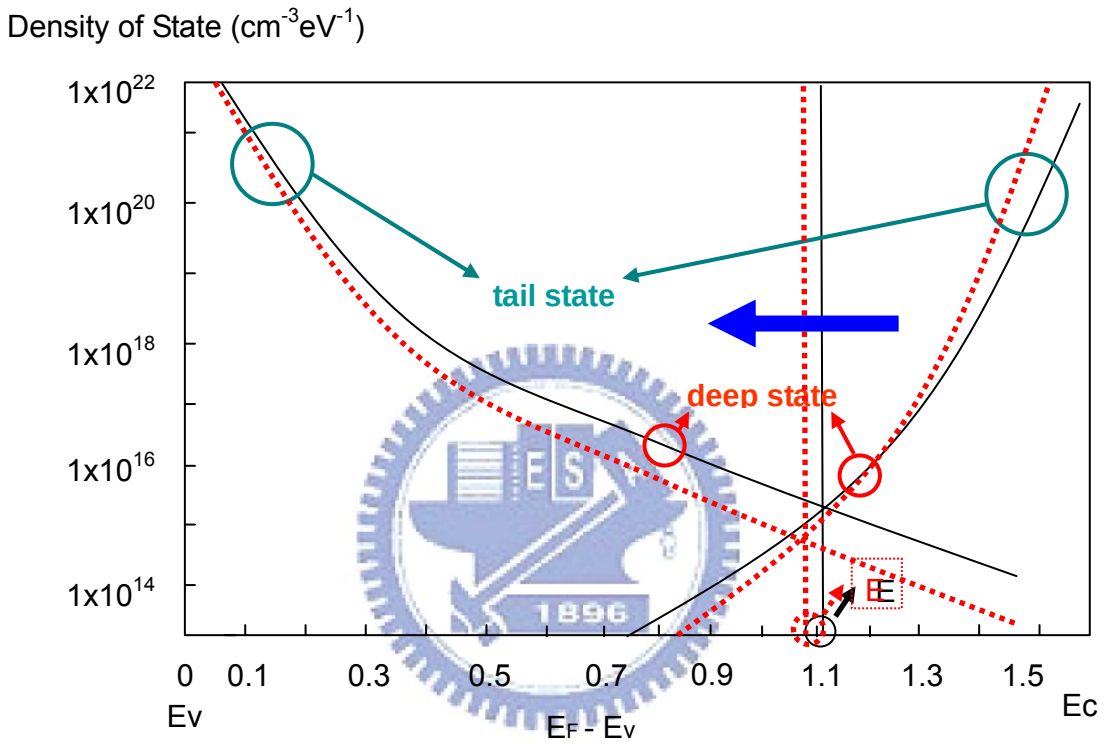
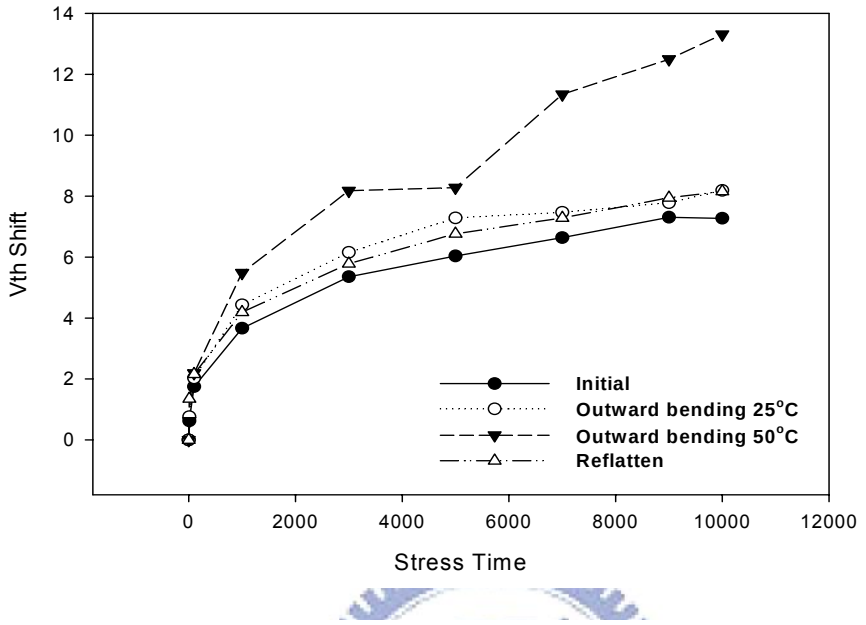


Fig. 3-11

The solid line represents the initial state for flatten status while the dotted line represents the condition under mechanical strain.



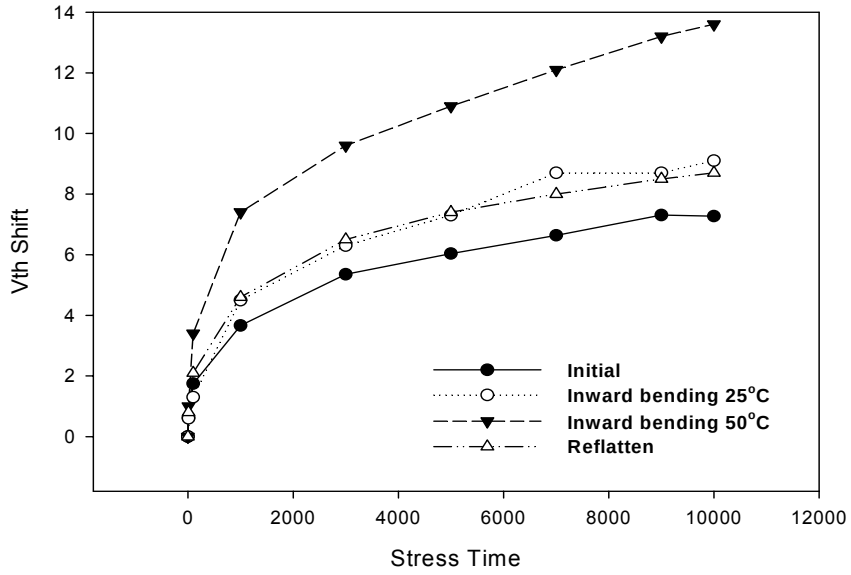
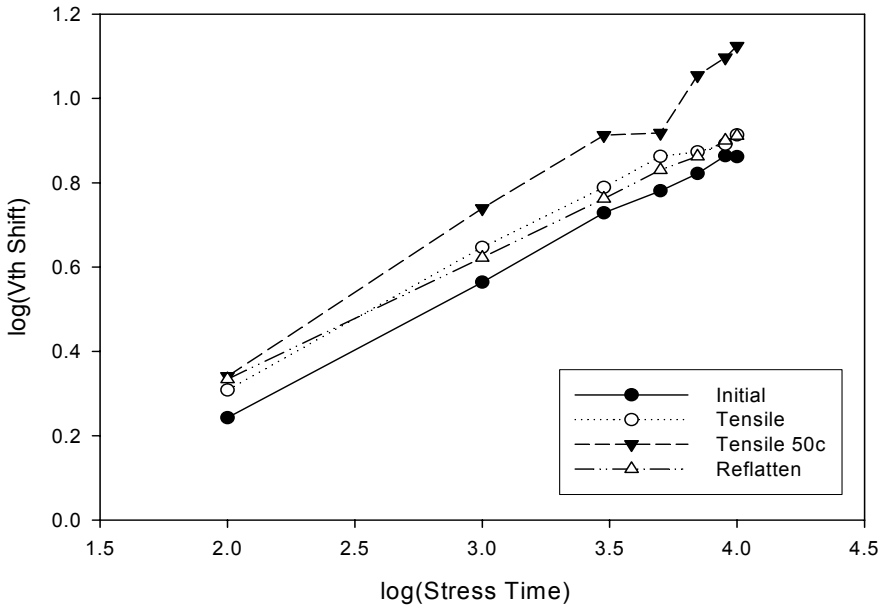


Fig. 3-12

The Vth shift curves of the TFTs of the flexible a-Si TFT before and after 10000 seconds of gate voltage 40V DC stress with different status.



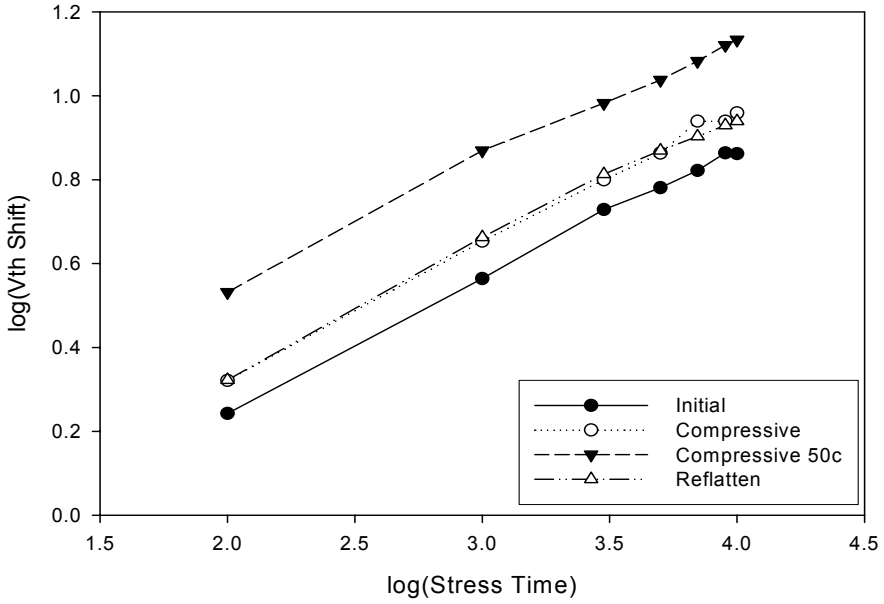


Fig. 3-13

The Vth shift curves using log scales is characterized by a power-law dependence of ΔV_T over time.

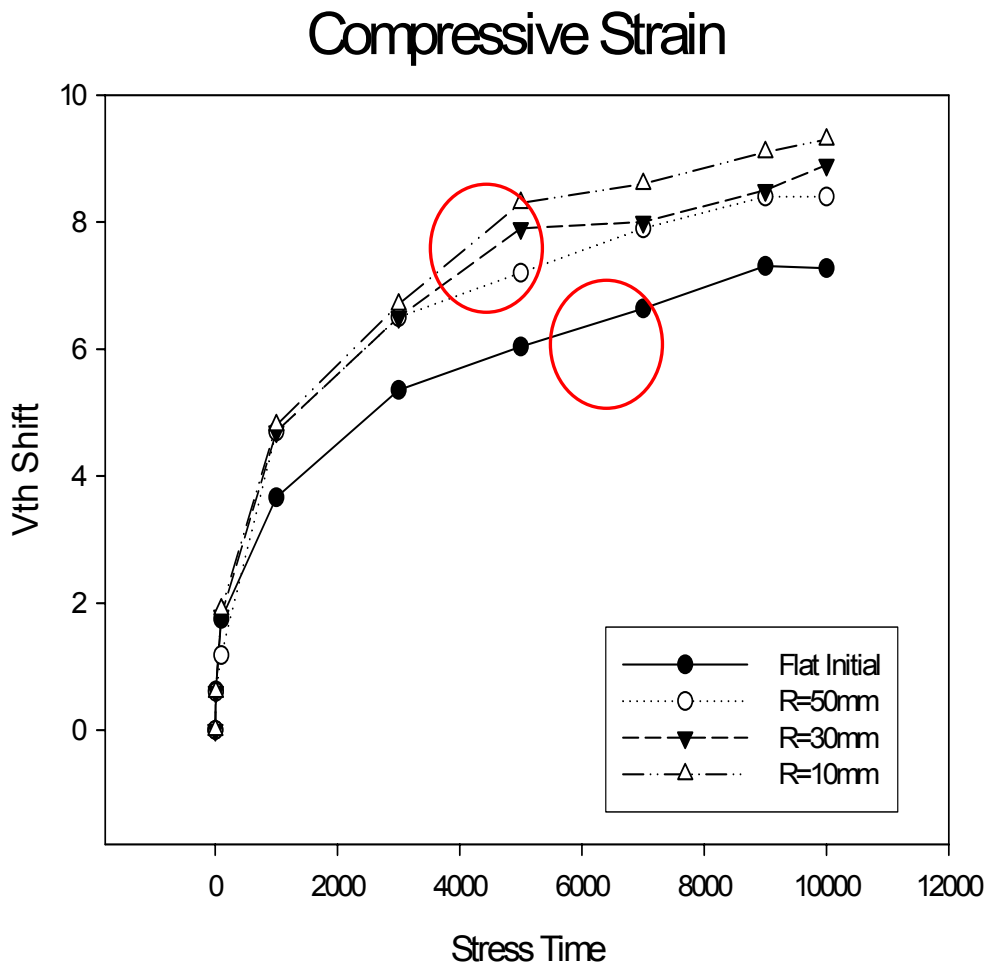


Fig. 3-14

The threshold voltage shift under initial flat status and compressive strain R_n = -10mm, -30mm, and -50mm.

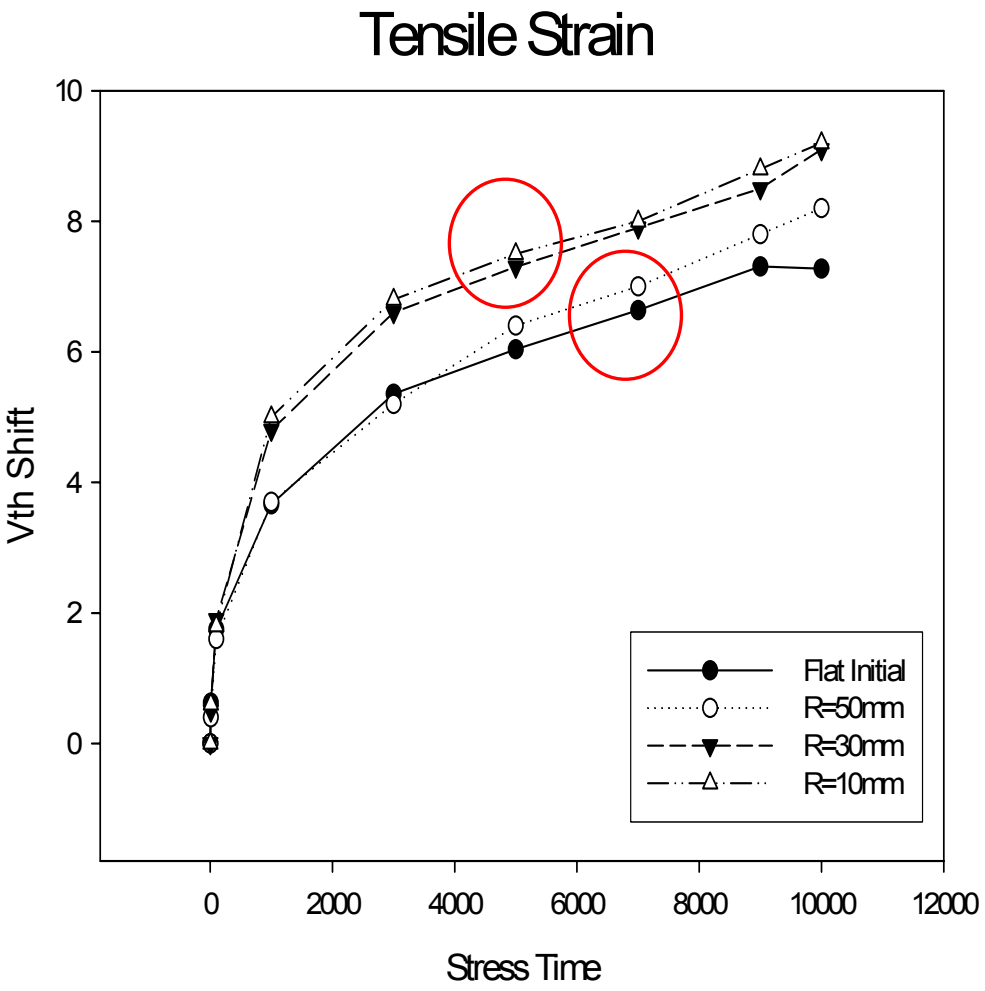


Fig. 3-15

The threshold voltage shift under initial flat status and tensile strain R_p = 10mm, 30mm, and 50mm.

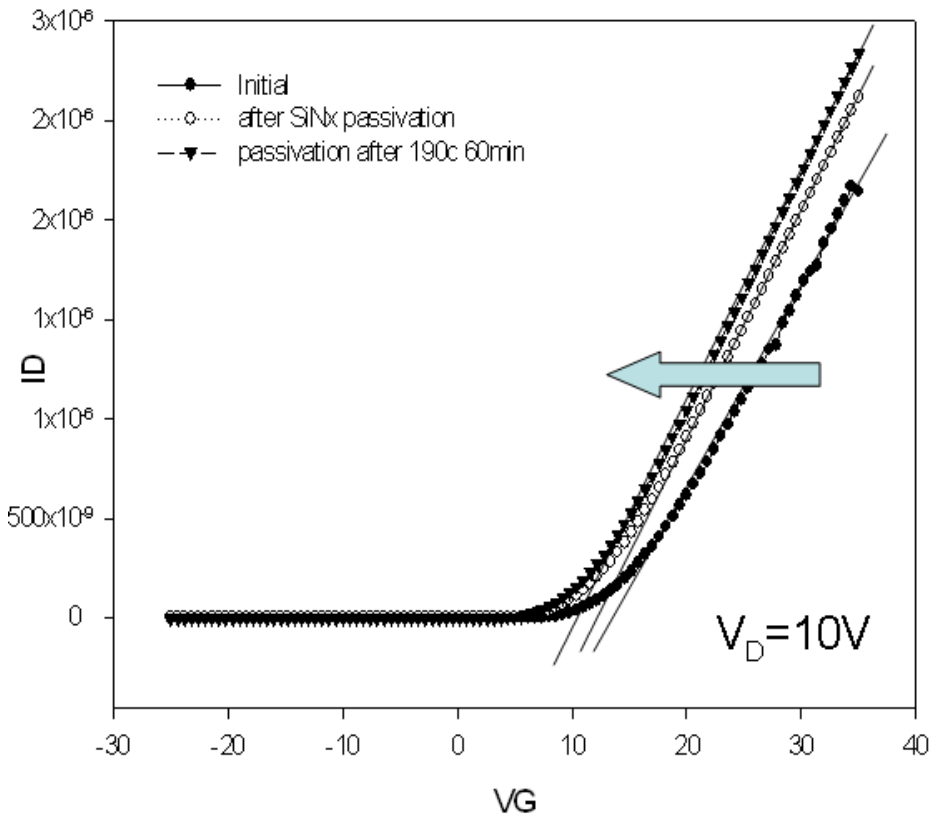


Fig. 3-16

The transfer curves show the comparison of the I_D-V_G figure operated under V_D = 10V of the flexible TFTs with and without passivating layer, and pre-annealing and the post-annealing

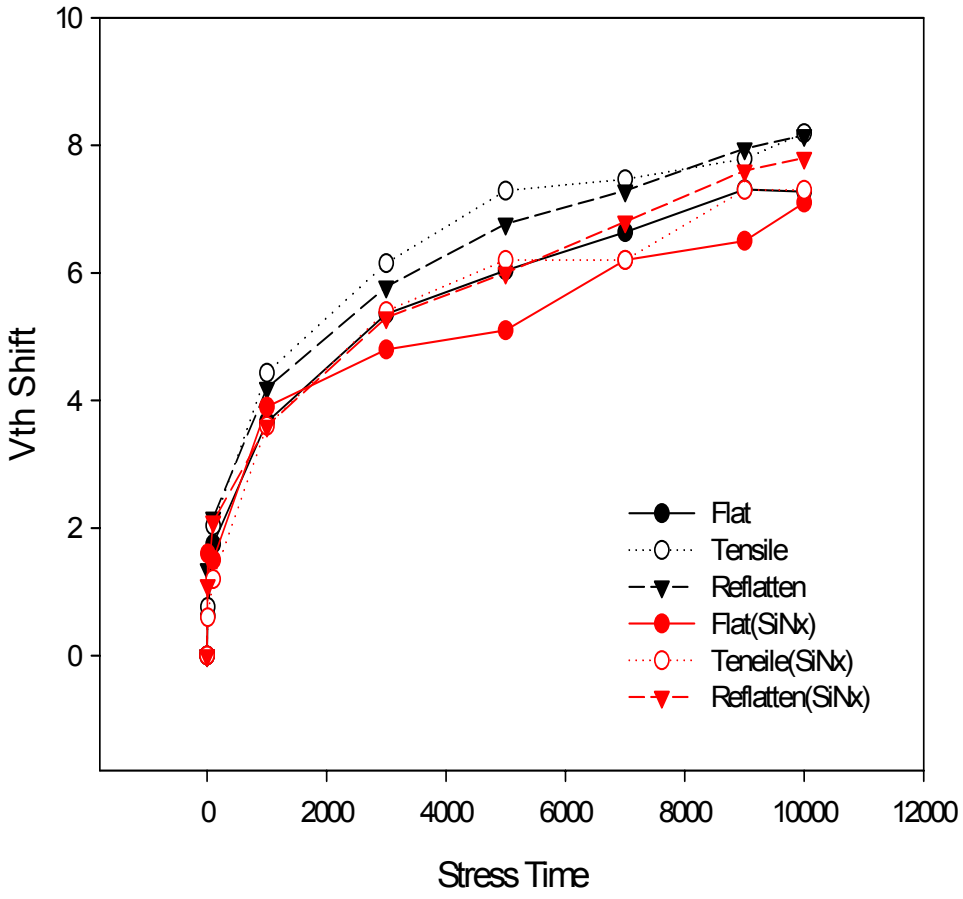


Fig. 3-17

The V_{TH} shift as a function of stress time under flat-tensile strain-reflatten conditions with and without SiNx passivation.

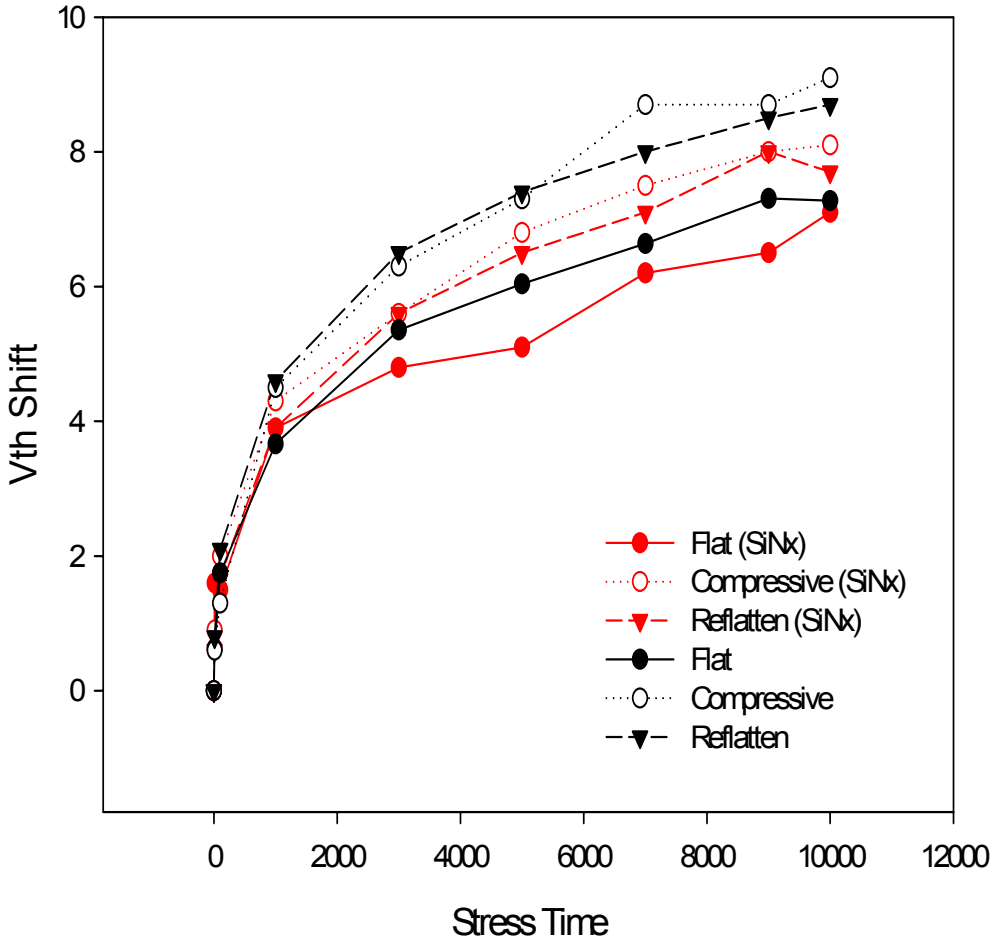


Fig. 3-18

The V_{TH} shift as a function of stress time under flat-compressive strain-reflatten conditions with and without SiNx passivation.

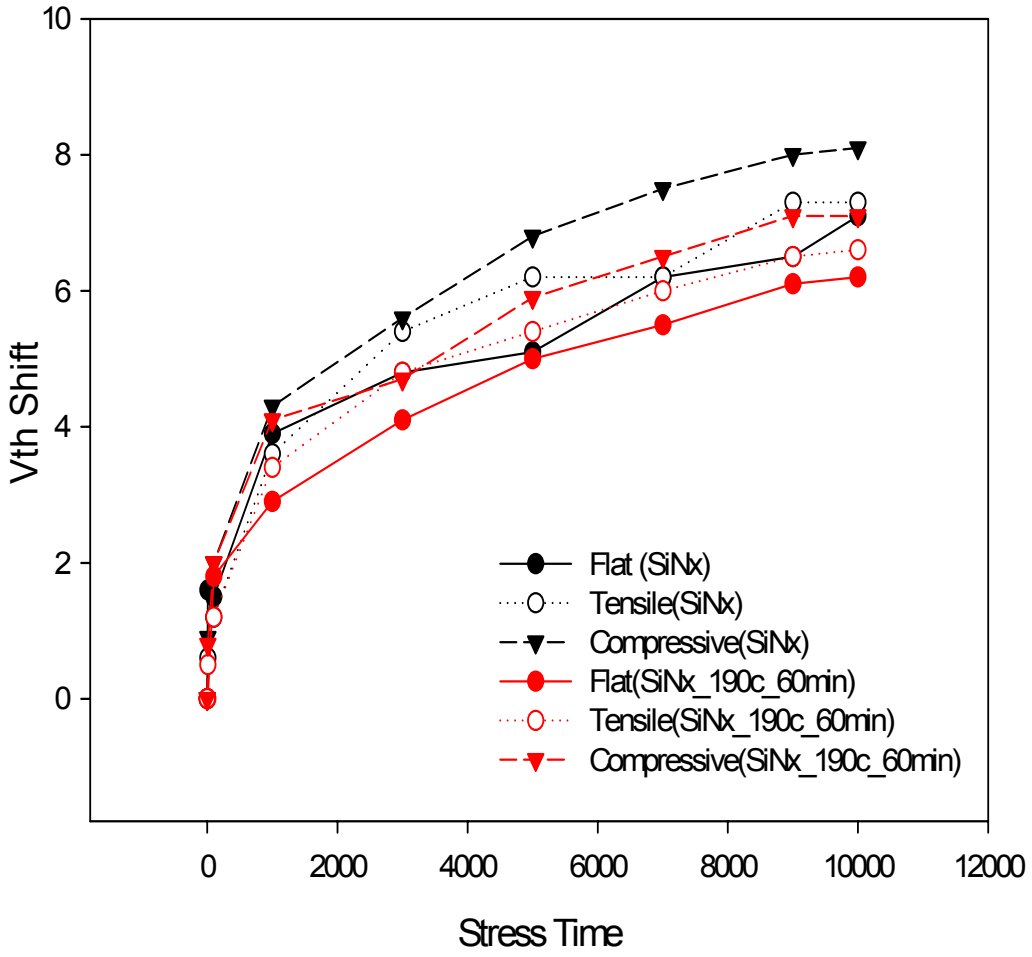


Fig. 3-19

The threshold voltage shift under three different conditions, including flat, tensile, and compressive status comparing the sample with and without post-annealing process.

Chapter 4

Conclusions

The reliability of mechanically strained a-Si:H TFTs was studied in this work. We start from proposing a flexible a-Si TFT, which is inverted staggered structure with back channel etching method, on stainless steel foil under 190℃ process temperature. The strain stress was applied cylindrically on TFTs and parallel to the active channel path of it. Experimental results indicated the influence of mechanical strain was permanent, which can obviously impact the threshold voltage, sub-threshold swing and mobility of TFTs. We could find the variation of threshold voltage shift ($\triangle V_{th}$) in the I_D-V_G results. When the sample was bent at the first time, a-Si:H material would suffer from a mechanical stress, and was easy to break the weak Si-Si bond in it. The phenomenon of $\triangle V_{th}$ was related to the creation of dangling bonds in acceptor-like state which originated from the broken of weak bonds in donor-like state. That explained the permanent strain effect on device, and had seldom V_{th} variation under bending strain afterward. The stability measurement was performed by DC gate bias stress and lasted up to 10^4 seconds By changing the temperature condition in gate bias stress experiment, we could infer the state creation mechanism was dominated in our bias stress condition because of the temperature-dependence relationship. This V_{th} metastability mechanism strongly proposed our model for the difference between the-first-time bending and the multi-time bending performance. And we find a consistent result indicating that the compression will cause

more degradation on flexible a-Si TFT than tension.

Via extracting the parasitical resistance and activation energy, we have some probing conclusions about the change of electrical performance when flexible a-Si TFT is applied bending force. The mechanism of strained degradation is independent of parasitical resistance. And then the activation energy analysis supports the conclusions we made for variation of the mobility and threshold voltage under mechanical strain.

In this thesis, we also have investigated the electrical stability of flexible a-Si TFT under mechanical strain with and without silicon nitride passivating layer. The process temperature of flexible a-Si:H TFTs, including the passivating silicon nitride layer, was well-controlled below 200℃. The bias stress result indicated the a-Si:H TFTs with passivation layer was improved, and the threshold voltage (V_{th}) have less variation under both outward and inward bending. By following the industrial process, we performed 190℃ post-annealing process while the TFTs were completely fabricated. The V_{th} was shifted left and the reliability of flexible TFTs become better than that without post-annealing process. That's related to the passivating effect of hydrogen ion under passivation layer and post-annealing process.

Reference

Chapter 1

[1.1] R. Baeuerle, J. Baumbach, E. Lueder, and Siegordner, in SID '99 Digest, Society of Information Display, p. 14 (1999).

[1.2] M. J. Powell, *The physics of amorphous-silicon thin-film transistors*, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 36. NO. 12. DECEMBER 1989

[1.3] M. J. Powell. B. C. Easton, and D. H. Nicholls., *Annealing and light induced changes in the field effect conductance of amorphous silicon*, J. Appl. Phys., vol. 53, pp. 5068-5078, 1982

[1.4] M. Shur and M. Hack, *J. Appl. Phys.*, vol. 53, pp. 3831-3842., 1984

[1.5] M. Grunewald. P. Thomas, and D. Wurtz, *Phys. Status Solidi (b)*, vol. 100, pp.139- 143, 1980

[1.6] R. L. Weisfield and D. A. Anderson, *Phil. Mug. B*, vol. 44, pp. 83-93, 1981.

[1.7] T. Noda. Y. Ogawa, and T. Kurobe, *Trans. IECE (Japan) E*, vol. 64. pp. 134-140, 1981.

[1.8] F. Djamdji and P. G. LeComber. *Phil. Mag. B*, vol. 56, pp. 31-50, 1987.

[1.9] H. Gleskova, S. Wagner V. Gasparik and P. Kovac, *150°C Amorphous Silicon Thin-Film Transistor Technology for Polyimide Substrates*, Electrochem. Soc. 148 (7) G370-G374 (2001)

[1.10] H. Gleskova and S. Wagner, *Amorphous silicon thin-film transistors on compliant polyimide foilsubstrates,* IEEE Trans. Electron Devices, VOL. 20, NO. 9 (1999)

[1.11] Sigurd Wagner, Helena Gleskova, I-Chun Cheng, Ming Wu, *Silicon for thin-film transistors* , Thin Solid Film, 430 15–19 (2003)

[1.12] Z. Suo, E. Y. Ma, H. Gleskova and S. Wagner, *Thin-film transistor circuits on*

large-area spherical surfaces, Appl. Phys. Lett., 81, 2091 (2002)

[1.13] A. Sazonov and A. Nathan. , *120 °C fabrication technology for a-Si:H thin film transistors on flexible polyimide substrates*, J. Vac Sci. Technol. A, 18, 780 (2000)

[1.14] M.J Powell, *Charge trapping instabilities in amorphous silicon-silicon nitride thin-film transistors,* Appl. Phys. Lett. 43, pp.597, Jul 1983.

[1.15] A. R. Hepburn, J. M. Marshall, C. Main, M. J. Powell, and C. van Berkel, *Metastable Defects in Amorphous-Silicon Thin-Film Transistors*, Phys. Rev. Lett. 56, 2215 - 2218 (1986)

[1.16] C. van Berkel and M. J. Powell, *Resolution of amorphous silicon thin-film transistor instability mechanisms using ambipolar transistors,* Appl. Phys. Lett. **51**, 1094 (1987)

[1.17] S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur, and J. Jang, *Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate*, J. Electrochem. Soc., 151, G167 (2004).

[1.18] H. Gleskova and S. Wagner, *Electron mobility in amorphous silicon thin-film transistors under compressive strain*, Appl. Phys. Lett., 79, 3347 (2001).

[1.19] H. Gleskova, P. I. Hsu, Z. Xi, J. C. Sturm, Z. Suo, and S. Wagner, *Field-effect mobility of amorphous silicon thin-film transistors under strain* , J. Non-Cryst. Volumes 338-340, 15 June 2004, Pages 732-735.

Chapter 3

[3.1] Sung Hwan Won, Jang Kyun Chung, Chang Bin Lee, Hyun Chul Nam, Ji Ho Hur, and Jin Jang, *Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate*, .J. Electrochem. Soc., Volume 151, Issue 3, pp. G167-G170 (2004)

[3.2] H Gleskova, S Wagner, W Soboyejo, Z Suo, *Electrical response of amorphous silicon thin-film transistors under mechanical strain,* Journal of Applied Physics 92, 6224 (2002)].

[3.3]K.terada and H.Muta, "*A New method to Determine Effective MOSFET Channel length,*" Jap. J. Appl. Phys., 18(5), 935(1979)

[3.4]J. G. J. Chern, P. Chang, R. F. Motta, and N. Godinho, "*A New Method to Determine MOSFET Channel Length*," IEEE Electron Device lett. 1(9), 170(1980)

[3.5] R. E. I. Schropp, J. Snijder, and J. F. Verwey, *A self-consistent analysis of temperature-dependent field-effect measurements in hydrogenated amorphous silicon thin-film transistors,* J. Appl. Phys. 60**,** 643 (1986);

[3.6] R. Schumacher, P. Thomas, K. Weber, W. Fuhs, F. Djamdji, P. G. Le Comber; R.E.I. Schropp, "*Temperature-dependent effects in field-effect measurements on hydrogenated amorphous silicon thin-film transistors*", Philosophical Magazine Part B, Volume 58, Issue 4 October 1988 , pages 389 – 410

[3.7] M. J. Powell, C. van Berkel, A. R. Franklin, S. C. Deane and W. I. Miline , "*Defect pool in amorphous –silicon thin-film transistors*,' Phys. Rev. B, vol.45, pp.4160-4170, Feb. 1992