國立交通大學

電機學院光電工程學系
顯示科技研究所

碩士論文

低溫複晶矽薄膜電晶體於背光下之電性研究

Study on Electrical Characteristic of Low Temperature Polycrystalline Silicon Thin Film Transistors under Illumination

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碩士論文

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摘要

近年來液晶顯示器的需求急速升溫，中小尺寸高亮度高對比的顯示器需求也是成長近乎供不應求，例如在投影元件應用、行動通訊以及車用面板上都是。然而亮度提高相對的也會提高薄膜電晶體元件的光漏電流，此一漏電流的提高，會降低畫面顯示的對比度以及顯示顏色的偏差。因此降低或抑制元件在高亮度下的光漏電流是重要的。

本論文中，先提出了一種具有金屬遮光層的薄膜電晶體。與傳統電晶體的差異為在其緩衝層底部沉積一層不透光的金屬材料，藉此隔絕光線直接入射至主動層。雖然此種新式結構可以有效的抑制光漏電效應，但由於本身結構使然，這種元件會受到汲極電壓與金屬遮光層的耦合效應，使得起始電壓在不同的汲極電壓操作下會有飄移的問題。為了改善耦合效應，在此研究中更近一步提出二種不同結構的遮光層元件，其金屬遮光層皆非完全覆蓋，預期能改善起始電壓飄移的問題。

第一種元件具有不連續的金屬遮光層，有效降低起始電壓飄移的幅度。且其遮光層的缺口可控制光線入射的位置，用來釐清照光產生光漏電的機制，並提出一物理模型。

第二種為局部遮光層的元件，完全解決了起始電壓飄移的問題。在線性區的操作下，能有效抑制光漏電，但是在飽和區的操作，受到汲極電壓與金屬遮光層的耦合效應，造成光漏電上升，同時也提出一物理模型來解釋此現象。

此外，我們利用不連續金屬遮光層的元件，釐清照光時次臨界擺幅劣化的原因，並提出一物理模型。

最後，為了模擬元件在實際應用時的衰退，分別在暗態及亮態的環境下做了直流電壓以及交流電壓的可靠度測試，並提出薄膜電晶體在亮態下操作的衰退機制。

Study on Electrical Characteristic of Low Temperature Polycrystalline Silicon Thin Film Transistors under Illumination

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English Abstract

The market for liquid crystal displays has been rapidly expanding in recent years. The demand for a high luminance and a high contrast ratio in liquid crystal displays (LCDs) is continuing to grow and seems insatiable. However, high luminance would increase photo leakage current (PLC) in the TFTs, which would cause a low contrast ratio. Consequently, it is necessary to suppress the PLC in LCDs with high illumination.

In this thesis, the Poly-Si TFT with a metal shielding layer is proposed. The metal shielding layer was deposited before buffer layer to block light beams directly illuminated on the active layer. The Metal-Shielding TFT has lower OFF-Current under illumination, but it induces another issue which is threshold voltage shift. In order to overcome the issue, the Split-Shielding TFT and Partial-Shielding TFT are proposed.

The metal layer in Split-Shielding TFT is not continuous; it reduces the ratio of threshold voltage shift. In addition, the split location of metal layer can control the exposed region of active layer. Based on the experiment results, the model is proposed to explain the relationships of photo leakage current with exposed region.

The Partial-Shielding TFT solves the issue of threshold voltage shift absolutely. It has lower OFF-Current under illumination in linear region, but not in saturation region. A model is proposed to explain the phenomenon. Besides, the mechanism of the degradation of sub-threshold swing in poly-Si TFT which is exposure to back-light is clarified.

Finally, we also apply the DC bias stress and AC bias stress on the device to test the devises stability under dark and illumination respectively. According to the result of this experiment, a model is proposed to explain the degradation under illumination.

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林威廷 2008 年 6 月

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Chapter 1 Introduction

1.1 Overview of Low-Temperature Polycrystalline Silicon Thin Film Transistors

Thin film transistor (TFT) is a metal-oxide-silicon field effect transistor (MOSFET) fabricated on an insulator substrate by employing all thin film constituents. Thin film transistors have been widely used as switching devices in flat panel display, such as active-matrix liquid crystal display (AMLCDs)[1]-[3], and organic light-emitting displays (OLEDs)[4]. Except large area displays, Poly-Si TFTs have been applied into some memory devices such as dynamic random access memories (DRAMs)[5], static random access memories (SRAMs)[6], electrical programming read only memories (EPROM)[7], electrical erasable programming read only memories (EEPROMs)[8]. Poly-Si TFTs are also very potential to be used on devices such as linear image sensors [9], thermal printer heads [10], photodetector amplifier[11], scanner[12], neutral networks[12], and three dimension LSIs [13]. Especially, the application in AMLCDs is the major reason to push the Poly-Si TFTs technology programming rapidly.

Poly-silicon is a silicon-based material, which contains numerous Si grains with sizes ranging from 0.1 to several um. In semiconductor manufacturing, poly-silicon is usually prepared by LPCVD (Low Pressure Chemical Vapor Deposition) and then annealed above 900 C, i.e. so called SPC (Solid Phase Crystallization) method. Obviously, the same way could not be applied on the flat panel display industry since glass's strain temperature is only about 650 C. Therefore, Low temperature poly-silicon (LTPS) technology is the novel technology specific for the flat panel display application. Presently there are several approaches in the preparation of LTPS film on glass or plastic substrate：Metal Induced Crystallization (MIC)、Cat-CVD、Laser anneal.

The preparation of LTPS film is apparently more complicated than a-Si, but LTPS TFT has 100 times higher mobility than a-Si TFT and can carry out CMOS process on the glass substrate. The Poly-Si TFTs are currently investigated for applications in AMLCD. The possibility to integrate on the same substrate driving circuitry as well as switching devices seems to represent a major advantage of the poly-silicon technology over the amorphous silicon on, because the mobility of Poly-Si TFTs is usually larger than that of the amorphous silicon TFTs, for Poly-Si TFTs, a mobility larger than 50 cm^2/v-s is easily achieved by presently mature technology, that is enough to used as peripheral driving circuits. Therefore the pixel array and the peripheral circuits can be made on the same glass, bring the era of system-on-glass (SOG) technology. The process complexity can be greatly simplified to lower the cost. In addition, due to the higher mobility of Poly-Si TFTs , the dimension of the Poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high density、high resolution AMLCDs.

In small size AMLCD application, such as the projector, which must be high resolution and small size to reduce the cost associated with the projection optical system and remain the graphic quality. On the other hand, Poly-Si TFTs also play the role of light shutters in projection display. The higher durability against luminance and heat is required because those devices are placed close to a high-power lamp. Undoubtedly, Poly-Si TFT technology is the most promising approach.

However, some problems still exist in applying Poly-Si TFTs on large-area displays. In comparison with single-crystalline silicon, Poly-Si is rich in grain boundary defects as well as intra-grain defects, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of Poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously[14]. Moreover, the relatively large leakage current is one of the most important issues of conventional Poly-Si TFTs under OFF-state operation[15]-[16]. The dominant mechanism of the leakage current in poly TFTs is field emission via grain boundary traps due to the high electric field near the drain junction. To solve these problems, some crystallization methods such as excimer laser annealing (ELA) have been introduced to enlarge the grain size[17]. A drain offset region or lightly-doped drain (LDD) region is used to effectively lower leakage current by decreasing drain electric field[18]. Now, some studies of Poly-Si TFTs also focus on developing new technologies to lower the maximum fabrication temperature, which enables the use of low-quality glass and therefore reduce production cost[19]. Some reported papers focus on the fabrication and characterization of small-dimensional Poly-Si TFTs[20], which has high driving ability and high resolution and can be applied on AMLCD peripheral circuitry or the high-resolution projectors. In summary, it is expected that the Poly-Si TFTs will becomes more and more important in future technologies, especially when the 3-D circuit integration era is coming. More researches studying the related new technologies and the underlying mechanisms in Poly-Si devices with shrinking dimensions are therefore worthy to be indulged in.

1.2 Motivation

The market for liquid crystal displays has been rapidly expanding in recent years. The demand for a high luminance and a high contrast ratio in liquid crystal displays (LCDs), such as small-medium LCDs for projection device, mobile displays and displays for cars, is continuing to grow and seems insatiable. However, high luminance would increase photo leakage current (PLC) in the TFTs, which diminishes the voltages that are held across the pixel electrodes or affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. For instance, the off current of Poly-Si TFTs exposure at the 2160nits backlight is higher that in the dark, which is about higher three order. Fig.1.1.1 shows the I_D-V_G transfer curves of standard Poly-Si TFT at the linear operation under the dark and photo states. The leakage current of Poly-Si TFTs in the dark was around 10^{-14} A as the gate bias is varied from 0 to -12 V. With the same range of gate bias, the leakage current of Poly-Si TFTs under illumination is as high as three orders of magnitude, about 10^{-11}A. It is clearly observed that the on/off current ratio of Poly-Si TFTs was substantially decreased to seriously affect the function of TFTs used as the pixel switch under illumination environment. In addition, the sub-threshold swing is increased under illumination, about 0.49 V/decade, as the initial value in dark is 0.28 V/decade. The variation of sub-threshold swing is about 75%. Since the light from back-light is mainly absorbed at the interface of Poly-Si and the glass substrate, plenty of light-induced electron-hole pairs are accumulated in the bottom of Poly-Si film to generate the I_{PLC}.

We proposed a light-shielding structure, it used an opaque material to shield the light. It is the most effective to cut-off the light from the backlight source. And we make the shielding layer with several kind structures. The first is full shielding layer, second is split shielding layer, and finally the partial shielding layer.

1.3 Organization of This Thesis

This thesis is divided into four chapters. After a brief introduction given in Chapter 1, the fabrication of the poly-Si TFTs device structure in Chapter 2 has been described. In addition, brief descriptions about the instruments for cryogenics system and current-voltage (I-V) measurement are also included. At the end, we describe the methods of device parameter extraction.

In Chapter 3, the photo leakage current of poly-Si TFT with full shielding structure, split shielding structure, and partial shielding structure has been measured. Then, we describe the photo leakage current mechanism of poly-Si TFT, giving a brief description about the degradation mechanism of sub-threshold swing when measurement under illumination.

In Chapter 4, brief descriptions about the DC stress definition and the degradation mechanism of DC stress under darkness and illumination are given. We also give descriptions about the AC stress definition and the degradation mechanism of AC stress, showing and analyzing the electrical characteristics of poly-Si TFTs with various AC stress conditions under darkness and illumination.

Finally, we summarize our conclusion in Chapter 5.

Chapter 2 Device Fabrication and Experiment

2.1 Fabrication Process of Poly-Si TFTs

The top gate n-channel and self align light drain doping (LDD) TFTs were fabricated on Corning1737 glass substrate [21]. First, the buffer SiNx/oxide layer and 50 nm thickness a-Si:H film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, we dehydrogenated aSi:H film in a furnace at 450℃. Then the poly silicon channel was formed by 308nm XeCl excimer laser irradiation at 350mJ/cm^2. In this work, 95% laser overlap ratio was adopted to obtain large grain size and better uniformity of active layer. As the SEM Fig.2.1.1, the average grain size of polycrystalline silicon was found to be 280~300nm [22]. The island was patterned by plasma dry etching Fig.2.1.2. The 100nm thickness gate insulator was deposited by TEOS (Tetra-Ethyl-Ortho-Silicate)-base oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed at 530℃/1hr thermal furnace and RTA irradiation, as shown in Fig.2.1.3-2.1.4. Finally, the interlayer oxide and inter-connection metal were deposited and pattern. The H2 plasma hydrogenation was performed in a commercial RF parallel-plate plasma reactor at 100W, 480℃ 15min in H2 and Argon gas mixture. The SiO2/SiNx with 300nm and 100nm interlayer film and source/drain contact holes etching and S/D metal patterning, as shown in Fig. 2.1.5. Finally, the planer layer (UHA2) and ITO were employed on our device Fig.2.1.6 [23]-[25]; the device electrical measurements were finished by HP4156C.

2.2 Devices Structure of Metal Shielding layer

Fig.2.2.1 was shown the shielding structure with molybdenum (Mo), it was oversimplification and directly perceived way to suppress or cutoff the backlight to reach the Poly-Si active layer. The section 2.3 specified how the process to be implemented.

2.3 Experimental procedure of Metal Shielding Layer Structure

The n-channel Poly-Si TFTs with LDD structure were fabricated on Corning1737 glass substrate. First of all, a 50nm thick molybdenum film was sputtered and was patterned using additional mask to be a shielding layer on the glass substrate. The buffer layer and a thin 50 nm-thick undoped a-Si film were sequentially deposited by PECVD at 380℃, followed by dehydrogenated via furnace annealing process at 450℃. Then the a-Si films were crystallized by 308nm XeCl excimer laser with the line-shaped beam power of 350mJ/cm^2. The 100nm thickness gate insulator was deposited by TEOS oxide. The source/drain regions were defined by a mask and formed by the mass-separated ion implanter technique. Then, MoW was sputtered and patterned as a gate metal [26]. Following, implantation for LDD region is preformed on overall device after the S/D photoresistor is removed. The doping activation was performed by RTA irradiation. The dimensions of TFTs in this work were L = 18 μm, W = 18 μm and the LDD length is 1.25 μm.

2.4 Introduction of Instruments

The electrical test setup of HP4156C semiconductor parameter analyzer is utilized in this experiment, illustrated in Fig.2.4.1, a probe station is situated inside a dark box. The ground probe station is furnished with an electrically isolated, water-cooled thermal chuck. The chuck is controlled by Temptronic TPO315A thermal controller, which can operate temperature from 25°C to 300°C. An Agilent 4156C precision semiconductor parameter analyzer can provide I-V measurement, bias for BTS, and quasi C-V measurement, etc. We employ the ICS (Interactive Characterization Software) to obtain the output and transfer characteristics, like V_D- I_D, V_G- I_D (Linear), V_G- I_D (saturation), and extract the typical semiconductor parameters.

2.5 Electrical Characterization Measurement and Analysis

2.5.1 Output characteristics

The typical TFT output characteristics are shown in Fig.2.5.1. They represent the dependence of the Drain-Source current (I_{DS}) on the Drain-Source voltage (V_{DS}) at different gate voltage (V_{GS}). The Drain-Source current increase linearly at low Drain-Source voltage (Linear regime/operation) and saturates at high Drain-Source voltage (Saturation regime /operation). The saturation values of I_{DS} depend on the applied gate voltage. When the low gate voltage is applied, the thickness of the induced channel is small and current is low. On the other hand, thicker channel is induced at high gate voltage and the saturation current is higher. Well-separated output characteristics are an indication of good ohmic contact at drain and source. The transistor enters in saturation regime when $V_{DS} > V_{SAT}$, where $V_{SAT}=V_{GS}-V_T$. In I_D-V_D curve, the points corresponding to $V_{DS} = V_{SAT}$ are connect the blue line described the following equation:

$$I_{DS} = \frac{1}{2} \times \mu_{fe} \times Cox \times \frac{W}{L} \times \left[(V_{GS} - V_T)^2 \right] \tag{2-1}$$

When W and L are the width and length of the transistor channel, μ_{fe} is the field-effect electron mobility and C_{ox} is the gate insulator capacitance. The threshold voltage and the field mobility effect mobility can be determined from measuring the saturation current, plotting the square root of the measured I_{DS} vs. V_{GS} in saturation ($V_{DS} \geqq V_{GS}-V_T$).

Of course, the Poly-Si TFTs are not perfect device as the single crystalline; it is since the grain boundary [27]. The region of operation in Poly-Si TFT roughly:

A. Cut-off : Current is due to reverse-bias drain junction leakage trap-assisted mechanisms.

B. Subthreshold : Current is due to carrier diffusion. Limited by source junction potential barrier.

C. Pseudo-subthreshold : Current is due to carrier drift. Inversion-charge density Q_{inv} increases ~linearly with V_G-V_T. The field mobility μ_{fe} increases ~ exponentially with V_G → I_D increases ~ exponentially with V_G.

D. Above threshold : Current is due to carrier drift, Qinv V_G-V_T; μ_{fe} ~ constant → I_D increases linearly with V_G

Refer to the Fig.2.5.2.

2.5.2 Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameter extraction such as the threshold voltage V_T, subthreshold swing S.S, field-effect mobility μ_{FE} from the device characteristics.

Several methods are used to determinate the threshold voltage, V_T , which is the most important parameter of the semiconductor devices. The method to determinate the threshold voltage in this thesis is the constant drain current method, the voltage at a specific normalized drain current NI_D is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the specific normalized current $NI_D = I_D/(W/L)$ is defined at 10nA for V_D operated in linear region and 100nA for V_D operated in saturation region, to extract the threshold voltage of TFTs in most papers.

The subthreshold swing S.S (V/dec) is a significant parameter to describe the control ability of gate bias toward drain current and the efficiency of the switch turning on and off. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. It should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to the short-channel effects such as charge sharing, avalanche multiplication, and punch through-like effects. It is also related to the gate voltage due to some undesirable factors such as serial resistance and interface state. In this experiment, the subthreshold swing is defined as one-second of the gate voltage required to decrease the threshold current by two orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to the threshold voltage.

The field-effect mobility (μ_{FE}) is determined from the transconductance g_m at low drain voltage (linear region). The transfer characteristics of Poly-Si TFTs are similar to those of conventional MOSFETs, ignoring any other non-ideal effect and assuming the electric field in the channel is uniform, so the first order I-V relationship in the bulk Si MOSFETs can be applied to the Poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_T)V_D - \frac{1}{2} {V_D}^2] \qquad (2\text{-}1)$$

where C_{ox} is the gate oxide capacitance per unit area

W is channel width

L is channel length

V_T is the threshold voltage.

If V_D is much smaller than (V_G-V_T) (i.e., $V_D << V_G-V_T$) and $V_G > V_T$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} (V_G - V_T) V_D \qquad (2\text{-}2)$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D = const.} = \frac{W C_{ox} \mu_{FE}}{L} V_D \qquad (2\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m \qquad (2\text{-}4)$$

The mobility value was taken from Equation (2-4) with maximum μ_{FE}.

The extraction method of the trap density N_t is following. From the Seto's model, the grain boundary potential barrier height V_B can be expressed by the following equation

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^2}{8\varepsilon_s n} \qquad \text{(2-5)}$$

where V_B is the grain boundary potential barrier height

n is the carrier concentration

N_t is the grain boundary trap density

The grain boundary potential barrier height V_B is related to the carrier concentrations inside the grain and the trapping states located at grain boundaries. Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of Poly-Si TFTs. As proposed by Levinson et al. [28], the I-V characteristics including the trap density can be obtained by the following equation

$$I_D = \mu_0 C_{ox}\frac{W}{L}\left(V_G - V_{TH}\right)V_D \exp\left(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}\left(V_G - V_{TH}\right)}\right) \qquad \text{(2-6)}$$

This equation had been further corrected by Proano et al. by considering the mobility under low gate bias [29]. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}\left(V_G - V_{FB}\right)} \qquad \text{(2-7)}$$

The drain current of Poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_G - V_{FB}) V_D \exp\left(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox} / \varepsilon_s}}{C_{ox}^2 (V_G - V_{FB})^2} \right) \tag{2-8}$$

The effective trap state density then can be obtained from the slope of the curve $\ln\left[I_D / \left(V_G - V_{FB} \right) \right]$ versus $\left(V_G - V_{FB} \right)^{-2}$ as in Fig.2.5.3 and we can calculate the slope from it. The grain boundary trap-state density can be determined from the square root of the slope directly, expressed by the simplified equation below.

$$N_{trap} = \frac{C_{ox}}{q} \sqrt{|Slope|} \tag{2-9}$$

Chapter 3 Poly-Si TFT with Metal Shielding Layer

3.1 Full Metal Shielding TFT

The cross-sectional view of proposed TFT is illustrated in Fig.3.1.1. A thin metal film which is deposited on the glass substrate is to block the light emitted into poly-Si thin film. Fig.1.1.1 shows the I_D-V_G transfer curves of standard poly-Si TFT at the linear operation under the dark and photo states. As the gate bias is varied from 0 to -12 V, the leakage current of poly-Si TFTs in the darkness was around 10^{-14}A. With the same range of gate bias, the leakage current of poly-Si TFTs under illumination raises three orders of magnitude, about 10^{-11}A. It is clearly observed that the on/off current ratio of poly-Si TFTs was substantially decreased and seriously affect the function of TFTs used as the pixel switch under illumination environment. In addition, the sub-threshold swing is increased under illumination, about 0.49 V/decade, as the initial value in dark is 0.28 V/decade. The variation of sub-threshold swing is about 75%. Since the light from back-light is mainly absorbed at the interface of poly-Si and the glass substrate, plenty of light-induced electron-hole pairs are accumulated in the bottom of poly-Si film to generate the I_{PLC} [30].

To solve this issue, the poly-Si TFT with full metal shielding structure was proposed. The I_D-V_G transfer curves of proposed poly-Si TFT under the dark and photo states are shown in Fig.3.1.2. It is clearly observed that the I_{PLC} is entirely eliminated in the proposed poly-Si TFT. The leakage current is about 10^{-12} A under illumination at the linear operation, as same as that in the dark state. The sub-threshold slope is also absolutely unchanged under illumination by the light-shielding structure. Fig.3.1.3 shows comparison of the photo leakage current of full metal shielding TFT and convention TFT. The Metal shielding TFT reduce photo leakage well even the brightness enhances to 5620nits.

The drain voltage is 0.1V when measure I_D-V_G relationships in linear region, and in saturation region (drain voltage is 5V, 9V, and 15V). Fig.3.1.4 plots the I_D-V_G relationships of

Full-Metal-Shielding TFT. It is clearly that the V_{TH} of Poly-Si TFT with partial metal shielding layer is dependent of drain bias. The V_{TH} decreases when the drain voltage increases. The V_{TH} is 0.738V when the drain voltage is 0.1V, and the V_{TH} is -1.038V when the drain voltage is 15V. The shift of V_{TH} is 1.776V. The V_{TH} of proposed TFT is dependent of drain voltage so that the drain current would increase with drain bias.

Since the metal film is located under the poly-Si active layer, a parasitic capacitance in the overlap of source and drain side is generated. The positive voltage at drain side would lead to a positive potential distribution, V_M, in the metal film owing to the coupling effect. V_M is regarded as the substrate bias to affect the threshold voltage of the proposed poly-Si TFTs[31]. The threshold voltage shifts in negative are explained by the positive V_M induces the back channel in the bottom of Poly-Si layer shown in Fig.3.1.5. Therefore, the split metal shielding structure for poly-Si TFT is proposed and discussed in the next section.

3.2 Split Metal Shielding TFT

Shown as Fig.3.2.1-3.2.5, there are five kind of Poly-Si TFT with split metal shielding layer. We assign numbers to those devices is M1, M2, M3, M4, and M5. The split of metal shielding layer located at different place. The split of M1 device is the nearest to the Source, and followed by M2, M3, M4, and M5.When we put a light source under the device, the light beams will go through the splits to different location of semiconductor layer.

Fig.3.2.6-3.2.7 plots the I_D-V_G relationships of M1 and M2 devices. It is found that the V_{TH} shift slightly when compare with full metal shielding TFT. Fig.3.2.8-3.2.10 plots the I_D-V_G relationships of the M3, M4 and M5 devices. It is clearly that the V_{TH} of poly-Si TFT with split metal shielding layer is independent of drain bias. The detail results are listed in Table.1.

Then, we want to know where the critical region is to induce photo leakage current when the device exposure with light. Fig.3.2.11 shows the I_D-V_G relationship of M1 device and Full-Metal-Shielding device with the drain voltage is 0.1V. Measuring in darkness environment, the photo leakage current of M1 device and Full-Metal-Shielding device are the same. Fig.3.2.12 shows the I_D-V_G relationship under darkness and the drain voltage is 9V. Fig.3.2.13 shows the I_D-V_G relationship under 5620nits brightness and the drain voltage is 0.1V. Fig.3.2.14 shows the I_D-V_G relationship under 5620nits brightness and the drain voltage is 9V. The photo leakage current of M1 still keep the same with Full-Metal-Shielding device. It determines that the light beams go through the split in M1 device will not affect photo leakage current. The electron-hole pairs produced by light cannot separate and diffuse to Drain no matter the capacity of drain voltage. The electrons and holes will combine in recombination center, Shown as Fig.3.2.15.

Fig.3.2.16 shows the I_D-V_G relationship of M2 device and Full-Metal-Shielding device with the drain voltage is 0.1V. Measuring in darkness environment, the photo leakage current of M2 device and Full-Metal-Shielding device are the same. Fig.3.2.17 shows the I_D-V_G relationship under darkness and the drain voltage is 9V. Fig.3.2.18 shows the I_D-V_G relationship under 5620nits brightness and the drain voltage is 0.1V. Fig.3.2.19 shows the I_D-V_G relationship under 5620nits brightness and the drain voltage is 9V. The photo leakage current of M2 still keep the same with Full-Metal-Shielding device. It determines that the light beams go through the split in M2 device will not affect photo leakage current. The electron-hole pairs produced by light cannot separate and diffuse to Drain no matter the capacity of drain voltage. The electron and hole will combine in recombination center, Shown as Fig.3.2.20.

Fig.3.2.21 shows the I_D-V_G relationship of M3 device and Full-Metal-Shielding device with the drain voltage is 0.1V. Measuring in darkness environment, the photo leakage current of M3 device and Full-Metal-Shielding device are the same. Fig.3.2.22 shows the I_D-V_G

relationship under darkness and the drain voltage is 9V. Fig.3.2.23 shows the I_D-V_G relationship under 5620nits brightness and the drain voltage is 0.1V. The photo leakage current of M3 still keep the same with Full-Metal-Shielding device. It is particularly when measures under 5620nits brightness and the drain voltage is 9V, shown as Fig.3.2.24. The photo leakage current of M3 device increases slightly and large than Full-Metal-Shielding device. It determines that the light beams go through the split in M3 device will affect photo leakage current slightly. Fig.3.2.25 shows the photo leakage current model of M3 TFT. When the drain voltage is 0.1V, the electron-hole pairs produced by light cannot separate and diffuse to Drain. The electron and hole will combine in recombination center. But when the drain voltage is 9V, the electron field in active layer is strong. The high drain voltage will also induce the floating potential, V_M, in the Metal layer. The V_M will induce the back channel in the bottom of Poly-Si layer. The electron-hole pairs produced by light cannot separate and drift to Drain.

Fig.3.2.26 shows the I_D-V_G relationship of M4 device and Full-Metal-Shielding device with the drain voltage is 0.1V. Measuring in darkness environment, the photo leakage current of M4 device and Full-Metal-Shielding device are the same. Fig.3.2.27 shows the I_D-V_G relationship under darkness and the drain voltage is 9V. Fig.3.2.28 shows the I_D-V_G relationships under 5620nits brightness and the drain voltage is 0.1V. The photo leakage current of M4 still keep the same with Full-Metal-Shielding device. It is particularly different when measures under 5620nits brightness and the drain voltage is 9V, shown as Fig.3.2.29. The photo leakage current of M4 device is large than Full-Metal-Shielding device. It determines that the light beam go through the split in M4 device will affect photo leakage current. Fig.3.2.30 shows the photo leakage current model of M3 TFT. When the drain voltage is 0.1V, the electron-hole pairs produced by light cannot separate and diffuse to Drain. The electron and hole will combine in recombination center. But when the drain voltage is 9V, the electron field in active layer is strong. The high drain voltage will induce the floating potential, V_M, in the Metal layer. The V_M will induce the back channel in the bottom of Poly-Si layer. The electron-hole pairs produced by light cannot separate and drift to Drain.

Fig.3.2.31 shows the I_D-V_G relationship of M5 device and Full-Metal-Shielding device with the drain voltage is 0.1V. Measuring in darkness environment, the photo leakage current of M5 device and Full-Metal-Shielding device are the same. Fig.3.2.32 shows the I_D-V_G relationship under darkness and the drain voltage is 9V. The photo leakage current of M5 still keep the same with Full-Metal-Shielding device. It is particularly different when measures under 5620nits brightness and the drain voltage is 0.1V or 9V, shown as Fig.3.2.33-3.2.34. The photo leakage current of M5 device is large than Full-Metal-Shielding device. It determines that the light beam go through the split in M5 device will affect photo leakage current, Show as Fig.3.2.35. Compare to M4 device, M5 device has large photo leakage current under brightness when the drain voltage is 0.1V. It is because the split of M5 device located in the edge of Drain, the electron-hole pairs produced by light can separate and diffuse to Drain. But the split of M4 has a distance to Drain, the electron will combine with holes in recombination center during it diffuse to Drain.

Fig.3.2.36 reveals the comparison of I_{PLC} which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 0.1V for TFT, the vertical axis is the normalization of drain current, and the horizontal axis is illumination of light source under the device. The M5 devices have the highest of photo leakage current, and the M4, M3, M2, and M1 devices are lower. It indicates that the location of split will influence photo leakage current. The semiconductor layer absorbs light to produce electron-hole pairs. If the distance from split to Drain was short, the electron-hole pairs will separate. Then the electrons arrive to Drain, inducing photo leakage current. However, if the distance from split to Drain is long, the electron-hole pairs will not separate and arrive to Drain. The electron-hole pairs will be combined during the electrons diffuse to Drain.

Fig.3.2.37 reveals the comparison of I_{PLC} which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 9V for TFT, the vertical axis is the normalization of drain current, and the horizontal axis is illumination of back light source. When the drain voltage enhance to 9V, the distribution of the curves are different. The M5, M4, and M3 devices are the higher of photo leakage current, the M2, and M1 devices are lower. It indicates that the location of split will influence photo leakage current. Enhancing the drain voltage will change the distribution of curves. When drain voltage increased to 9V, the limit diffusion distance from split to Drain is increased. Therefore, the M4 and M3 devices have larger photo leakage current. But the electron-hole pairs of M1 and M2 devices still cannot separate and arrive to Drain, so the leakage current of M1 and M2 are similar, and smaller than others.

3.3 Partial Metal Shielding TFT

The partial metal shielding layer is located in channel (Channel-shielding TFT) and junction region of channel (Drain-shielding TFT and Source-shielding TFT) as shown in Fig.3.3.1-3.3.3, respectively. As the shielding metal is located in the channel and shorter than the gate metal shown in Fig.3.3.1, the space between the edge of shielding metal and the gate metal is set to 3μm. Fig.3.3.2-3.3.3 plots the Poly-Si TFT with shielding metal remained to be located in junction side. Similarly, the overlap region between the edge of shielding metal and the gate metal is 3μm. Therefore, the effect of location for I_{PLC} is investigated employing the two types of Poly-Si TFT with different partial metal shielding structure.

Fig.3.3.4-3.3.6 plots the I_D-V_G relationships of poly-Si TFT with partial metal shielding layer located in channel region (Channel-shielding TFT) and drain junction region (Drain-shielding TFT) and source junction region (Source-shielding TFT) as drain voltage is varied at dark state. It is clearly that the V_{TH} of poly-Si TFT with partial metal shielding layer is independent of drain bias and the location of shielding metal.

Then, we measure with a light source under the device, controlling input current to decide illumination. The condition of illumination is 2160nits. Fig.3.3.7 plots the I_D-V_G relationships of Poly-Si TFT with different kind of metal shielding layer. The drain voltage is 0.1V, and the illumination is 2160 nits. The Drain-shielding TFT reduces photo leakage current as well as Full-shielding TFT. The capacity of the off current is about 10^{-12}~10^{-11}A. The Source-shielding TFT and the Channel-shielding TFT have larger photo leakage current, the capacity is about 10^{-11}A.

We increase the drain voltage but keep the same illumination. Shown as Fig.3.3.8, the drain voltage is 5V. It is clearly that only Full-shielding TFT has smaller photo leakage current, the Drain-shielding TFT cannot keep the same capacity of photo leakage current with Full-shielding TFT. Shown as Fig.3.3.9-3.3.10, the drain voltage is 9V and 15V. The photo leakage current of Drain-shielding TFT increases as Source-shielding TFT and the Channel-shielding.

Fig.3.3.11 reveals the comparison of I_{PLC} which is extracted at a voltage $|V_G$-$V_{TH}|$ of 7V as V_D is 0.1V for TFT with Full-shielding TFT and partial metal shielding layer located in channel region (Channel-shielding TFT), drain side (Drain-shielding TFT) and source side (Source-shielding TFT) as brightness of back-light is in Channel creased (2160, 3100, 4110,and 5620nits). The I_{PLC} of Full-shielding TFT and Drain-shielding TFT are much lower than that of Channel-shielding TFT and Source-shielding TFT. The maximum values of I_{PLC} of Full-shielding TFT, Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT are 4pA, 4.1pA, 19.2pA and 24.5pA. In addition, the I_{PLC} of Full-shielding TFT and Drain-shielding TFT exhibit a weak dependence on the increasing brightness of back-light. The result confirms that drain side is the dominant region for I_{PLC} of Poly-Si TFT operated in linear region. Fig.3.3.12 shows the I_{PLC} of Full-shielding TFT, Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT as drain voltage is 9V. It is observed the shielding effect of Full-shielding TFT is reduced markedly. The Drain-shielding TFT cannot keep the same I_{PLC} with Full-shielding TFT, but it is still less than that of Channel-shielding TFT and Source-shielding TFT.

While Poly-Si TFT is exposure to back-light, the excess electron-hole pairs are generated. The regions generating photo-induced electron-hole pairs can be divided into two parts. One is drain junction region, and the other is channel region. The excess electron-hole pairs, generated in drain junction, would be separated due to the electric field and the excess electrons could flow to drain to become leakage current. By contrast, since Si is an indirect band-gap material, photo-induced electron-hole pairs in channel region could not be recombined directly. Therefore, the excess electrons in channel region would diffuse to drain to form current. It is inferred that the I_{PLC} is attributed to the diffusion current and drift current from channel region and drain junction, respectively. As shown in Fig.3.3.13, the band diagram to explain the generation of I_{PLC} for Source-shielding TFT is proposed. Since the shielding metal is located in source side, the excess electrons generated at channel and junction region flow to drain by diffusion and drift, leading to the I_{PLC}. Fig3.3.14 shows the band diagram of Drain-shielding TFT under illumination. As the shielding metal is located in drain side, light emitting to the junction region is blocked to eliminate the junction part of I_{PLC}. In addition, the electrons induced by light outside the shielding metal are difficult to diffuse to drain since the excess electrons must to pass through an intrinsic Poly-Si region, while drain voltage is 0.1V, as shown in Fig3.3.15. Hence, Drain-shielding TFT operated in linear region exhibits a highest immunity to illumination environment compared to Source-shielding TFT and Channel-shielding TFT. However, as the high voltage is applied at drain, a positive potential distribution, V_M, in the shielding metal of Drain-shielding TFT owing to the coupling effect is generated due to the parasitic capacitance in the overlap of drain and shielding metal. Hence, electrons induced by V_M gather to form the back channel near drain in the bottom of Poly-Si layer, as illustrated in Fig3.3.16. So that excess electrons at channel region would flow to drain through the back channel under high drain bias, generating I_{PLC}.

Therefore, the shielding effect of Drain-shielding TFT under illumination would be suppressed by applied high drain voltage.

3.4 Electrical Characteristics of Poly-Si TFT under Illumination

In this chapter, I_{PLC} and S.S behavior of Poly-Si TFT with specific process steps under illumination is discussed. In order to clarify the factors of affecting the sub-threshold properties of Poly-Si TFT under illumination, a patterned metal shielding layer is used to investigate the electrical characteristics of Poly-Si TFTs under light exposure. By patterned metal shielding structure, the exposure region is controlled to be located in the drain or source junction. Based on the analysis of measurement results, the key factors effectively influent the photo leakage and the sub-threshold swing are observed clearly in this work.

Fig.3.4.1 shows the poly-Si TFT with split metal shielding layer, the split located near the drain junction. Fig.3.4.2 shows the I_D-V_G characteristics of shielding TFT with low drain bias measured in forward and reverse modes at dark. The exposure region is located close to the drain and source junction for forward and reverse measurement, respectively. The two curves are almost identical and V_{TH} of TFT in forward mode (Forward TFT) is as same as that of TFT in reverse mode (Reverse TFT). However, the V_{TH} of Reverse TFT is slightly less than that of Forward TFT while drain voltage is 9V, as shown in Fig.3.4.3. Since the shielding layer for Forward TFT has a gap in drain junction, the potential distribution coupling from drain voltage would not extend into channel region. Therefore, V_{TH} of Forward TFT is independent of applied drain bias. By contrast, the shielding metal of Reverse TFT is distributed over most of channel region from drain. It is indicates that the potential distribution induced by high drain voltage, V_M, in the metal film of Reverse TFT would affect the V_{TH}. In addition, the S.S of Forward TFT and Reverse TFT is unchanged by drain voltage at dark.

Fig.3.4.4 plots transfer curves of Forward TFT operated in linear region at the dark and photo states. As the gate bias is -12V, the leakage current of Forward TFTs is about 10^{-14}~10^{-13}A at dark but is significantly increased under illumination. The I_{PLC} is 2.5x10^{-11}A, approximately three orders of magnitude greater than the dark leakage current. In addition, the S.S is slightly raised under illumination. The S.S under dark and photo states is 0.36 V/decade and 0.41 V/decade, respectively. As the drain bias is 9V, the I_D-V_G relationships of Forward TFT at dark and photo states are illustrated in Fig.3.4.5. Similarly, a markedly high I_{PLC} and the nearly unaltered S.S of Forward TFT under illumination are observed clearly. Since the width of depletion region at drain would be increased with high drain bias, the more electron-hole pairs induced by light would be separated in the depletion region. Therefore, in forward mode, the I_{PLC} at high drain voltage is higher than that under low drain voltage.

The I_D-V_G characteristics of Reverse TFT are also investigated in this work, as shown in Figs.3.4.6-3.4.7, respectively. As V_D is 0.1V, the I_{PLC} of Reverse TFT is 2.7x10^{-12}A, as low as one order of magnitude, compared to that in Forward TFT under same drain voltage. Furthermore, the S.S under illumination in Fig.3.4.6 is almost unchanged. The increase ratio of S.S in Reverse TFT is about 12.96% as drain bias is 0.1V. Fig.3.4.7 indicates that the S.S of Reverse TFT with high drain voltage, however, is substantially degraded under illumination. It is increased 54.08% of the magnitude of that at dark state. The detail results of the variation of S.S are listed in Table.2. With high drain bias, the I_{PLC} is also increased in Reverse TFT but still lower than that in Forward TFT. From the comparison in Forward TFT and Reverse TFT with high and low drain bias, it is inferred the significant increase of S.S in the Reverse TFT would be attributed to that the exposure region is located in source junction and the device is operated with high drain voltage.

For Forward TFT, the exposure region is located at the drain junction so that plenty of electron-hole pairs originated from light would be easily separated due to the electrical field at junction. Therefore, excess electrons could flow directly to the drain, leading to the I_{PLC}, as shown in Fig.3.4.8. By contrast, the exposure region of Reverse TFT is close to source side. As the drain bias is low, numerous electron-hole pairs generated in source junction is difficult to be separated by lateral electrical field. Therefore, the excess electrons flowing to drain is fewer to cause the lower I_{PLC}. However, as the drain voltage is high, a positive potential distribution, V_M, in the metal film owing to the coupling effect is generated from the parasitic capacitance in the overlap of drain and metal shielding layer [32]. Hence, electrons induced by V_M gather to form the back channel in the bottom of Poly-Si layer, as illustrated in Fig.3.4.9. So that excess electrons at source junction would flow to drain through the back channel and excess holes is residual to be accumulated in the source junction to form the floating body which offers a positive potential. It can be inferred that the degraded S.S in Poly-Si TFTs under illumination is mainly caused by the floating body with positive potential near the source side. The key factors to affect I_{PLC} and the S.S under illumination are clarified clearly using the patterned metal shielding layer in Poly-Si TFTs.

When the gate bias is below the threshold and the semiconductor surface is in weak inversion or depletion, the corresponding drain current is the sub-threshold current.[] In weak inversion and depletion, the electron charge is small, the drain current is dominated the diffused electron from source in n-type Poly-Si TFT. Therefore, it would be affected strongly by the barrier height of source. As the gate bias is applied, the barrier height of source is lowered to increase the amount of electron in channel diffused from source. Therefore, it is clearly observed that the S.S current is dependent of the applied gate voltage. The sub-threshold current in poly-Si TFT is empirically expressed [33]:

$$\mathbf{I_{sub} = I_{sub0} \exp\left[\frac{q(V_G - V_{G0})}{nk_B T}\right]}$$

For simplity and giving more clear physics picture, it is also can be expressed as following equation [34]:

$$\mathbf{I_{sub}} \propto \mathbf{exp}(\boldsymbol{\beta\varphi_s})$$

It indicates that, the drain current varies exponetntially with $\boldsymbol{\varphi_s}$ in the subthreshold region, where $\boldsymbol{\varphi_s}$ is the suface potential.

Based on the experimental results of treated TFT and shielding TFT, a model of band diagram to explain the S.S degradation of Poly-Si TFT is proposed, as shown in Fig.3.4.10. First, as the excess electron-hole pairs are generated under illumination with positive drain voltage, the light-induced electrons flow to drain directly, forming the photo leakage current. Therefore, the residual excess holes are accumulated in the Poly-Si film to form the floating body with a positive channel potential, ΔV. Hence, the source barrier is lowered by ΔV due to the floating positive potential distributed in the channel. While the applied gate bias is swept from negative to positive directions and smaller than the threshold voltage, TFT would be operated at sub-threshold region. So the source barrier would be lower again by the positive gate bias. However, the more lowering source barrier induce that the excess holes accumulated in channel are more easily diffuse to the source to reduce the positive channel potential. So that the fewer channel potential leads to a raise of source barrier. It means that the source barrier is not only controlled by applied gate bias but also affected by the floating body with positive potential, ΔV when Poly-Si TFTs are under illumination. In our method of treated TFT, the trap states on the top face of buffer layer can effectively recombine the excess electron-hole pairs induced by back light. So that amount of accumulated holes is also reduced effectively to suppress the effect of floating body. Hence, the improvement of sub-threshold swing is clearly observed in this work. In addition, the results of shielding TFT confirm that the effective region affecting by floating positive potential is the source junction.

Chapter 4 Bias Stress of Poly-Si TFT under Illumination

4.1 DC Stress under illumination

Fig.4.1.1 shows the Poly-Si TFTs with lightly doped drain (LDD) structure. We stressed the poly-Si TFT as V_G=5V and V_D=20V are applied. During the stress time of 1000sec, we measured the I_D-V_G in 1, 10, 100, and 1000sec, comparing the device behavior which was stressed in light and dark. Fig.4.1.2 shows the I_D-V_G of TFTs in linear region in dark. It could be observed that the on current decrease 74% after 1000sec dark stress. The decrease of the off current means the decrease of the mobility which owing to the tail states increase. The V_{TH} and S.S do not change after 1000sec stress, so the deep state does not increase. Fig.4.1.3 shows the I_D-V_G of TFTs in linear region in darkness. The on current decreases 60% after 1000sec light stress. Fig.4.1.4 shows the on current variation in dark stress and light stress. We could observe that the on current decrease less as we measured the TFT under light stress than under dark stress.

Fig.4.1.5 shows our proposed model. In the dark, as high drain voltage and small gate voltage are applied, impact ionization is occurred in the junction between channel and drain due to the high electric field. The damage in the junction is remarkable when the high electric field is applied. Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film. As the electron-hole pairs are generated, the electric field in the junction of channel and drain decrease. So the on current decreases less when we measured the TFT under light stress than under dark stress.

In order to verify the model, we employed a Poly-Si TFT with lateral body thermal (LBT) as shown in Fig.4.1.6. The lateral body thermal is near the Drain thermal as the drain voltage is applied on the n+ region which near p+ region. The p+ region could sense hole current which generated by impact ionization under high electric field of drain. The device behavior of LBT TFT is almost the same as conventional TFT.

From Fig.4.1.7, we measured the dependence of the body current (I_{body}) and on the gate voltage (V_G) of LBT poly-Si TFTs with the increasing brightness of back-light (2160, 3100, 4110, 5620 nit). As the brightness increases cause the electric field decreases, the holes which inject into p+ region decreases, so the body current decreases. It clarified that the electric field in the junction between channel and drain decrease when the device exposure to light.

4.2 AC Stress under illumination

Under AC stress, a pulse voltage is applied to the gate electrode, source and drain is grounded, as shown in Fig.4.2.1. Fig.4.2.2 shows the waveform of the AC signal. The basic parameters of AC signal consist of frequency (Freq.), signal high level (V_{G_high}), signal low level (V_{G_low}), high-level time (T_{high}), low-level time (T_{low}), rising time (T_r), and falling time (T_f). T_r (rising time) is the time that voltage signal rises from V_{G_high} to V_{G_low}, while T_f (falling time) is the time that voltage signal falls from V_{G_high} to V_{G_low}. The total stress time is the summation of T_{high} under the stress condition. The AC stress condition in the experiment is the gate voltage swing form V_{TH} − 15V to V_{TH}+15V, frequency of 500kHz, T_{high} and T_{low} of both 1us, T_r and T_f of both 100ns, and the total stressing time of 2000sec.

During the stress time of 2000sec, we measured the I_D-V_G in 0, 1, 10, 100, 1000, and 2000sec, comparing the device behavior which was stressed in the light and dark. Fig.4.2.3 shows the I_D-V_G of TFTs in linear region in the dark. It could be observed that the on current decreases 66.3% after 2000sec stress under darkness. Fig.4.2.4 shows the I_D-V_G of TFTs in linear region under darkness. The on current decreases 74.1% after 2000sec stress under illumination. The ON-Current decrease less when we measured the TFT under darkness stress than illumination stress.

Fig.4.2.5-4.2.7 shows a schematic diagram for degradation model of the poly-Si TFTs under dynamic operation. When a high voltage is applied to the gate, the device turns on and operates in ON state. The electrons gather to form a channel, as shown in Fig.4.2.5. When the gate voltage drops, the electrons in the channel move rapidly to the source and drain shown in Fig.4.2.6. Some of the trapped electrons are exposed to the high electric field and grain energy from the field. Hot electrons are generated at this moment and form electron traps shown in Fig.4.2.7, and a density of state (DOS) in tail edge of poly-Si is increased by the hot electrons. The impact ionization is dependent with current density and electric field.

Fig.4.2.8 shows the comparison of dark Stress and illumination stress. The carrier density is larger in illumination stress than dark stress, because light will induce electron-hole pairs. But the junction electric field is smaller in illumination stress than dark stress. In the experiment, we suggest that the key factor is current density. So the degradation is quite obvious when stress under illumination.

4.3 AC Stress of Split Shielding TFT under illumination

In this section, we changed device in the AC stress experiment. Fig.4.3.1 shows the top gate poly-Si TFT with a split metal shielding layer. The split located near Drain junction. When the device exposure in illumination, the shielding layer will block the light beams.

Fig.4.2.2 shows the waveform of the AC signal. The AC stress condition is the same with previous experiment. The gate voltage swing form V_{TH} − 15V to V_{TH}+15V, frequency of 500kHz, T_{high} and T_{low} of both 1us, T_r and T_f of both 100ns, and the total stressing time of 2000sec.

During stress time of 2000sec, we measured the I_D-V_G in 0, and 2000sec, comparing the device behavior which was stressed in the light and dark. Fig.4.3.2 shows the I_D-V_G of TFTs in linear region in dark. It could be observed that the on current decreases 25% after 2000sec stress under darkness. Fig.4.3.3 shows the I_D-V_G of TFTs in linear region under darkness. The on current decreases 21.7% after 2000sec stress under illumination. The ON-Current decrease less when we measured the TFT under illumination stress than darkness stress.

The impact ionization is dependent with current density and electric field. Fig.4.3.4 shows the comparison of illumination stress and dark stress. In this experiment, most of light beams are blocked by metal shielding layer. So the photo-induced electron-hole pairs are less than previous experiment. But there is a split in the shielding layer near the drain junction. The junction electric field decrease when the AC stress measurement under illumination. As a result, we suggest that the key factor is the electric field of drain junction. So the degradation is quite obvious when stress under darkness.

Chapter 5 Conclusion

We have demonstrated a top gate Poly-Si TFT with the light-shielding structure first. The proposed Full-Metal-Shielding TFT is free of photo leakage current under illumination for high image quality AMLCD application.

And then, we proposed the TFTs with split metal shielding layer to indicate the split location is the key factor to induce photo leakage current. So we can suggest that the critical region to induce photo leakage current of poly-Si TFT under illumination. Besides, it dependent of increasing drain bias. In the experiment, the critical region is very short and located in drain junction with low drain bias. The enhancement of the drain bias will extend the critical region. The photo leakage current will increase when the light beams go through the split that has a little distance to drain under a high drain bias.

In addition, the threshold voltage shift of the Full-Metal-shielding TFTs and Split -Metal-shielding TFTs rise with the increasing drain bias in dark state, which is explained by the coupling effect. In order to overcome this issue and investigate the generation mechanism of I_{PLC}, Poly-Si TFT with the partial shielding metal located in junction and channel region is fabricated. The V_{TH} of Poly-Si TFT with partial metal shielding layer is independent of increasing drain bias. Furthermore, the Drain-shielding TFT exhibits impressively low I_{PLC}. But the shielding effect of the Source-shielding TFT and Channel-shielding TFT are rather poor. The I_{PLC} of Drain-shielding TFT, Channel-shielding TFT and Source-shielding TFT are 4.1, 19.2 and 24.5 pA as brightness of back-light is 5610 nits. From the comparison of I_{PLC} of Drain-shielding TFT, Source-shielding TFT and Channel-shielding TFT, the band diagram of Poly-Si TFT under illumination is proposed. Unfortunately, the shielding effect of Drain-shielding TFT would be suppressed as the high drain voltage. It is due to back channel effect.

We also study the electrical characteristic of poly-Si TFT with patterned metal shielding layer under illumination. The I_{PLC} and S.S properties of Poly-Si are discussed in detail by two approaches. The Forward TFT exhibits the significantly high I_{PLC} and the slightly modified S.S under illumination. By contrast, the I_{PLC} in Reverse TFT is lower than that in Forward TFT at the same drain bias. The S.S under illumination is almost unchanged in reverse mode at low drain bias. However, a remarkable degradation in S.S is observed in Reverse TFT with high drain bias operation. The increased ratio of sub-threshold swing for this case is 64%. Based on the results and proposed model, the causes of I_{PLC} and degraded S.S in Poly-Si TFTs under illumination are demonstrated in this work.

Finally, we study the degradation mechanism of DC stress and AC stress under illumination. We propose a model of DC stress under illumination first. Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film. As the electron-hole pairs are generated, the electric field in the junction of channel and drain decrease. So the degree of the degradation of light stress is smaller than dark stress.

In AC stress experiment, we employed two kind of poly-Si TFTs to clarify the photo effect of AC stress. One is convention TFT, and the other is a new structure TFT with split metal shielding layer. The result of AC stress experiment with convention TFT is that the degradation is quite obvious when stress under illumination, owing to the high current density. Although it is known that the impact ionization is dependent with current density and electric field, in this experiment, we suggest that the key factor is current density.

There is a different AC stress result when experiment with split metal shielding TFT. The degradation is quite obvious when stress under darkness. Most of light beams are blocked to metal shielding layer, so the current density just raises a little. But the light beams go through the split to drain junction procured junction electric field decrease. In the experiment, we suggest that the key factor is the electric field of drain junction, not current density. So the degradation is quite obvious when stress under darkness.

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Figures

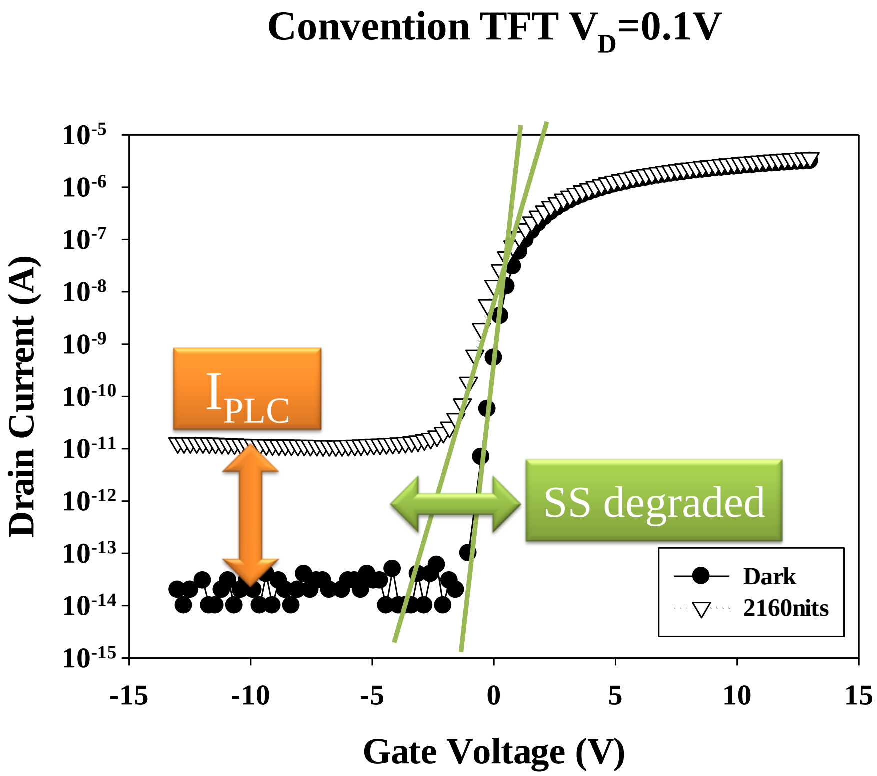


Fig.1.1.1 The I_D-V_G transfer curves of standard Poly-Si TFT.

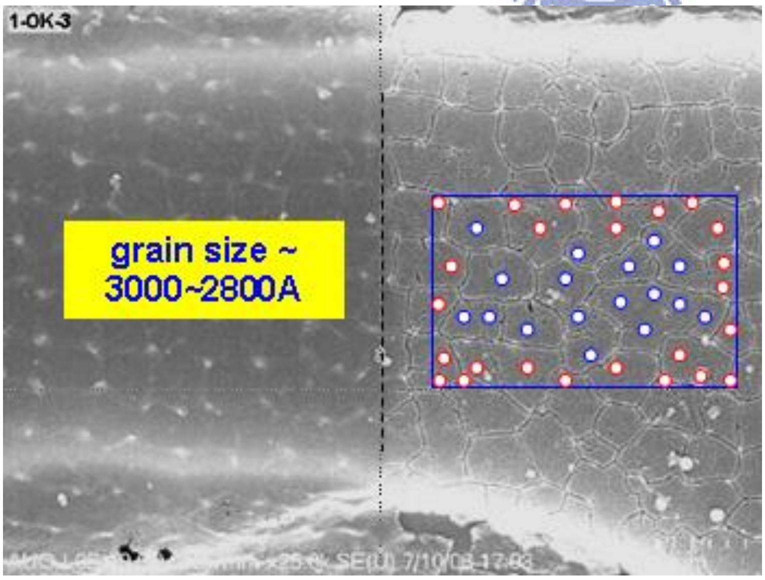
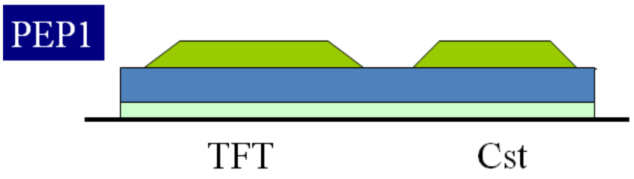
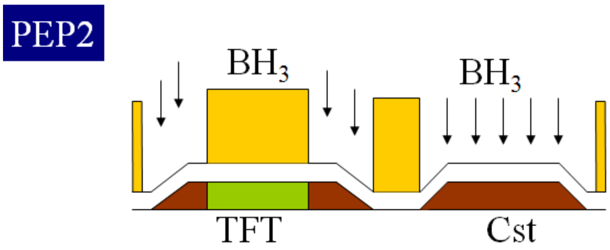


Fig.2.1.1 The average grain size of polycrystalline silicon was found to be 280~300nm.



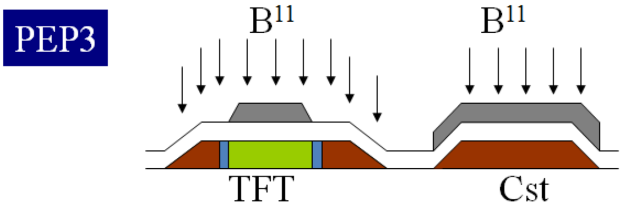
- Buffer layer and aSi deposition
- Poly-Si island formation.
- Channel Doping.

Fig.2.1.1 Pep1 Process Flow of LTPS PMOS TFT.



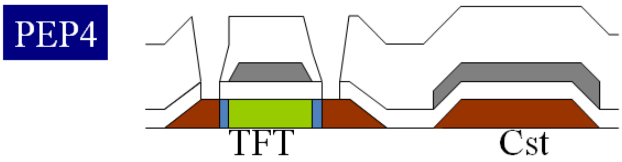
- GI deposition.
- P+ doing by Ion Implant.

Fig.2.1.2 Pep2 Process Flow of LTPS PMOS TFT.



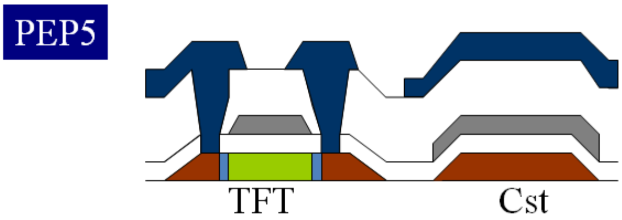
- GE formation.
- P^- self-aligned doped by I/I.

Fig.2.1.3 Pep3 Process Flow of LTPS PMOS TFT.



- ILD Deposition.
- Activation + Hydrogenation.
- Via1 hole opening

Fig.2.1.4 Pep4 Process Flow of LTPS PMOS TFT.



- S/D Formation.

Fig.2.1.5 Process Flow of LTPS PMOS TFT.

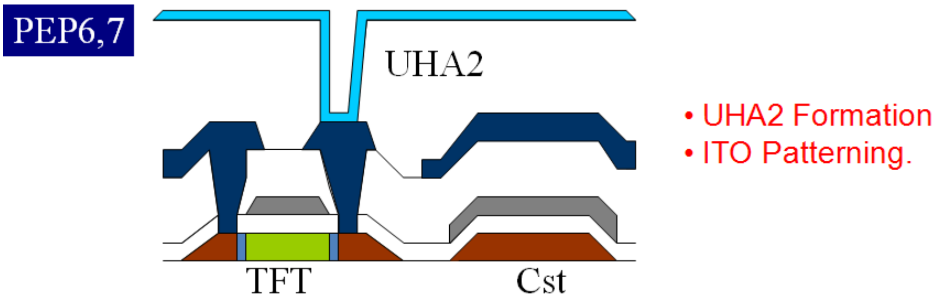


Fig.2.1.6 Pep6,7 Process Flow of LTPS PMOS TFT.

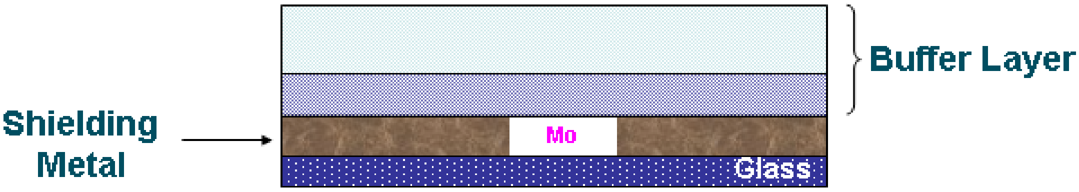


Fig.2.2.1 Structure of shielding metal which was employed Molybdenum.

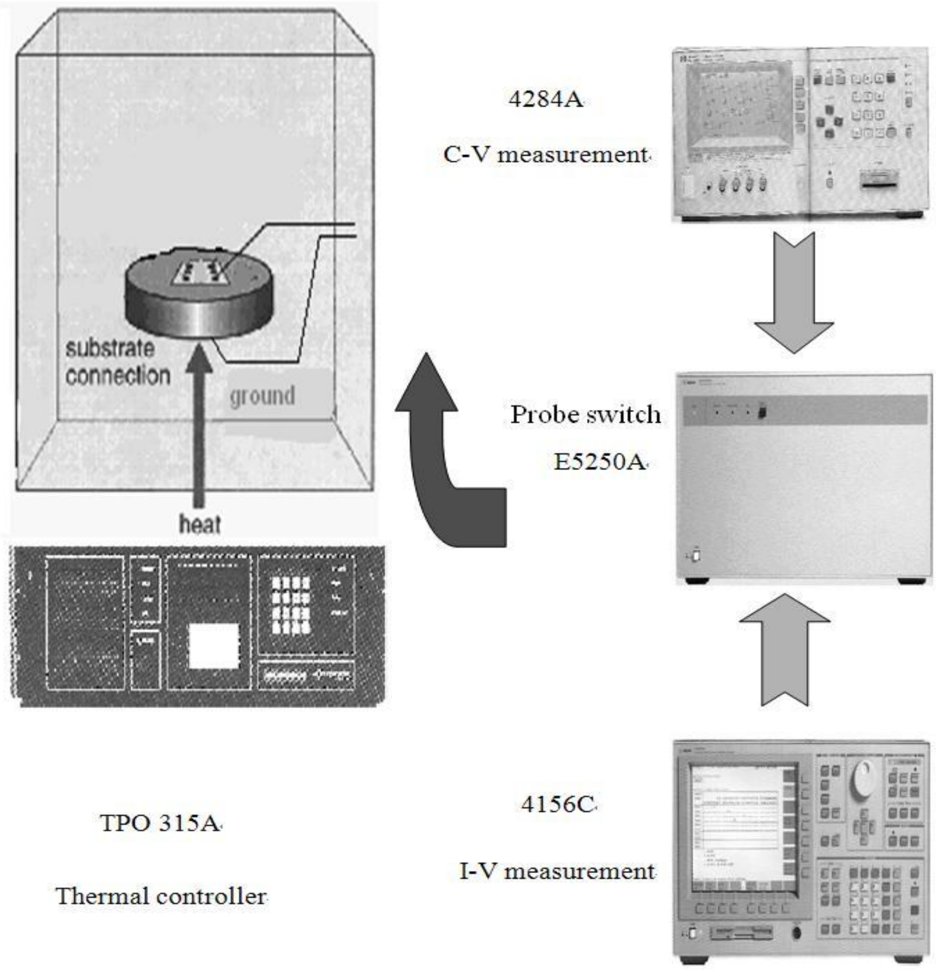


Fig.2.4.1 I-V/C-V instruments set up in the laboratory.

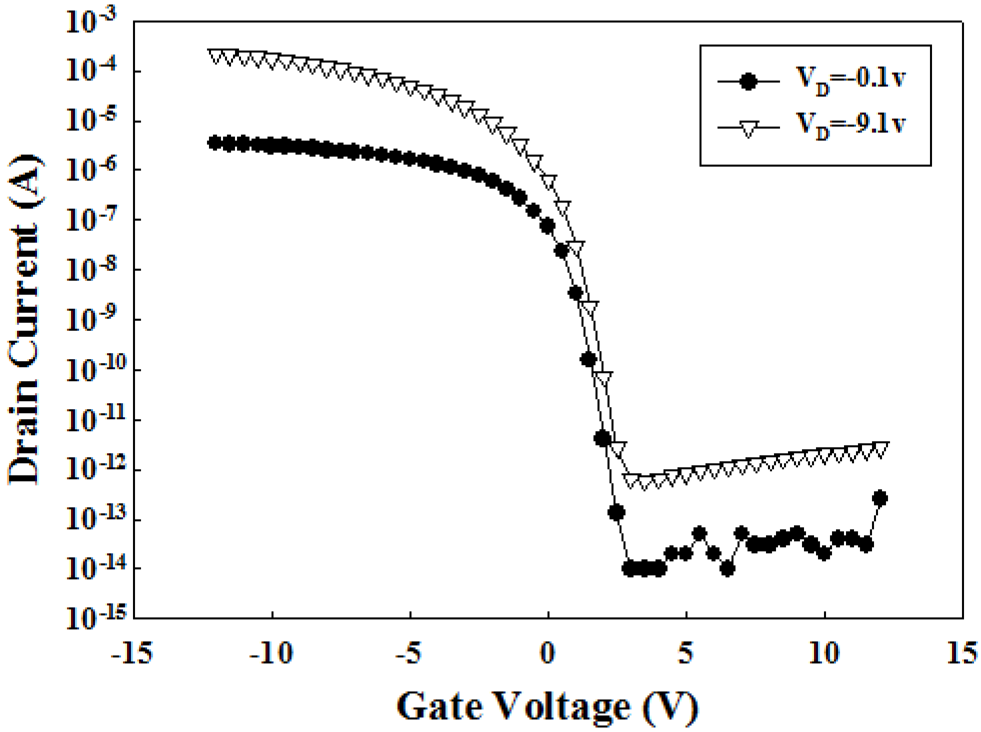


Fig.2.5.1 The typical TFT output characteristics.

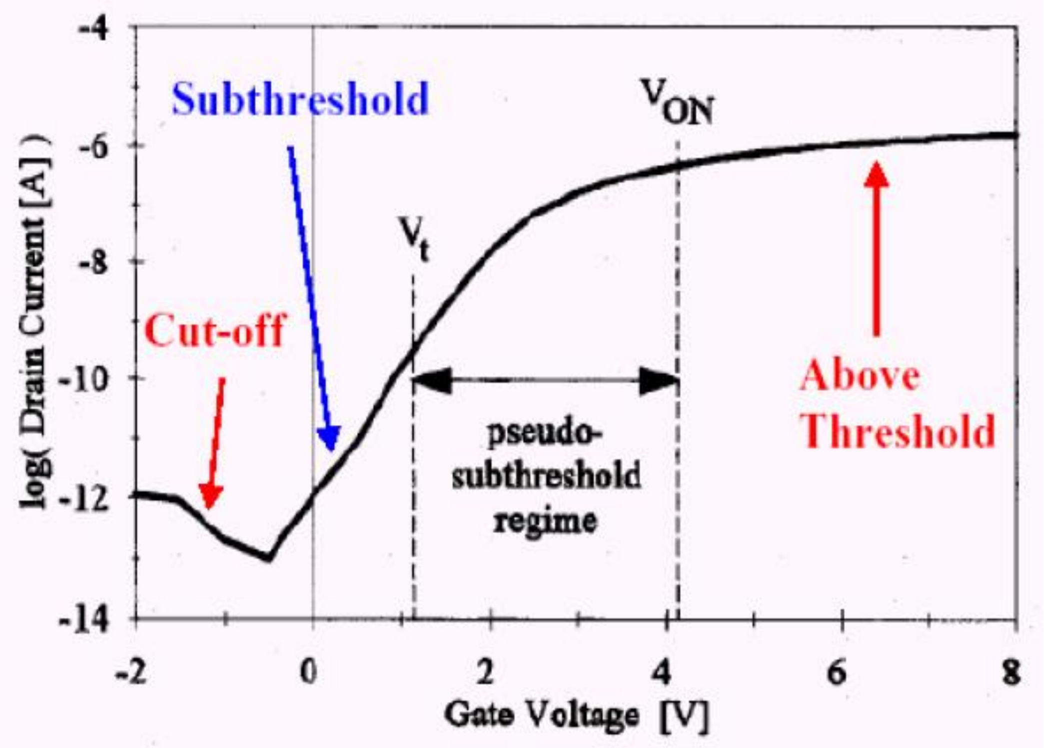


Fig.2.5.2 Poly TFT Transfer Characteristics (I_D-V_G Curve).

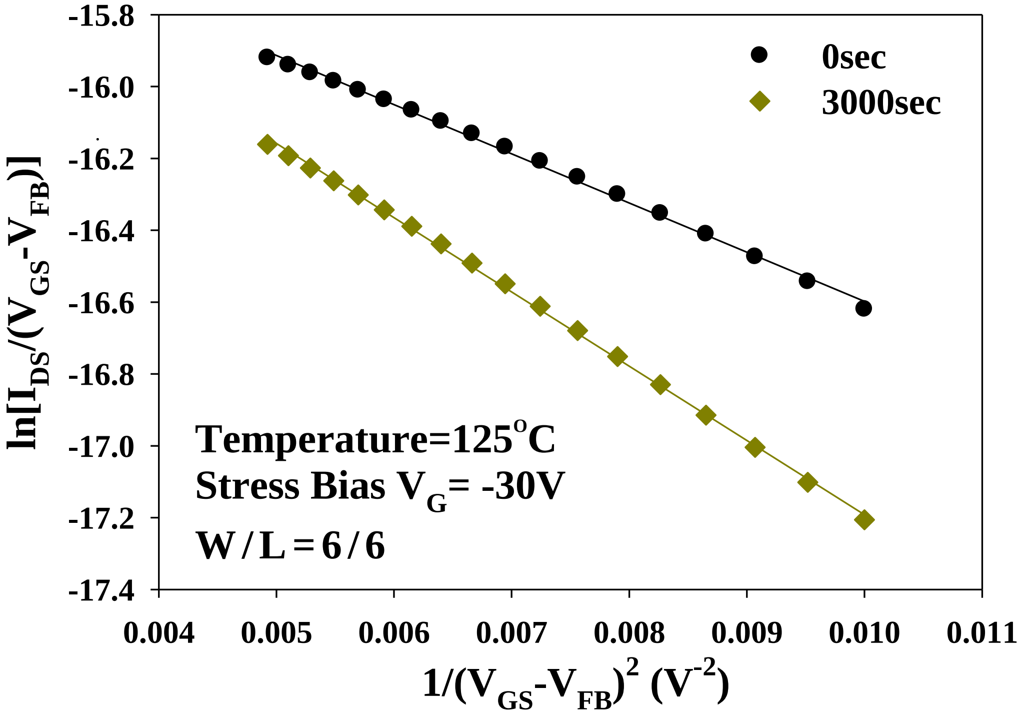


Fig.2.5.3 Plotting of $\ln\left(\frac{I_D}{(V_G-V_{FB})}\right)$ versus $(V_G-V_{FB})^{-2}$.

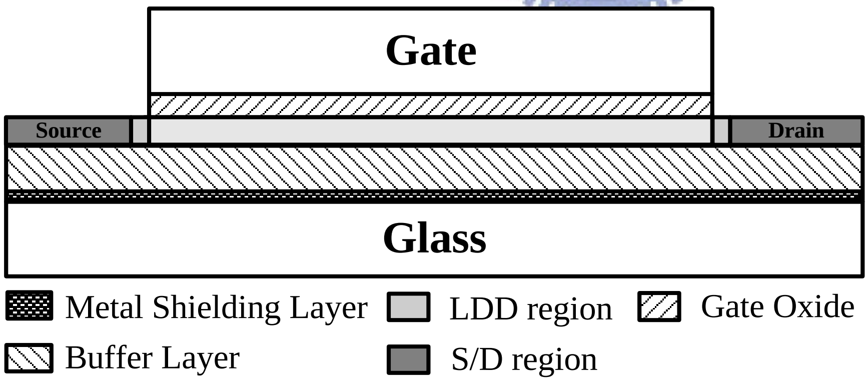


Fig.3.1.1 The cross-sectional view of proposed TFT.

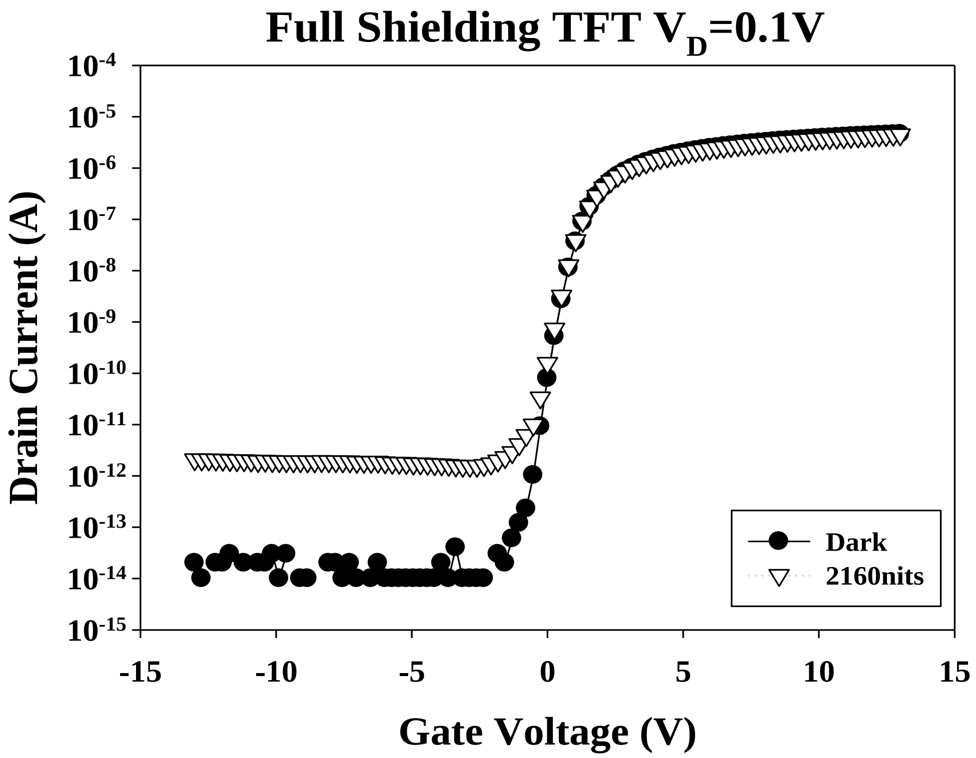


Fig.3.1.2 The I_D-V_G transfer curves of full shielding TFT.

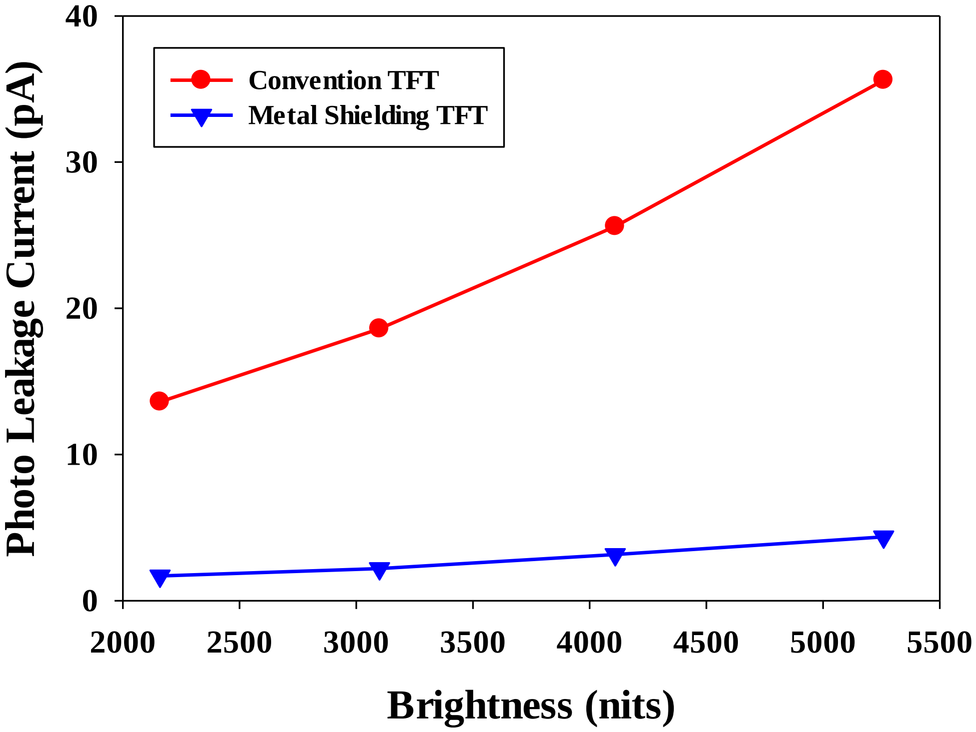


Fig.3.1.3 The photo leakage current of full metal shielding TFT and convention TFT.

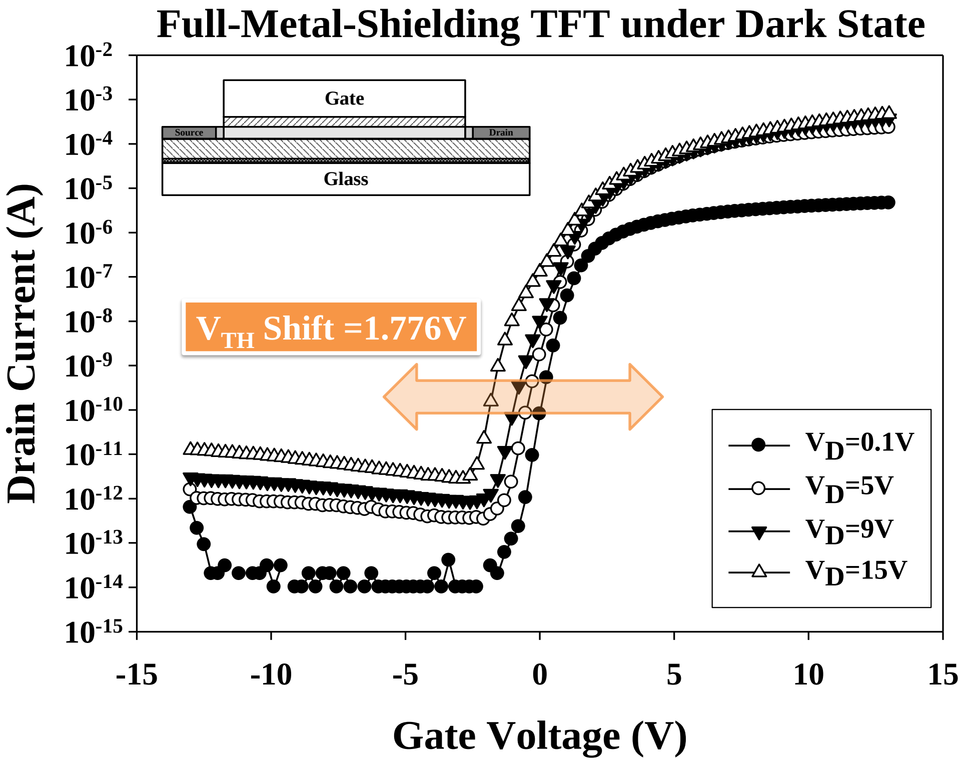


Fig.3.1.4 The I_D-V_G relationships of Full-Metal-Shielding TFT.

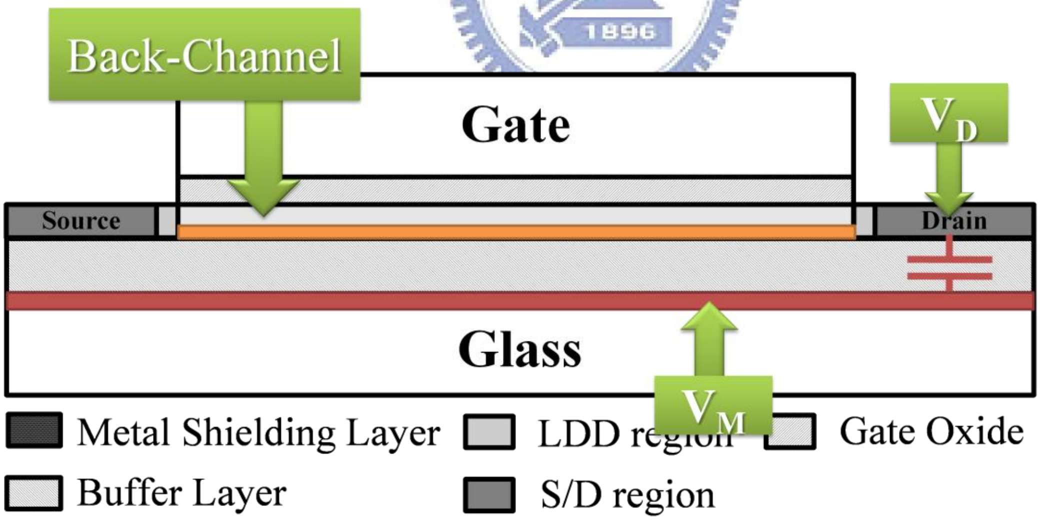


Fig.3.1.5 Back channel effect of full shielding TFT.

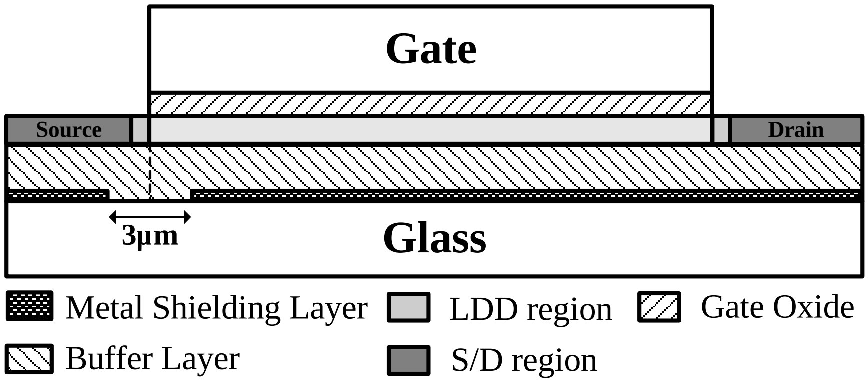


Fig.3.2.1 Poly-Si TFT with split metal shielding layer, M1.

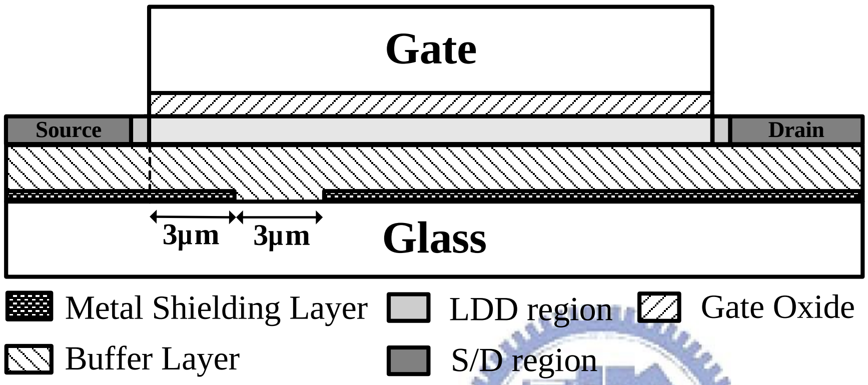


Fig.3.2.2 Poly-Si TFT with split metal shielding layer, M2.

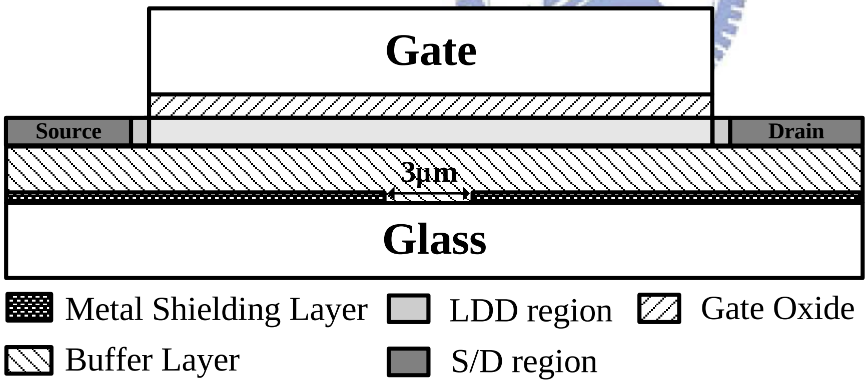


Fig.3.2.3 Poly-Si TFT with split metal shielding layer, M3.

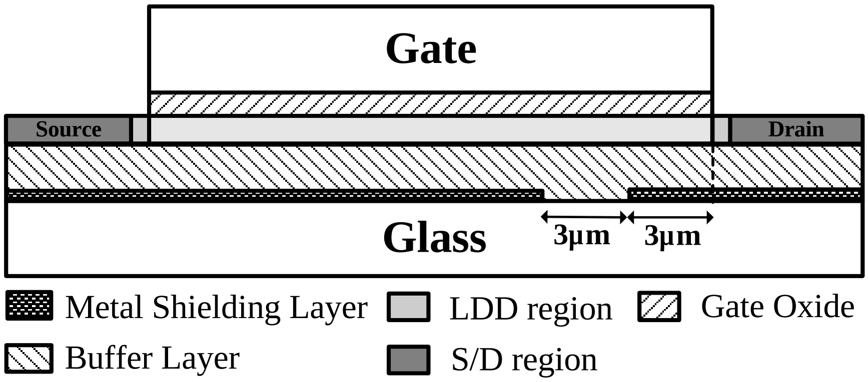


Fig.3.2.4 Poly-Si TFT with split metal shielding layer, M4.

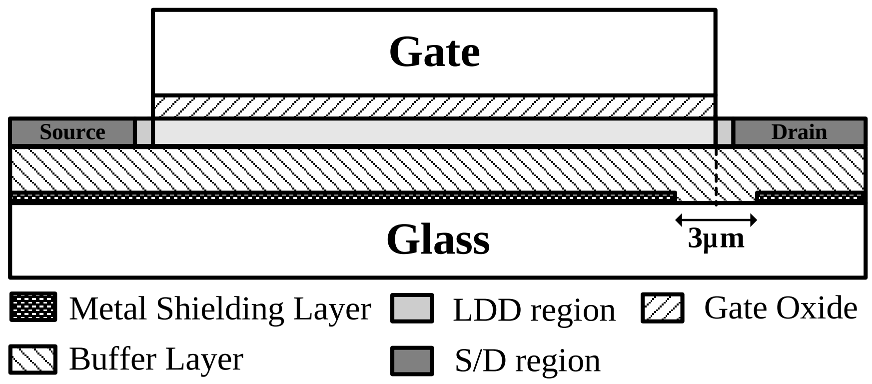


Fig.3.2.5 Poly-Si TFT with split metal shielding layer, M5.

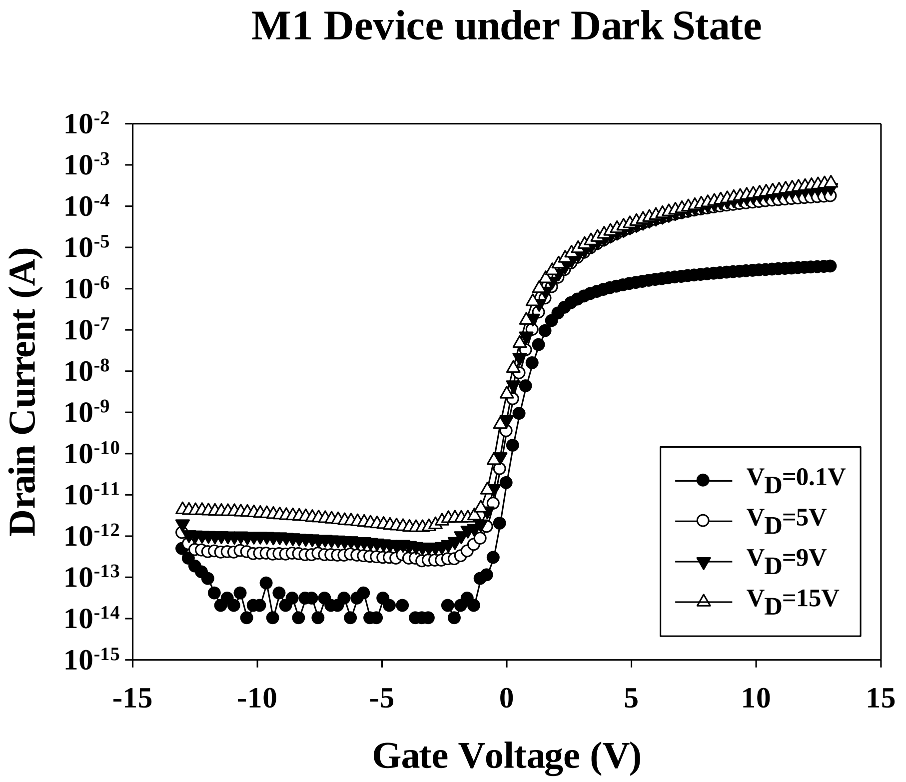


Fig.3.2.6 The I_D-V_G relationships of M1 devices.

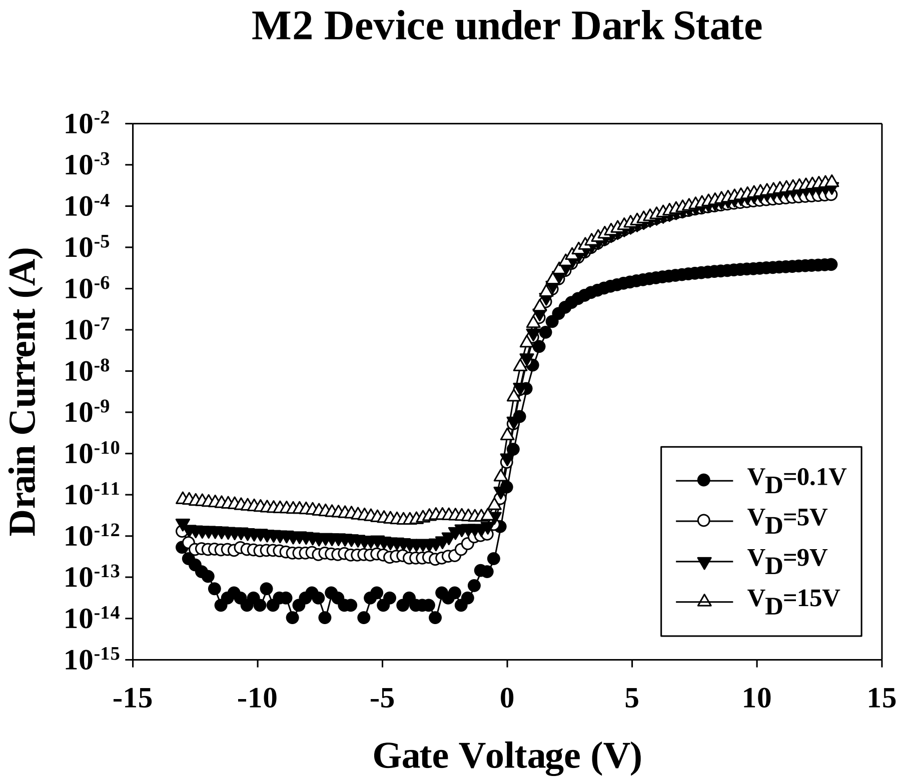


Fig.3.2.7 The I_D-V_G relationships of M2 devices.

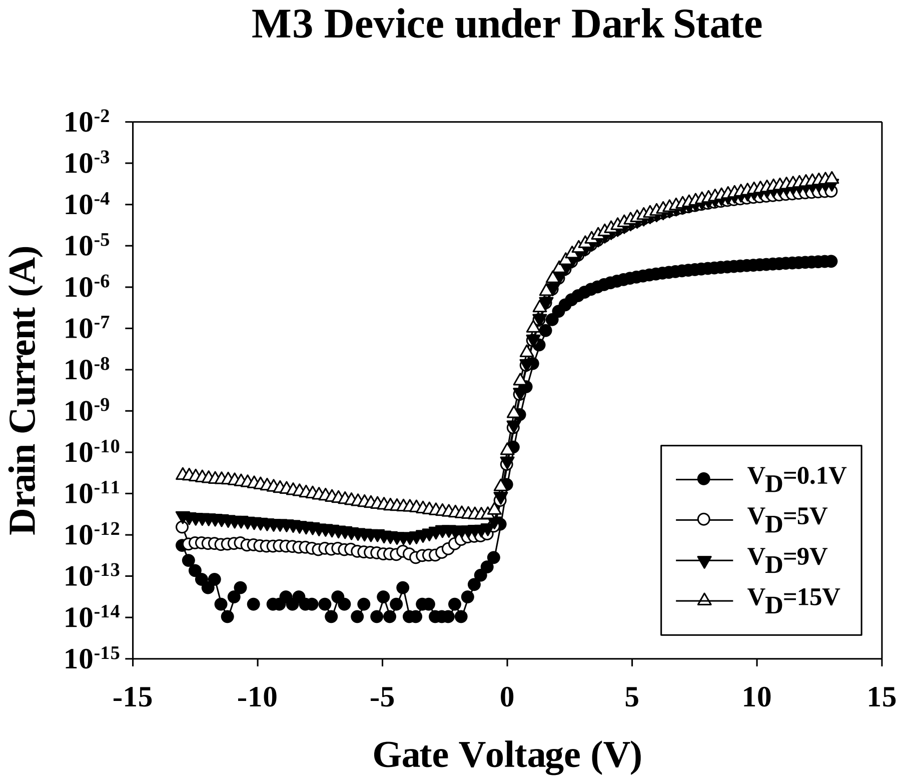


Fig.3.2.8 The I_D-V_G relationships of M3 devices.

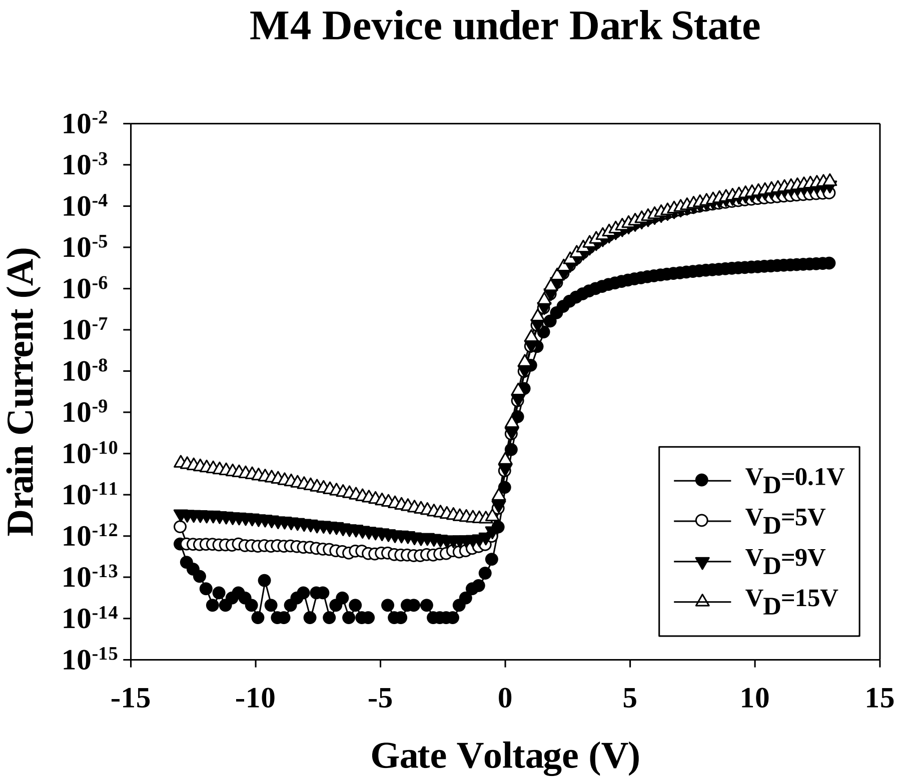


Fig.3.2.9 The I_D-V_G relationships of M4 devices.

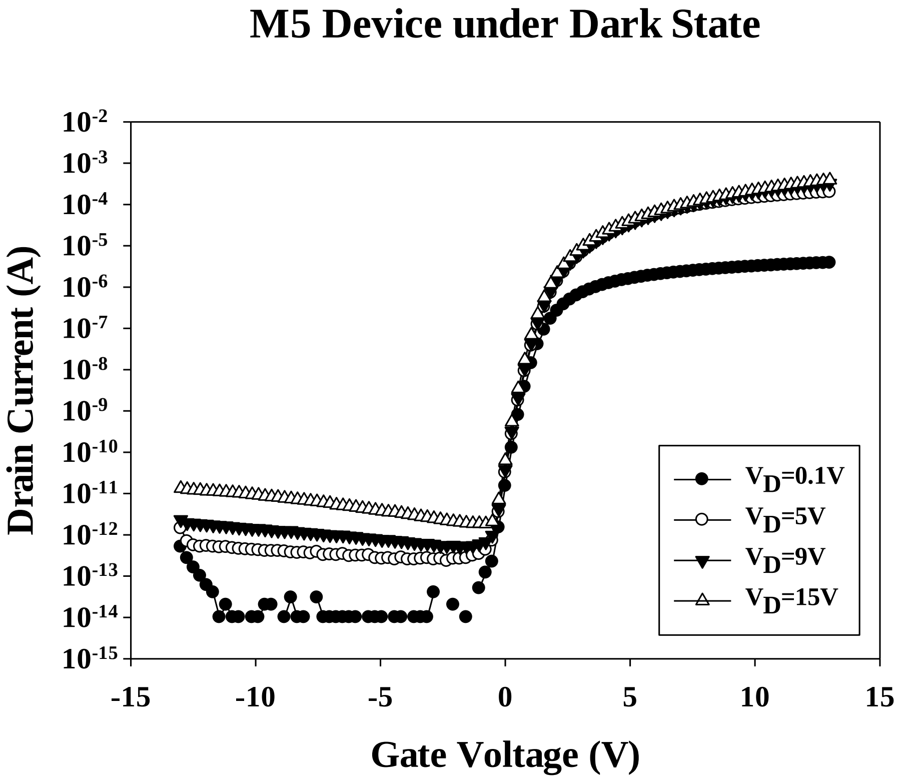


Fig.3.2.10 The I_D-V_G relationships of M5 devices.

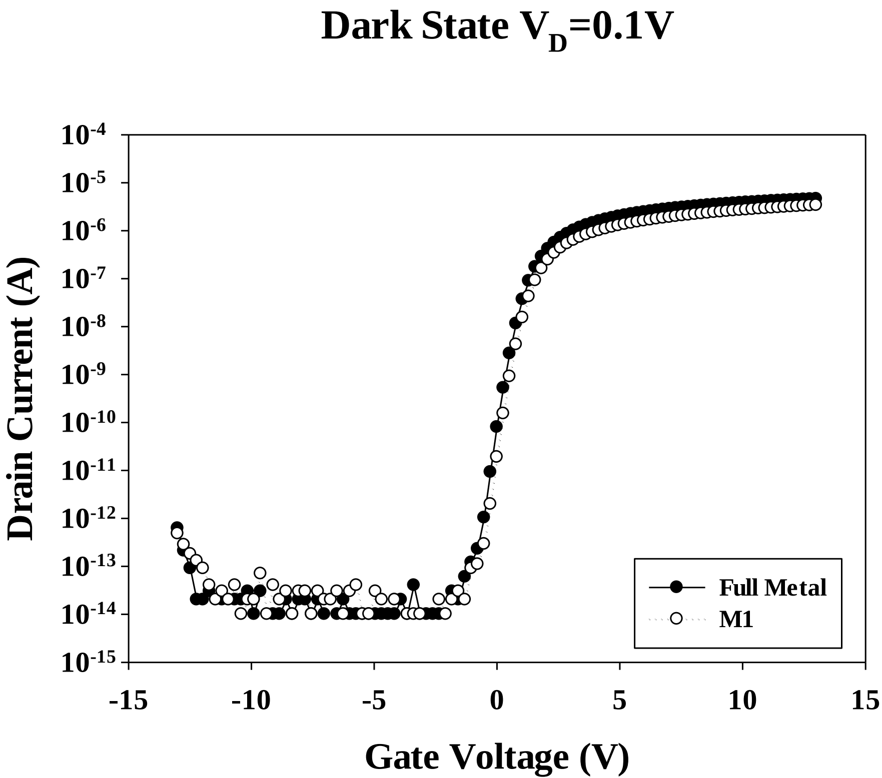


Fig.3.2.11 The I_D-V_G relationship of M1 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under darkness.

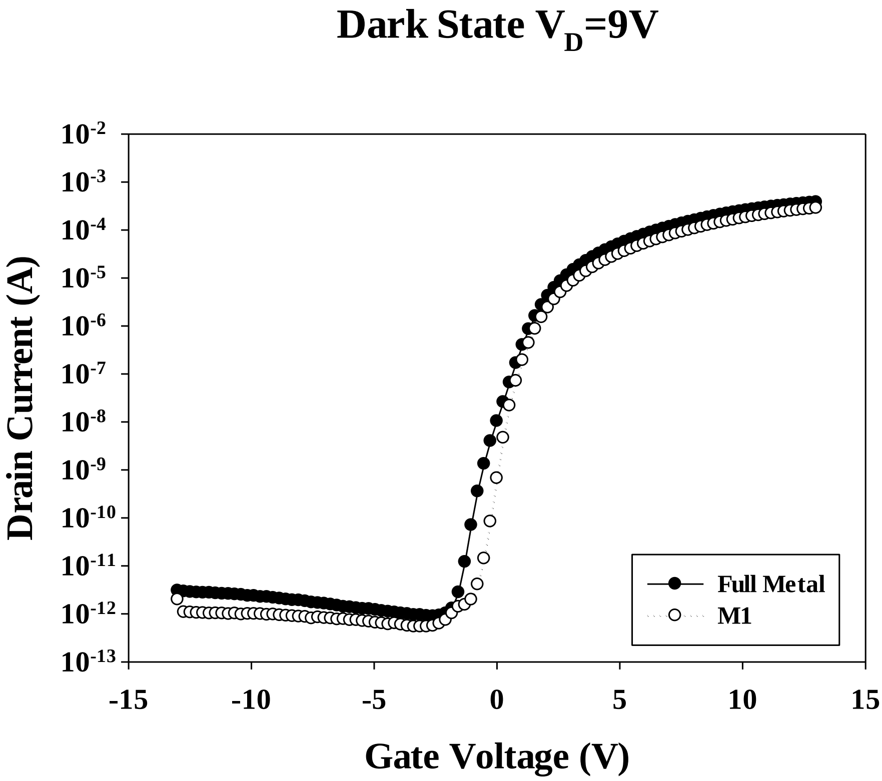


Fig.3.2.12 The I_D-V_G relationship of M1 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under darkness.

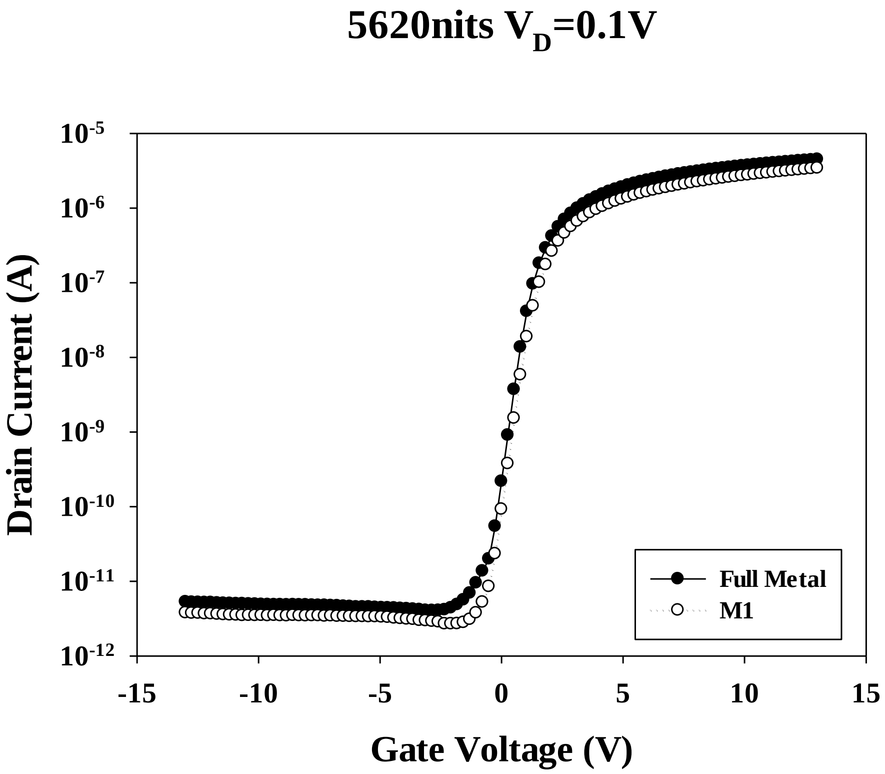


Fig.3.2.13 The I_D-V_G relationship of M1 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under illumination.

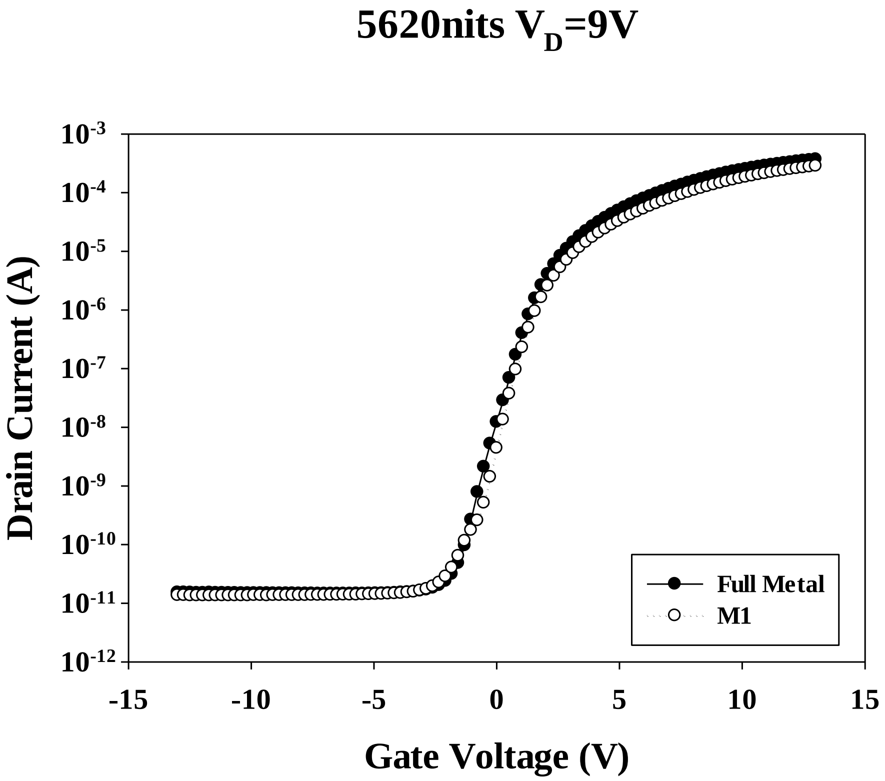


Fig.3.2.14 The I_D-V_G relationship of M1 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under illumination.

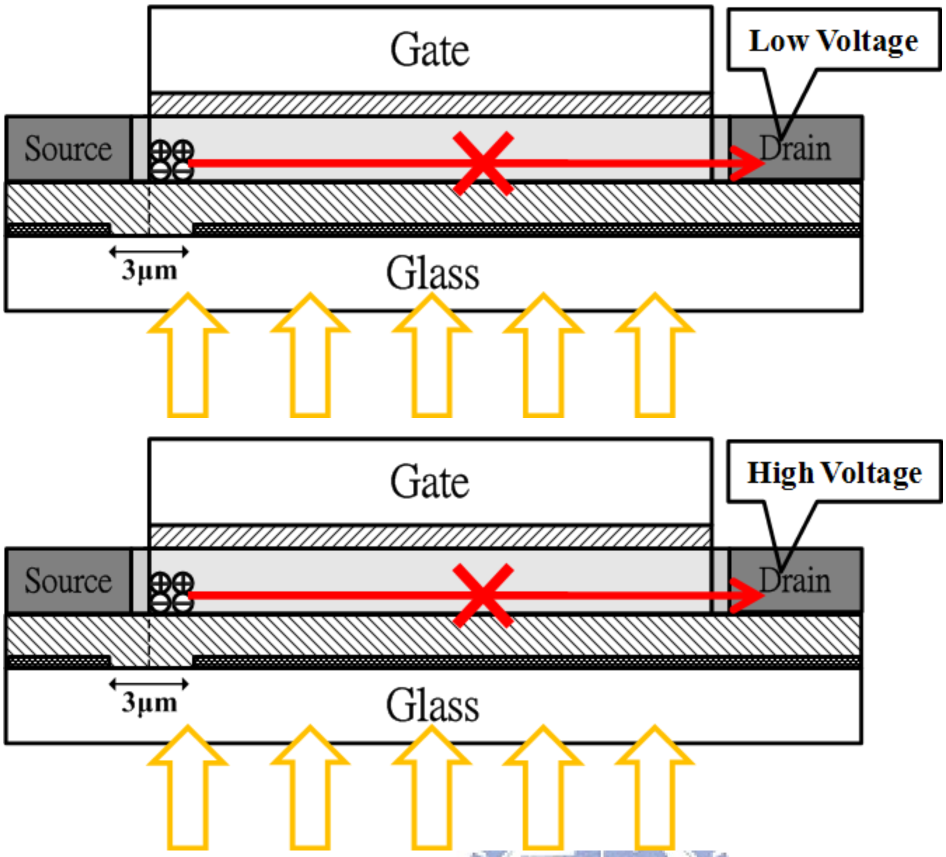


Fig.3.2.15 The photo leakage current model of M1 TFT.

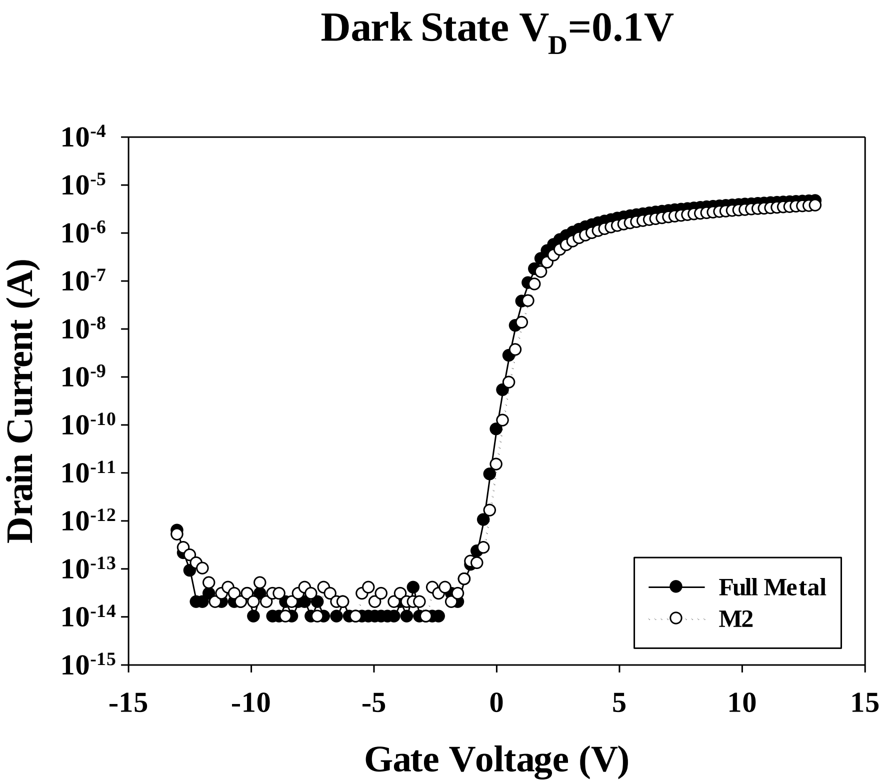


Fig.3.2.16 The I_D-V_G relationship of M2 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under darkness.

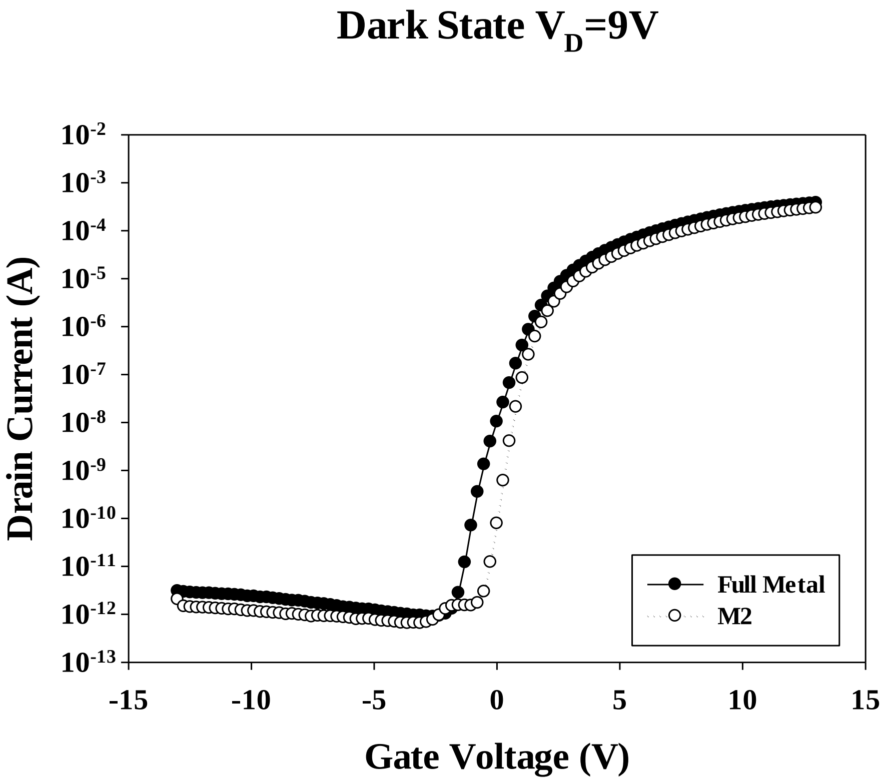


Fig.3.2.17 The I_D-V_G relationship of M2 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under darkness.

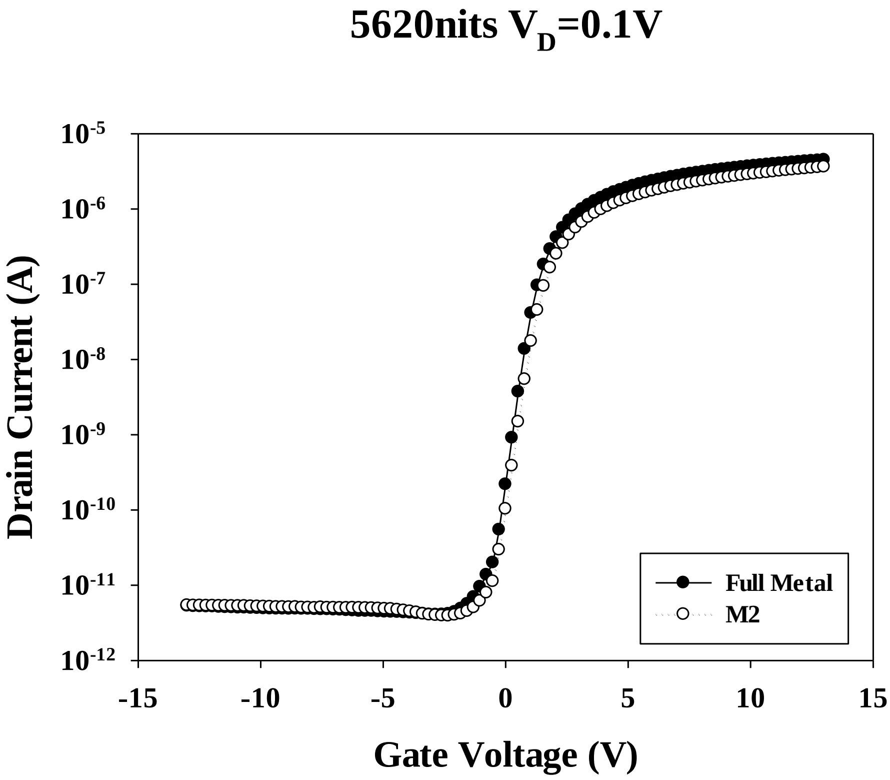


Fig.3.2.18 The I_D-V_G relationship of M2 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under illumination.

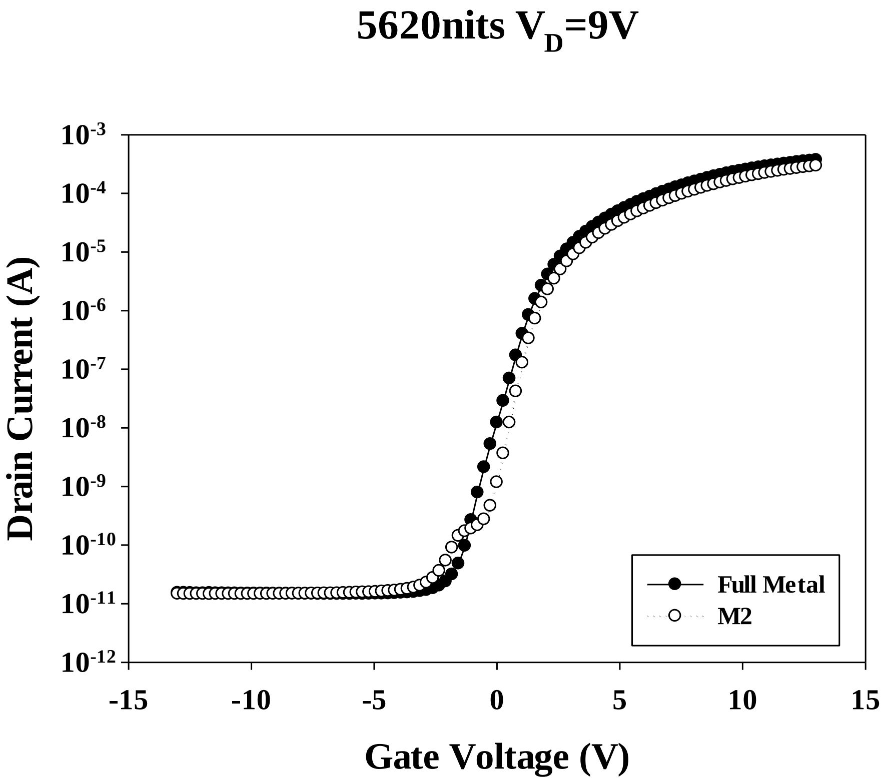


Fig.3.2.19 The I_D-V_G relationship of M2 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under illumination.

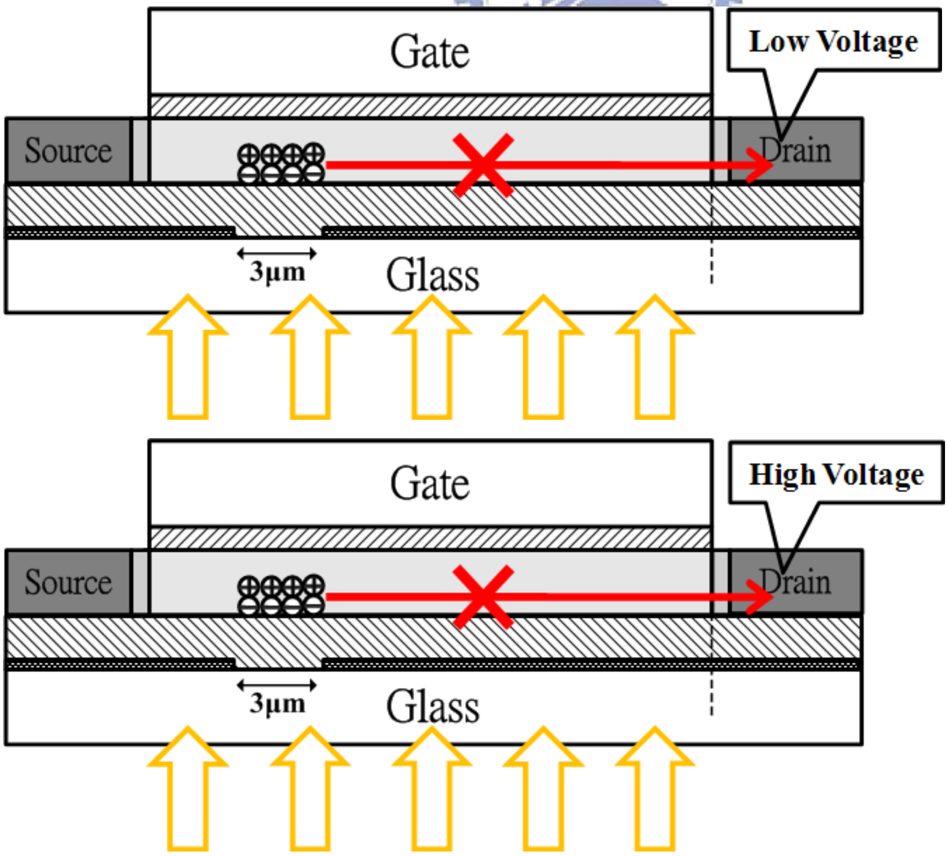


Fig.3.2.20 The photo leakage current model of M2 TFT.

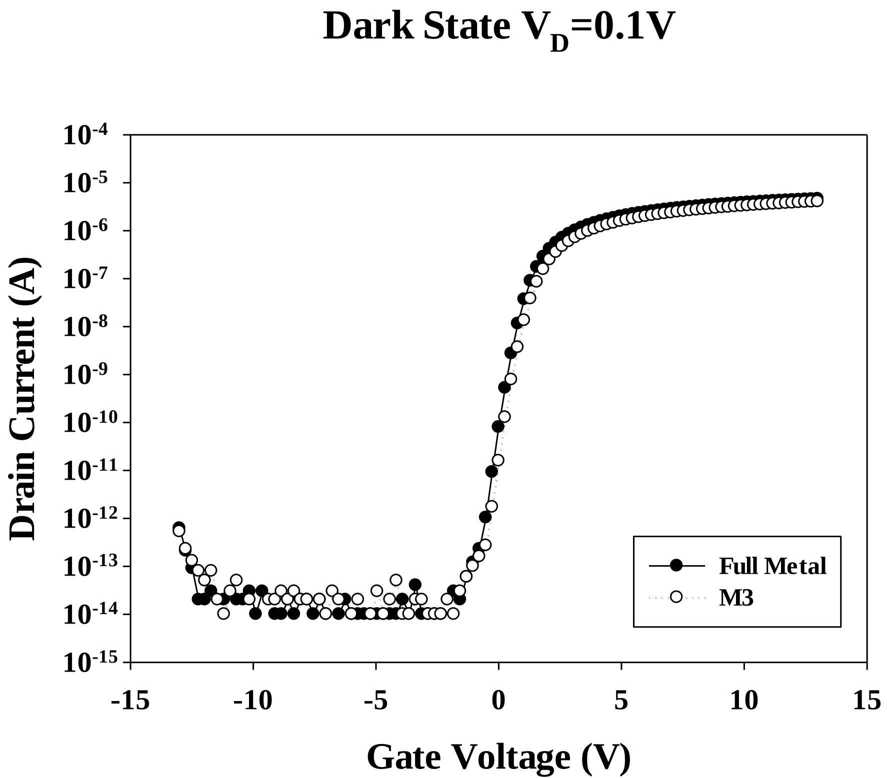


Fig.3.2.21 The I_D-V_G relationship of M3 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under darkness.

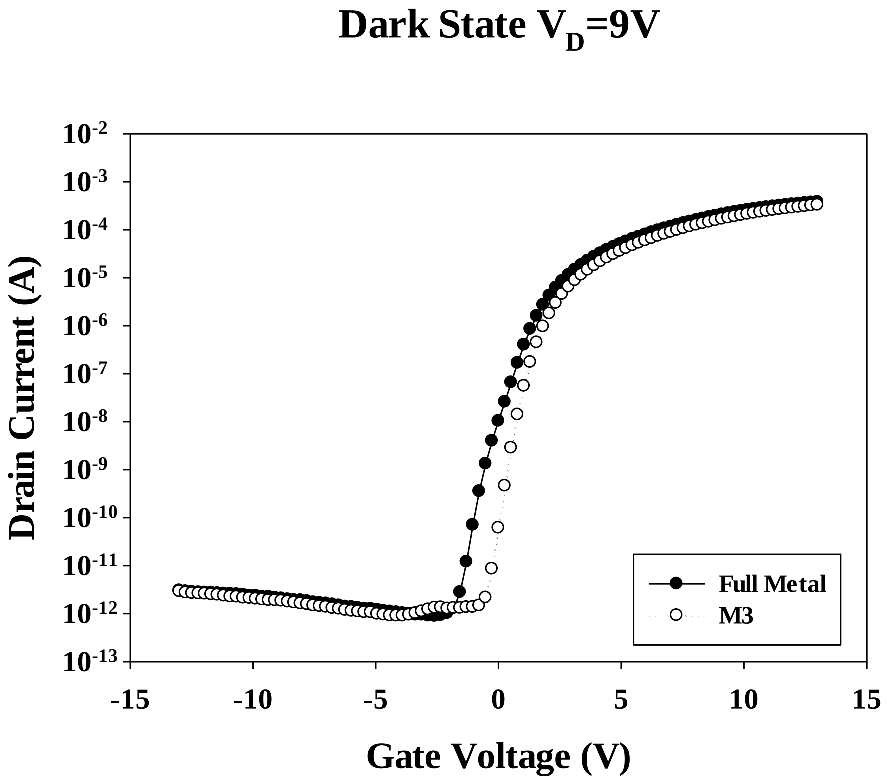


Fig.3.2.22 The I_D-V_G relationship of M3 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under darkness.

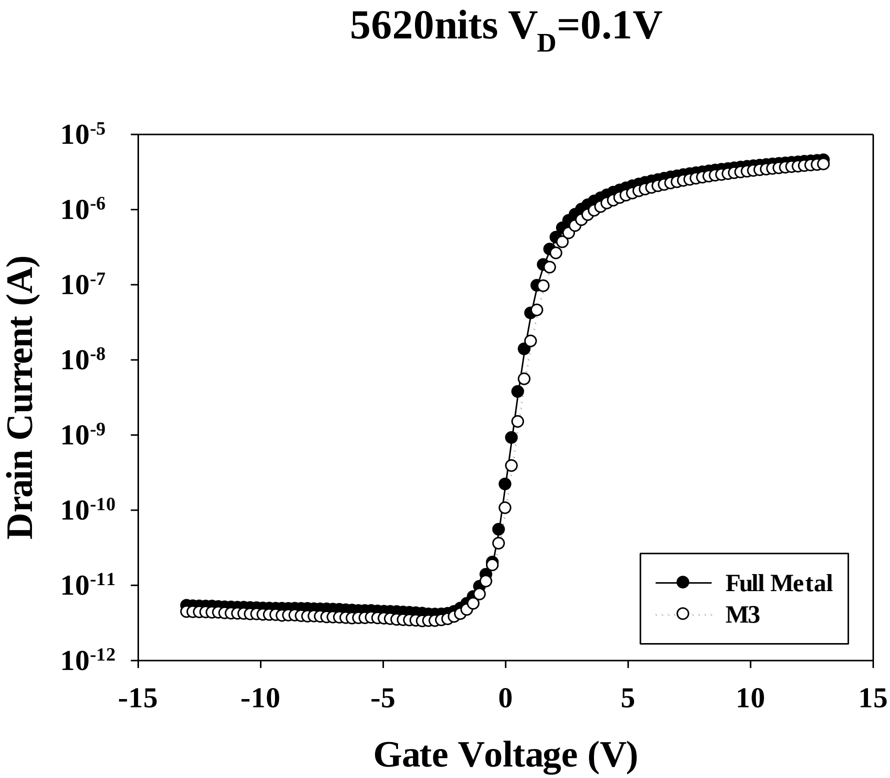


Fig.3.2.23 The I_D-V_G relationship of M3 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under illumination.

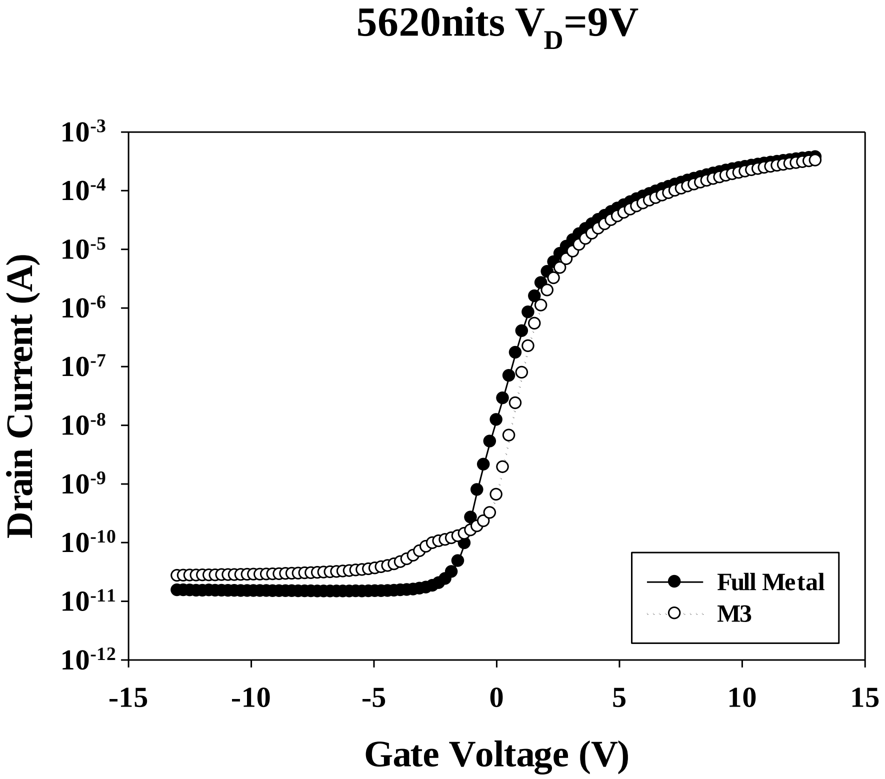


Fig.3.2.24 The I_D-V_G relationship of M3 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under illumination.

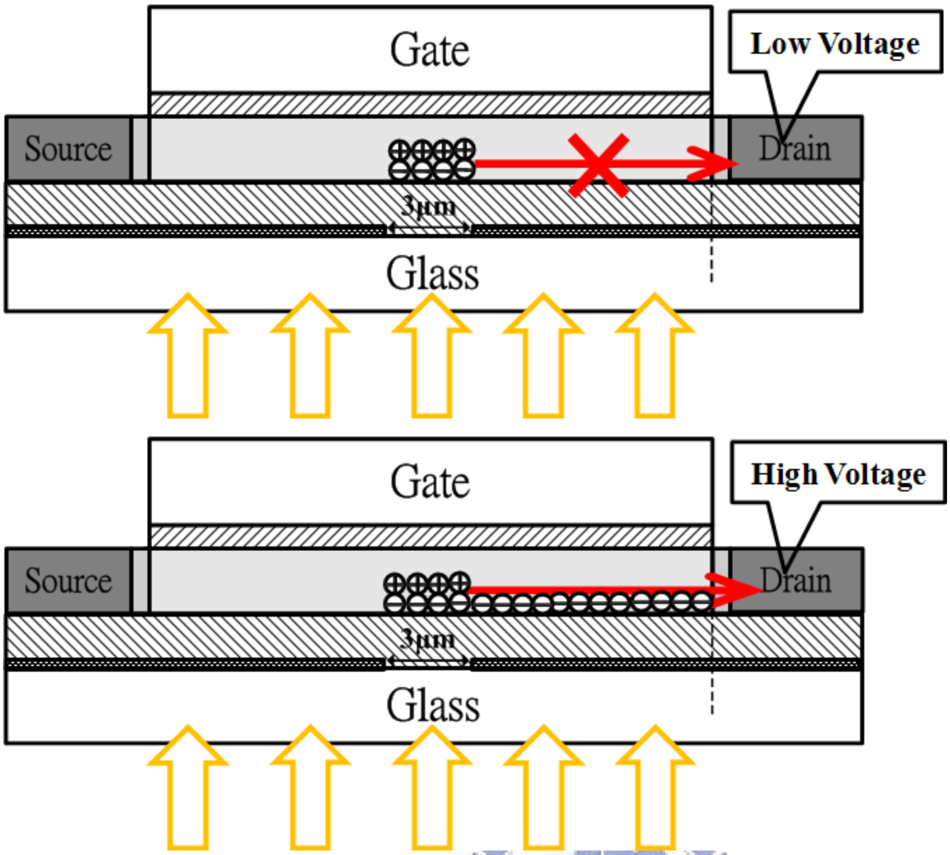


Fig.3.2.25 The photo leakage current model of M3 TFT.

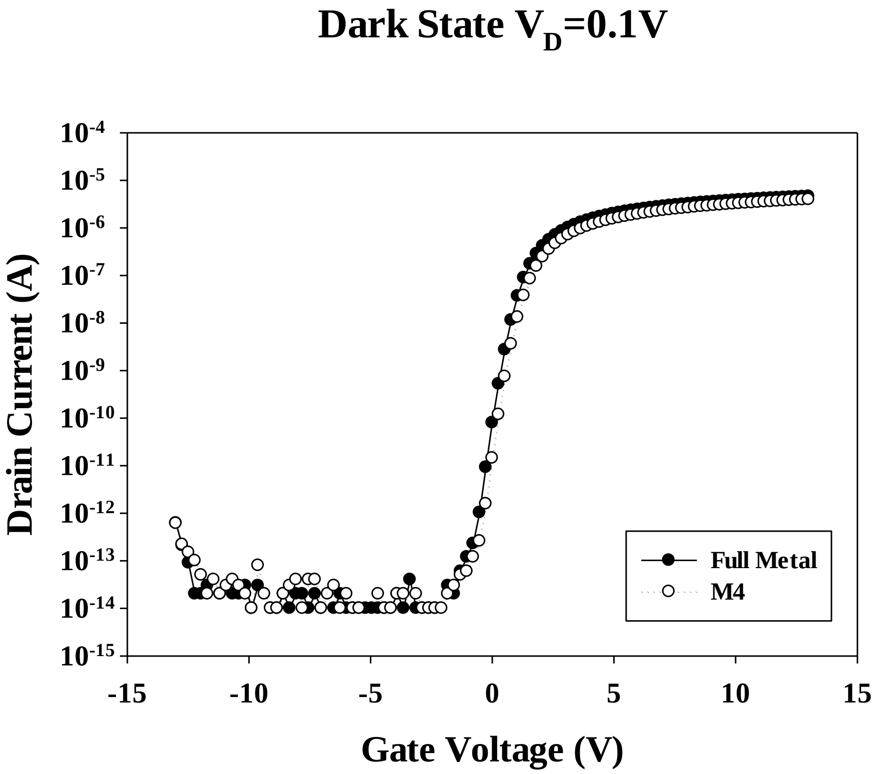


Fig.3.2.26 The I_D-V_G relationship of M4 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under darkness.

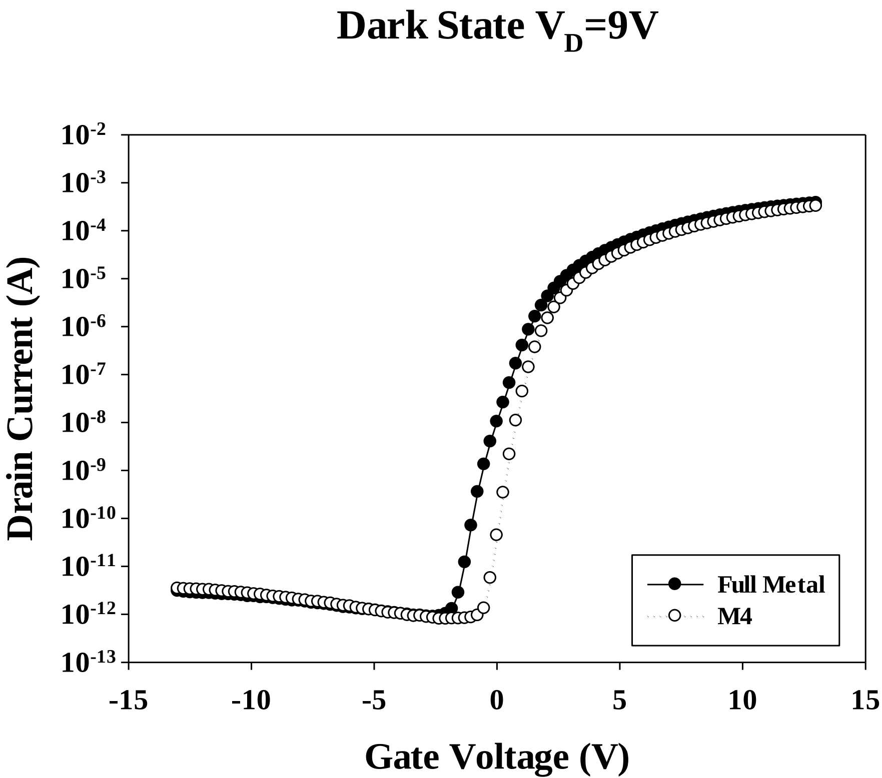


Fig.3.2.27 The I_D-V_G relationship of M4 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under darkness.

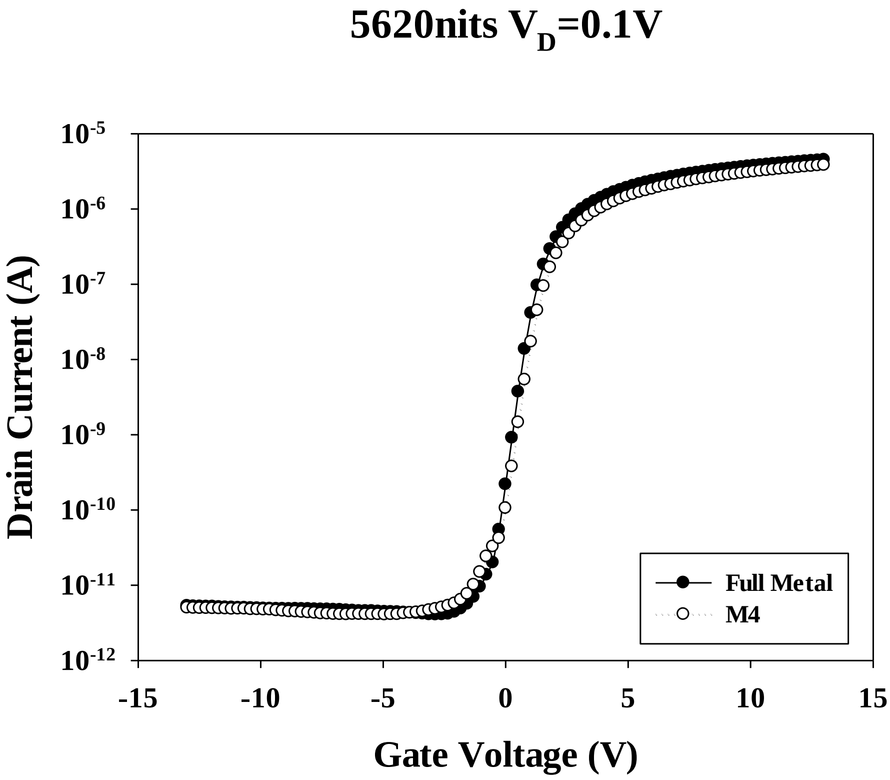


Fig.3.2.28 The I_D-V_G relationship of M4 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under illumination.

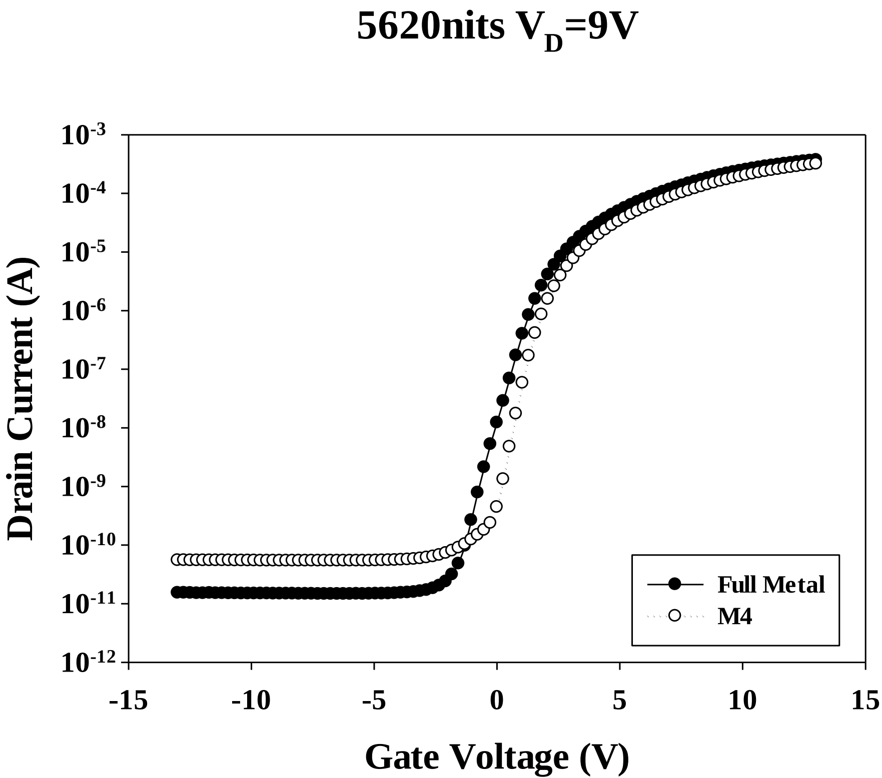


Fig.3.2.29 The I_D-V_G relationship of M4 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under illumination.

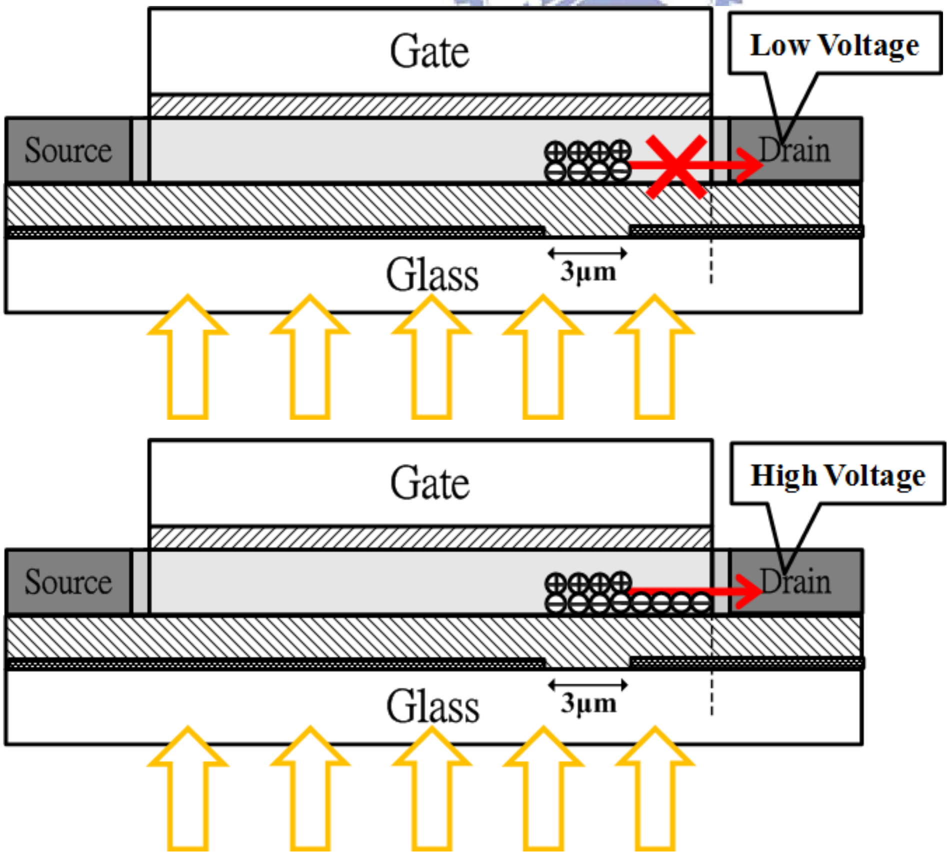


Fig.3.2.30 The photo leakage current model of M4 TFT.

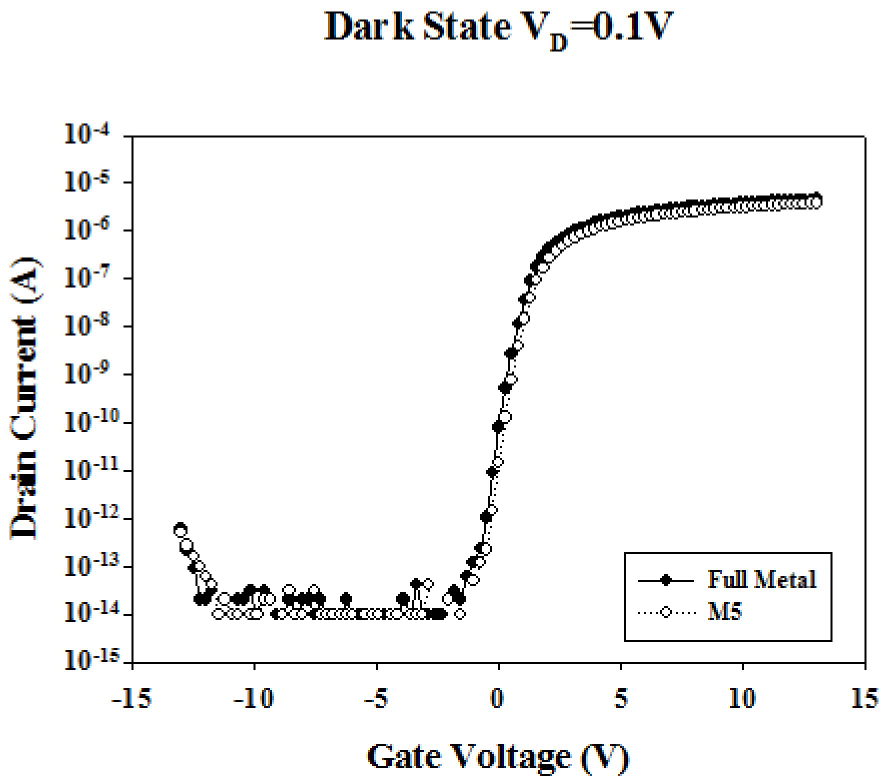


Fig.3.2.31 The I_D-V_G relationship of M5 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under darkness.

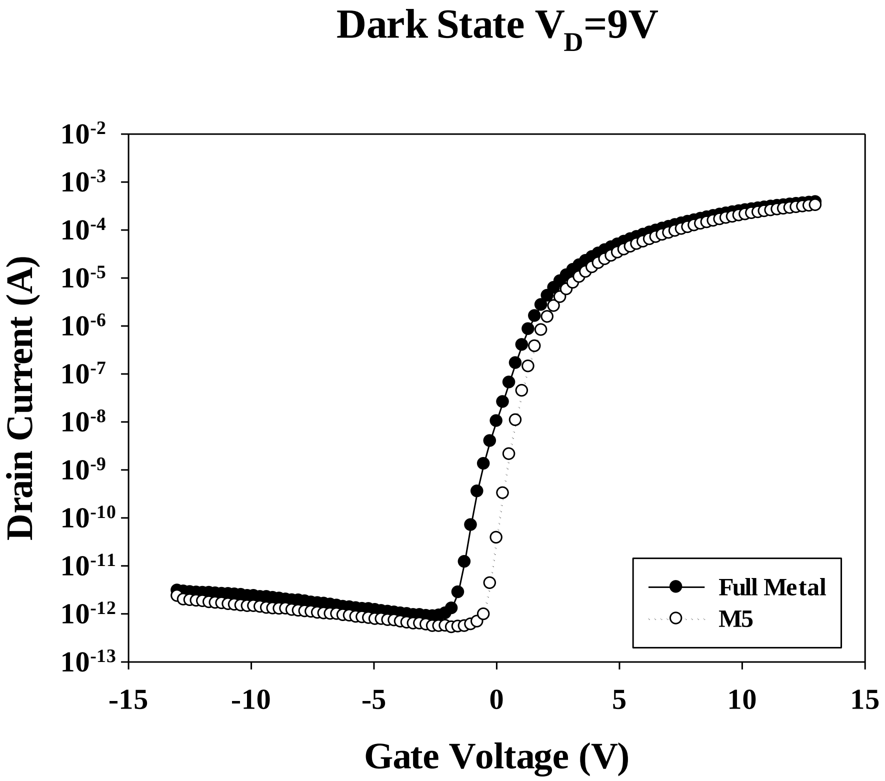


Fig.3.2.32 The I_D-V_G relationship of M5 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under darkness.

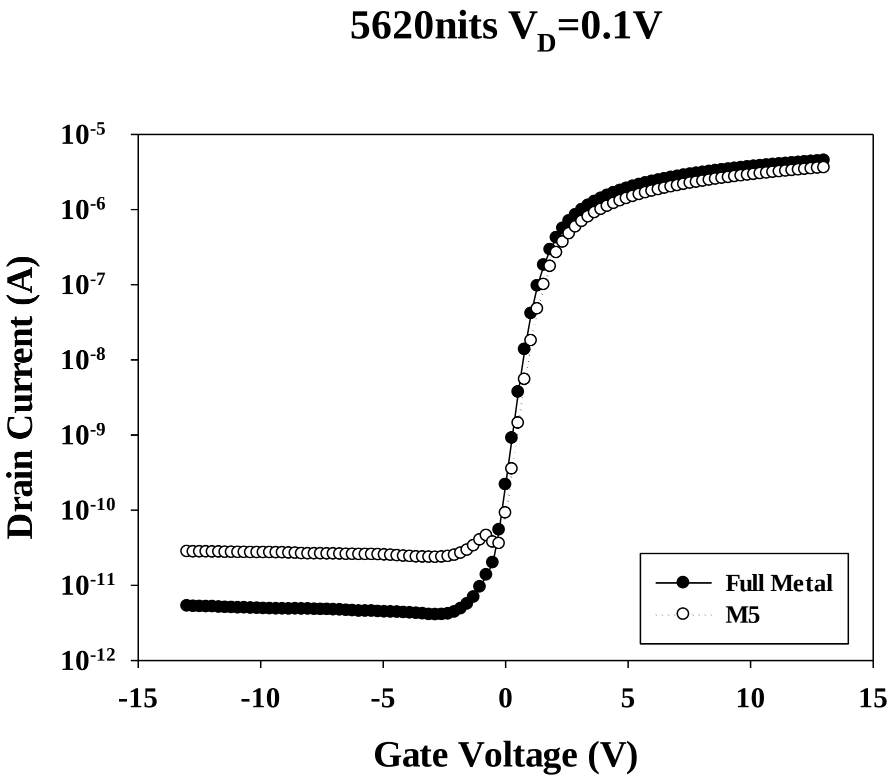


Fig.3.2.33 The I_D-V_G relationship of M5 TFT and Full-Metal-Shielding TFT with the drain voltage is 0.1V under illumination.

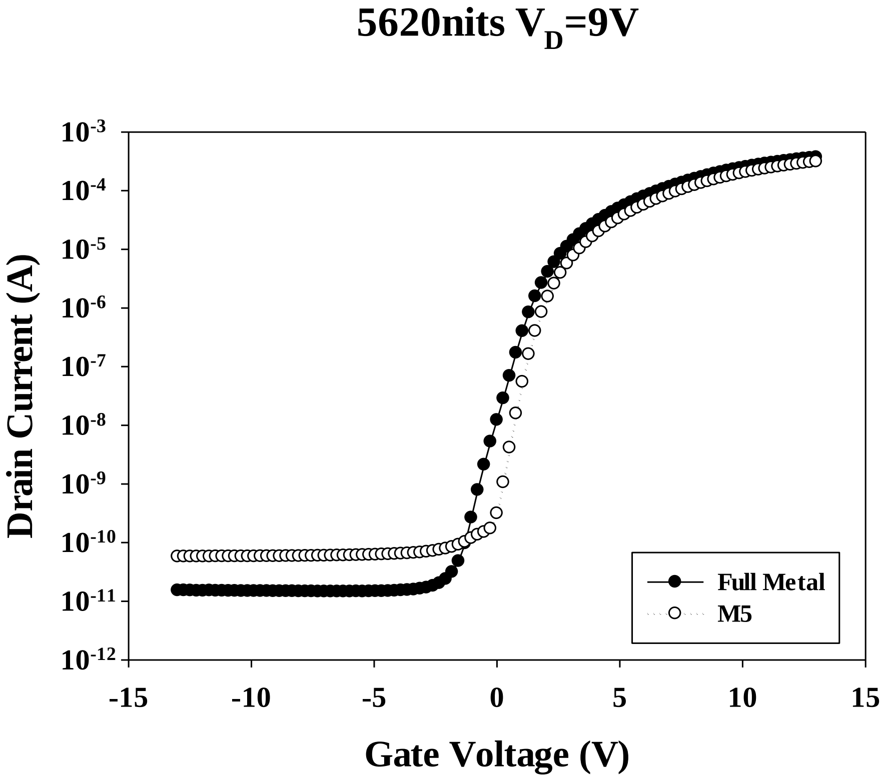


Fig.3.2.34 The I_D-V_G relationship of M5 TFT and Full-Metal-Shielding TFT with the drain voltage is 9V under illumination.

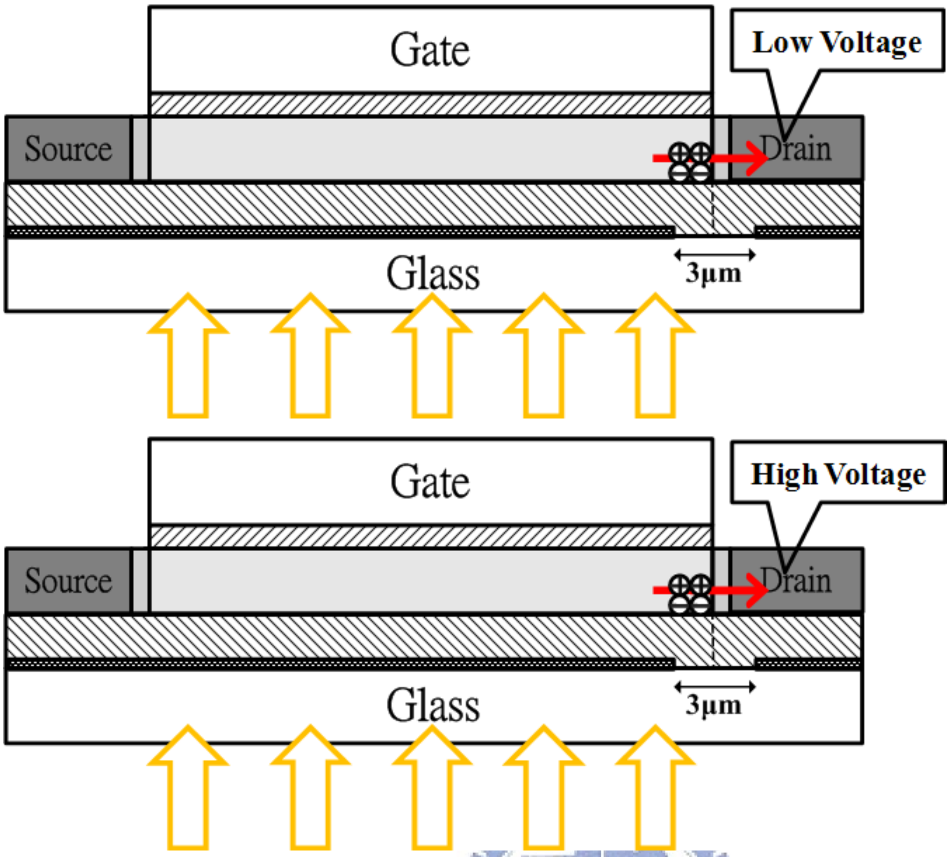


Fig.3.2.35 The photo leakage current model of M5 TFT.

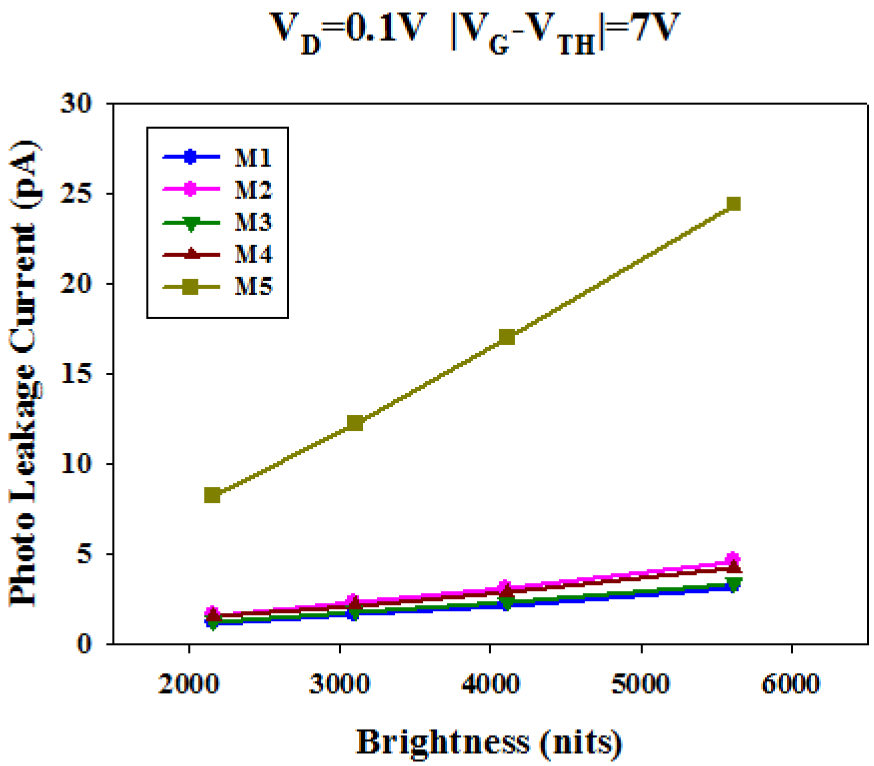


Fig.3.2.36 The I_{PLC} extracted at a voltage $|V_G\text{-}V_{TH}|$ of 7V as V_D is 0.1V for TFT.

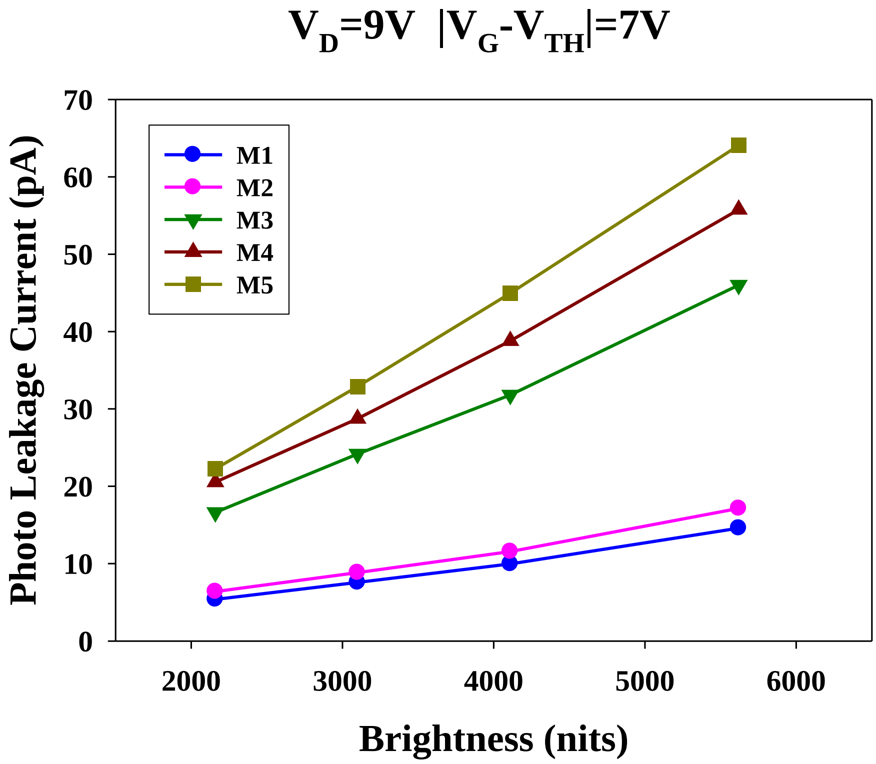


Fig.3.2.37 The I_{PLC} extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 9V for TFT.

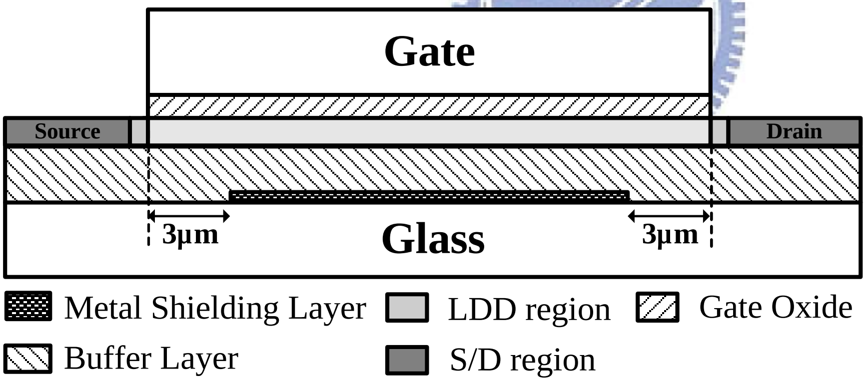


Fig.3.3.1 The partial metal shielding layer is located in channel region.

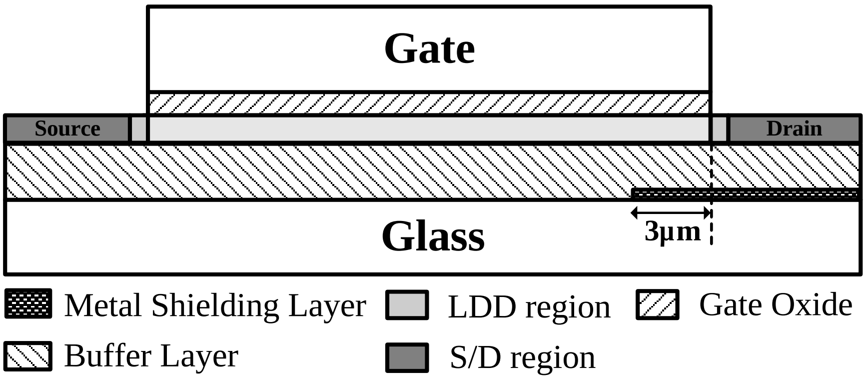


Fig.3.3.2 The partial metal shielding layer is located in drain junction region.

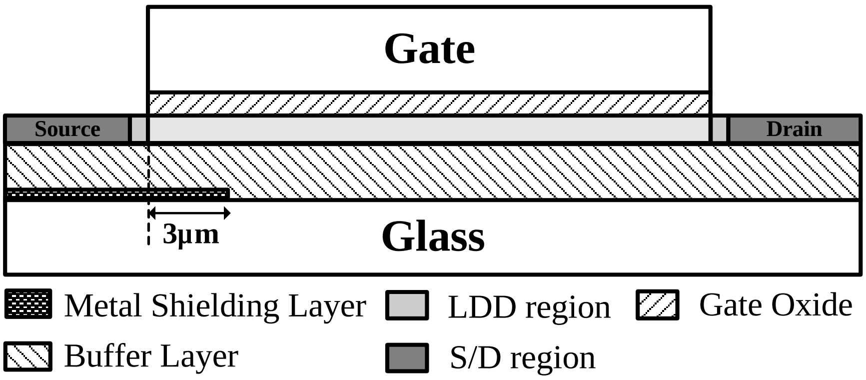


Fig.3.3.3 The partial metal shielding layer is located in source junction region.

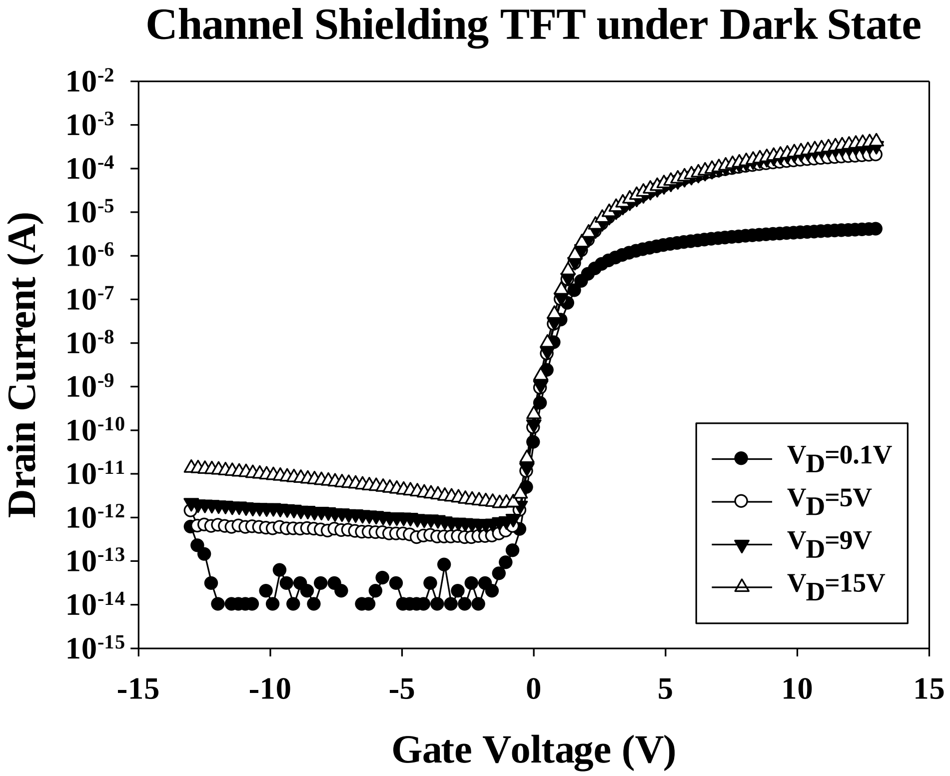

Channel Shielding TFT under Dark State

Fig.3.3.4 The I_D-V_G relationships of poly-Si TFT with partial metal shielding layer located in channel region.

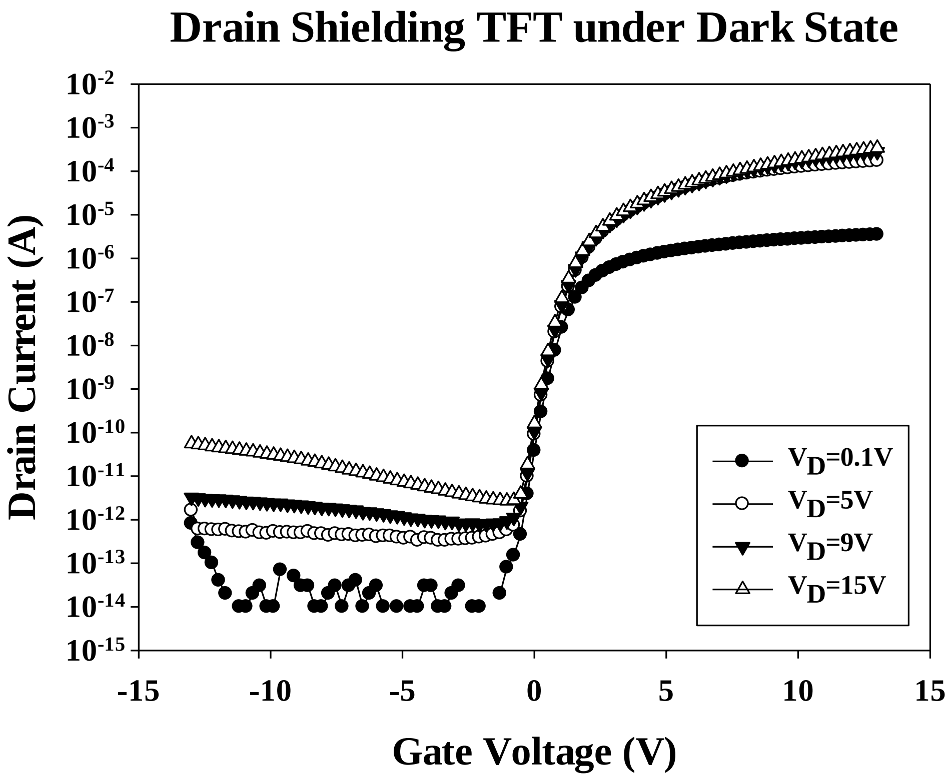


Fig.3.3.5 The I_D-V_G relationships of poly-Si TFT with partial metal shielding layer located in drain junction region.

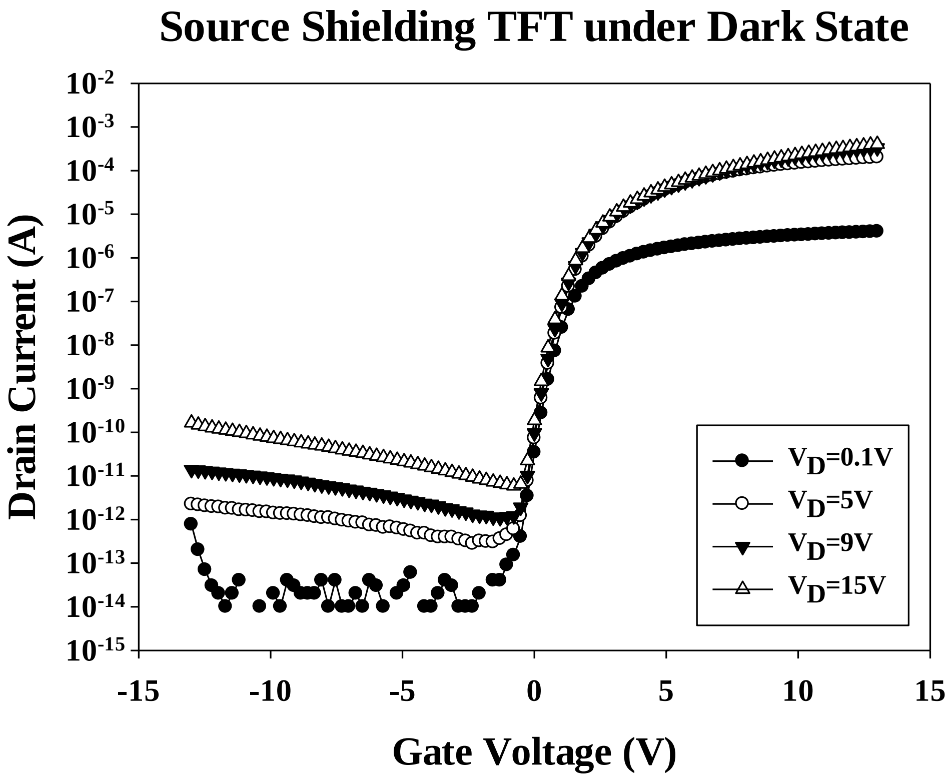


Fig.3.3.6 The I_D-V_G relationships of poly-Si TFT with partial metal shielding layer located in source junction region.

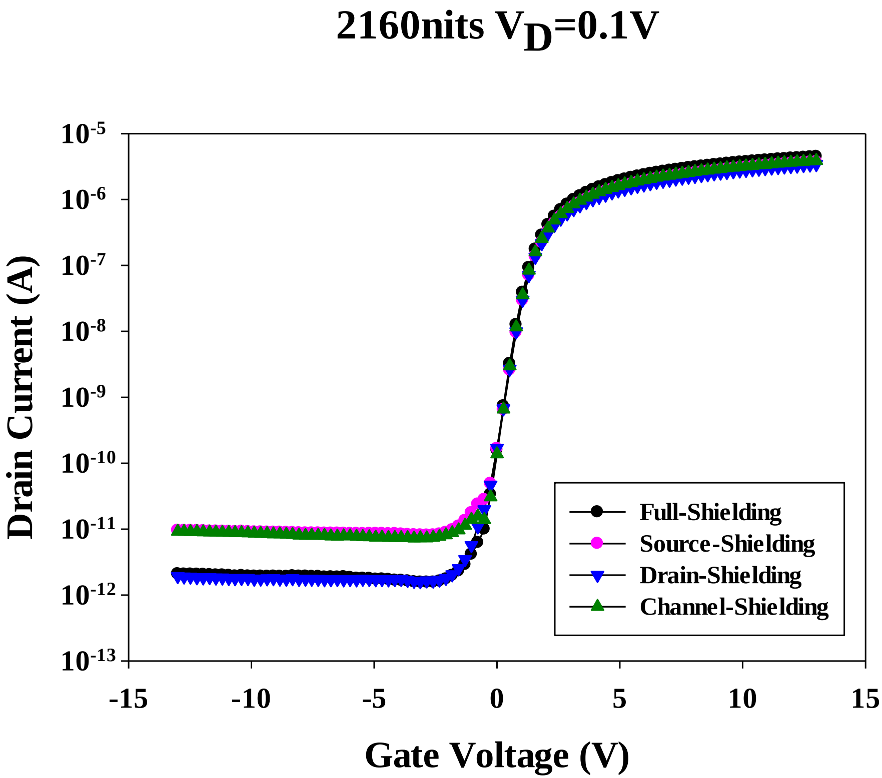


Fig.3.3.7 The I_D-V_G relationships of Poly-Si TFT with metal shielding layer. The drain voltage is 0.1V, and the illumination is 2160 nits.

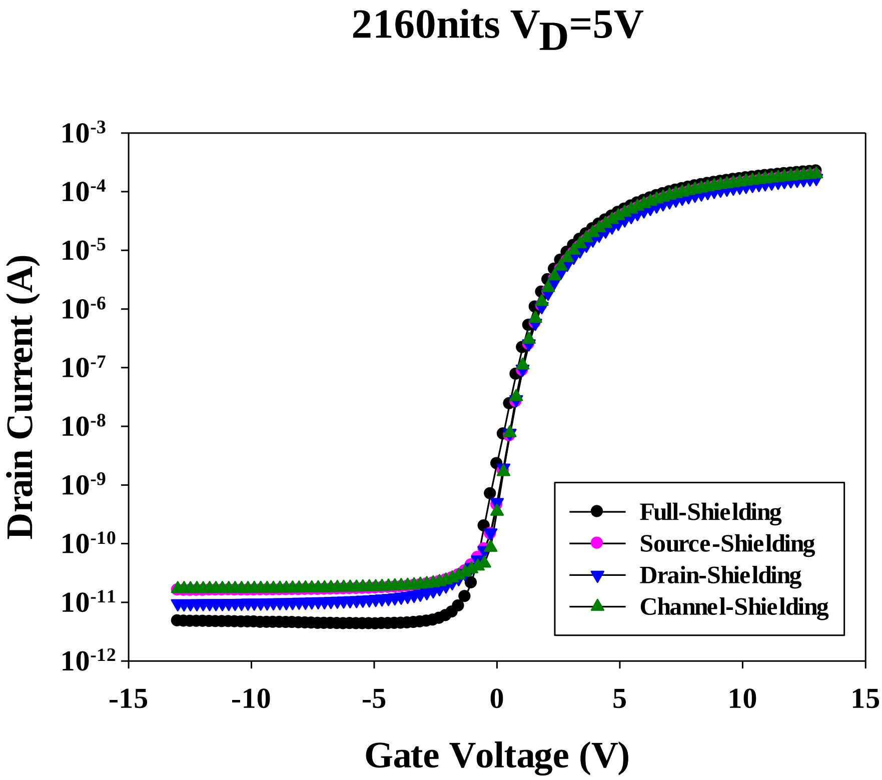


Fig.3.3.8 The I_D-V_G relationships of Poly-Si TFT with metal shielding layer. The drain voltage is 5V, and the illumination is 2160 nits.

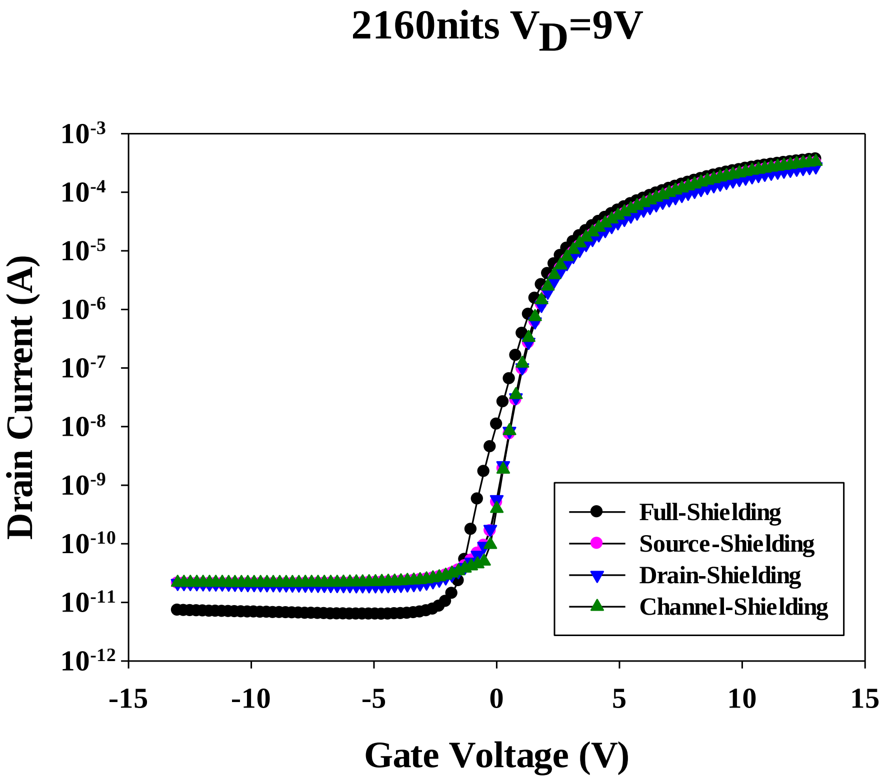


Fig.3.3.9 The I_D-V_G relationships of Poly-Si TFT with metal shielding layer. The drain voltage is 9V, and the illumination is 2160 nits.

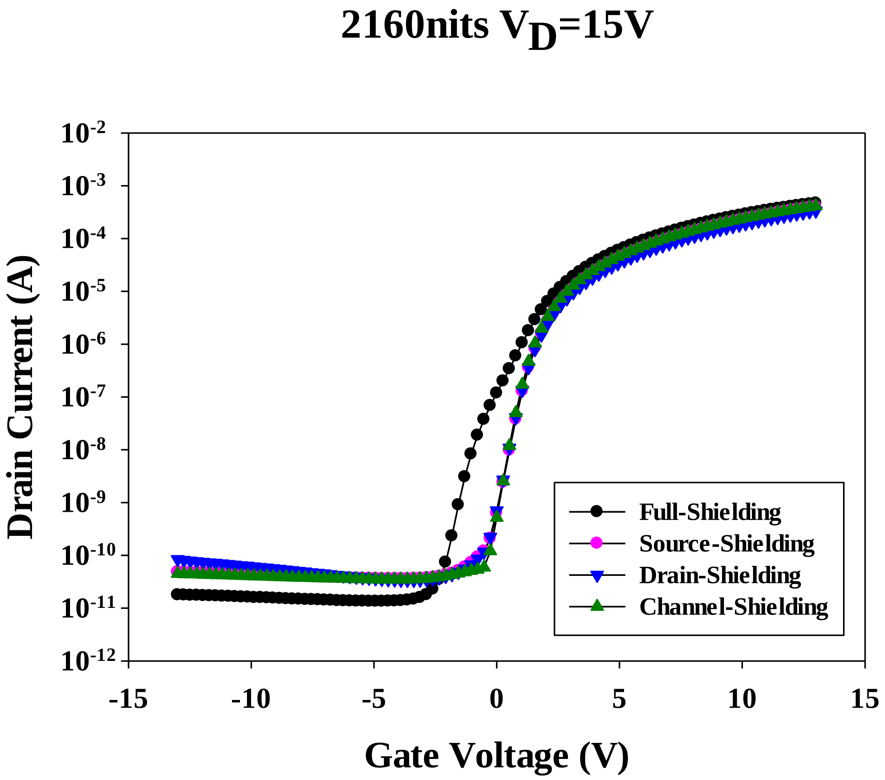


Fig.3.3.10 The I_D-V_G relationships of Poly-Si TFT with metal shielding layer. The drain voltage is 15V, and the illumination is 2160 nits.

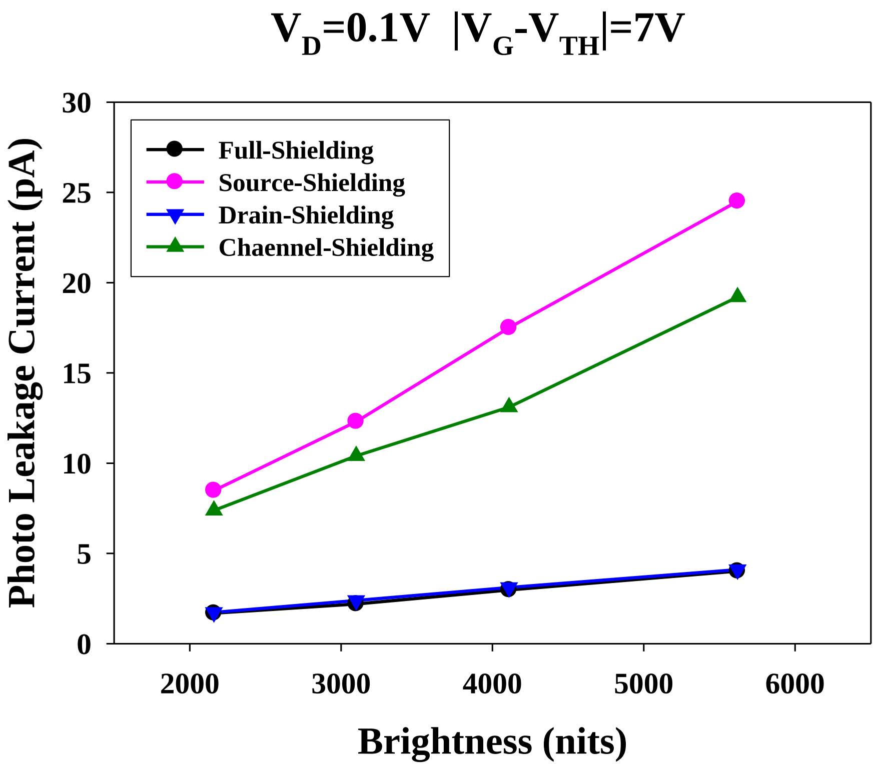


Fig.3.3.11 The I_{PLC} extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 0.1V for TFT.

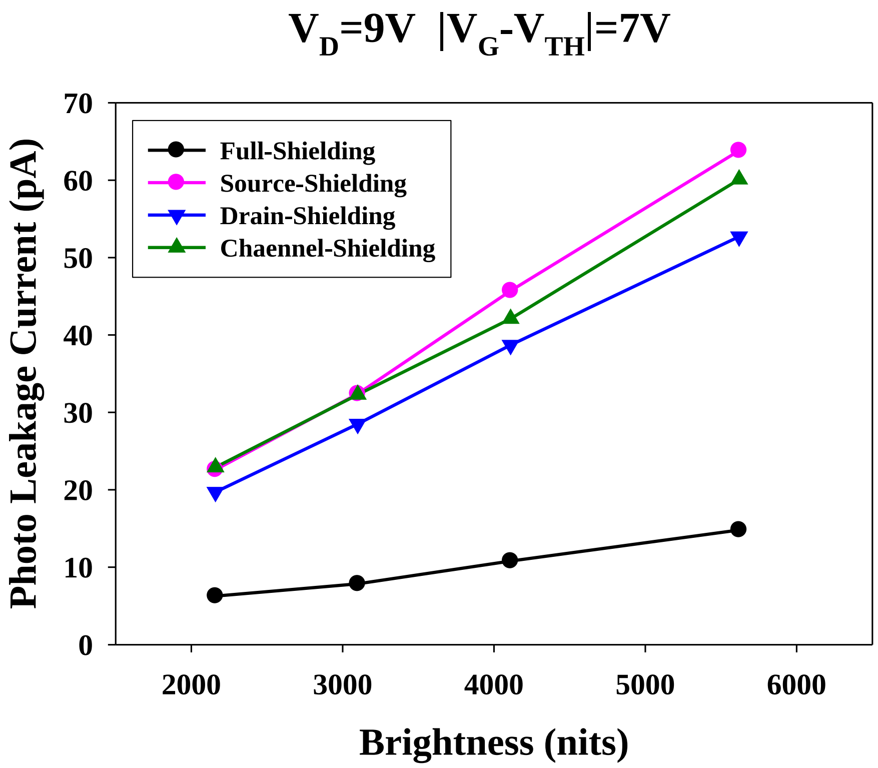


Fig.3.3.12 The I_{PLC} extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is 9V for TFT.

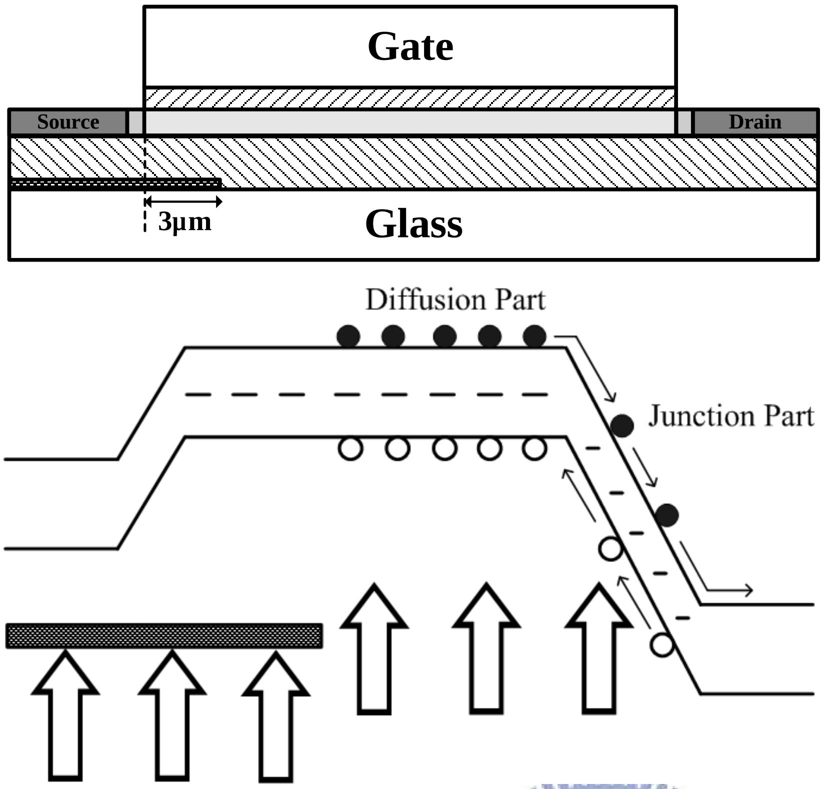


Fig.3.3.13 The band diagram of Source-shielding TFT under illumination.

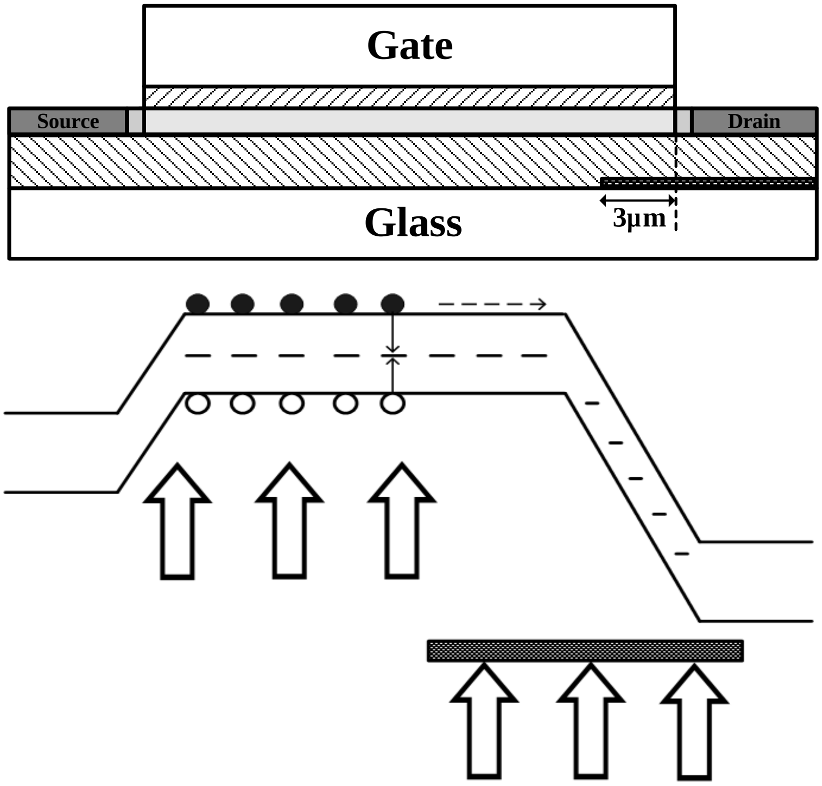


Fig.3.3.14 The band diagram of Drain-shielding TFT under illumination.

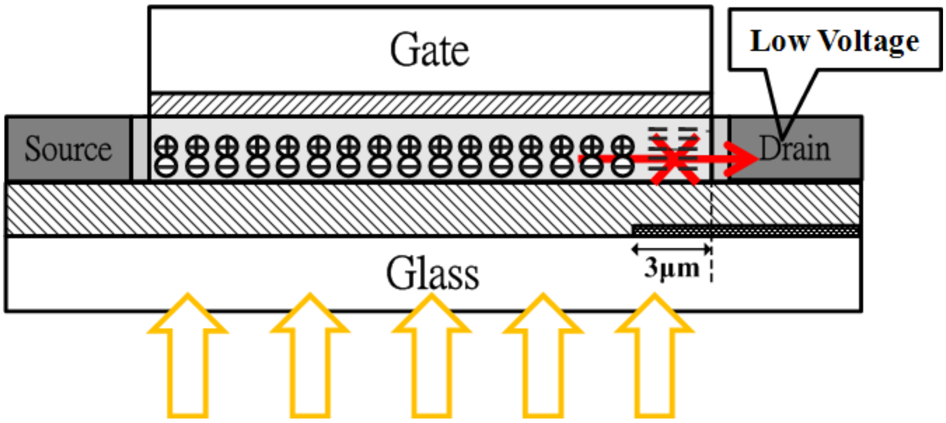


Fig.3.3.15 The photo leakage current model of Drain-shielding TFT at linear region.

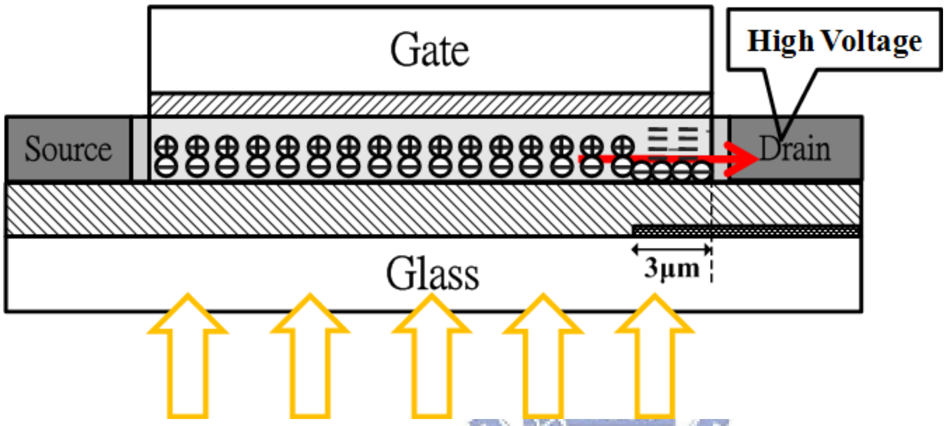


Fig.3.3.16 The photo leakage current model of Drain-shielding TFT at saturation region.

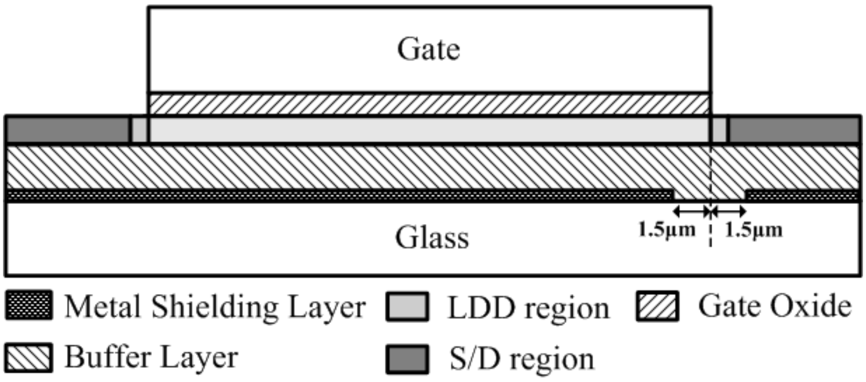


Fig.3.4.1 Poly-Si TFT with split metal shielding layer, the split near the drain junction.

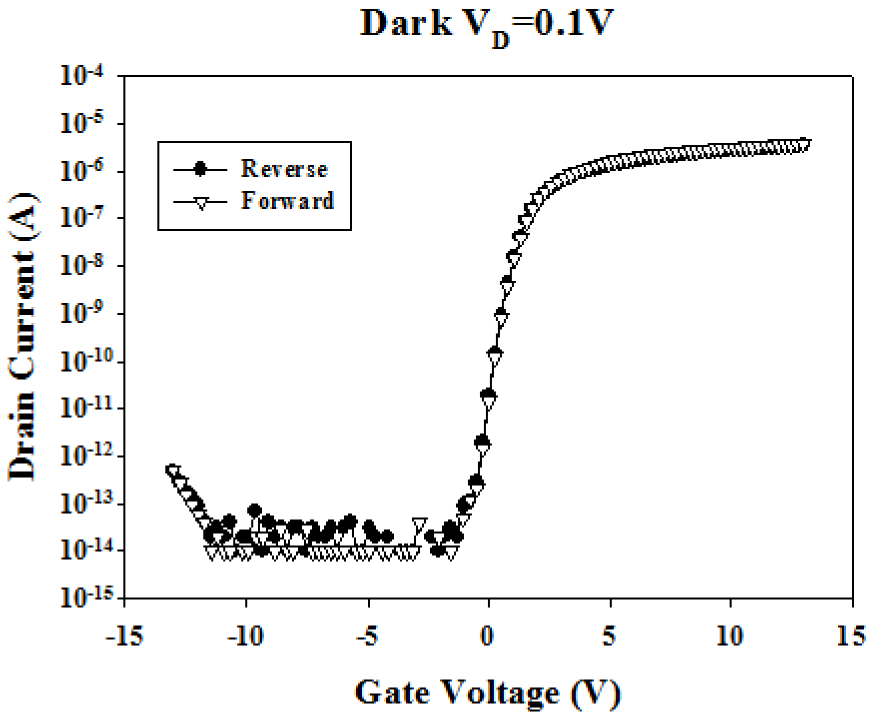


Fig.3.4.2 The I_D-V_G characteristics of shielding TFT with low drain bias measured in forward and reverse modes at dark.

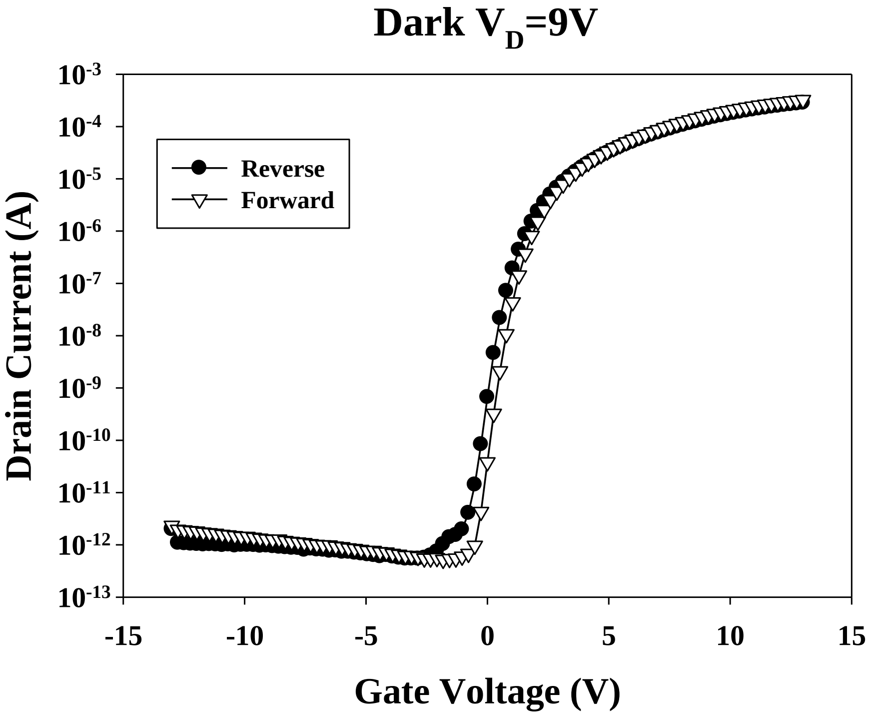


Fig.3.4.3 The I_D-V_G characteristics of shielding TFT with high drain bias measured in forward and reverse modes at dark.

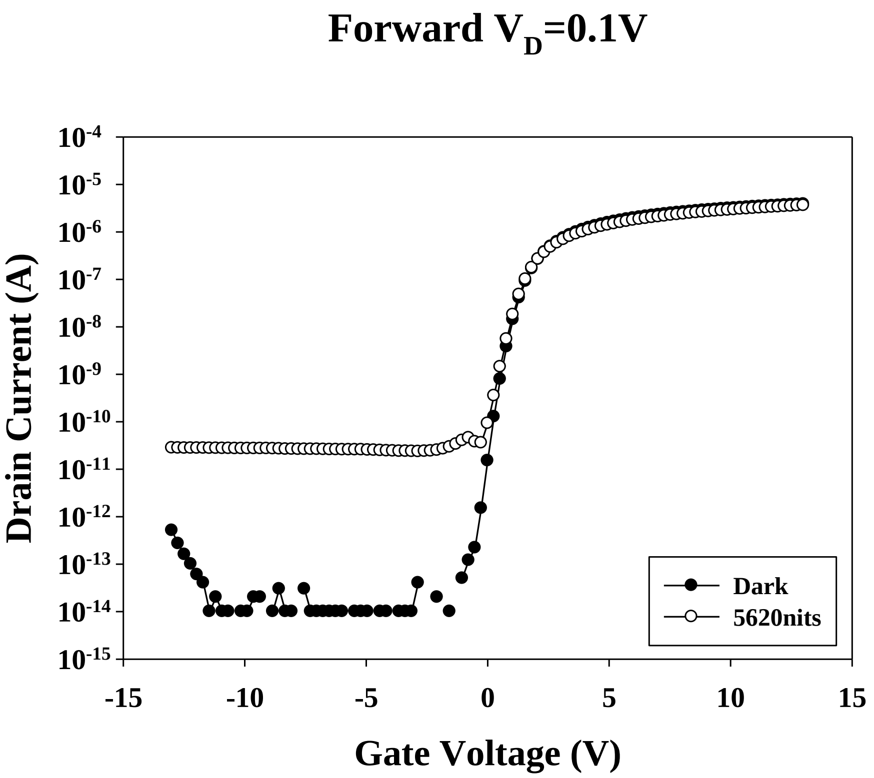


Fig.3.4.4 The I_D-V_G relationships of Forward TFT operated in linear region at the dark and photo states.

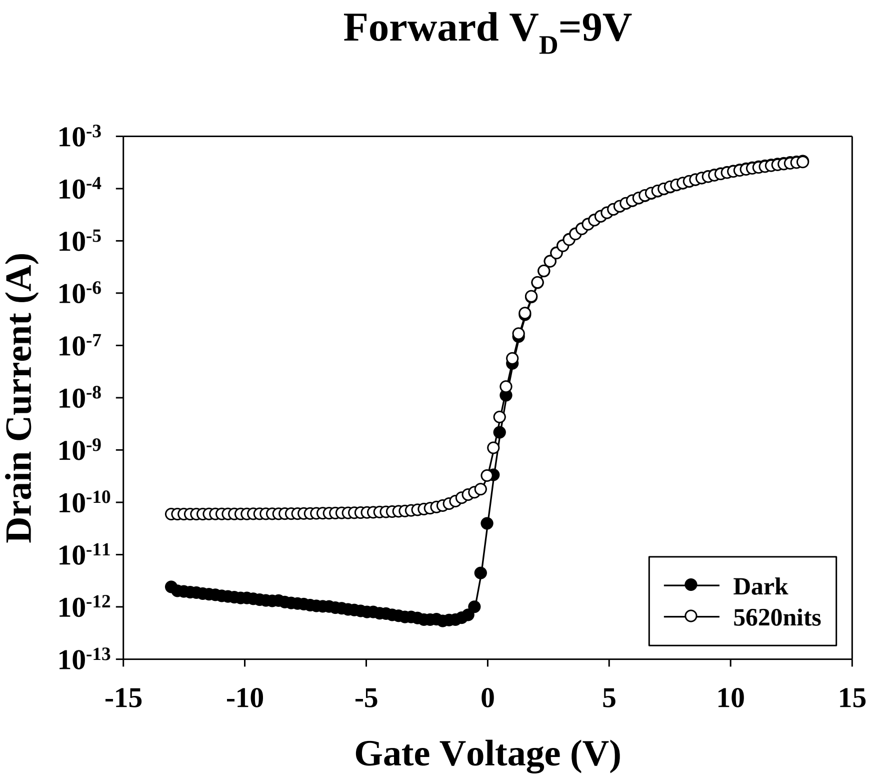


Fig.3.4.5 The I_D-V_G relationships of Forward TFT operated in saturation region at the dark and photo states.

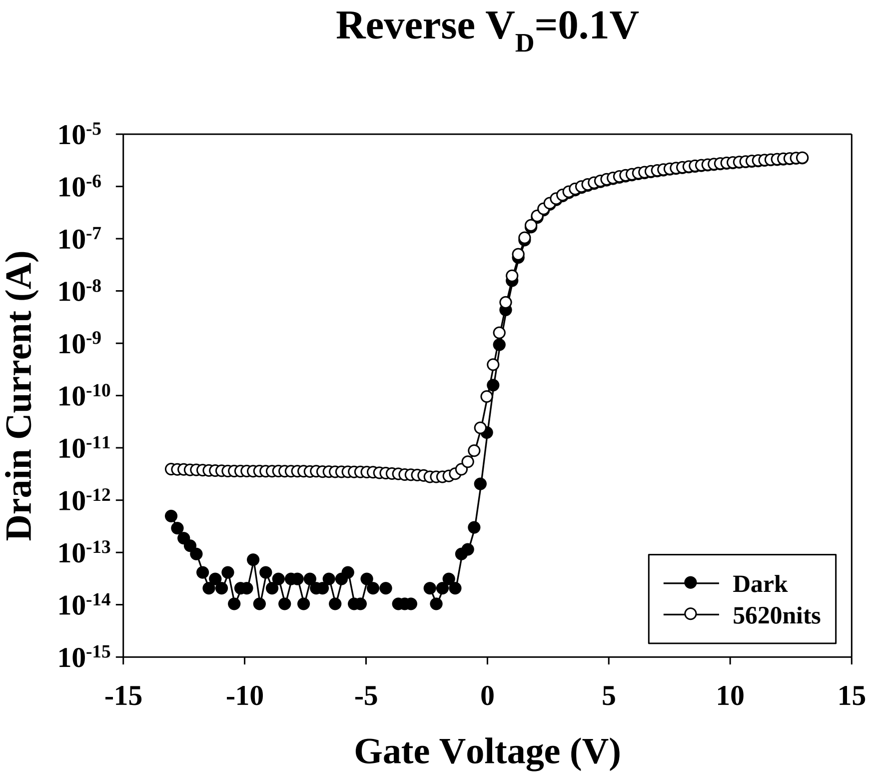


Fig.3.4.6 The I_D-V_G relationships of Reverse TFT operated in linear region at the dark and photo states.

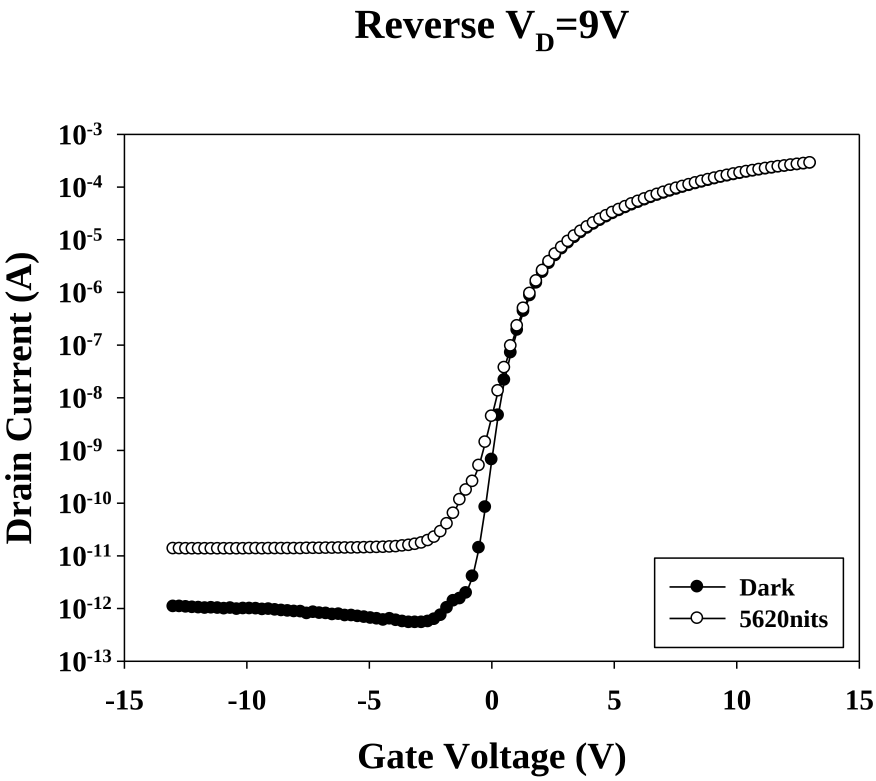


Fig.3.4.7 The I_D-V_G relationships of Reverse TFT operated in saturation region at the dark and photo states.

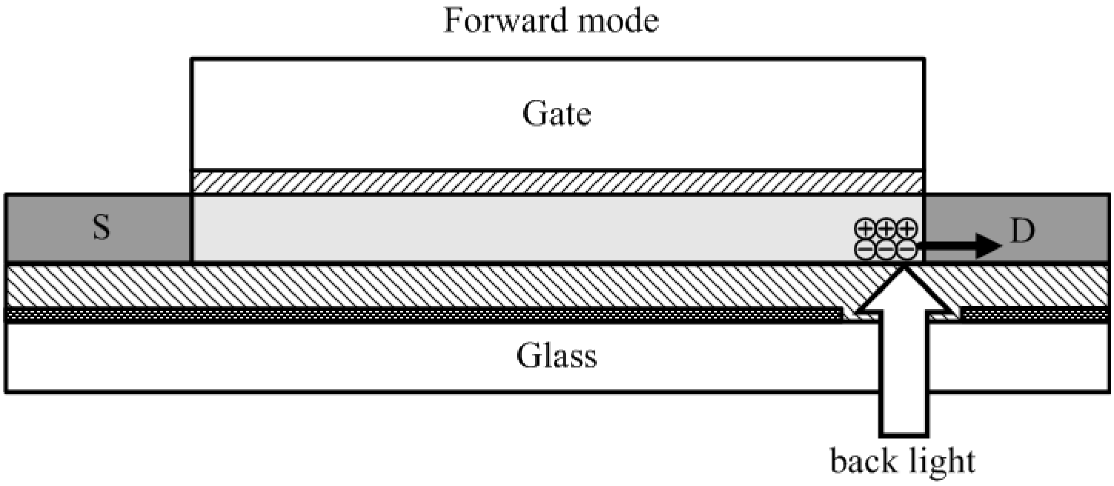


Fig.3.4.8 The photo leakage current model of Forward TFT.

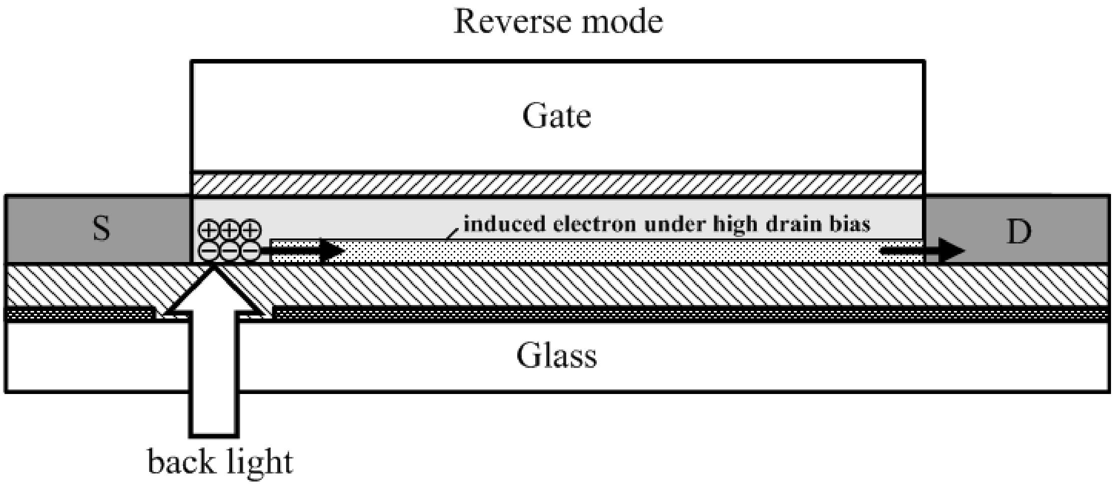


Fig.3.4.9 The photo leakage current model of Reverse TFT.

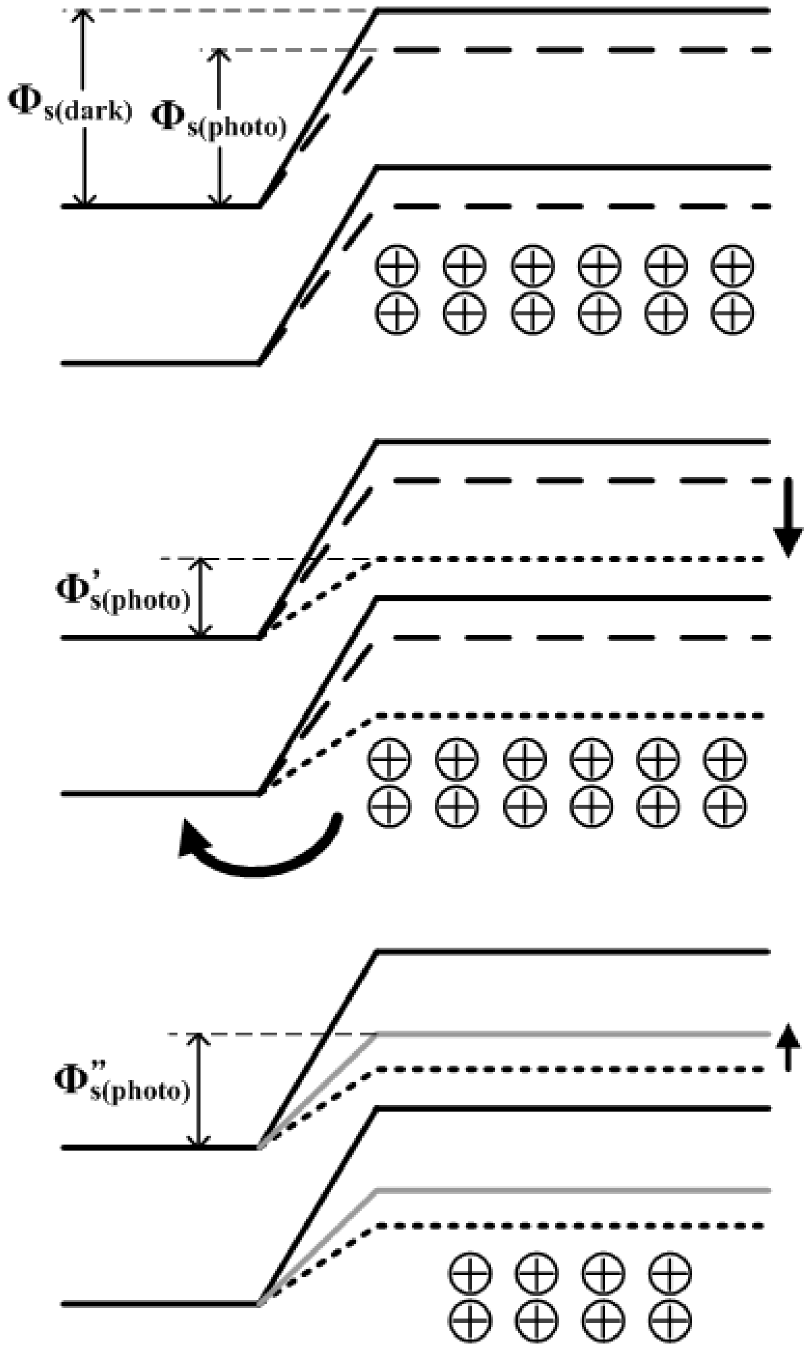


Fig.3.4.10 The model of band diagram to explain the S.S degradation of Poly-Si TFT.

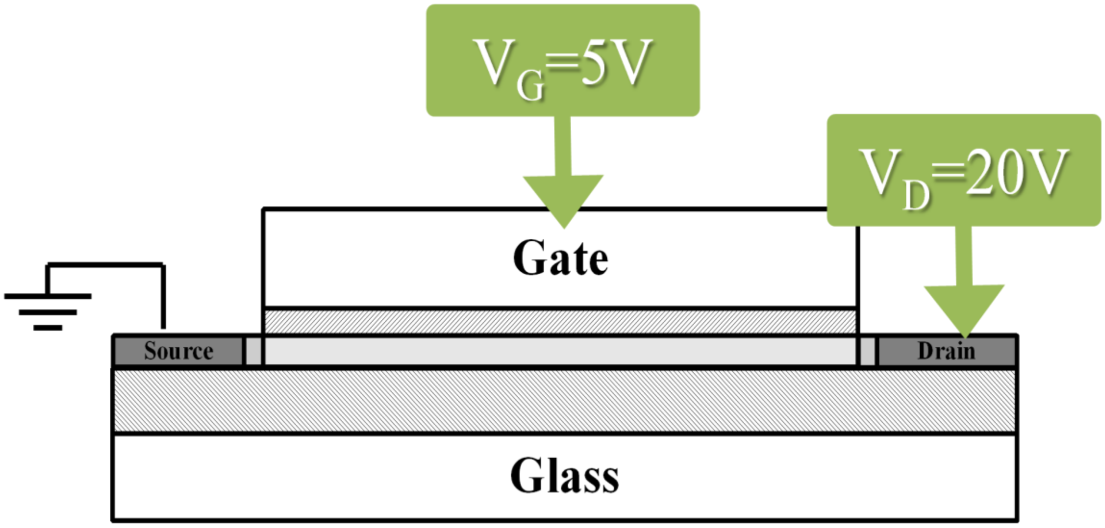


Fig.4.1.1 The Poly-Si TFTs with lightly doped drain (LDD) structure. It is stressed as V_G=5V and V_D=20V.

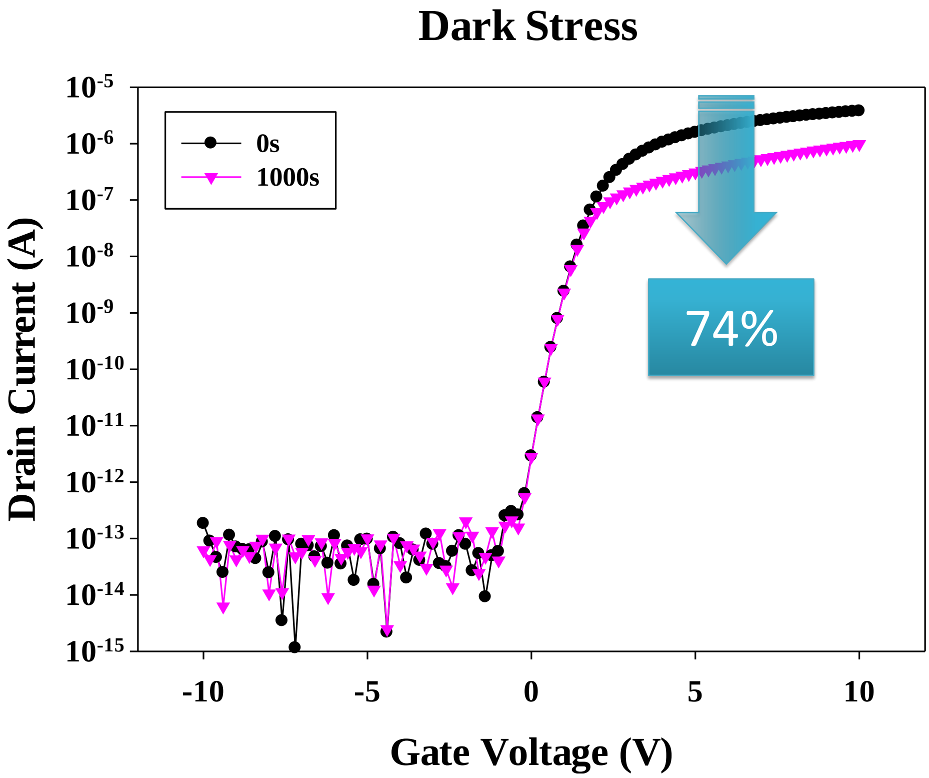


Fig.4.1.2 The I_D-V_G of TFTs in linear region after darkness stress.

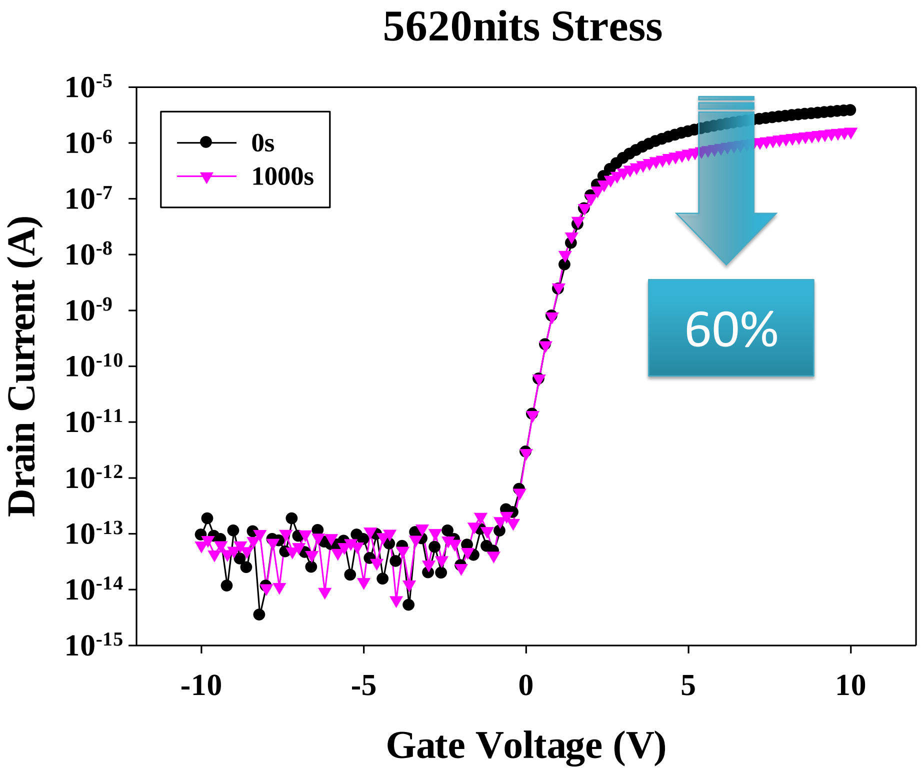


Fig.4.1.3 The I_D-V_G of TFTs in linear region after illumination stress.

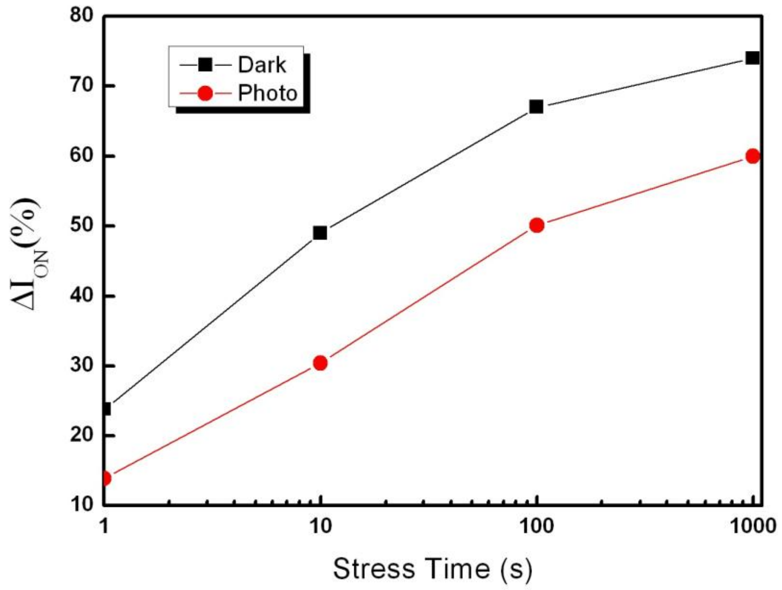


Fig.4.1.4 The on current variation in dark stress and light stress.

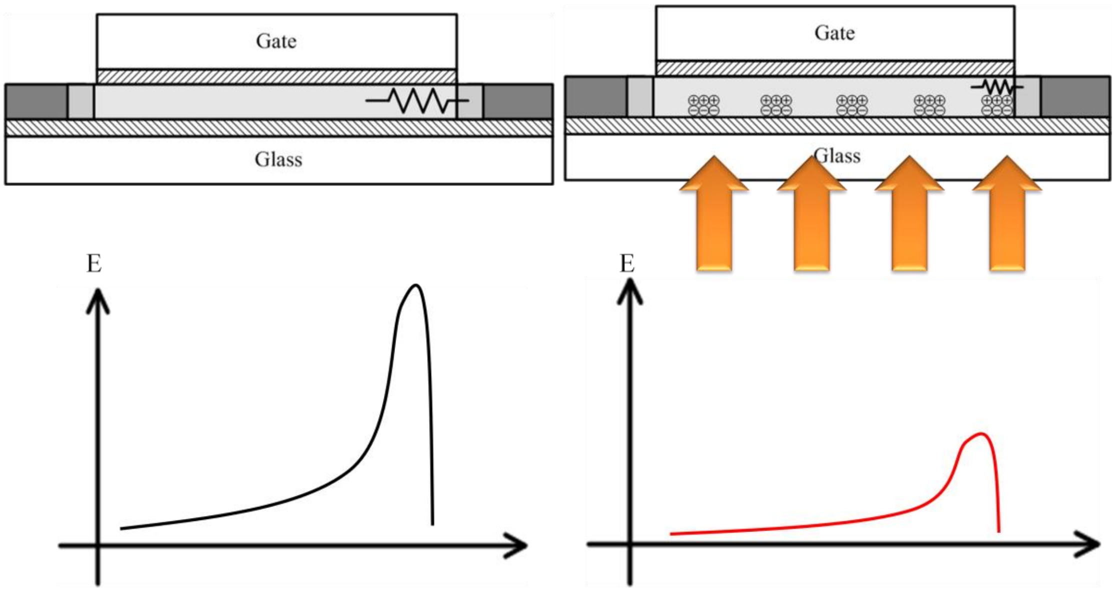


Fig.4.1.5 Our proposed model as high drain voltage and small gate voltage are applied.

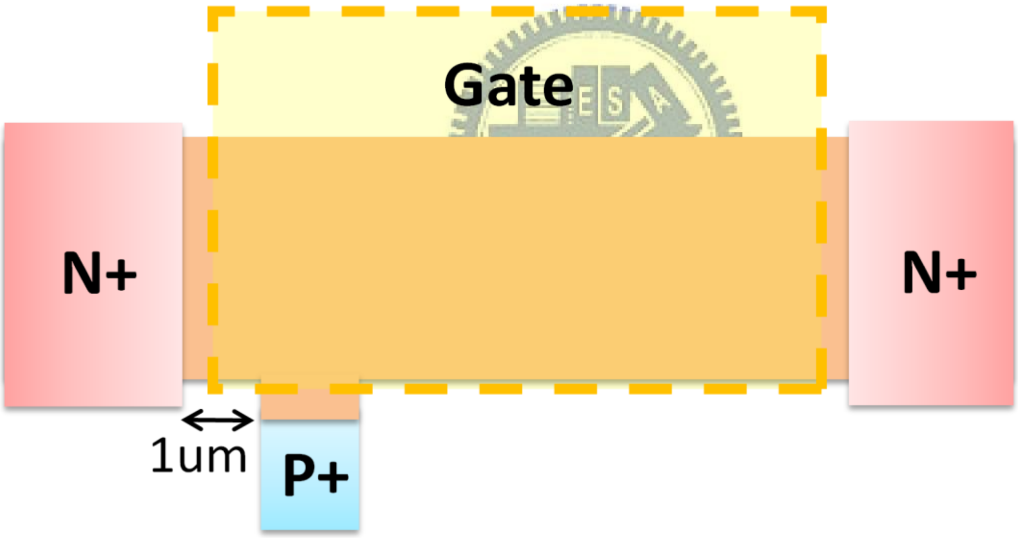


Fig4.1.6 Poly-Si TFT with lateral body thermal (LBT).

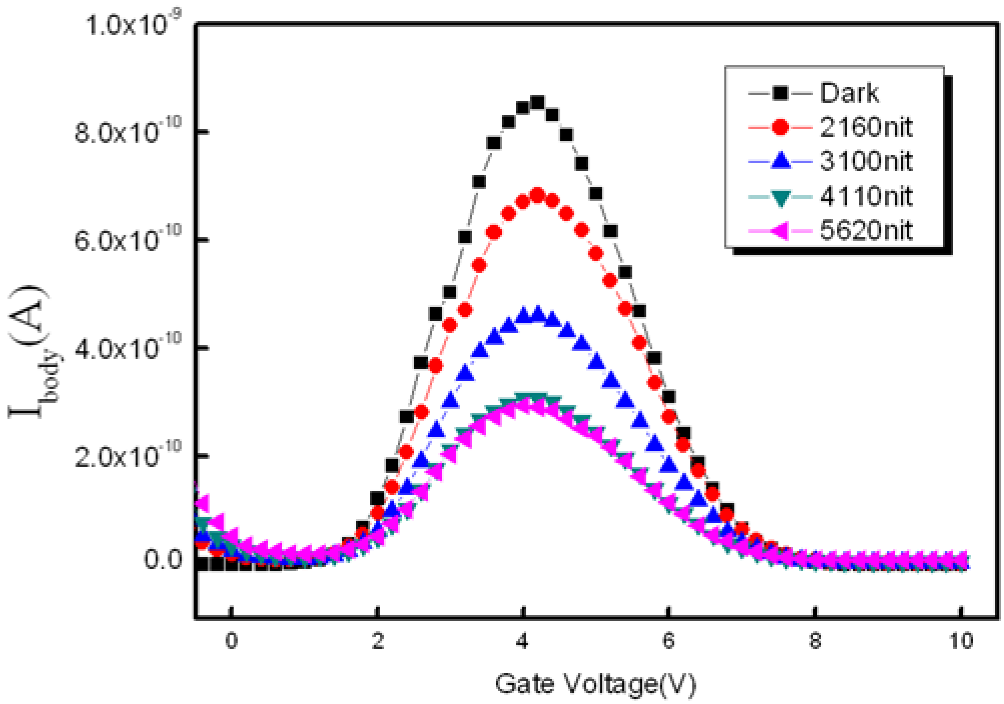


Fig.4.1.7 The I_{body}-V_G relationships of LBT poly-Si TFTs with the increasing brightness of back-light.

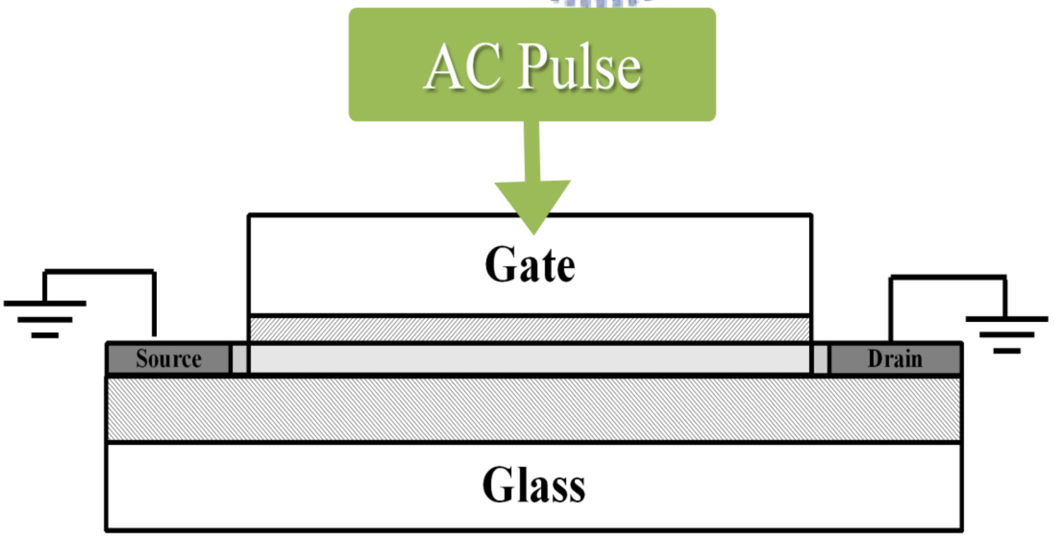


Fig.4.2.1 The gate electrode applies a AC pulse voltage, and source and drain is grounded.

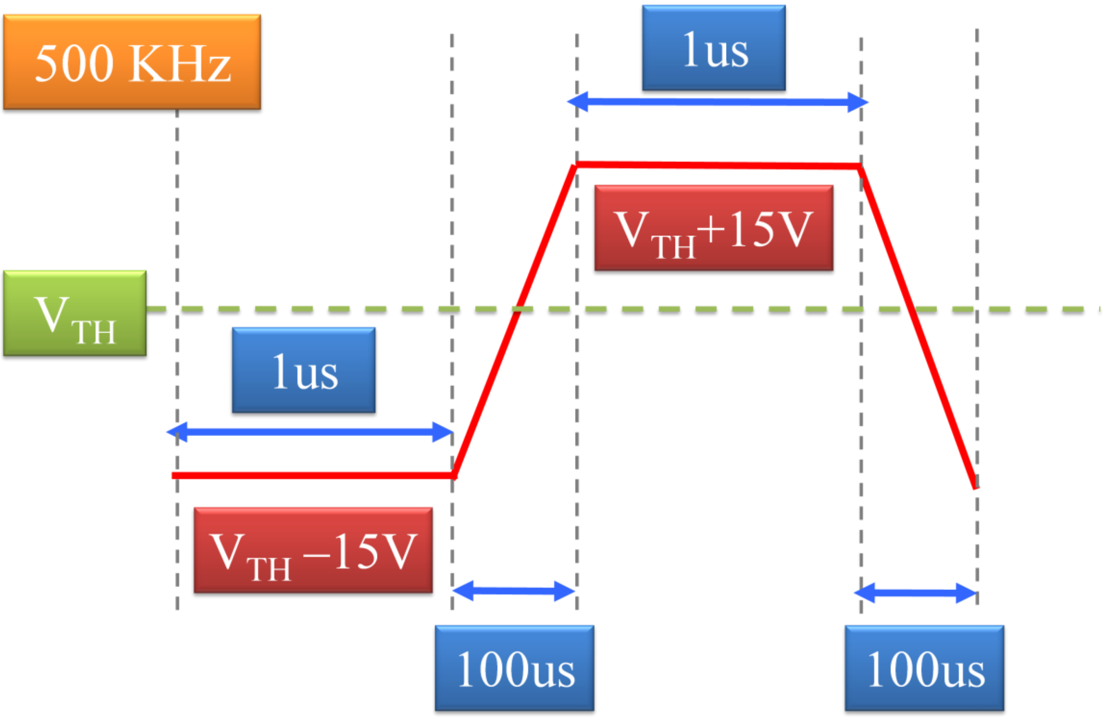


Fig.4.2.2 The waveform of the AC signal.

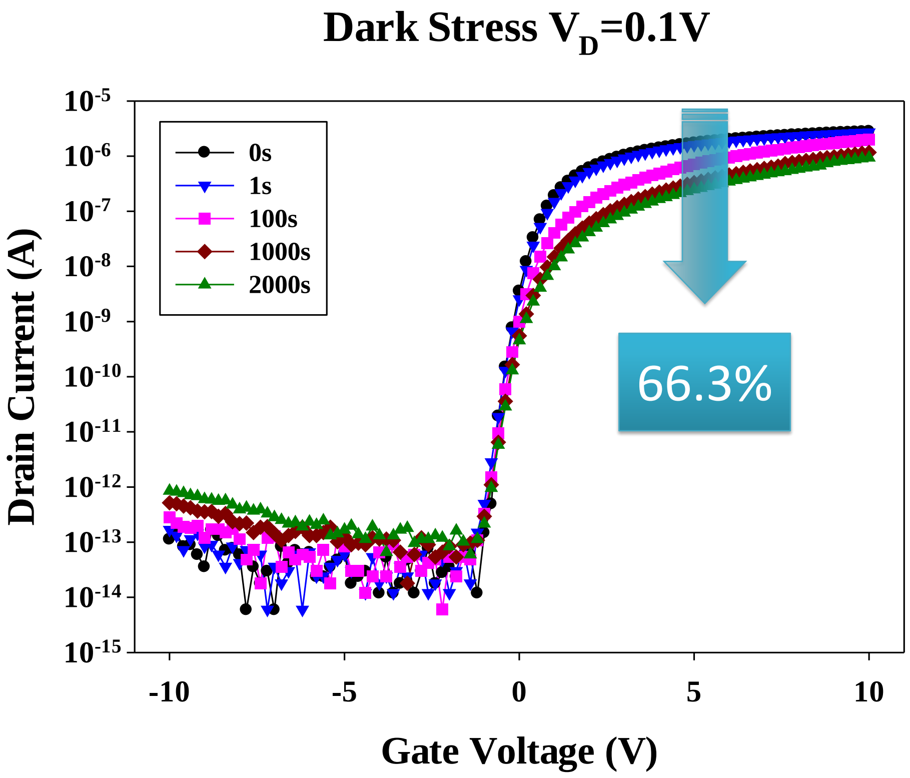


Fig.4.2.3 The I_D-V_G of TFTs in linear region after darkness stress.

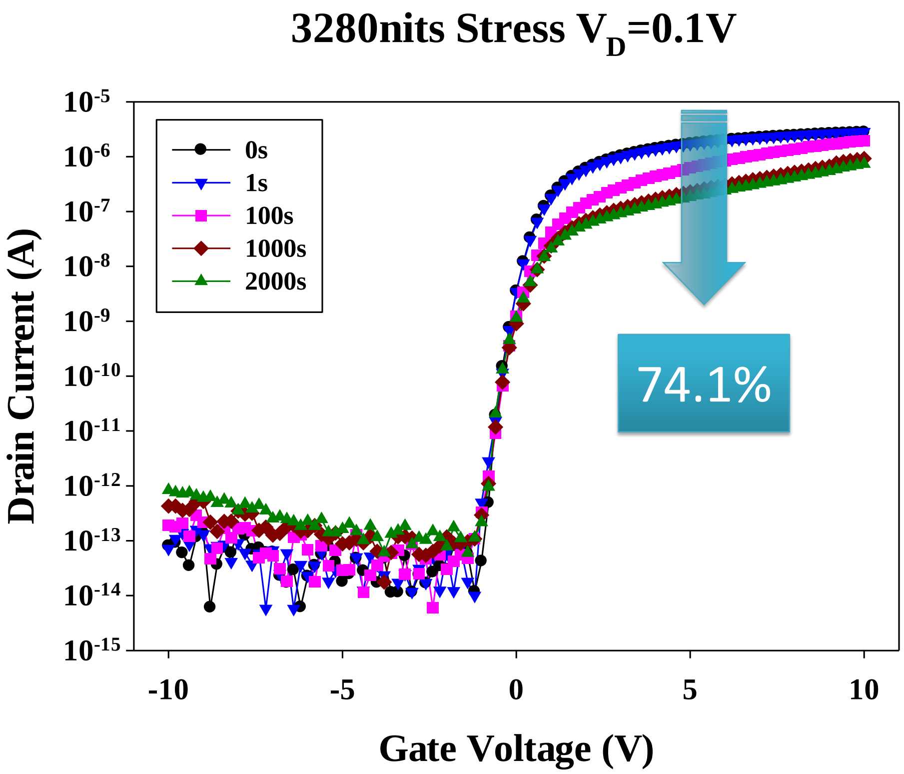


Fig.4.2.4 The I_D-V_G of TFTs in linear region after illumination stress.

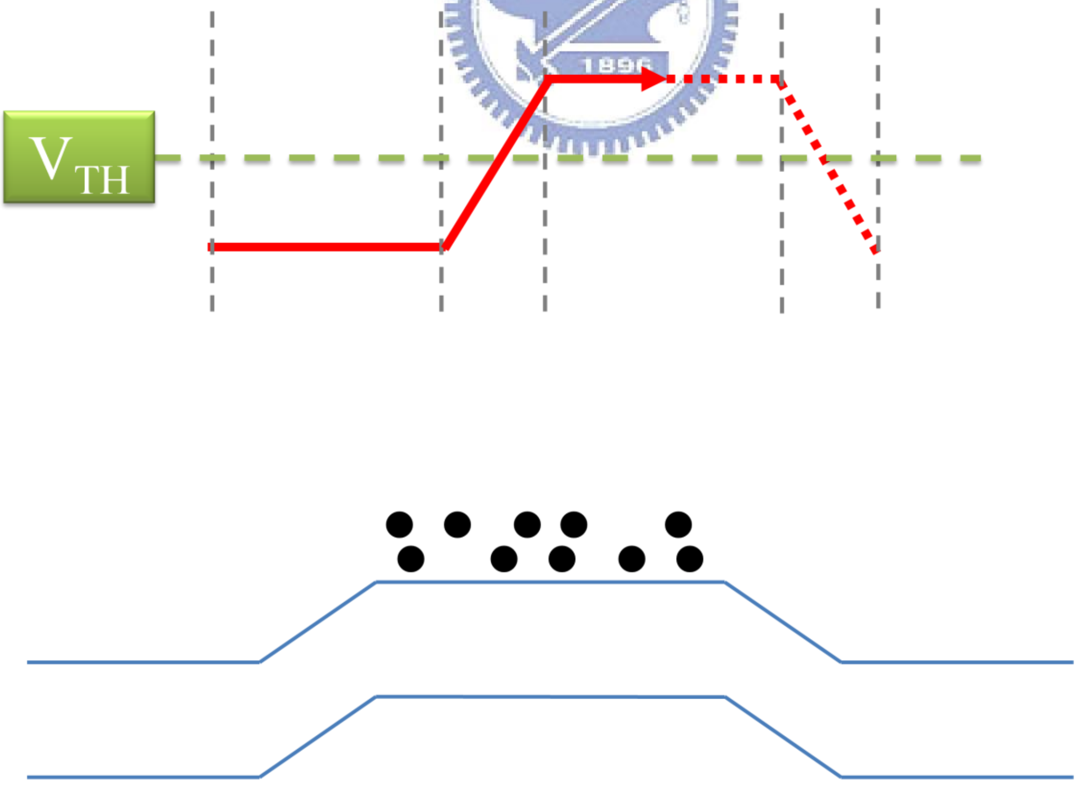


Fig.4.2.5 When a high voltage is applied to the gate, the device turns on and is operating in ON state. The electrons gather to form a channel.

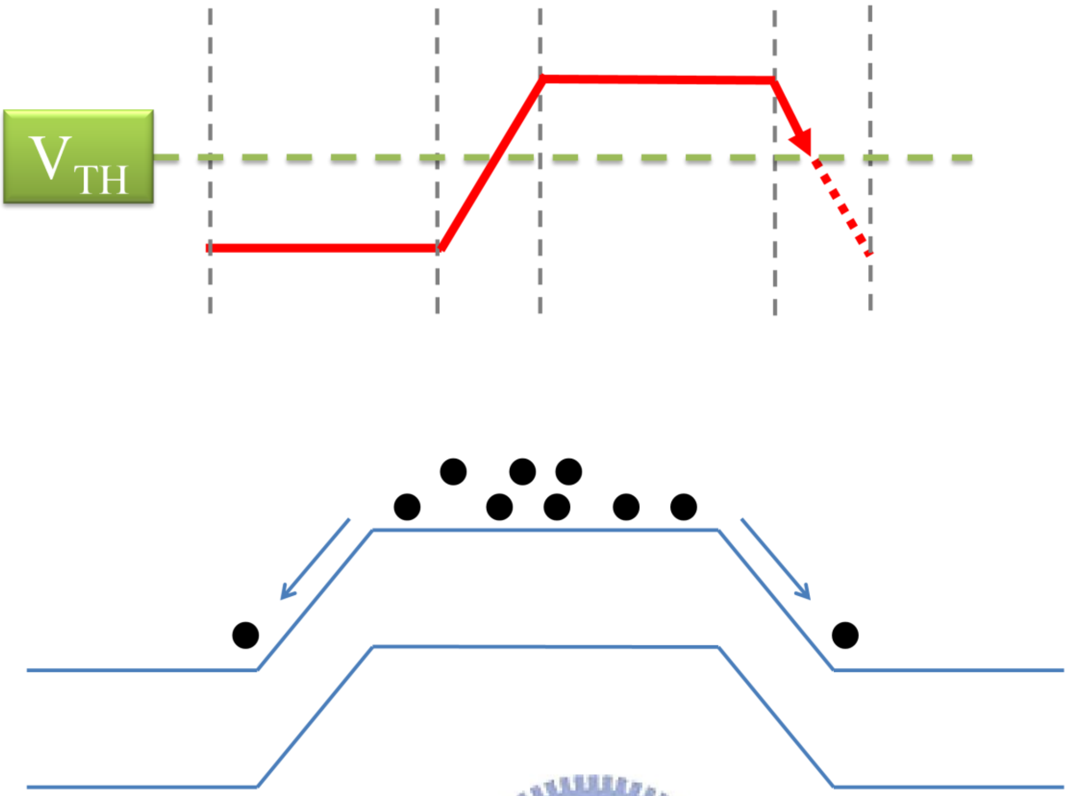


Fig.4.2.6 When the gate voltage drops, the electrons in the channel move rapidly to the source and drain.

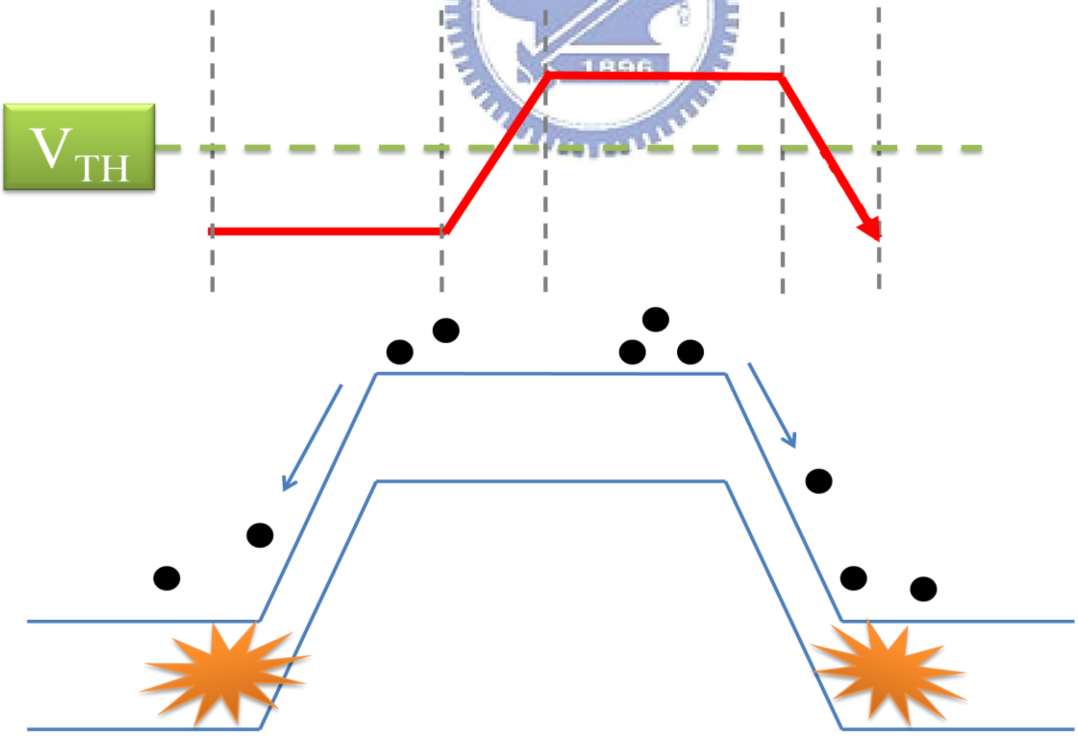


Fig.4.2.7 Some of the trapped electrons are exposed to the high electric field and grain energy from the field. The density of state (DOS) in tail edge of poly-Si is increased by the hot electrons.

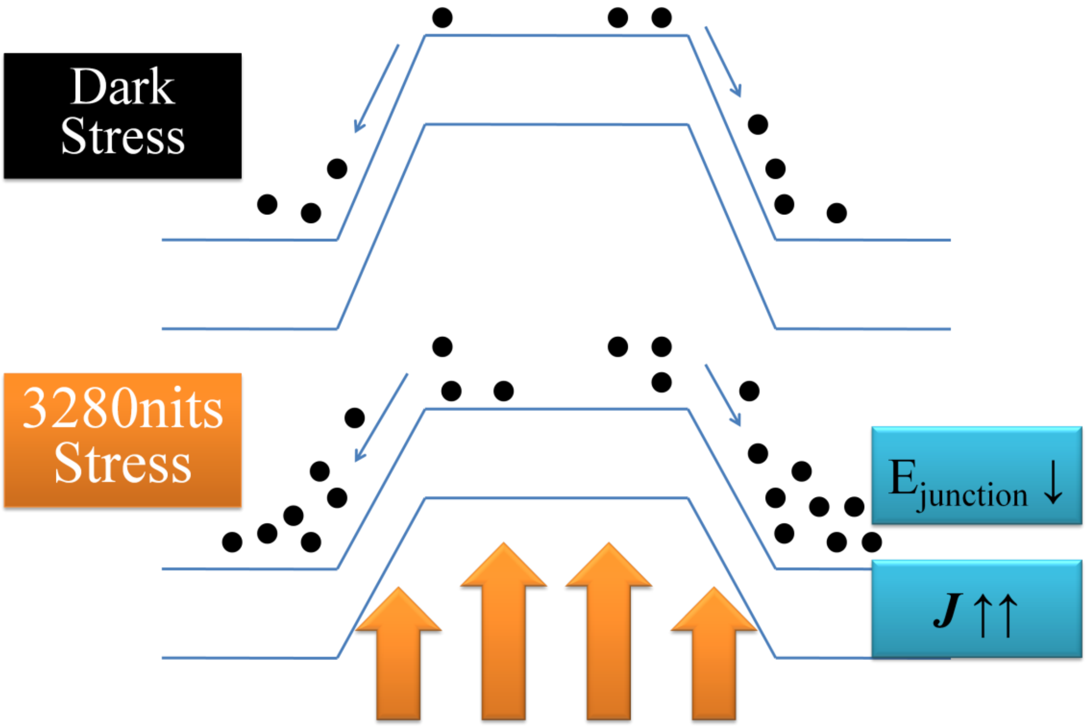


Fig.4.2.8 shows the comparison of dark Stress and illumination stress.

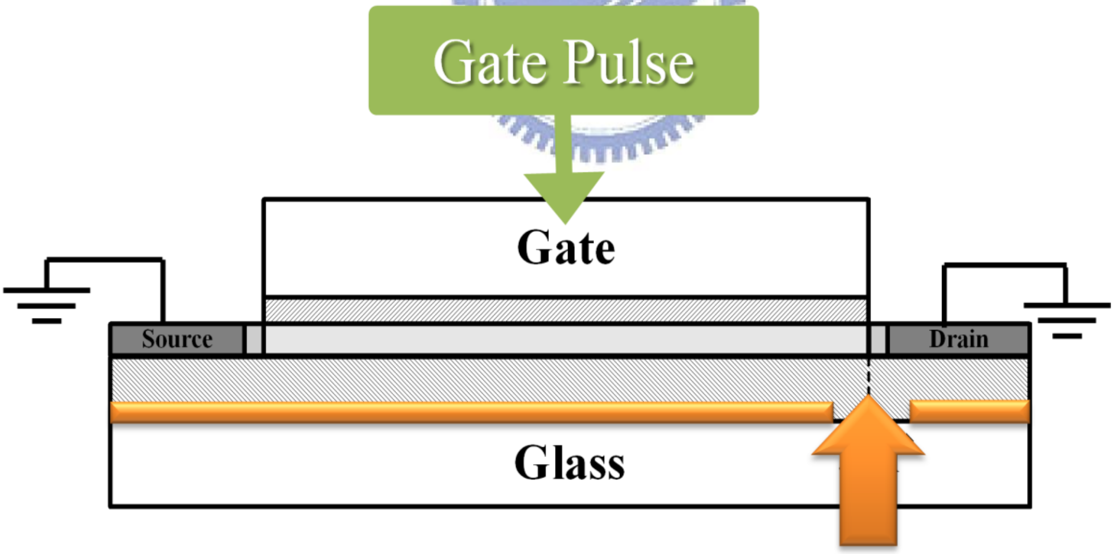


Fig.4.3.1 The poly-Si TFT with a split metal shielding layer. The gate electrode applies a AC pulse voltage, and source and drain is grounded.

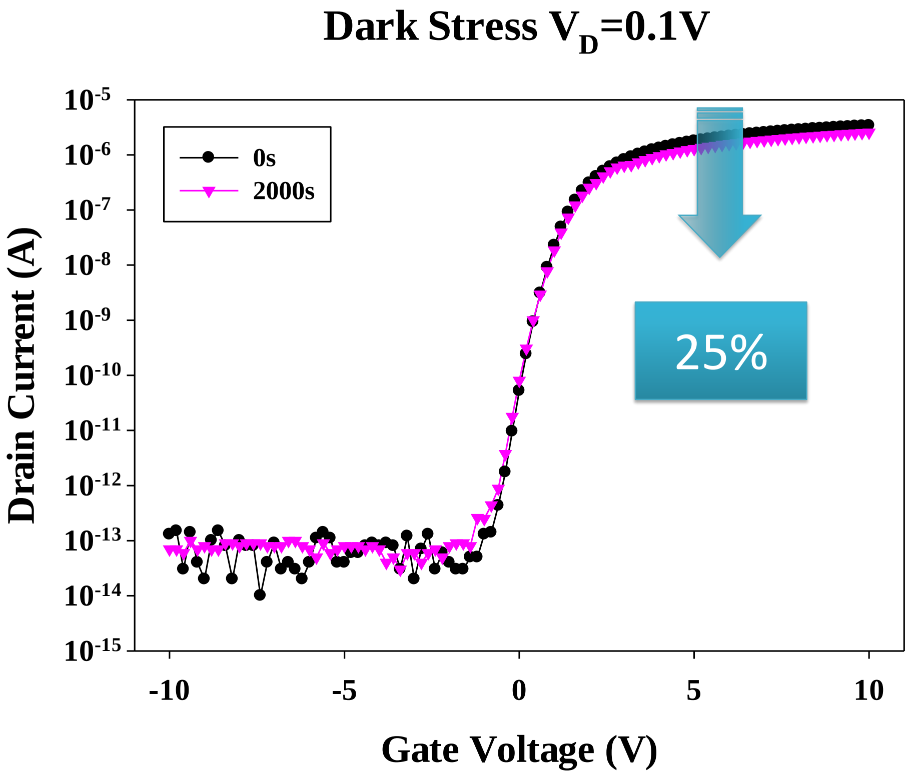


Fig.4.3.2 The I_D-V_G of TFTs in linear region after darkness stress.

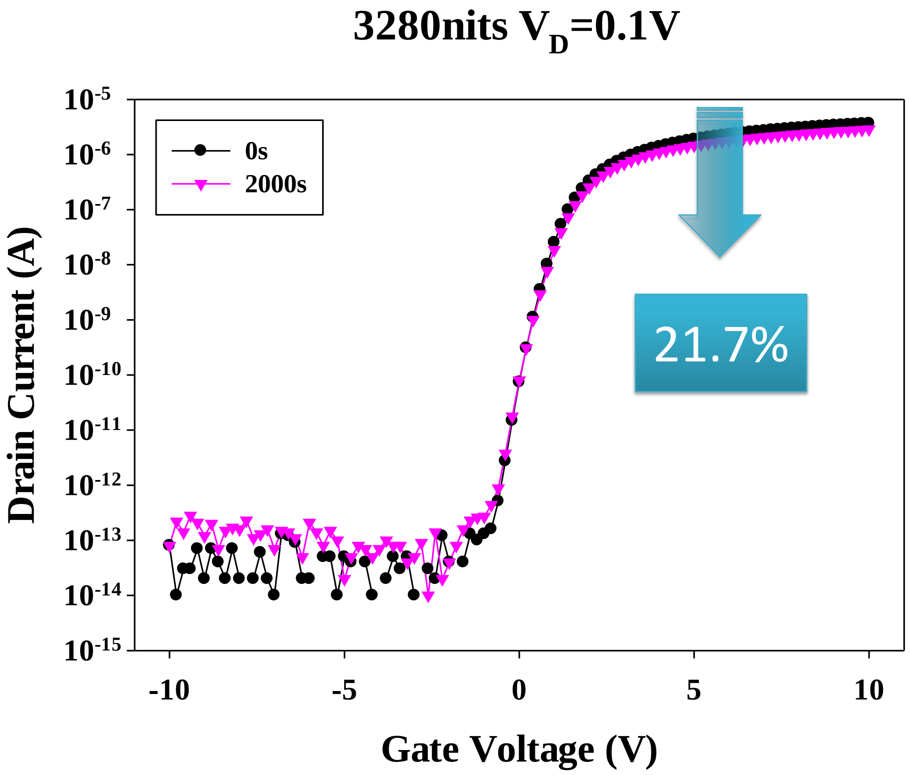


Fig.4.3.3 The I_D-V_G of TFTs in linear region after illumination stress.

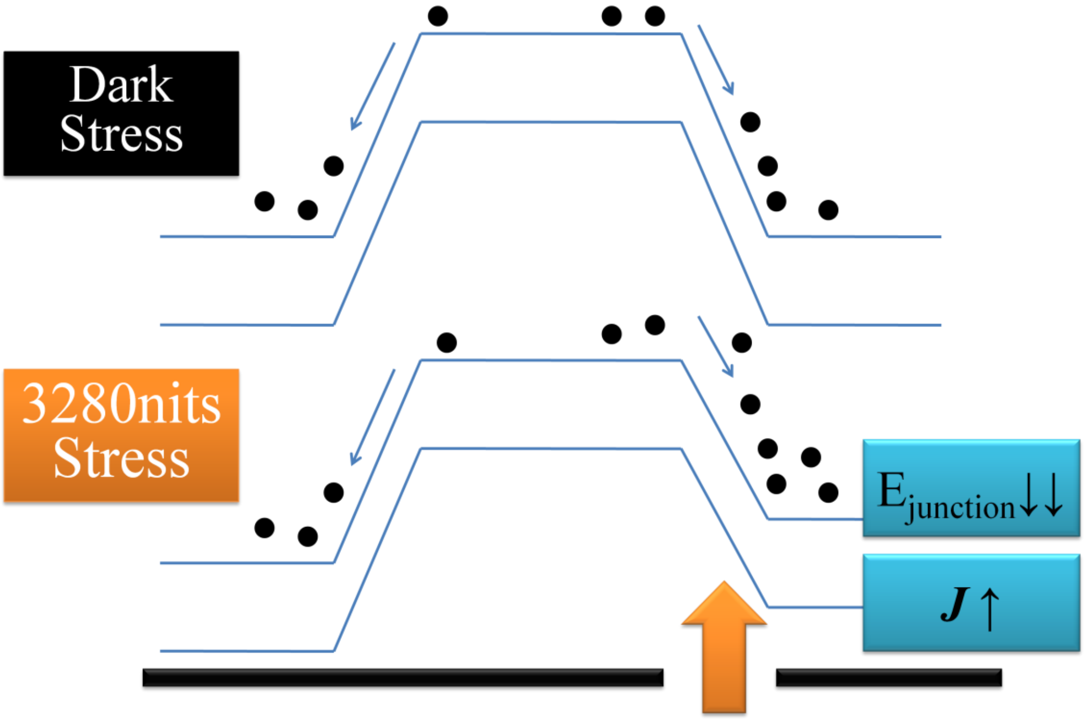


Fig.4.3.4 The band diagram of dark Stress and illumination stress.

Tables

Table.1 The comparison of the threshold voltage shift for different structure TFTs.

	V_{TH} (V) V_D=0.1V	V_{TH} (V) V_D=15V	V_{TH} Shift (V)
Full Shielding	0.738	-1.038	1.776
M1	0.917	0.211	0.706
M2	0.952	0.454	0.498
M3	0.949	0.580	0.369
M4	0.953	0.654	0.299
M5	0.936	0.645	0.291

Table.2 The comparison of the variation of sub-threshold swing for different TFTs under illumination.

ΔSS (%)	Forward V_D=0.1V	Forward V_D=9V	Reverse V_D=0.1V	Reverse V_D=9V
2160nits	8.62	3.12	7.96	36.04
3100nits	11.50	7.32	7.96	42.45
4110nits	13.51	10.00	9.91	46.60
5620nits	14.55	12.82	12.96	54.08

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碩士論文題目:

低溫複晶矽薄膜電晶體於背光下之電性研究

Study on Electrical Characteristic of Low Temperature Polycrystalline Silicon Thin Film Transistors under Illumination