A 2.5-V 14-bit, 180-mW Cascaded $\Sigma\Delta$ ADC for ADSL2+ Application

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***Abstract*—This paper presents a sigma-delta ($\Sigma\Delta$) analog-to-digital converter (ADC) for the extended bandwidth asymmetric digital subscriber line application. The core of the ADC is a cascaded 2-1-1 $\Sigma\Delta$ modulator that employs a resonator-based topology in the first stage, three tri-level quantizers, and two different pairs of reference voltages. As shown in the experimental result, for a 2.2-MHz signal bandwidth, the ADC achieves a dynamic range of 86 dB and a peak signal-to-noise and distortion ratio of 78 dB with an oversampling ratio of 16. It is implemented in a 0.25-μm CMOS technology, in a 2.8 mm^2 active area including decimation filter and reference voltage buffers, and dissipates 180 mW from a 2.5-V power supply.**

***Index Terms*—Analog-to-digital conversion, asymmetric digital subscriber line (ADSL), multistage, resonator-based topology, sigma-delta $\Sigma\Delta$ modulation.**

I. Introduction

THE asymmetric digital subscriber line (ADSL) has become emerging technology for high-speed wireline networking. The front-end receivers demand low-cost, low-power, high-performance analog-to-digital converters (ADCs). The newly released ADSL standard ADSL2+ requires an ADC to have a 14-bit dynamic range and 2.2-MHz signal bandwidth. How to choose the ADC architecture for optimizing the tradeoff among power, resolution, and bandwidth becomes a key issue. Thus, this paper presents a sigma-delta $(\Sigma\Delta)$ ADC applying three architectural approaches for the core modulator to achieve a good tradeoff for ADSL2+ application.

Pipelined and $\Sigma\Delta$ converters, among the existing ADC architectures, are the most suitable candidates to meet the requirements of ADSL2+. Generally speaking, pipeline ADCs can achieve wide bandwidth, but have limited dynamic range, high power dissipation, and large silicon area. On the other hand, the state-of-the-art $\Sigma\Delta$ ADCs can achieve high dynamic range and high bandwidth with noise shaping and oversampling techniques. Papers [1]–[4] have presented high-order single-bit $\Sigma\Delta$ modulators for ADSL application (of approximately 1.1-MHz signal bandwith) by using a high oversampling ratio (OSR). In order to reduce the OSR while maintaining a desired dynamic range for ADSL2+ application, several papers [5]–[8] have presented $\Sigma\Delta$ modulators with high-order multibit topologies. Their signal bandwidth can be up to 2 MHz when the resolutions are above 13 bits and the OSRs range from 8 to 16. Although their designs meet the requirements of ADSL2+, they require data-weighted averaging (DWA) algorithms to solve the nonlinear problem of multibit digital-to-analog converters (DACs). The DWA circuits usually consume extra power (30–40 mW with 2.5-V supply) [7], [8] and cost additional silicon area. The work in [9], instead of using a DWA, uses the cascaded architecture with the single-bit quantizer in the first stage to relieve the linearity requirement of feedback DACs. To improve the dynamic range, they further employed a multibit quantizer in the last stage. However, the leakage quantization noise and less aggressive noise shaping practically of such cascaded architecture limit the achievable dynamic range. Therefore, how to make the tradeoffs among power consumption, resolution, and bandwidth becomes an important issue in the design of $\Sigma\Delta$ modulators.

To achieve the optimal tradeoff among power dissipation, resolution, and bandwidth for ADSL2+ application, this paper applies three architectural approaches for the cascaded architecture. Our goal is to improve the cascaded architecture in terms of dynamic range and power dissipation while keeping the active area low. First of all, the structure of the proposed modulator is 2-1-1 cascaded architecture. The first stage employs a resonator-based topology. The resonator-based topology adds in-band zeros in the noise transfer function (NTF) and, hence, suppresses the quantization noise over the signal band. The suppression of the quantization noise can effectively improve the dynamic range for low-OSR modulator [10]. Furthermore, by adding an input feedforward path into the first stage, the swing ranges and distortions of integrator outputs are reduced [11], [12]. This arrangement allows us to apply low-voltage supplies for the proposed $\Sigma\Delta$ modulator and save the power consumption. The second approach is to use a tri-level quantizer in each stage. The tri-level quantizers make the proposed modulator need no additional calibration algorithms for solving the nonlinear problem of DACs. The extra calibration circuit is costly and power-consuming. Finally, we employed two different pairs of reference voltages for comparators and DACs to enhance the achievable dynamic range; a pair of ± 0.9V is used in the first stage, and another pair of ± 0.45V is used in the succeeded stages.

A functioned ADC chip for ADSL2+ has been realized in 0.25-μm CMOS technology using the proposed modulator. To produce the Nyquist-rate signal, following the $\Sigma\Delta$ modulator, we designed a three-stage digital decimation filter. The decimation filter consists of a fifth-order comb filter, a 31-tap FIR filter, and a fourth-order IIR filter. As shown in the experimental results, the ADC, for a 2.2-MHz signal bandwidth, can achieve a

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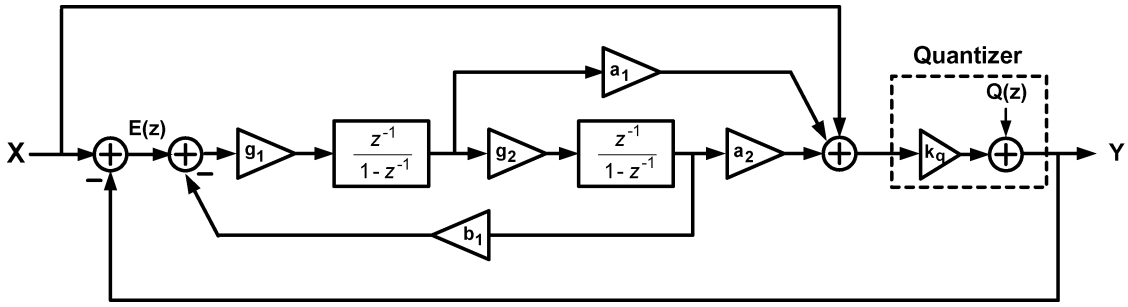

Fig. 1. Resonator-based second-order tri-level modulator.

dynamic range of 86 dB and a peak signal-to-noise and distortion ratio (SNDR) of 78 dB. It costs an active area of 2.8 mm^2 and consumes 180 mW from a 2.5-V supply voltage.

This paper is organized as follows. Section II describes the system-level design and architectural decisions of the proposed ADC with nonideality analysis. Section III provides circuit details for the implementation of the proposed modulator. Section IV reports the measured results of the fabricated chip. Finally, Section VI concludes our work in terms of chip features.

II. Architectural Consideration

The cascaded architecture has been widely used for low OSR modulator to solve the stability problem of high-order modulation. In this paper, we adopt the cascaded 2-1-1 to design the proposed modulator for two reasons. First, in practical, the $\Sigma\Delta$ modulator will approach the limitation of performance when the order is higher than four [10]. The fifth or higher order $\Sigma\Delta$ modulators will not provide significant improvement than the fourth-order $\Sigma\Delta$ modulator. Second, the paper [13] presents an in-depth study on comparison of 2-1-1 and 2-2 architectures and shows that the 2-1-1 architecture practically outperforms the 2-2 one for low OSR design.

As mentioned in Section I, the design of cascaded architecture requires tradeoffs among power dissipation, resolution, and bandwidth. When making the tradeoffs, there exist several architectural decisions to be made in the design of the cascaded modulator. The following subsections will describe the architectural considerations of our study.

A. Topology Design of the First Stage

Since the first stage processes the input signal and generates the quantization noise to the succeeding stages, the performance of the entire modulator is bounded by behaviors of the first-stage topology, such as noise-shaping capability, linearity, and tone behavior. To design a high-dynamic-range, low-power $\Sigma\Delta$ modulator for ADSL2+ application, a resonator-based second-order modulator is used in the first stage, as shown in Fig. 1. It uses a low-Q resonator-based loop filter that introduces a pair of zeros into noise transfer function (NTF). The NTF of the resonator-based modulator can be expressed as

$$\mathrm{NTF}(z) = \frac{1 - 2z^{-1} + (1+r)z^{-2}}{1 - (2 - k_q c)z^{-1} + (1 + r + k_q d - k_q c)z^{-2}} \tag{1}$$

where $c = g_1 a_1$, $d = g_1 g_2 a_2$, and $r = g_1 g_2 b_1$. Note that r is the loop gain of the resonator and k_q is the gain of the quantizer. The zeros of NTF create a notch around the edge of signal band and hence suppress the in-band quantization noise. The suppression can significantly improve the signal-to-noise ratio (SNR) of modulators, especially for a low OSR modulator [10]. The feedforward path from input to the adder followed by the quantizer is used to reduce the distortion caused by integrator nonidealities [12]. The following equation shows the signal transfer function (STF) induced by the feedforward path:

$$\mathrm{STF}(z) = \frac{k_q\left[1 - (2-d)z^{-1} + (1 + r + c - d)z^{-2}\right]}{1 - (2 - k_q d)z^{-1} + (1 + r + k_q c - k_q d)z^{-2}}. \tag{2}$$

Based on (2), the error signal $E(z)(= X(z) - Y(z))$ becomes

$$\begin{aligned} E(z) &= [1 - \mathrm{STF}(z)]\,X(z) - \mathrm{NTF}(z)Q(z) \\ &= (1 - k_q)\mathrm{NTF}(z)X(z) - \mathrm{NTF}(z)Q(z). \end{aligned} \tag{3}$$

In (3), the term $(1 - k_q)$ can be treated as the impact factor of $X(z)$ to $E(z)$. Obviously, the smaller the impact factor is, the less sensitive the loop filter is to the input signal. When k_q is a unity, the $E(z)$ does not have the component $X(z)$ and the integrators of the loop filter will only process the quantization noise $Q(z)$. In this case, the distortion caused by integrator nonidealities can be significantly reduced [11]. Unfortunately, k_q cannot be a unity in practical design because there always exists quantization error between the input and output of a quantizer. In the case of using the single-bit quantizer, k_q varies with the input signal of the quantizer, and its value can be much greater than unity. The variation of k_q causes the sensitivity of the loop filter to the input signal to be high. To take advantage of making k_q unity, one can use the multibit quantizer to lower the sensitivity as much as possible [12]. Nevertheless, when using the multibit quantizer, the modulator requires the data-weighted averaging (DWA) algorithm to compensate for the nonlinearity of the multibit DAC. Here we replace multibit quantizer with a tri-level one in that the k_q variation of tri-level quantizer can be reduced and the performance is improved as compared with a single-bit quantizer. Although the tri-level DAC introduces distortion, the 14-bit linearity can be achieved by careful sizing of the transistors composing the OTA and symmetrical layout without using the DWA circuitry. The next subsection will detail the design of the tri-level quantizer.

B. Analysis of Tri-Level Quantization

The tri-level quantization technique has been proved to be able to achieve high dynamic range without using DWA circuitry [14]. In our work, the use of tri-level quantization is twofold: 1) to keep the impact factor of $X(z)$ to $E(z)$ lower than that of the single-bit quantizer so the performance can meet the requirement of ADSL applications and 2) to have the nonlinearity of the feedback DAC lower than multibit quantizers so that the DWA is not a necessity for high dynamic range. Based on (3), the input signal $X(z)$ and quantization error $Q(z)$ are the two input sources of the first integrator. Since the $Q(z)$ is assumed to be a white noise, the term $(1-k_q)\mathrm{NTF}(z)X(z)$ becomes the major distortion source of the first integrator. Thus, to reduce the harmonic distortion, the term $(1-k_q)$ has to be as small as possible. From [10], the "equivalent gain" of a quantizer is defined as

$$k_q = \frac{rms(V_o)}{rms(V_i)} = \lim_{n\to\infty}\sqrt{\frac{\sum_{n=1}^{N} V_o^2[n]}{\sum_{n=1}^{N} V_i^2[n]}} \tag{4}$$

where V_o and V_i are the output voltage and input voltage of the quantizer, respectively. The equivalent gain can only be used to evaluate the static performance of the modulator. In order to observe the dynamic performance of distortion, we defined $k_q(n)$ as $V_o(n)/V_i(n)$ and the output voltage of the tri-level quantizer as

$$V_o(n) = \left\{ \begin{array}{c} V_{\mathrm{cm}} + V_r, \quad \text{if } V_i \geq V_{\mathrm{cm}} + V_{\mathrm{th}} \\ V_{\mathrm{cm}}, \quad \text{if } V_{\mathrm{cm}} + V_{\mathrm{th}} > V_i > V_{\mathrm{cm}} - V_{\mathrm{th}} \\ V_{\mathrm{cm}} - V_R, \quad \text{if } V_i \leq V_{\mathrm{cm}} - V_{\mathrm{th}} \end{array} \right\} \tag{5}$$

where V_{cm} and V_{th} are the common-mode voltage and threshold voltage of the quantizer, respectively. Here, we calculate the k_q for both tri-level and two-level quantizers by considering practical design conditions. If the voltage set $[V_{\mathrm{cm}}, V_r, V_{\mathrm{cm}}]$ is equal to [1.25 V, 1 V, 0.35 V], Fig. 2 plots k_q versus input voltage for both tri-level and two-level quantizers. As shown in the plot, the variation of $(1-k_q)$ of the tri-level quantizer is narrower than that of the single-bit quantizer. Hence, the use of a tri-level quantizer can lower the sensitivity of the loop filter to the input signal.

To see if the tri-level quantizer is sufficient for the ADSL2+, we applied single-bit and tri-level quantizers for the resonator-based modulator and observed the third harmonic distortion. Considering a nonideal integrator with finite unity gain frequency (GBW), the output voltage of the integrator is given by

$$v_o(t) = v_o(nT_s - T_s) + V_s\left(1 - e^{-\frac{t}{\tau}}\right), \quad 0 < t < \frac{T_s}{2} \tag{6}$$

where $V_s = V_{\mathrm{in}}(nT_s - T_s)$ and $\tau = 1/(2\pi\mathrm{GBW})$. With a finite GBW, the incomplete settling causes the harmonic distortion in the integrator outputs. Given $V_{\mathrm{th}} = 0.45$ V, OSR $= 16$, $f_s = 70.4$ MHz, and GBW $= 240$ MHz, we employed sinusoids with -6 dB and 500 kHz as the input signals to simulate the output harmonic distortion of the first integrator. Fig. 3 shows an illustration of the third-harmonic distortion results for the first integrator with tri-level and single-bit quantizers. As shown in Fig. 3, the third-harmonic distortion of a resonator-based modulator with tri-level quantizer is lower than -90 dB and, hence, its linearity can be greater than 90 dB. Compared with the single-bit version, the use of a tri-level quantizer lowers the sensitivity of the loop filter to the input signal and consequently reduces the distortion caused by integrator setting error. Furthermore, the linearity of 90 dB is higher than the requirement of a 14-bit ADC (e.g., 86 dB), so it is possible for us to make the overall ADC achieve 14-bit resolution without using a DWA.

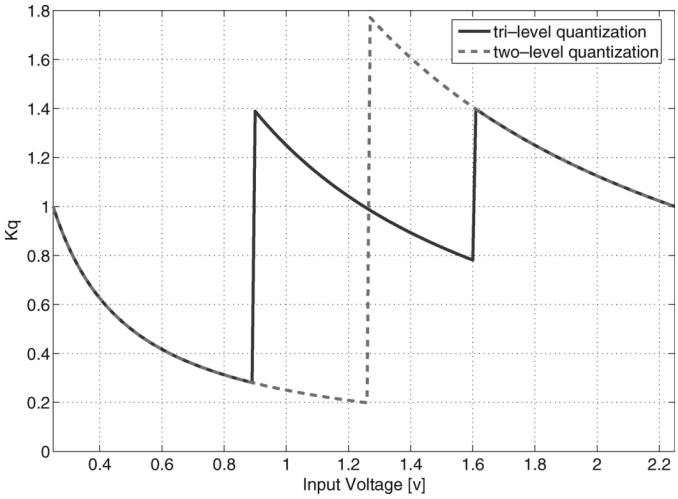

Fig. 2. Nonlinear gain of tri-level and two-level quantizers.

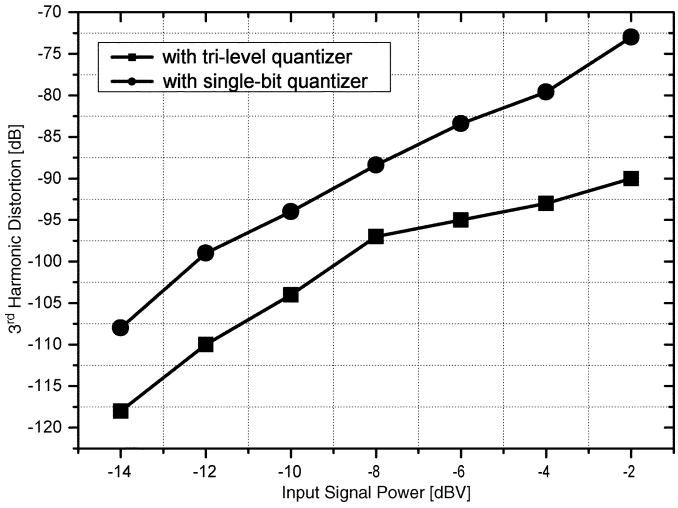

Fig. 3. Simulated third-harmonic distortion of a resonator-based modulator with tri-level and single-bit quantizers. ($V_{\mathrm{th}} = 0.45$ V, fin $= 500$ kHz, OSR $= 16$, fs $= 70.4$ MHz).

C. Design of Resonator-Based MASH 2-1-1

Fig. 4 illustrates the block diagram of a resonator-based cascaded modulator, which is referred to as RMASH 2-1-$1_{1.5\mathrm{b}}$. The first stage, as mentioned above, uses the resonator-based 1.5-bit modulator, and the following two stages are the first-order 1.5-bit modulators. With digital error cancellation logic (ECL), the NTF of theoretical quantization noise (TQN) of the RMASH 2-1-$1_{1.5\mathrm{b}}$ is given by

$$\mathrm{NTF}_{\mathrm{TQN}}(z) = d_2\left[1 - 2z^{-1} + (1+r)z^{-2}\right] \cdot (1 - z^{-1})^2 Q_3(z) \tag{7}$$

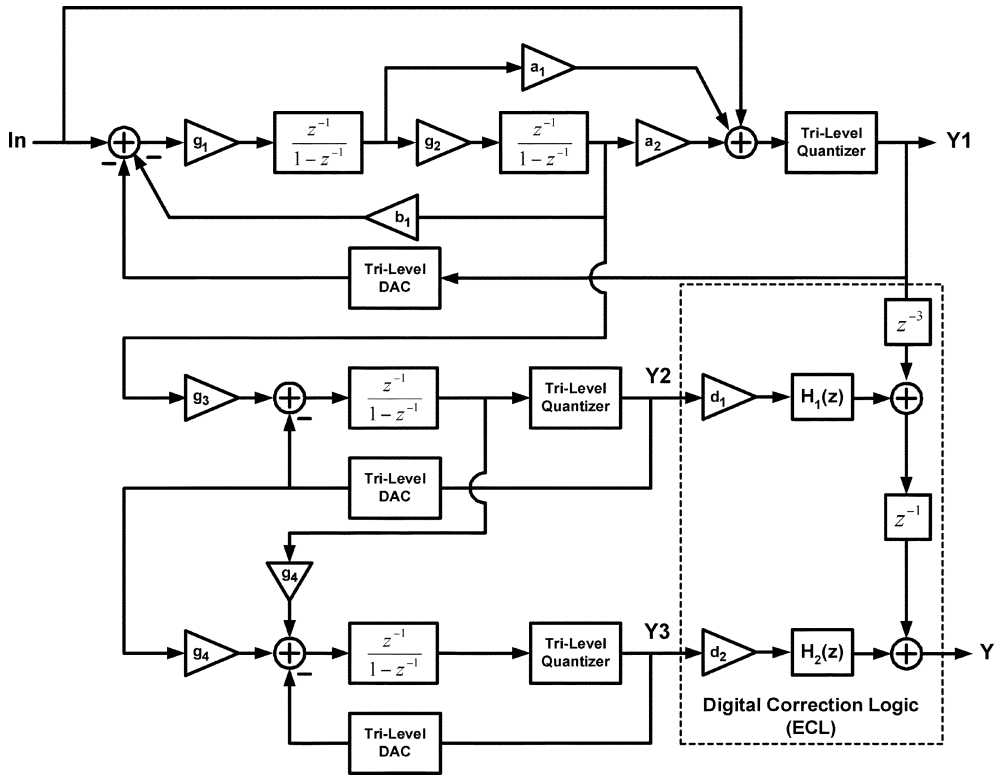

Fig. 4. Block diagram of RMASH 2-1-$1_{1.5b}$.

where $Q_3(z)$ is the quantization noise of the tri-level quantizer in the third stage and d_2 is the inverse of $g_1g_2g_3g_4$. Obviously, the $\mathrm{NTF_{TQN}}$ can be improved by tuning parameters, $d2$, r, and $Q3(z)$. With the careful selection of the resonator loop gain r, the NTF zeros can produce a notch near the edge of the signal band to suppress the quantization noise over the desired signal band. According to [15], the NTF zeros are placed at the corner frequency of the signal band, and the value of r can be chosen by the following expression:

$$r = g_1 g_2 b_1 \approx [2\pi \cdot (f_{\mathrm{notch}}/f_s)]^2 . \tag{8}$$

At an OSR of 16, with in-band zeros, the fourth-order NTF can improve the SNDR by 14 dB.

Furthermore, we applied two pairs of reference voltages (TPRVs) for the proposed modulator: a pair of $\pm$0.9V for the tri-level quantizer of the first stage and another pair of $\pm$0.45V for the quantizers in the second and third stages. The high-voltage pair can have the first stage operating at high dynamic range while the low-voltage pairs can reduce the output swing of the second stage and the power of Q_3. The reason why we tried to reduce the output swing of the second stage is because the reduction implies the scaling of g_3 and the SNDR can be improved by reducing d_2.

Given the OSR of 16 and the d_2 of 2, Fig. 5 shows the NTFs of the proposed RMASH 2-1-$1_{1.5b}$ with TPRVs and conventional MASH 2-1-$1_{1.5b}$ without TPRVs. We can see the performance gain of 20 dB in the shadow region. Fig. 6 illustrates the SNDR versus OSR in comparison to the modulators. The single-loop modulator with 4-bit quantizer ideally has the best SNDR; however, it usually requires additional power-consuming costly

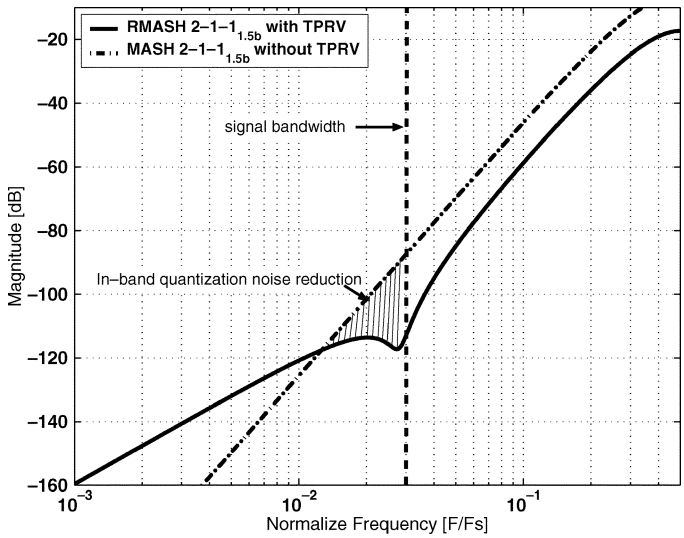

Fig. 5. TQN plots of RMASH 2-1-$1_{1.5b}$ with TPRVs and MASH 2-1-$1_{1.5b}$ without TPRVs.

DWA circuitry to improve the linearity of a multibit DAC. At an OSR of 16, the proposed RMASH 2-1-$1_{1.5b}$ has an SNDR of over 90 dB and outperforms the traditional MASH 2-1-1 with a 3-bit quantizer in the last stage.

In general, the leakage quantization noise is the major concern in the design of a cascaded $\Sigma\Delta$ modulator. The leakage quantization noise is mainly caused by the finite OTA gain and capacitor mismatching of the first-stage integrators. In the RMASH 2-1-$1_{1.5b}$, the capacitor mismatching is especially critical because the SNR improvement mainly relies on the

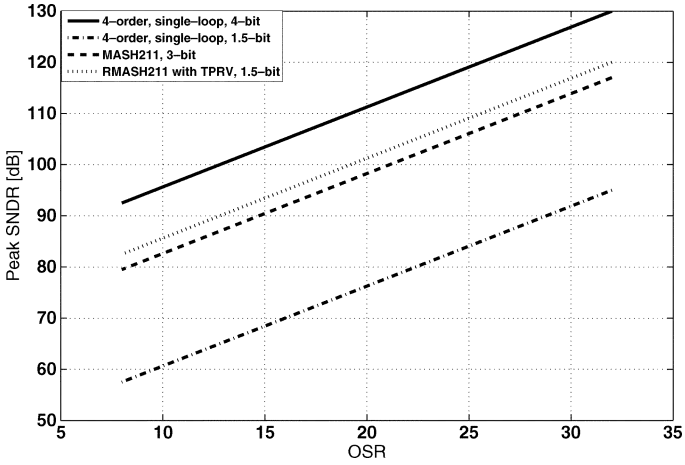

Fig. 6. Peak SNDR versus OSR plots for four different modulators.

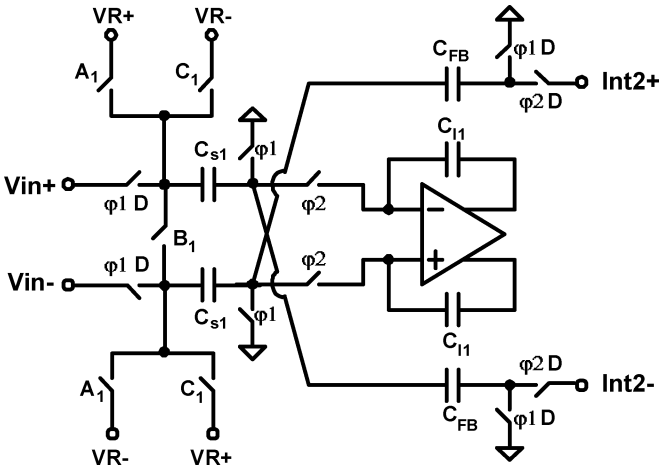

Fig. 7. Circuit implementation of the first integrator in the first stage of RMASH 2-1-$1_{1.5b}$.

in-band zeros induced by the first-stage resonator. Therefore, we have to select coefficients of the loop filter in the first stage carefully to achieve the desired SNR. Fig. 7 shows a circuit implementation of the first integrator where $g_1 = C_{S1}/C_{I1}$ and $b_1 = C_{FB}/C_{S1}$. Given the notch and sampling frequencies of 2.25 and 70.4 MHz, respectively, the resonator loop gain r, based on (8), approximates to 0.04. In order to simplify the design of the digital cancellation filters $H_1(z)$ and $H_2(z)$, we scaled the value of r to be the power of 2 (say 0.03125), which shifts the notch frequency to 2 MHz. This arrangement only degrades the theoretical SNR by 1.5 dB. In general, the g_1 and g_2 should be as large as possible to keep the thermal noise low, and thus b_1 has to be relatively small for the given r. Consequently, the difference between C_{S1} and C_{FB} may become large and cause a large ratio mismatch [16]. For instance, if $g_1 = 1$, $g_2 = 0.5$, and $C_{S1} = 1.5$ pF, b_1 and C_{FB} will be 0.0625 and 93.75 fF, respectively. The value of C_{S1} is much larger than that of C_{FB}. To reduce the mismatch of C_{S1} and C_FB, we scaled g_1 and g_2 down to 0.5 and 0.25, respectively. In this case, $b1$ and C_{FB} become 0.25 and 375 fF, respectively, and the mismatch can be reduced. Table I shows the coefficient sets of the RMASH 2-1-$1_{1.5b}$ we used in this study. As shown

TABLE I
COEFFICIENTS OF RMASH 2-1-$1_{1.5b}$ FOR OSR = 16

Coefficients	Values	Coefficients	Values
g1	0.5	b1	0.25
g2	0.25	a1	2
g3	2	a2	4
g4	2	d2	2

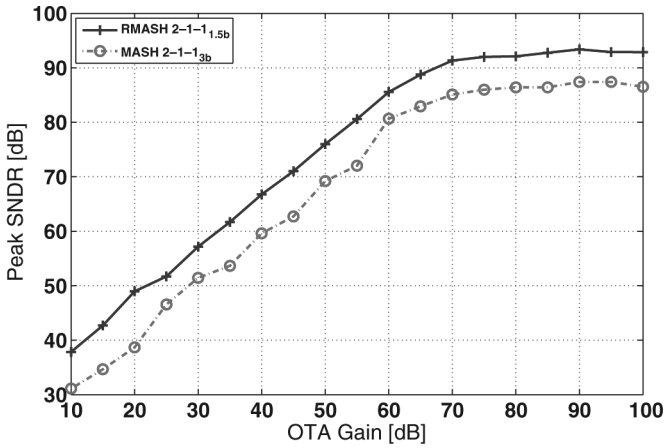

Fig. 8. Plots of simulated SNDR versus OTA dc gain. (OSR = 16).

in Fig. 8, the proposed RMASH 2-1-$1_{1.5b}$ can achieve a peak SNDR of 92 dB and a dynamic range of 95 dB, respectively.

D. Analysis of Integrator and Tri-Level DAC Nonidealities

In switched-capacitor (SC) cascaded modulators, the capacitor mismatch and finite OTA gain are two main nonidealities. These nonidealities can lead to imperfect cancellation of the first- and second-stage quantization noises at modulator output and thus degrade the performance. In addition, in the RMASH 2-1-$1_{1.5b}$, the nonlinearity of tri-level DACs can also introduce distortion to the modulator output, especially for the first-stage DAC. The work in [2] gives the practical model of a nonideal integrator for behavioral simulation to determine the minimum requirement of OTA gain. By applying their model to our simulation, Fig. 9 shows that increasing the finite OTA gain above 70 dB will not significantly improve the performance. Thus, in our study, we set the finite OTA gain to 70 dB. Given 70-dB OTA gain and 0.5% capacitor mismatching. Fig. 9 illustrates that the RMASH 2-1-$1_{1.5b}$ can achieve a peak SNR of 86 dB. Note that the sensitivity to finite OTA gain and capacitor mismatch of the RMASH 2-1-$1_{1.5b}$ is similar to that of a traditional MASH 2-1-1_{3b}. This is because the SNDR improvement relies on in-band NTF zeros and TPRVs. However, with the same OTA gain and capacitor mismatch, the RMASH 2-1-$1_{1.5b}$ still has a higher peak SNDR.

To consider the nonidealities of tri-level DACs, reference [14] has provided a good study and insight into this issue. The authors concluded that the discrete-time error-function tri-level DAC approximates a quadratic polynomial, which is expressed as

$$e_{\mathrm{DAC}}[k] \approx \frac{V_{\mathrm{OS}}}{2V_R}\left(1 + y_1[k]^2\right) \tag{9}$$

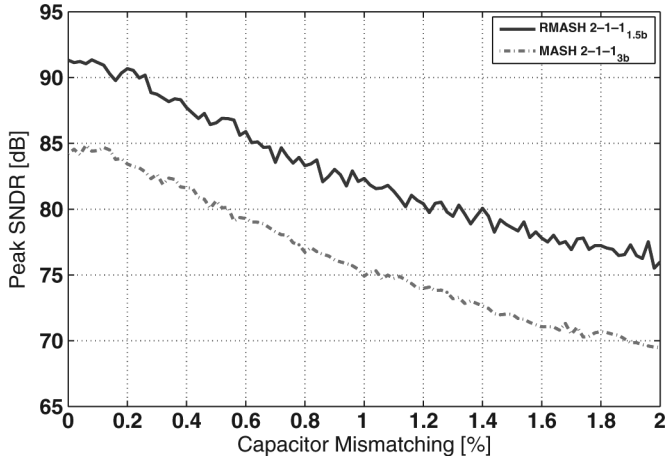

Fig. 9. Plots of simulated SNDR versus capacitor mismatch. (OSR $= 16$).

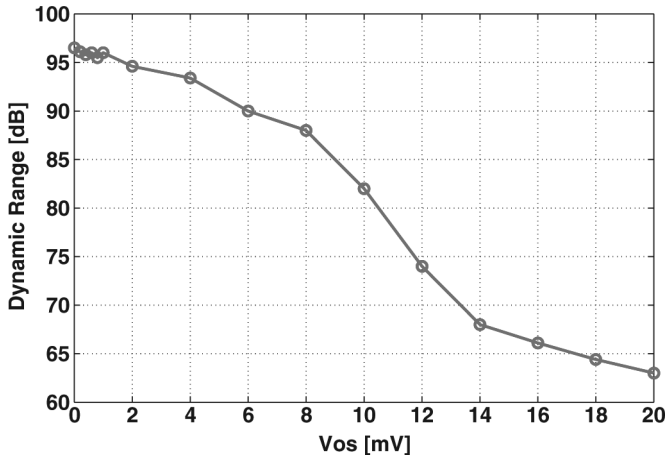

Fig. 10. Plot of simulated dynamic range versus OTA offset voltages.

where $V_{\rm OS}$, V_R, and $y_1[k]$ denote the offset voltage of the OTA, the reference voltage, and output of a tri-level quantizer, respectively. As shown in (9), the nonideality of a tri-level DAC mainly depends on the offset voltage of the OTA for a given reference voltage. Fig. 10 shows the simulated dynamic range of RMASH 2-1-1 as a function of offset voltage of the OTA. To target the dynamic range of 90 dB, an offset voltage of 5 mV is required. The offset voltage of 5 mV is achievable by carefully sizing and paying attention to the layout of the input differential pairs of the OTA.

E. Digital Decimation Filter

Since the digital output of the $\Sigma\Delta$ modulator is an oversampled noise-shaped signal, the complete ADC chip requires a digital decimation filter to perform down-sampling and out-band noise filtering. In this study, we designed a three-stage decimation filter to meet the linearity requirement of ADSL2+. The design of the decimation filter determines the filter types and coefficients by considering the finite word-length effect and the SNDR requirement and results in a three-stage digital filter. Fig. 11 shows the block diagram of the three-stage decimation filter. The first stage is a fifth-order cascaded integrator-comb

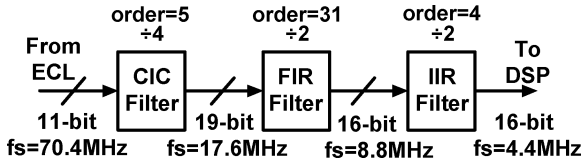

Fig. 11. Block diagram of the three-stage decimation filter.

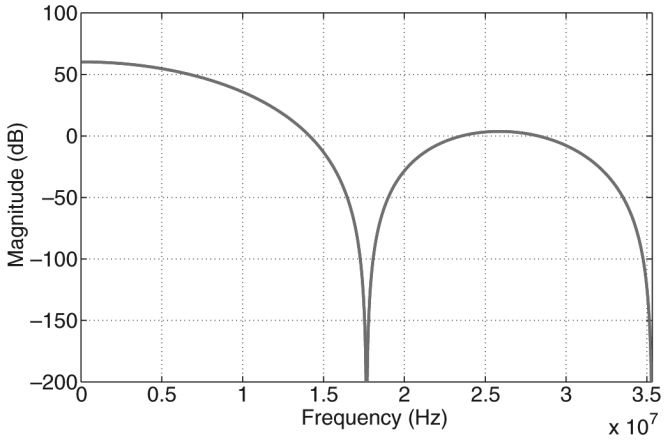

Fig. 12. Frequency response of the fifth-order CIC filter.

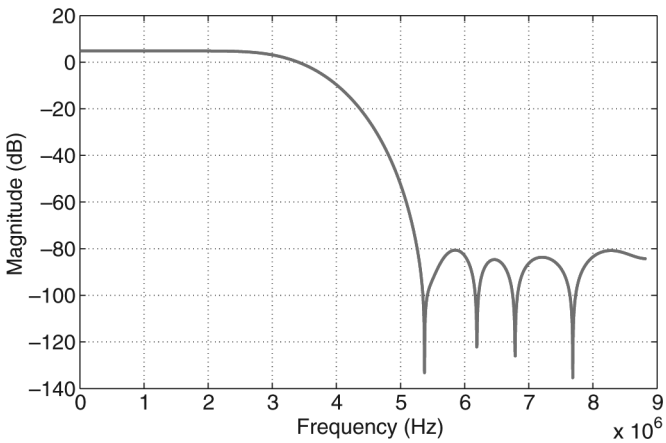

Fig. 13. Frequency response of the 31-tap FIR filter.

(CIC) filter with the down-sampling ratio of 4, and its transfer function is shown as follows:

$$\mathrm{CIC}(z) = \left(\frac{z^{-1}}{1-z^{-1}}\right)^5 z^{-4}(1-z^{-4})^5. \qquad (10)$$

Fig. 12 illustrates the frequency response and circuit implementation of CIC filter. Following the CIC filter, the second stage is a 31-tap finite impulse response (FIR) filter with a down-sampling ratio of 2. Fig. 13 shows its frequency response with finite word-length effect. Finally, the third stage is an infinite impulse response (IIR) filter with a down-sampling ratio of 2. The IIR filter is synthesized by the fourth-order Chebyshev Type II topology. The frequency response of the IIR filter is shown in Fig. 14.

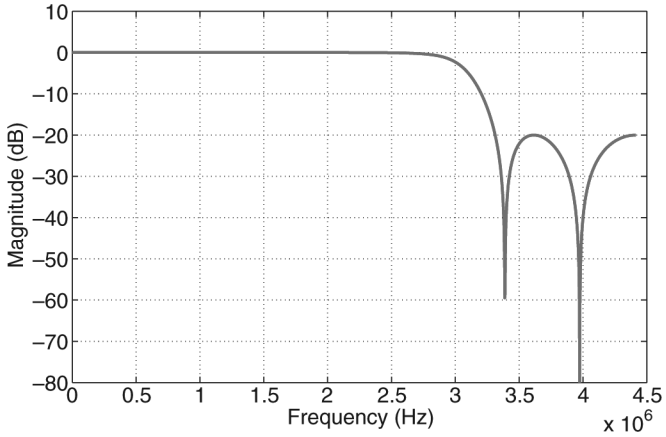

Fig. 14. Frequency response of the fourth-order IIR filter.

TABLE II
CIRCUIT SPECIFICATIONS FOR 14-bit 4.4 MS/s RMASH 2-1-$1_{1.5b}$

Optimized Spec. For	14-bit@4.4MS/s	
Modulator	Topology	RMASH 2-1-$1_{1.5b}$
	Oversampling ratio	16
	Sampling frequency	70.4MHz
	Clock jitter	15ps
	Reference voltage	±0.9V for 1st stage
		±0.45V for other stages
OTAs	Gm	10mS for 1st stage
		5mS for other stages
	DC-gain	75 dB for 1st stage
		60 dB for other stages
	Output swing range	1.2V
	Max. output current	3mA for 1st stage
		1mA for other stages
	Unity gain bandwidth	300MHz for 1st stage
		200 MHz for other stages
	Input noise	8nV/$\sqrt{Hz}$
	Input offset	2.5mV
Integrators	Input sampling capacitor	2pF
	Unit capacitor	0.5pF
	Capacitor deviation	0.5%
	Switch on-resistance	150Ω
Comparators	Offset	±15mV

III. CIRCUIT IMPLEMENTATION

A. Specifications for Building Blocks

Upon simulating the behavior of the proposed modulator, we determined the specifications of analog building blocks with consideration of power–performance tradeoffs. Table II summarizes the circuit specifications for the 14-bit 4.4 MS/s RMASH 2-1-$1_{1.5b}$. To evaluate the robustness, we modeled the critical circuit parameters as Gaussian distribution with the standard deviation of 20% and executed the Monte Carlo analysis by using MATLAB. The critical parameters are dc gain, transconductance, unity-gain bandwidth (GBW), output current, and input offset of OTAs, on-resistance of switches, and clock jitter. In addition, the standard deviations of integrator and feedforward gains are 0.5% and 2%, respectively. As shown in Fig. 15, the mean, minimum, and standard deviations of peak SNDR are 84.6 dB, 81.5 dB, and 0.72%, respectively.

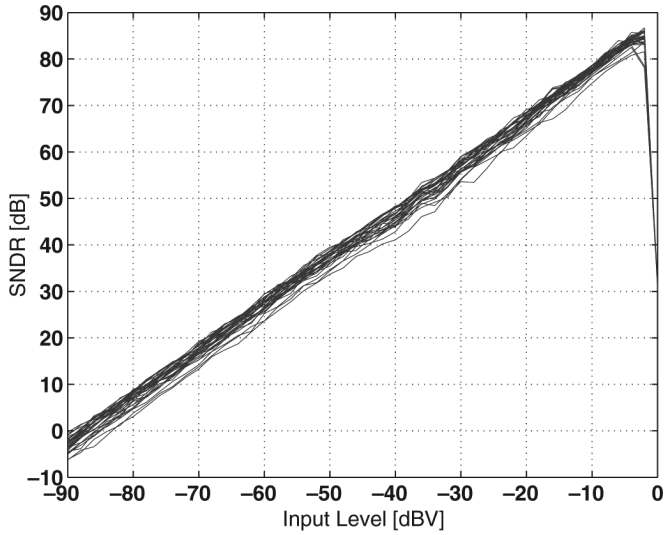

Fig. 15. Plots of simulated SNDR versus input level with 30 Monte Carlo analysis runs.

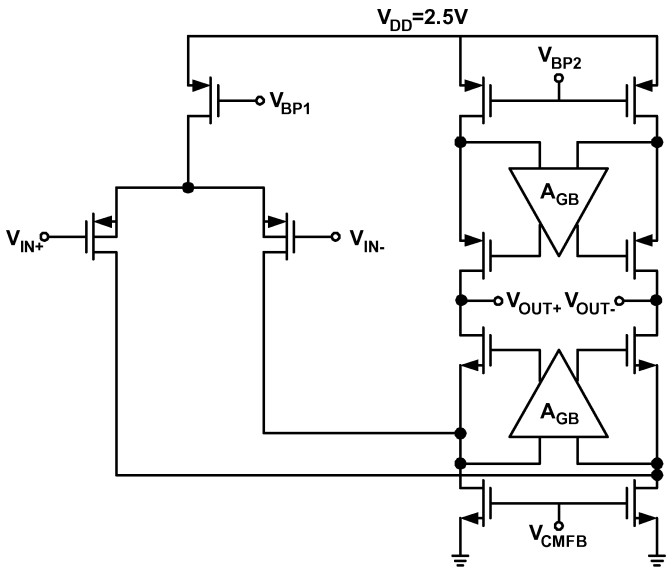

Fig. 16. Circuit schematic of the OTA.

B. OTA Circuit

According to Table II, the proposed modulator requires the dc gain of 75 dB and GBW of 300 MHz for the OTA with a supply voltage of 2.5 V. To meet the requirements, we chose a folded-cascode OTA with an additional gain-boosting amplifier. By carefully designing and sizing the gain-boosting amplifiers, the induced nondominant pole can be located at 1 GHz. The output swing of the first-stage integrators can be slightly reduced by using the tri-level quantizer and the input feedforward path. Hence, for a supply voltage of 2.5 V, the single-end output swing of the OTA is approximately 1 V.

Fig. 16 shows the schematic of the folded-cascode OTA being used for the first-stage integrators. The value of output swing of the OTA extracted from the system-level simulation is 1.2 V. In order to tolerate the process variation, we over-designed the output swing of the OTA to be 1.4 V in circuit-level specification, and a dc gain of more than 75 dB is accomplished over the entire output range. The OTA, including gain-boosting and biasing

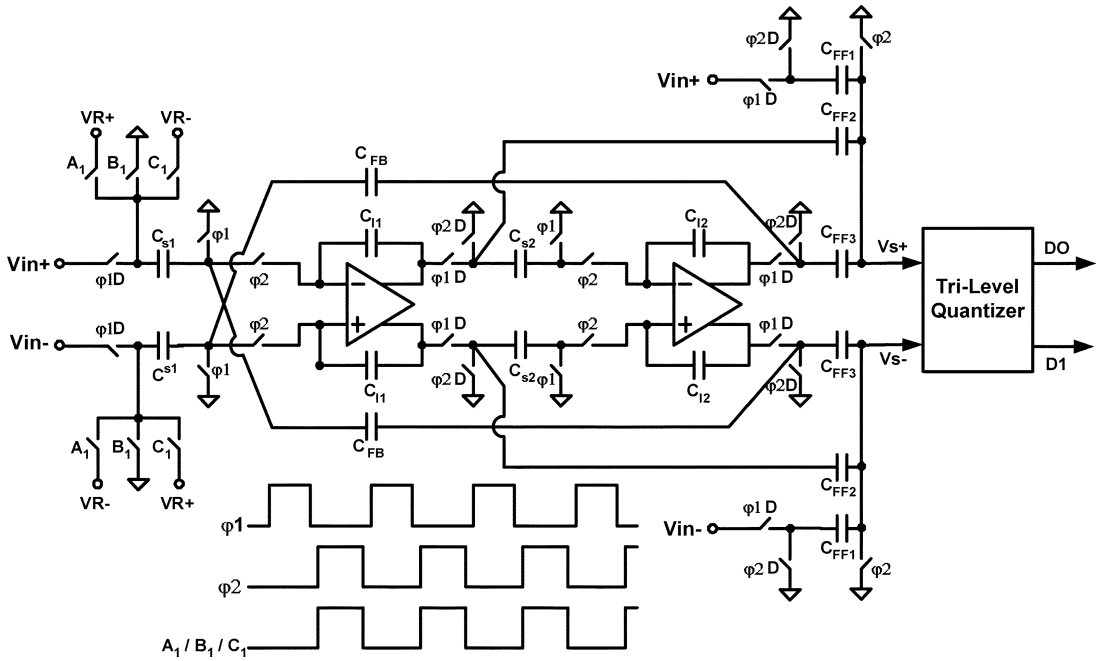

Fig. 17. Circuit implementation of the first-stage modulator.

circuits, dissipates 15 mW from a 2.5-V supply and achieves a GBW of 300 MHz with a capacitive loading of 5 pF, while the phase margin is 75°. The total thermal noise contribution over the 2.2-MHz signal bandwidth is about 12.6 μV. The SC common-mode feedback is used for the designed OTA because it does not dissipate the static power. The capacitors used in the common-mode feedback (CMFB) circuitry are properly chosen to maximize the gain bandwidth and thus avoid the settling error. We also used a similar OTA for other stages, and it dissipates 0.7 times the power consumption that the first-stage OTA consumes.

C. First-Stage Circuit

Fig. 17 illustrates the circuit diagram of the first-stage modulator. Since the dynamic range of the modulator is targeted at 90 dB at the sampling rate of 70.4 MHz, the sampling capacitor is chosen to be 1.5 pF and, accordingly, the integrating and resonator feedback capacitors are 3 and 0.375 pF, respectively. The closed-loop bandwidth of the front-end integrator is about 255 MHz, which is larger than three times the sampling frequency. Because the feedback gain of the tri-level DAC is equal to one, we can use the share-capacitor switching technique to eliminate coefficient mismatch. The share-capacitor switching technique is to have the input sampling and feedback DAC share a common sampling capacitor C_{S1} [17]. However, the dependent load on the reference voltage may cause harmonic distortion. In our work, we used a dummy SC network to reduce the distortion [18]. The output two-bit code of the tri-level quantizer is used to switch A_1, B_1, and C_1 at the integrating phase.

The summing circuit in front of the quantizer is implemented by using a passive SC network to avoid the use of an additional OTA and save the power dissipation. The summed signal can be expressed as

$$V_S(z) = \frac{C_{\mathrm{FF1}}V_{\mathrm{in}}(z) + C_{\mathrm{FF2}}Int1(z) + C_{\mathrm{FF3}}Int2(z)}{C_{\mathrm{FF1}} + C_{\mathrm{FF2}} + C_{\mathrm{FF3}}} \quad (11)$$

where C_{FF1}, C_{FF2}, and C_{FF3} are the capacitors for feedforward gains. According to behavioral simulation, the feedforward gains are not critical and can tolerate the variation up to 2%. This allows the use of small capacitance to implement the feedforward gains. We set the values of C_{FF1}, C_{FF2}, and C_{FF3} to 0.125, 0.25, and 0.5 pF, respectively. Note that the summed signal is scaled down by 1/7 when comparing with the parameters of Table I and Fig. 1. In order not to affect the desired performance of the modulator, the reference voltages of the quantizers must be scaled down by a factor of 1/7 from the nominal value. This also scales down the quantizer step size and, hence, increases the requirement of the comparator resolution. In our case, the required step size of the tri-level quantizer is about 150 mV. This requirement is feasible because, in practice, the CMOS comparator with preamplifier can provide a resolution better than 50 mV.

D. Tri-Level Quantizer Circuit

The circuit diagram of the tri-level quantizer is shown in Fig. 18. As mentioned above, the SC network must scale down the reference voltages, VR+ and VR-, by a factor of 1/7. So, we set the values of the capacitors C_{Q0} and C_{Q1} to 0.125 and 0.75 pF, respectively. In our design, we used a high-speed high-accuracy CMOS comparator with a preamplifier which is presented by [19]. The clock $\varphi 2A$ is used to control the generation of A_1, B_1, and C_1. Because of the time-delay of AND gates, the nonoverlapping interval of $\varphi 2A$ is limited to 1$\sim$2 ns when we have a sampling rate of 70.4 MHz.

E. Cancellation Filter and Decimation Filter Circuit

The implementation of the digital cancellation filter and decimation filter is based on the cell-based synthesis flow. According to the coefficients listed in Table I, the transfer functions

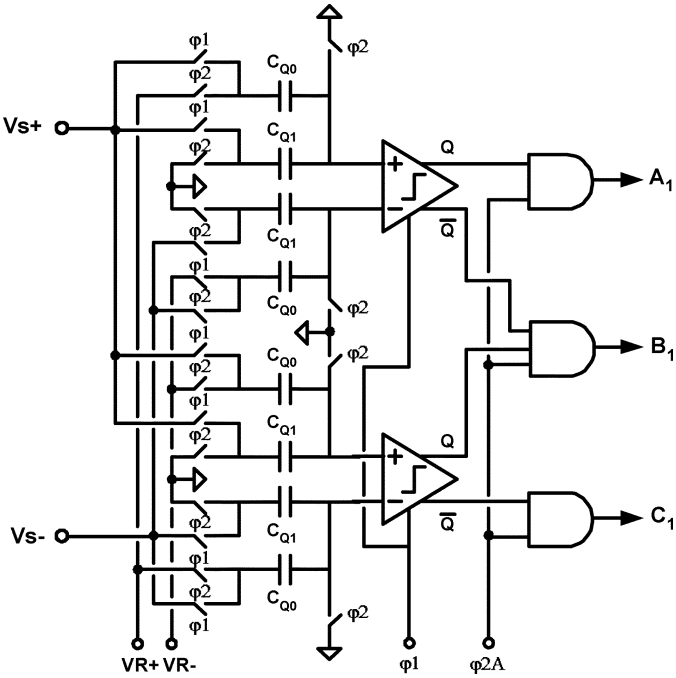

Fig. 18. Circuit implementation of the tri-level quantizer.

of the digital cancellation filters $H_1(z)$ and $H_2(z)$ are shown as follows:

$$H_1(z) = 1 - 2z^{-1} + 1.03125z^{-2} \quad (12)$$

$$H_2(z) = 1 - 3z^{-1} + 3.03125z^{-2} - 1.03125z^{-3}. \quad (13)$$

Fig. 19 illustrates the implementation structure of $H_1(z)$ and $H_2(z)$. By precision and error analysis, the output bit width of the digital cancellation filter is chosen to be 11 bits. The following equations are the transfer functions of the CIC filter and 31-tap FIR, respectively:

$$\begin{aligned} \mathrm{CIC(z)} &= z^{-9}\left(\frac{1-z^{-4}}{1-z^{-1}}\right)^5 \\ &= z^{-4}\left[(1+z^{-1})(1+z^{-2})z^{-1}\right]^4 \\ &\quad \cdot \left[(1+z^{-1}+z^{-2}+z^{-3})z^{-1}\right] \\ \mathrm{FIR(z)} &= a_0 z^{-1} + a_1 z^{-2} + a_2 z^{-3} + \ldots + a_{30} z^{-31} \end{aligned} \quad (14)$$

where

$$\begin{aligned} \mathrm{a0} &= \mathrm{a30} = -0.000061035 \\ \mathrm{a1} &= \mathrm{a29} = -0.0003662 \\ \mathrm{a2} &= \mathrm{a28} = -0.000366211 \\ \mathrm{a3} &= \mathrm{a27} = 0.001464844 \\ \mathrm{a4} &= \mathrm{a26} = 0.0036315918 \\ \mathrm{a5} &= \mathrm{a25} = -0.000823975 \\ \mathrm{a6} &= \mathrm{a24} = -0.012054443 \\ \mathrm{a7} &= \mathrm{a23} = -0.010437012 \\ \mathrm{a8} &= \mathrm{a22} = 0.019775390 \\ \mathrm{a9} &= \mathrm{a21} = 0.043701172 \\ \mathrm{a10} &= \mathrm{a20} = -0.002899160 \end{aligned}$$

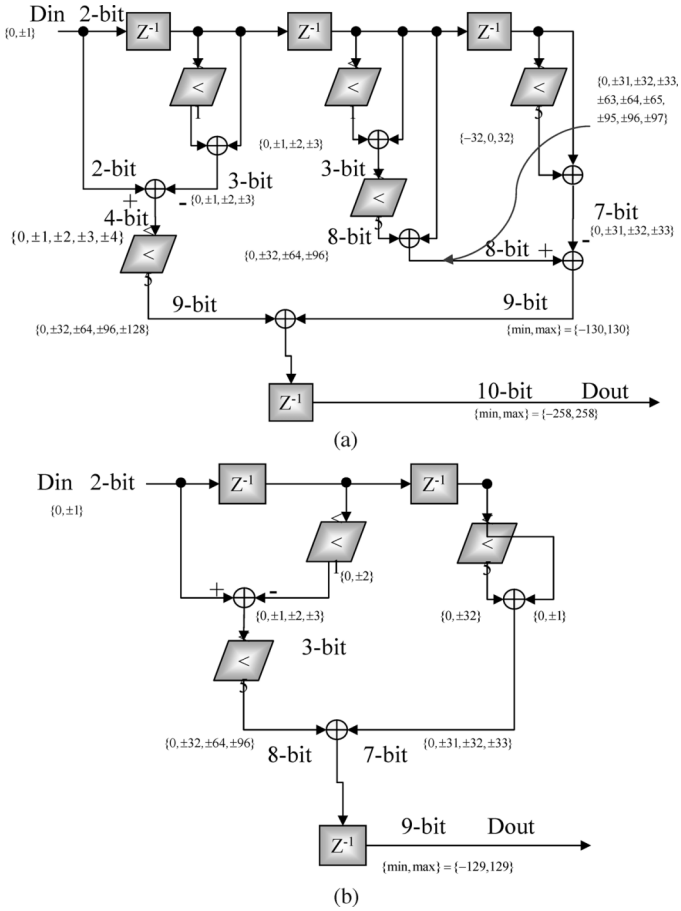

Fig. 19. (a) $H_1(z)$ and (b) $H_2(z)$ of circuit implementation of the cancellation filters.

$$\begin{aligned} \mathrm{a11} &= \mathrm{a19} = -0.09893799 \\ \mathrm{a12} &= \mathrm{a18} = -0.088989258 \\ \mathrm{a13} &= \mathrm{a17} = 0.154602051 \\ \mathrm{a14} &= \mathrm{a16} = 0.516235351 \\ \mathrm{a15} &= 0.692199707. \end{aligned} \quad (15)$$

By precision and error analysis, the output bit width of the CIC filter, FIR, and IIR are 19, 16, and 16 bits, respectively. The fourth-order IIR is a Chebyshev type-II filter. The stability of the fourth-order Chebyshev filter is guaranteed by considering the signal swing and filter coefficients. The overall SNDR of the decimation filter is designed to be higher than 80 dB to satisfy the requirement of ADSL2+ performance.

IV. Experimental Results

The modulator is designed for a sampling rate of 70.4 MHz and a fixed OSR of 16, so the signal bandwidth is 2.2 MHz. The modulator was fabricated in a 0.25-μm 1P5M CMOS technology with metal–insulator–metal (MIM) capacitors. The power dissipation of the modulator and digital decimation filter with I/O pads is 62.5 and 120 mW with a 2.5-V supply, respectively. Fig. 20 shows the chip microphotograph in which the experimental ADC includes the clock generator, reference buffer, bandgap circuitry, and decimation filter. To measure the performance data, the chip was mounted onto a four-layer

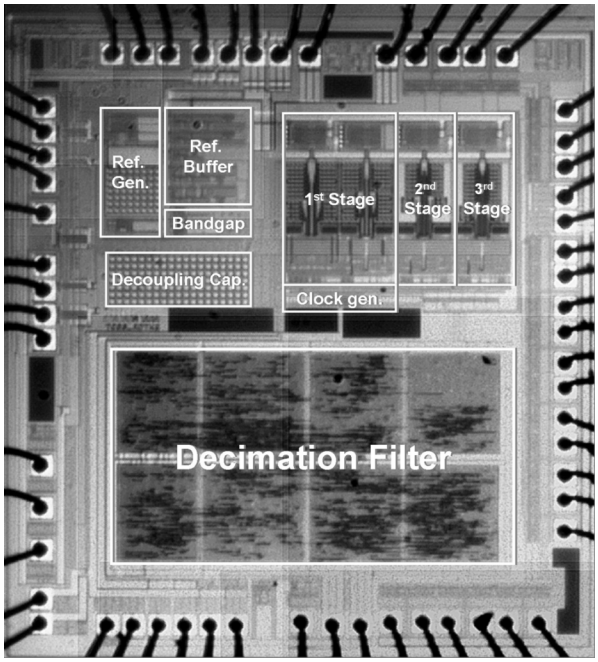

Fig. 20. Chip microphotograph.

printed circuit board to separate the analog signal from the digital signal and hence reduce the crosstalk. The input clock is generated from an external 70.4-MHz low-jitter crystal with independent power supply voltages to avoid the switching-noise coupling. With a sampling rate of 70.4 MHz, the ADC achieves a dynamic range of 86 dB and a peak SNDR of 78 dB. Note that the overall power dissipation of the ADC can be further reduced by synthesizing the digital decimation filter with lower supply voltage. Fig. 21 illustrates the measured SNR and SNDR against input level for the ADC. The measured output spectrum for a 500 kHz sinusoidal input is shown in Fig. 22, and, accordingly, the SFDR is 89 dB. To quantitatively evaluate the efficiency among power dissipation, dynamic range, and conversion rate, we use the formulas for the effective number of bits (ENOB) of the ADC and the figure-of-merit (FOM) as shown below [20]:

$$\text{ENOB} = \frac{\text{dynamic range} - 1.76}{6.02}$$
$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} \times \text{Conversion Rate}} 10^{12}. \qquad (16)$$

Fig. 23 shows the FOM distribution of our work and existing wideband (>1 MHz) SC $\Sigma\Delta$ modulators. Table III summarizes the measured performance and specifications of the proposed modulator and compares with the other wideband SC $\Sigma\Delta$ modulators as well.

V. Conclusion

This paper addresses a low-power, high-linearity cascaded $\Sigma\Delta$ ADC architecture appropriate for ADSL2+ application. This study uses three approaches to improve performance and reduce power consumption: using the resonator-based topology, applying the tri-level quantization, and using two pairs of reference voltages. The proposed modulator has been fabricated in TSMC 0.25-μm 1P5M CMOS technology. As shown in the experimental result, the designed ADC can achieve a peak SFDR of 89 dB, a dynamic range of 86 dB, and a peak SNDR of 78 dB.

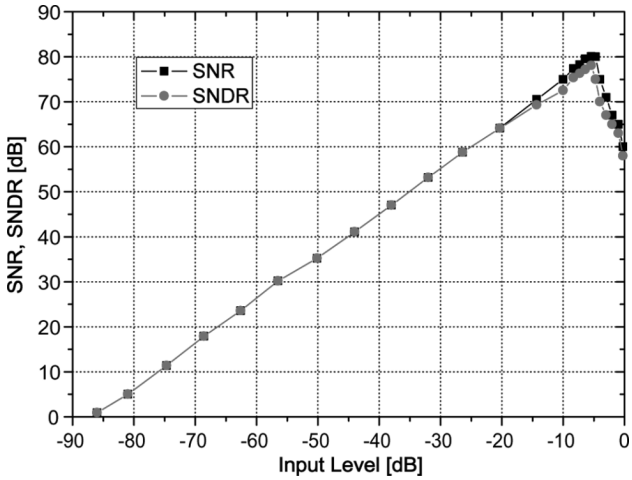

Fig. 21. Plots of measured SNDR and SNR versus input signal level.

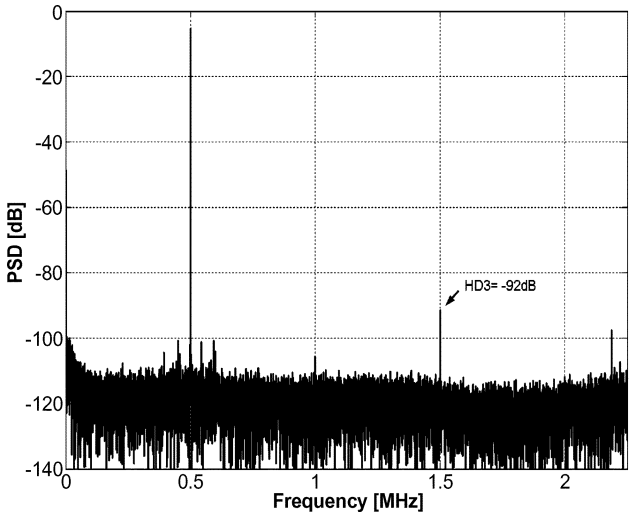

Fig. 22. Measured output PSD of proposed RMASH 2-1-$1_{1.5b}$ ADC.

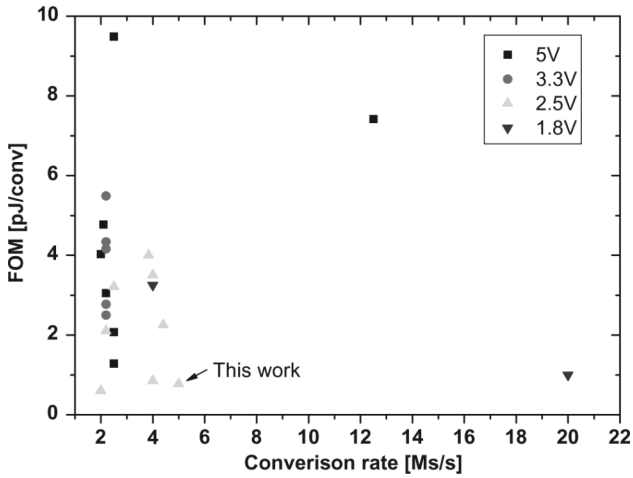

Fig. 23. FOM distribution of wideband SC $\Sigma\Delta$ modulators with respect to conversion rate.

TABLE III
CIRCUIT SPECIFICATIONS FOR 14-bit 4.4 Ms/s RMASH 2-1-$1_{1.5b}$

Refs	Topology	Bandwidth (MHz)	OSR	SNDR/DR (dB)	Technology (CMOS)	Die Size (mm2)	Power (mW)	FOM (pJ/conv)
[5]	5th	2	8	82 / 83	0.18-μm 1.8V	2.9	150	3.25
[6]	2nd	1.92	12	70 / 76	0.18-μm 2.7V	1.4	50	2.53
[7]	4th	2	12	74 / 80	0.25-μm 2.5V	2.6	105	3.21
[8]	2-2-1	2	16	87 / 95	0.5-μm 2.5V	10	150	0.82
[9]	2-1-1	2.2	16	72.7 / 78	0.25-μm 2.5V	2.78	65.8	2.3
this work	2-1-1	2.2	16	78.5 / 86	0.25-μm 2.5V	1.4	62.5	0.87
						2.8*	182.5*	2.5*

*Include digital decimation filter

ACKNOWLEDGMENT

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