國立交通大學

材料科學與工程學研究所
碩士論文

磷化銦鎵高電子遷移率電晶體暨砷化銦鎵金氧半

高電子遷移率電晶體於高頻與數位應用之探討

Study of InGaP HEMTs and In$_x$Ga$_{1-x}$As

MOS-HEMTs for RF and Digital Applications

研究生　　鍾榮濤

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中華民國九十七年八月

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摘要

不同載子參雜方式的磷化銦鎵高電子遷移率電晶體的高頻與數位特性在此被研究。在高頻無線通訊應用上，為了要提升線性度，載子被均勻參雜於蕭基層與參雜載子於通道層。以均勻參雜載子的方式製成之元件，三階交叉點可達 22.19 dBm；通道參雜載子的方式製成之元件線性工作範圍達 14.23 dB，並且三階交叉點電源損耗比值接近 4.97。在數位邏輯應用上，均勻參雜載子的方式製成之元件可提升次臨線傳導斜率，以及開關電流比值；通道參雜載子的方式製成之元件的短通道效應也有所降低。

在數位應用時，高銦含量的砷化銦鎵通道材料是必須的，使元件能具有好的數位特性表現以及較高速的轉導特性。以原子層沉積氧化鋁做為閘極絕緣層也能降低漏電流並提高崩潰電壓。砷化銦鎵金氧半假晶式高電子遷移率電晶體和砷化銦金氧半高電子遷移率電晶體被製作出來並展現出良好的絕緣性。此外，將空橋結構應用於砷化銦金

氧半高電子遷移率電晶體做出不同閘極寬度的元件，可做為數位應用

上不同扇出層級之元件。

Study of InGaP HEMTs and In$_x$Ga$_{1-x}$As MOS-HEMTs for RF and Digital Applications

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Abstract

The RF and digital performance of InGaP/In$_{0.22}$Ga$_{0.78}$As pseudomorphic high electron mobility transistors (PHEMTs) with different doping profiles are investigated. In order to improve the device linearity for RF applications, the uniformly-doped and channel-doped structures are designed and the devices are compared. The uniformly-doped device shows higher IP3 of 22.19 dBm, and the channel-doped device shows higher Δ (IP3-P$_{1dB}$) of 14.23 dB and higher IP3 to DC power consumption ratio (IP3/P$_{DC}$) of 4.97 compared to other devices. Figures of merits of these devices for digital applications are also evaluated. SS and I$_{ON}$/I$_{OFF}$ ratio parameters can be improved by uniformly-doping in the Schottky layer and DIBL parameter can be reinforced by extra doping in the channel layer.

For digital applications, the InGaAs channel with high indium concentration is required for better performance and higher transconductance. In addition, atomic layer deposition (ALD) Al$_2$O$_3$ is introduced to act as the gate insulator to reduce gate leakage current and increase breakdown voltage. Thus, the InAlAs/In$_{0.7}$Ga$_{0.3}$As

metal-oxide-semiconductor metamorphic HEMTs (MOS-MHEMTs) and InAlAs/InAs MOS-HEMTs were fabricated and the insulating properties were improved. Moreover, the InAlAs/InAs MOS-HEMTs employing air-bridge structure with different gate widths exhibit similar threshold voltage, leading to the possibility for digital utilization of different fan-out level.

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Chapter 1
Introduction

1.1 General Background

The RF and digital performance of high electron mobility transistors (HEMTs) have been widely investigated. For high frequency wireless communication, as the density in information traffic increasing, the requirements of device linearity become more demanding. In addition, the device linearity could be improved by varying the doping profiles. The device linearity of InGaP/InGaAs HEMTs with different doping profiles will be discussed in this dissertation.

For digital applications, recent years have seen that high electron mobility transistors (HEMTs) have attracted more attention because it is a potential candidate for future low-power logic applications[1]. Current Si technology roadmap is expected to come to the end when the physical gate length is shrunk to 10 nm which is believed to be the scaling limit for CMOS. For the next generation device technology, endowed with high electron mobility, III-V material HEMTs exhibit superior device performance such as higher transconductance, higher current density, lower power consumption and higher operating frequency in comparison with Si MOSFETs as Fig.1-1 indicates[2].

Owing to the high mobility and small energy band gap, InGaAs is widely used as the channel material to form hetero-junctions of HEMTs[3]. Accompanying with the Indium content of InGaAs increases, the electron mobility increases dramatically from 4600 $cm^2V^{-1}S^{-1}$ (In: 0%)

to 20000 $cm^2V^{-1}S^{-1}$ (In: 100%) at 295K. Meanwhile, the energy band gap decreases, resulting in high gate leakage problem and low breakdown voltage. As the Fig.1-2 shows, the lattice constant increases as the band gap decreases, where also causes larger lattice mismatch with Silicon, leading to difficulty of integration between InGaAs and Si.

The logic suitability of InAlAs/$In_{0.7}Ga_{0.3}$As and InAlAs/InAs InP HEMTs were estimated by D-H Kim et al., and high performance at low bias voltage (V_{DS}=0.5V) for low-power logic applications were also obtained[4]. Including subthreshold slope (S), drain-induced barrier lowering (DIBL) and I_{ON}/I_{OFF} ratio, above figures of merit (FOM) which are defined by Dr. Chau [1] are exhibited. However, further researches are of importance on solving the gate leakage problems, improving electrical characteristics and integrating III-V materials on silicon.

In this study, HEMTs with InGaAs channel of three different Indium concentrations ($In_{0.22}Ga_{0.78}$As, $In_{0.7}Ga_{0.3}$As and InAs) were fabricated to investigate low-power logic suitability. In the first part, InGaP/$In_{0.22}Ga_{0.78}$As pseudomorphic high electron mobility transistors (PHEMTs) with various doping profiles were manufactured to identify the effects of doping profiles for RF and digital applications. In the second part, atomic layer deposition (ALD) Al_2O_3 will be introduced as gate insulators for InAlAs/$In_{0.7}Ga_{0.3}$As metal-oxide-semiconductor metamorphic high electron mobility transistors (MOS-MHEMTs) formation to solve the gate leakage problems. Finally, the fabrication of InAlAs/InAs/InP MOS-HEMTs employs air-bridge structure to develop several fan-out level devices. The RF and digital performances of HEMTs will be shown in the later chapters.

1.2 Thesis Content

The contents of this thesis are composed of literature review, fundamentals of electrical characteristics, issue I~III, and conclusions. In Chapter 2, the literature survey on the HEMTs for digital applications and the fabrication of MOS-HEMTs are reviewed. In Chapter 3, the fundamentals of electrical characteristics are addressed. In Chapter 4, the brief introduction, experiment, results and discussion of issue I (digital and RF performance of HEMTs with different doping profiles) are described. In Chapter 5, the motivation, process flow, results and discussion of issue II (introducing ALD Al_2O_3 as gate insulator for MOS-HEMTs fabrication) are discussed. In Chapter 6, the introduction, experiment, results and discussion of issue III (employing air-bridge structure on InAs MOS-HEMTs for digital applications) are exhibited. Finally, the conclusions will be given in Chapter 7.
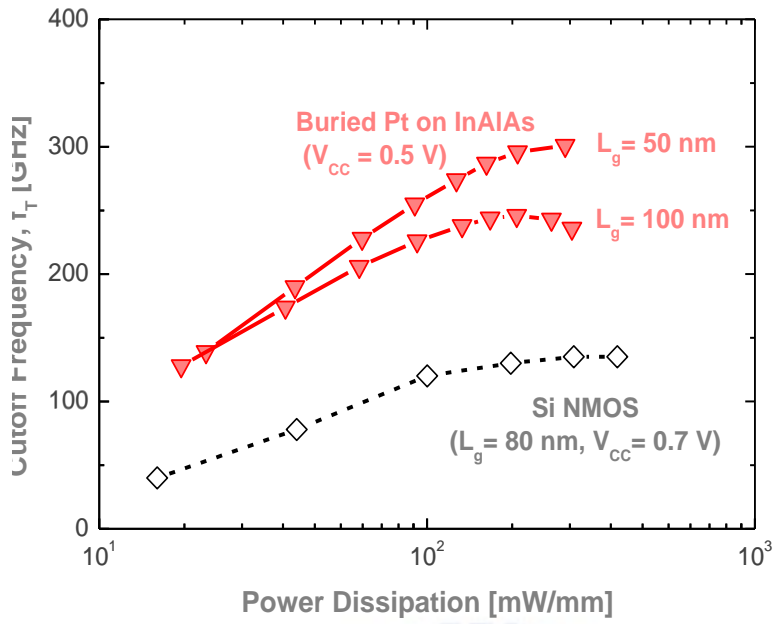
Fig. 1-1 Cutoff frequency versus power dissipation curves of HEMTs and Si-MOS
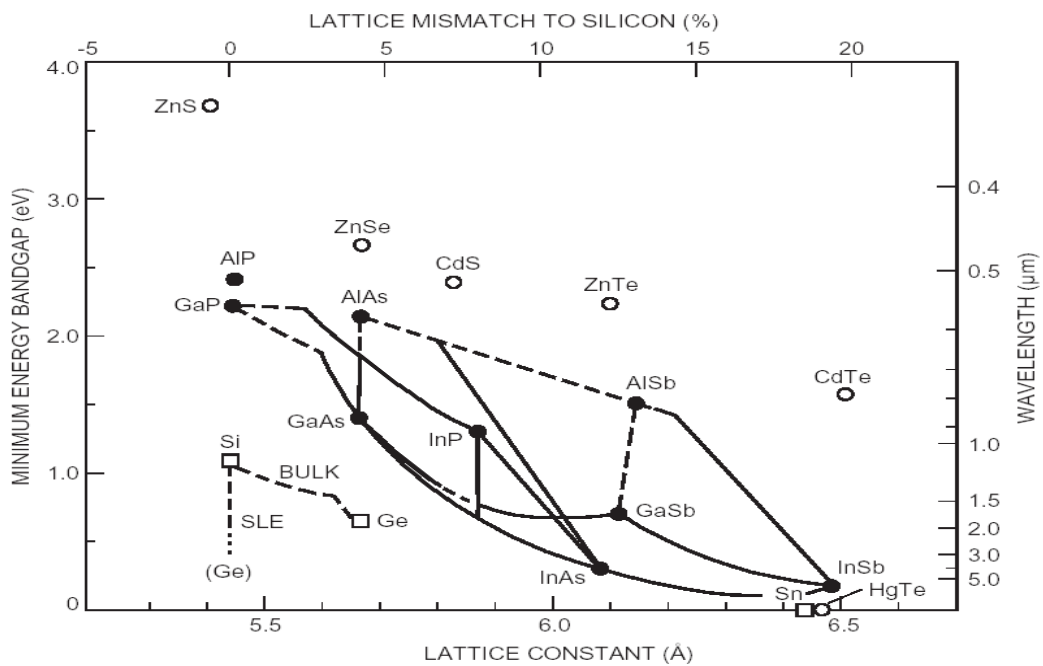
Fig. 1-2 Energy band gap versus lattice constant diagram of III-V materials

Chapter 2 Literature Review

2.1 HEMTs for digital applications

The alternative devices of Si MOSFET for digital applications are researched because the Si technology roadmap is expected to come to the end. III-V material HEMTs are the potential candidates due to superior device performance as mentioned in the former chapter.

Recently, the 40nm InAs HEMT and the $In_{0.7}Ga_{0.3}As$ HEMT which have been fabricated by Dae-Hyun Kim and Jesús A. del Alamo exhibit impressive results for high-performance low-power application[2.4]. The 100nm $In_{0.7}Ga_{0.3}As$ HEMTs yield drain induced barrier lowering (DIBL) as low as 80 mV/V, subthreshold slope (S) of 77 mV/decade, and I_{ON}/I_{OFF} ratio in excess of 10^3 with a gate delay of about 1.2 ps. Moreover, the 40nm InAs HEMTs demonstrate DIBL = 80 mV/V, S = 70 mV/decade, I_{ON}/I_{OFF} ratios in excess of 10^4 and f_T= 475 GHz. These remarkable results imply that InAs is a material with great potential for beyond Si CMOS logic applications.

The high performance of the HEMTs could be summarized to optimize the following three parameters. One is the gate length. The shrink of gate length leads to higher G_m and cutoff frequency. Another is the gate-to-channel thickness. Thinner insulator devices exhibit more positive V_T, higher current drive and better short channel effects, such as lower output conductance, less DIBL and sharper subthreshold slope. The other parameter that has to be moderated is the lateral recess length which

is the effective factor of gate-to-drain capacitance (C_{GD}). The optimized lateral recess length is 150 nm.

2.2 Logic parameters for low-power application

The calculating methods of the logic parameters, including subthreshold slope (SS), drain-induced barrier lowering (DIBL), I_{ON}/I_{OFF} ratio and gate delay time, above figures of merit (FOM) are defined by Dr. Chau[2]. The bias point is set at V_{DS}=0.5 volt. The I_{ON}/I_{OFF} ratio can be defined as the following. First, we defined the threshold voltage as the value of V_{GS} for which the drain current is 1 mA/mm at $V_{DS} = V_{CC}$. Then, we selected I_{ON} as 2/3 V_{CC} above V_T, and I_{OFF} as 1/3 V_{CC} below. The above methodology is displayed in Fig. 2-1.

The definition of the subthreshold slope (SS) and drain-induced barrier lowering (DIBL) are illustrated in Fig. 2-2. The steepness of the transition between the on and off states is evaluated through the SS. The smaller magnitude of SS means one can apply less gate voltage to control the on and off current. The tightness of the threshold voltage is evaluated by DIBL, which measures the change in V_T as a result of a change in V_{DS}. If DIBL is small, V_T is insensitive to manufacturing circuit design.

Finally, the gate delay time is of importance to evaluate the response time of gate. The following formula gives the estimating equation, where C is total gate capacitance, which could be calculated by measuring high frequency S-parameters.

$$\frac{C\,V}{I} = \frac{(C_{GS} + C_{GD})|_{V_{cc},\,I_{ON}} \times V_{CC}}{I_{ON}}$$

2.3 MOS-HEMTs fabrication

Owing to the high performance of the above devices, InAs HEMT is expected to be the most potential candidate for the next generation technology[5]. However, the small band gap of InAs channel leads to the impact ionization between gate and grain, and the Schottky gate also suffers from gate leakage problem. Therefore, the insulating layer is introduced to solve the problem, including high aluminum content native oxide of InAlP or InAlAs[6], ALD high-k dielectrics such as Al_2O_3[7] and HfO_2[8].

2.4 Surface treatment

Surface treatment is of importance to be handled before applying the insulating layers to restrain interface trap density which would cause the undesired Fermi level pinning of the carriers. Several surface treatment solutions have been exhibited with high capability of passivation, such as HCl, NH_4OH and $(NH_4)_2S_X$. The devices treated by NH_4OH and $(NH_4)_2S_X$ reveal compatibility between the oxide layer and semiconductor[9].
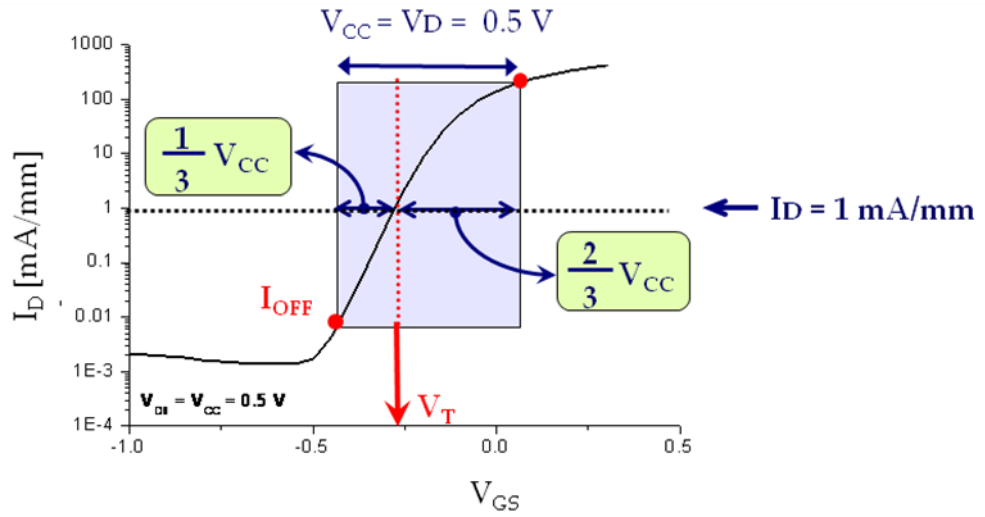
Fig. 2-1 The definition of threshold voltage (V_T) and I_{ON}/I_{OFF} ratio
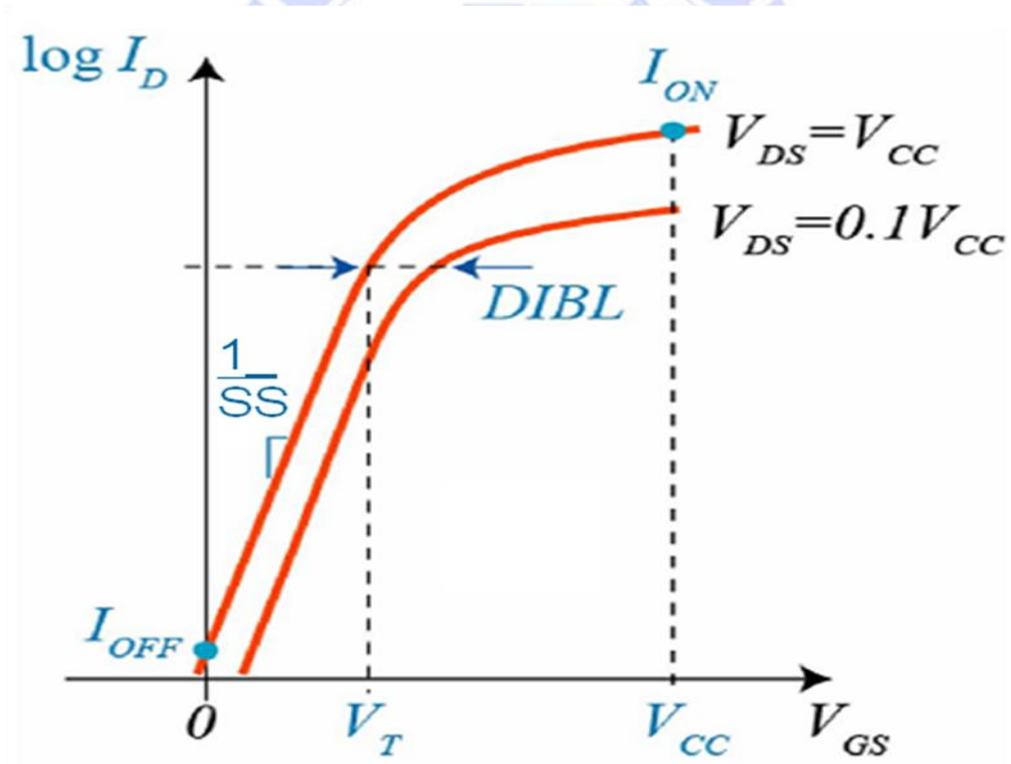
Fig. 2-2 The definition of subthreshold slope (SS) and drain induced barrier lower (DIBL)

Chapter 3
Fundamentals of Electrical Characteristics

For devices used in high frequency operation, we need to consider the operation frequency, linearity, power density, power efficiency, and noise figure. In this chapter, the correlation of the device performance with the device structure used will be discussed. These include the improvement of device breakdown voltage, noise figure, linearity, and f_T, f_{max} based on the improved design of the device structure.

3.1 Device model

PHEMT developed is characterized using on-wafer probing and the bias-dependent S-parameters are measured and followed by equivalent circuit parameter extraction. The small-signal equivalent circuit (Figure 3-1) used for parameter extraction also requires "cold measurement" ($V_{ds}=0$). The cold measurement data are used to estimate the value of the parasitic elements following the procedures proposed by Berroth and Bosch for MESFETs.

As shown in Figure 3-1, the symbols for the device parameters could be explained as following.

(a) C_{gs}：the capacitance between gate and source has the expression.

$$C_{gs} = C_{gsi} + C_{gsf}$$

where C_{gsi} is an intrinsic component which for a given L_g is proportional to $1/D_g$, and C_{gsf} is a fringing capacitance which is an additional parasitic capacitance. D_g is gate-to-channel distance, and C_{gs} is expected to be proportional to $1/D_g$ and increases with recess depth. The magnitude of C_{gsf} is relatively small compared to the intrinsic C_{gsi} value [3].

(b) C_{gd} ：the capacitance between gate and drain is given as ：

$$C_{gd} = C_{gd,dep} + C_{gd,met} = C_{gdi} + C_{gdair} + C_{gdsc}$$

$C_{gd,met}$ is the feedback capacitance due to the gate-drain metallization depending on the gate-to-drain distance. $C_{gd,dep}$ is the feedback capacitance due to the gate-drain depletion [4].

In another expression, C_{gd} is a parasitic capacitance between gate and drain, and it consists of three terms: C_{gdi} (the capacitance of the gate-drain surface depletion region), C_{gdair} (a weak contribution through the air), and C_{gdsc} (an intrinsic component due to the short channel effect). By a deeper recess, C_{gdi} and C_{gdair} decrease due to lateral extension of the recess notch. C_{gdsc}, on the other hand, increases due to the reduced short channel effect. Since the later effect is important for shallow recess, the overall C_{gd} characteristics show first a slow rate of decrease in capacitance with recess and later on a much faster rate of decrease, and the ratio of C_{gs} and C_{gd} increases with deeper recess [3].

(c) R_i ：the series resistance between gate and drain

(d) G_d ：the conductance between drain and source

(e) C_{ds} ：the capacitance between source and drain

(f) L_g：the inductance of the gate metal

(g) R_g：the resistance of the gate

(h) G_m：transconductance

(i) R_s：the resistance of the sum of gate-source intervening material and

the ohmic contact of the source electrode.

(j) L_s：the inductance of the sum of gate-source intervening material and

the ohmic contact of the source electrode.

(k) R_d：the resistance of the sum of gate-drain intervening material and the

ohmic contact of the drain electrode.

(l) L_d：the inductance of the sum of gate-drain intervening material and

the ohmic contact of the drain electrode.

3.2 Noise figure (NF)

In wireless communication, the generation of noise will affect the quality of the signal transmission. The transferred signals cannot be discriminated if the noise disturbance is too large. There are many different types of noise generation, and the two most influential of them are "thermal noise" and "shot noise". In real amplifiers, thermal noise consists of the resistance in circuit, the electrode impedance of the transistor, and the resistance of the semiconductor layer. Shot noise is due to the electron migration. The equivalent circuit with noise source is shown in Figure 3-2.

According to the Nyquist theorem, the effective noise power P_{nav} in the bandwidth Δf can be expressed as：

$$P_{nav} = kT\Delta f$$

where k is the Boltzmann's constant, and T is the absolute temperature. If we show with noise voltage：

$$\overline{e^2} = 4kTR\Delta f$$

Therefore, the source resistance R_s, gate resistance R_g, and the drain resistance R_d would generate resistance thermal noise $\overline{e_s^2}$, $\overline{e_g^2}$, and $\overline{e_d^2}$. The noise figure can be expressed as [5]：

$$F_{mim} = 1 + K_f \frac{f}{f_T} \sqrt{G_m (R_s + R_g) + K_i} \tag{1}$$

3.3 Linearity

Linearity of amplifiers is often assessed by the third-order intercept point (IP3). If an amplifier is presented with two signals closely spaced in frequency, and a perfectly linear amplifier would simply amplify the two signals. However, the real amplifier is never with perfectly linearity, and nonlinearity will result in additional output signals. A nonlinear amplifier will have a transfer function that can be approximated as：

$$P_o = a_1 P_{in} + a_2 P_{in}^2 + a_3 P_{in}^3 + \ldots \tag{2}$$

where P_{in} and P_o are the input and output power, and a_i are coefficients. A linear amplifier would have $a_i = 0$ for $i > 1$. Consider an input signal with

two closely spaced frequencies, f_1 and f_2：

$$P_{in} = P_1\sin(2\pi\ f_1 t) + P_2\sin(2\pi\ f_2 t) \tag{3}$$

If Eq. (3) were substituted into Eq. (2), we can use elementary algebra and trigonometric identities to show that the output power (P_o) contains the following components：

$a_1 P_1 \sin 2\pi f_1 t$

$a_1 P_2 \sin 2\pi f_2 t$ (fundamentals)

$\dfrac{1}{2} a_2 P_1^2 \sin 2\pi(2f_1)t$

$\dfrac{1}{2} a_2 P_2^2 \sin 2\pi(2f_2)t$ (second-order products)

$\dfrac{3}{4} a_3 P_1^2 P_2 \sin 2\pi(2f_1 \pm f_2)t$

$\dfrac{3}{4} a_3 P_1^2 P_2 \sin 2\pi(2f_1 \pm f_2)t$ (third-order products)

$\vdots$

Assuming $P_1 = P_2$, second-order product power is proportional to the square of the input signal power, third-order product power is proportional to the cube of the input signal power, and so on. But only the odd and greater than third-order terms have greater attribution to the fundamental signal. So we usually consider the fundamental signal and the third-order product signal only. Figure 3-3 is the output power diagram of the fundamental and the third-order product signals. From Figure 3-3, we can identify the third-order intercept point (IP3). The P_{in} value of IP3 is also called IIP3, which is important for low noise amplifier. From the fundamental diagram of microwave front-end device (Figure 3-4), the low noise amplifier is used to receive signals. So a higher IIP3

value results in a higher linearity of the amplifier, and the less distortion of the input signals.

3.4 Breakdown voltage (BV$_{gd}$)

3.4.1 Physics for device breakdown

Breakdown in HEMT devices may result from many effects, such as avalanche multiplication, thermionic or thermionic-field emission across the insulator, and electron tunneling through the insulator, which is also referred to as "impact ionization" at a potential step. The insulator contains Schottky layer and channel layer, and the impact ionization mechanism consists of two steps. First, electrons are injected by thermionic field emission from the gate to the insulator. Second, because of the large conduction band offset and the electron field in the insulator, these hot electrons enter into the high field gate-drain region of the channel. Then the electrons immediately relax their energy through impact ionization.

For the InAlAs/n$^+$-InGaAs HEMT, the off-state breakdown voltage increases with lower InAs mole fraction in the insulator and enhanced channel bandgap (by quantum size effects in thin channels). The insulator with lower InAs content has a larger schottky barrier height, and enhances breakdown by suppressing thermionic emission. Besides, increase in channel bandgap (by quantum size effects) also increases breakdown voltage by suppressing impact ionization [6].

Different kinds of devices may suffer from different breakdown mechanisms, depending on the details of the design such as insulator thickness, recess, and channel composition. Breakdown voltage also shows a negative temperature coefficient. The channel electrons heated by the lateral electric field give rise to impact ionization and light emission. We were able to identify two main different light emission mechanisms. They are conduction band to conduction band transitions for low energy photons, and conduction band to valence band transitions for high energy photons. The correlation between the gate current and the light intensity allowed us to separately evaluate the electron and hole components of the gate current.

For InAlAs/InGaAs heterostructure FET, the gate current at room temperature is strongly influenced by Real Space Transfer (RST) of both hot holes and electrons across the InAlAs barrier. According to the I_d vs. V_{ds} curve, the negative gate current reaches a maximum when V_{gs}=0V and then decreases by increasing the gate voltage toward negative values. This increase in the gate current is due to the RST and collection of holes generated by impact ionization at the drain end of the channel, where the maximum electric field occurs [7].

The gate-to-drain breakdown voltage BV_{gd} is defined as the gate-to-drain voltage when the gate current is 1mA/mm.

3.4.2 Analytic model for design

Figure 3-5 shows a schematic cross-section of an InAlAs/InGaAs

HEMT with the depletion region near the gate electrode at the saturation region. The gate is assumed to be formed symmetrically between drain and source electrodes, and the channel is to be depleted between the gate and drain because of drain-gate voltage V_{gd}. The length of the depletion region between the gate and drain is denoted as L_{dep}.

From Figure 3-5, the lateral electrical field in the channel E_{ch} can be obtained by assuming that all electric field lines associated with lateral spreading of the depletion region terminate over some distance L_0 along the gate metal. This assumption was proposed by Wemple et al. to describe the breakdown voltage of GaAs-based MESFETs with a recessed gate, and the breakdown phenomena can also be successfully explained using this assumption. This assumption was applied to a HEMT structure to describe the breakdown. The distance L_0 plays a roll in the adjustable parameter of the model but not in $L_0 << L_g$. The lateral electrical field in channel E_{ch} is obtained by applying Gauss's law to the geometry of Figure 3-5.

$$E_{ch} = \frac{q n_s x}{\varepsilon L_0} \tag{4}$$

where x is the coordinate along the gate, the origin of which is at the edge of the gate, ε is the dielectric constant of material of the channel, and n_s is sheet carrier concentration in the channel.

The breakdown voltage BV_{gd} can be defined as the gate-to-drain voltage when E_{ch} is equal to avalanche electric field E_a. If the distance x_b where E_{ch} is equal to E_a where smaller than L_r, BV_{gd} can be defined and obtained by integrating Eq. (4) with respect to x from 0 to L_{dep}.

$$BV_{gd} = \frac{\varepsilon L_0 E_a^{\ 2}}{2qn_s} \quad \text{when } x_b < L_r \tag{5}$$

where the voltage drop between the gate and drain is assumed to mainly occur in the depletion region. Using this assumption, the length of the depletion region L_{dep} can be obtained by integrating Eq. (4) with respect to x from 0 to L_{dep}.

$$L_{dep} = \sqrt{\frac{2\varepsilon L_0}{qn_s} V_{gd}} \tag{6}$$

The depletion region spreads with V_{gd} and the breakdown phenomena occur when L_{dep} is equal to x_b. Note that the expression of BV_{gd} in Eq. (5) means that the breakdown voltage is not improved by widening the gate recess region and it is determined by only the structure of the epitaxial layers.

Figure 3-6 shows the dependence of the breakdown voltage BV_{gd} on the width of the gate recess. They can be calculated by using a simple model that was already described before. The calculated breakdown voltage increased with the width of gate recess and then saturated. This tendency was also confirmed experimentally [8].

3.4.3 Improvement of the breakdown voltage

In the off state, the gate leakage current is generally attributed to a two-step process. First, impact ionization in the channel creates electron-hole pairs. Second, the resulting holes reach the gate where they are collected, thus generating an excess leakage current. Consequently, two parameters are of a prime importance on the high voltage behavior of

the HEMTs. They are the band-gap (E_g) of the channel material that mainly determines the impact ionization rate, and the energy barrier seen by the holes created in the channel (E_B) in their path toward the gate. In order to prevent this leakage, several improvements of the structure design were proposed which all tend to either minimize the ionization mechanism in the small band-gap InGaAs channel or to increase the holes barrier. There are several methods to decrease the leakage current and improve the breakdown voltage, which are described as following.

(a) The reduction of the channel thickness leads to a larger gap by quantization effects.

(b) A suitable channel design reduces the electric field in the channel.

(c) An Al-rich InAlAs spacer or an InGaP spacer increases the hole barrier [9].

(d) Different gate metal will lead to different barrier height.

(e) Mesa sidewall etch will reduce the gate leakage current and improve the breakdown voltage.

InAlAs/InGaAs HFETs fabricated by conventional mesa isolation have a potential parasitic gate leakage path where the gate metallization overlaps the exposed channel edge at the mesa sidewall. The parasitic gate leakage path is formed by the low Schottky contact of the exposed channel edge with the gate metallization. It has been proven that the existence of this path by fabricating special heterojunction diodes with different mesa sidewall gate metal overlap lengths. The sidewall leakage current is a function of the crystallographic of the sidewall, and increase with channel thickness, sidewall overlap area, and InAs mole fraction in the channel. In HFETs fabricated alongside the diode, sidewall leakage

increased the subthreshold and forward gate leakage currents, which will lead to the reduction of the breakdown voltage [10].

3.5 Extrinsic transconductance (g_m)

The transconductance of the HEMTs indicates the ability of the gate voltage on the control of the drain current. It can be defined as：

$$g_m = \frac{dI_D}{dV_G} = \frac{\varepsilon_2}{d_2} Z_G v_{sat}$$

(7)

where the v_{sat} is the electron velocity of the "two dimensional electron gas" (2-DEG).

The measurement requires specification of the initial gate voltage, the gate voltage step, and the drain voltage at which the measurement is made. Because of the nonlinear behavior of source-drain current as a function of gate voltage, g_m typically will become less as the bias approaches pinch-off approaches. This also means that a smaller voltage step will yield a higher transconductance. The extrinsic transconductance is a function of the total gate width of the device, so the width must also be given. Besides, g_m may also be normalized to a unit gate width, usually mmho/mm.

3.6 Unit current gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max})

The intrinsic device model for the HEMT device is shown in Figure 3-7. If we only consider the intrinsic part, the current can be expressed as：

$$i_1' = y_{11}'V_1' + y_{12}'V_2'$$
$$i_2' = y_{21}'V_1' + y_{22}'V_2'$$

(8)

assume $(\omega C_{gs}R_i)^2 \ll 1$, then we can get：

$$y_{11}' = \omega^2 C_{gs}^2 R_i + j\omega(C_{gs} + C_{gd})$$
$$y_{12}' = -j\omega C_{gd}$$
$$y_{21}' = G_m - j\omega(C_{gd} + C_{gs}G_m)$$
$$y_{22}' = G_d + j\omega(C_{gd} + C_{ds})$$
$$\frac{i_2'}{i_1'} = \frac{y_{21}'}{y_{11}'} = \frac{G_m - j\omega(C_{gd} + C_{gs}R_iG_m)}{\omega^2 C_{gs}^2 R_i + j\omega(C_{gs} + C_{gd})}$$

(9)

assume
$$G_m \gg |\omega(C_{gd} + C_{gs}R_iG_m)|$$
$$\omega(C_{gs} + C_{gd}) \gg \omega^2 C_{gs}^2 R_i$$

f_T is defined as the frequency when current gain $\frac{i_2'}{i_1'} = 1$, and can be expressed as：

$$f_T \cong \frac{G_m}{2\pi(C_{gs} + C_{gd})}$$

(10)

f_{max} can be obtained by using unilateral gain：

$$U = G_{U\,max} = \frac{|y_{21}' - y_{12}'|^2}{4\,\mathrm{Re}(y_{11}')\,\mathrm{Re}(y_{22}')}$$
$$= \frac{1}{4}\frac{1}{f^2}\left(\frac{G_m}{2\pi C_{gs}}\right)^2 \frac{1}{R_iG_d}$$
$$= \frac{1}{4}\frac{f_T^2}{f^2}\frac{1}{R_iG_d}$$

(11)

when U=1, f_{max} can be expressed as：

$$f_{max} = \frac{f_T}{2\sqrt{R_i G_d}} \tag{12}$$

If we further consider gate resistance R_g, ohmic contact resistance R_s and R_d, then the small signal equivalent circuit is shown as Figure 3-8.

assume $(\omega C_{gs} R_i)^2 \ll 1$

$\qquad G_m \gg | \omega(C_{gd} + C_{gs} R_i G_m) |$

$\qquad \omega(C_{gs} + C_{gd}) \gg \omega^2 C_{gs}^2 R_i$

$\qquad G_m \gg | G_d + j\omega(C_{gd} + C_{ds}) |$

then $\qquad |Y'| = y_{11}' y_{22}' - y_{12}' y_{21}' \cong j\omega C_{gd} G_m$

Transfer y parameter into Z parameter：

$$Z_{11} = \frac{y_{22}'}{|Y'|} + R_g + R_s$$

$$Z_{12} = \frac{-y_{12}'}{|Y'|} + R_s$$

$$Z_{21} = \frac{-y_{21}'}{|Y'|} + R_s$$

$$Z_{22} = \frac{y_{11}'}{|Y'|} + R_d + R_s$$

and $\qquad |Z| = Z_{11} Z_{22} - Z_{12} Z_{21}$

$$\frac{i_2}{i_1} = \frac{y_{21}}{y_{11}} = \frac{\dfrac{Z_{21}}{|Z|}}{\dfrac{Z_{22}}{|Z|}} = \frac{-y_{21} + R_s |Y|}{y_{11} + (R_d + R_s)|Y|}$$

$$= \frac{-G_m + R_s \left\{ [j\omega(C_{gs} + C_{gd})][G_d + j\omega(C_{gd} + C_{ds})] + j\omega C_{gd} G_m \right\}}{j\omega(C_{gs} + C_{gd}) + (R_d + R_s)\left\{ [j\omega(C_{gs} + C_{gd})][G_d + j\omega(C_{gd} + C_{ds})] + j\omega C_{gd} G_m \right\}}$$

$$\frac{i_2}{i_1} \cong \frac{G_m}{j\omega(C_{gs} + C_{gd}) + (R_d + R_s)\left\{ [j\omega(C_{gs} + C_{gd})]G_d + j\omega C_{gd} G_m \right\}}$$

$$f_T \cong \frac{G_m}{2\pi\left\{ (C_{gs} + C_{gd})[1 + (R_d + R_s)G_d] + C_{gd} G_m (R_d + R_s) \right\}} \tag{13}$$

and we can get f_{max} [5]：

$$f_{\max} = \frac{f_T}{\sqrt{4\dfrac{G_d}{G_m}(G_m R_i + \dfrac{R_s + R_g}{1/G_m + R_s}) + \dfrac{4}{5}\dfrac{C_{gd}}{C_{gs}}(1 + \dfrac{2.5C_{gd}}{C_{gs}})(1 + G_m R_s)^2}} \qquad (14)$$

f_T and $f_{\max}$ are parameters often used to indicate the high frequency capability of the transistors.
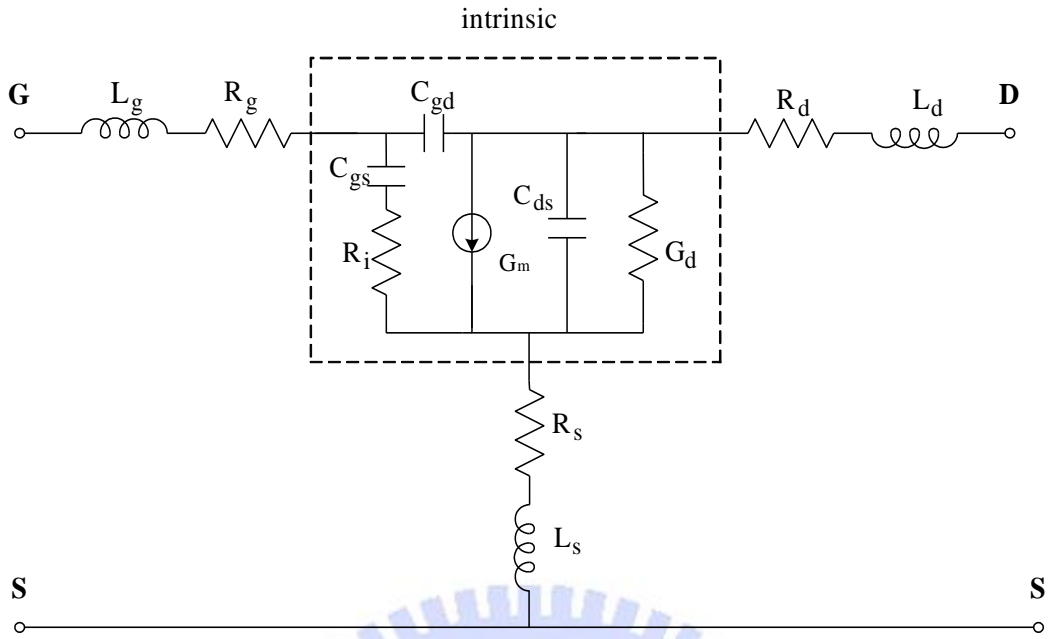
Fig. 3-1 PHEMT small signal device model
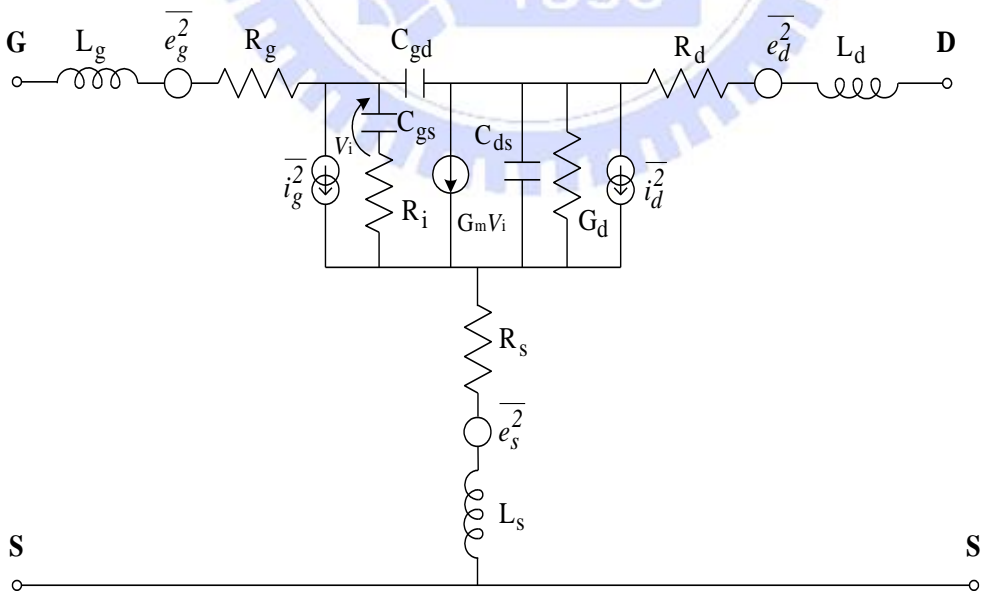
Fig. 3-2 PHEMT equivalent circuit with noise source
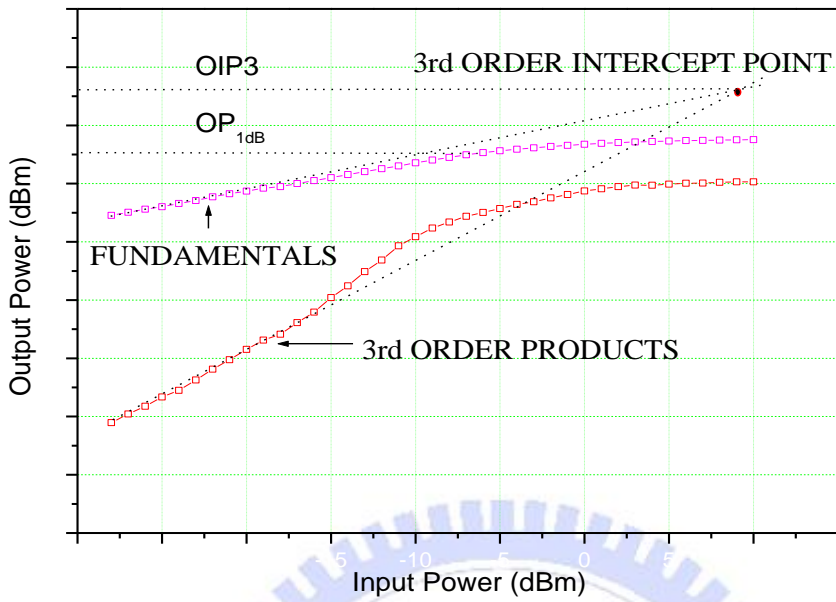
Fig. 3-3 Output power diagram of fundamental andthird-order product

signals
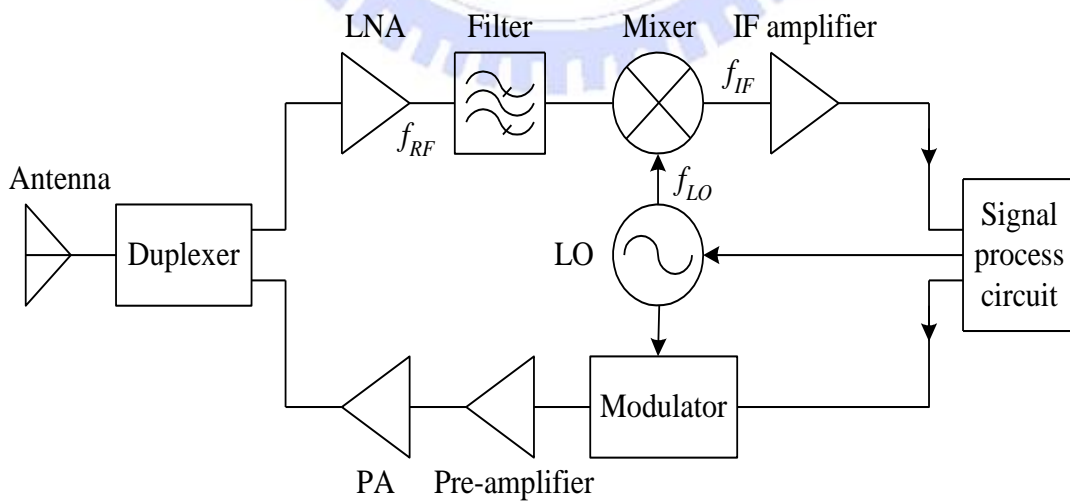
Fig. 3-4 Fundamental diagram of the microwave front-end device
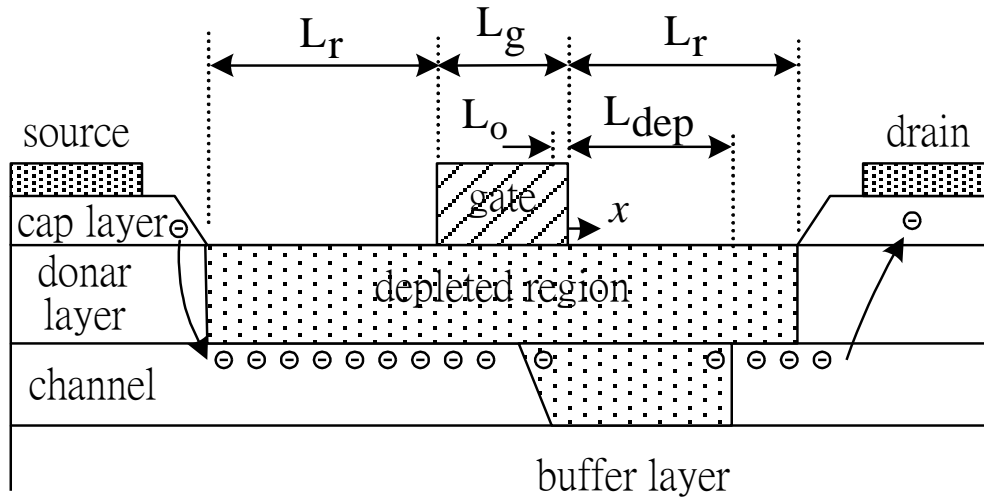
Fig. 3-5 A schematic cross-section of the InAlAs/InGaAs PHEMT
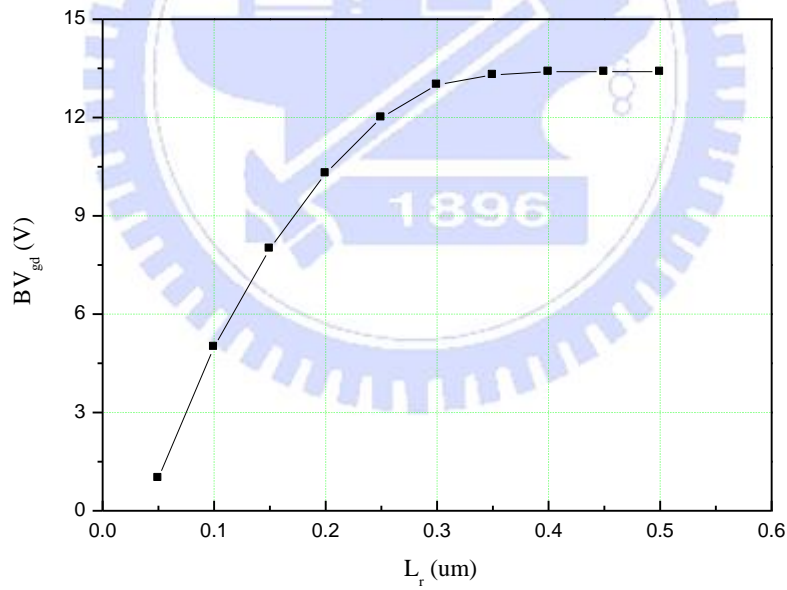
Fig. 3-6 Dependence of the breakdown voltage (BV_{gd}) on the gate recess width
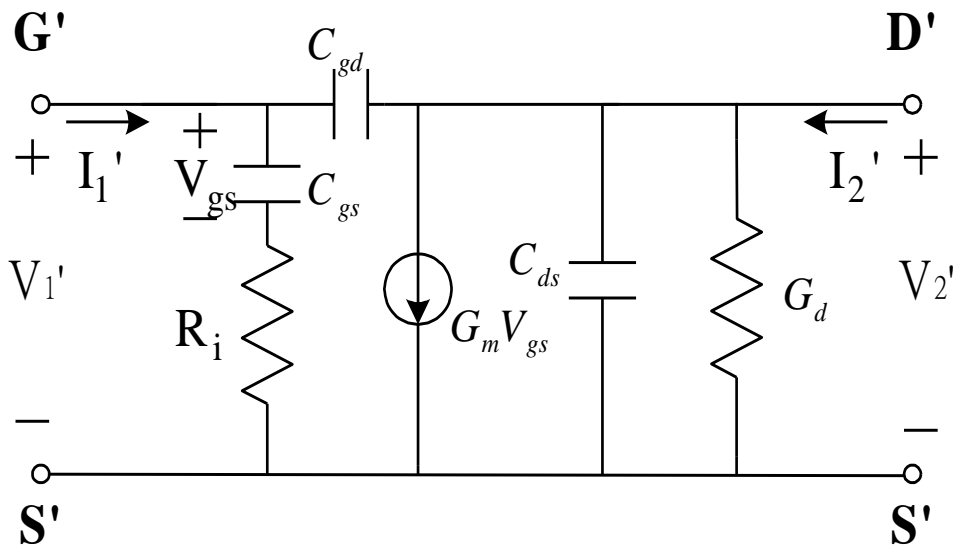
Fig. 3-7 PHEMT intrinsic device model
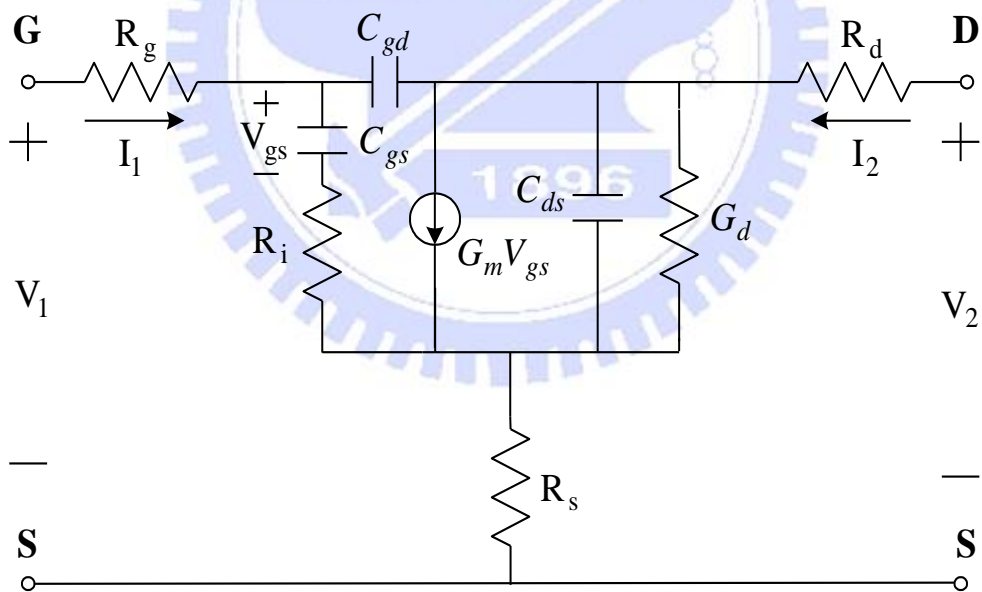
Fig. 3-8 PHEMT small signal equivalent circuit

Chapter 4
RF and Digital Performance of HEMTs with Different Doping Profiles

4.1 Introduction

For high frequency wireless communication, as the density in information traffic increasing, the requirements of device linearity become more demanding. In addition, the device linearity could be improved by varying the doping profiles. The device linearity of InGaP/InGaAs HEMTs with different doping profiles will be discussed in this chapter.

InGaP/In$_{0.22}$Ga$_{0.78}$As pseudomorphic high electron mobility transistors (PHEMTs) have been widely discussed for the radio frequency (RF) applications[10-12]. Unlike general AlGaAs Schottky layer forms a deep-complex (DX) center at the desired doping level, wider band gap InGaP presents better insulating property. Moreover, the high etching selectivity between InGaP and GaAs can be achieved, which improves the uniformity of gate recess[13].

For digital applications, endowed with smaller lattice constant compared to In$_{0.7}$Ga$_{0.3}$As and InAs, In$_{0.22}$Ga$_{0.78}$As displays relatively higher possibility to integrate with Silicon. Due to the lower mobility of In$_{0.22}$Ga$_{0.78}$As, various doping methods are employed for performance

reinforcement.

4.2 Device Fabrication

The epitaxial layers of the InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs were grown by metal-organic chemical vapor deposition (MOCVD) on GaAs substrate along the (100) axis. The schematic cross-sectional view of our InGaP/In$_{0.22}$Ga$_{0.78}$As HEMT structure with various doping profiles are shown in Fig. 4-1~4-3.

Fig. 4-1 shows the illustration of δ-doped InGaP/In$_{0.2}$Ga$_{0.78}$ As HEMT which consists of , from bottom to top, GaAs buffer layer, AlGaAs barrier layer, δ-doped carrier supply layer with Si doping concentration of 4.0×10^{12}/cm^2 which provides carriers, AlGaAs spacer layer, δ-doped carrier supply layer, InGaP Schottky layer and n-GaAs cap layer with Si doping concentration of 3.0×10^{12}/cm^3. It is worth noticing that the upper barrier material is InGaP which is different from the lower AlGaAs. The former has wider band-gap leading to higher breakdown voltage, and the later AlGaAs/InGaAs hetero-junction causes higher g$_m$ value than that with InGaP spacer.

Fig. 4-2 exhibits the structure of InGaP/In$_{0.22}$Ga$_{0.78}$As HEMT with uniformly-doping profile which indicates the carriers are doped in the Schottky layer. Other layers are as the same as the δ-doped for comparison. Fig. 4-3 shows the diagram of channel-doped InGaP/In$_{0.22}$Ga$_{0.78}$As HEMT. The carriers are supplied by Si δ-doped layer and lightly doped channel with concentration of 4.0×10^{12}/cm^3.

The detailed manufacturing process on the $InGaP/In_{0.22}Ga_{0.78}As$ HEMT devices are described at the following sections. Besides, the three kinds of devices HEMTs were fabricated by the same process flow for comparison. The flow chart of the process for device fabrication is illustrated in Fig. 4-4.

4.2.1 Wafer cleaning

The purpose of wafer cleaning is to remove undesirable impurities and particles on the surface. The wafers were immersed in Acetone (ACE) and isopropyl alcohol (IPA) each for five minutes, and blown dry by nitrogen gas.

4.2.2 Mesa isolation

The active region of devices is defined by S1818 photoresist, and other potions were wet etched to the buffer layer. The mesa isolation was carried out by $HF:H_2O_2:H_2O$ (5:1:40) solution to etch the GaAs cap layer, and $HCl:H_2O$ (1:1) solution to etch the InGaP Schottky layer. Then, the etching depth will reach about 4000Å by utilizing $HF:H_2O_2:H_2O$ solution again. The etching depth is measured by α-step measurement.

4.2.3 Ohmic formation

A low contact resistance junction is formed between the ohmic metal (Au/Ge/Ni/Au) and the cap layer, where germanium is used for doping GaAs during alloy, and nickel acts as a wetting agent in order to prevent the AuGe metal from "balling up".

The ohmic contact region is defined by AZ5214E photoresist with undercut profile. The wafers are dipped in 20% HCl solution for 15 seconds to remove the native oxide. Ohmic metal was then deposited on the substrates by using an electron-beam evaporator at a pressure of ~1×10^{-6} Torr. After ACE lift-off procedure, the wafer was thermally alloyed at 340℃ for 30 seconds by using rapid thermal anneal (RTA) system. After all, the contact resistance is obtained via measuring the transmission line method (TLM), and the specific contact resistivity is 1.9176×10^{-6} $\Omega\,cm^2$.

4.2.4 Recess and gate formation

The double gate recess process is used here.

The 1st recess slot was defined by e-beam photolithography to form the pattern defined by copolymer photoresist. Citric acid (C.A.) based solution (CA:H_2O_2:H_2O) was used to etch the cap layer, and HCl based solution (HCl:H_2O) was used to etch the InGaP shottky layer until it reaches the target current which was confirmed by measuring the drain-to-source current.

For high speed application, short gate length with low gate resistance is desired. The T-shaped gate structure is the most common approach for

obtaining low gate resistance. In the T-gate structure design, the gate length is defined by the small footprint and the wide top offers low gate resistance.

After removing the 1st recess photo-resist, the gate openings are defined by e-beam lithography to form the T-shaped profile consisting of Copolymer/PMMA/Copolymer to obtain a T-gate. Then, the HCl based solution was used to execute the 2nd recess, which can further increase the breakdown voltage. After that, the wafers are dipped in the 20% HCl solution for 15 seconds to remove the native oxide fallowed by depositing Ti/Pt/Au by e-gun evaporation system, where Titanium provides good adhesion to substrate, platinum acts as a barrier to prevent gold diffusing into GaAs, and gold provides high electrical conductivity. Finally, the wafer was immersed into ACE to lift-off the undesired metal. As the result, the gate length of the InGaP HEMT in this chapter is 0.3μm.

4.2.5 Device passivation

In order to protect the devices from environmental contamination and mechanical damages, the silicon nitride film (SiN_X) was formed by PECVD. The wafer was first dipped in the solution of $NH_4OH:H_2O=1:50$ for 10 seconds to clean the surface and decrease the surface dangling bonds. The silicon nitride film was grown at 250℃. RF power was 35W, and the precursors were SiH_4/Ar, NH_3 and N_2. The film thickness was about 1000Å and its refractive index was about 2.0, which were measured by ellipsometer.

After the passivation process, the contact via was defined for interconnections. Then the silicon nitride film was etched by reactive ion etching (RIE) system. The reactive plasmas are CF_4 and O_2, the RF power is 80W, and the pressure is 60 mtorr.

4.2.6 Air-bridge plating

Electrical plating is usually the last major step of the front-side process, and plated air-bridges are commonly used in GaAs devices and MMICs to interconnect source pads of the HEMTs.

First, a layer of photo-resist was spun and patterned to open areas over metal pads. Then, a thin coating of Ti/Au/Ti was applied to the entire wafer, where Titanium is deposited to improve the adhesion. The thin metal layer can conduct the plating current to the whole wafer. Next, a second coating of photo-resist was applied and patterned. Then the wafer was electroplated with gold for 2μm thickness. After plating, the top resist layer, thin Ti/Au/Ti metal, and lower resist layer were removed individually, leaving only the plated air-bridge.

4.3 Results and Discussion

4.3.1 Devices for RF applications

Three different types of 0.25μm × 160μm InGaP/InGaAs HEMTs are shown in Fig.4-1~4-3 were fabricated, tested and compared. Fig. 4-5 shows the I_{DS} vs. V_{DS} curves of the three different types of devices. For Comparing these devices, those different types devices have designed with similar I_{DSS} (I_{DS} @ V_{GS} = 0V) and pinch off voltage. The characteristics of the Gm dependence on the gate bias are shown in Fig. 4-6(a). It can be observed that extra doping in the channel and using uniformly-doped will result in device flatter Gm distribution, but both have lower maximum Gm value as compared to the conventionalδdoped device. The I_{DS}-V_{GS} curve comparison of these devices is shown in Fig. 4-6(b). The channel doped device has a maximum I_{DS} value of 634.3mA/mm which is higher than the others. The DC characteristics of these three 0.25 um × 160 um devices are compared in Table I.

To evaluate the device linearity, IP3 of these devices were measured. The IP3 measurements were carried out by injecting two signals with the same amplitude but at two different frequencies: 5.8 GHz and 5.801GHz, with the devices biased at V_{DS} = 1.5V, and adjust the I_{DS} to get the IP3 vs. I_{DS} curve. Fig. 4-7 shows the IP3 versus I_{DS} curves of these three different 0.25μm × 160μm devices, the load impedance was tuned for maximum

power for each individual device. It shows that the channel doped and uniformly-doped devices have higher IP3 values. The uniformly-doped devices device has wider high IP3 region versus different I_{DS} The measured maximum IP3 of these devices are listed in Table 5-2. The tuning at Γ_{source} and Γ_{load} of the conventional δ doped, uniformly-doped and channel doped devices are $\Gamma_{source} = 0.50 \angle 56.7^o$, $0.05 \angle -176.17^o$, and $0.02 \angle -83.6^o$ and $\Gamma_{load} = 0.14 \angle 47.1^o$, $0.58 \angle 32.3^o$ and $0.51 \angle 56.0^o$ respectively. The uniformly-doped device shows higher IP3 of 22.19 dBm, and the channel doped device shows higher Δ(IP3-P_{1dB}) of 14.23 dB, and higher IP3 to DC power consumption ratio (IP3/P_{DC}) of 4.97 compared to other devices. Overall, the uniformly doped and channel doped device has higher value of figure of merit for device linearity. From the data in Fig.4-6 and Fig.4-7, it can be concluded that extra doping in the channel region or using uniformly-doped can achieves flatter Gm distribution versus V_{GS} bias and thus higher IP3 of these devices even though the conventional δ doped device exhibits higher peak Gm value.

4.3.2 Devices for Logic applications

For better logic performance, the reduction of gate-to-channel distance is of importance, and further recess is required to reduce the

depth. Electrical characteristics of the 0.3μm InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs with three different structures are plotted in Fig. 4-1~4-3 and analyzed under the bias condition that drain-to-source voltage (V$_{DS}$) is equal to 0.5 volts. Extrinsic transconductance (G$_m$) versus gate-to-source voltage (V$_{GS}$) curves are displayed in Fig.4-8. Among the devices, although the δ-doped one shows the highest peak G$_m$ of 308 mS/mm, the uniformly-doped one exhibits positive shift in the threshold voltage, leading to lower power dissipation. The peak G$_m$ of channel-doped one is compressed due to lightly doping in the channel.

Fig. 4-9 presents the subthreshold characteristics of the manufactured InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs at a V$_{DS}$ of 0.5volts. The lowest off-state current is determined by the gate leakage current, which indicates the well insulating property of the δ-doped device. It is worth noticing that the uniformly-doped device reveals sharpest subthreshold slope, contributing to better logic performance.

The gate leakage current and the breakdown voltage diagram are illustrated in Fig. 4-10 and 4-11. Due to the good insulating property, the δ-doped InGaP/In$_{0.22}$Ga$_{0.78}$As device displays high gate-to-drain breakdown voltage (BV$_{DG}$) is 15 volts and low leakage current density of 10^{-4} mA/mm, which reaches the acquirements of logic gate (about 10^{-10} A/device). In addition, the BV$_{DG}$ of the uniformly-doped and channel-doped devices are 7.4 and 4.8 volts, respectively. Further insulating improvement are needed to reinforce for these two kinds of doping methods.

Table 4-3 lists the logic parameters of the three InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs with various doping profiles. All the parameters are defined as

the chapter 3 exhibits and measured at a V_{DS} of 0.5volts. In comparison with the δ-doped device, on the one hand, uniformly-doped device shows smaller subthreshold slope (SS) of 111mV/decade and higher I_{ON}/I_{OFF} ratio where implies that uniformly doping in the Schottky layer could sharpen the V_G-I_D curve; on the other hand, channel-doped device presents smaller drain induced barrier lowering (DIBL) of 78 mV/V where manifests that extra doing in the channel could help devices working at low bias point.

4.4 Conclusions

Electrical characteristics of the 3μm InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs with different doping profiles for low-power digital applications are illustrated. The δ-doped InGaP/In$_{0.22}$Ga$_{0.78}$As device presents possible large scale integration of devices, attributing to the well insulating properties. In addition, SS and I_{ON}/I_{OFF} ratio parameters can be improved by uniformly-doping in the Schottky layer; DIBL parameter can be reinforced by extra doping in the channel layer. However, further insulating layer should be applied to the uniformly-doped and channel-doped devices for preventing them suffering from the gate leakage problem.

Table 4-1 Comparison of the DC characteristics of the three different types of devices

Device Type			Conventional δ doped InGaP/InGaAs PHEMT	Channel doped InGaP/InGaAs PHEMT	Uniformly doped InGaP/InGaAs PHEMT
Doping density	Delta doping (cm^{-2})	above	4.0×10^{12}	4.0×10^{12}	undoped
		below	2.0×10^{12}	2.0×10^{12}	
	Channel doped (cm^{-3})		undoped	5.0×10^{17}	undoped
	Uniformly doped carrier layers (cm^{-3})	above	undoped	undoped	3.0×10^{18}
		below			2.0×10^{18}
I_{DSS} (I_{DS} @ V_{GS}=0, mA/mm)			356.9	359.6	361.0
I_{DS}-max (mA/mm)			509.3	634.3	589.9
Gm_{max} (mS/mm)			372.1	368.4	340.0
Pinch-off voltage			-1.25	-1.35	-1.4

Table 4-2 Comparison of the IP3 of the three different types of devices

Device Type	I_{DS} (mA)	DC bias point: V_{DS} = 1.5V			
		Operation frequency: 5.8GHz			
		P1dB (dBm)	IP3 (dBm)	Δ (IP3-P1dB) (dB)	IP3/PDC
Conventional delta-doped InGaP/InGaAs PHEMT	22.34	5.79	17.38	11.59	1.63
Uniformly- doped InGaP/InGaAs PHEMT	22.48	9.69	22.19	12.5	4.91
Channel doped InGaP/InGaAs PHEMT	16.96	6.79	21.02	14.23	4.97

Table 4-3 Logic parameters of the 0.3μm InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs

with different doping profiles

	Channel doped	Uniform doped	Delta doped
BV$_{GD}$ (V)	5	7	15
DIBL (mV/V)	78	111	134
SS (mV/dec)	166.7	111.1	150
I$_{on}$/I$_{off}$	~1000	~7000	~800
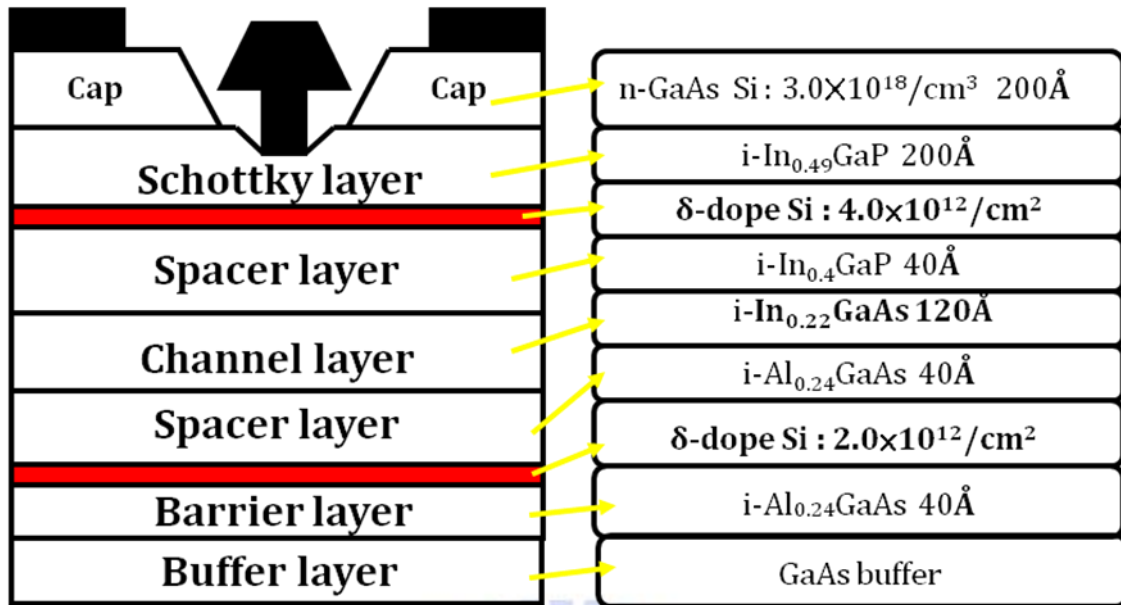
Fig. 4-1 Structure of δ-doped InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMT
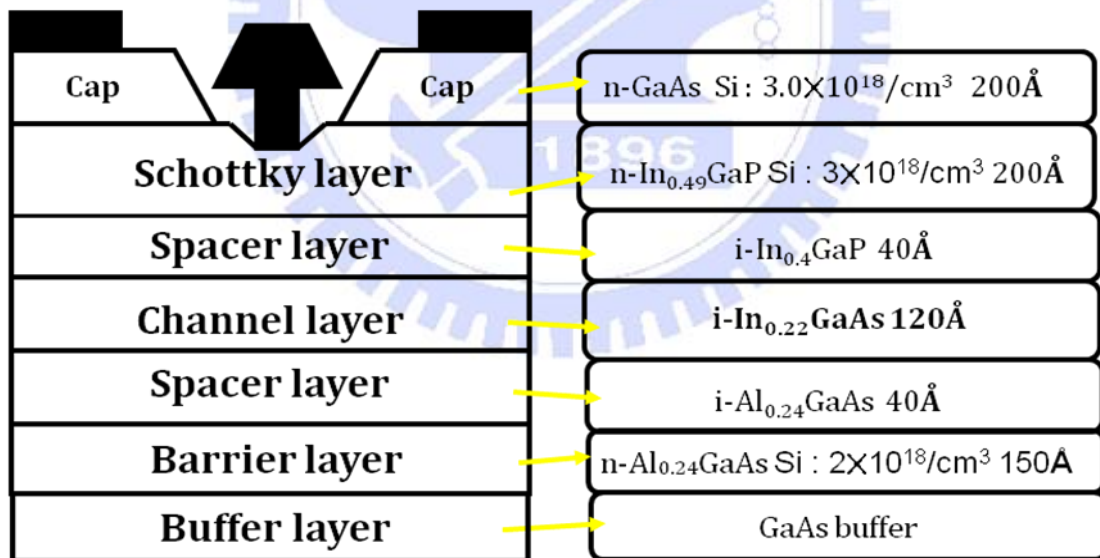
Fig. 4-2 Structure of uniformly-doped InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMT

Cap	n-GaAs Si : $3.0 \times 10^{18}/cm^3$ 200Å
Schottky layer	i-$In_{0.49}$GaP 200Å
	δ-dope Si : $4.0 \times 10^{12}/cm^2$
Spacer layer	i-$In_{0.4}$GaP 40Å
Channel layer	n-$In_{0.22}$GaAs Si : $4 \times 10^{18}/cm^3$ 120Å
	i-$Al_{0.24}$GaAs 40Å
Spacer layer	δ-dope Si : $2.0 \times 10^{12}/cm^2$
Barrier layer	i-$Al_{0.24}$GaAs 40Å
Buffer layer	GaAs buffer
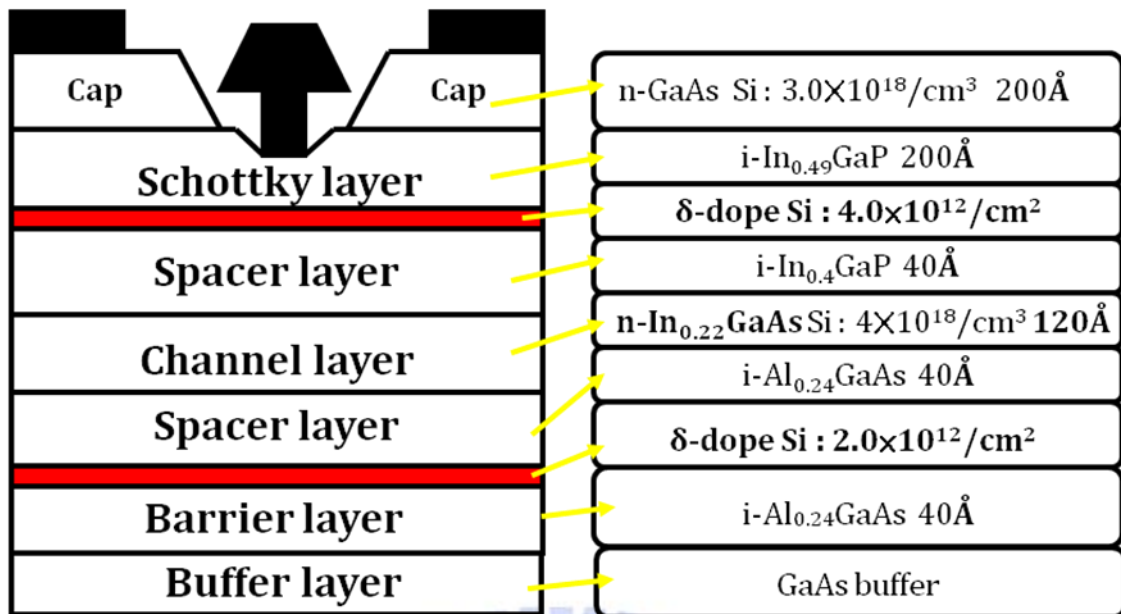
Fig. 4-3 Structure of channel-doped InGaP/$In_{0.22}$Ga$_{0.78}$As PHEMT

MESA → Ohmic → 1st recess → 2nd recess → T-gate formation → SiN$_x$ passivation → Nitride Via → Air-bridge
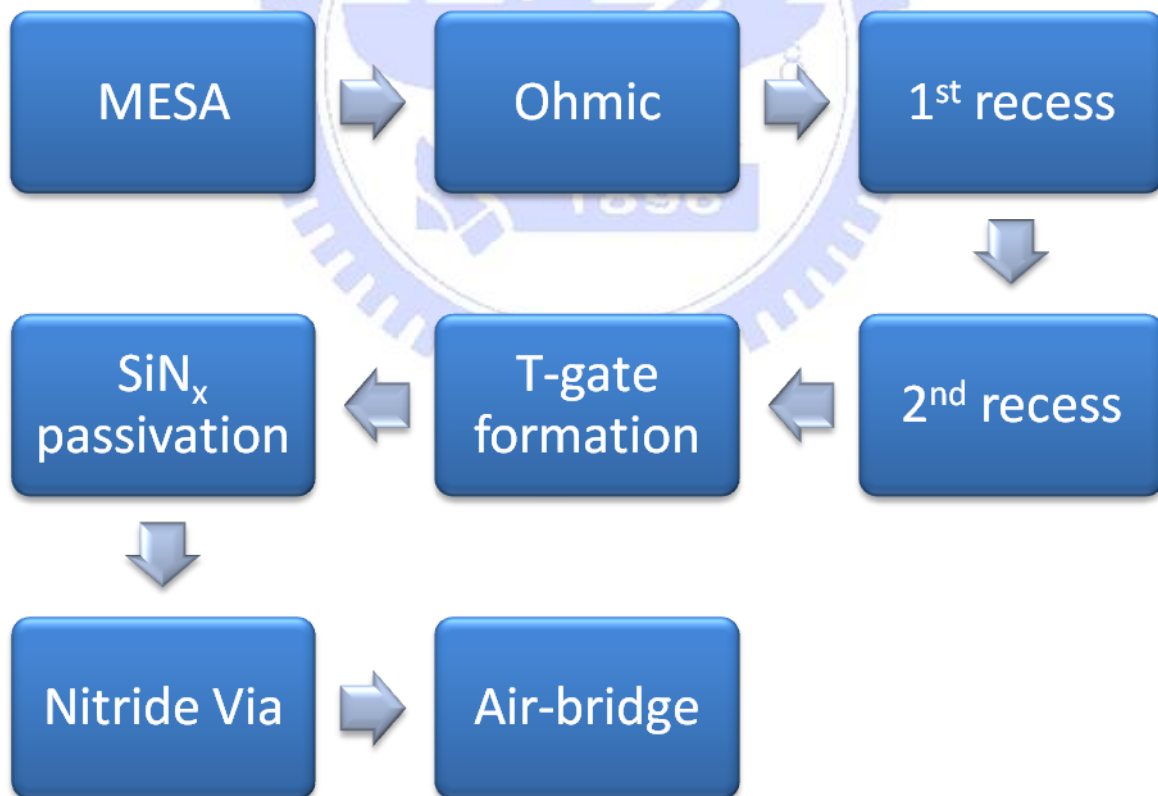
Fig. 4-4 Process flow of 0.3μm InGaP/$In_{0.22}$Ga$_{0.78}$As PHEMT
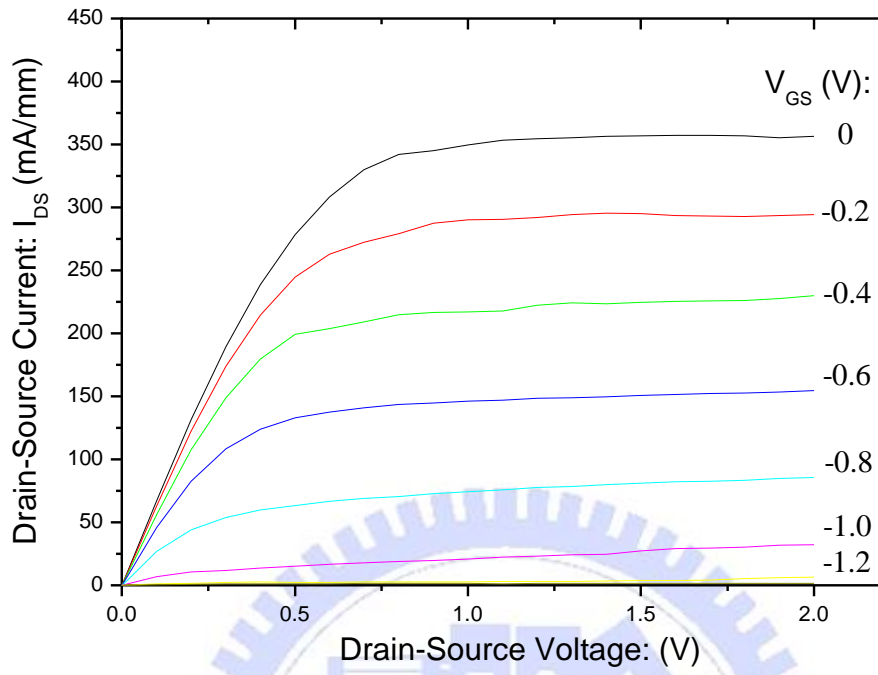
(a)
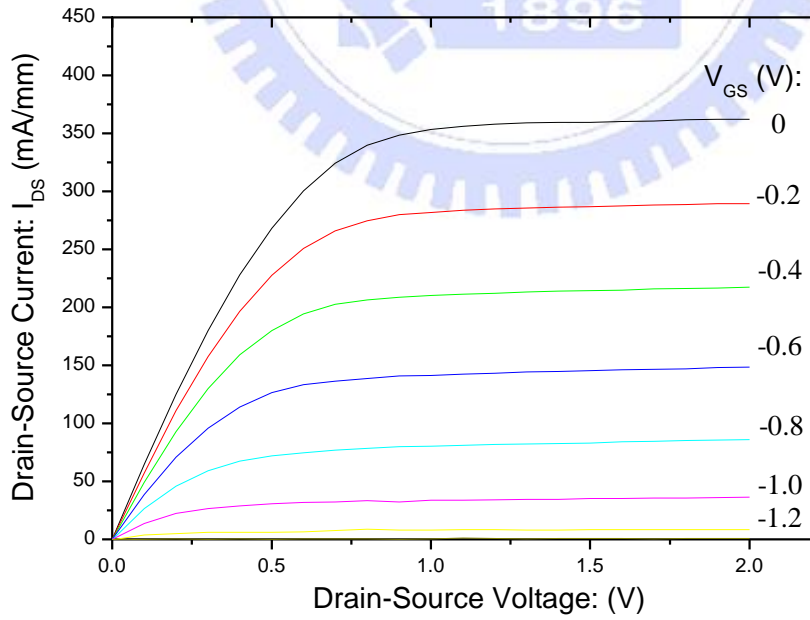
(b)
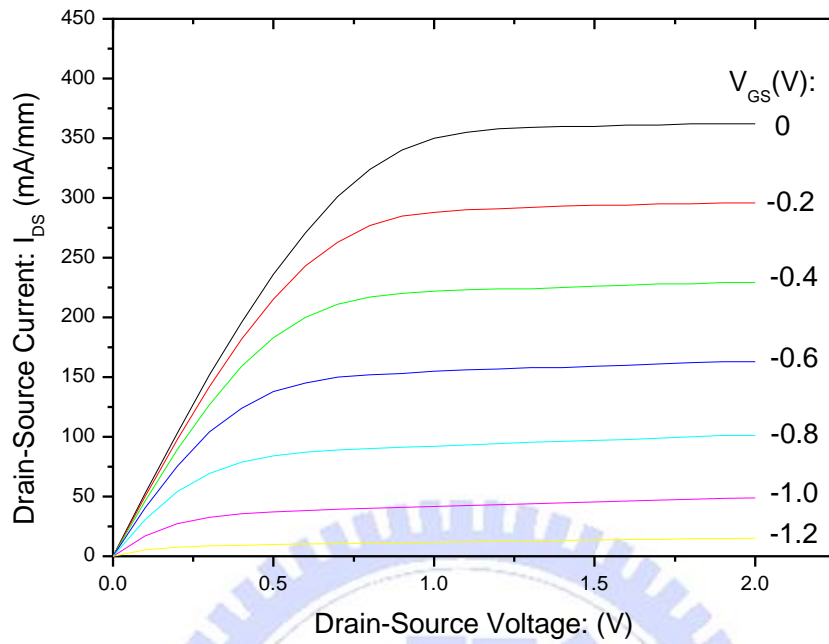
(c)

Fig. 4-5 I_{DS} vs. V_{DS} curves for the three different types of 0.25 x 160

μm^2 devices: (a)δ -doped device, (b) Channel doped PHEMT,

(c) Uniformly-doped PHEMT
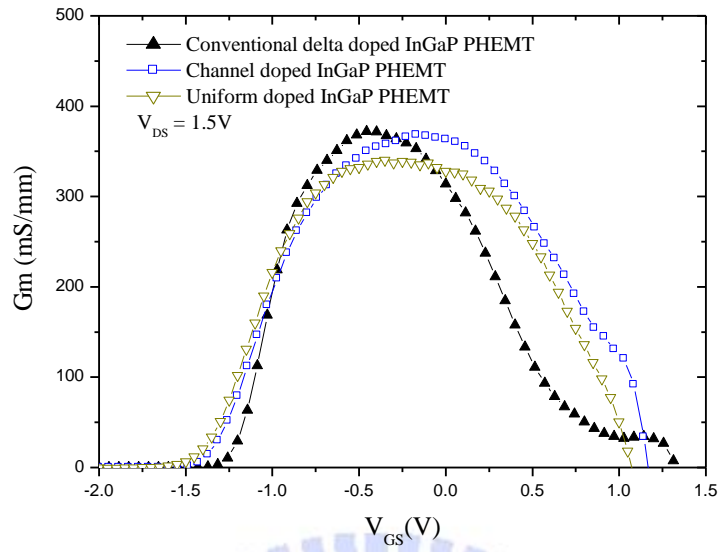
(a)
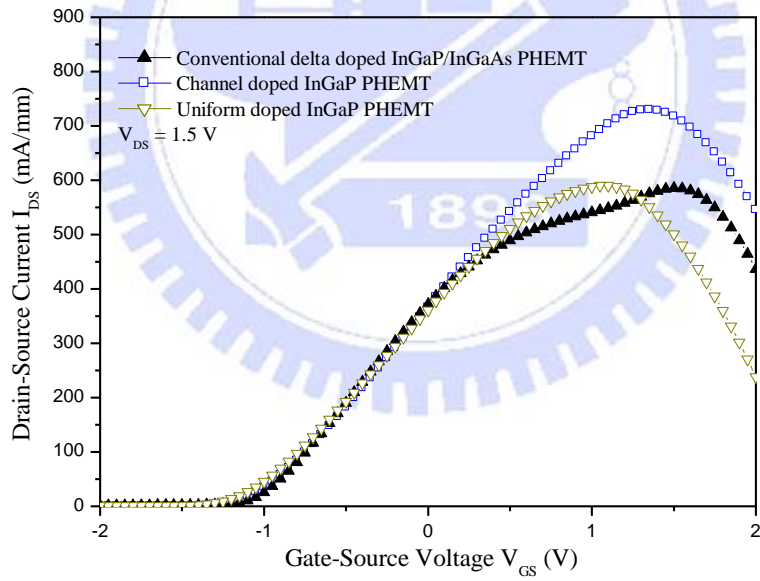
(b)

Fig. 4-6 (a) Extrinsic transconductance (G_m) vs. V_{GS} curves, (b) I_{DS} vs.

V_{GS} curves for the three different types of devices studied, the

device size is $0.25 \times 160 \ \mu m^2$ and the V_{DS} bias is 1.5V
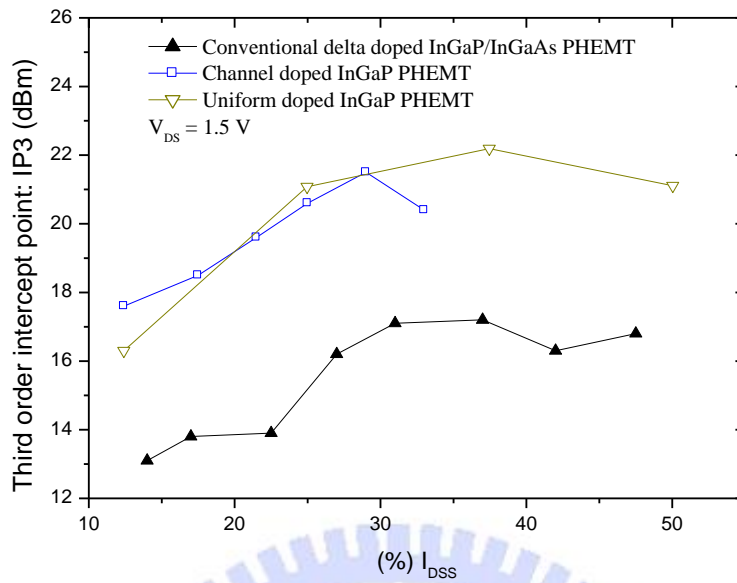
Fig. 4-7 IP3 vs. I_{DS} curves of the three $0.25 \times 160\mu$ m^2 InGaP/InGaAs

PHEMTs in this study, the test frequency is 5.8GHz and V_{DS} =

1.5V
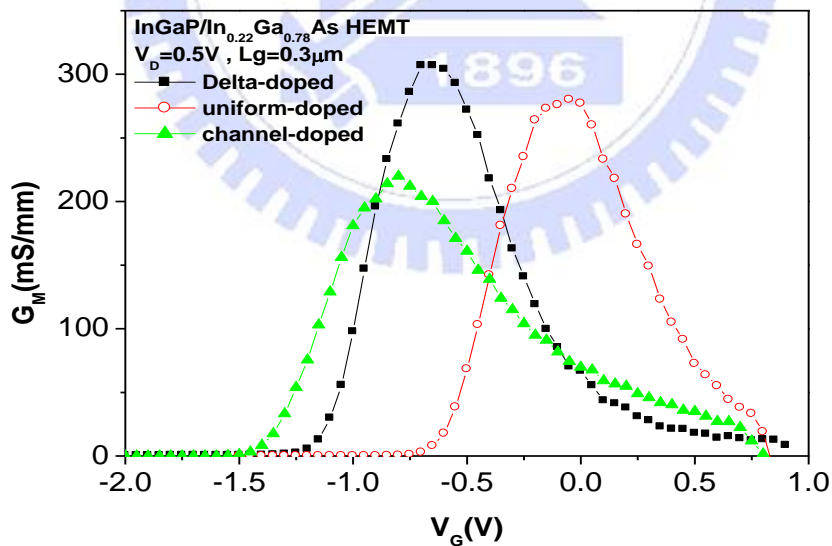
Fig. 4-8 Extrinsic transconductance (G_m) versus gate-to-source voltage

(V_{GS}) curves of the $0.3 \times 200\mu m^2$ InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMT
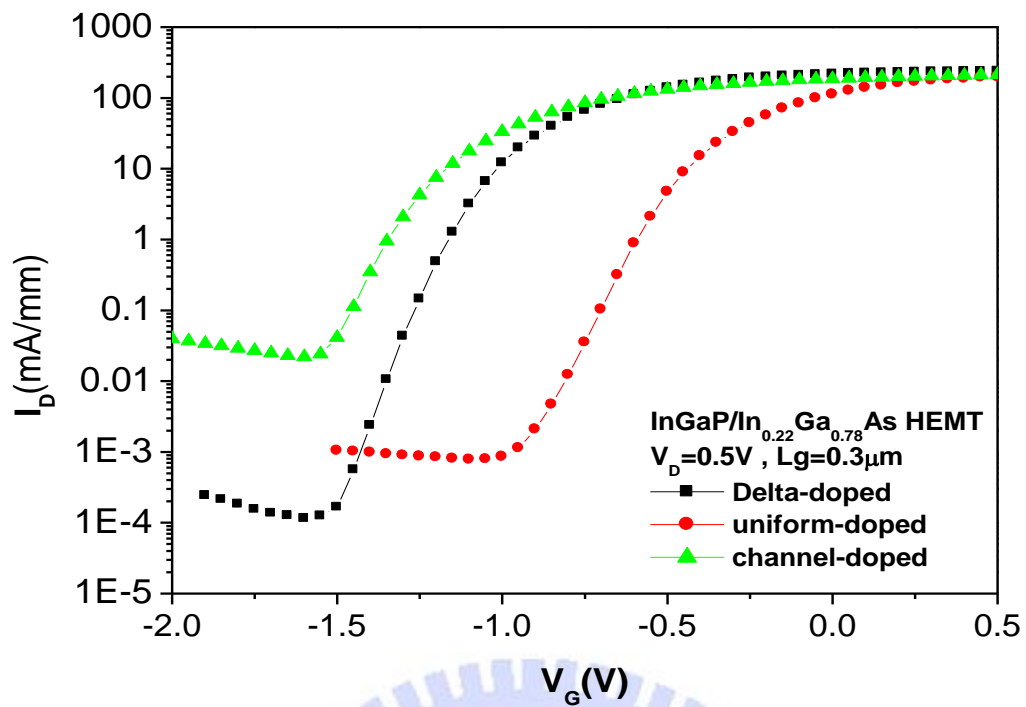
devices

Fig. 4-9 Subthreshold characteristics of the $0.3 \times 200 \mu m^2$ InGaP/ In$_{0.22}$Ga$_{0.78}$As PHEMT devices
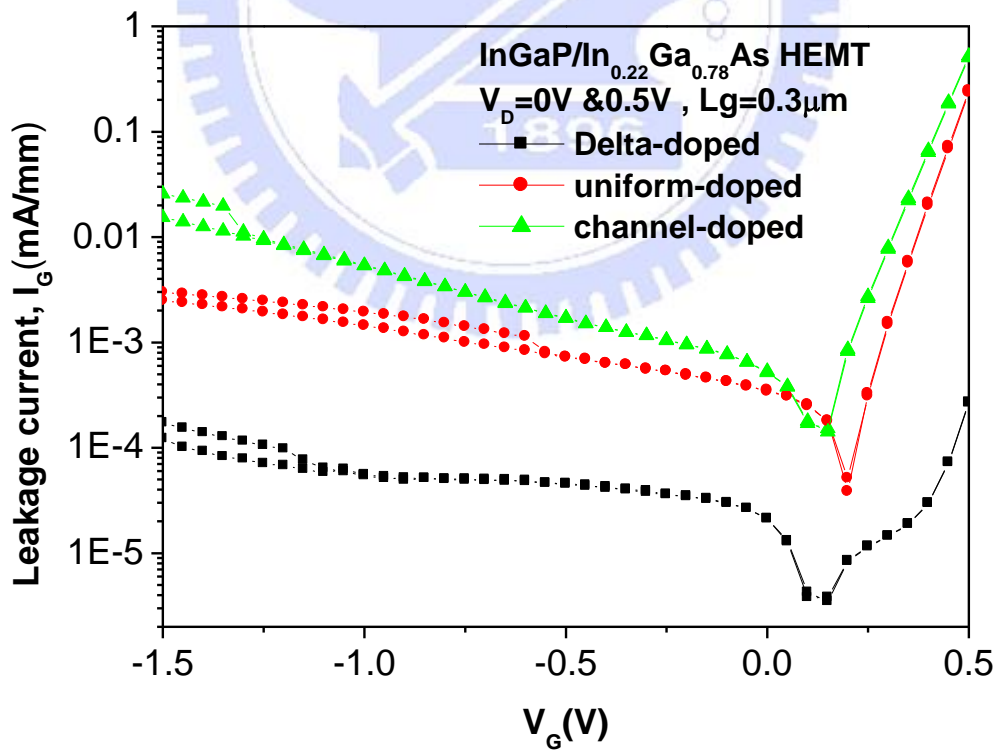
Fig. 4-10 Gate leakage current of the $0.3 \times 200 \mu m^2$ InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMT devices
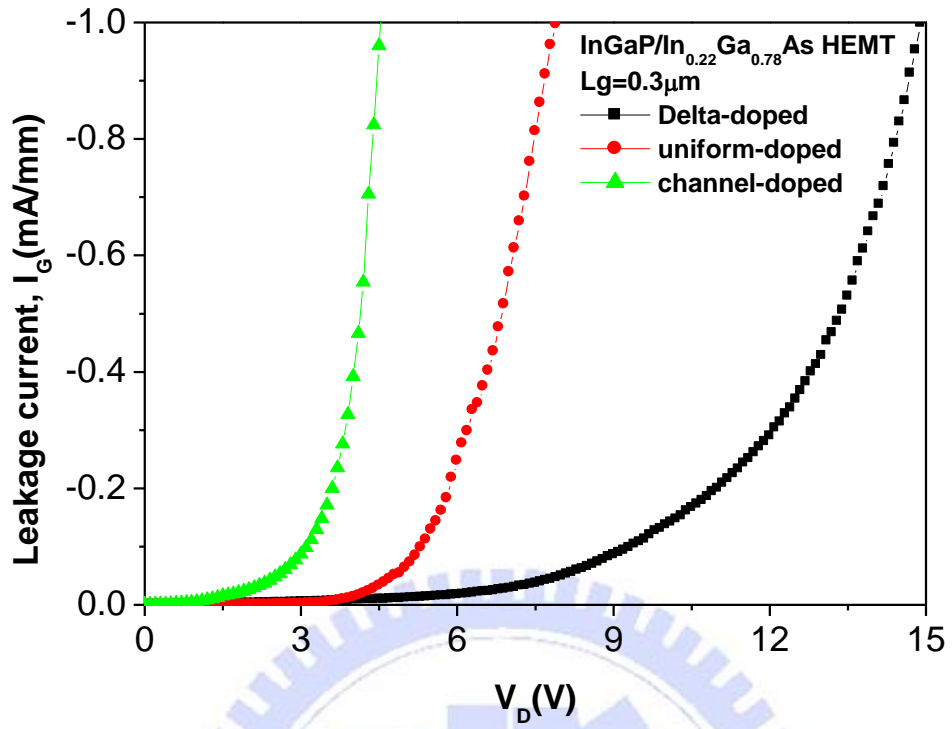
Fig. 4-11 Gate-to-drain breakdown voltage (BV_{DG}) of the $0.3 \times 200 \mu m^2$

InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMT devices

Chapter 5
Introducing Al_2O_3 as Gate Insulator for InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMTs Fabrication

5.1 Introduction

Considering HEMTs for digital applications, the InGaAs channel with high indium concentration is required for better performance and higher transconductance. Meanwhile, unlike the excellent insulating property of metal-oxide- semiconductor (MOS) structure in Si MOSFET, the Schottky gate in HEMT device suffers from high leakage current, which results in restricted input handling voltage. Furthermore, owing to this obstacle, these transistors could not be integrated in large scale. In order to reduce the gate leakage current, insulating layers were introduced into the gate formation, including high aluminum content native oxide of InAlP or InAlAs[6], ALD high-k dielectrics such as Al_2O_3[7] and HfO_2[8].

ALD Al_2O_3 is introduced in this study due to its relatively high band gap (about 8.7eV) and remains amorphous under typical processing conditions. In addition, Al_2O_3 also performs high breakdown electric field (5~20 MV/cm), high thermal stability (up to 1000℃) and strong adhesion with dissimilar materials[14]. With well-controlled thickness and uniform

Al$_2$O$_3$ layer deposited by ALD technology which employs surface saturation reaction technique, ALD Al$_2$O$_3$ is the leading candidate for the gate insulators in MOS-HEMT device. The comparison of other insulating material properties is shown in Table 5-1[15].

It is worth noticing that surface treatment is of importance to be handled before applying the insulating layers to restrain interface trap density which would cause the Fermi level pinning of the carriers. (NH$_4$)S$_X$ is convinced as a useful surface treatment solution and both Schottky capacitors and MOS devices are manufactured by several research groups[8, 13, 16]. Moreover, MOS-HEMT treated by (NH$_4$)S$_X$ have already been utilized for fabrication, which presents higher breakdown voltage and lower leakage current in comparison with conventional HEMTs[17].

In this study, we focus on the characteristics of the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMTs with ALD Al$_2$O$_3$ as the gate insulator and conventional HEMTs with the same structures will also be fabricated in order to make comparisons. Besides, including subthreshold slope (S), drain-induced barrier lowering (DIBL) and I$_{ON}$/I$_{OFF}$ ratio, above figures of merit (FOM) for logic application will also be exhibited to realize the logic potential of MOS-HEMTs.

5.2 Device Fabrication

The epitaxial layers of the InAlAs/In$_{0.7}$Ga$_{0.3}$As MHEMTs were grown by molecular beam epitaxy (MBE) on GaAs substrate. The

schematic cross-sectional view of our δ-doped InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMT structure is shown in Fig. 5-1.

Fig. 5-1 demonstrates the illustration of δ-doped InAlAs/In$_{0.7}$Ga$_{0.3}$As MHEMT which consists of , from bottom to top, InAlAs buffer layer, In$_{0.52}$Ga$_{0.48}$As/In$_{0.7}$Ga$_{0.3}$As/In$_{0.52}$Ga$_{0.48}$As composite channel, InAlAs spacer layer, δ-doped carrier supply layer with Si doping concentration of 5.0×10^{12}/cm^2, InP etching stop layer, InAlAs Schottky layer and n-InGaAs cap layer with Si doping concentration of 2.0×10^{19}/cm^3. It is worth noticing that the high etching selectivity between InP and InAlAs is of importance for device fabrication, attributing to the 1st recess is done before Ohmic formation due to the post-depositing annealing temperature of ALD Al$_2$O$_3$ is higher than the rapid thermal annealing temperature of the Ohmic metal.

The detailed manufacturing process on the InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMT device is described at the following sections. Besides, the conventional MHEMT is also fabricated by the same process flow for comparison. The flow chart of the process for device fabrication is illustrated in Fig. 5-2.

5.2.1 Wafer cleaning

The purpose of wafer cleaning is to remove undesirable impurities and particles on the surface. The wafers were immersed in Acetone (ACE) and isopropyl alcohol (IPA) each for five minutes, and blown dry by

nitrogen gas.

5.2.2 Mesa isolation

The active region of devices is defined by S1818 photoresist, and other potions were wet etched to the buffer layer. The mesa isolation was carried out by H_3PO_4:H_2O_2:H_2O (5:1:40) solution to etch the InGaAs cap layer and the InAlAs Schottky layer. HCl:H_2O (1:1) solution to etch the InP etching stop layer. Then, the etching depth will reach about 4000Å by utilizing H_3PO_4:H_2O_2:H_2O solution again. The etching depth is measured by α-step measurement.

5.2.3 1st recess

The gate recess slot was defined by S1818 photoresist to form the pattern. Succinic acid (SA) based solution (SA:H_2O_2:H_2O) was used to etch the cap layer and part of the InAlAs shottky layer.

5.2.4 Surface treatment

Surface treatment is of importance to be handled before applying the insulating layers to restrain interface trap density which would cause the undesired Fermi level pinning of the carriers. After the treatment, the native oxide is eliminated and a passivating thin film is formed on the top of the semiconductor, what prevents inner semiconductor react with

oxygen in atmosphere.

Here, we choose $(NH_4)S_X$ as our surface treatment solution. The HCl:H_2O (1:4) solution was applied for removing the native oxide, followed by dipping the wafer in $(NH_4)S_X$ for 30 minutes at 60℃. The depth of the passivating thin film can be determined by the immersing time and reacting temperature.

5.2.5 Atomic layer deposition (ALD) Al_2O_3

Compared with traditional MOCVD and PVD, ALD sufficiently employs surface saturation reactions, endowed with stability of width and depth control. The depth width ratio of 100:1 can be achieved with high density and high purity thin film. Unlike the process temperature of MOCVD which is handled at more than 500℃, the art of ALD could deposit thin film at less than 400℃.

The process temperature of ALD Al_2O_3 is 300℃, and the uniform Al_2O_3 layer is deposited for the depth of 12μm, followed by the post-deposition annealing (PDA) at 500℃.

5.2.6 Ohmic formation

The ohmic contact region is defined by AZ5214E photoresist with undercut profile. The wafers are dipped in HF: H_2O (1:10) for 1 minute to

remove the Al_2O_3, and 20% HCl solution for 15 seconds to remove the native oxide. Ohmic metal was then deposited on the substrates by using an electron-beam evaporator at a pressure of ~$1x10^{-6}$ Torr. After ACE lift-off procedure, the wafer was thermally alloyed at 240℃ for 30 seconds by using rapid thermal anneal (RTA) system. After all, the contact resistance is observed via measuring the transmission line method (TLM), and the specific contact resistivity is 3.2854×10^{-6} Ω cm^2.

5.2.7 Gate formation

The gate slot was defined by AZ6310 photoresist, and the wafers were then dipped in the 20% HCl solution for 15 seconds to remove the native oxide fallowed by depositing Ti/Pt/Au by e-gun evaporation system. Finally, the wafer was immersed into ACE to lift-off the undesired metal. As the result, the gate length of the $InAlAs/In_{0.7}Ga_{0.3}As$ MHEMTs in this chapter is 0.8μm.

5.3 Results and Discussion

Electrical characteristics of the 0.8μm $InAlAs/In_{0.7}Ga_{0.3}As$ MOS-MHEMT and conventional MHEMT are plotted and analyzed. Fig. 5-3 demonstrates the diagram of drain current (I_D) versus the drain voltage (V_D), which indicates that the saturation current of the MOS-MHEMT is reduced referring to the conventional MHEMT at the

same gate-to-source voltage (V_{GS}). The decline of the I_D reveals the reduction of carrier concentration within the channel affected by the oxide layer, attributing to the larger barrier height between the gate metal and Schottky layer. As the result, the electrical field in the channel between gate and drain is decreased, leading to the capability for biasing at higher V_D. Extrinsic transconductance (G_m) versus gate-to-source voltage (V_{GS}) curves are displayed in Fig.5-4. Due to the influence mentioned above, the G_m peak of the MOS-MHEMT is compressed from 215 mS/mm to 170 mS/mm.

The breakdown voltage diagram is illustrated in Fig. 5-5. At the beginning, the leakage current increases dramatically, where might caused by the defects of the MHEMT structure. However, the MOS-MHEMT displays smaller slope of the curve which implies the oxide layer could effectively decrease the leakage current. In addition, after introducing Al_2O_3 as gate insulator, the leakage current is reduced about one order, where is observed in the Fig. 5-6.

Table 5-2 summarizes the logic parameters of the InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMT and conventional MHEMT. All the parameters are defined as the chapter 3 exhibits and measured at a V_{DS} of 0.5volts. In comparison with the conventional MHEMT, MOS-MHEMT shows almost the same logic performance. The slightly larger subthreshold slope (SS) is due to the increase of the gate-to-channel distance which attributes to the insertion of the Al_2O_3 layer between the metal and Schottky layer. In addition, the worse drain induced barrier lowering (DIBL) value is because of the reduction of carrier concentration within the channel, contributing to the reduction of the

electric field. Therefore, MOS-HEMT requires larger bias voltage to function device, where manifests the decline of the DIBL parameter.

Overall, the MOS-MHEMT device not only displays fantastic insulating property but presents almost the same logic performance parameters in Gm, SS and DIBL without dramatically decreasing. Those results indicate the possibility of MOS-HEMT for logic application.

5.4 Conclusions

The 0.8μm InAlAs/$In_{0.7}Ga_{0.3}As$ MOS-MHEMT and conventional HEMT were fabricated, and the parameters for low-power digital applications were calculated for comparison. MOS-MHEMT exhibits better insulating property, meanwhile, the digital parameters are almost the same. That result leads to the possibility of InAlAs/$In_{0.7}Ga_{0.3}As$ MOS-MHEMT for digital utilization. Further gate length scaling down is necessary to improve the device performance.

Table 5-1 Comparison of relevant properties for high-K candidates

Material	Dielectric constant (k)	Band gap E_G (eV)	$\triangle E_C$ (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphorus
Si_3N_4	7	5.1	2	Amorphorus
Al_2O_3	9	8.7	2.8	Amorphorus
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal, cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhomic
TiO_2	80	3.5	1.2	Tetrag. (rutile, anatase)
HfO_2	25	5.7	1.5	Mono., tetrag., cubic
ZrO_2	25	7.8	1.4	Mono., tetrag., cubic

Mono. = monoclinic.
Tetrag. = tetragonal

Table 5-2 Logic parameters of the 0.8μm $InAlAs/In_{0.7}Ga_{0.3}As$ MOS-MHEMT and conventional HEMT

	MOS-HEMT	HEMT
DIBL (mV/V)	67	45
SS (mV/dec)	128	115
I_{on}/I_{off}	~1000	~1000
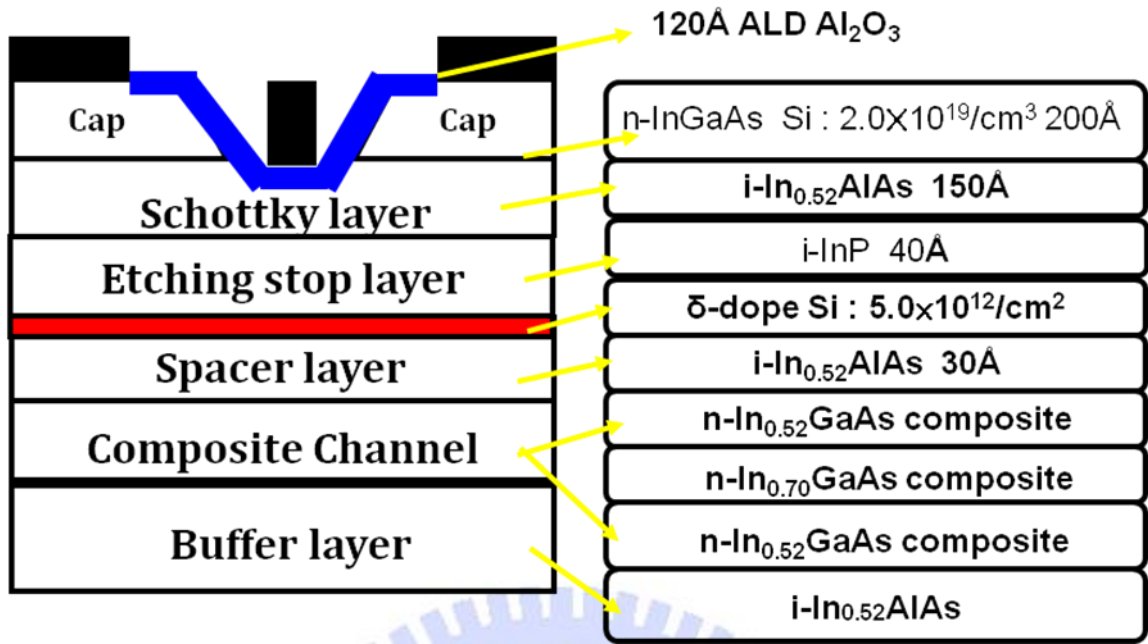
Fig. 5-1 Structure of 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT
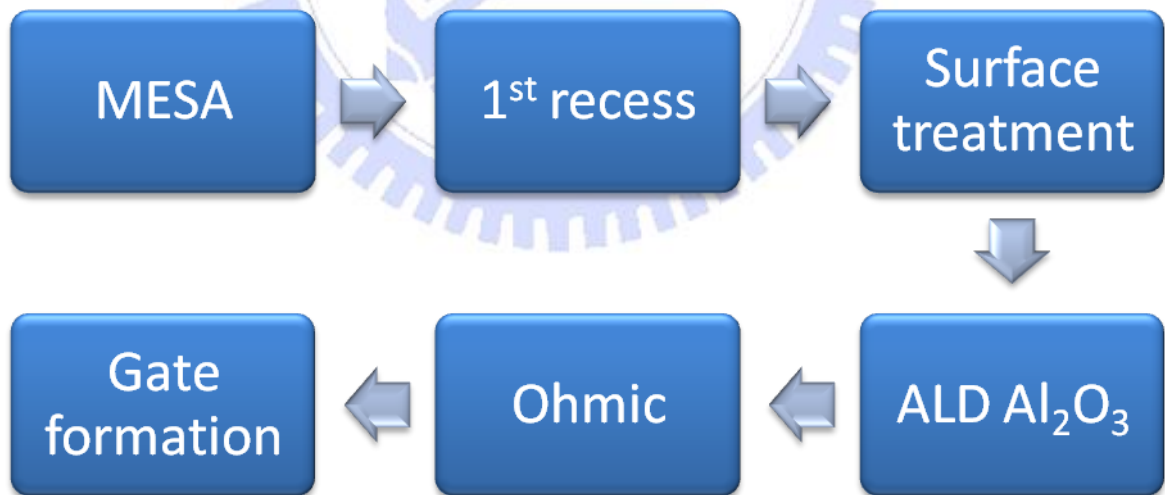
Fig. 5-2 Process flow of 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT
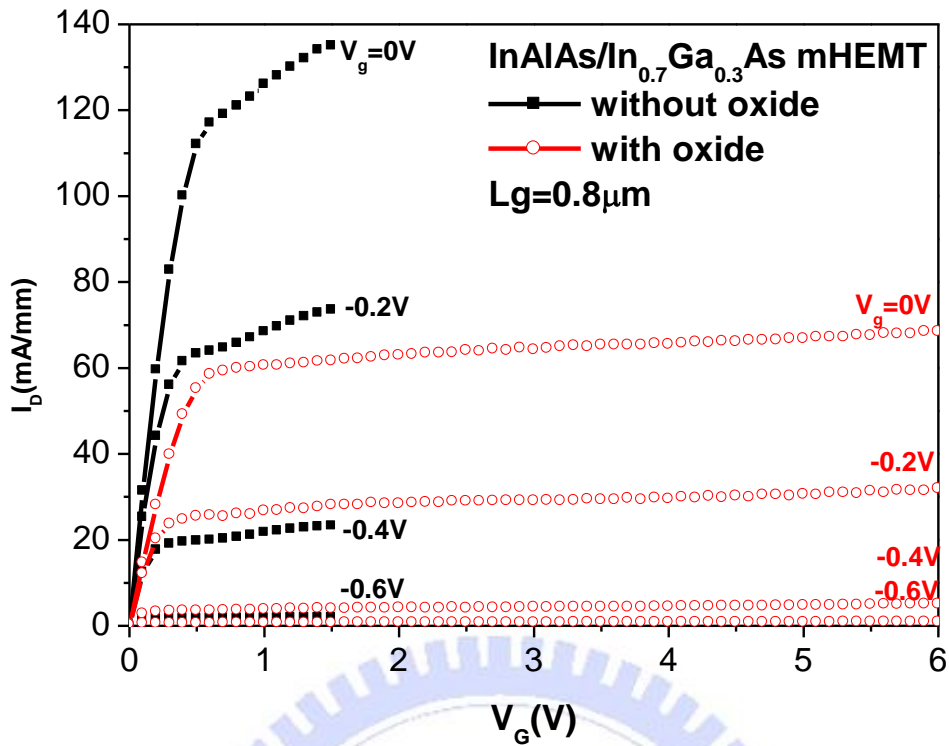
Fig. 5-3 Drain current (I_D) versus the drain voltage (V_D) curves of the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT and conventional HEMT
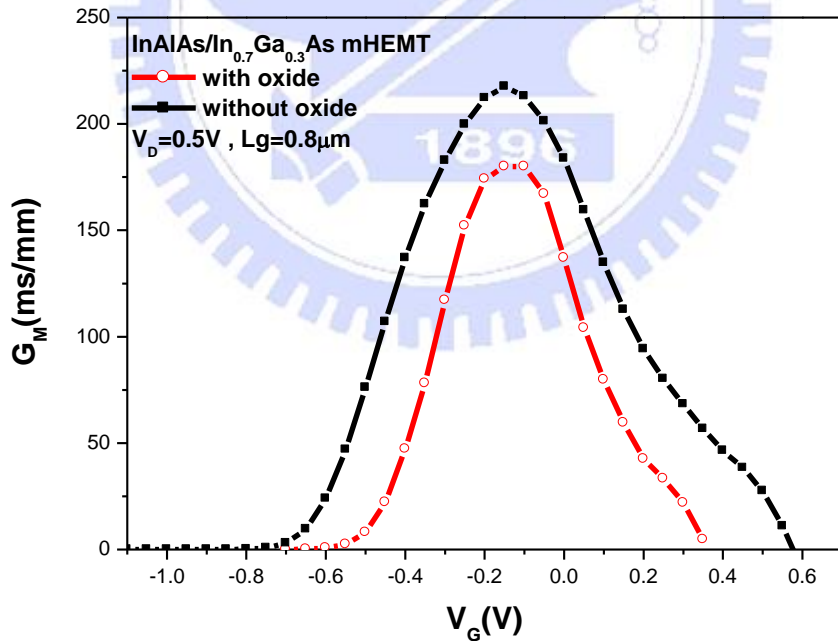
Fig. 5-4 Extrinsic transconductance (G_m) versus gate-to-source voltage (V_{GS}) curves of the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT and conventional HEMT
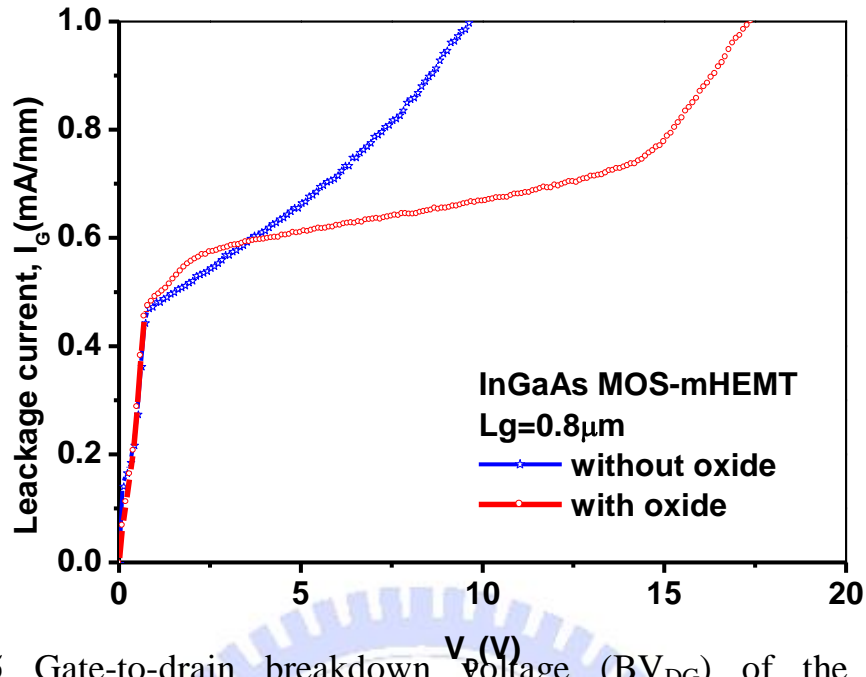
Fig. 5-5 Gate-to-drain breakdown voltage (BV$_{DG}$) of the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT and conventional HEMT
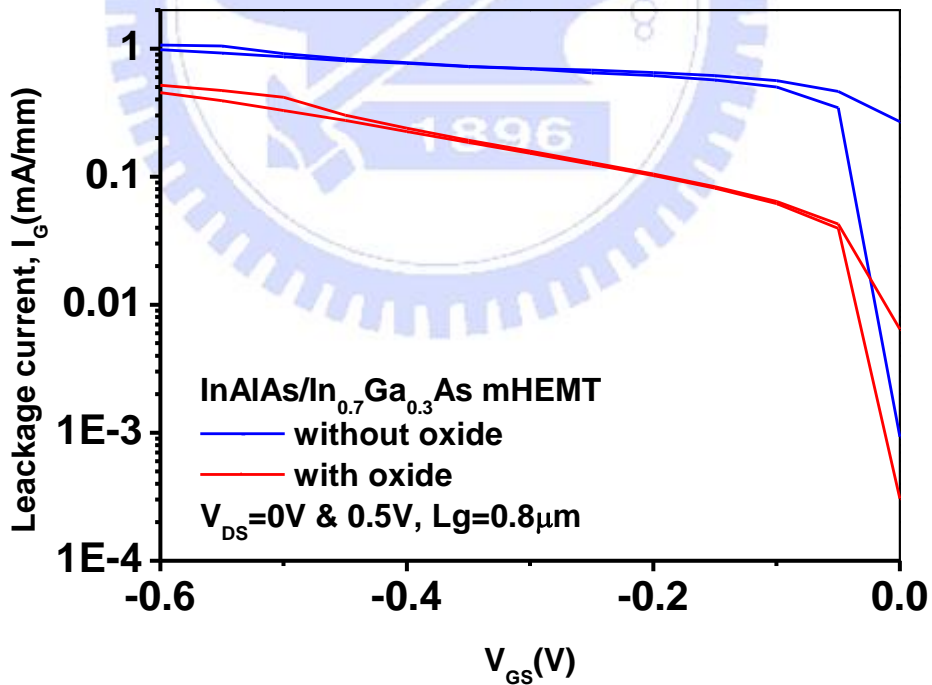
Fig. 5-6 Gate leakage current density performance of the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS- MHEMT and conventional HEMT

Chapter 6
Employing Air-bridge Structure on InAlAs/InAs MOS-HEMTs for Digital Applications

6.1 Introduction

For further digital performances improvement of the InAlAs/In$_{0.7}$Ga$_{0.3}$As MHEMT, endowed with high electron mobility (33,000 cm^{2}V^{-1}s^{-1}) and high saturation drift velocities (8×10^{7}cm/sec), InAs is expected to be the solution to the channel material to improve the device performance for the next generation utilization.

However, conventional InAlAs/InAs MHEMTs drastically suffer from low breakdown voltages due to the enhanced impact ionization effects that occur in the narrow-bandgap InAs channel[2]. Further insulating layer is necessary to be employed to reduce the effects, as the former chapter shows. After the ALD Al$_2$O$_3$ is introduced, the carrier concentration within the channel is reduced affected by the oxide layer, attributing to the larger barrier height between the gate metal and Schottky layer.

Another issue is worth noticing that devices with different gate width are needed for different level usage. Fan-out is a measure of the ability of a logic gate output, implemented electronically, to drive a number of inputs of other logic gates of the same type. Therefore, employing the air-bridge structure on InAs MOS-HEMTs could fabricate devices with

different amount of driving current.

In this study, we focus on the characteristics of the 0.8μm InAlAs/InAs/InP MOS-HEMTs with air-bridge structure. Devices with various gate widths were fabricated and the electrical characteristics were also investigated to identify the similarity of the performance. Besides, including subthreshold slope (S), drain-induced barrier lowering (DIBL) and I_{ON}/I_{OFF} ratio, above figures of merit (FOM) for logic application will also be exhibited to realize the logic potential of MOS-HEMTs.

6.2 Device Fabrication

The epitaxial layers of the InAlAs/InAs HEMTs were grown by molecular beam epitaxy (MBE) on InP substrate. The schematic cross-sectional view of our δ-doped InAlAs/InAs MOS-HEMT structure is shown in Fig. 6-1.

Fig. 6-1 shows the illustration of δ-doped InAlAs/InAs HEMT which consists of, from bottom to top, InAlAs buffer layer, $In_{0.70}Ga_{0.30}As/InAs/In_{0.70}Ga_{0.30}As$ composite channel, InAlAs spacer layer, δ-doped carrier supply layer with Si doping concentration of $5.0×10^{12}/cm^2$, InAlAs Schottky layer, InP etching stop layer, and n-InGaAs cap layer with Si doping concentration of $2.0×10^{19}/cm^3$. It is worth noticing that the high etching selectivity between InP and InAlAs is of importance for device fabrication, attributing to the 1st recess is done before Ohmic formation due to the post-depositing annealing temperature of ALD

Al_2O_3 is higher than the rapid thermal annealing temperature of the Ohmic metal.

The detailed manufacturing process on the InAlAs/InAs MOS-HEMT device is described at the following sections. The flow chart of the process for device fabrication is illustrated in Fig. 6-2.

6.2.1 Wafer cleaning

The purpose of wafer cleaning is to remove undesirable impurities and particles on the surface. The wafers were immersed in Acetone (ACE) and isopropyl alcohol (IPA) each for five minutes, and blown dry by nitrogen gas.

6.2.2 Mesa isolation

The active region of devices is defined by S1818 photoresist, and other potions were wet etched to the buffer layer. The mesa isolation was carried out by H_3PO_4:H_2O_2:H_2O (5:1:40) solution to etch the InGaAs cap layer and the InAlAs Schottky layer. HCl:H_2O (1:1) solution to etch the InP etching stop layer. Then, the etching depth will reach about 4000Å by utilizing H_3PO_4:H_2O_2:H_2O solution again. The etching depth is measured by α-step measurement.

6.2.3 1st recess

The gate recess slot was defined by S1818 photoresist to form the pattern. Succinic acid (SA) based solution (SA:H_2O_2:H_2O) was used to etch the cap layer and part of the InAlAs shottky layer.

6.2.4 Surface treatment

Here, we choose $(NH_4)S_X$ as our surface treatment solution. The HCl:H_2O (1:4) solution was applied for removing the native oxide, followed by dipping the wafer in $(NH_4)S_X$ for 30 minutes at 60℃. The depth of the passivating thin film can be determined by the immersing time and reacting temperature.

6.2.5 Atomic layer deposition (ALD) Al_2O_3

The process temperature of ALD Al_2O_3 is 300℃, and the uniform Al_2O_3 layer is deposited for the depth of 12μm, followed by the post-deposition annealing (PDA) at 500℃.

6.2.6 Ohmic formation

The ohmic contact region is defined by AZ5214E photoresist with undercut profile. The wafers are dipped in HF: H_2O (1:10) for 1 minute to remove the Al_2O_3, and 20% HCl solution for 15 seconds to remove the native oxide. Ohmic metal was then deposited on the substrates by using an electron-beam evaporator at a pressure of ~1×10^{-6} Torr. After ACE lift-off procedure, the wafer was thermally alloyed at 240℃ for 30 seconds by using rapid thermal anneal (RTA) system. After all, the contact resistance is observed via measuring the transmission line method (TLM), and the specific contact resistivity is 1.3945×10^{-7} $\Omega\,cm^2$.

6.2.7 Gate formation

The gate slot was defined by AZ6310 photoresist, and the wafers were then dipped in the 20% HCl solution for 15 seconds to remove the native oxide fallowed by depositing Ti/Pt/Au by e-gun evaporation system. Finally, the wafer was immersed into ACE to lift-off the undesired metal. As the result, the gate length of the InAlAs/$In_{0.7}Ga_{0.3}As$ MHEMTs in this chapter is 0.8μm.

6.2.8 Device passivation

In order to protect the devices from environmental contamination and mechanical damages, the silicon nitride film (SiN_X) was formed by PECVD. The wafer was first dipped in the solution of $NH_4OH:H_2O=1:50$ for 10 seconds to clean the surface and decrease the surface dangling bonds. The silicon nitride film was grown at $250℃$. RF power was 35W, and the precursors were SiH_4/Ar, NH_3 and N_2. The film thickness was about 1000Å and its refractive index was about 2.0, which were measured by ellipsometer.

After the passivation process, the contact via was defined for interconnections. Then the silicon nitride film was etched by reactive ion etching (RIE) system. The reactive plasmas are CF_4 and O_2, the RF power is 80W, and the pressure is 60 mtorr.

6.2.9 Air-bridge plating

First, a layer of photo-resist was spun and patterned to open areas over metal pads. Then, a thin coating of Ti/Au/Ti was applied to the entire wafer, where Titanium is deposited to improve the adhesion. The thin metal layer can conduct the plating current to the whole wafer. Next, a second coating of photo-resist was applied and patterned. Then the wafer was electroplated with gold for 2μm thickness. After plating, the top resist layer, thin Ti/Au/Ti metal, and lower resist layer were removed individually, leaving only the plated air-bridge.

6.3 Results and Discussion

Electrical characteristics of the 0.8μm InAlAs/InAs MOS-HEMT with various gate widths are plotted and analyzed. Fig. 6-3 demonstrates extrinsic transconductance (G_m) versus gate-to- source voltage (V_{GS}) curves. The peak G_m of the devices slightly decreases as the gate width increases. Meanwhile, the driving current increases, which is shown in Fig.6-4. Moreover, the threshold voltage of each device doesn't change a lot with the variation of the gate widths.

The breakdown voltage diagram is illustrated in Fig. 6-5, which displays high gate-to-drain breakdown voltage (BV_{GD}) is achieved. All the BV_{GD} of the InAlAs/InAs MOS-HEMT with various gate widths are around 17volts. In addition, the leakage current are reduced to less than 1 $\times 10^{-7}$ A/device in the Fig. 6-6. Those diagrams imply the good insulating property of InAlAs/InAs MOS-HEMT employing air-bridge structure.

Table 6-1 summarizes the logic parameters of the InAlAs/InAs MOS-MHEMT. All the parameters are defined as the chapter 3 exhibits and measured at a V_{DS} of 0.5 volt. All the devices with different gate widths perform almost the same logic performance, indicating that the possibility of InAlAs/InAs MOS-HEMT with different gate widths for logic applications of various fan-out level.

6.4 Conclusions

The 0.8μm InAlAs/InAs MOS-HEMTs with different gate widths were fabricated and the good insulating property was demonstrated. Meanwhile, the digital parameters and threshold voltage don't vary with the various gate widths, leading to the possibility of InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMT for digital utilization of different fan-out level. Further gate length scaling down is necessary to improve the device performance.

Table 6-1 Logic parameters of the 0.8μm InAlAs/InAs MOS-HEMT with various gate widths

	50μm	200μm	300μm	500μm
I_{DS} (mA)	11.7	30.6	36	48
DIBL (mV/V)	244	212	186	145
SS (mV/dec)	160	150	145	142
I_{on}/I_{off}	~400	~700	~900	~1000

120Å ALD Al_2O_3

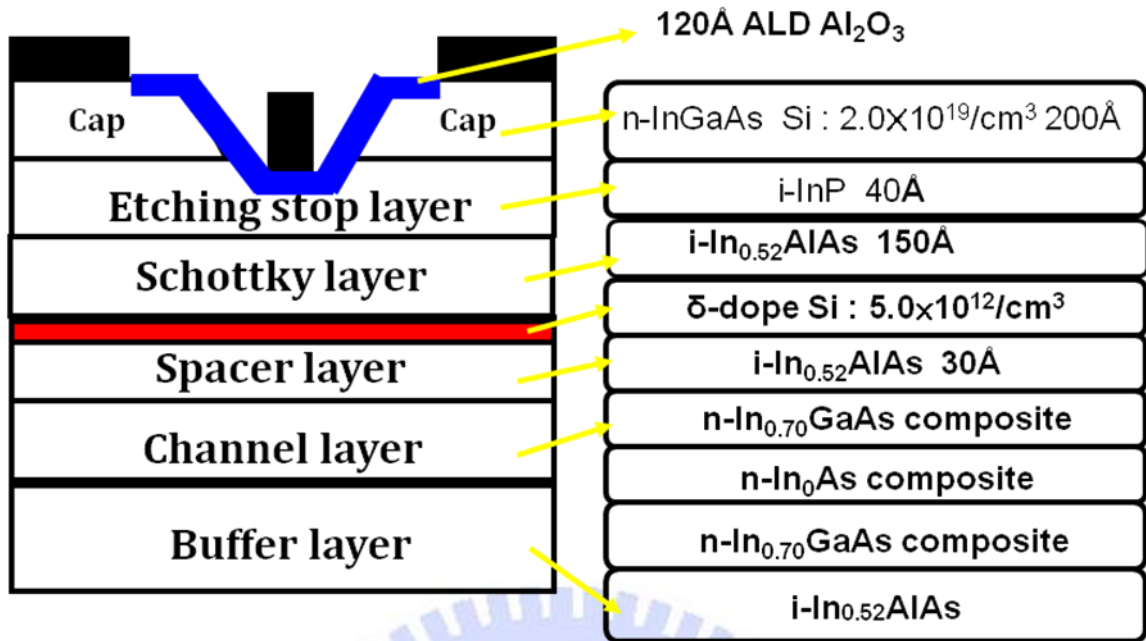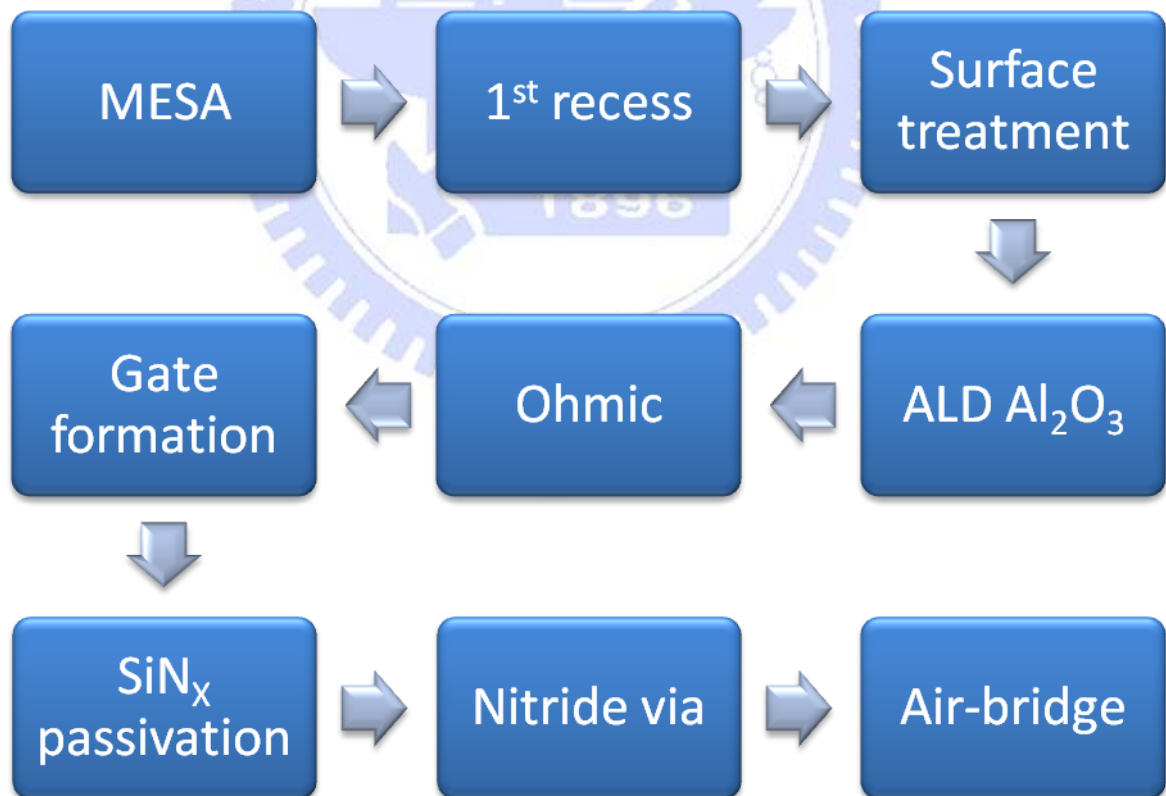|	
	n-InGaAs Si : $2.0 \times 10^{19}/cm^3$ 200Å
Cap	i-InP 40Å
Etching stop layer	i-$In_{0.52}$AlAs 150Å
Schottky layer	δ-dope Si : $5.0 \times 10^{12}/cm^3$
Spacer layer	i-$In_{0.52}$AlAs 30Å
Channel layer	n-$In_{0.70}$GaAs composite
	n-In_0As composite
	n-$In_{0.70}$GaAs composite
Buffer layer	i-$In_{0.52}$AlAs

Fig. 6-1 Structure of 0.8μm InAlAs/InAs MOS- HEMT

Fig. 6-2 Process flow of 0.8μm InAlAs/InAs MOS-HEMT
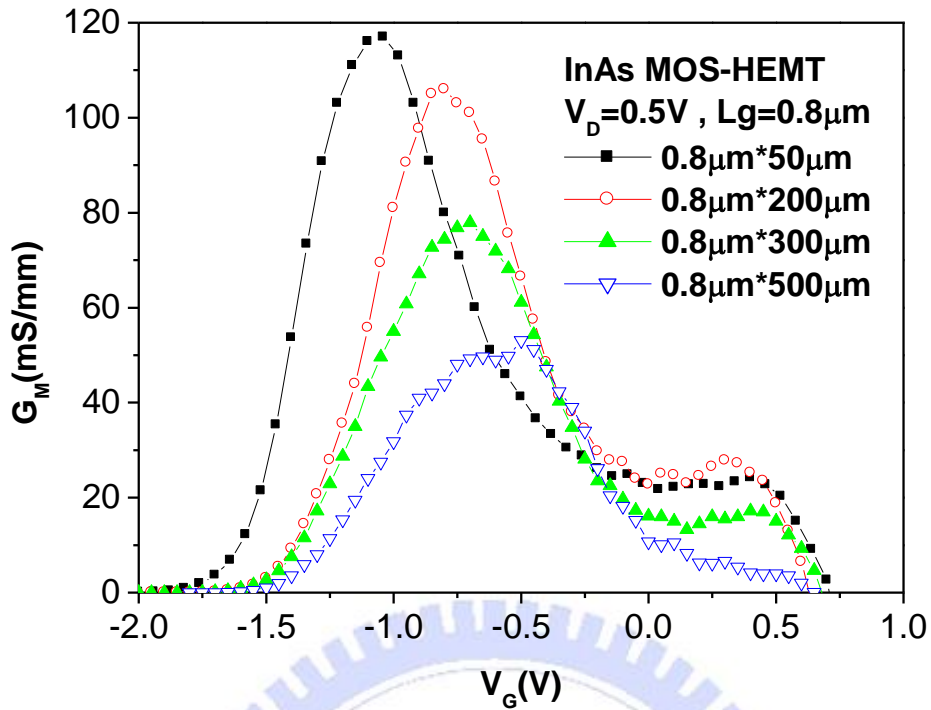
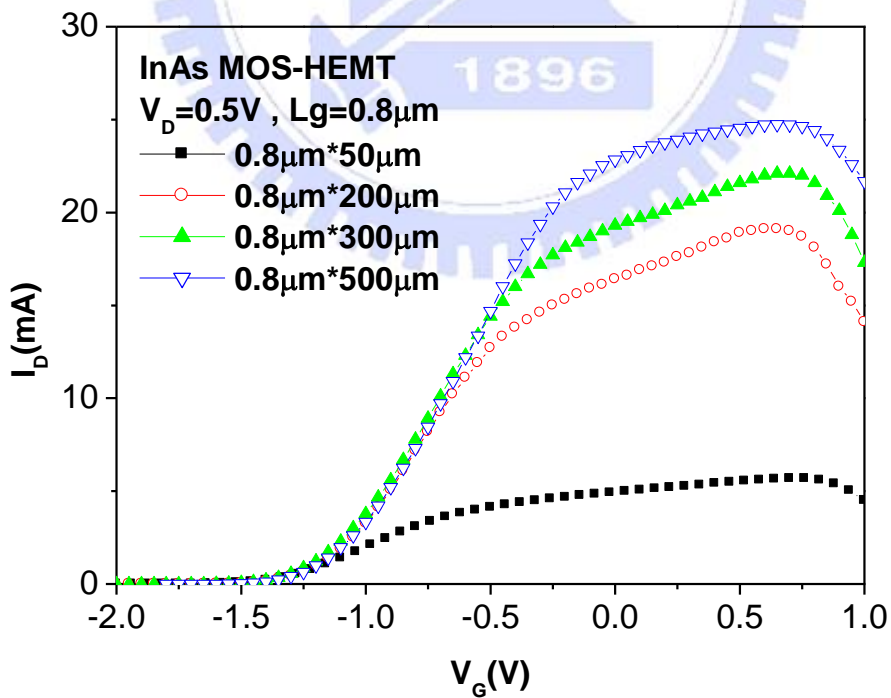Fig. 6-3 Extrinsic transconductance (G_m) versus gate-to-source voltage (V_{GS}) curves of the 0.8μm InAlAs/InAs MOS-HEMT

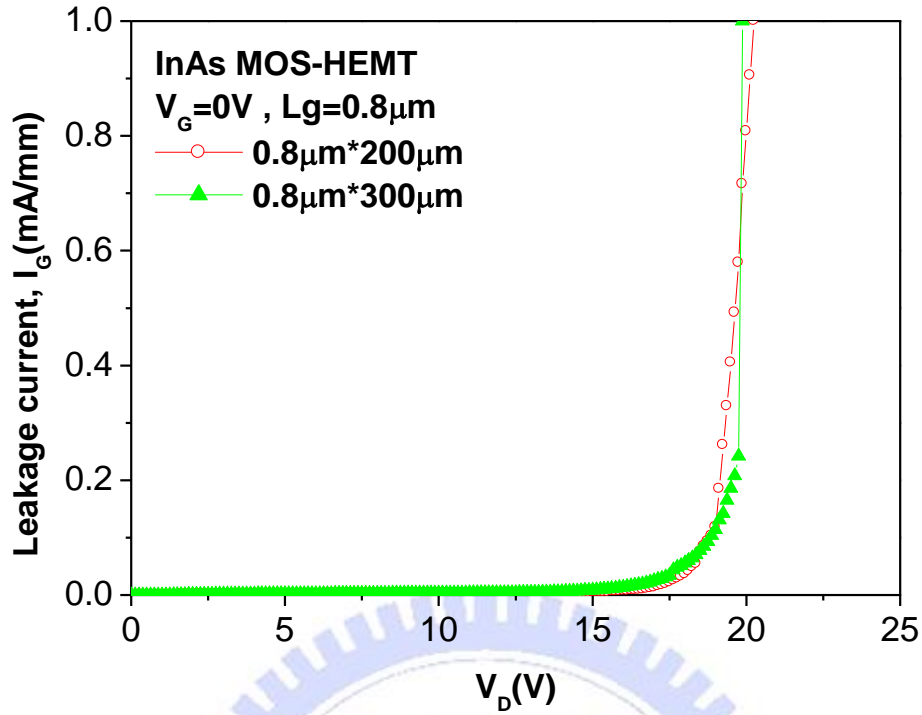Fig. 6-4 Drain current (I_D) versus gate-to-source voltage (V_{GS}) curves of the 0.8μm InAlAs/InAs MOS-HEMT

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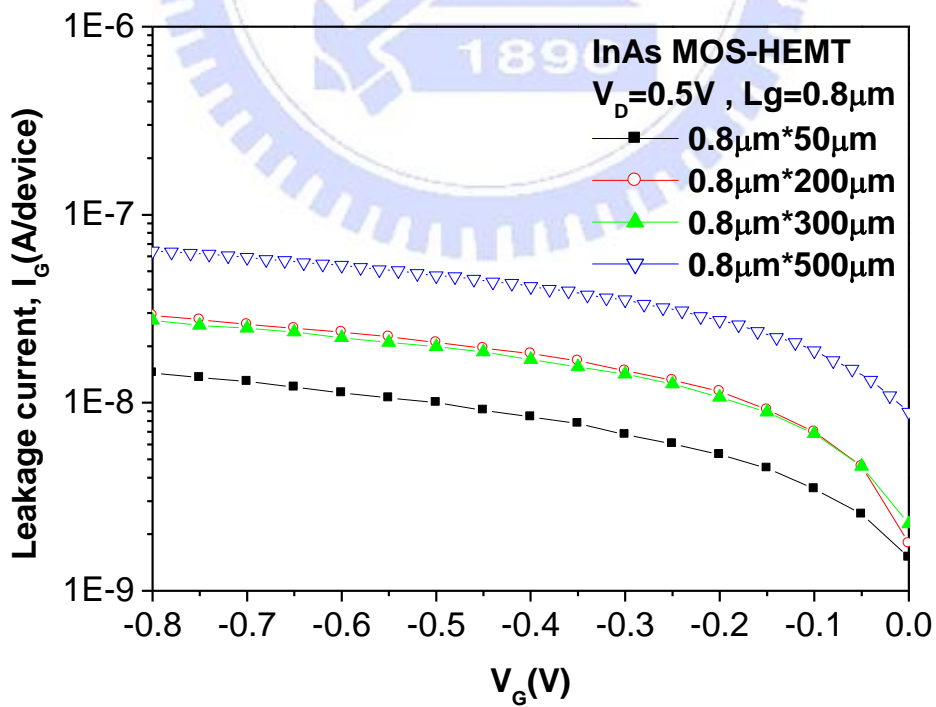Fig. 6-5 Gate-to-drain breakdown voltage (BV_{DG}) of the 0.8μm
InAlAs/InAs MOS- MHEMT

Fig. 6-6 Gate leakage current density performance of the 0.8μm
InAlAs/InAs MOS- HEMT

Chapter7
Conclusions

In this study, 0.3μm InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs, 0.8μm InAlAs/ In$_{0.7}$Ga$_{0.3}$As MOS-MHEMTs and 0.8μm InAlAs/InAs MOS-HEMTs were fabricated. The electrical characteristics of InGaP/In$_{0.22}$Ga$_{0.78}$As PHEMTs with different doping profiles were evaluated for both RF and digital application. On the device linearity issue, the uniformly-doped device shows higher IP3 of 22.19 dBm, and the channel doped device shows higher Δ (IP3-P$_{1dB}$) of 14.23 dB, and higher IP3 to DC power consumption ratio (IP3/P$_{DC}$) of 4.97 compared to other devices. Overall, the uniformly doped and channel doped devices have higher value of figure of merit for device linearity. From the aspect of digital application, SS and I$_{ON}$/I$_{OFF}$ ratio parameters can be improved by uniformly-doping in the Schottky layer and DIBL parameter can be reinforced by extra doping in the channel layer.

For high-speed digital application, the InGaAs channel with high indium concentration is required for better gate delay performance, and ALD Al$_2$O$_3$ was introduced as gate insulator to improve the insulating property. Both the 0.8μm InAlAs/In$_{0.7}$Ga$_{0.3}$As and InAlAs/InAs MOS-HEMTs demonstrate better insulating properties. Moreover, the digital parameters and threshold voltage didn't vary with the various gate widths, leading to the possibility of InAlAs/In$_{0.7}$Ga$_{0.3}$As MOS-MHEMT employing air-bridge structure for digital utilization of different fan-out level.

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