國立交通大學

材料科學與工程研究所

碩士論文

應用鈀/鍺/銅歐姆接觸至砷化銦鎵之全面銅金屬化磷化銦鎵/砷化鎵異質接面雙載子電晶體

Fully Cu-Metallized InGaP/GaAs HBTs Using Pd/Ge/Cu Ohmic Contact to N-type InGaAs

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Fully Cu-Metallized InGaP/GaAs HBTs Using Pd/Ge/Cu Ohmic Contact to N-type GaAs

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應用鈀/鍺/銅歐姆接觸至砷化銦鎵之全面銅金屬化

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摘要

在這篇論文中，成功的發展出使用鈀/鍺/銅歐姆接觸至 N 型砷化銦鎵上，且成功的運用至全面銅金屬化磷化銦鎵/砷化鎵異質接面雙載子電晶體中。

在低溫退火(250°C)下，鈀/鍺/銅歐姆接觸即具備了低接觸電阻(1 x 10^{-6} Ω-cm^2)。經由 X 光繞射儀、歐傑電子縱深分析、穿透式電子顯微鏡和能量分散式 X 射線分析的分析結果，鈀/鍺/銅歐姆接觸形成機制和微結構反應都已被研究了解；且鈀/鍺/銅歐姆接觸經過 250°C、24 小時的熱穩定測試後，其接觸電阻幾乎沒有變化。

接著將鈀/鍺/銅歐姆接觸應用至全面銅金屬化磷化銦鎵/砷化鎵異質接面雙載子電晶體，並使用鉑/鈦/鉑/銅為 P 型砷化鎵歐姆接觸、鈦/鉑/銅

為連接導線（其中鉑為銅之擴散阻障層）。量測結果顯示，全面銅金屬異質接面雙載子電晶體的直流特性和使用傳統金金屬化的特性相當；此外，將元件施以在高電流密度 100kA/cm^{2}之電流加速測試 24 小時後，其元件特性也並沒有明顯改變。結果顯示將鈀/鍺/銅歐姆接觸應用至全面銅金屬化磷化銦鎵/砷化鎵異質接面雙載子電晶體其元件特性十分的優異。

Fully Cu-Metallized InGaP/GaAs HBTs Using Pd/Ge/Cu Ohmic Contact to N-type InGaAs

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Abstract

The Pd/Ge/Cu ohmic contacts to n-type InGaAs is investigated. The Au-free fully Cu-metallized InGaP/GaAs HBTs using Pd/Ge/Cu ohmic contact to n-type InGaAs also has been successfully fabricated for the first time.

Low specific contact resistivity of $1x10^{-6}$ Ω-cm^2 was achieved at a low annealing temperature (250 °C). The ohmic contact formation mechanisms and microstructure evolution were investigated using x-ray diffraction (XRD), Auger electron spectroscopy (AES) depth profiles, transmission electron microscopy (TEM) and energy dispersive spectrometer (EDX). The thermal stability test of the Pd/Ge/Cu ohmic contact on InGaAs was also performed at 250 °C for 72 hours and showed no obvious degradation on Pd/Ge/Cu ohmic contact after the annealing. In addition, the sheet resistance got to high temperature of 550 °C for 20min also showed no obvious rising.

The Pd/Ge/Cu ohmic contact was applied to the fully Cu-metallized InGaP/GaAs HBTs as the emitter and collector metals. The base metal was Pt/Ti/Pt/Cu, SiN_x was used for passivation, and Ti/Pt/Cu was used for interconnect metals with Pt as the diffusion barrier. The common emitter I-V curves and current gain (β) of these Cu-metallized HBTs using Pd/Ge/Cu ohmic contact on InGaAs cap layer showed similar electrical characteristics as those for conventional Au-metallized HBTs.

The high current test was performed at a high emitter current density of 100kA/cm^2 for the fully Cu-metallized HBT with Pd/Ge/Cu ohmic contact showed almost no obvious degradation in electrical characteristics. The results show that the novel Pd/Ge/Cu ohmic contact can be used on InGaAs Cap layer of fully Cu-metallized InGaP/GaAs HBTs exhibit good device performance.

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Chapter 1
Introduction

1.1 General Background

Copper (Cu) has been widely used in the silicon (Si) based VLSI metallization [1-3]because of its lower electrical resistivity, higher resistance to electromigration and stress voiding as compared to commonly used aluminum (Al). As for GaAs-based devices, there are only few papers discussed about Cu metallization[4-5]. The most commonly used interconnect metal for III-V devices is Au, if Cu replaces Au as the metallization metal for heterojunction bipolar transistors (HBTs), the resulting improvement in electrical conductivity could increase the transmission speed of the circuits, and the heat dissipation will be improve as well. The price of Cu is about 4000 times cheaper than that of Au, and therefore the manufacturing cost will be substantially reduced. A comparison of the characteristics of the metallization metals is list in Table 1.

InGaAs has been studied as a material for high-speed device such as a heterojunction (HBT) [6] and a high electron mobility transistor (HEMT) [7] due to its high electron mobility and high electron saturation velocity. The objective of this study is to develop the Cu-metallized ohmic contact on InGaAs for the GaAs devices to implement a fully copper metallized InGaP/GaAs HBTs. Conventionally, Au/Ge/Ni ohmic contact system is the most widely used material system for the n-type ohmic contacts of the GaAs-based devices. However, this ohmic system was not compatible with other Cu metallization

process. In addition, the Au/Ge/Ni ohmic contact system have several drawbacks, such as large spread of the contact resistivity, poor contact edge definition, and the annealing temperature was high due to the eutectic Au/Ge alloy (The Au-Ge eutectic temperature is 361 °C.).

This study reports a novel low resistance Pd/Ge/Cu ohmic contact system to n-type InGaAs with a wide annealing temperature range (220 °C ~ 450 °C). A low contact resistivity of 1.0 x 10^{-6} Ω-cm^2 was achieved at a low annealing temperature of 250 °C. In this study, the formation mechanisms of the Pd/Ge/Cu ohmic contact on InGaAs system will also be discussed.

The DC and Power characteristics of the fully Cu-metallized HBT are evaluated in this dissertation. Here, we report the fabrication and electrical performance of the Cu metallized InGaP/GaAs HBTs with Pd/Ge/Cu as the emitter and collector ohmic contact metal. The fully Cu-metallized used Pt/Ti/Pt/Cu for base metal, and SiN for passivation, and Ti/Pt/Cu for interconnect with Pt as the diffusion barrier.

Besides, the traditional GaAs HBTs using Au metallization as the ohmic and interconnect metal were also fabricated in order to compare the characteristics with fully Cu-metallized GaAs HBTs.

1.2 Dissertation Content

The contents of this dissertation include: literature review, experiment, results, discussion and conclusions. In Chapter 2, the literature of ohmic contact for n-type InGaAs and GaAs-based HBTs are reviewed. In Chapter 3, the study of ohmic contact, the samples preparation for material analysis, and the fully Cu-metallized GaAs HBT device process flow are described. In addition, the results of multilayer interfacial material analysis, the DC and Power characteristics and the reliability tests for the fully Cu HBTs will also be presented. The Pd/Ge/Cu ohmic contact, formation mechanism, the DC and Power characteristics of the HBT devices using the Pd/Ge/Cu ohmic will be discussed in Chapter 4. Finally, the conclusions will be given in Chapter 5.

Table

Table 1 Properties comparisons of possible interlayer metals

Property	Cu	Ag	Au	Al
Resistivity(μΩ・cm)	1.67	1.59	2.35	2.66
Young's modulus・10^{-11} dyn/cm^2	12.98	8.27	7.85	7.06
Thermal Conductivity (W/cm)	3.98	4.25	3.15	2.38
CTE・10^6	17	19.1	14.2	23.5
Melting Point (℃)	1085	962	1064	660
Specific heat Capacity (J/Kg•K)	386	234	132	917
Corrosion in air	Poor	Poor	Excellent	Good
Deposion				
Sputtering	Yes	Yes	Yes	Yes
CVD	Yes	No	No	No
Evaporation	Yes	Yes	Yes	Yes
Etching				
Dry	No	No	No	Yes
Wet	Yes	Yes	Yes	Yes
Resistance to Electromigration	High	Very Low	Very High	Low
Delay Time(ps/mm)	2.3	2.2	3.2	3.7

Chapter 2
Literature Review

2.1 Cu Metallization

As the dimension of the devices shrink, the intrinsic switching speed, higher package density and higher complexity circuit of the device can be significantly improved. However, the increasing in wiring resistance resulting from the reduction in interconnection lines feature size and the resistance-capacitance (RC) time delays become the major limitations in achieving high circuit speeds. The device performance is severely impacted by interconnect parasitic considerations and to a lesser extent by active device switching speeds. In addition, as the dimensions of the devices shrink, problems associated with electromigration in aluminum-based interconnection lines have serious deleterious effects on device reliability.

Copper is being evaluated for silicon based VLSI metallization because it's lower bulk electrical resistivity of 1.67 μΩ·cm as compared to 2.66 μΩ·cm of Al and the lower resistivity can greatly improve the RC time delay. Moreover, Cu has superior resistance to electromigration and stress voiding as compared to commonly used Al. Unfortunately, Cu atoms are quite mobile in most metals, as well as in silicon even at modest temperature. Moreover Cu is a deep level dopant in silicon, which resulting in the deterioration of devices such as leakage current and threshold voltage instability.

For III-V-based devices, Au was commonly used as the metallization metal. If Cu is used as the metallization metal instead of Au, there will be several advantages such as lower resistivity, higher thermal conductivity, and lower cost

as shown in table 1. But as in the Si case, Cu also diffuses very fast into GaAs when Cu is directly contact with the GaAs substrate without any diffusion barrier [8]. Copper is a deep dopant in GaAs, if Cu diffuses into ohmic contact, the passivation layer SiN_x and device active region, it will deteriorate the electrical properties of the devices. Figure 1 shows that the Cu-diffusion changes the EL2 centre into a deep donor (T3) with a lower activation energy, 0.7 eV [9]. Therefore, a very effective diffusion barrier is necessary to prevent Cu from diffusing and intermixing into the underlying materials both for Si and III-V systems.

2.2 Ohmic Contact for GaAs-Based Devices

The definition of ohmic contact on a semiconductor is to allow electrical current to flow into or out of the semiconductor freely without barrier [10]. The contact should have a linear I-V characteristic, be stable over time and temperature, and contribute as little contact resistance as possible.

2.2.1 Requirements for A Good Ohmic Contact Material

The requirements for a good ohmic contact include: [11]

1. Low contact resistance

The first requirement for ohmic contacts of most devices is low contact resistivity, the resistance must be low enough not to affect the device I-V characteristics. The requirement for the reduction of the contact resistances has been continuing, because as the size of the device shrink to improve the device performance according to the scaling rule, the specific contact resistivity must decrease in order to keep the same contact resistance.

2. Thermally stable:

The second requirement for the ohmic contacts in GaAs devices is thermal stability during device fabrication and device operation.

In addition, a smooth surface, good adhesion, shallow horizontal and verticle diffusion depths, and low metal sheet resistance are required for ohmic contact in GaAs device. The requirements for ohmic contact are illustrated in Figure 2.

2.2.2 Guideline for Low Resistance Ohmic Contact Formation

When a metal deposited on a semiconductor, the Fermi levels in the metal and the semiconductor must be equal. For the Fermi levels to be equal in both sides, an energy barrier $e\Phi_B$ must exist between the metal and semiconductor interface [12]. The carriers can not transport freely because of the energy barrier. The carrier transport mechanisms through the metal/semiconductor interface are strongly influenced by the doping concentration in the semiconductor and the temperature.

The current density (J) between contact metal and n-type semiconductor is shown below:

$$J = \exp(-q\Phi_B/E_{00}) \qquad (2.1)$$

When

$$E_{00}=(qh/4\pi) \times (N_D/\varepsilon m^*)^{1/2}$$

ε :dielectric constant

N_D: doping concentration

m*:effective electron mass

χ :electron affinity

Equation 2.1 indicates that the current density increases when the doping concentration increases. When the semiconductor is extremely heavily doped (>high-$10^{18}cm^{-3}$), the electrons can tunnel through the energy barrier between metal and semiconductor to form good ohmic contact. This is called “tunneling mechanism”. The band diagram is shown in Figure 3. These diagrams give us guidelines to design the ideal M/S interfacial structure for low resistance ohmic formation.

Higher doping level is easy achievable in p-type GaAs. Because the dopants used in the p-type GaAs are not amphoteric and DX centers are associated with donors only, the ohmic contact to highly doped p-type GaAs can be easily formed. However, for n-type GaAs, the upper limit of the Si doping concentration achieved by the conventional ion-implantation technique is about 10^{18} cm^{-3}. This level is limited by the formation of DX centers in n-type GaAs.

Due to this limitation on the of doping concentration, the formation of ohmic contact on n-type GaAs is difficult. The best way to modify the interfacial microstructure to produce low resistance ohmic contact is to form a new intermediate semiconductor layer (ISL) with low energy barrier or high carrier density at the metal/semiconductor interface after heat-treatment as shown in Figure 4. This fabrication process are called “deposition and anneal ohmic contact” [11].

The most common method of forming “deposition and anneal ohmic contact” on n-type GaAs is to apply an appropriate metallization scheme to the heavily doped GaAs followed by annealing process. During the annealing process, one of the constituent metals diffuses into the wafer and dopes the cap

GaAs layer heavily.

This ohmic contact fabrication technique needs a relatively simple fabrication system and with excellent reproducibility. Thus, this technique is suitable for manufacturing devices and used in a wide variety of GaAs devices.

However, the big disadvantage for this technique is that the process parameters can not easily be found, such as the contact metals, thickness of each metal layer, annealing time and temperature, diffusion coefficients, stress, surface energy, etc.

There are many kinds of "deposition and anneal ohmic contact" reported from the literatures. Ge-based ohmic contact, one of the famous ohmic contact systems, will be described in the following section.

2.2.3 Ge-based Ohmic Contact Materials

AuGeNi contact materials were invented by Braslau et al. in 1967. [13], and have been extensively used as n-type ohmic contact materials for advanced GaAs devices over 30 years. Although AuGeNi ohmic contacts provided low contact resistance and excellent reproducibility, this ohmic contact also has several drawbacks such as rough surface morphology, deep reaction depth in GaAs substrate, complex alloying process, and thermal instability after contact formation. These reasons cause the large scale spread of the contact resistivity. To overcome these problems, many groups develop different ohmic contacts and try to apply them to the future sub-micron GaAs devices. The most popular ohmic contact system is Ge-based ohmic contact materials. Because Ge was found to dope heavily in the GaAs surface after heat-treatment, the contact resistivity of traditional Ge-based ohmic contacts is below $10^{-6}\Omega cm^2$ range.

In order to increase the donor concentration, a small amount of elements

can be added. These additional elements increase the donor concentration in the GaAs surface layer and decrease the energy barrier height at the contact metal/GaAs interfaces.

To increase the donor concentration, “direct” doping elements and “indirect” doping elements were chosen in the past. The ”direct” doping elements were Sn, Sb, and Te which would increase the donor concentration in the GaAs surface layer by diffusing after heat-treatment. The “indirect” doping elements were Pd, Pt, and Au. Because the mixing enthalpy of the Ga with those elements (M) is smaller than that with As, Ga would form M-Ga phases with these elements in the GaAs surface. And Ge atoms could easily diffuse to the Ga vacancies in the vicinity of the GaAs surface to increase the donor concentration in the GaAs surface layer and reduce the Rc values [14]. In addition, Ag and Cu also belong to the “indirect” doping elements with wide solubility with Ga in a wide temperature range, forming M(Ga) solid solutions [15]. The formation of M(Ga) solid solutions would also incease the Ga vacancy concentration and facilitate heavy doping of Ge atoms in the GaAs surface layer.

Pd/Ge/Cu ohmic contact is also one kind of the Ge-based ohmic contacts, but the formation mechanism is different from other Ge-based ohmic contacts reported in literature. Before introducing the formation mechanisms of Pd/Ge/Cu ohmic contact, PdGe and Cu_3Ge ohmic contact will be briefly introduced in next paragraphs.

Marshell et al. [16] developed the PdGe ohmic contact in 1980. PdGe ohmic contact is based on solid phase regrowth, not based on complex alloying process like traditional AuGeNi ohmic contact. The advantages of PdGe ohmic contact are uniform and shallow reaction, good thermal stability, and planer interface. The formation mechanism of PdGe is complex. When annealing at

100℃, Pd layer reacted with GaAs to form Pd_xGaAs ternary phase. The TEM image is shown in Figure 5 [17]. Because the mixing enthalpy of PdGa is smaller than PdAs, it could creat Ga vacancies in the near-interface region of the GaAs substrate. But at this temperature, ohmic contact is still not formed. After annealing above 300℃, the Pd reacted with amorphous Ge layer to form PdGe compounds and bring in some excess Ge atoms. Also at this temperature Pd_xGaAs ternary phase decomposed to form Pd atoms with GaAs layers. Then excess Ge atoms can dope the regrown GaAs layer and become highly doping layer and finally excess Ge atoms become epitaxial crystal Ge layer between the regrown GaAs and PdGe layer. The final structure is shown in Figure 6. Table 2 shows the summery of the contact resistivity of PdGe contact from four literatures. The lowest contact resistivity was about $10^{-6}\ \Omega cm^2$ on n-type GaAs with Si doping concentration of $10^{18}\ cm^{-3}$.

M. O. Aboelfotoh et al. [18] have developed the Cu_3Ge ohmic contact in 1994. This ohmic contact system is very unique. After annealing, Cu layer reacts with the Ge layer to become Cu_3Ge structure. Because the chemical potential of Ga atom in the Cu_3Ge is lower than that in the GaAs substrate, Ga atoms diffuse out to the Cu_3Ge compound and creat many Ga vacancies. Ge atoms can dope in near-interface region of GaAs to highly doping. It also can be seen by SIMS profile in Figure 7. Besides, this compound is crystal structure and has long range order. The grain boundary of Cu_3Ge compound is vertical to the GaAs surface. It can increase conductivity. The TEM image is shown in Figure 8.

Giving a summary of these two ohmic contact systems, the formation of the low resistance ohmic contact has two conditions. First, create Ga vacancies and then Ge atoms doping into near-interface region of GaAs substrate. It can use

some elements reacted with GaAs to form ternary phase. And after annealing, MGaAs phase decomposed to metal and regrown n^+- GaAs layer same as the formation mechanism of the PdGe ohmic contact. It uses the chemical potential of Ga atoms in the ohmic compound is lower than in the GaAs so that Ga atoms diffuse out to create Ga vacancies as the formation mechanism of Cu_3Ge ohmic contact. Second, it forms the low resistivity metallic compound like Cu_3Ge crystal structure. Furthermore, we can combine high doping with low barrier high mechanism to form a good Ohmic contact. The Image shows in Figure 9.

2.3 GaAs Based Heterojunction Bipolar Transistors

The concept of the heterojunction bipolar transistor was first introduced by William Shockley in 1948. A detailed theory related to this device was developed by H. Kroemer in 1957 [23]. Kroemer realized that the use of a wide-band-gap emitter and low-band-gap base would provide band offsets at the heterointerface that would favor the injection of the electrons, in an n-p-n transistor, into the base while retarding hole injection into the emitter. These advantages would be maintained, even when the base is heavily doped, as is required for low base resistance, and the emitter is lightly doped. Thus in an HBT, high emitter injection efficiency would be maintained while parasitic resistances and capacitances would be lower than for a conventional homojunction bipolar transistor.

The cross section of a basic n-p-n AlGaAs/GaAs heterojunction bipolar transistor is shown in Figure 10. The n-type emitter is formed in the wide-band-gap AlGaAs while the p-type base is formed in the lower band gap GaAs. The n-type collector, in this basic device, is also formed on GaAs. To

facilitate the formation of the ohmic contacts, a heavily doped n^+-GaAs layer is present between the emitter contact and the AlGaAs layer. The energy band diagram of this device is shown in Figure 11.

Some inherent advantages of HBTs over silicon bipolar transistors are as follows [24]:

(1) Due to the wide-band-gap emitter, a much higher base doping concentration can be used, decreasing base resistance.

(2) Emitter doping can be lowered and minority carrier storage in the emitter can be made negligible, reducing base-emitter capacitance.

(3) High electron mobility, built-in drift fields, and velocity overshoot combine to reduce the electron transit time.

(4) Semi-insulating substrates help reduce pad parasitics and allow convenient integration of devices.

(5) Early voltages are higher and high injection effects are negligible due to high base doping.

Figure 12 shows the band diagram of a homojunction BJT and HBT. The energy band gap difference between the emitter and the base gives the HBT a substantial edge over BJT. When the base-emitter junction of a BJT is forward biased, both the electrons forward-injection into the base and the hole back-injected into the emitter experience the same amount of energy barrier. For the HBT, when the base-emitter junction is forward biased, the holes, which are back inject from the base into emitter, experience a $\triangle E_g$ larger energy barrier than the electrons, which are injected into the base. So, the HBT provides a design freedom meaning that a HBT structure design can have a heavily base dope to reduce the base resistance, while still maintaining a high current gain.

We can quantify the advantage of HBT compared to BJT by calculating the ratio of the collector current to the base current [25].

$$\frac{Ic}{I} = \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \frac{{n_{iB}}^2}{{n_{iE}}^2} = \frac{D_{nB} X_E N_E}{D_{pE} X_B N_B} \exp\left(\frac{\Delta E_g}{kT}\right) \tag{2.2}$$

Equation (2.1), which relates the intrinsic carrier concentration to the energy gap, was used in the derivation. It's defined as the current gain which is one of the most important parameters in bipolar transistors.

Among several HBT device structures, InGaP/GaAs HBTs are becoming attractive as compared with the AlGaAs/GaAs HBTs in the circuit applications such as high-speed analog-to-digital converters, high-power microwave amplifiers, and high-speed optical communication circuits due to their robust reliability and excellent DC and RF performances. In addition, several advantages have been claimed for this material system, such as large valence-band discontinuity, very low interface recombination velocities with GaAs, significantly less oxidation in comparison with AlGaAs, no DX centers issue, and good selective etch with GaAs [26].

Table

Table 2 Summary of PdGe ohmic contact data from literature

Pd / Ge (Å)	ρ_c (Ωcm^2)	Doping (cm^{-3})	Formation Condition	Ref.
500 / 1260	$\sim 10^{-6}$	1×10^{18}	Anneal 325℃ for 30min	[18]
500 / 1260	2.84×10^{-6}	2×10^{18}	Anneal 330℃ for 30min	[19]
500 / 1250	1.4×10^{-6}	3×10^{18}	RTA 425 ℃ for 60sec	[20]
200 / 400	5.33×10^{-6}	2×10^{18}	RTA 350 ℃ for 45sec	[21]

Figure

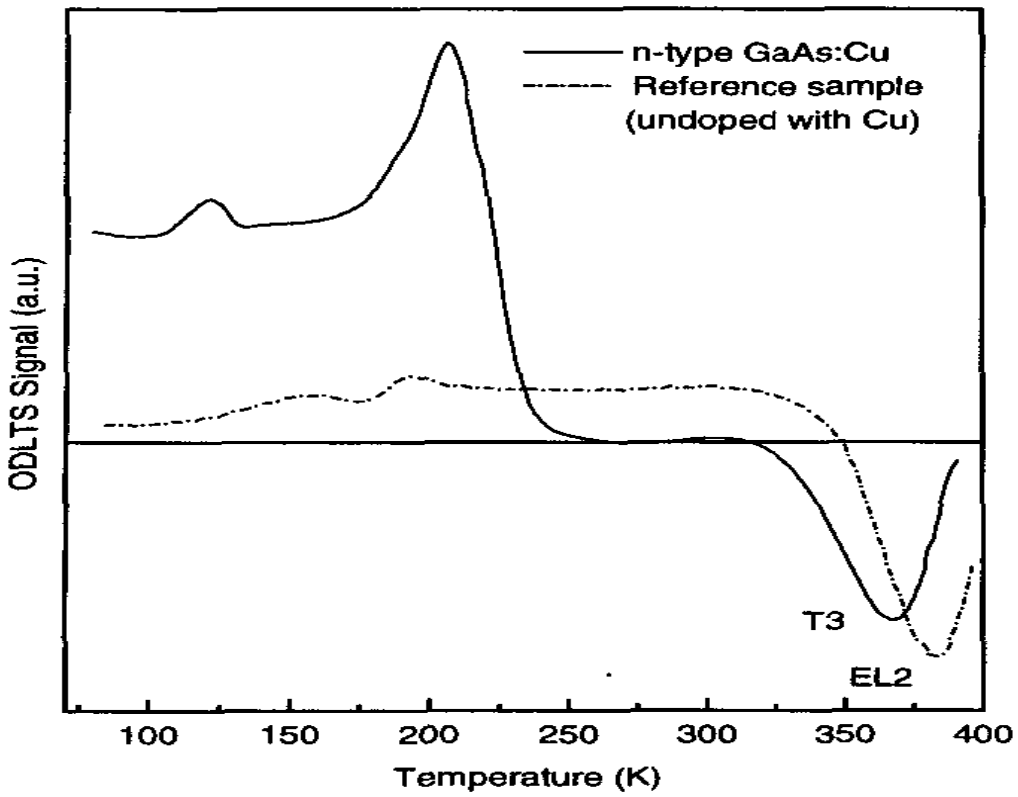


Fig1. Optical DLTS spectra from n-type GaAs. The rate window was $30s^{-1}$.

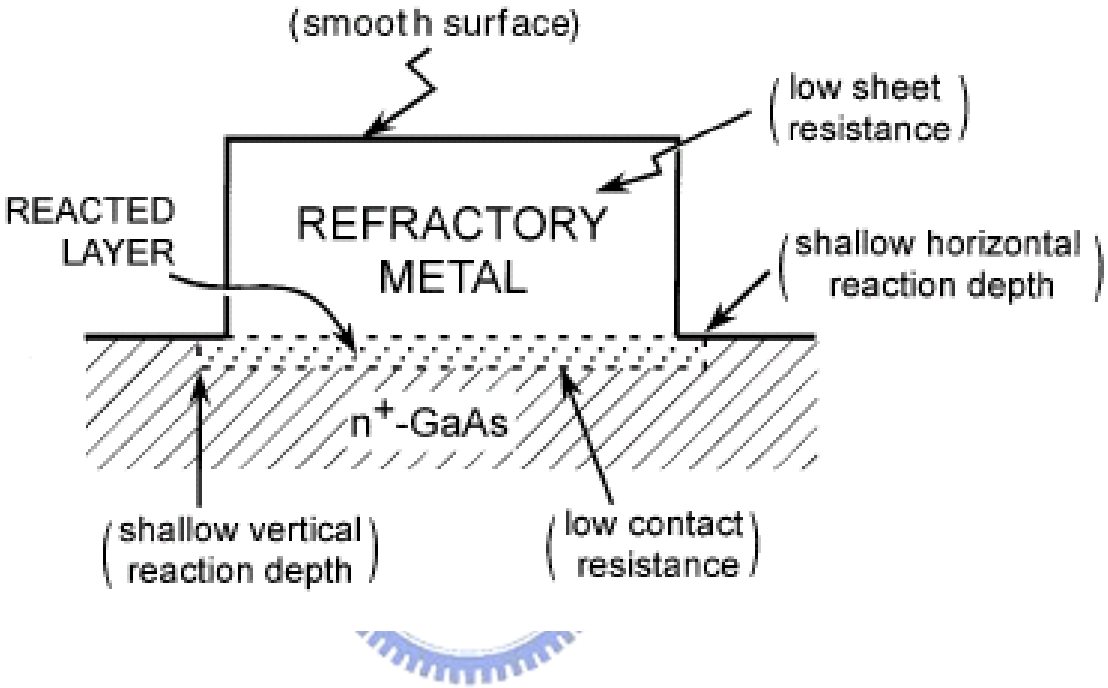


Fig2. Ideal interfacial structure for the low-resistance ohmic contact

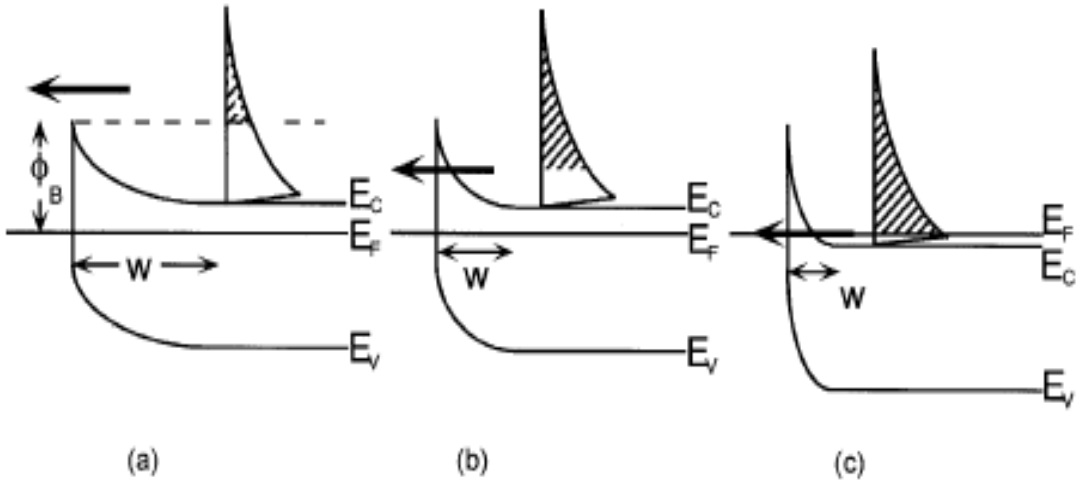


Fig3. Conduction mechanisms through metal/semiconductor interface

(a) lightly doped ($N_D < 10^{17}$ cm^{-3})

(b) intermediate level of 10^{17}–10^{18} cm^{-3}

(c) heavily doped (N_D > high-10^{18} cm^{-3})

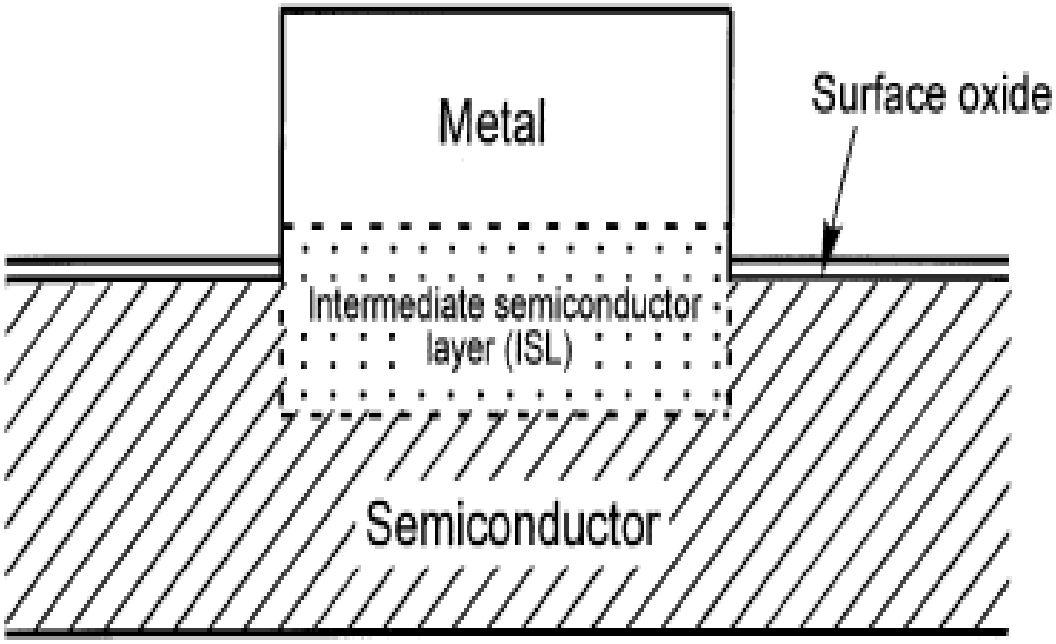


Fig4. Cross-section of the metal/semiconductor interface with ISL

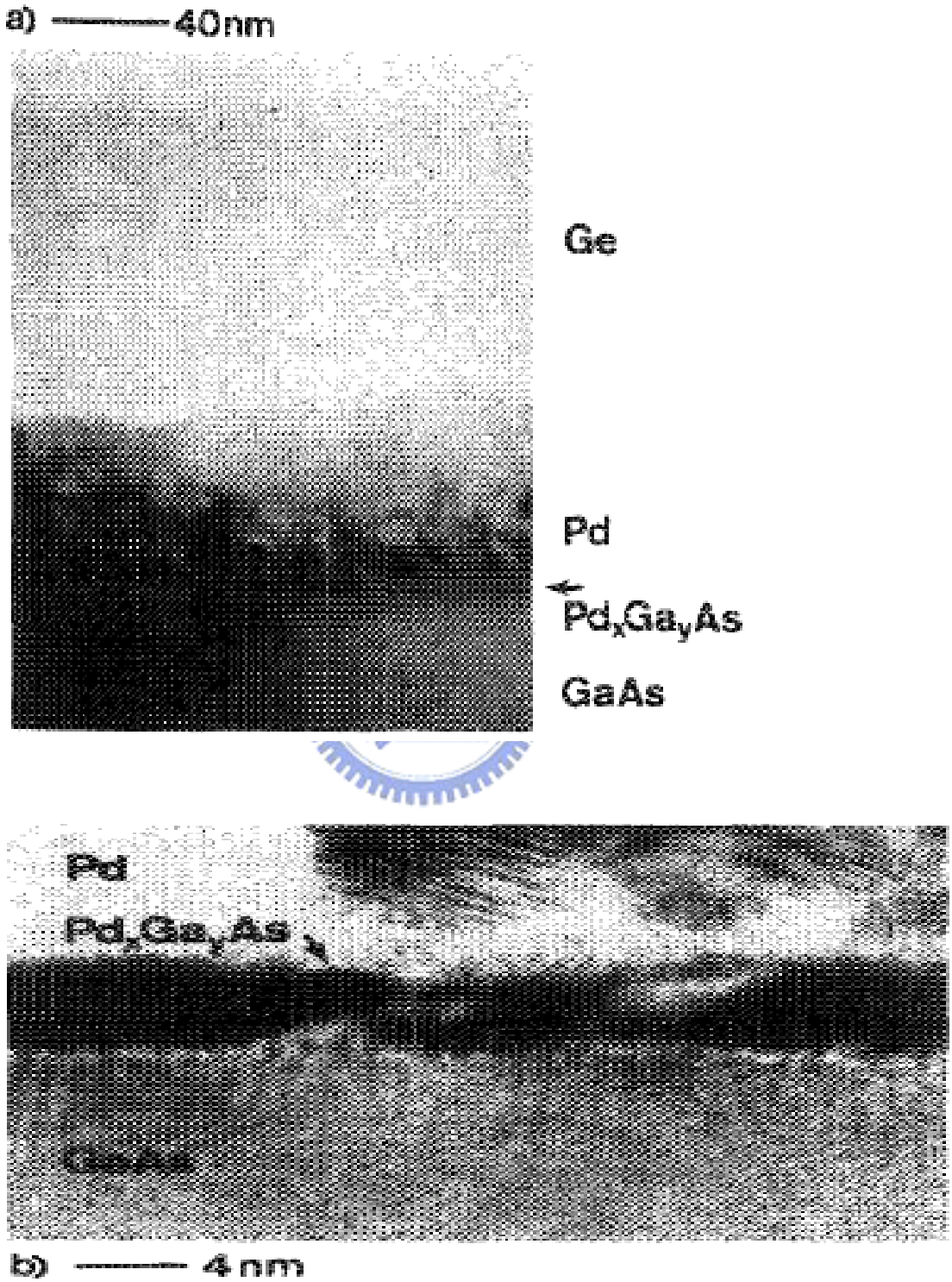
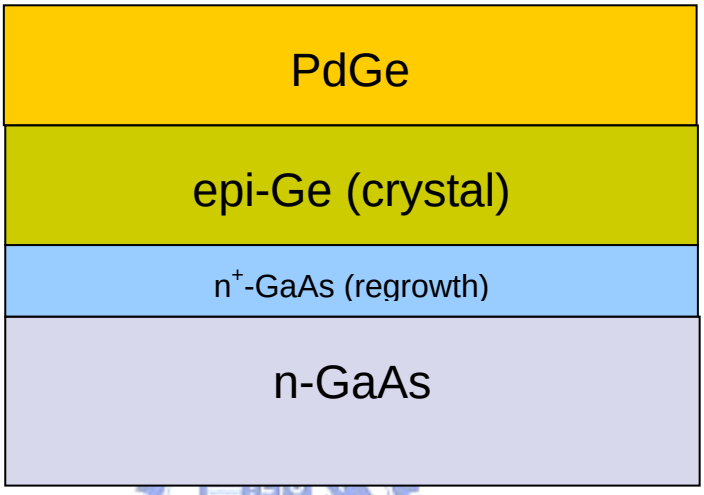


Fig5. The TEM image of the Pd /Ge contact after annealing at about 100℃



(a)

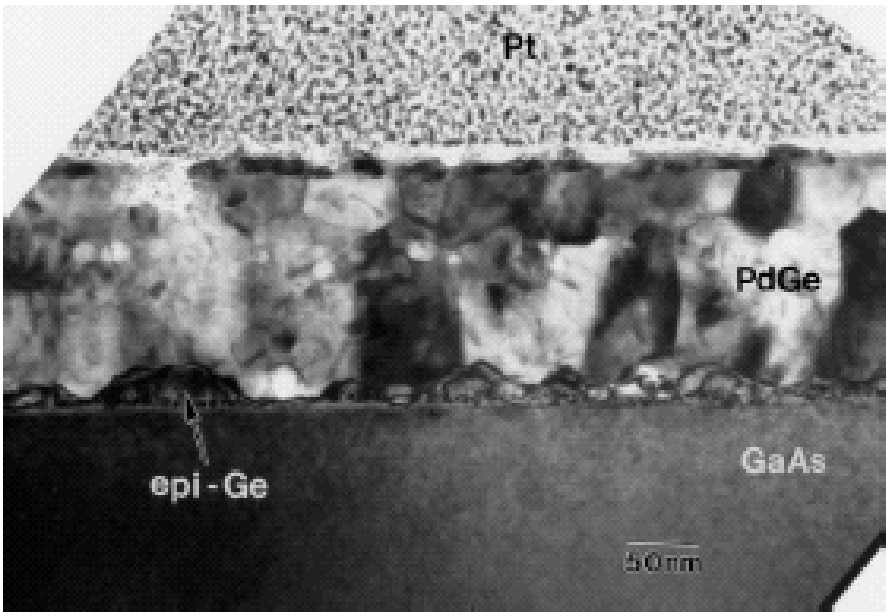


Fig6. (a) The structure and (b) TEM image of the PdGe contact

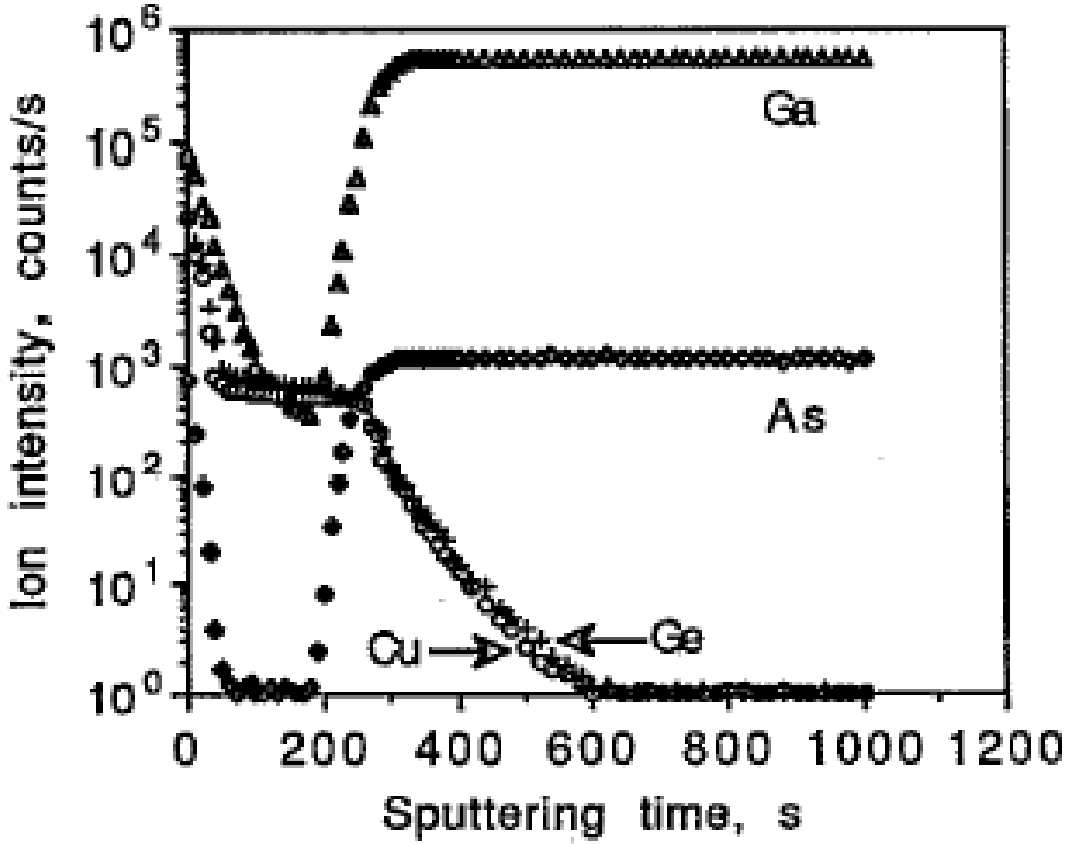


Fig7. SIMS profiles of an Cu_3Ge contact formed at 400℃ for 30min

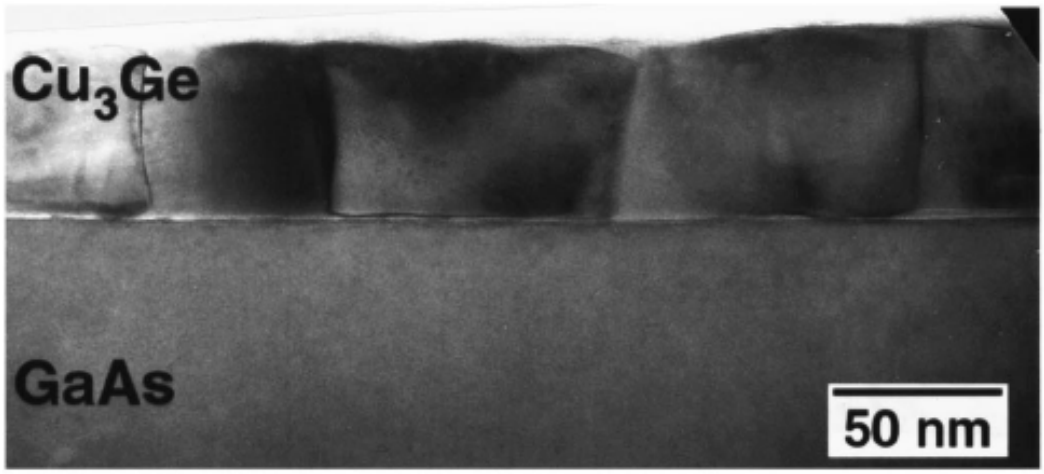


Fig8. TEM image of an Cu_3Ge contact formed at 400℃ for 30min

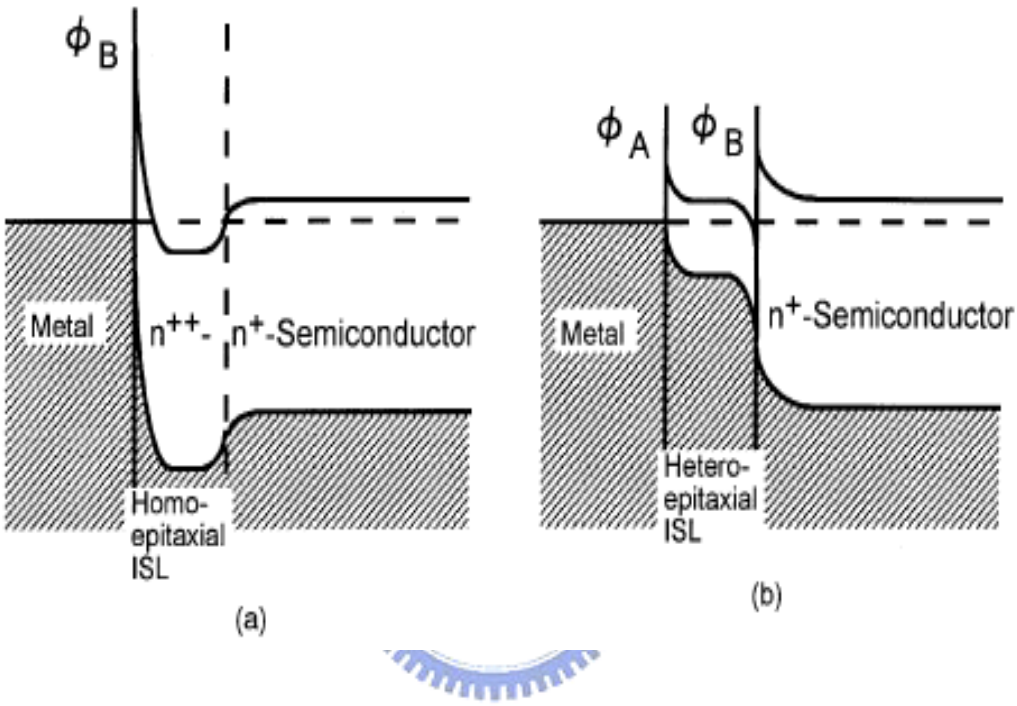


Fig9. Energy band diagrams of metal/semiconductor interfaces with (a) highly doped ISL (b) low energy barrier ISL.

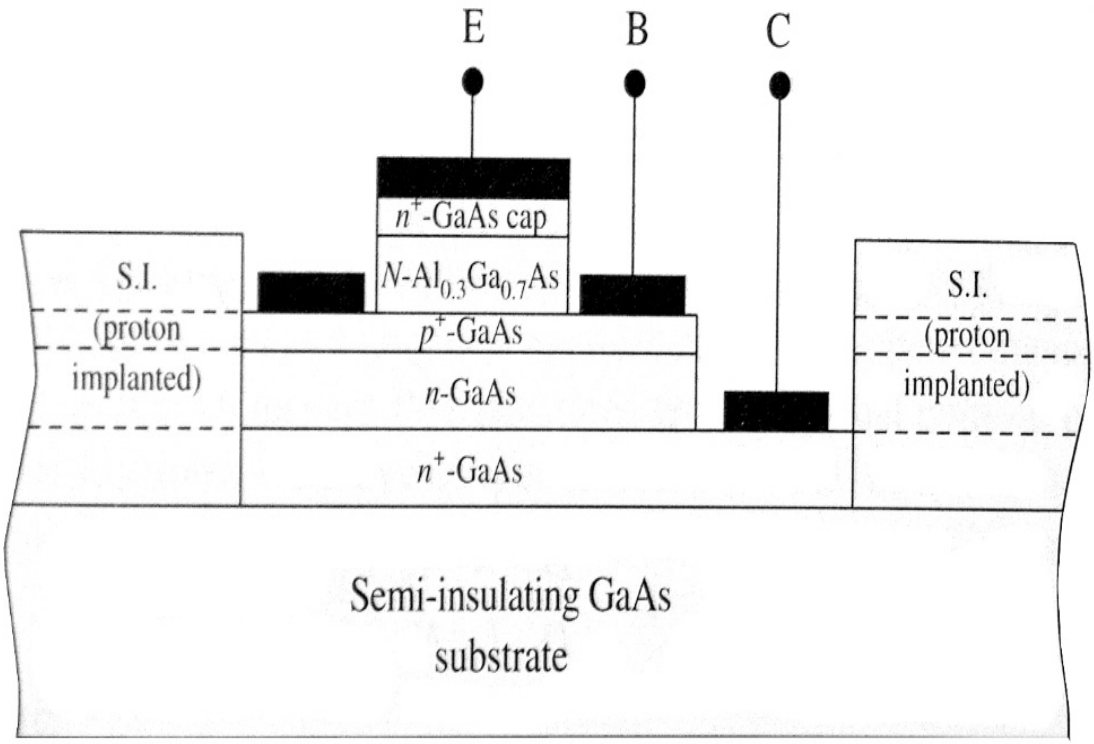


Fig10. Schematic of the cross section of an HBT structure

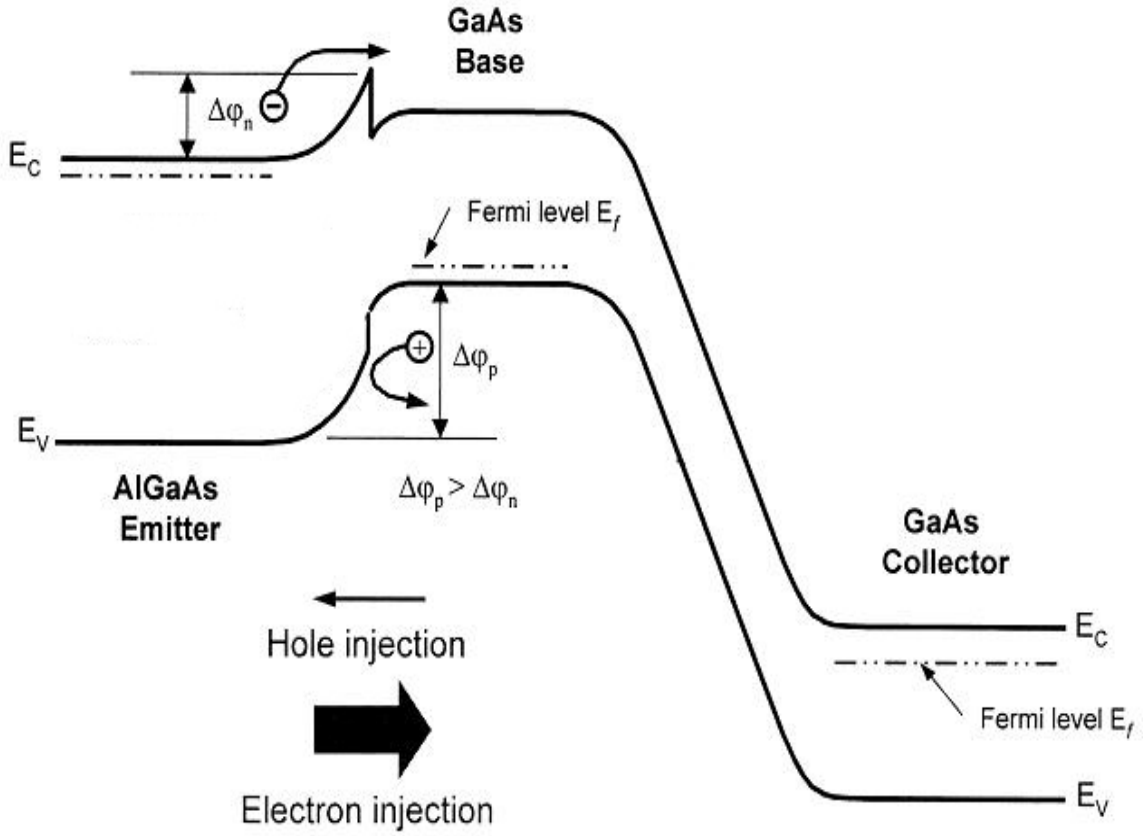


Fig11. Energy band diagram of an HBT structure

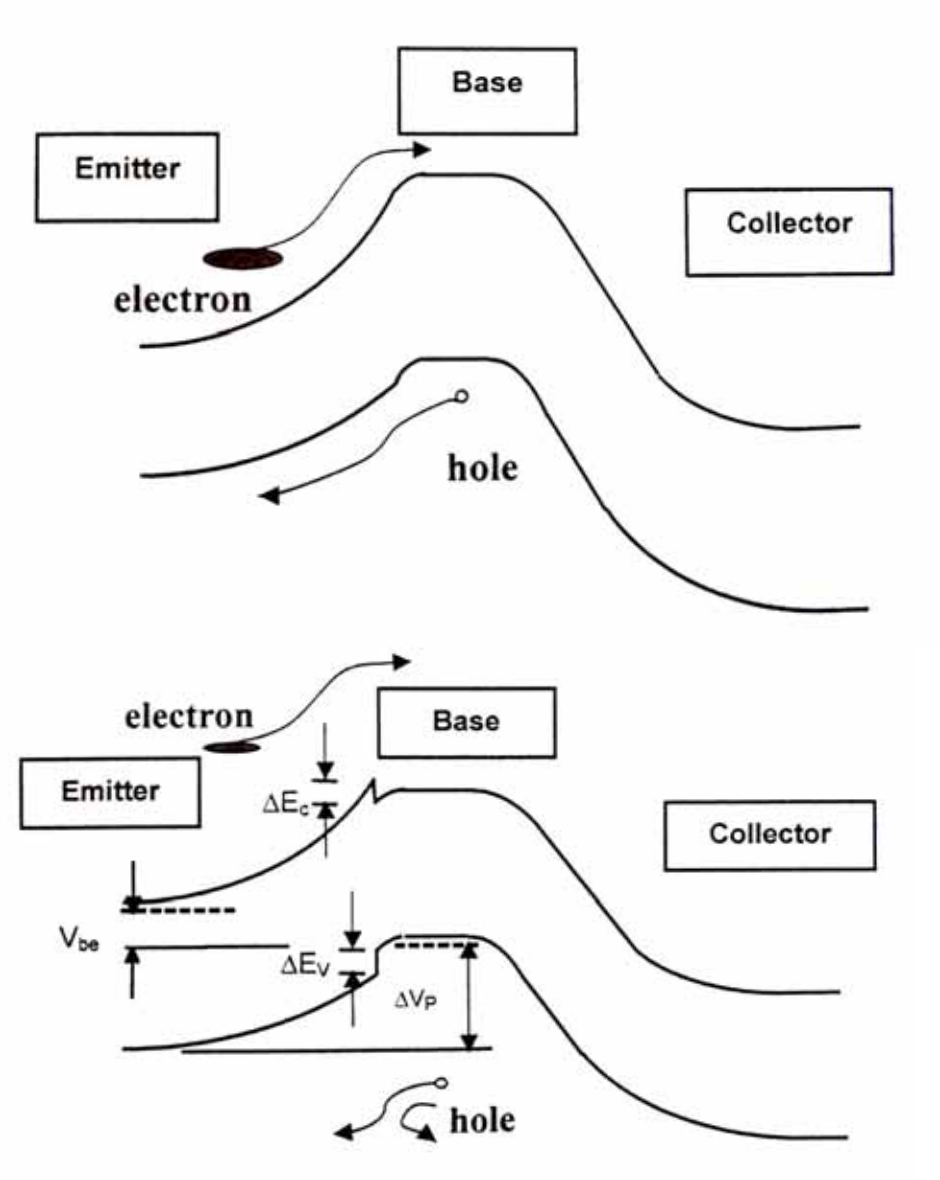


Fig12. The band diagrams of (a) a homojunction bipolar transistor and (b) a heterojunction bipolar transistor.

Chapter 3
Experiment

The contents of our experiments can be divided into three parts. First, the Pd/Ge/Cu ohmic contact formation on n-type InGaAs was studied. Second, the Pd/Ge/Cu ohmic contact was applied on the InGaP/GaAs HBTs as the n-type InGaAs contact metal to form Au-free fully Cu-metallized InGaP/GaAs HBTs. Third, material analysis and electrical characterizations of the devices were performed.

3.1 Research of Ohmic Contact

The specific contact resistances of the n-InGaAs/ Pd (15nm)/ Ge (150nm)/ Cu (150nm) were carried out by transmission line (TLM) method. The TLM patterns were fabricated by I-line photolithography. The InGaAs mesa was etched by $H_3PO_4/H_2O_2/H_2O$ solutions. After the conventional organic solvent cleaning process, the substrates were chemically cleaned in a solution of HCl：H_2O (1：1 by volume) to remove the native surface oxide layer, the samples were load into the evaporation chamber. Pd (15nm)/ Ge (150nm)/ Cu (150nm) compositions were then deposited on the substrates using an electron-beam evaporator in a pressure of ~$1x10^{-6}$ Torr. After the metal evaporation, the samples were immersed into ACE and IPA with the common lift-off process, followed by a high pressure DI water rinse to remove the residues. After lift off, the samples were annealed in a conventional tube furnace at various temperatures from 150^{o}C to 450 ^{o}C for 20 minutes.

The thermal stability test of the Pd/Ge/Cu ohmic contact was performed by high-temperature annealing test (250^{o}C) in a N_2-ambient tube furnace for 24 hours. The ohmic contact resistances (R_C) of the samples were measured using the transmission line model (TLM). The sheet resistance (R_{sh}) is directly measured using a four-terminal sensing measurement (also known as a four-point probe measurement (Fig18)) for the sample treatment at different temperature.

So as to understand the formation mechanism of Pd/Ge/Cu ohmic contact, the Pd/Ge/Cu multilayer was analyzed by XRD, TEM, AES, and AFM. Phase identification was analyzed by the X-ray diffraction (XRD). The interface microstructure of the n-InGaAs/Pd/Ge/Cu ohmic contact materials was observed by transmission electron microscopy (TEM) and the interfacial elements analysis was studied by using Auger electron spectroscopy (AES). The surface morphology was observed by atomic force microscope (AFM).

3.2 Device Structure and Fabrication

3.2.1 Device Structure

The epitaxial layers of the InGaP/GaAs single heterojunction bipolar transistors (SHBTs) with InGaAs cap layer were grown by molecular beam epitaxy (MOCVD) on semi-insulating (100) GaAs substrate. The InGaP/GaAs HBT epitaxial layer structure is shown in Table 3.The GaAs subcollector layer was grown on a 3-inch diameter semi-insulating substrate, and it was heavily

doped to reduce the *n*-type ohmic contact resistance. The lightly *n*-type doped GaAs collector layer and the heavily *p*-type doped GaAs base layer were grown on it subsequently. The emitter layer is InGaP, and the heavily doped GaAs/InGaAs layer on the top serves as the ohmic cap layer.

3.2.2 Device Fabrication

The details of the Cu-metallized InGaP/GaAs HBT device fabrication are described as follows. Besides, the traditional Au-metallized InGaP/GaAs HBTs which use Au/Ge/Ni/Au and Pt/Ti/Pt/Au as *n*-type and *p*-type ohmic contacts metals and Ti/Au as the interconnect metal were also fabricated for comparison. The flow charts of the process flow for device fabrication were shown in Figure 13.

(1) Wafer Cleaning:

The wafers were immersed into ACE and IPA separately, each for five minutes to remove any contaminants from the wafer surface, and then they were blown to dry by nitrogen gas.

(2) Emitter Mesa, Collector Mesa, and Isolation:

The InGaP/GaAs HBT devices were fabricated using a standard triple mesa process. The GaAs and InGaAs layers were etched by etchant composed of phosphoric acid, hydrogen peroxide, and D.I. water. And the InGaP layer was etched by a mixture of phosphoric acid and hydrogen chloride acid. The $Al_{0.3}GaAs$ was etched by CA (Citric acid). After each etching process, the devices were rinsed by D.I. water and blown dry by nitrogen gas. The first step of the fabrication was to define the emitter mesa area. The emitter mesa was etched and stopped

on the InGaP emitter layer. The collector mesa was etched and stopped on the GaAs subcollector layer. During the isolation etch, the GaAs subcollector was etched to the extent of undercut to separate each devices and to reduce the leakage current from the substrate. The process flow diagrams of the triple mesa process are shown in Figure 13.1-Figure 13.3.

(3) Emitter, Collector Metal deposition :

The metallization metals in this fabrication were all defined by AZ5214E photo resist. After the metallization, a standard lift off process was used to remove the unwanted metals. The emitter and collector ohmic contacts were Pd (15 nm)/Ge (150 nm)/Cu (150 nm). After the emitter and collector metal depositions, a high temperature alloying process using tube furnace was conducted to form the ohmic contacts. To confirm the alloying process, the ohmic contact resistance of device was measured in process control monitor by using the transmission line model (TLM) method. The diagram of the metal deposition process is shown in Figure 13.4.

(4) Base metal deposition:

For GaAs HBTs, the base layer is formed by GaAs with carbon doping to form p^+ type doping. In order to form ohmic contact on p^+-GaAs layer, the Pt (5 nm)/Ti (20 nm)/Pt (60 nm)/Cu (100 nm) was used. Before the deposition of the base metal, the material of GaAs emitter layer under the base ohmic contact photo-resist opening was etched to expose the underlying base layer. The metals were all deposited by e-gun evaporator and completed by lift off process. The

diagram of the process flow of the base metal deposition is shown in Figure 13.5

(6) Passivation, Contact Via, and Metal Line:

Device passivation was realized by 100 nm PECVD silicon nitride film. This passivation protects the critical area of the originally exposed wafer surface from humidity, chemicals, gases, and particles. Passivation Vias between ohmic contact metals and interconnect metals were etched by reactive ionic etcher (RIE). The schematics of the device passivation and contact via are as shown in Figure 13.6-Figure 13.7. After opening the connecting via on the nitride film, the Ti (30 nm)/Pt (60 nm) and interconnect Cu (400 nm) metals were sequentially deposited by e-gun evaporator over patterned resist. The metals were then removed by an ACE wet solvent lift-off process, followed by a high pressure DI water rinse to remove the residues. The schematic of the finished device is as shown in Figure 13.8. After all process, the DC and Power characteristics of the HBT devices were measured. The devices were stressed using a current-accelerated test for reliability evaluation.

3.3 Specific Contact Resistance Measurement

The transmission line method (TLM) pattern, as illustrated in figure 14, was designed in the process control monitor (PCM) in order to measure the ohmic resistance and to identify the ohmic contact characteristics. The resistance between two adjacent electrodes is expressed by the following equation

$$R = 2R_C + R_S L/W$$

where R is measured resistance, R_C is contact resistance, R_S is sheet resistance of channel region, W is electrode width, and L is the space between electrodes.

The resistance between the two adjacent electrodes can be plotted as a function of the space between electrodes. In this study, the distances between TLM electrodes are, 2.5 um, 3.5 um, 4.5 um, and 6.5 um, respectively. The plot is shown in the figure 15. Extrapolating the data to L=0, one can calculate a value for the term R_C. The specific contact resistance ρ_C is defined by

$$\rho_C = \frac{W^2 R^2}{R_S}$$

3.4 Material Analysis

3.4.1 X-ray Diffraction

The phase transformation of samples annealed at different temperatures was identified by SEIMENS D5000 X-ray diffractometer. *X*-rays are not readily reflected by crystal surfaces like a mirror, rather they are scattered through many atomic layers. *X*-rays can appear to be reflected by ordered layers of atoms or molecules if the distance between the layers, as seen from the oblique viewpoint of an incoming *X*-ray, is the same as the X-ray wavelength. The scattered *X*-rays from each layer reinforce in the direction of a detector positioned as though it was going to collect a reflected signal. Knowing the combined angle of tilt (2theta) of the *X*-ray source and the detector relative to the sample surface, the spacing between the atomic layers can be calculated, as long as the *X*-ray wavelength is known. This is the *d* spacing. It is directly related to the sine of the tilt angle.

There are infinite sets of d spacings in a crystalline solid. Crystals typically

have many different atomic layers in different directions. Atoms or molecules occupying layers in some directions are densely packed with atoms (scattering centers). Stronger signals are observed than with less densely packed layers in other directions. A scan from 10 degrees to 80 degrees usually yields a diffraction pattern unique to that crystal.

The *X*-ray is from the K_α peak of Cu (K_α=1.5406Å) which is filtered by Ni-filter. The angle between the *X*-ray and the sample was fixed at about 2.5 degree. The detector scanned the samples between 2θ = 20~90 degrees.

3.4.2 Auger electron spectroscopy

Auger electron spectroscopy represents today the most important chemical surface analysis tool for conducting samples. AES is based on the use of primary electrons with typical energies between 3 and 30 keV and the possibility to focus and scan the primary electron beam in the nanometer and micrometer range analyzing the top-most atomic layers of matter. Auger electrons render information essentially on the elemental composition of the first 2-10 atomic layers. Figure16 shows schematically the distribution of electrons, i.e. primary, backscattered and Auger electrons together with the emitted characteristic *X*-rays under electron bombardment. Under typical experimental conditions the latter have a larger escape depth due to a much smaller ionization cross section with matter, i.e. a higher probability to escape matter. Auger electrons with energies up to 2 keV, however, have a high probability to escape only from the first few monolayers because of their restricted kinetic energy. Consequently, they are much better suited for surface analysis. A second important detail shown in figure16 reveals that the diameter of the analyzed zone can be larger

than the diameter of the primary beam due to scattering of electrons.For depth profile analysis, AES combines with ion beam sputtering yielding in-depth information beyond the escape depth limit of a few nm of the Auger electrons. Sputtering is done either simultaneous or alternating ion bombardment of a raster scanned noble ion beam of known beam energy and current over the samples surface. The ion beam has to be well aligned with the electron beam in order to avoid crater edge effects. Auger analysis should be performed in the center of the ion crater.

3.4.3 TEM and EDX

The transmission electron microscopy is analytical tool that allows detailed micro-structural examination through high-resolution and high-magnification imaging. It also enables the investigation of crystal structures, orientations and chemical compositions in phases, precipitates and contaminants through diffraction pattern, x-ray, and electron-energy analysis. In our experiment, we use JEOL HRTEM (JEM-2100F) for microstructure observation and EDX analysis. It can achieve magnifications of up to 800,000X and detail resolution below 1 nm. Quantitative and qualitative elemental analysis can be provided from features smaller than 2nm. TEM is one of the most powerful tool for material analysis. But sample preparing is always a difficult and time consuming process. Since the electron beam must trans-through the specimen and remain bright enough to get image, the specimen must be thinned to less than 100nm, and even less than 50nm for high resolution.

3.4.4 Atomic Force Microscopy

The AFM is commonly employed to detect changes in surface structure on

the atomic scale. The AFM has a cantilever which has a sharp, force-sensing tip at its end. It is the tip that interacts with the surface of the sample. As the interaction force between the cantilever tip and the surface varies, deflections are produced in the cantilever. These deflections may be measured, and used to compile a topographic image of the surface as shown in figure17

3.5 DC and Power Measurements

3.5.1 DC Measurements

The DC current-voltage (*I-V*) characteristics of the HBT devices were measured by HP4142B. The collector to emitter voltage (V_{CE}) was biased from 0 to 3 volts for the 3×20 um^2 and 4×20 um^2 emitter area HBT devices. During the measurement of the *I-V* curves, there were three probes contacted onto the pads of emitter, base and collector.

In this study, the DC characteristics (common emitter I-V curve and gummel plot) of the Cu-metallized InGaP/GaAs HBT with Pd/Ge/Cu ohmic contact were compared with the traditional Au-metallized HBT.

Fully Cu-metallized InGaP/GaAs HBT with Pd/Ge/Cu ohmic contact were tested by using current accelerated test for reliability evaluation. The high current test was performed at a high emitter current density of 100kA/cm^2 at collector-emitter voltage of 1.5V for 24 hours.

3.5.2 Power Measurements

The power performance of the HBTs was measured at 2 GHz by using a load-pull system. The bias conditions of the base current and the collector

voltage were 0.03mA~0.15mA and V_{CE} = 2.4 V, respectively for the 4×20 um^2 emitter area HBT devices.

3.5.3 Reliability Test

Fully Cu-metallized InGaP/GaAs HBT with Pd/Ge/Cu ohmic contact were tested by using current accelerated test for reliability evaluation. The high current test was performed at a high emitter current density of 100kA/cm^2 at collector-emitter voltage of 1.5V for 24 hours.

Table

Table 3 The typical epitaxial layer structure of the InGaP/GaAs HBT

Layer	Material	Type	Doping	Thickness（Å）
Emitter Cap	$In_{0.6}GaAs$	*n*+	1×10^{19}	800
Emitter Cap	GaAs	*n*+	4×10^{18}	1250
Emitter	InGaP	*n*	3×10^{17}	500
Base	GaAs	*p*+	4×10^{19}	800
Collector	GaAs	*n*-	4×10^{16}	7500
Etch stop layer	InGaP	*n*	1×10^{18}	200
Subcollector	GaAs	*n*+	4×10^{18}	5000
	$Al_{0.3}GaAs$		undoped	1800
Substrate	GaAs			

Figure

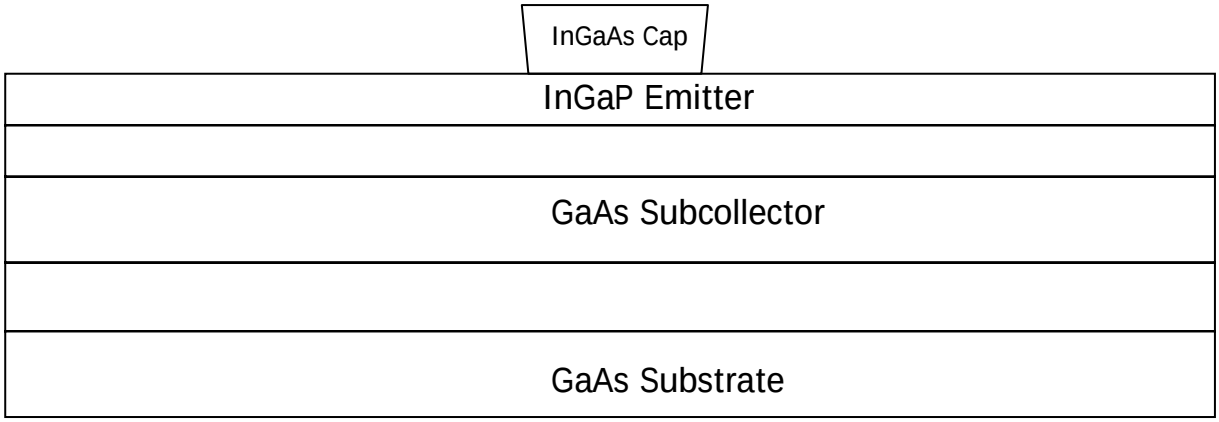


Fig 12.1 Emitter mesa etch

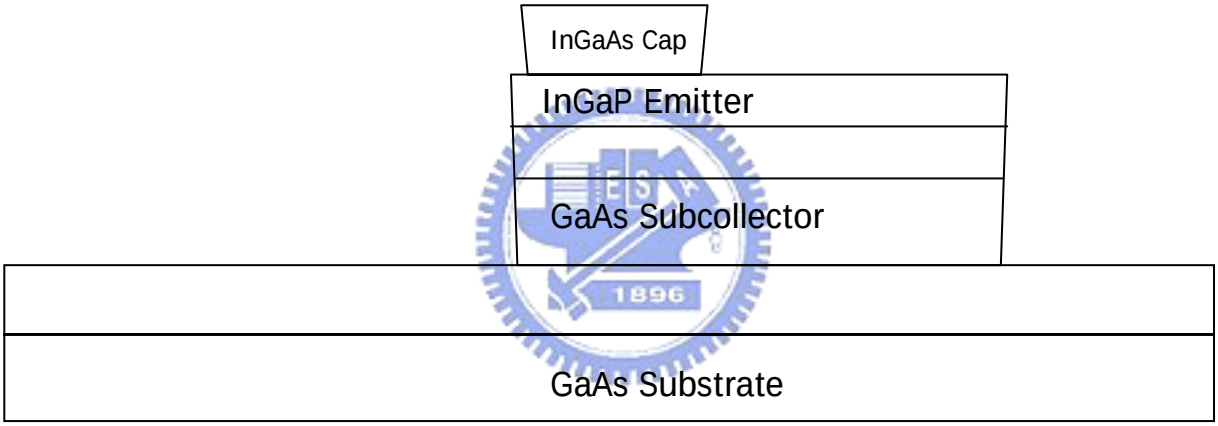


Fig 13.2 Base and collector mesa etch

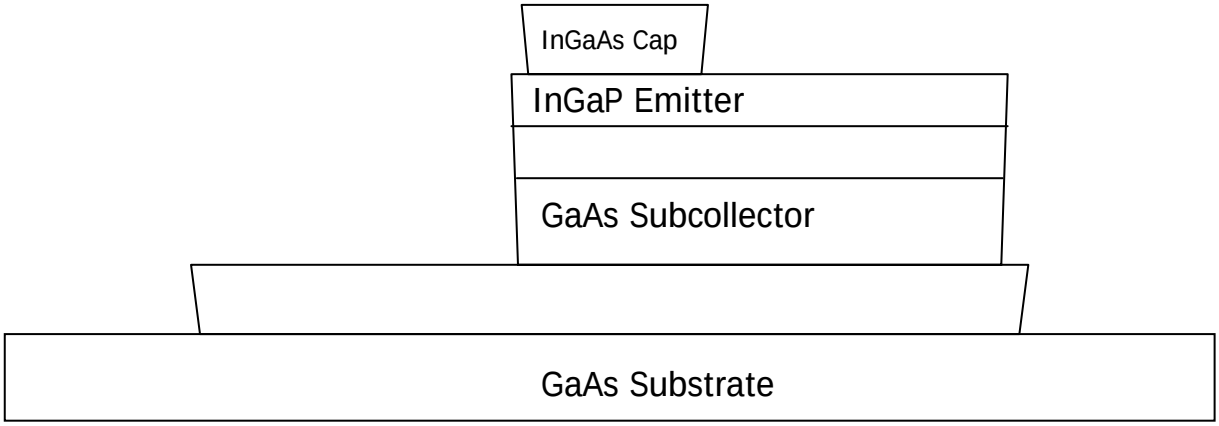


Fig 13.3 Mesa isolation

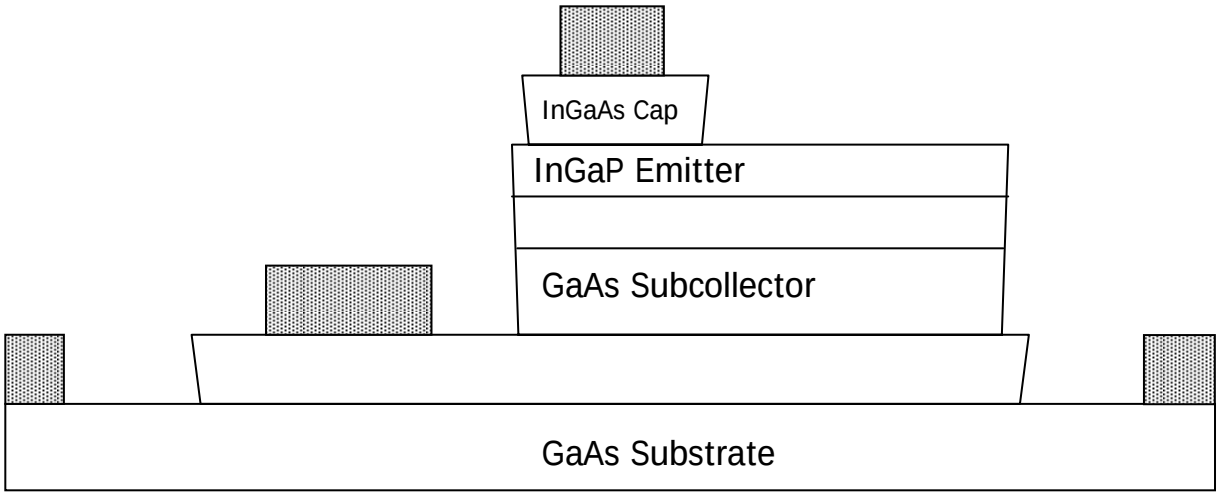


Fig 13.4 Emitter and collector ohmic contact metal formation

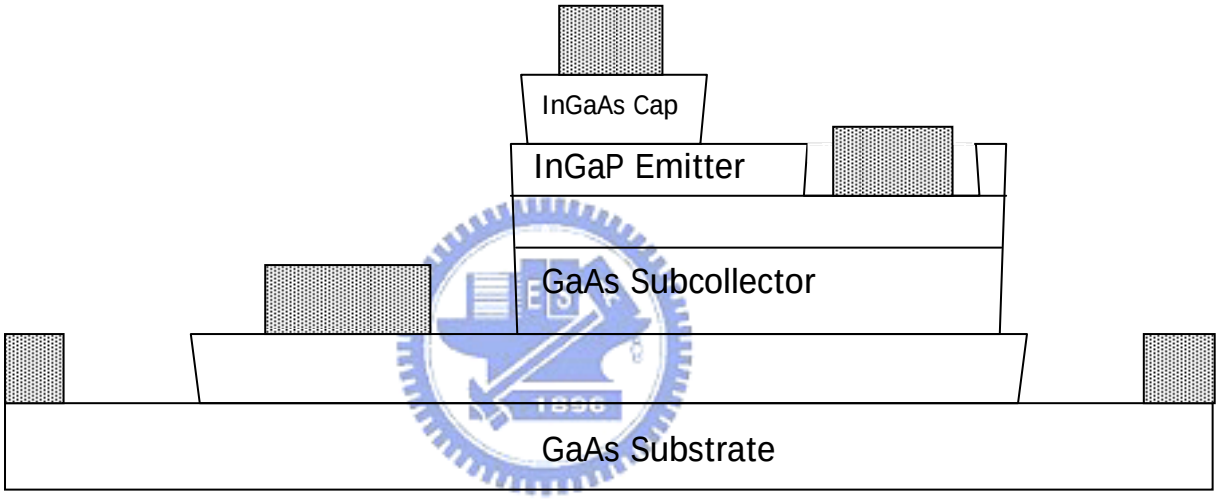


Fig 13.5 Base ohmic contact metal formation

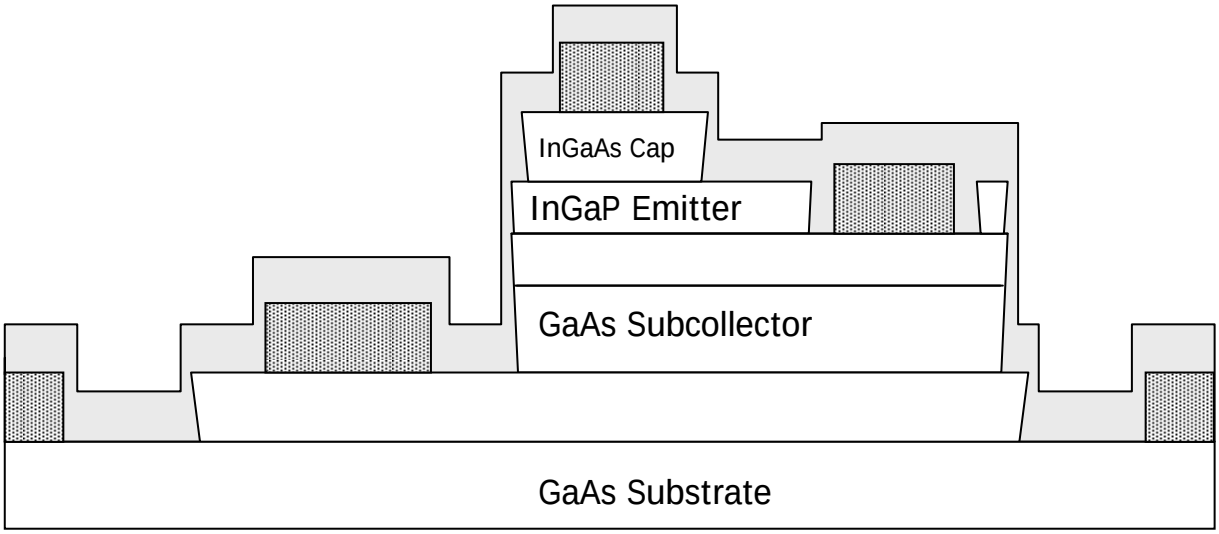


Fig 13.6 Silicon Nitride Deposition

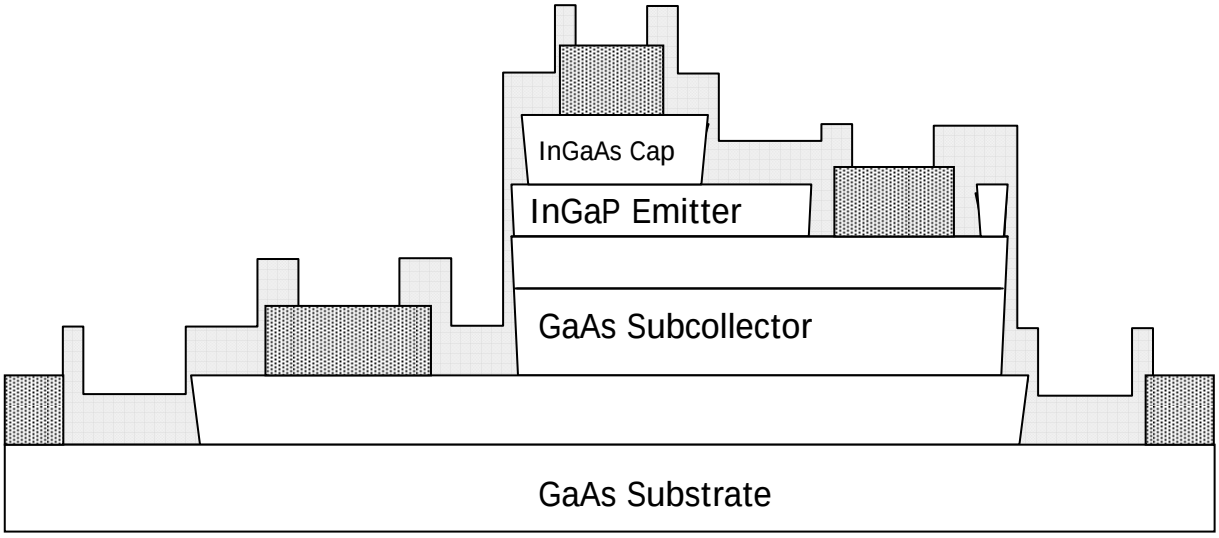


Fig 13.7 Nitride via etch

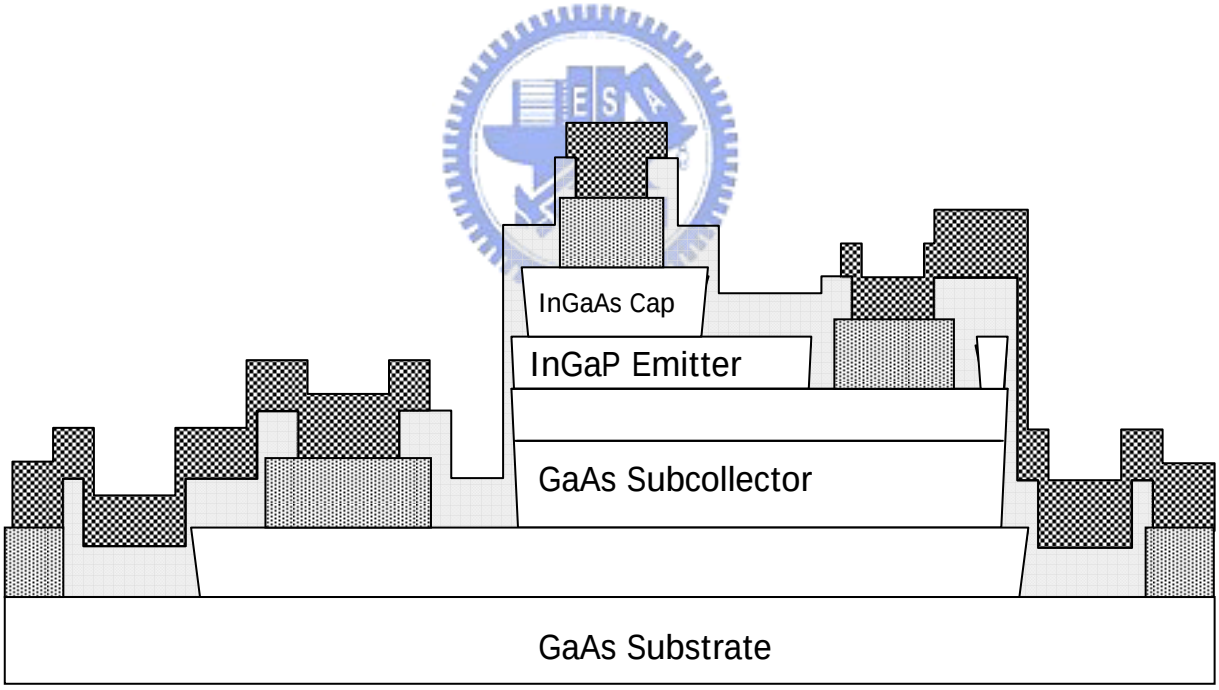


Fig 13.8 Interconnect metal line

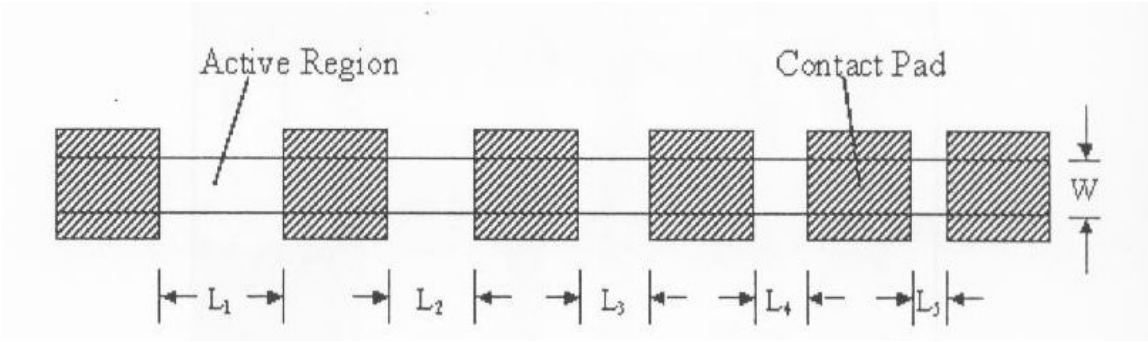


Fig14. Illustration of transmission line methods (TLM) patterns

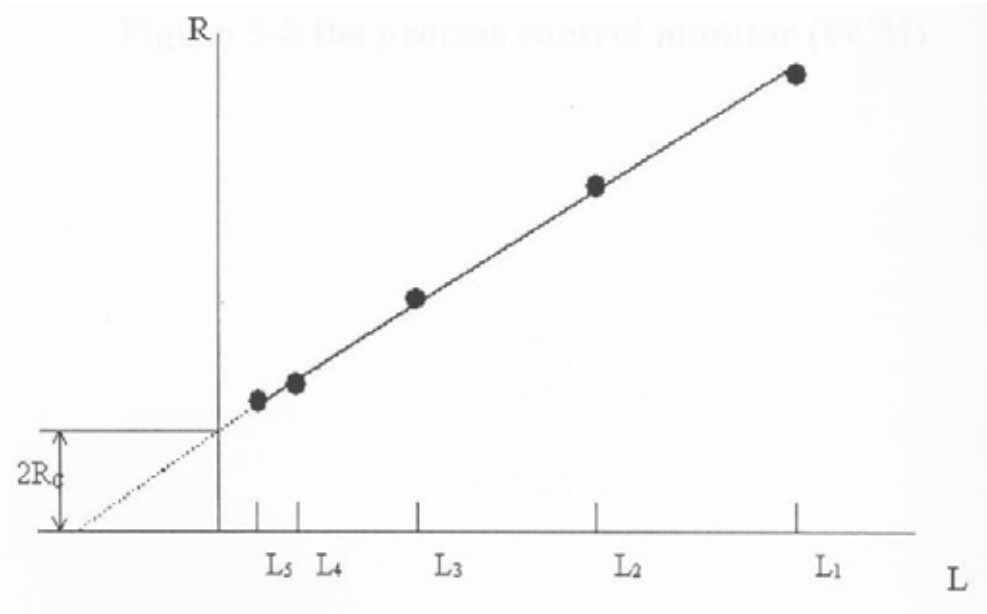


Fig15. Illustration of utilizing TLM identify ohmic contact resistance

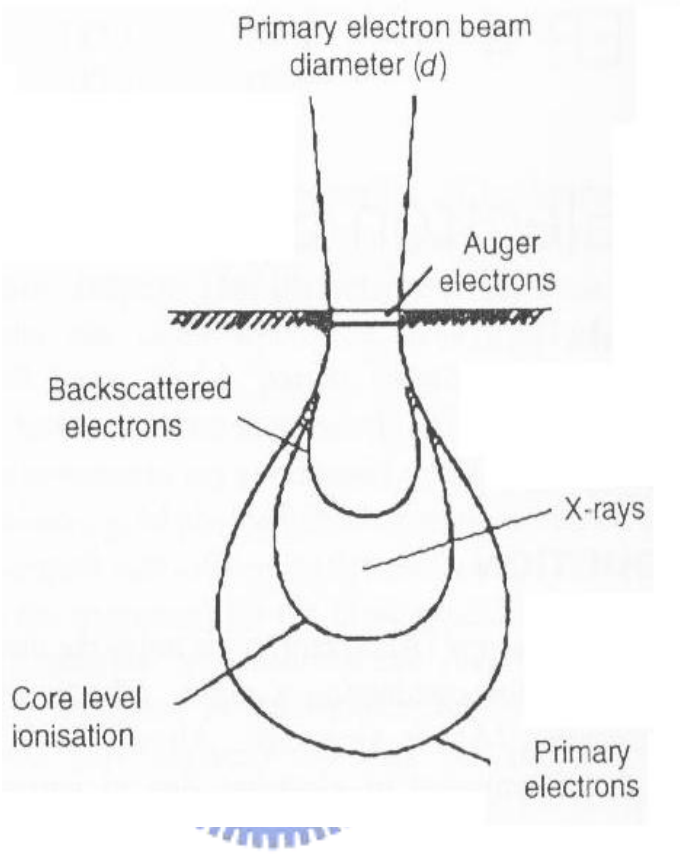


Fig16. Distribution schematic of primary, backscattered and Auger electrons together with X-rays

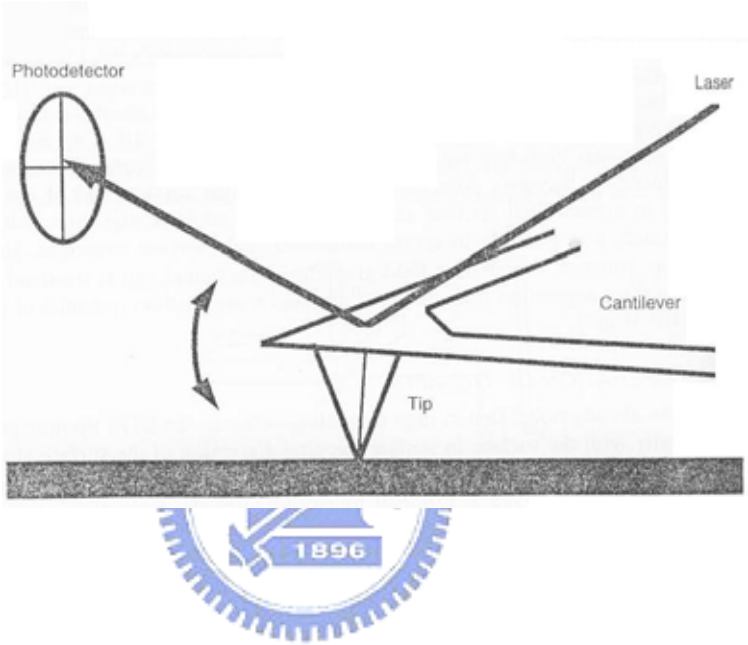


Fig17. Schematic illustration of the operation of the AFM

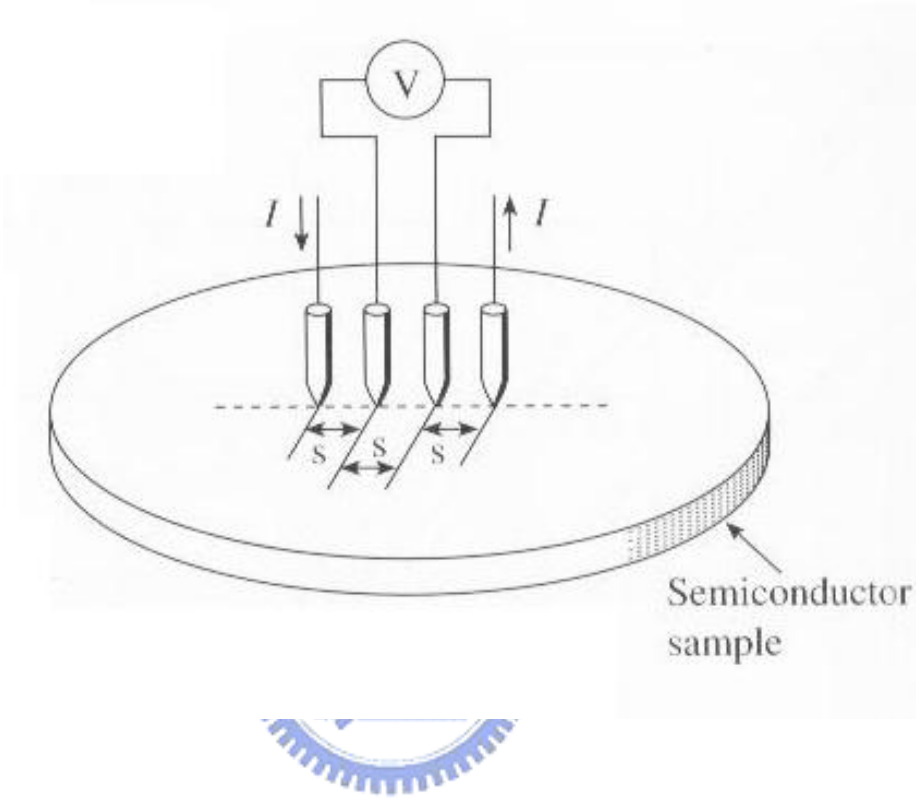


Fig18. Illustration of four-point probes technique

Chapter 4
Results and Discussion

In this chapter, the results of Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) ohmic contact on n-type InGaAs are discussed. The formation mechanism of the Pd/Ge/Cu ohmic contact was evaluated based on the results of XRD, AES, AFM, TEM and EDX. In the last half of the chapter, the results of DC and Power measurements of fully Cu-metallized InGaP/GaAs HBT with InGaAs cap layer using Pd/Ge/Cu ohmic contact are presented.

4.1 Contact Resisitivity of The Pd/Ge/Cu Ohmic Contact

The Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) multilayer metals were deposited on the InGaAs wafer with Si-doped epitaxial layer (1250 Å, $1x10^{19}$ cm^{-3}). The results of the contact resistivities of the Pd(150 Å)/Ge(1500 Å)/Cu(1500 Å) ohmic contact extracted from the transmission line measurements (TLM) as a function of annealing temperature after annealing in a traditional tube furnace at different temperatures for 20 min are shown in Figure 19. Low ohmic contact resisitivity can be obtained when the Pd/Ge/Cu ohmic samples were annealed at 200°C ~ 300°C for 20 min. The lowest specific contact resistivity was 1.0×10^{-6} Ω-cm^2 after the sample was annealed at 250 °C for 20 min.

4.2 Formation Mechanism of The Pd/Ge/Cu Ohmic Contact

The formation mechanism of the Pd/Ge/Cu ohmic contact was investigated by results of XRD, Auger, AFM, TEM and EDX. Use X-ray diffraction for phase identification, Auger for interfacial elements material analysis, TEM image and EDX analysis for microstructure observation, and AFM for surface morphology observation. The results are shown below.

4.2.1 X-ray Diffraction for Phase Identification

Figure 20 shows the x-ray diffraction profiles for the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) ohmic contact structure as deposited and after annealing at 150 °C, 250°C, 350°C, and 450 °C for 20 min. It can be seen from the XRD spectra that the diffraction peaks of Ge and Cu remained observable for the as deposited sample. It indicated that the Pd/Ge/Cu multi-layers did not react with each other for the as deposited sample. However, it is obvious from these data that the diffraction peaks of the Cu_3Ge compounds occurred and the diffraction peaks of Cu disappeared as the annealing temperature was higher than 250°C. The ohmic contact behavior was related to the formation of the Cu_3Ge compounds as the annealing temperature was above 250°C

4.2.2 Auger for interfacial elements material analysis

Figures 21(a) to (c) show the AES depth profiles of the InGaAs/Pd/Ge/Cu/Cr samples as-deposited and after 250^{o}C, and 450^{o}C annealing for 20 minutes. As can be seen from figures 21(b), there is no obvious atomic inter-diffusions between Pd and the InGaAs layer after annealing at temperature of 250^{o}C. However, Ge did diffuse into the InGaAs layer. It may

cause the high doping forming at the surface of InGaAs layer. The inter-diffusions occured between Cu and Ge, which can be seen for the XRD analysis at temperature of 250°C. However, as shown in Figure 21(c), after annealing at temperature of 450°C, the Cu atoms penetrated the Pd layer and diffused into the InGaAs layer, and the figure shows the serious intermixing of Cu, Ge, and the InGaAs layer. Furthermore, In atom diffused upward and only appeared on the surface of the sample. Supplementary evidence will be described from TEM and EDX data in the next section.

4.2.3 TEM image and EDX analysis

Figure 22 shows the TEM image of the as-deposited Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) structure deposited on InGaAs substrate. From this figure, the Pd, Ge, and Cu layers can be seen clearly. The thin Pd layer enhanced the adhesion of the ohmic metal and the Cr layer on the top was used as the anti-oxidation layer for Cu.

Figure 23 ~ Figure 25 shows the TEM images and EDX profiles of Pd/Ge/Cu ohmic metal structure after annealing at 250°C and 450°C for 20min respectively. The TEM image of the Pd/Ge/Cu ohmic metal structure after annealing at 250°C for 20 min is shown in Figure 23(a). From the figure, the Cu/Ge compound started to form grains with vertical grain boundary and long range order [27]. From the EDX analysis, the grains were Cu_3Ge compound as shown in Figure 23(b). Literature shows that the compound has low metallic resistivity and Ga has lower chemical potential in Cu_3Ge than in GaAs compound [27]. On the other hand, Figure 24(a) shows the HRTEM image of the near-interface region between InGaAs substrate and ohmic compound after 250°C annealing. The Pd_xGaAs phases started to appear at the InGaAs surface

after 250°C annealing. Due to the Pd_xGaAs compound, it may create more Ga vacancies. The Ge atoms could easily diffuse into the Ga vacancies in the vicinity of the InGaAs surface, resulting in a heavy doping n^+-InGaAs layer. So the ohmic contact characteristics of the Pd/Ge/Cu appeared after annealing at 250°C for 20 min.

The EDX profiles in Figure 24(b) show that there is still no Cu atom diffusing into GaAs the substrate near the Pd/InGaAs interface after 250 ℃ annealing.

However, after annealing at 450°C for 20 min, obvious atomic inter-diffusion and interfacial reactions started to occur as can be seen from Figure 25. The ohmic contact characteristics of the Pd/Ge/Cu ohmic system started to degrade after 450°C annealing, the possible reasons for ohmic contact degradation are As atoms diffused out and Ga atoms diffused into the Ge layer. (Ga atoms acted as acceptors which reduced the donor concentration.)

Figure 26 shows the EDX profiles of sample's surface after 450°C annealing. The out-diffusion of In atom would deteriorate the ohmic contact due to an increase in barrier height. The out-diffusion of As atom is also responsible for the degraded ohmic contact at 450℃ because it enhances the Ge atoms to occupy the As sites where they behave as acceptors.

4.2.4 AFM for surface morphology observation

Figure 27 is the AFM surface morphology of the as-deposited sample and samples subjected to annealing at temperature of 250°C and 450°C. The root-mean-square (rms) roughness of the sample as-deposited was 1.597 nm. The roughnesses of the samples annealed at temperature of 250°C and 450°C

were 2.058 nm and 2.918 nm, respectively. From the results of AFM, the surface of sample is rougher when the annealing temperature increases.

4.3 Thermal Stability Test for the Pd/Ge/Cu Ohmic Contact

To study the thermal stability of the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) ohmic contact, the Pd/Ge/Cu multilayer layer were annealed at 250°C for 24 hours and the specific contact resistivity was measured used TLM patterns. Figure 28 shows the long time thermal stability test results. From this figure, it can be seen that there was no obvious degradation on the Pd/Ge/Cu ohmic system after annealing at 250 ℃ for 24 hours. Figure 29 and Figure 30 show the thermal stability test of sheet resistance, and both of them have no obvious increase for high temperature test or log time annealing test.

4.4 DC and Power Measurements

4.4.1 DC Measurements

Figure 31 shows the optical microscope images of the fully Cu-metallized InGaP/GaAs HBTs with Pd/Ge/Cu ohmic contact after fabrication. Figure 32 shows the typical common emitter characteristics of HBTs with emitter area of 4 x 20μm^2. In the figure, one group of curves belongs to the fully Cu-metallized HBTs and the other belongs to the traditional Au-metallized HBTs. It can be seen from Figure 32 that these two devices show similar knee voltage and offset voltage. We did not observe an increase in the knee voltage or the decay of the collector current, which indicates that the characteristics of the InGaP/GaAs

HBTs with Pd/Ge/Cu ohmic contact are reasonably good. The common emitter current gain is around 110 for both cases. Gummel plots of the HBTs with the traditional Au HBT and Au free fully Cu HBT were also compared. The results are shown in Figure 33. The two HBTs also showed similar behaviors.

To test the reliability of the Pd/Ge/Cu as the n-type ohmic metal for the Cu-metallized HBTs, both copper and gold metallized HBTs with 4x20μm^2 emitter area were subjected to current accelerated stress test with high current density of 100 kA/cm^2. It is much higher than 25kA/cm^2 required for the normal device operation and the purpose is to shorten the stress time so that the stress tests could be performed at wafer level without using any package and the results could be obtained in a few hours [27]. Figure 34 plots the current gain (β) of the fully Cu-metallized HBTs with Pd/Ge/Cu ohmic contact after stressed at the high current density of 110 kA/cm^2 with V_{CE} of 2.5V for a period of 24 hours. The measurements were made at an amibient room temperature of T_A = 25°C. It can be seen from the data that the current gain of the device showed no significant change with time.

4.4.2 Power Measurements

The power performance of the HBTs was measured at 2 GHz by using a load–pull system. Measurements were carried out at collector current levels between 3 and 15 mA and V_{CE} = 2.4 V. The results of power measurement were shown in Figure35. For Au-HBTs, turning for maximum power-added efficiency (PAE) match, the output power (Pout) was 12.46 dBm and the maximum PAE was 46.2%, with the DC bias conditions of V_{CE} = 2.4 V and I_C =13mA . With the same DC bias conditions, Cu-HBTs, the output power (Pout) was 11.70dBm and the maximum PAE was 42.1%.

Figures

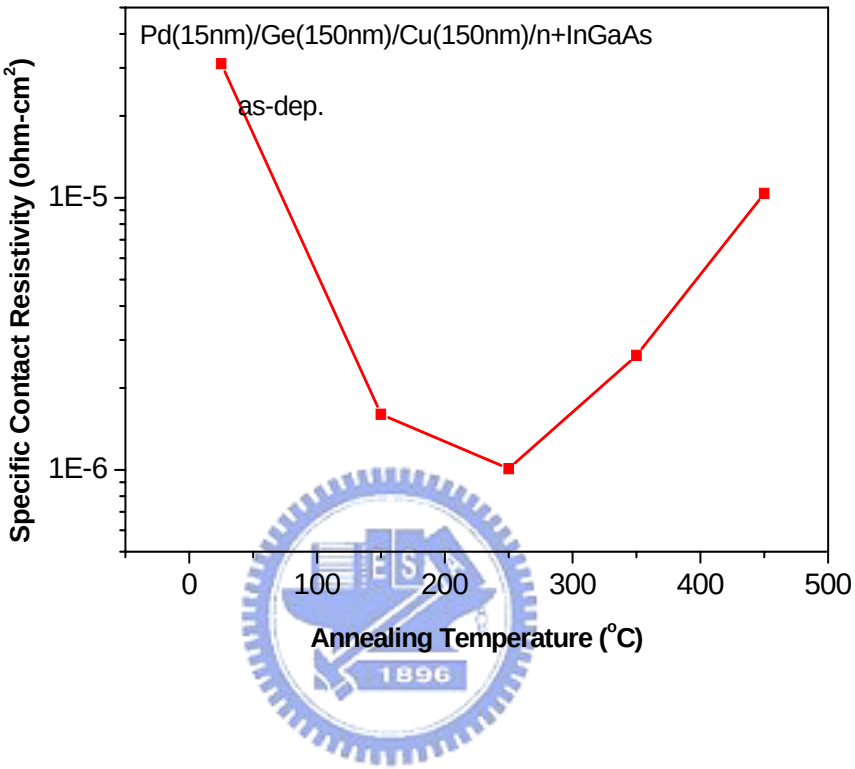


Fig19. The specific contact resistivity of the Pd(15nm) / Ge(150nm) / Cu(150nm) contact on n-type GaAs as a function of annealing temperature.

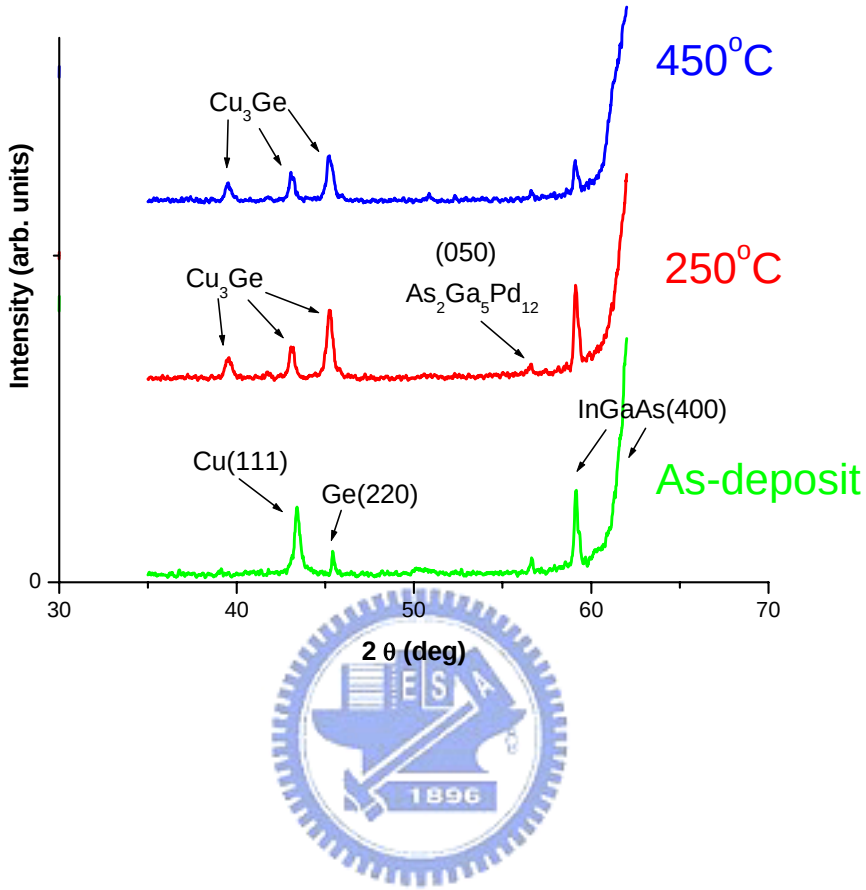


Fig20. The X-ray diffraction patterns for the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) contact after annealing at 250 °C for 20min, 450 °C for 20min, and the as-deposited sample.

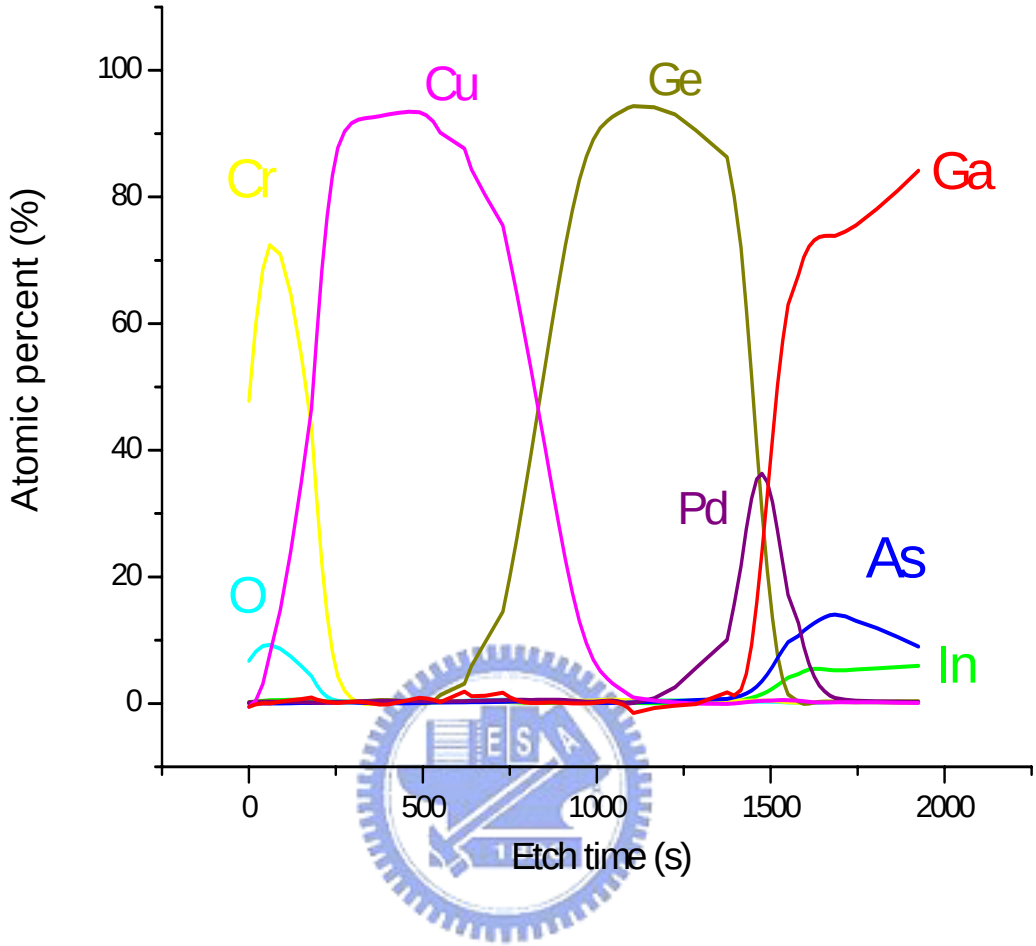


Fig21. (a) AES depth profiles of the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) contact for as-deposited sample

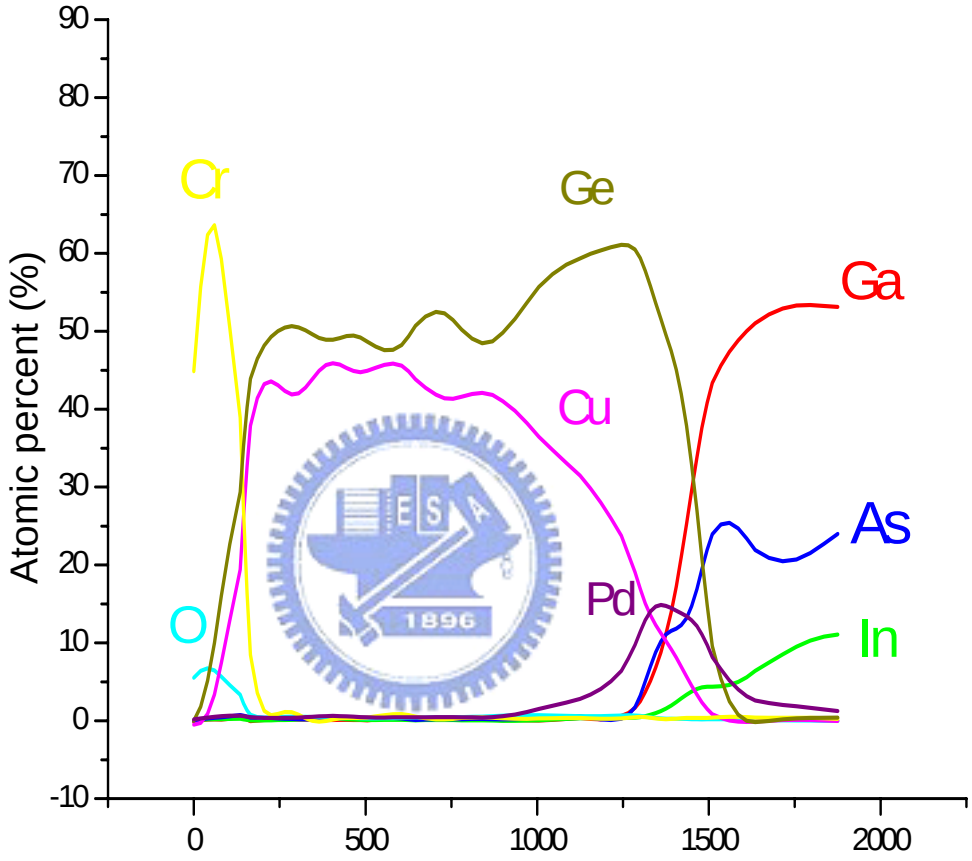


Fig21. (b) AES depth profiles of the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) contact for 250℃

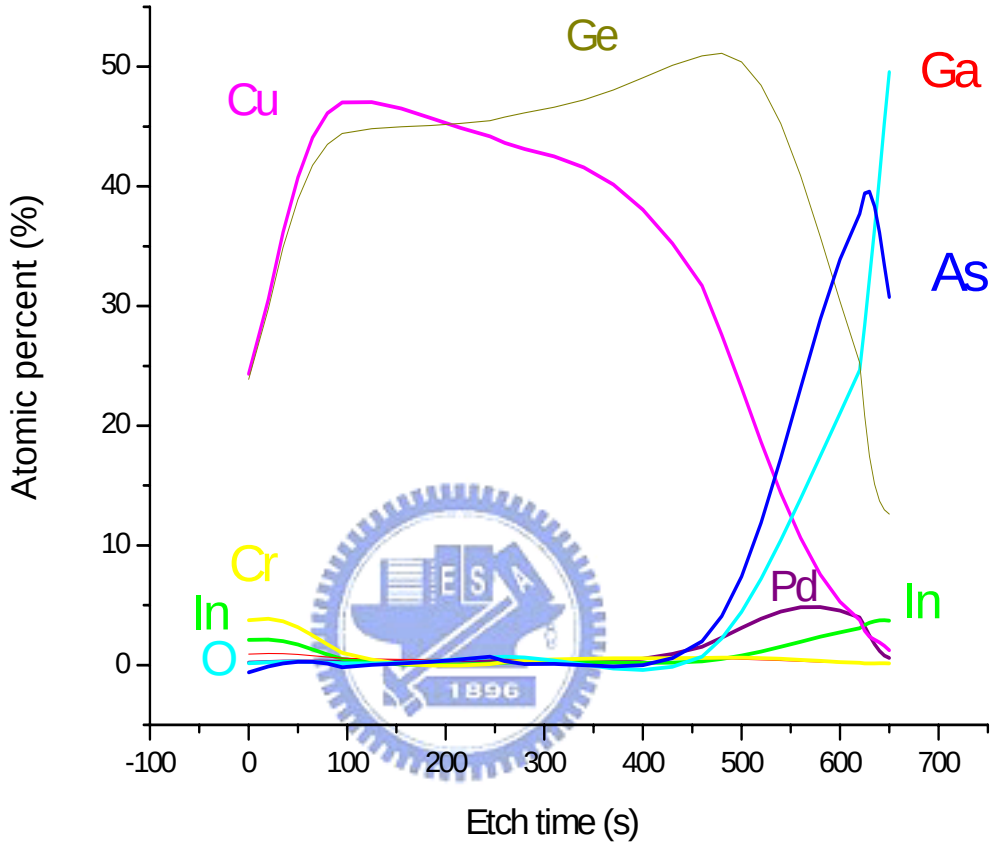


Fig21. (c) AES depth profiles of the Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) contact for 450℃

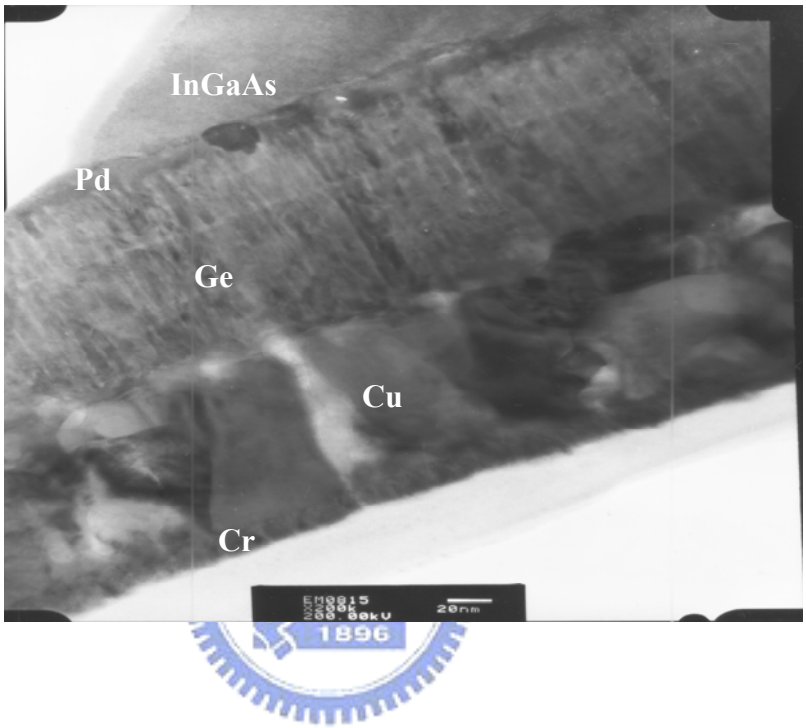
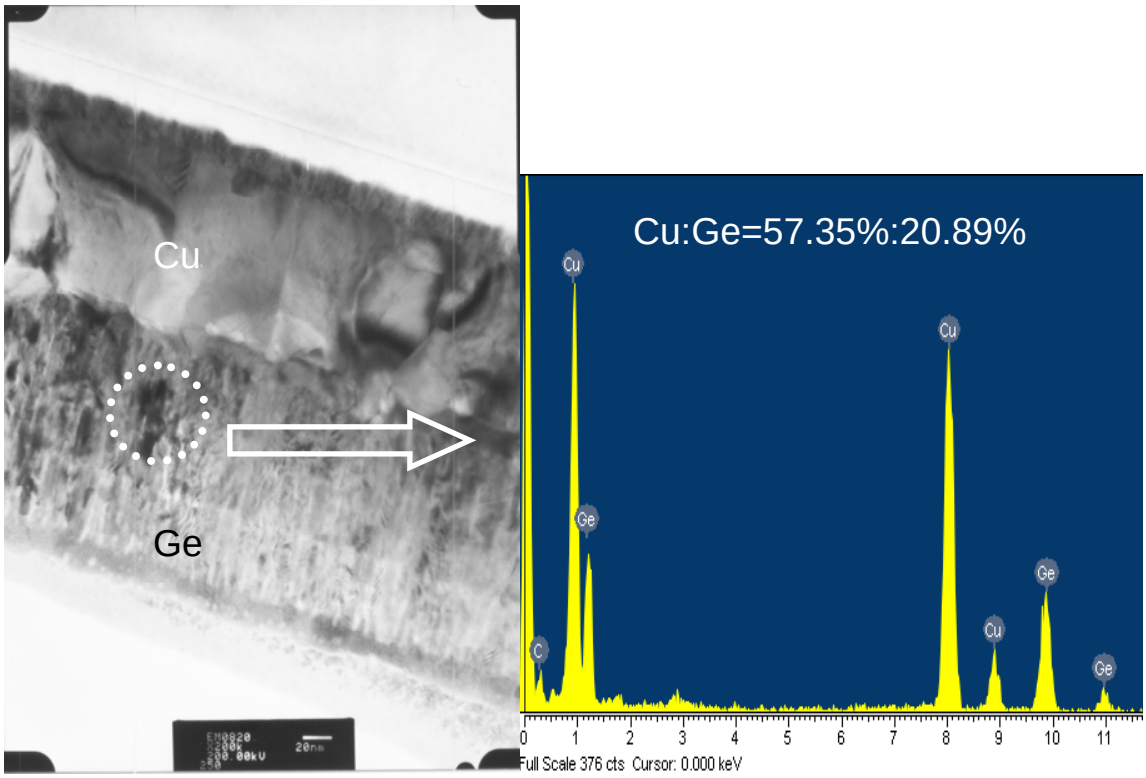


Fig22. The TEM image of the Pd(15nm) / Ge(150nm) / Cu(150nm) contact for the as-deposited sample.



(a) (b)

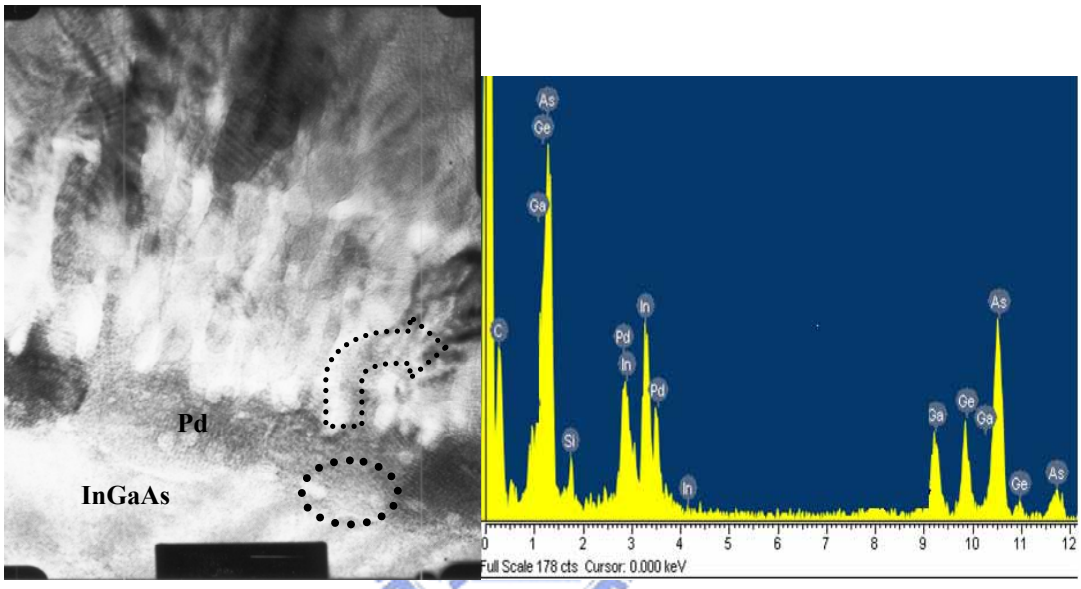
Fig23.

(a) The TEM image of the Pd/Ge/Cu contact cross section,

(b) The EDX profiles of the Ge/Cu compound grains

after annealing at 250℃ for 20 min.

Element	Ge	Pd	Ga	As	In
Atomic%	10.95	14.37	11.11	30.35	22.49
Weight%	9.31	17.91	9.07	26.64	30.25

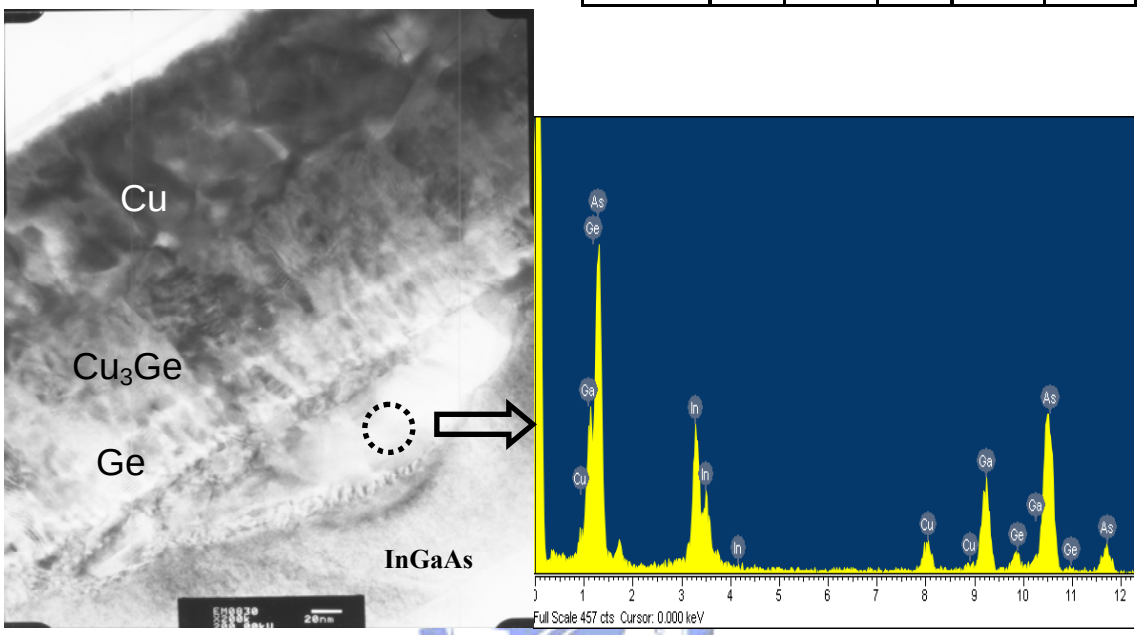


(a) (b)

Fig24. (a) The high resolution TEM image of the interface between the Pd metal layer and the InGaAs substrate after annealing at 250℃ for 20 min.

(b) The EDX profiles of the Pd/InGaAs interface after annealing at 250℃ for 20 min.

Element	Cu	Ga	Ge	As	In
Atomic%	6.19	19.81	3.77	43.07	27.16
Weight%	4.69	16.46	3.26	38.44	37.16



(a) **(b)**

Fig25.

(a) The TEM image of the Pd/Ge/Cu contact cross section,

(b) The EDX profiles of near the surface of InGaAs

after annealing at 450℃ for 20 min.

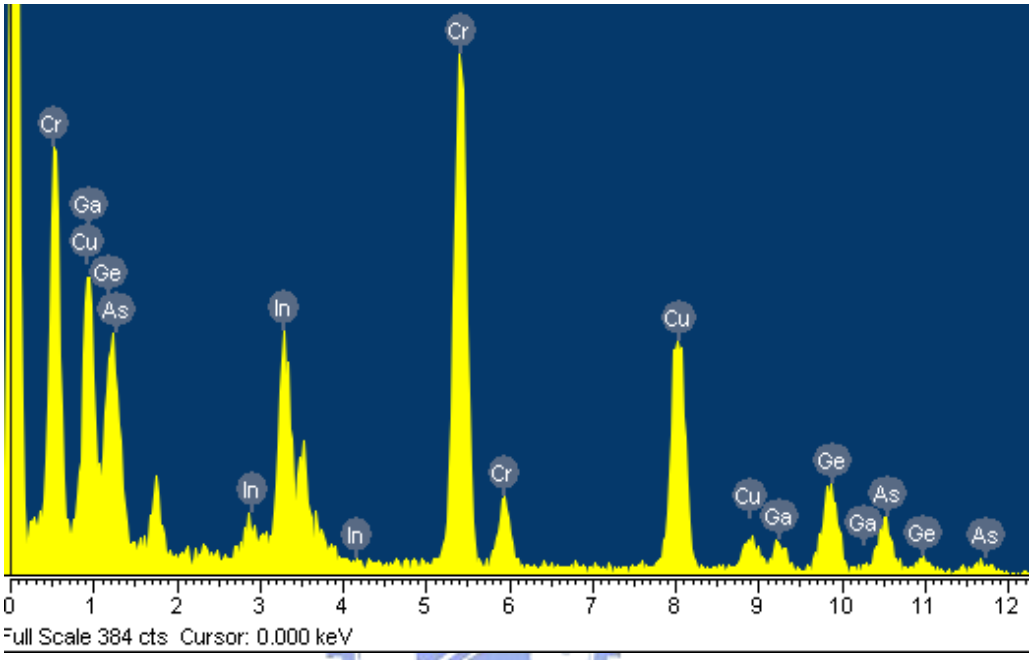
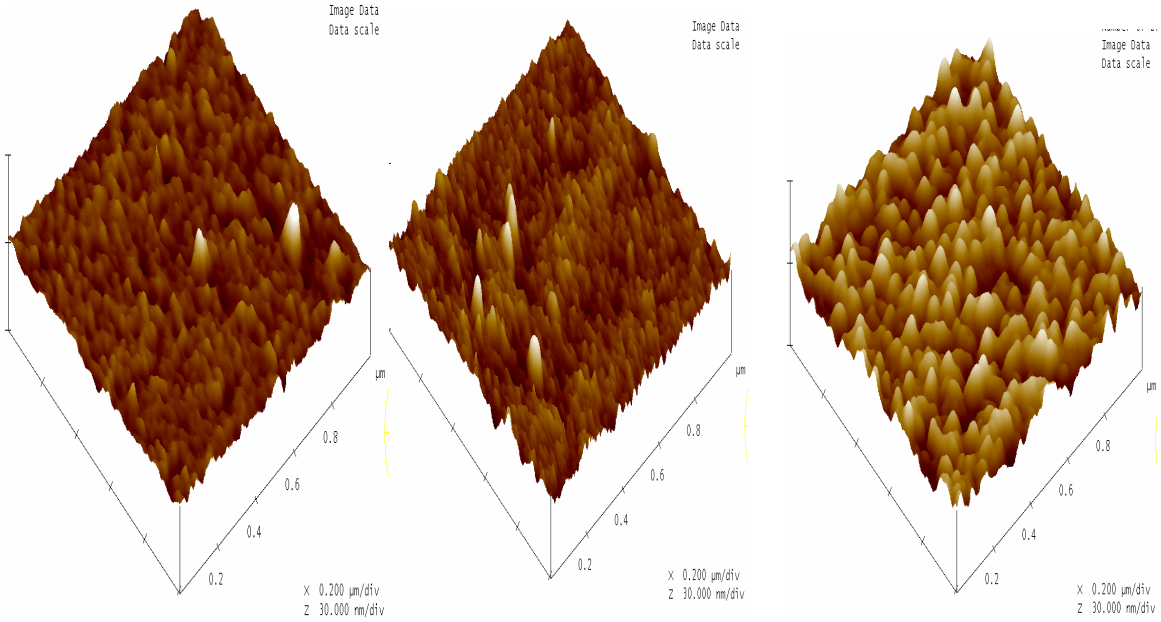


Fig26. The EDX profiles of sample's surface after annealing at 450℃ for 20 min.



(a)	(b)	(c)
As-deposit	**@250℃**	**@450℃**
Rms : 1.597 nm	**2.058 nm**	**2.918 nm**
(Ra) : 1.151 nm	**1.497 nm**	**2.344 nm**

Fig27. AFM Surface Morphology

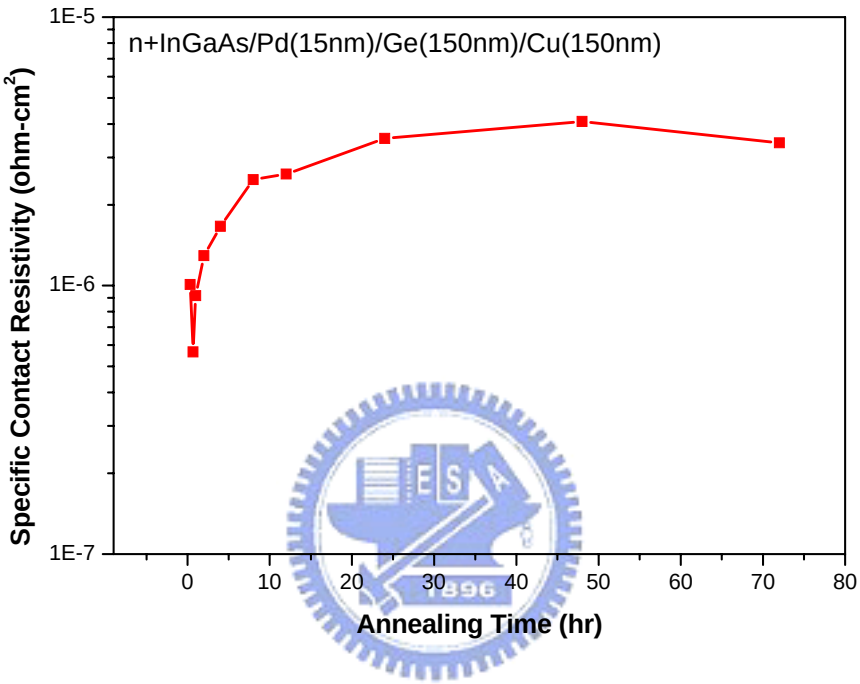


Fig28. The specific contact resistivities of the Pd/ Ge/ Cu ohmic contact on n-type InGaAs as a function of aging time.

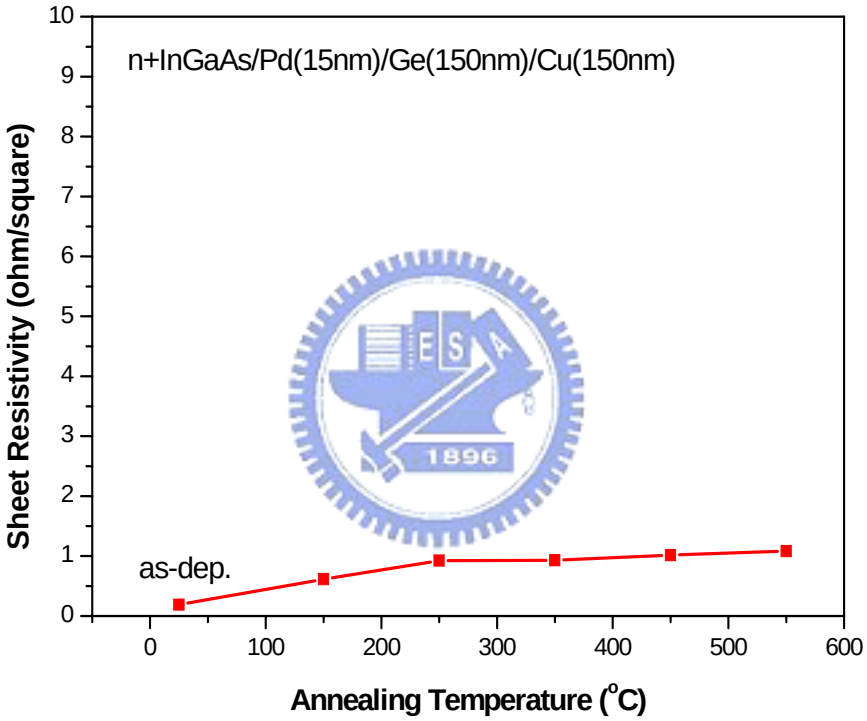


Fig29. Sheet Resistance of the n+InGaAs/Pd/Ge/Cu Structure annealed at different temperatures for 20 min.

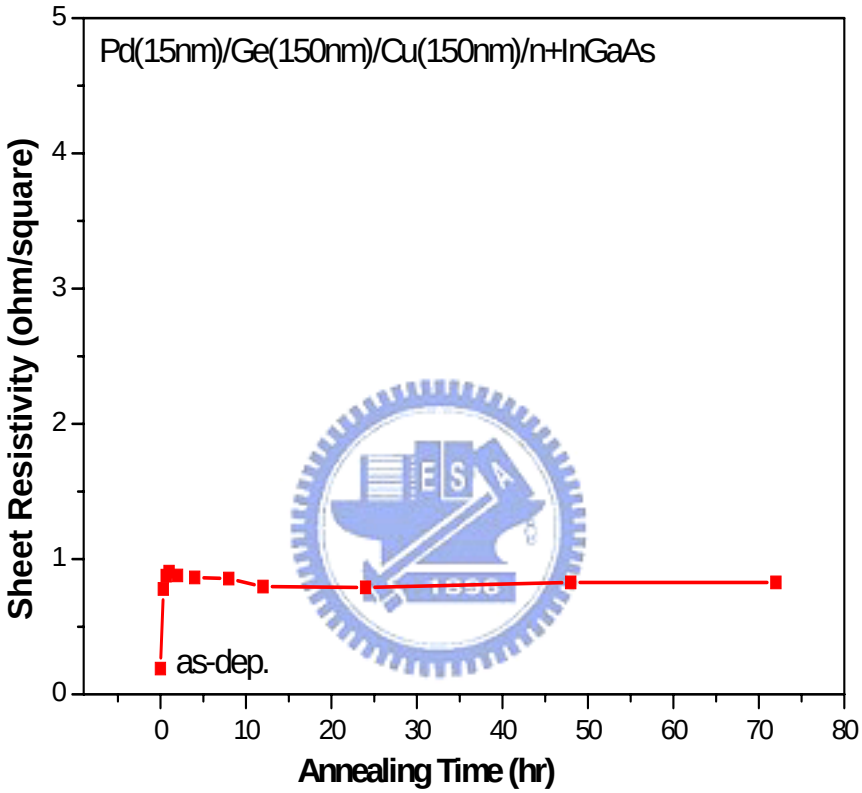


Fig30. Sheet Resistance of the n+InGaAs/Pd/Ge/Cu Structure annealed at 250℃ for long annealing time test.

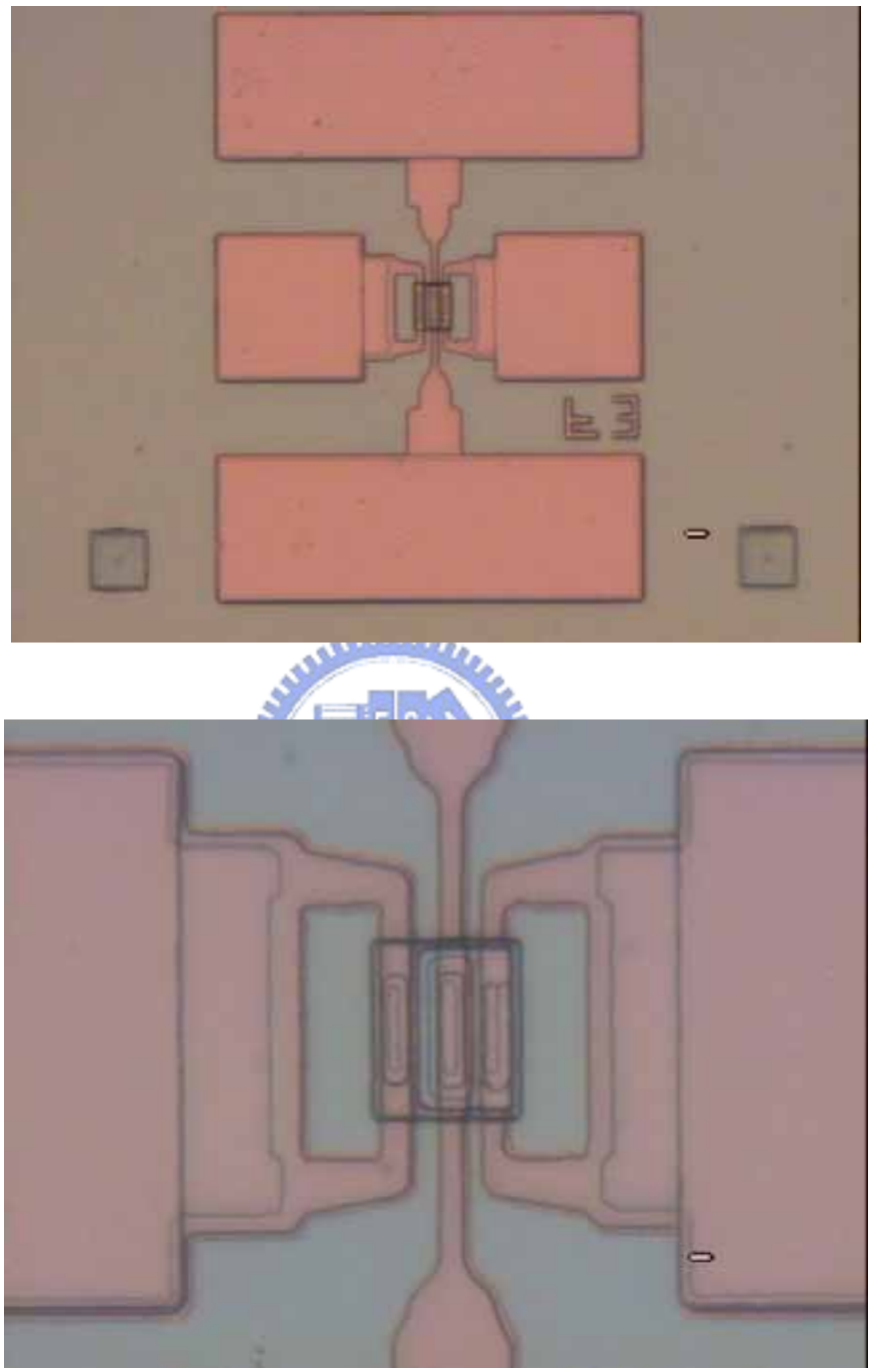


Fig31. The OM images of fully-Cu InGaP/GaAs HBT with Pd/Ge/Cu as n-type ohmic contact device.

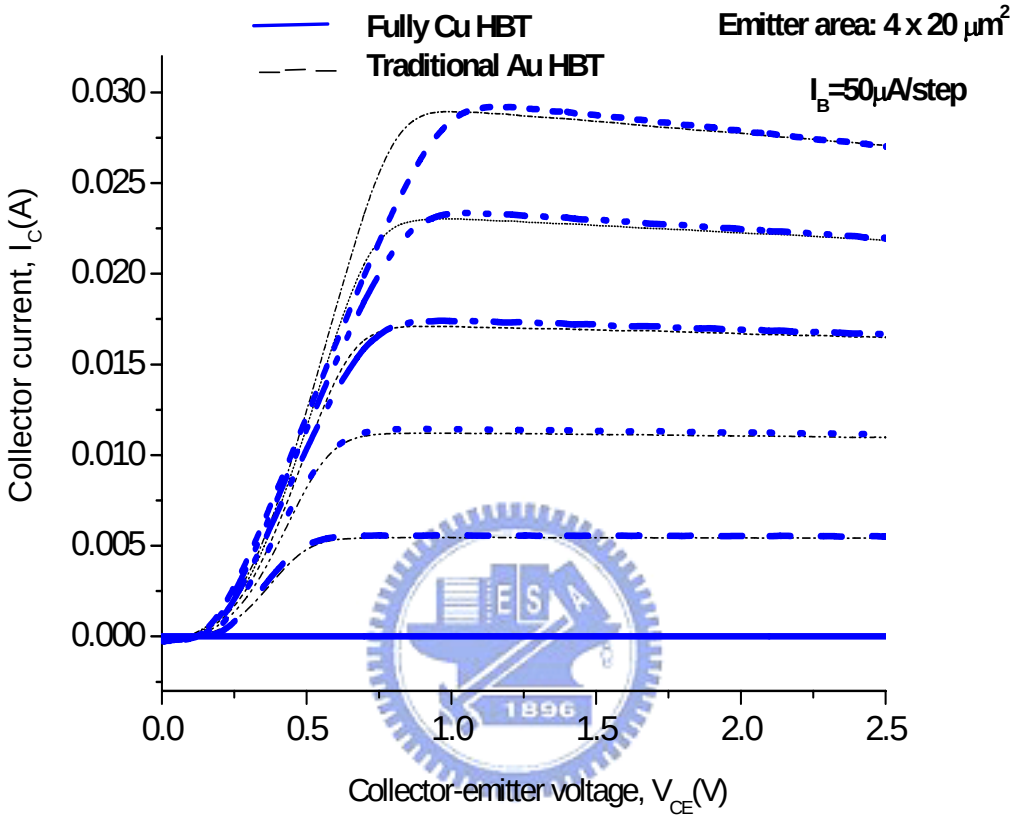


Fig32. Comparison of the typical I_C-V_{CE} characteristics for the emitter area (4 x 20 μ m^2) HBTs with Cu and with Au metallizations.

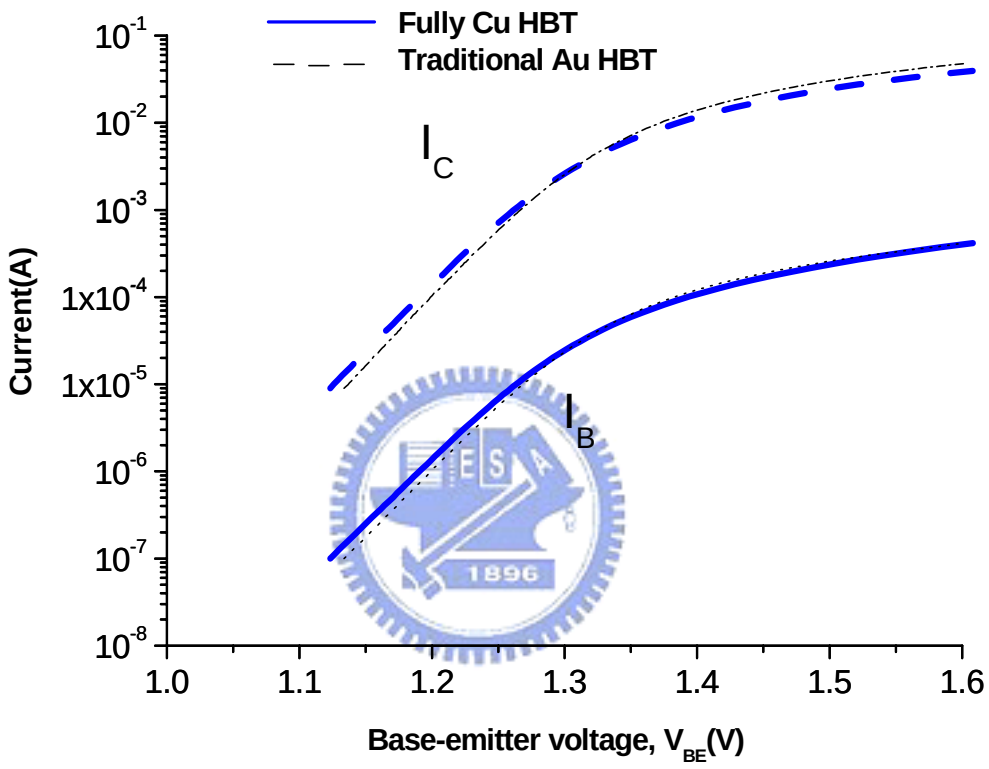


Fig33. Comparison of Gummel plots for the emitter area(4 x 20 μ m^2) HBTs with Cu and with Au metallizations.

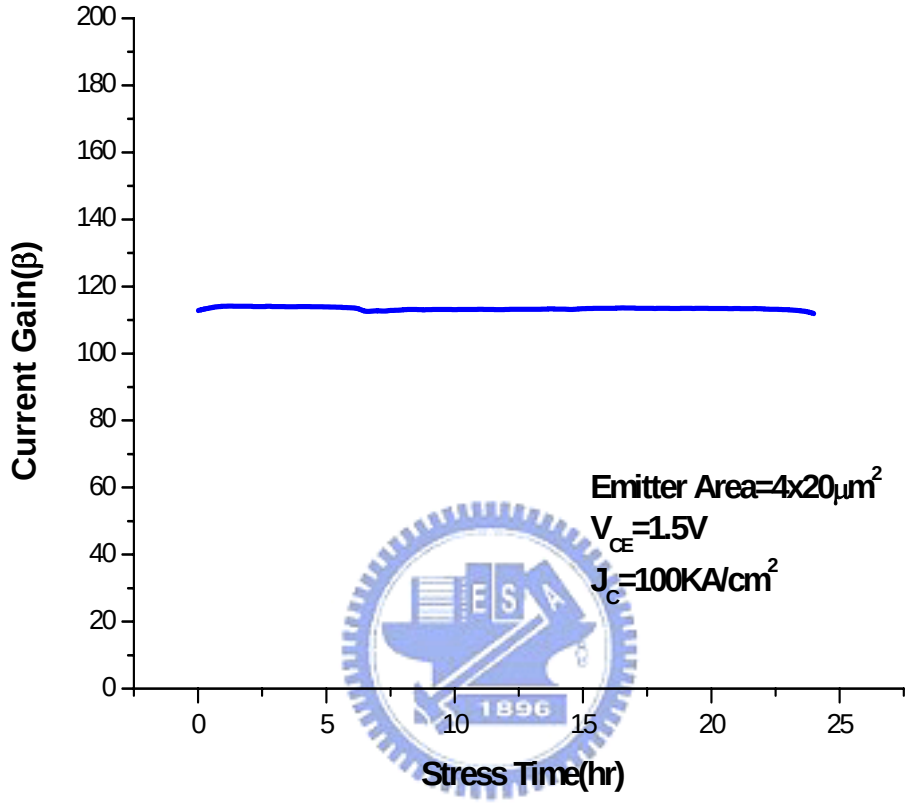
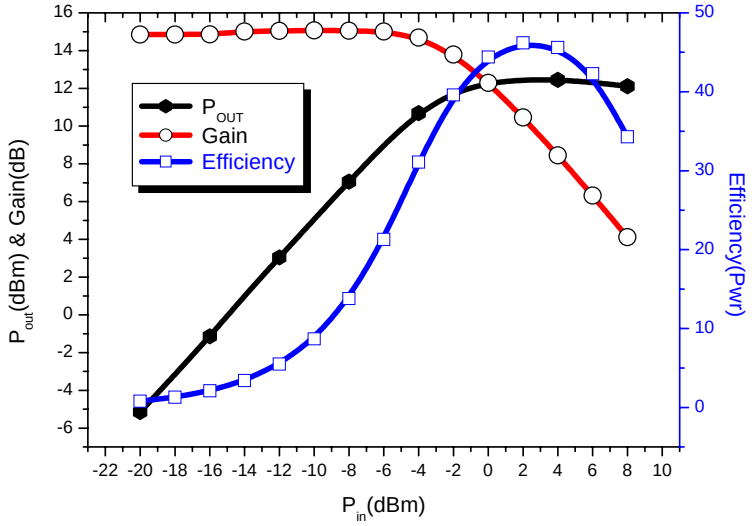
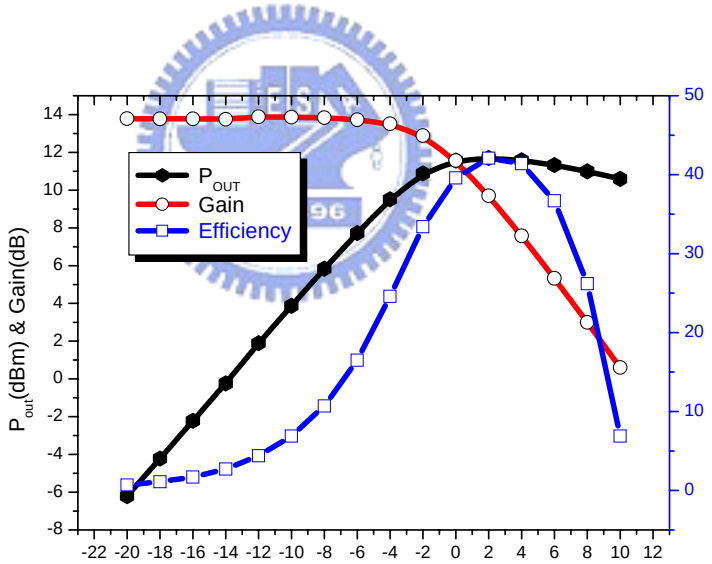


Fig34. The current gain (β) as a function of stress time at constant I_B for the 4x20- μ m^2-emitter-area fully Cu-metallized HBT with Pd/Ge/Cu ohmic contact.



(a)



(b)

Fig35. Measured output power as a function of input power for the 4 μm × 20 μm HBT at 2 GHz with bias V_{CE}=2.4V, I_C=7mA. The device was tuned for maximum power added efficiency. (a)Au-metallized (b)Cu-metallized HBTs.

Chapter 5
Conclusions

The fully Cu-metallized InGaP/GaAs HBTs using Pd/Ge/Cu ohmic contact to n-type InGaAs has been successfully fabricated and demonstrated. The optimized Pd (150 Å)/Ge (1500 Å)/Cu (1500 Å) metal structure forms a low contact resistivity ohmic contact to n-type InGaAs at a low annealing temperature. Low ohmic contact resistivity can be obtained when the Pd/Ge/Cu ohmic samples were annealed at 200°C ~ 330°C for 20min. The lowest specific contact resistivity achieved was 1.0×10^{-6} Ω-cm^2 when annealed at 250 °C for 20 min.

From XRD, Auger, AFM, TEM, and EDX studies, the low contact resistivity was due to the formation of the Cu_3Ge compound and the Pd_xGaAs compound in conjunction with the outdiffusion of Ga into the ohmic metal and the diffusion of Ge into the Ga vacancies. The contact resistivity of Pd/Ge/Cu ohmic contact was also very stable after annealing at 250°C for 24 hours. Overall, the Pd/Ge/Cu ohmic contact has a low contact resistivity, good thermal stability, and good surface morphology.

The common emitter I-V curves, Gummel plot, and power characteristic of these Cu-metallized HBT using Pd/Ge/Cu ohmic contact on InGaAs cap layer showed similar electrical characteristics as those conventional Au-metallized HBT. The common emitter current gain for the 4x20-μm^2-emitter-area fully Cu-metallized HBT using Pd/Ge/Cu ohmic contact and the traditional

Au-metallized HBT were both around 110. Current accelerated stress (100 kA/cm2 for 24 hrs) for the fully Cu metallized HBTs show almost no degradation.

The overall results show that the novel Pd/Ge/Cu ohmic contact can be used on the InGaP/GaAs HBTs with good electrical performance to achieve a Fully Cu-metallized device.

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