國立交通大學

材料科學與工程學系

博士論文

磁阻式元件之磁阻抗及氧化鎢電阻式記憶體的研究

Study of Magneto Impedance for Magneto Resistive Memory and Tungsten Oxide for Resistive Memory

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摘要

本論文主要研究磁阻式元件之磁阻抗行為及氧化鎢記憶體特性，以求對於電阻式記憶體的物理特性能有更深入地了解。

磁阻式元件是磁性隨機存取記憶體中扮演相當重要的角色，其中包含類自旋閥元件及穿隧式磁阻元件。磁阻式元件的直流電性行為已經被廣泛的研究，然而關於交流電性的行為則是很少被研究。因此在本篇論文的前半部分我們主要探討磁阻式元件的交流特性。

我們提供了一個藉由類自旋閥的交流特性，來對奈米氧化層在類自旋閥的貢獻做非破壞性的分析。此外我們以等效電路模型來解釋穿隧式磁阻元件的交流特性，並且在穿隧式磁阻元件 Ru (5nm) /Cu (10nm) /Ru(5nm) /IrMn(10nm) /CoFeB(4nm) /Al(1.2nm)-oxide /CoFeB (4nm) /Ru (5nm) 發現在很高的交流頻率 17.7 百萬赫茲，此元件的虛部磁阻抗，有非常劇烈的變化可達 17000%，這個發現使的磁穿隧元件有潛力應用於高頻的感應式元件。

本論文的後半部分，研究有關於氧化鎢電阻式隨機存取記憶體。由於電阻式隨機存取記憶體，具有極佳的微縮能力及具備做成三維元件的可能性，所以一直被看好能取代電子式儲存的記憶體；然而其基礎理論並不完備，且元件的表現還有待更進步。因此我

們提出了一個具新穎性的氧化鎢電阻式隨機存取記憶體，其製作方式只需在現有半導體製程多一道曝光程序，並且完全符合CMOS製程。我們以快速氧化技術所製備的氧化鎢電阻式隨機存取記憶體，可表現出極佳的元件特性，例如低電流操作、極短時間操作、好的記憶維持能力及可達百萬次的操作次數。

對於氧化鎢電阻式隨機存取記憶體，我們進一步發現頂部電極的功函數大小可以改變傳導機制，在低功函數頂部電極其電流傳導機制符合空間電荷限制電流的理論，而在高功函數頂部電極其電流傳導機制符合熱離子發射理論。此研究提供了藉著改變頂部電極，有機會改善元件的特性表現。所以根據這個發現，我們設著去研究利用鎳當頂部電極的氧化鎢電阻式隨機存取記憶體。此新元件表現出非常好的特性，如低於200微安培的操作電流、大於100倍的阻值變化及在攝氏85度的環境下，大於300年的記憶維持能力。

Study of Magneto Impedance for Magneto Resistive Memory and Tungsten Oxide for Resistive Memory

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ABSTRACT

This dissertation is devoted to study the magneto impedance effect of magneto resistive elements, and tungsten oxide resistive memory extensively for providing in-depth their physical understanding.

The magneto resistive elements such as pseudo spin valve (PSV) and magneto tunneling junction (MTJ) play a role for magneto random access memory (MRAM). The DC behaviors for magneto resistive elements have been widely studied, but the AC behaviors are still rare. Thus, in the first half of this dissertation we focus on the AC behaviors of magneto resistive elements.

By using AC characteristics, we provide a new non-destructive analysis method to study the nano-oxide layer effects of PSV. Besides, the equivalent circuit model is used to describe the AC behaviors for MTJ. For Ru (5nm) /Cu (10nm) /Ru(5nm) /IrMn(10nm) /CoFeB(4nm) /Al(1.2nm)-oxide /CoFeB (4nm) /Ru (5nm) system, a huge imaginary part of magneto impedance ratio more than 17000% is observed at high frequency 17.7MHz. Magneto impedance effect of the MTJ is potentially a sensitive sensor for high frequencies.

In the second half of this dissertation, tungsten oxide resistive random access memory is studied extensively. Although resistive random access memory (RRAM) is forecasted to be the promising solutions to replace the electron storage memory due to its excellent scalability and 3D possibility, up to now, the fundamental understanding is still very limited and device performance is required to improve. Thus, we proposed a novel WO_X for the RRAM system, because it requires only one extra mask under standard CMOS process. By using rapid thermal oxidation (RTO) for the WO_X RRAM, we have demonstrated its good performance such as low switching current, fast programming speed, good thermal stability, and high endurance > 1M times for nonvolatile memory.

Under this study, we further find the work function (WF) of the electrode is a key element determining the conduction mechanism for WO_X RRAM. SCLC (space charge limit current) mechanism and thermionic emission mechanism are identified for low WF and high WF electrodes, respectively. These studies imply that the device performance may be significantly improved by selecting the proper electrode. With this guideline, $Ni/WO_X/W$ device is investigated. The new $Ni/WO_X/W$ device shows very good performance that operates at <200uA switching current, a 100X resistance ratio window, and extremely good data retention of > 300 years at 85 ^{o}C.

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在交大三年多求學的日子，我得到很多人的幫忙及支持，使的我在攻讀博士的生涯能克服層層的阻礙，並且對於未來的挑戰更有信心去面對。所以這本論文是代表著我對您們獻上我由衷的感謝，及對我們一起走過不可抹滅的足跡。

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CHAPTER 1

Introduction

1.1 Background and Motivation

Non-volatile memories have drawn much attention in the world. The applications for portable and electronics such as digital still camera (DSC), cellular phone, digital audio machines (MP3 player), memory cards, routers, and so on are indispensable in our life. At the present the electron storage memories like conventional floating gate flash memories, NOR and NAND flash, are popular for non-volatile memory that drive the progress of the world around forty years. Recently, in order to keep corresponding to the market of non-volatile semiconductor memories, owing to its high density and low cost, both for NOR and NAND flash are the most important electronic devices. Up to now, flash memories could scale down to 32nm technology node. However, beyond 32nm technology node, the flash memories face the scaling issues due to physical limitation. Therefore, finding the way to replace the electronic storage memory is a hot and interesting topic for memory research.

Resistive storage memory plays a key role for memory research due to its potential to replace the electronic storage memory. For the purposes of Phase change memory (PCM), magnetic random access memory (MRAM), and resistive random access memory (RRAM) are considered in place of the electronic storage memory because good performance such as high endurance, random access and high operation speed.

MRAM has been developed more than twenty years. This technology always can find new ways to overcome the hinder of technology issues. For instance, the spin transfer torque technique was used to solve the scaling issue for conventional field driven MRAM. Although the operation architecture changes a lot for MRAM evolution, the basic magneto resistive elements are used and dominate the performance of either conventional MRAM or STT

MRAM.

The DC behaviors for magneto resistive elements such as pseudo spin valve (PSV), and magneto tunneling junction (MTJ) have been widely studied, but the AC behaviors are rare. This motivates us to investigate the AC behaviors for PSV and MTJ. In this thesis, the magneto impedance behaviors of the PSV and MTJ are studied. By using the AC analysis, the nano-oxide layer (NOL) effects of PSV could be modeled. Moreover, the equivalent circuit model was used to describe the AC behaviors for the MTJ.

Recently, resistance-based memory has attracted much attention for high-density memory applications because of its simple structure, small cell size, high speed, and low power consumption. Resistance switching memories including transition metal oxides (TMO) and programmable metallization cell (PMC), such as TiO_X [72], NiO_X [67], MoO_X [73], CuO_X, TaO_X, CoO_X [74], and Cu/WO_X [75] have been studied extensively. Although a lot of groups devote to study the RRAM for its conducting mechanism, switching mechanism, and device performance, up to now, their switching and conducting mechanisms are still not clear due to the complexity of the many oxides.

Compatibility with the CMOS process is a major criterion in choosing the metal oxide for RRAM design. Tungsten oxide (WO_X)-based RRAM is attractive because it requires only one extra mask without contamination issue, new equipment or new material to the standard CMOS process. The device performances of WO_X-based RRAM are further studied. The WO_X converting by rapid thermal oxidation (RTO) provides the suitable performance such as low switching current, high resistance window, fast programming speed, good thermal stability, and high endurance for nonvolatile memory. Besides the conducting mechanism is also investigated by using different work function electrodes connecting with WO_X elements.

1.2 Thesis Organization

This thesis consists seven chapters.

At first, chapter 1 gives a brief introduction and organization for this dissertation. Chapter 2 reviews the previous literatures of emerging resistive memories such as PCM, MRAM, and RRAM.

In chapter 3, the magneto impedance behavior of the PSV is addressed. The NOL effect of the PSV is studied. The new non-destructive analysis method via the magneto impedance spectroscopy for investigate the PSV with different thickness of NOL is provided. Also, the magneto impedance behavior study for MTJ is shown in chapter 4. The equivalent circuit model can well describe the AC phenomenon of the MTJ.

In chapter 5 and 6, the main discussion shifts to RRAM research. The tungsten oxide RRAM by using down stream plasma oxidation (DSPO) is proposed in chapter 5. The device analysis and performance are introduced. Chapter 6 shows the further improved WO_X device by using rapid thermal oxidation (RTO) process. The first time transient effect study for WO_X device is demonstrated, and it reveals ultra fast program speed for RTO WO_X RRAM. Moreover the performance, operation method, and conduction mechanism are explained in detail.

Finally, the summary and future prospects will be given in chapter 7, respectively.

CHAPTER 2

Basic of MRAM and RRAM

2.1 Magnetoresistive Random Access Memory (MRAM)

2.1.1 Magnetoresistance Effect

In this section, we will discussion the magnetoresistance, include pseudo spin valve effect and tunneling magnetoresistance effect.

The pseudo spin valve is composed of a hard magnetic layer, HM, and a soft magnetic layer, SM, magnetically separated with a nonmagnetic layer, NM. The HM has a larger coercivity than the SM. A prototype pseudo spin valve film proposed by Shinjo et al. is $[NiFe(3)/Cu(5)/Co(3)/Cu(5)]^{15}$ multilayered film [1]. NiFe is used for the SM and Co is used for the HM. This multilayered film showed a MR ratio of ~8%. The magnetocrystalline anisotropy energy, E_a, for the films having cubic symmetry is given as

$$E_a=K_1/8(1-\cos 4\theta)+\ldots$$

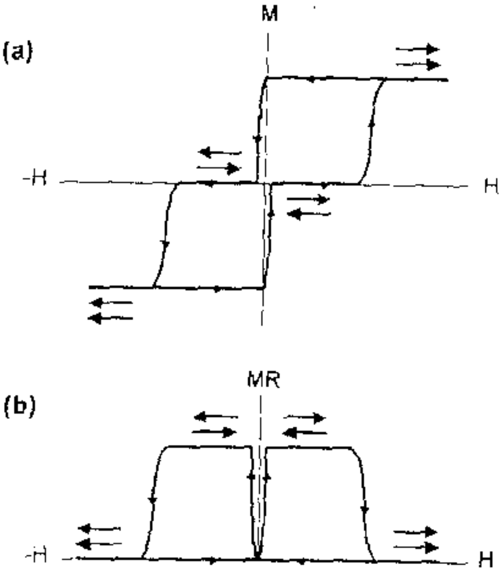

Fig. 2.1. (a) Magnetization curve and (b) MR curve of the pseudo-spin-valve, where the magnetization directions of the SM and the HM are denoted with gray and black arrows, respectively.

When the magnetization rotates in the (100) plane, where θ is the angle between the magnetization direction and the [010] axis. The K_1 is the negative for fcc NiFe and Co. Therefore, the NiFe and Co layers have the easy axis along the [011] direction. This is the reason why the magnetization reversal of the NiFe and Co layers take place. These characteristics are suitable for the application of pseudo-spin-valve to MRAM devices, as the magnetization reversal of the HM(=Co) layers is used for the data writing and that of SM(=NiFe) layers is used for data reading, The switching field of SM is lower than that of the HM layers. The schematic magnetization curve and the MR curve of the pseudo-spin-valve are shown in Fig. 2.1(a) and (b). With the application of a small magnetic field that causes magnetization reversal of the SM, but not of the HM, the magnetization directions of the SM and the HM take an antiparallel configuration. Then, the pseudo-spin-valve shows high resistance. With the application of a large magnetic field that causes magnetization reversal of the HM, the magnetization directions of the SM and HM take a parallel configuration and the pseudo-spin-valve shows low resistance. Pseudo-spin-valve shows a symmetric MR curve with the magnetic field direction, while the exchange-biased spin valves show a nonsymmetric one as shown in Fig. 2.2, as the HM in the pseudo-spin-valve has uniaxial anisotropy, while the pinned magnetic layer (PL)/ antiferromagnetic (AF) in the exchange-bias spin valve has unidirectional anisotropy.

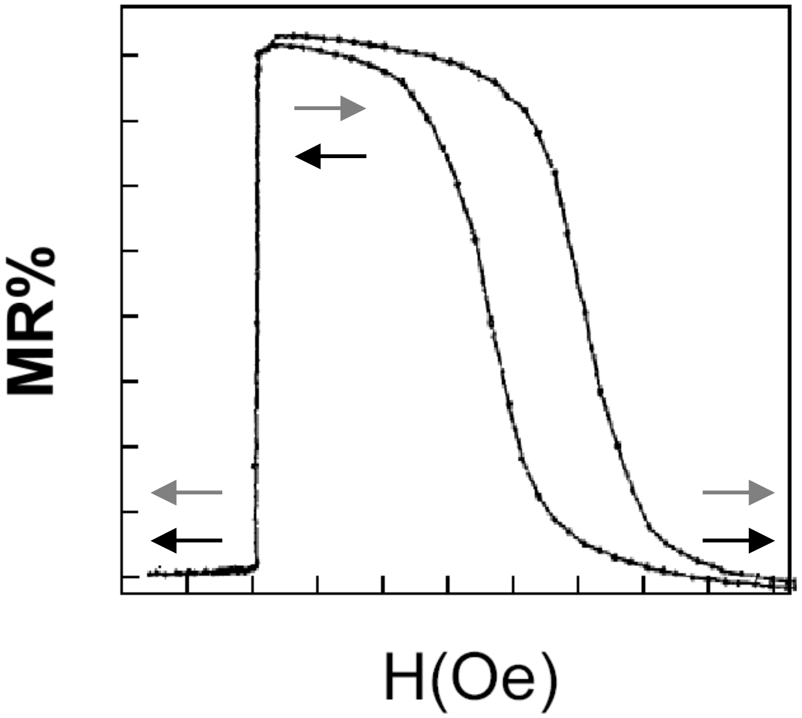

Fig. 2.2. MR curve for the single spin valve, where the magnetization directions of the FM and the PL are denoted with gray and black arrows, respectively.

The exchange-biased spin valve shows a reversible MR curve with the magnetic field. But the pseudo-spin-valve shows an irreversible one. This is a disadvantage of pseudo-spin-valve for application to MR heads. However, pseudo-spin-valves are studied for application to MRAM (magnetic random access memory) devices [2,3].

Tunneling magnetoresistance (TMR) is observed for ferromagnetic spin tunneling junctions (MTJ) consisting of ferromagnetic-insulator- ferromagnetic layers [4-6]. When the insulating layer, usually referred to as the barrier layer, is very thin (the order of 1nm), electrons can tunnel through this forbidden region as a result of the wave-like nature of electrons for a voltage applied between the two electrodes, and can only be described in terms of quantum mechanics. The basic principle of TMR is the dependence of the tunneling probability on the relative orientation of magnetization in the two ferromagnetic electrodes. The tunneling conductance is spin dependent due to the spin dependent density of states (DOS) at the Fermi level for ferromagnets. When the applied voltage is small enough for electrons near the Fermi level to tunnel, the tunneling conductance G in the MTJ can be written as (2.1.1)-(2.1.2) by neglecting the spin dependency of the tunneling probability [7],

$$G = R^{-1} = \sum_{\sigma} |T|^2 D_{1\sigma}(E_F) D_{2\sigma}(E_F) \tag{2.1.1}$$

$$|T|^2 \exp(-2s\chi) \tag{2.1.2}$$

$$\chi = \left[8\pi^2 m \times (\varphi - E_F)/h^2\right] \tag{2.1.3}$$

where R, T, $D_{i\sigma}(E_F)$ are the junction resistance, tunneling probability, DOS at the Fermi level for spin σ band of the i-th ferromagnet, respectively, andφ,s, $\chi$and h are the barrier height and thickness, electron wave vector in the barrier and the Planck constant, respectively. The TMR is defined as

$$TMR = (R_{AP} - R_P)/R_P \tag{2.1.4}$$

where R_P and R_{AP} are the resistance for parallel and antiparallel spin configurations of two ferromagnetic electrodes, respectively. If we assume that spin is conserved during tunneling as shown Fig. 2.3, (2.1.1)-(2.1.4) lead to Julliere's model [4],

$$TMR = 2P_1P_2/(1 - P_1P_2) \tag{2.1.5}$$

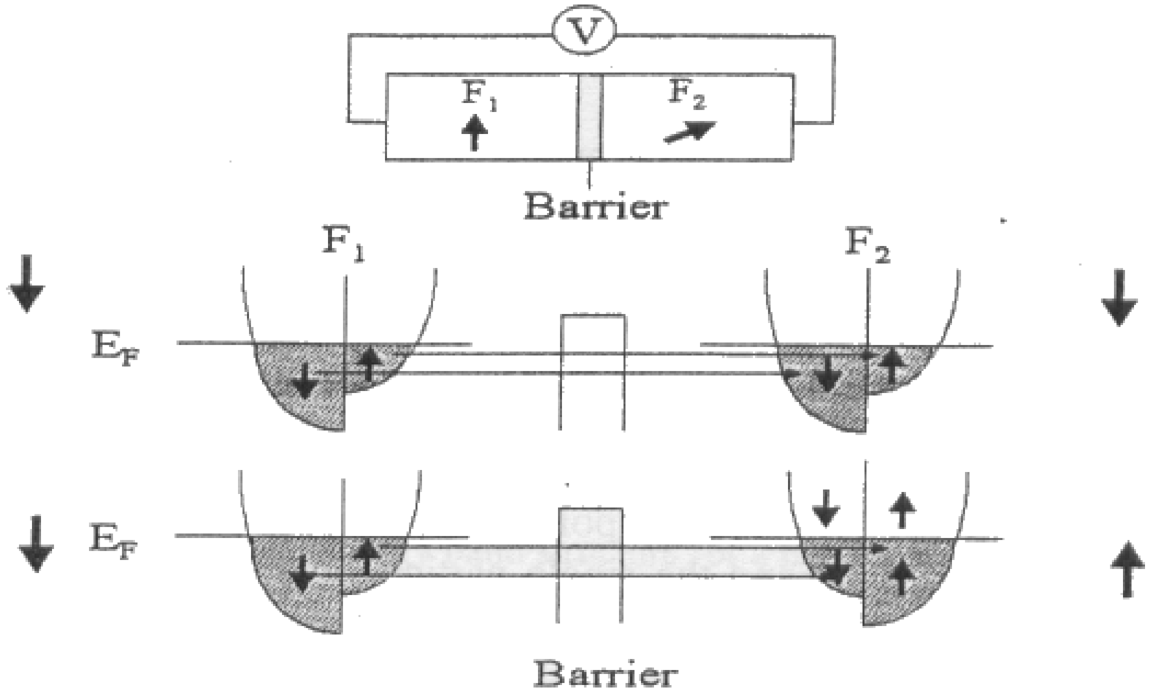

Fig. 2.3. A schematic model for spin dependent tunneling

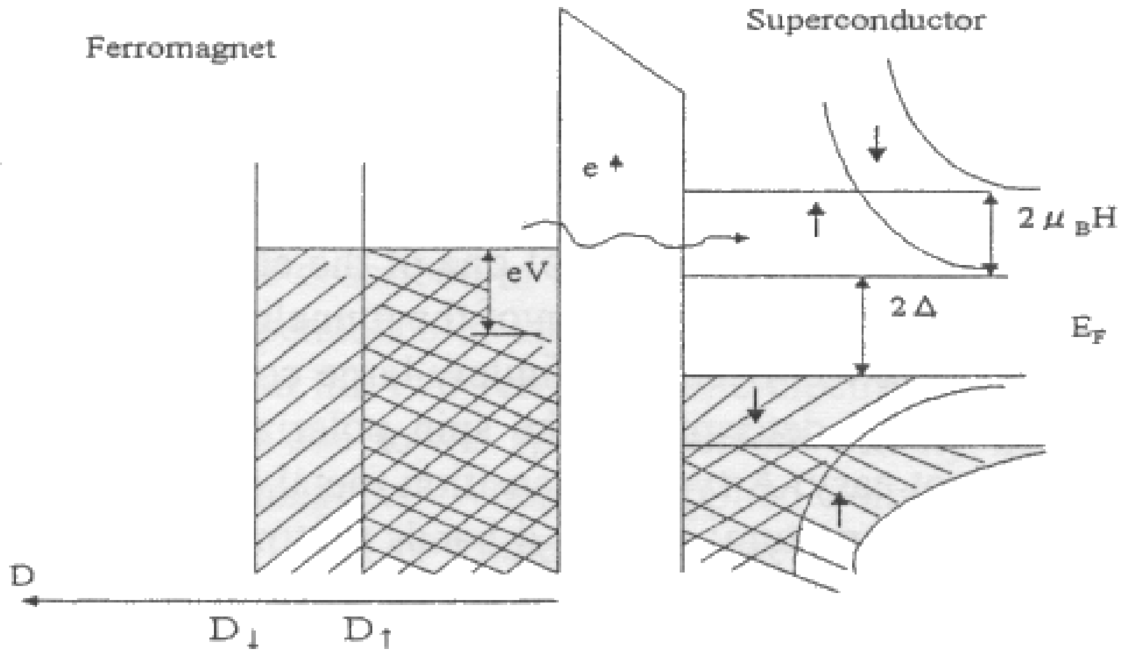

Fig. 2.4. Probing the spin polarization of tunneling electrons from the ferromagnet to the superconductor

Pi is the spin polarization of tunneling electrons of ferromagnet i and given by

$$P_i = \left(D_{i\uparrow} - D_{i\downarrow}\right)/\left(D_{i\uparrow} + D_{i\downarrow}\right) \qquad (2.1.6)$$

TMR can vary over a wide range depending on the P values of ferromagnets as verified by (2.1.5) and (2.1.6). For vanishing polarization of one of the electrodes the magnetoresistance disappears, while for full polarization of the tunneling electrons of both electrodes (P_1=P_2=1) the effect will become infinitely large corresponding to a value of 1 in (2.1.5). Unfortunately, determining the spin polarization at the Fermi energy of a ferromagnet is not easy. A typical transition metal ferromagnet has two components to its electronic structure; narrow d-bands that may be fully or partially spin polarized and broad s-bands with a lesser degree of spin polarization due to hybridization with the d-bonds. The value of P is controlled by extending to which these s- and d-bonds cross the Fermi energy. If the orbital character at the Fermi surface of the ferromagnetic metal is primarily d-like, then the spin polarization will be high. If the orbital character, however, is s-like or s-d hybridized, then the spin polarization can be low or high depending on the detail of the electronic structure. The magnetization of a material may show that all the electronic spins associated with the d orbits are aligned but the spin polarization at E_F can de depressed. On the other hand, metallic oxide ferromagnets, for example, have a greater opportunity for high spin polarization because of the predominance of the d orbital character at E_F.

Measuring the spin polarization requires a spectroscopic technique that can discriminate between the spin-up and spin-down electrons near E_F spin polarized photoemission spectroscopy is technically capable of providing the most direct measurement of P, but lacks the necessary energy resolution (~1meV). An effective alternative to photoemission is the use of spin polarized tunneling in a planar junction geometry which does allow the electronic spectrum near E_F to be probe with sub-meV energy resolution.

Tedrow and Meservey pioneered this technique by marking superconductor/insulator/ferromagnet junctions and Zeeman splitting the superconductor’s strongly peaked single-particle excitation spectrum by the application of a magnetic field [8]. The spin-splitting of the quasiparticle density of states in a superconductor by the application of a magnetic field allows probing the spin polarization of tunneling electrons from the ferromagnet, which is schematically shown in Fig. 2.4. The resulting spectrum of the superconductor roughly corresponds to two fully spin polarized peaks (neglecting spin-orbit coupling effects) that can be used to detect the spin polarization of a current from the ferromagnetic film. Another method of measuring spin polarization of a metal was developed recently [9], which is a metallic point contact between the point contact measures the conversion between superconducting pairs and the single particle charge carriers of the metal. The conversion of normal current to supercurrent at a metallic interface is called Andreev reflection.

The values of P measured are shown in Table 2.1.1 for various ferromagnets except for the theoretically expected values for half metals with P=1, which have an energy gap in the minority spin (down spin) band as shown schematically in Fig. 2.5, thus only majority spin (up spin) electrons at the Fermi level. The spin polarization of tunneling electrons seems to be nearly proportional to the magnetic moment μ of the electrode as shown for Ni-Fe alloys in Fig. 2.6 [8], while it is not always proportional to μ of the ferromagnetic electrode as shown in Fig. 2.7 [10], which exhibits TMR and μ^2 as a function of the composition of Fe-Co alloy electrodes used for the junctions.

Table 2.1.1 Spin polarization of various magnetic materials

Magnetic material	Spin polarization	Magnetic materials	Spin polarization
Fe	0.44	NiMnSb	1,0.58
Co	0.35	PtMnSb	1
Ni	0.23	CrO2	1
$Ni_{80}Fe_{20}$	0.25,0.45	Fe_3O_4	1
$Fe_{50}Co_{50}$	0.53	$(La\text{-}Sr)MnO_3$	1

Equation (2.1.5) assumes that all electrons at the Fermi level have the same probability of tunneling and also neglects the influence of the barrier. In fact, however, TMR depends on tunneling barrier height for the MTJ using CoFe electrodes. The TMR is larger for the higher barrier height. The barrier height can be estimated by Simmons' expressions (2.1.7)-(2.1.10)

$$J=\beta\left(V+V^{3}\right), \ldots\ldots (2.1.7)$$

$$\beta=\left[3e^{2}(2m\phi)^{1/2}/2h^{2}s\right]\exp\left(-A\phi^{1/2}\right)\left[\Omega^{-1}cm^{2}\right], \ldots\ldots (2.1.8)$$

$$\gamma=(Ae)^{2}/96\phi-Ae^{2}/32\phi^{1/4}, \ldots\ldots (2.1.9)$$

$$A=4\pi(2m)^{1/2}s/h=1.02\left[\overset{o}{A}/(eV)^{1/2}\right], \ldots\ldots (2.1.10)$$

for lower bias voltage, where J, ϕ and s are current density [A/cm^2], barrier height [eV] and barrier thickness [cm], respectively.

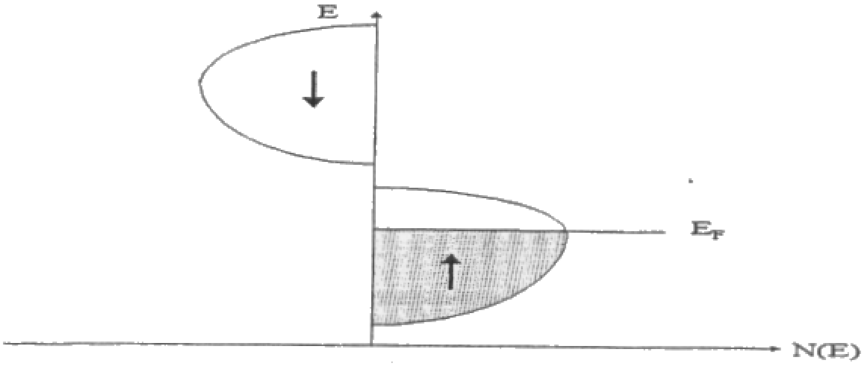

Fig. 2.5. Schematic energy band structure for a half metal

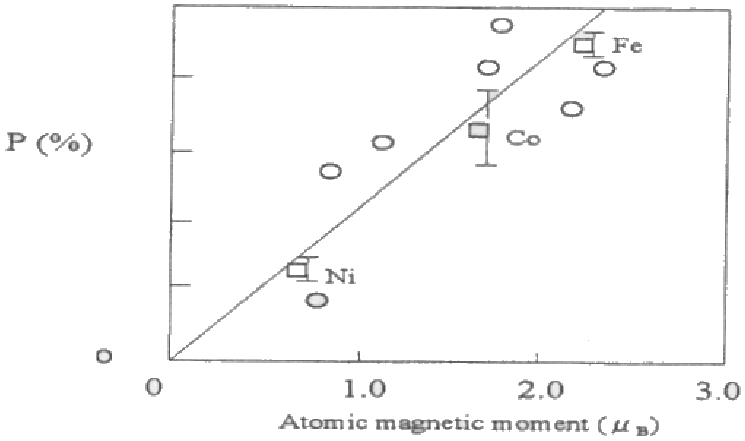

Fig. 2.6. Spin polarization of tunneling electrons versus the magnetic moment μ of the electrode.

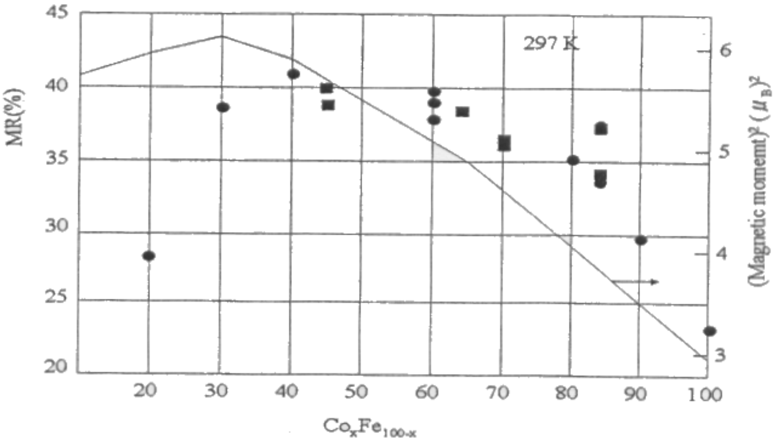

Fig. 2.7. TMR and μ^2 as function of the composition of Fe-Co alloy electrodes used for the junctions.

2.1.2 Magneto Impedance Theory

Magneto impedance, MI = $M|Z|e^{i\theta}$ = MR +iMX, in which X = X_L-X_C, originates mainly from the inductance and capacitance of the magneto device. Z is the impedance, θ is the phase angle, R is the real part of magneto impedance, and X is the imaginary part of magneto impedance.

In 1999, X.Q. Xiao [11] shows giant magnetoimpedance (GMI) effect in films with a sandwiched structure [12]. As compared to single layered films, the sandwiched films have much higher GMI ratio at relatively low frequencies. This is because of the separation of the ac current path from the magnetic flux path. The inner highly conductive metal reduces the entire resistance of the sandwiched film, and the outer magnetic layers form a magnetic alloy closed-loop structure. Therefore, less power is dissipated in the films to generate the ac transverse field. In the FeNiCrSiB/Cu/FeNiCrSiB structure, GMI ratios of 63% and 77% have been obtained at 13 MHz in longitudinal and transverse fields, respectively as shown in Fig. 2.8. These values are almost twice as large as those obtained in single layered FeNiCrSiB films.

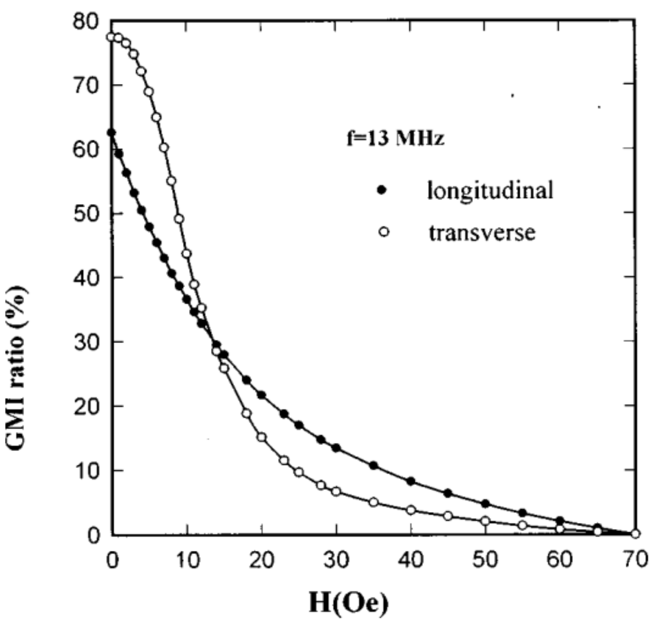

Fig. 2.8. Field dependence of △｜Z｜/｜Zs｜ at 13 MHz in longitudinal (filled symbols) and transverse (hollowed symbols) field.

In 2000, M.F. Gillies [13] further proposed the magneto impedance effect for magneto tunneling junctions [14]. The structure is the Si/SiO2/Co/AlOx /Co. Due to differing conductivities charge collects at the interface between the dielectrics as well as on the capacitor plates (Maxwell Wagner capacitor model). This results in two contributions to the impedance. In the case of the magnetic tunnel junctions studied, they extend this simple analysis to more than two layers in order to provide a model with which the complicated results of the impedance measurements as shown in Fig. 2.9 (a) and (b). By this AC analysis, the oxide/Co multilayer proved a very useful way of determining the total oxide thickness as a function of oxidation time and allowed a rough check of what was determined from the impedance measurements. The strength of the impedance measurements is that they provide a “fingerprint" of the oxide, rather than definitive fit parameters, and in so doing help to characterize the oxide.

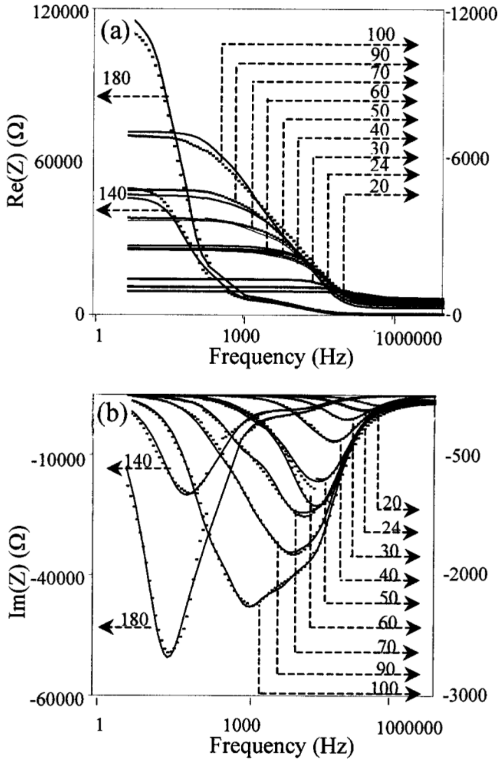

Fig. 2.9. (a) Real and (b) imaginary parts of impedance for junctions with different oxidation times (in seconds). In both figures the dots show the measured results and the solid lines are fits.

2.1.3 Field Driven Magnetization Switching Designs

In most of today's MRAM designs, the memory element is a magnetic tunnel junction (MTJ) that consists of two magnetic electrodes sandwiching an insulative tunnel barrier, as shown in Fig. 2.10 [15-18]. The resistance of these magnetic tunnel junctions depends on the relative orientation of the magnetic moments in the two magnetic electrodes interfacing with the tunnel barrier [19-22]. When the magnetic moments of the two magnetic layers are antiparallel, the resistance of the tunnel junction is significantly higher than when they are in parallel. The magnetic electrodes are shaped like an ellipse to create a shape-defined magnetic anisotropy. The magnetic moment will always be resting along the long axis of the element, referred to as the magnetic easy axis, as shown in Fig. 2.11 [23]. Assuming we can "fix" or "pin" the direction of the magnetic moment of the bottom layer, referred to as the reference layer, along the easy axis, the magnetic moment orientation of the storage layer along the easy axis will give rise to two states with distinctively different resistance values, thereby, the two states in binary bit. The magnetization of the reference layer is "fixed" via a multilayer structure, which includes an antiferromagnetic layer at the bottom. The reference layer is part of a trilayer known as synthetic antiferromagnet (SAF) that is free of stray field. A good example is CoFe/Ru/CoFe with Ru of thickness around 8A˚. The antiferromagnetic layer yields an interfacial exchange field that "pins" the magnetic moment of the bottom SAF layer (pinned layer).

In a memory element array, each memory element is connected to a transistor, which performs the read addressing for reading back the memory state of an individual cell. The memory state writing of an individual memory element in the array is performed by a x-y grid of conducting wires, referred to as word lines and digital lines, placed over and below the memory elements with a memory element located at each cross, as shown in Fig. 2.12.

A current flowing through a selected word line (running in the y-direction in the figure) generates a magnetic field along the easy axis H_x while a current flowing through a selected digital line (running in the x-direction) generates a field H_y in a direction transverse to the easy axis. A simple theoretical analysis shows that the field threshold for resulting in a magnetic switching is given by $H_x^{2/3}+H_y^{2/3}=H_k^{2/3}$ often referred to as the Stoner–Wohlfarth switching astroid, where H_k is the anisotropy field of the element [24]. According to the above equation, the switching field threshold is the lowest when both field components are equal in magnitude: The memory state of the element at the cross of the activated word line and digital line can be changed. Whereas the rest of the elements along the selected word or digital lines, known as the half-selected elements, shall not be affected since they only experience one of the two fields, provided each field component is below H_k.

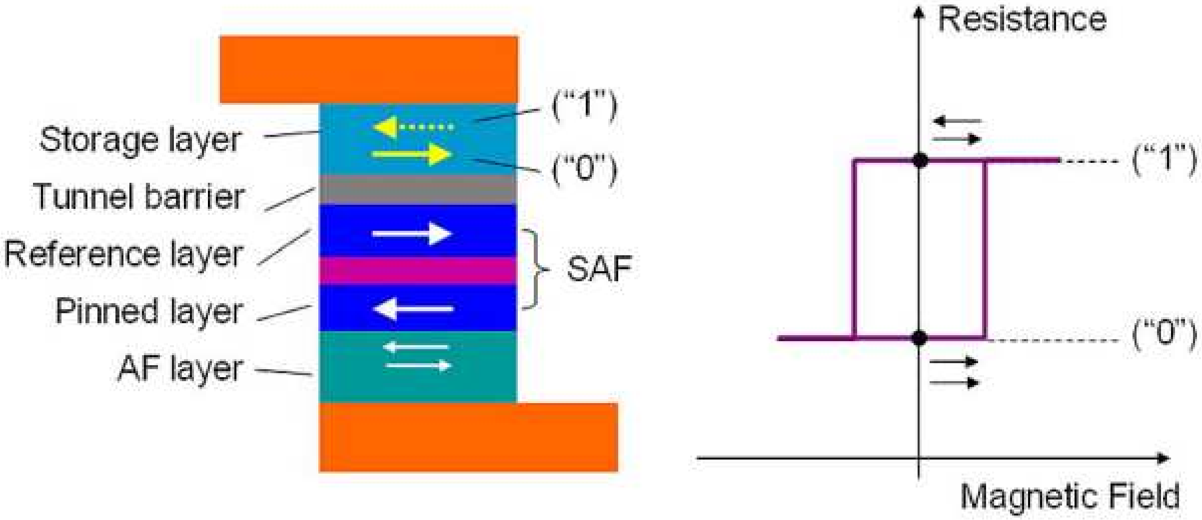

Fig. 2.10. Schematic drawing of a typical magnetic tunnel junction memory element and corresponding memory states that have two distinctive resistance values due to the magnetoresistive effect.

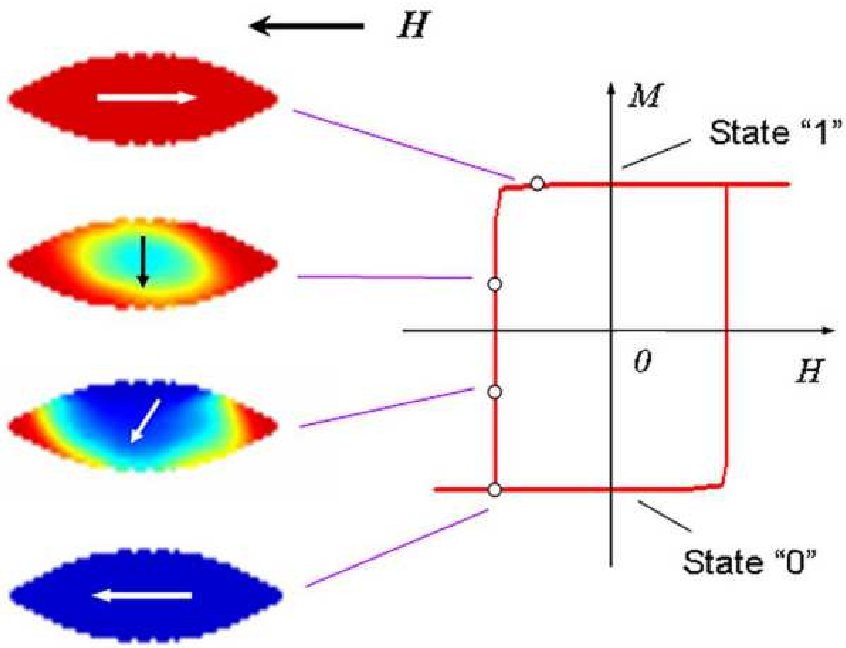

Fig. 2.11. Simulated magnetic switching of an eye-shaped magnetic element. The magnetization reversal starts at the center of the element with quasi-coherent magnetization rotation. The reversed region expands towards the ends as the reversal completes.

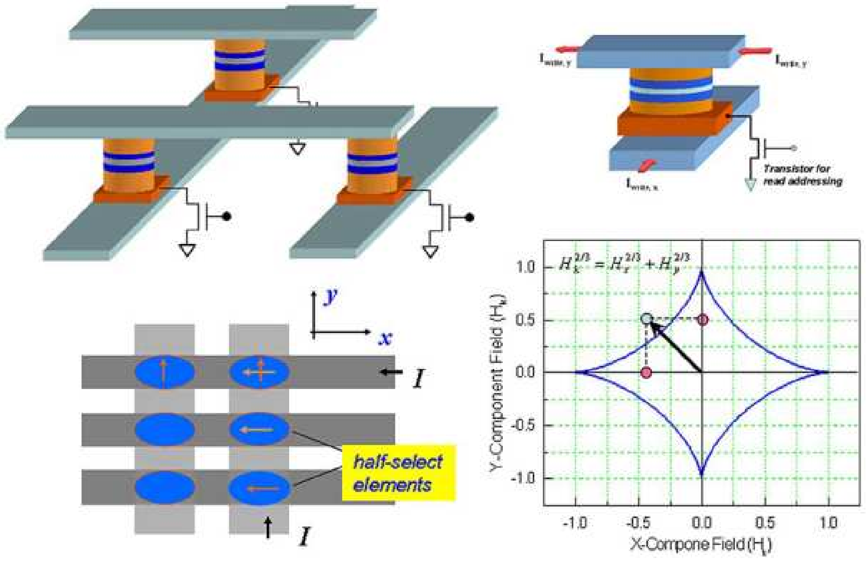

Fig. 2.12. Schematic drawing of the memory element array. Each memory element is connected to a field effect transistor for read addressing. A grid of x-y conducting wires, known as the digital lines (wires along the x-direction) and word lines (wires along the y-direction), is placed over and below the memory elements for providing the magnetic field for the write operation. Each memory element is located at a cross in the x-y wire grid. The lower bottom shows the switching field threshold contour, known as the Stoner–Wohlfarth switching astroid. The magnetization of the storage layer will remain unchanged if the field applied is located within the enclosed region of the astroid. Otherwise, the magnetic moment will irreversibly switch to the direction of the word line field.

2.1.4 Spin Torque Transfer Driven Switching Designs

Right before the turn of the century, researchers demonstrated magnetic switching of a patterned magnetic element at deep submicrometer dimension by direct perpendicular current injection [25-28], a phenomenon previously predicted by theorists Berger and Slonczewski, known as spin torque transfer [29,30]. When current is injected normally through a uniformly and firmly magnetized ferromagnetic layer, i.e., the reference layer, acts as a “spin filter”: the injected electrons with spin parallel to the magnetization direction of the ferromagnetic layer get transmitted and the electrons with antiparallel spins get, partially, reflected. The current becomes spin polarized in the vicinity of the reference layer. If another magnetic layer, i.e., the free layer, is placed within the range of the spin polarization, the spin polarized current would result in a torque, referred to as spin torque that is, to rotate the local magnetic moment away from the equilibrium orientation direction causing the magnetic moment to precess around the local effective magnetic field. This spin torque will be present until the local magnetization becomes parallel to the spin polarization direction. The current spin polarization is opposite in sign at the opposite side of the reference layer with respect to the direction of injection. Reversing current direction, thus, reverses the sign of the spin torque, as illustrated in Fig.2.13. If the spin torque, proportional to the injected current density, in the free layer exceeds the restrain torque caused by local magnetic anisotropy, magnetization rotation occurs. The critical current density to irreversibly reverse the magnetic moment of the free layer is given by the following [20]:

$$J_{C0} = \left(\frac{\alpha}{\eta}\right)\left(\frac{2e}{\hbar}\right)(M_S t_F)(H_k + 2\pi M_S)$$

where M_S, t_F, and H_k are the saturation magnetization, the thickness, and the anisotropy field of the free layer, respectively. Also in the above equation, α, known as the Gilbert damping constant, is a phenomenological parameter measuring the magnitude of the damping torque that yields a natural dissipation of the magnetic energy into other nonmagnetic energy form(s), such as heat. The most commonly recognized energy dissipation channel is the coupling between spin waves and lattice vibration, known as magnon–phonon interaction. With a slight manipulation, above equation can be rewritten as

$$I_{C0} = \left(\frac{2e}{\hbar}\right)\left(\frac{2\alpha}{\eta}\right)\left(K_u V + \pi M_S^2 V\right)$$

where A, V, and K_u are the surface area, the volume, and the anisotropy energy constant of a free layer, respectively, and I_{C0} is the critical current amplitude. The term K_uV on the right-hand side is the anisotropy energy of the free layer, namely, the magnetic energy stored in the memory element or the energy barrier between the two memory states. It is important to note that the volume V in the above equation should be the activation volume, which could be smaller than the actual volume of a memory element. The term arises from the surface demagnetizing energy due to the out-of-plane precession of the magnetization during the switching. It is important to note that the surface demagnetizing energy is typically greater than the energy stored in the bit. The fact that the Gilbert damping constant appears in above equation reflects the nature of spin torque transfer driven magnetization reversal.

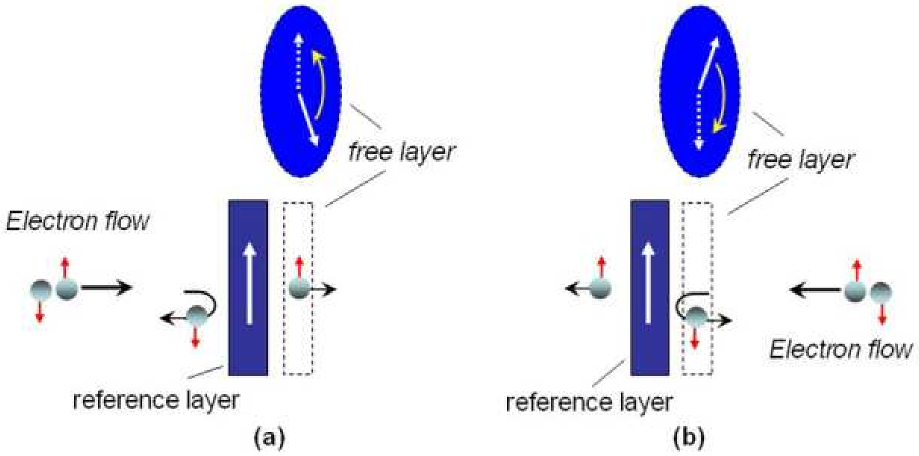

Fig. 2.13. Illustration of spin torque transfer. Injecting a current through a ferromagnetic layer of a ‘‘fixed’’ magnetization, the current will be spin polarized. Placing a free layer nearby, the spin polarized current will result in a torque that will act to rotate free-layer magnetization away from the equilibrium orientation. The sign of spin polarization direction outside of the ‘‘fix’’ layer reverses with reversing direction of current.

In a free layer at equilibrium absent spin torque transfer, the magnetization is always parallel to the local effective magnetic field, a direct result of the existed damping torque due to energy dissipation. When free-layer magnetization is in the opposite direction of the current spin polarization, the spin torque is effectively antidamping: its direction is exactly opposite to that of the damping torque. When the magnitude of spin torque becomes greater than that of the damping torque, the energy of the local magnetic moment increases with time and an irreversible magnetization reversal could eventually occur. A smaller damping torque will yield a smaller critical current for irreversible magnetization reversal. When the energy barrier between the two memory states becomes comparable to the thermal activation energy, k_T where k is the Boltzmann constant and T is the absolute temperature, memory state switching can occur at a current level below switching threshold, as illustrated in Fig.2.14. The probability per unit time for a transition between the memory states to occur is given as

$$p^{\pm} = f_0 e^{-\frac{E_b^{\pm}}{kT}}$$

where f_0 is known as the attempt frequency and its value is believed to be on the order of 10^9 to 10^{10} Hz. With an injected current pulse at a density and a pulse duration, the memory state switching probability is [31.32]

$$p(\Delta t) = 1 - \exp\left\{ -f_0 \Delta t \cdot \exp\left[-\frac{E_b}{kT} \left(1 - \frac{J}{J_{co}} \right) \right] \right\}$$

The above relationship is often used for quantitative determination of the energy barrier [32].

Fig. 2.15 shows a schematic view of a typical STT-MRAM memory cell along with a representative example of a magnetic memory element stack [33,34]. For switching the memory state of an element with 50nm/100nm for short/long axes, the injected current pulse is typically 200 μA in amplitude and 5 ns in duration, corresponding to a switching energy on the order of a few pJ. Compared to the toggle MRAM, whose switching energy per bit is on the order of 100 pJ, the energy consumption is substantially reduced. The STT-driven magnetization reversal offers a means to switch the magnetic state of the storage layer by directly injecting current through the memory element, hence eliminating the x-y grid of write lines and half-select problem discussion in previous sections.

In addition, the spin torque transfer is significantly more efficient in terms of switching free-layer magnetic moment for elements in deep submicrometer dimensions or below. Therefore, it could be the dream memory since it has the potential to replace all the existing memory devices in a computer, maybe even the hard disk drives, becoming the “universal memory”.

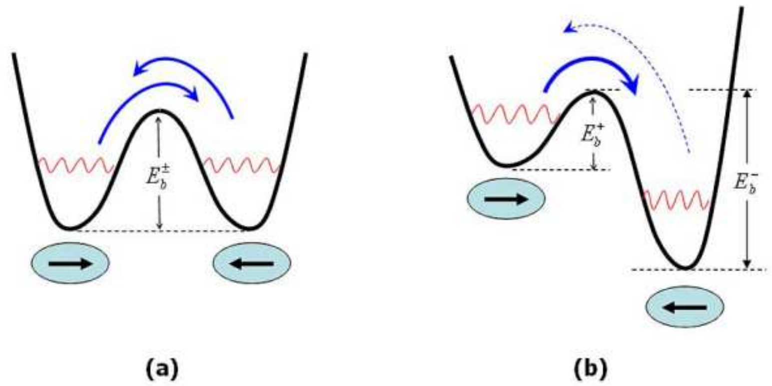

Fig. 2.14. Illustration of (a) thermally excited magnetization switching and (b) thermally assisted magnetization switching in which the energy barrier is lowered due to the presence of either a magnetic field or a spin torque transfer by injected spin polarized current.

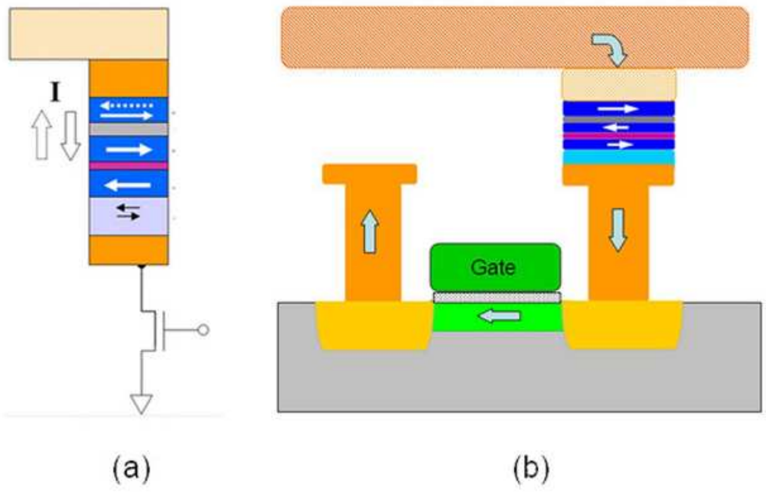

Fig. 2.15. Illustration of a spin torque transfer MRAM memory cell. (a) Schematic view and (b) illustration of the memory cell with addressing transistor on a Si wafer.

2.2 Resistive Random Access Memory (RRAM)

Starting in the 1960s, a huge variety of materials in an MIM configuration have been reported to show hysteretic resistance switching, with a first period of high research activity until the mid-1980s. A second, on-going period started in the late-1990s, triggered by Asamitsu et al. [35], Kozicki et al. [36] and Beck et al. [37], recently reviewed [38,39].

2.2.1 Unipolar and Bipolar Behaviors

In general, two switching schemes need to be distinguished. Switching is called unipolar (or: symmetric) when the switching procedure does not depend on the polarity of the voltage and current signal (Fig. 2.16a). In contrast, the characteristic is called bipolar (or: antisymmetric) when the set to an ON-state occurs at one voltage polarity and the reset to the OFF-state on reversed voltage polarity (Fig. 2.16b). In both characteristics, unipolar and bipolar, reading of the state is conducted at small voltages, which do not affect the state.

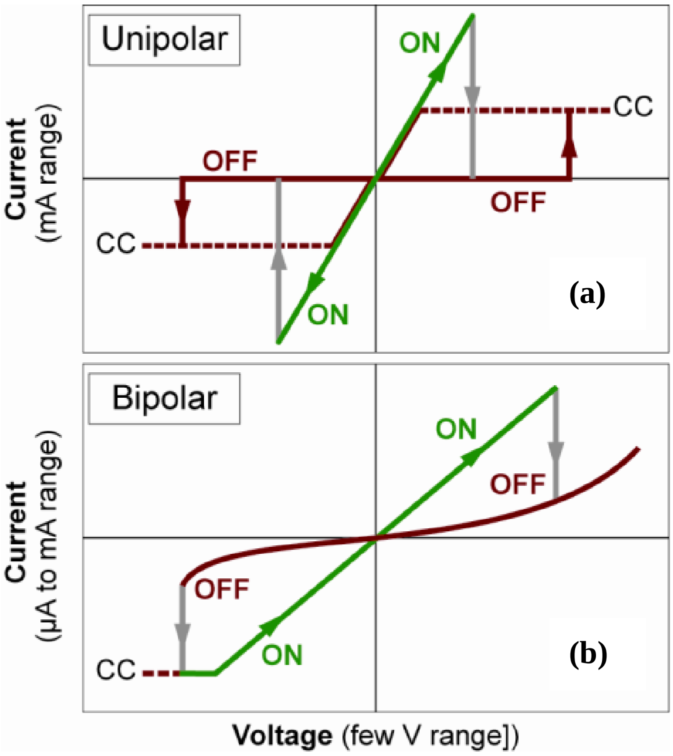

Fig. 2.16. Unipolar and bipolar switching schemes. CC denotes the compliance current, often needed to limit the ON current

2.2.2 Electrochemical Metallization Effect

One class within this category relies on an electrochemically active electrode metal such as Ag, the drift of the highly mobile Ag^+ cations in the ion conducting layer, their discharge at the (inert) counterelectrode leading to a growth of Ag dendrites which form a highly conductive filament in the ON state of the cell [40]. Upon reversal of polarity of the applied voltage, an electrochemical dissolution of the conductive bridges takes place, resetting the system into the OFF state (Fig. 2.17). The redox reactions for Ag_2S as an Ag ion conductor read as:

$$Ag^{+}(Ag_2S) + e' \underset{\text{Oxidation}}{\overset{\text{Reduction}}{\rightleftarrows}} Ag$$

The asymmetry of the OFF switching has been a matter of some debate, because it appeared to be unclear why the “opening” of the Ag bridge should occur at a different voltage polarity than the “closing”. Using a model system with an aqueous electrolyte we have recently been able to demonstrate that the asymmetry arises from the morphology, i. e. the needle-to-plane geometry of the configuration as shown by electrochemical simulations (Fig. 2.18) [41].

2.2.3 Valency Change Switching Effect

In many transition metal oxides, oxygen ions defects, typically oxygen vacancies, are much more mobile than cations. If the cathode blocks ion exchange reactions during an electroforming process, an oxygen deficient region starts to build and to expand towards the anode. Transition metal cations accommodate this deficiency by trapping electrons emitted from the cathode. In the case of TiO_2 or titanates, for example, this reduction reaction

$$ne' + Ti^{4+} \rightarrow Ti^{(4-n)+}$$

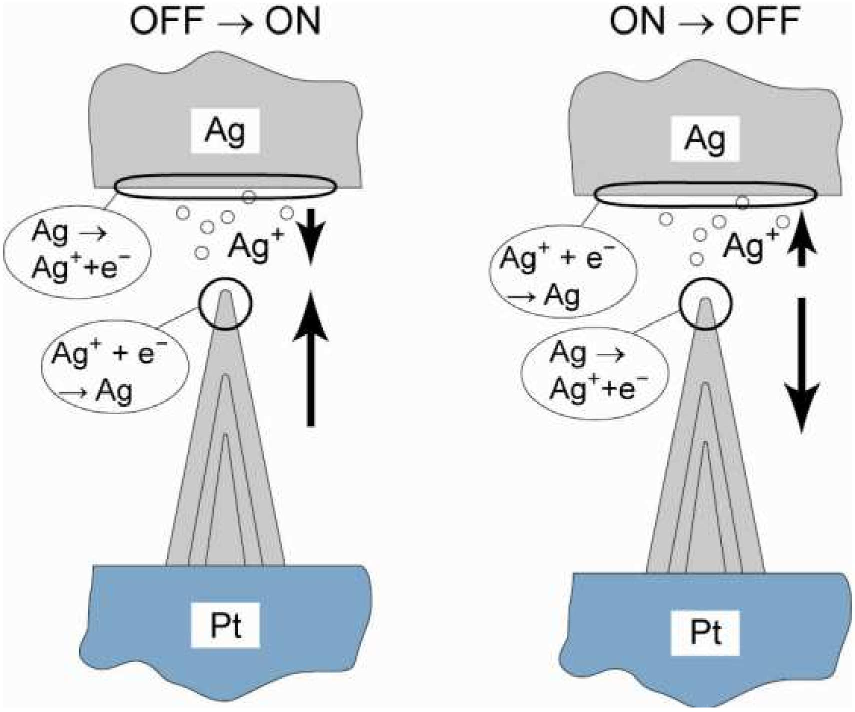

Fig. 2.17. Sketch of a resistive switching effect based on the electrochemical metallization process.

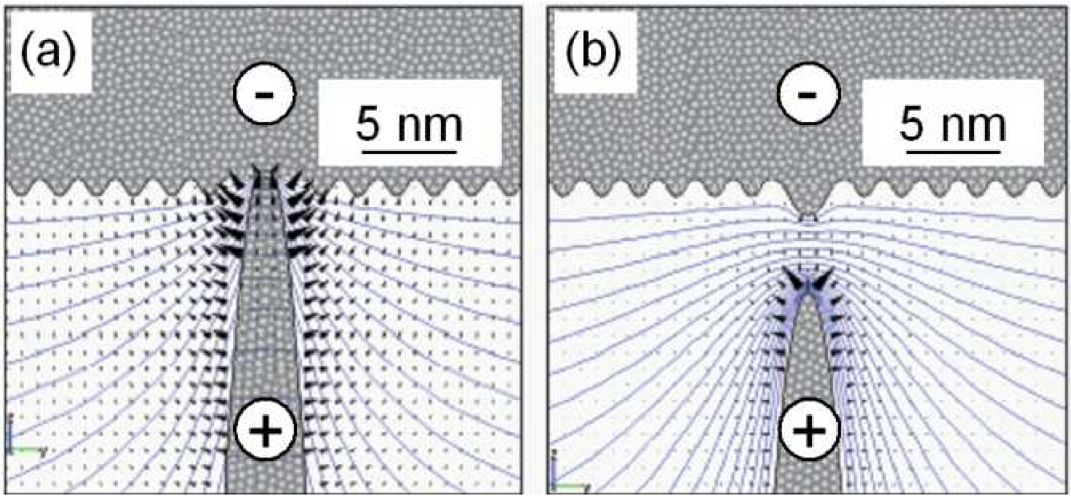

Fig. 2.18. Field simulation of the front-most Ag dendrite and the Ag electrode; (a) late ON state; (b) early OFF state.

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is equivalent to filling the Ti 3d band. The reduced valency states of the transition metal cations which are generated by this electrochemical process typically turn the oxide into a metallically conducting phase, such as, e. g., $TiO_{2-n/2}$ for approx. n>1.5. This “virtual cathode” moves towards the anode and will finally form a conductive path [42]. At the anode, the oxidation reaction may lead to the evolution of oxygen gas. As an alternative, material of or nearby the anode may be oxidized. Once the electroforming is completed, the bipolar switching obviously takes place through local redox reactions between the virtual cathode and the anode, i. e. by forming or breaking the conductive contact (Fig. 2.19).

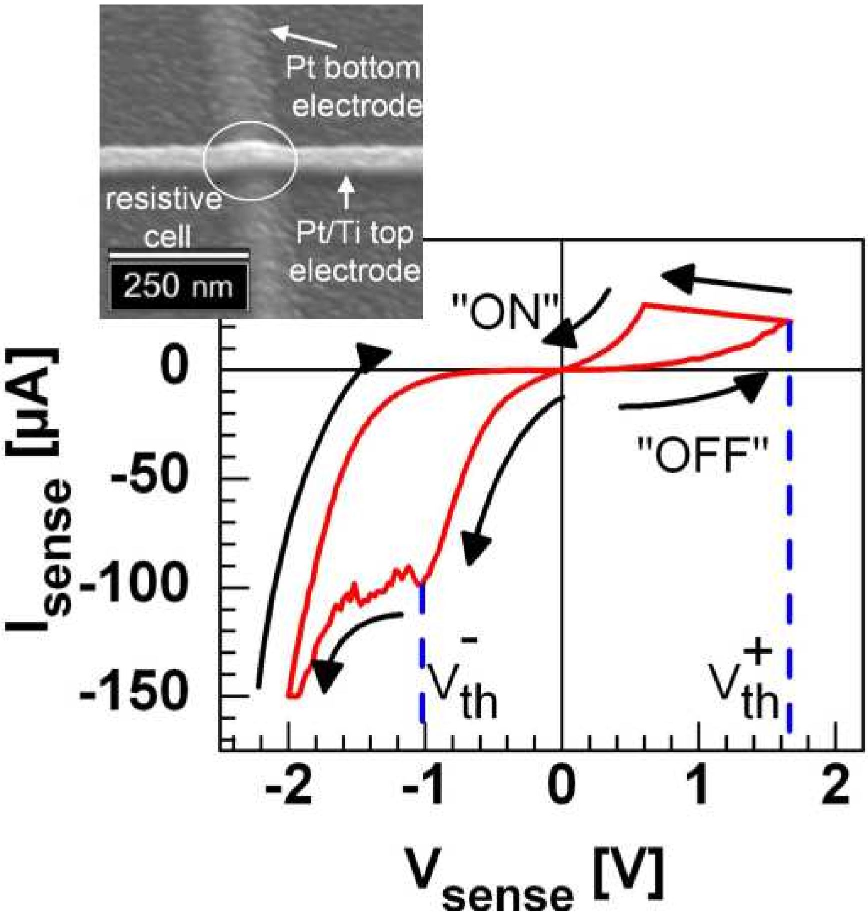

Fig. 2.19. I-V measurement of a 100 x 100 nm² Pt/TiO_2/Ti/Pt resistive switching cell. The SEM picture shows the single cell in cross junction configuration (C. Kügeler et al., unpublished data).

2.2.4 Thermochemical Effect

A typical resistive switching based on a thermal effect shows a unipolar characteristic. It is initiated by a voltage-induced partial dielectric breakdown in which the material in a discharge filament is significantly modified due to Joule heating. Due to the current compliance, only a weak conductive filament with a controlled resistance is formed. This filament may be composed of the electrode metal transported into the insulator, carbon from residual organics [43], or decomposed insulator material such as sub-oxides [44]. Recently, the filamentary nature of the conductive path in the ON-state has been confirmed. Pt/NiO/Pt thin film based cells have been successfully integrated into CMOS technology to demonstrate non-volatile memory operation [45]. A critical parameter for this unipolar switching effect seems to be the value of the current compliance. In passive arrays the storage cells need to incorporate diodes in series to the switchable resistors in order to avoid signal bypasses by cells in the ON-state. For oxide-baFsed unipolar cells, a sandwich concept has been proposed to integrate the diode function (Fig. 2.20) [46].

Resistive switching cells offer application opportunities, which go beyond mere high-density memory devices. In particular, they can be employed as reconfigurable switches in field-programmable gate-array (FPGA) type logic.

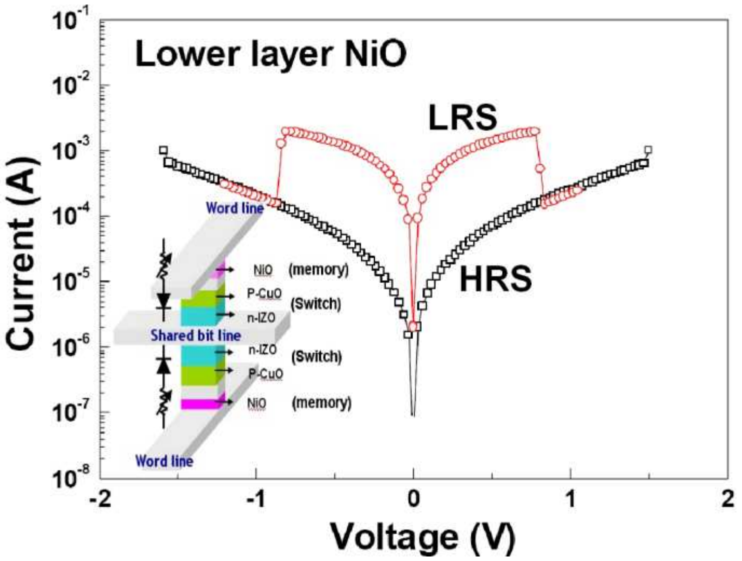

Fig. 2.20. 2-stack 1D-1R cross-point structure with oxide diodes as switch elements.

CHAPTER 3

Magneto Impedance Study for Pseudo Spin Valves

3.1 Introduction

Since the finding of the giant magneto resistance (GMR) effect in a magnetic multilayer, the pseudo spin valve (PSV) has shown great promise for applications in Magnetoresistive Random Access Memory (MRAM), pick-up heads, and magnetic sensors [47,48]. According to a previous report [49], the growth of PSV films on nano-oxide layers (NOLs) has led to an enhancement in GMR. A corresponding reduction in minimum film resistance by over 10% confirms that this enhancement originates from an increase in the mean free path of spin-polarized electrons due to the resultant of specular reflection on nano-oxide surfaces. Regarding thermal effects of a PSV with NOL, it is well known that formation of another NOL in the interface between spacer and magnetic layer degenerates the differential spin scattering. Therefore, the DC MR ratio of the PSV decreases with treatment at higher annealing temperatures [12]. In a non-metallic system, the impedance (Z) is comprised of resistance (R), inductance (L), and capacitance (C); therefore, equivalent circuit theory can be used to analysis the AC behavior [51,56]. In our previous work [52], we utilized the impedance technique to investigate the NOL behavior in PSV. In this study, we extend the impedance technique to report on the frequency response features of the magneto impedance (MI) behavior of PSV in more detail and use impedance spectroscopy to conduct nondestructive analysis of a PSV with an NOL after annealing.

Magneto impedance, $MI = M|Z|e^{i\theta}$ = MR (real part of magneto impedance) +iMX, in which $X = X_L - X_C$, of the PSV originates mainly from the inductance and capacitance of the device [13]. It may also contain a small amount of parasitic inductance and capacitance from the wire [54]. For a metallic multilayer such as PSV, X_L usually dominates, with X_C negligible.

The hysteresis loop of the PSV, and the corresponding behaviors of each component of the impedance, i.e., |Z|, θ (phase angle), R, and X, have been carefully examined.

As usual, the MI ratio is defined as 100 % × ($|Z|_{AP}$-$|Z|_{P}$) / $|Z|_{P}$, where the subscript P (AP) stands for the parallel (anti-parallel) magnetization orientation state of the PSV. The magneto phase ratio, MP, magneto reactance ratio, MX, and magneto resistance ratio, MR, are all defined similarly.

3.2 Experiment

A PSV with an NOL of NOL/PSV/substrate was grown by e-gun evaporation at R_T on a thermally oxidized Si (100) wafer with a size of 1 cm × 1cm. The NOL was obtained by oxidizing the thin magnetic layers of Co for ten minutes naturally. The PSV was Ta 0.6/Co-NOL/Co 3/Cu 5/Co 1/Py 3, where Py denotes $Ni_{80}Fe_{20}$ and all thicknesses shown in brackets are given in nanometers. The base pressure of the growing chamber was lower than 5 × 10^{-8} Torr, and during the growth, the pressure never exceed 10^{-7} Torr. The sample was subsequently annealed from R_T to 200℃ for 30 minutes below the pressure 1 × 10^{-2} Torr. The AC behavior was determined by using an HP4194 impedance analyzer with the 16047D fixture. A two-point contact was used in a frequency range from 100 Hz to 40 MHz with a fixed oscillating voltage of ±0.5 V. During the characterization, the ac sensing voltage and external applied field of up to ±100 Oe were applied along the easy axis of the PSV sample, i.e., a longitudinal configuration.

3.3 Magneto Impedance Behavior and Its Equivalent Circuit Analysis of a Co/Cu/Co/Py Pseudo Spin Valve with a Nano-Oxide Layer

3.3.1 Equivalent Circuit for Pseudo Spin Valve

Figure 3.1 shows the frequency dependence of |Z|, R, and X for the PSV at zero applied fields. The X curve was negative at low frequency. It turned positive at the frequency f ≥

476 kHz, indicative of the resonance frequency (f_r) of the circuit. This is in agreement with the simulated equivalent circuit consisting of an equivalent resistance R_{psv} (=103.71 Ω), inductance L_{psv} (=79.85 nH), capacitance C_{PSV} (= 20.83 pF) and a parasitic inductance L_p (=627.8 nH), capacitance C_p (=225.04 nF) and resistance R_{P1} (=1.72 Ω), R_{P2} (=12.86 Ω), respectively, as shown in the inset panel in Fig. 3.1.

The impedance of the equivalent circuit of the PSV is

$$Z = 1 / [1 / (R_{PSV} + i\, 2\, \pi\, f\, L_{PSV}) + (i\, 2\, \pi\, f\, C_{PSV})] + R_{P1} + i\, 2\, \pi\, f\, L_P + 1 / (1 / R_{P2} + i\, 2\, \pi\, f\, C_P),$$

(3.3.1)

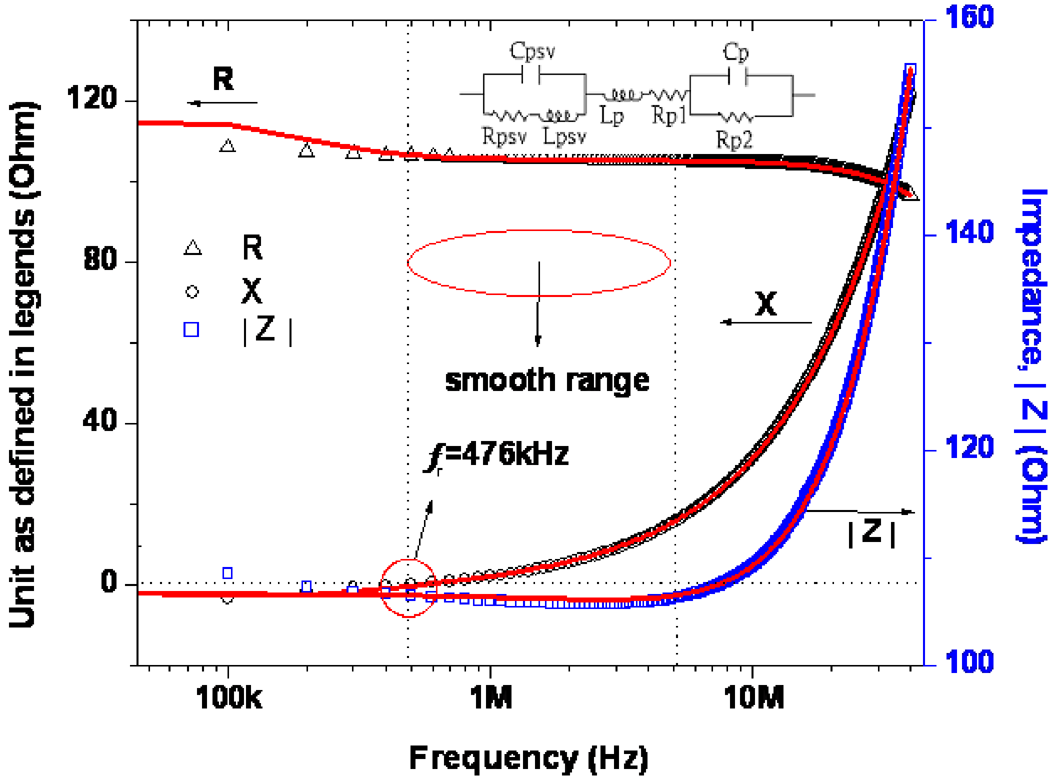

Fig. 3.1. The frequency dependences of |Z|, R and X for the PSV at zero field. The resonance frequency (f_r) is found at 476 kHz, where X vanishes. The experimental data (open symbols) are very close to the theoretical result (solid curves) calculated from the equivalent circuit shown in the inserted panel.

The solid line in |Z| shown in Fig. 3.1 represents the best fit with the experiment data based on eq. (3.3.1). The solid line and the data points fall exactly on top of each other, indicating that the PSV is well represented by the equivalent circuit. Based on this observation, we elaborate on the impedance behavior of PSV under various conditions. The frequency behavior of the PSV, being metallic, is dominated by X_L at high frequency, and X_C is significant only at low frequency. Note that X changes from negative to positive as the frequency is swept from 100Hz to 40 MHz. X vanishes at $f_r = 476$ kHz.

The real part and imaginary parts of the equivalent impedance of the PSV are

$$R_{eff} = R_{PSV} / [(1 - 4\pi^2 f^2 C_{PSV} L_{PSV})^2 + 4\pi^2 f^2 C_{PSV}^2 R_{PSV}^2] + R_{P1} + R_{P2} / (1 + 4\pi^2 f^2 C_P^2 R_{P2}^2)$$

$$X_{eff} = 2\pi f \{L_P + (L_{PSV} - 4\pi^2 f^2 C_{PSV} L_{PSV}^2 - C_{PSV} R_{PSV}^2) / [(1 - 4\pi^2 f^2 C_{PSV} L_{PSV})^2 + 4\pi^2 f^2 C_{PSV}^2 R_{PSV}^2] - C_P R_{P2}^2 / (1 + 4\pi^2 f^2 C_P^2 R_{P2}^2)\}, \qquad (3.3.2)$$

Note that R decreased very slowly at low frequency, and then dropped at a relatively faster pace at higher frequency. This was confirmed by observation. Furthermore, the |Z| value would have shown a minimum at f_r if the real part of the impedance R had remained constant. In fact, this was not the case. Consequently, the minimum value of |Z| drifted to somewhere between 476 kHz and 5 MHz (smooth range), as indicated in Fig. 3.1. For the present case, the minimum value of |Z| took place at a frequency near 2.4 MHz, where the slope of the |Z| curve is flat. Beyond this point, the impedance increased rapidly as X_L became dominant. As noted, the capacitance contribution from the equivalent circuit was minimal. Most of the capacitance effect shown in the equivalent circuit had its origin from the parasitic effects of the wire itself.

With the above-mentioned Eq. (3.3.1) and (3.3.2), the simulation value of the L_{PSV} is

79.85 nH. Let us make a rough order of magnitude estimate of the L value. By definition, L = BA / I, where B is the magnetic field; A (7.94×10^{-11} m^2) is the cross section area of the magnetic multilayer through which B passes, and I (4.37 mA) is the current through the sample. The Ms of the PSV measured by VSM is 595.7 emu / cm^3. By simple relation, L is roughly 13.6 nH. This is of the same order of magnitude as observed.

3.3.2 Magneto Impedance Behavior for Pseudo Spin Valve

Figures 3.2 (a) and (b) show the low frequency response of MI, MP, MR, and MX effects of the PSV at 100 Hz. The behavior of the PSV may be regarded as DC-like at this frequency, and both MX and MP may be treated as frequency independent. On closer inspection, however, the value of the MX at anti-parallel state at $f_r = 476$ kHz is clearly non-zero.

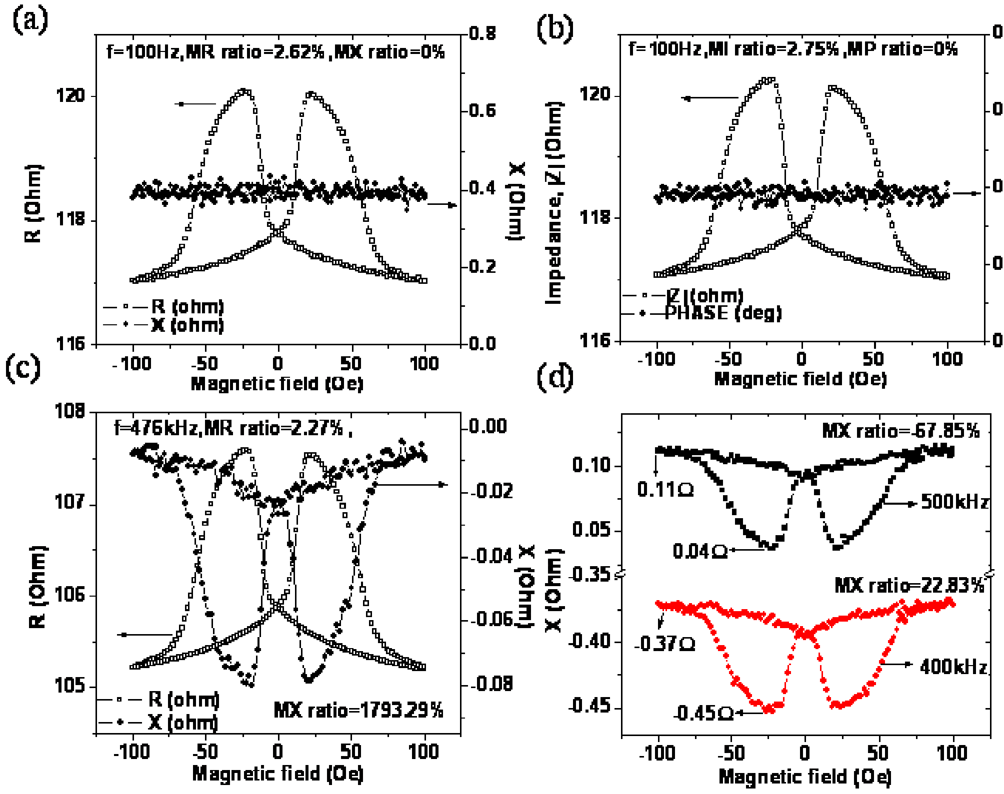

Fig. 3.2. (a), and (b) magneto impedance at 100 Hz. At this low frequency, the magneto transport property can be regarded as DC. (c) at resonance frequency f_r (476 kHz), MX shape of loop reverse to MR loop. (d) The value of MX is negative at $f < f_r$, and switches to positive at $f > f_r$.

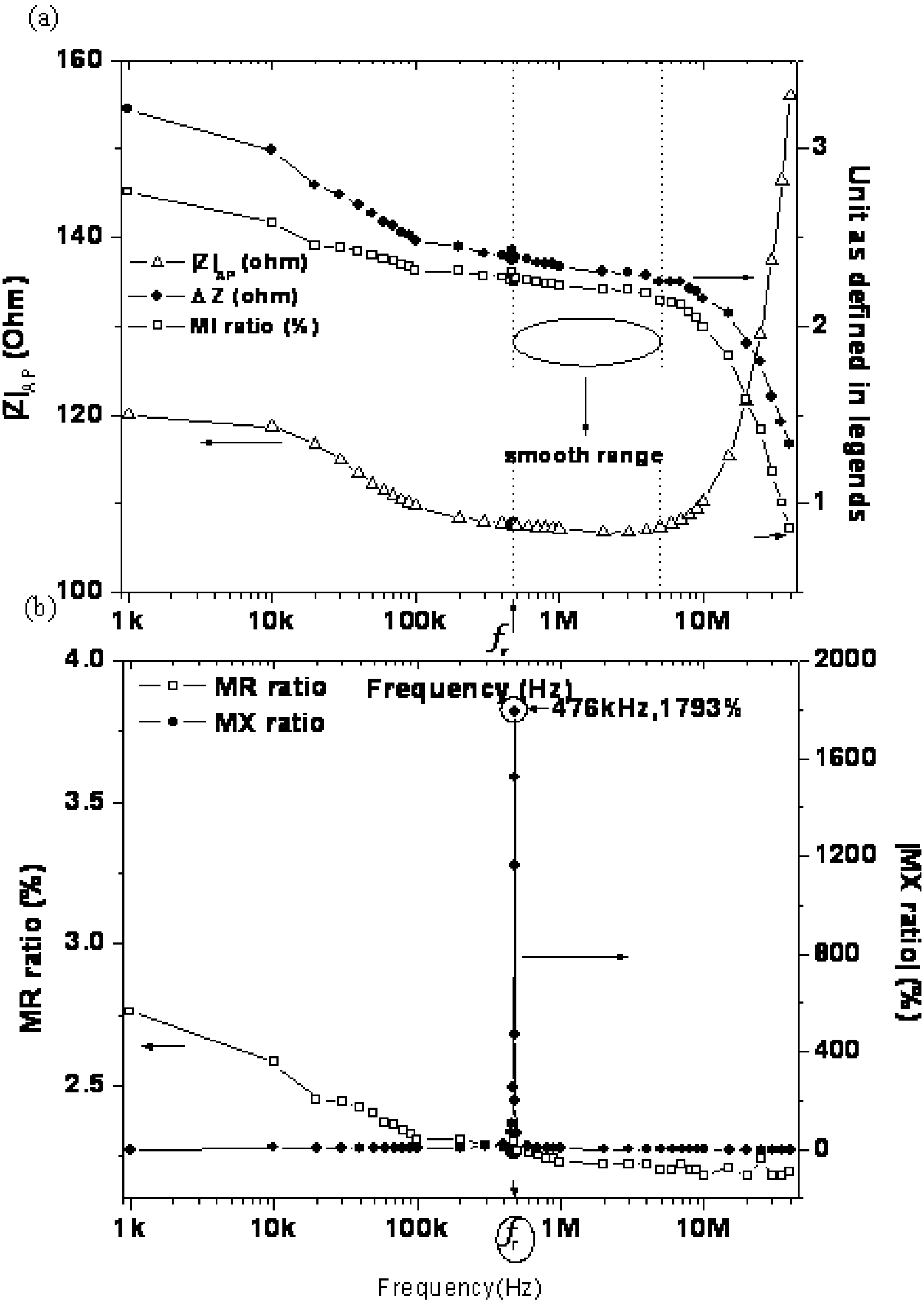

Fig. 3.3. (a) The frequency dependences of $|Z|_{AP}$, $\triangle Z$ and MI ratios. (b) The frequency dependences of MR and |MX ratio|.

Interestingly, it shows an inverted negative MR-like loop behavior, as shown in Fig. 3.2 (c). These results are agreement with a previous report [14]. An MX ratio of more than 1700% was observed. This is due to the fact that the imaginary part of Z at parallel state crosses zero at f_r. Figure 3.2 (d) shows that the MX values change from negative (at $f < f_r$) to positive (at $f > f_r$) at 400~500kHz. The f_r of the PSV is therefore bordering between 400 to 500 kHz in the present sample.

Figure 3.3 (a) shows the frequency dependence of $\triangle|Z|$ and $|Z|_{AP}$ and the MI ratio. The behavior of $|Z|_{AP}$ is nearly the same as that of $|Z|$, as shown in Fig. 3.1. As the frequency increases beyond the smooth range, $|Z|_{AP}$ increases steeply as the X_L increases. It is remarkable that $\triangle|Z|$ decreases slowly but steadily before reaching the smooth range, and then decreases sharply upon passing that smooth range. Since the MI ratio was defined as $\triangle|Z|$ divided by $|Z|_{AP}$, it was predictable that the MI ratio would decrease steadily with increasing frequency, as observed.

Based on these observations, it is reasonable to argue that the variation of the impedance $\triangle|Z|$ of the PSV can be simplified as compounded by the parallel and anti-parallel states of the moments of the PSV. We have

$$\triangle|Z| = Z_{AP} - Z_P = 1/\ ((1/R_{PSV\text{-}AP})^2 + (2\ \pi\ f\ C_{PSV\text{-}AP})^2) - 1/\ ((1/R_{PSV\text{-}P})^2 + (2\ \pi\ f\ C_{PSV\text{-}P})^2), \tag{3.3.3}$$

Since the R_{PSV} and C_{PSV} depend upon the magnetization state, the behavior of the $\triangle|Z|$ is sensitively influenced by the existence (or, effectively, the vacancy density) of the capacitance of the NOL in the PSV, and decreases as the frequency increases. The frequency dependences of the MR and the absolute value of the MX ratios are shown in Fig. 3.3 (b). The MR ratio changes only slightly as the frequency changes. In contrast, the |MX ratio| is sharply peaked at the f_r. The value of |MX ratio| is very small at a frequency away from the f_r but shows an astounding peak when X_{AP} is close to zero. A small change in X_{AP} would bring about a great change in the |MX ratio| (~ 1793% in the present sample).

3.3.3 Annealing Effect

The DC MR ratio of the PSV decreased as the annealing temperature increased, which occurred because NOL formed in the interface between spacer and magnetic layer. For this reason, we used the impedance technique to analysis the capacitance effect, which is caused by oxidation. Figure 3.4 shows that the resistance of the PSV increased from 21.80 to 28.98 ohm and the DC MR ratio of the PSV decreased from 5.41 to 0.48 % as the annealing temperature increased from R_T to 200°C, which indicates that oxidation occurred in the PSV.

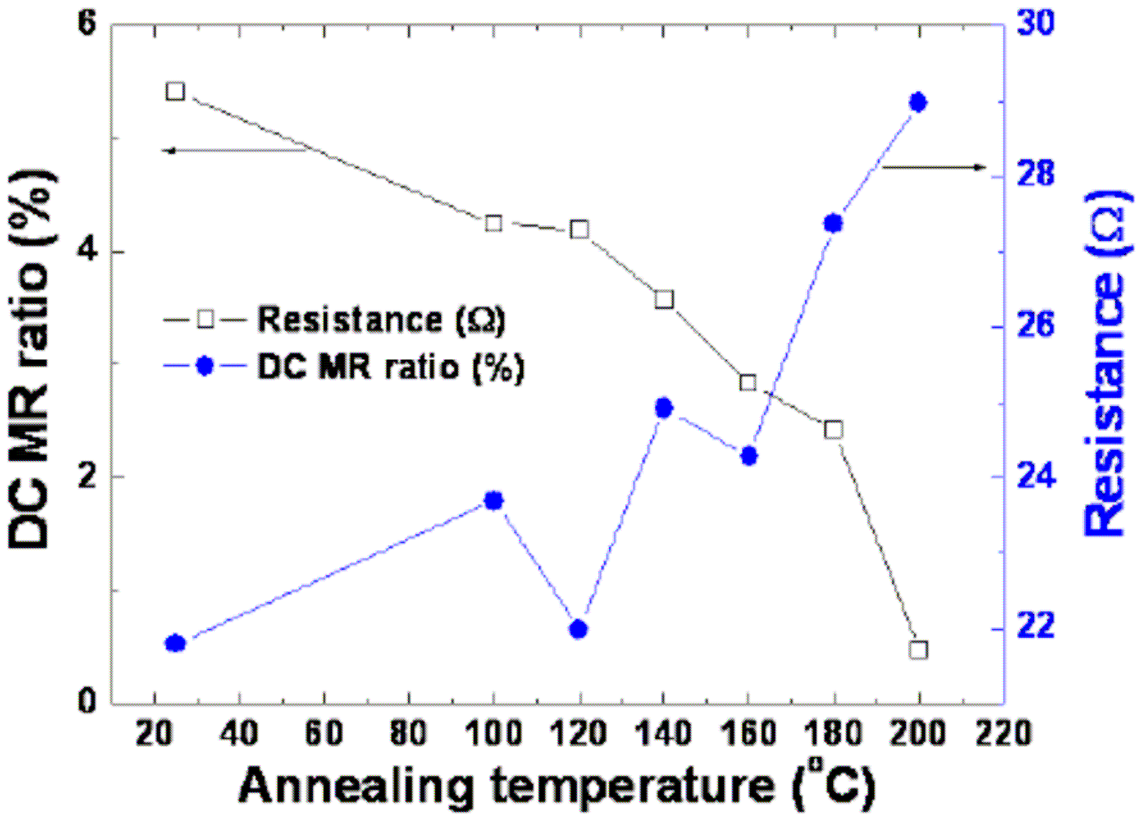

Fig. 3.4. The DC MR ratio and resistance (R) of the PSV are functions of the annealing temperature.

Therefore, the effective capacitance was measured by imaginary part of impedance (Im (Z)) curves, as shown in Fig. 3.5. Im (Z) reached a minimum at roll-off frequency (f_{roll}). The plot of f_{roll} as a function of annealing temperature is shown in Fig. 3.6; f_{roll} increased linearly from 345 to 465 kHz between annealing temperatures R_T to 200 °C. It is quite interesting to analyze the effective capacitance effects with changes in annealing temperature. According to the effective capacitance calculation, f_{roll} can be shown as:

$$f_{roll} = 1 / (2\pi R_{eff} C_{eff}), \tag{3.3.4}$$

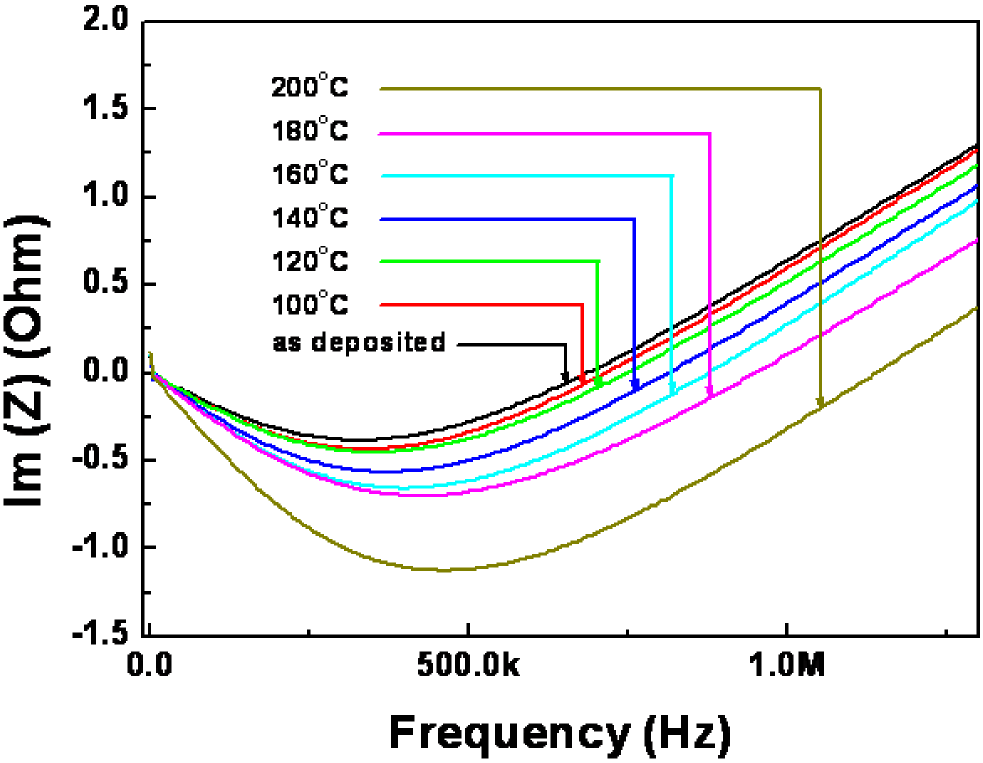

Fig. 3.5. Imaginary part of impedance curves for PSV with different AT temperatures ranging from R_T to 200°C.

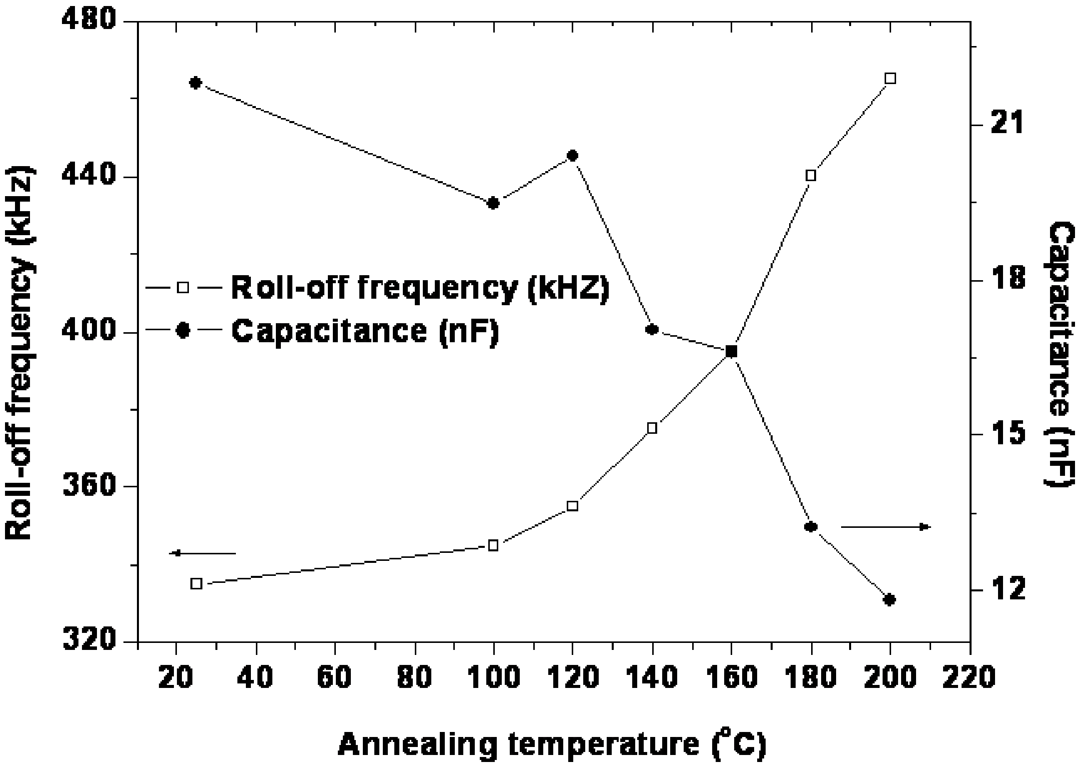

Fig. 3.6. The roll-off frequency and effective capacitance of the PSV are functions of the annealing temperature.

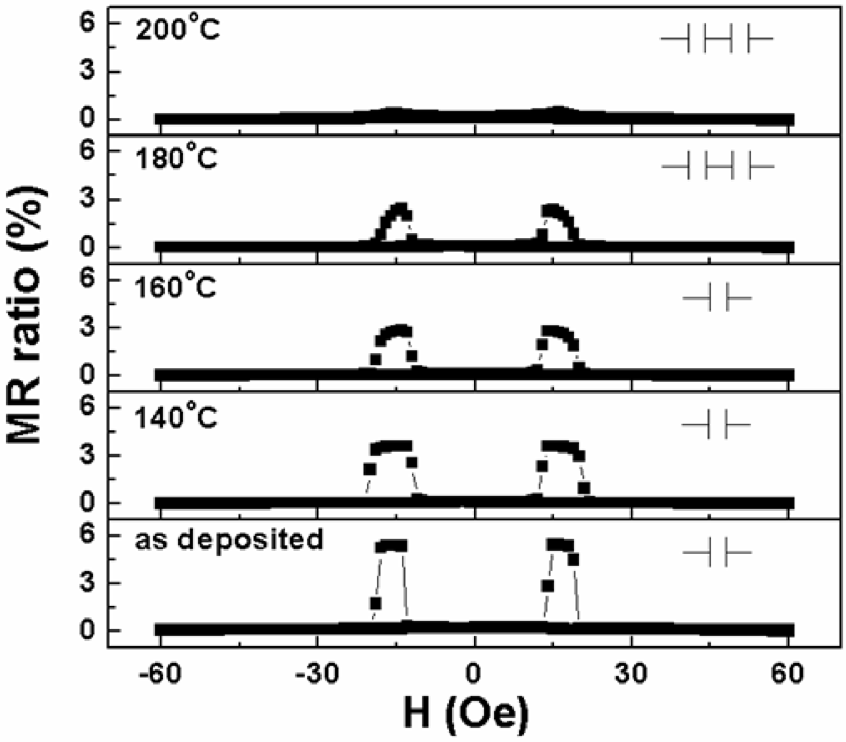

Fig. 3.7. The hysteresis loops of the PSV with AT temperatures R_T, 140°C, 160°C, 180°C, 200°C, respectively. The inset panels show the equivalent capacitor modes.

The effective capacitance is in reverse proportion to the f_{roll} and estimated values, and it varies from 21.8 to11.8 nF as annealing temperatures increases from R_T to 200 ^{o}C. One possible explanation is that the effective capacitance decreases as annealing temperature increases by hysteresis loops, as shown in Fig. 3.7. The coercivity (Hc) of Co is 20 Oe, and the H_C of Co-Py coupled is 12 Oe in the PSV, which was deposited at R_T. When the annealing temperature was increased to 140^{o}C, the H_C of Co was apparently incoherent in the PSV, indicating that the oxidation effect occurred in the Co layer. The oxidative thickness is in proportion to f_{roll} and in reverse proportion to C_{eff} [52]. The result of $f_{roll,}$ which increased as annealing temperature increased to 140^{o}C, indicated that the oxidative thickness of Co layer was increasing. This increase in thickness caused the resistance to increase and the DC MR ratio to decrease slightly. Above the annealing temperature of 140 ^{o}C, it is difficult to distinguish the Hc of Co or that of Co-Py, implying that the oxidation effect occurs in the Co/Cu or Co-Py/Cu interfaces. They could be regarded to two capacitors in series, thus causing a decrease in effective capacitance, as shown in the inset panel in Fig. 3.7. Therefore, the f_{roll} increases and effective capacitance decreases as the annealing temperature increases, indicating that the increase in annealing temperature causes the oxidative thickness to increase and oxidize more than one layer.

3.3.4 Conclusion

In conclusion, the AC behavior in the Pseudo spin valve led to interesting MR and MX loops, with the MR loop a reversal of the MX loop. The magneto impedance effect of PSV has been investigated at R_T. It is found that the PSV can be regarded as a combination of resistances (R_{PSV}, $R_{P1,}$ R_{P2}), inductances (L_{PSV}, L_P), and capacitances (C_{PSV}, C_p), and equivalent circuit theory can be used to analysis the AC behavior of this system. It is quite interesting that the |MX| ratio is more than 1700 % at f_r = 476 kHz. This suggests strongly that PSV is potentially a very sensitive frequency sensor. The magneto impedance behavior in the

Co/Cu/Co/NiFe pseudo spin valve with a nano-oxide layer after annealing treatment has also been studied. Its roll-off frequency increases from 345 to 465 kHz, and the effective capacitance decreases from 21.8 to11.8 nF as the annealing temperature increases from R_T to 200°C. We can utilize the equivalent capacitor circuit to explain the NOL behavior with annealing temperature. This study shows that impedance analysis is a useful technique, and its nondestructive measurement should be more widely appreciated.

3.4 Characterization of a Nano-Oxide Layer in a Pseudo Spin Valve by Complex Magneto-Impedance Spectroscopy

3.4.1 Magneto Impedance Study for Different Thickness of Bottom Nano-Oxide Layer

The different thickness of the bottom $Ni_{80}Fe_{20}$ NOL in PSV was obtained by deposited different thicknesses of the bottom $Ni_{80}Fe_{20}$ layer to undergo the same oxidation process. As shown in Fig. 3.8, the resistances for PSV with different thickness bottom $Ni_{80}Fe_{20}$ NOL are almost the same and the MR ratio increase from 3.24 % for the sample without $Ni_{80}Fe_{20}$ NOL to its maximum value of 7.1 % for the sample with 1 nm of $Ni_{80}Fe_{20}$ NOL. Further increment of the $Ni_{80}Fe_{20}$ NOL thickness did not bring MR ratio any enhancement. This indicates that the oxidation stopped at ~ 1 nm of the bottom $Ni_{80}Fe_{20}$. The inset panel in Fig. 3.8 shows the magneto impedance of the PSV with d = 1 nm, whose ratios of the real and the imaginary parts of impedance at zero frequency (f_Z) (the frequency at which the Im (Z) was closed to zero, under this definition, f_z = 415 kHz for d = 1 nm) are 3.4 % and -1300%, respectively. Such a huge MZ_{im} ratio was due to the fact that the imaginary part of Z crossed zero at f_Z. The reverse loop of Im (MZ) with respect to that of the Re (MZ) meant they were 90 degrees out of phase. The MZ_{Im} loop mainly came from the capacitance effect of the NOL layer in the PSV. That the magnetocapacitance was larger in the parallel state and smaller in the anti-parallel state was silimar to Ref. [55]; therefore, the MZ_{Im} behavior is reversed to MZ_{Re}. The most basic capacitance model is the Maxwell-Wagner capacitor, which consists of two dielectric materials. The charges collect at the interface between the dielectrics as well as on the capacitor plates due to different conductivities. The frequency dependence at zero filed on the Im (Z) of the PSV with the bottom $Ni_{80}Fe_{20}$ NOL whose thickness was ranged from 0 to 1 nm is shown in Fig. 3.9.

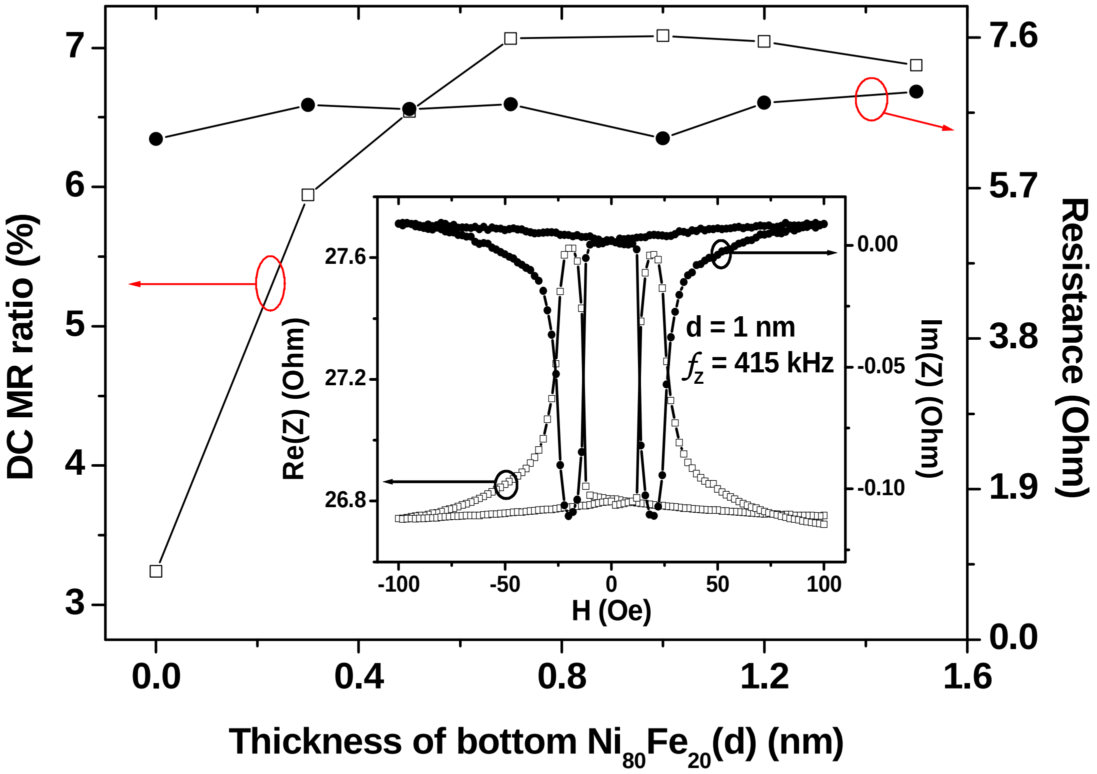

Fig. 3.8. The dependences on MR ratio, resistance, and thickness of the bottom $Ni_{80}Fe_{20}$ in the structure of Ta 0.6 / NOL / Co 3 / Cu 4 / Co 1 / $Ni_{80}Fe_{20}$ 3 / NOL / $Ni_{80}Fe_{20}$ (d) / substrate, in which the bottom $Ni_{80}Fe_{20}$ was naturally oxidized for ten minutes. The inset panel shows the magneto impedance at frequency 415 kHz for PSV with d = 1 nm, the shape of MZ_{Im} loop is reversed to that of MZ_{Re}.

Obviously, the different bottom $Ni_{80}Fe_{20}$ NOL thicknesses made shifts in f_r. The positive Im (Z) at high frequency came from the parasitic inductance of the measurement circuit. It was necessary and hard to subtract during the measuring; however, it did not influence the MZ_{Im} loop due to it was magnetic filed independent. The capacitance of the PSV originated from the top and the bottom NOLs. Fig. 3.10 (a) shows the dependence of d on the f_r and calculated capacitance.

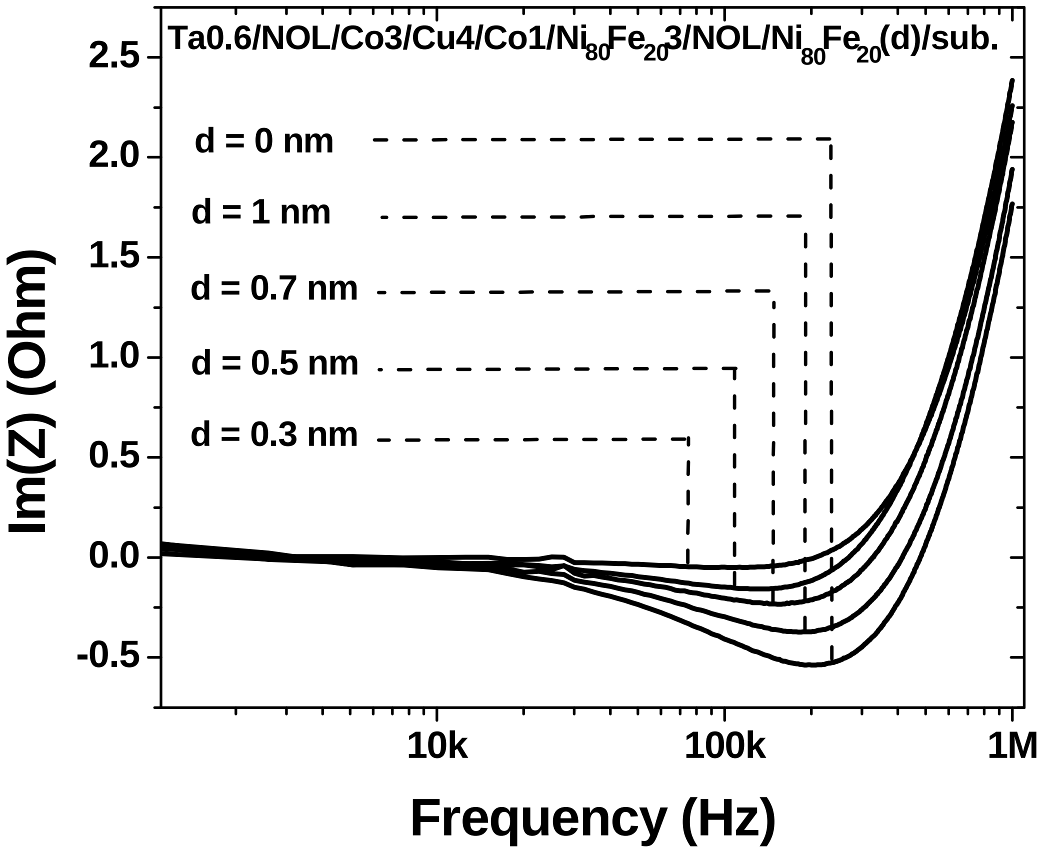

Fig. 3.9. The imaginary parts of impedance curves for PSV with different thicknesses of the bottom $Ni_{80}Fe_{20}$ NOL ranged from 0 to 1 nm at zero fields. Except the PSV without $Ni_{80}Fe_{20}$ NOL, the roll-off frequencies increases as the thickness of the $Ni_{80}Fe_{20}$ NOL increasing.

The C_{eff} was derived from the general definition of the f_r:

$$f_r = 1 / (2\pi RC_{eff}) \tag{3.4.1}$$

As described in Eq. (3.4.1), the roll-off frequency is reverse proportion to the capacitance. Since the parasitic inductance was hard to subtract, the equivalent circuit of the measurement, as shown in Fig. 3.10 (b), was used to calculate the C_{NOL}. As seen from Fig. 3.10 (a), the C_{eff} and C_{NOL} have very the same trend as d increasing, while the C_{int} was almost the same. The f_r increased linearly as d increasing to 1 nm; however, when d was larger than 1 nm, the un-oxidized $Ni_{80}Fe_{20}$ brought out an additional interface then made the C_{eff} and C_{NOL} increased.

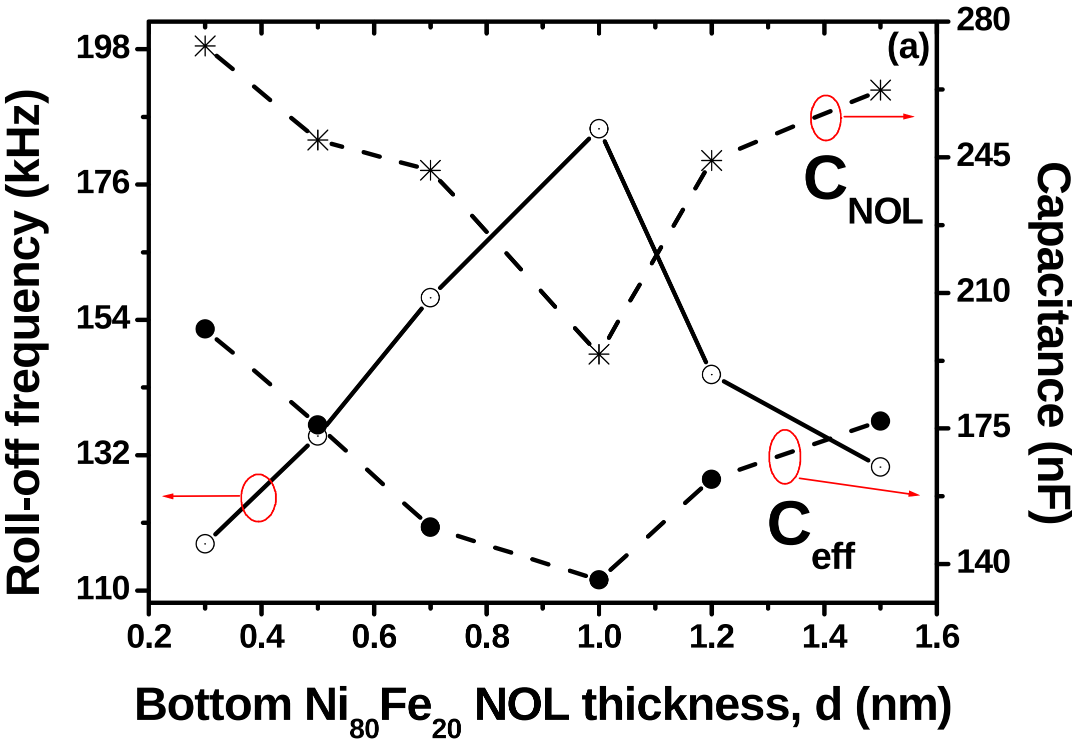

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Fig. 3.10. (a) The roll-off frequency and calculated effective and NOL capacitance are functions of the thickness of the bottom $Ni_{80}Fe_{20}$ NOL thickness. (b) The equivalent circuit of the measurement is a complex RLC combination.

The well known definition of capacitor plates is C = ε_0 A / d. Thus, the increasing of d caused the capacitance decreased. Since the top Co NOL had fixed thickness, the thicker bottom $Ni_{80}Fe_{20}$ NOL implied larger C_{NOL} and then larger f_r.

3.4.2 Double Nano-Oxide Layers Effect

Fig. 3.11 shows the frequency dependence of the Im (Z) for the PSV with different NOL structures. The bottom NOL of Ta1 /Co3 /Cu4.5 /Co1 /$Ni_{80}Fe_{20}$3 /NOL /Co1 /substrate and top NOL of Ta1 /NOL /Co3 /Cu4.5 /Co1 / $Ni_{80}Fe_{20}$3 /Co1 /substrate have similar structure, and only the position of the Co NOL was different.

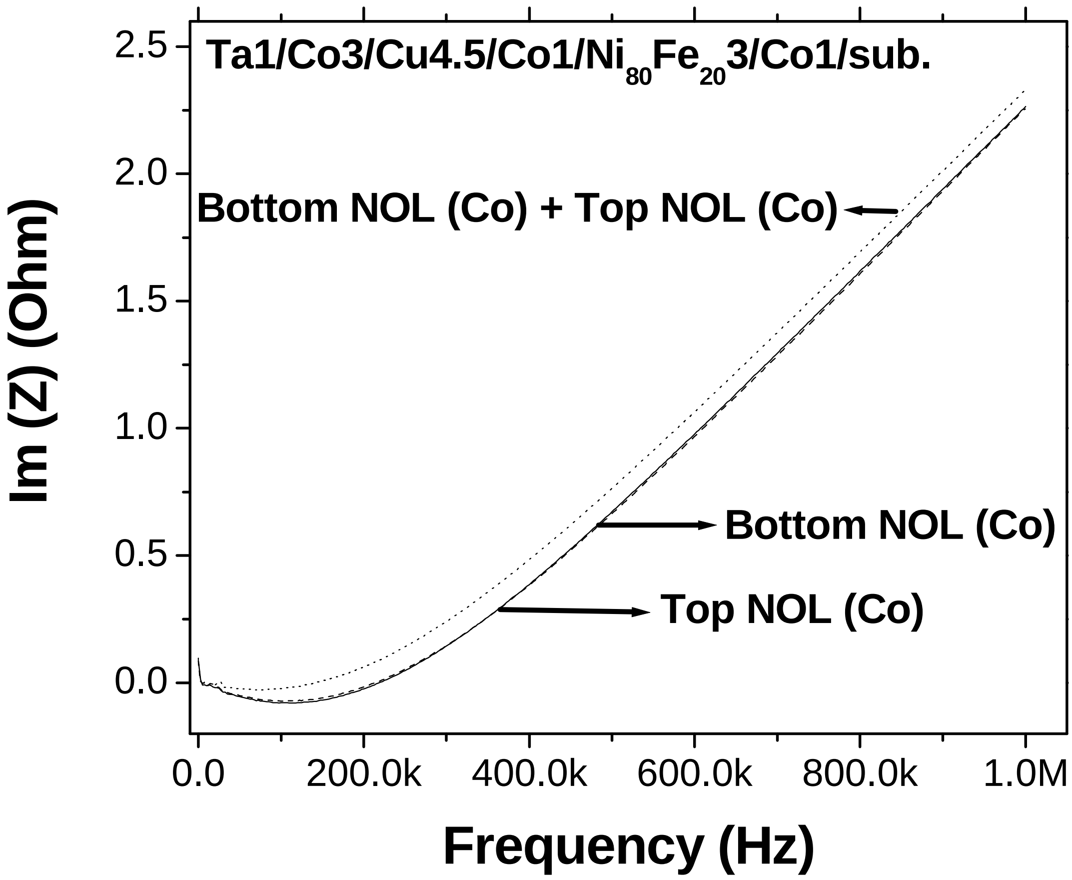


Fig. 3.11. The imaginary part of impedance curve for PSV with different NOL structures at zero fields. The film structure is Ta / (Co NOL) /Cu /Co /$Ni_{80}Fe_{20}$ / (Co NOL) /sub.

The Im (Z) curves were indistinguishable due to the same thickness of the oxide Co layers, and hence, they have a similar reactance effect. The Im (Z) curve of the PSV with double NOLs, the top Co NOL and the bottom Co NOL, is clearly different from that of the PSV with only one Co NOL. The f_r of the PSV with double NOLs is smaller than that of the PSV with only the top Co NOL or the bottom Co NOL. This result was agreed because of that two NOLs in the PSV brought out the larger capacitance.

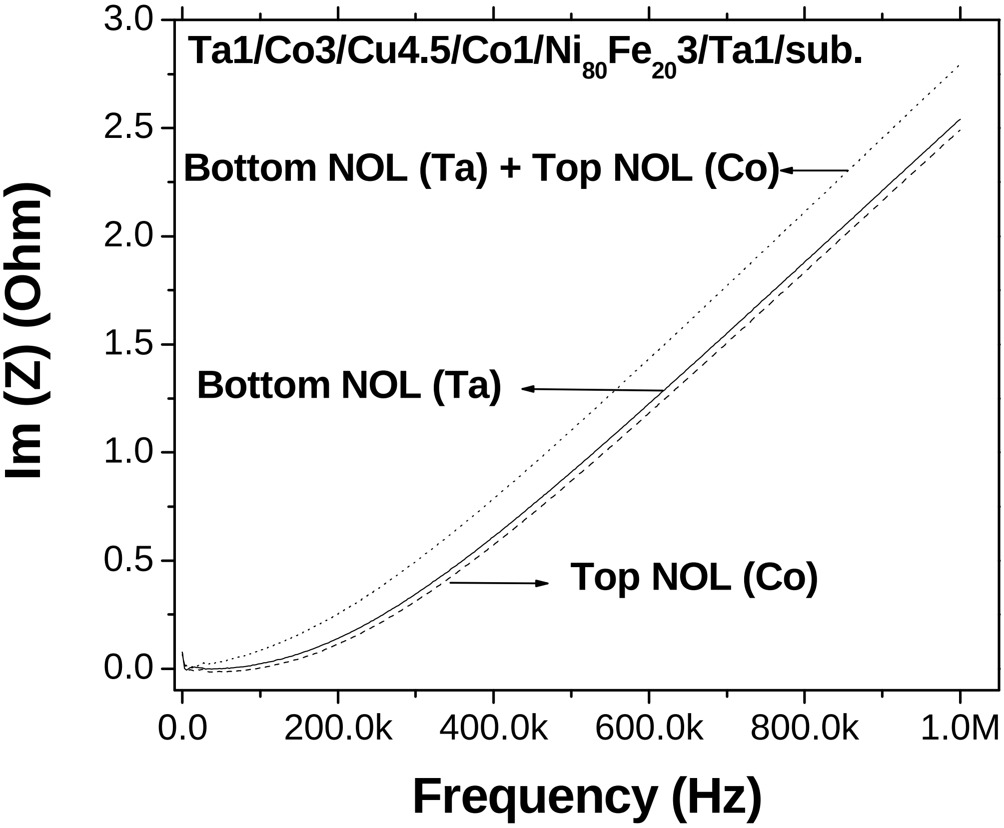


Fig. 3.12. The imaginary part of impedance curve for PSV with different NOL structures at zero fields. The film structure is Ta / (Co NOL) /Cu /Co /$Ni_{80}Fe_{20}$ / (Ta NOL) /sub.

It is interesting that the obvious change of the Im (Z) curves was found when the bottom NOL and the top NOL were different oxidized materials, such as Co and Ta, with the same oxidation process, as shown in Fig. 3.12. That the Im (Z) curves were separated obviously indicated that these PSVs with different capacitances. The f_r of the PSV with the bottom Ta NOL and the PSV with the top Co NOL is 30 kHz 37.5 kHz, respectively. This indicates that the capacitance effect of the bottom Ta NOL is larger than that of the top Co NOL. In general, Co is more easily oxidized than Ta because the condensed TaO_X on the surface of Ta would prevent the Ta under the TaO_x from following oxidation. Then, during the same oxidation time, the thickness of the top Co NOL is thicker than that of the bottom Ta NOL. Therefore, the f_r of the PSV with the top Co NOL is larger than that of the PSV with the bottom Ta NOL. The f_r of the PSV with double NOLs is 7.6 kHz. Obviously, the double NOL has the largest effective capacitance, which is contributed from the top NOL and the bottom NOL, and thus the smaller f_r.

3.4.3 Conclusion

In conclusion, the impedance spectroscopy to check the capacitance effect of the PSV with different NOL structures was introduced. The PSV with NOL brought out an enhancement on capacitance, and this was easily characterized by the shifts of the roll-off frequency. The roll-off frequency is linear to the NOL thickness, and showed the reverse proportion to the C_{eff} and calculated C_{NOL} when the bottom $Ni_{80}Fe_{20}$ layer was fully oxidized. By this non-deconstructive impedance spectroscopy analysis method, the properties of the NOL in PSV could be easily distinguished.

3.5 Summary

Magnetoimpedance behaviors and thermal effects of a Co/Cu/Co/Py pseudo-spin-valve (PSV) with a nano-oxide layer (NOL) were studied. The PSV can be regarded as a combination of resistances, inductances, and capacitances. In addition, equivalent circuit theory can be used to analyze the ac behavior of this system. The imaginary part of the magnetoimpedance (magnetoreactance) ratio is more than 1700% at the resonance frequency (f_r)=476 kHz at room temperature (R_T). The dc magnetoresistance (MR) ratio decreases as the annealing temperature increases because the NOL is formed at the interface between the spacer and the magnetic layer. The NOL deteriorates the differential spin scattering and reduces the dc MR ratio. Impedance spectroscopy was utilized to analyze the capacitance effect from NOL after annealing. The effective capacitance of the PSV was 21.8 nF at RT and changed to 11.8 nF after annealing at 200 °C. The useful equivalent capacitor circuit not only is a nondestructive measurement technology but can also explain the experimental results and prove the formation of the NOL.

CHAPTER 4

Magneto Impedance Study for Magneto Tunneling Junctions

4.1 Introduction

The magnetic tunnel junction (MTJ) is an excellent system for investigating the spin-polarized electron coherent tunneling effect and both theoretical and experimental studies on the MTJ are interesting topics of current research [50,53,55,57,58]. However, the studies of impedance as a function of magnetic field on MTJ are still rare which motivated us to study the impedance as a function of magnetic fields on an MTJ system.

Inverse MR behavior has been reported in the MTJ structure with a DC measurement [59,60], but the inverse magneto impedance (MZ) properties have not been studied yet. Most research on the hysteresis properties of MTJ focus on DC measurement and low frequency AC measurement, which show low resistance in the parallel state and high resistance in the anti-parallel state. In this study, the frequency was raised to 40 MHz, and the magneto impedance, $Z = |Z|e^{i\theta} = R+iX$ in which $X = X_L-X_C$ [53-55], of an MTJ device was studied. The MZ ratio is defined as 100 % × $(Z_{AP}-Z_P) / Z_P$, where the subscript P (AP) stands for the parallel (anti-parallel) magnetization orientation state of the MTJ.

4.2 Experiment

The MTJ structures of Ru(5) /Cu(10) /Ru(5) /IrMn(10) /CoFeB(4) /Al (1.2)-oxide /CoFeB(4) /Ru(5) with DC-MR of 14.3% were deposited on Si/SiO wafers using the Magnetron Sputtering System, where all thicknesses are given in nm, with the junction area 6um x 6um as shown in Figure 4.1. The AC behavior was determined by using the HP4194 impedance analyzer with the 16047D fixture. A two-point contact was used in a frequency range from 100 Hz to 40 MHz with a fixed oscillating voltage of 0.5V, together with an electromagnet which supplied a dc field up to ±500 Oe.

4.3 Enhancement and Inverse Behaviors of Magneto Impedance in a Magneto Tunneling Junction by Driving Frequency

4.3.1 Equivalent Circuit for Magneto Tunneling Junction

Figure 4.2 shows the frequency dependence of the real part of impedance (R_{AP}, R_P) and the imaginary part of impedance (X_{AP}, X_P) for the MTJ in the parallel and anti-parallel states. The R_{AP} and R_P curves decrease with increasing frequency, which indicates that the MTJ includes a significant capacitance effect.

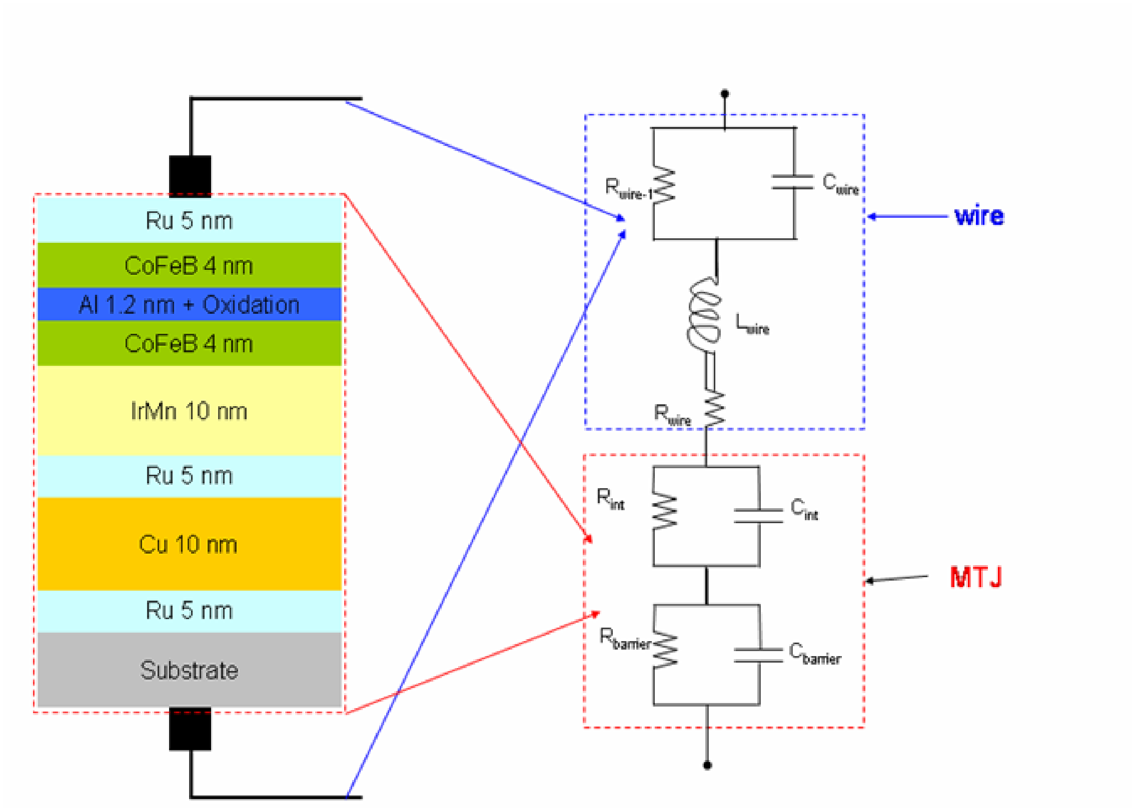


Fig. 4.1. (a) The structure of the magneto tunneling junctions is Ru (5nm) /Cu (10nm) /Ru(5nm) /IrMn(10nm) /CoFeB(4nm) /Al(1.2nm)-oxide /CoFeB (4nm) /Ru (5nm) and equivalent circuit with contributions from magneto tunneling junctions.

Therefore, a Maxwell-Wagner (M-W) model capacitor consisting of dielectric material [53] with the equivalent circuit (EC) theory could be used to analyze our sample.

The EC consists of two parts, the MTJ and the sensing circuit as sketched in Figure 4.1. In the MTJ part, the circuit contains not only the resistance (R_{barrier}) and capacitance (C_{barrier}) from the barrier but also has contributions from the interface, R_{int} and C_{int}, respectively. In the other part, the circuit components contain a resistor, a capacitor, and an ignorable inductor however, this part does not respond to the variation of the magnetic field. According to the EC theory, $Z = R_{eff} + iX_{eff}$ can be expressed as follows:

$$R_{eff} = R_{\mathrm{barrier}} / \{[1 + (2\pi f C_{\mathrm{barrier}} R_{\mathrm{barrier}})^2]\} + R_{\mathrm{int}} / \{[1 + (2\pi f C_{\mathrm{int}} R_{\mathrm{int}})^2]\} + R_{\mathrm{wire}} + R_{\mathrm{wire\text{-}1}} / \{[1 + (2\pi f C_{\mathrm{wire}} R_{\mathrm{wire\text{-}1}})^2]\} \qquad \text{eq.(4.3.1)}$$

$$X_{eff} = 2\pi f \{L_{\mathrm{wire}} - (C_{\mathrm{barrier}} R_{\mathrm{barrier}}^2 / [1 + (2\pi f C_{\mathrm{barrier}} R_{\mathrm{barrier}})^2] + C_{\mathrm{int}} R_{\mathrm{int}}^2 / [1 + (2\pi f C_{\mathrm{int}} R_{\mathrm{int}})^2] + C_{\mathrm{wire}} R_{\mathrm{wire\text{-}1}}^2 / [1 + (2\pi f C_{\mathrm{wire}} R_{\mathrm{wire\text{-}1}})^2]\} \qquad \text{eq.(4.3.2)}$$

4.3.2 Frequency Dependence for Magneto Tunneling Junction

The solid line of these equations as a function of frequency is displayed in Figure 4.2, which shows good agreement with experimental results (dot). The simulated values of R_{barrier}, R_{int}, C_{barrier}, and C_{int} in the parallel state are found to be 155.75 Ω, 83.60 Ω, 54.21 pF, and 38.16 pF, respectively, and those of R_{barrier}, R_{int}, C_{barrier}, and C_{int} in the anti-parallel state are 204.82 Ω, 69.37 Ω, 45.35 pF, and 43.45 pF, respectively. On closer inspection of the real part of the impedance value at the crossover frequency of 21.1 MHz, as shown in the inset panel, it emerges that the real part of the impedance in the parallel state is equal to that in the anti-parallel state, and after the crossover frequency 21.1 MHz, the real part of the impedance in the parallel state is larger than that in the anti-parallel state. This is due to the different frequency dependence of the resistance and capacitance of the MTJ in the parallel and anti-parallel states. Therefore, with an AC current in MTJ, the magnetic behavior can be switched by the driving frequency.

The imaginary part of the impedance of the MTJ in the parallel state X_P shows zero at a resonance frequency of 17.7 MHz. This means that the reactance effect is zero at the resonance frequency in the parallel state, but the reactance effect of the MTJ in the anti-parallel state at 17.7 MHz is not zero. According to the ratio calculation, it must have a high reactance ratio at 17.7 MHz. Therefore, we tried to take the hysteresis plots of R, X and Z of MTJ at the interesting frequencies.

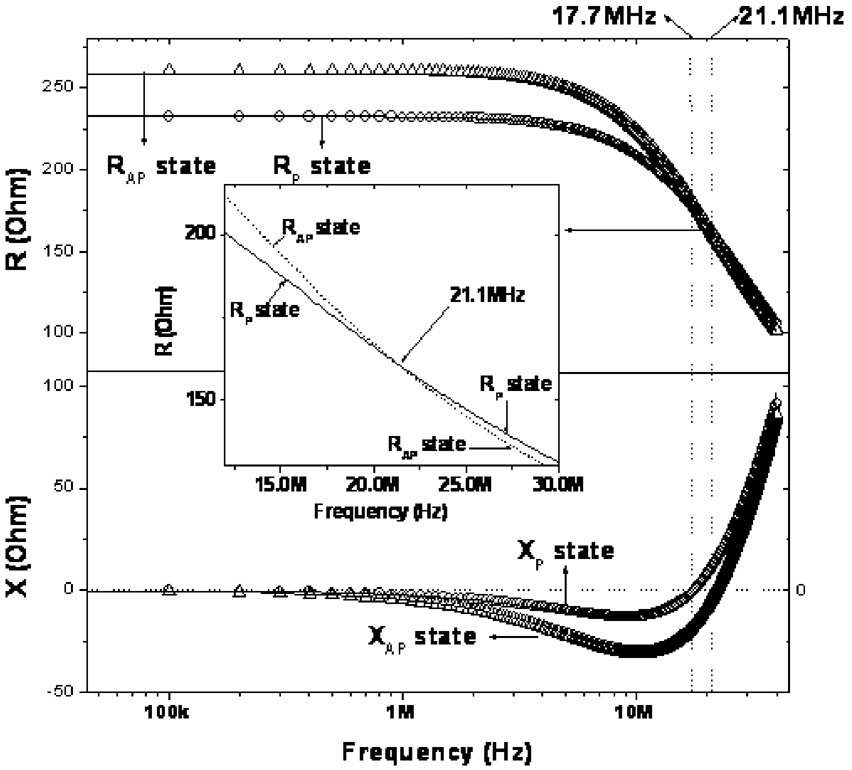


Fig. 4.2. The frequency dependences of the real part of the impedance (R) and the imaginary part of the impedance(X) for the magneto tunneling junctions in the parallel or anti-parallel states. The inset panel shows the crossover frequency of the real part of the impedance, which indicates that the magnetic behavior of MTJ is changed by the driving frequency.

Figures 4.3 (a), (b), and (c) show the real part(R), imaginary parts(X), and total impedance(Z) of the tunneling magneto-impedance (TMI) at frequencies of 100, 17.7M, 21.1M, and 40 MHz, respectively. The real part of the impedance decreases from 12.48% at 100Hz to 1.85% at 17.7 MHz. It is very small (0.37 %) at a frequency of 21.1MHz, and the MR ratio changes signs after crossing the 21.1 MHz line. The MR ratio becomes -3.63% at 40 MHz, as shown in Fig. 4.3 (a). The frequency dependent inverse behavior in the MR loop around a certain frequency is due to the competition among R and C parallel modes in the circuit. At a low frequency ($f < 21.1$ MHz), the effective impedance in this model, Z_R is smaller than Z_C, the R dominates, and most of the current goes through the R circuit. On the contrary, at a higher frequency ($f > 21.1$ MHz), Z_R is larger than Z_C, so the C dominates, and the reverse MR loop occurs. The imaginary part of the impedance is not changed by the applied magnetic field at 100 Hz. However, the imaginary part of the impedance exhibits the maximum value in its parallel state and the minimum value in its anti-parallel state at frequencies of 17.7 MHz, 21.1 MHz, and 40 MHz, as shown in Fig. 4.3 (b). The trend of the MX loop is mainly the capacitance effect in the MTJ. The capacitance is larger in the parallel state and smaller in the anti-parallel state [52, 55-56]. The magneto impedance MX shows maximum and minimum values of ± 17,000 % near a frequency of 17.7 MHz. This is due to the fact that the imaginary part of the impedance crosses zero at this resonance frequency. The frequency dependence by the total magneto-impedance effect MZ loop is similar to that of the MR loop behavior, as shown in Fig. 4.3 (c). MZ = MR + i MX, and the MR loop reverses the shape while crossing the crossover frequency 21.1 MHz. Consequently, MZ reverses its shape with quite similar behavior of the MR. Apparently, Fig 4.3 shows that the magnetization reversal depends on the driving frequency of the sensing current. However, this is not true, as shown by carefully examination by magneto-optical Kerr effect (MOKE) measurements, since the hysteresis loops extracted by MOKE at the same time of MI measurements did not show any difference at different frequencies even around the f_r.

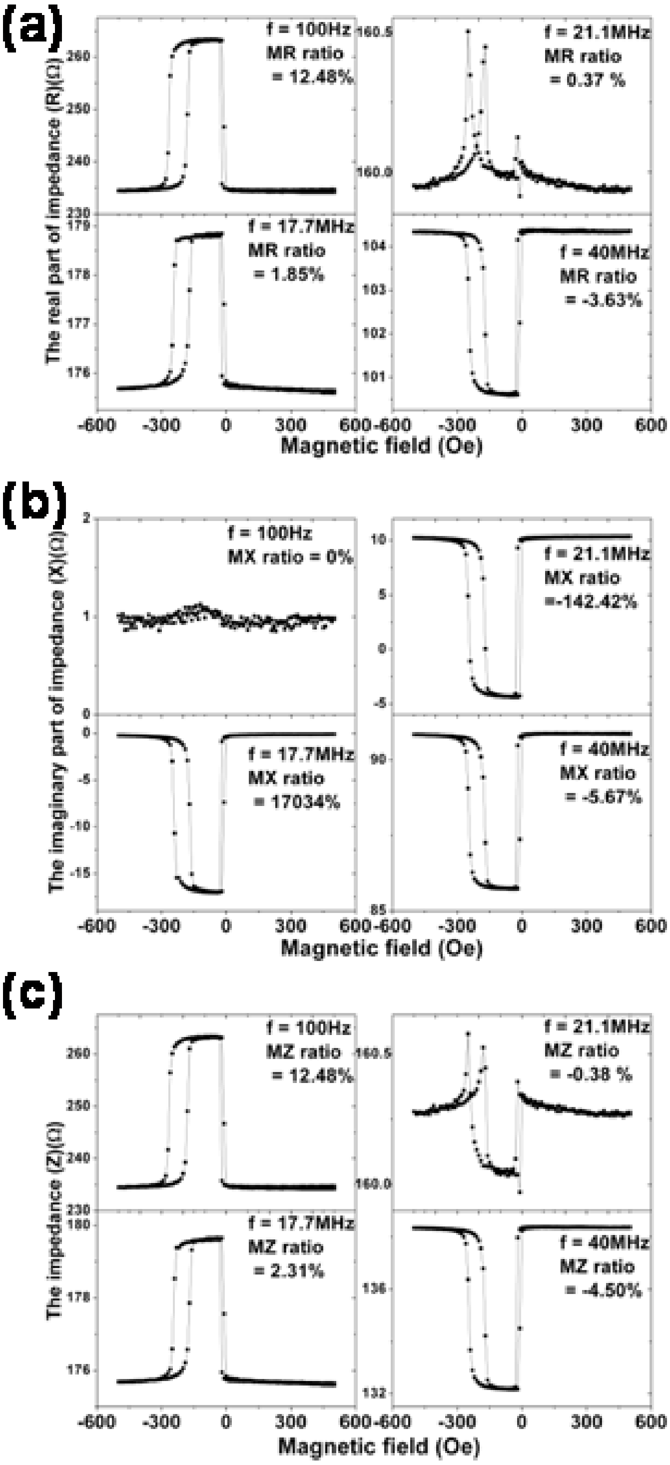


Fig. 4.3. (a) The real part of the impedance (R) curves at frequencies of 100Hz, 17.7MHz (resonance frequency), 21.1MHz (crossover frequency), and 40MHz for the magneto tunneling junctions. (b) The imaginary part of the impedance (X) curves at frequencies of 100Hz, 17.7MHz (resonance frequency), 21.1MHz (crossover frequency), and 40MHz for the magneto tunneling junctions. (c) The impedance (Z) curves at frequencies of 100Hz, 17.7MHz (resonance frequency), 21.1MHz (crossover frequency), and 40MHz for the magneto tunneling junctions.

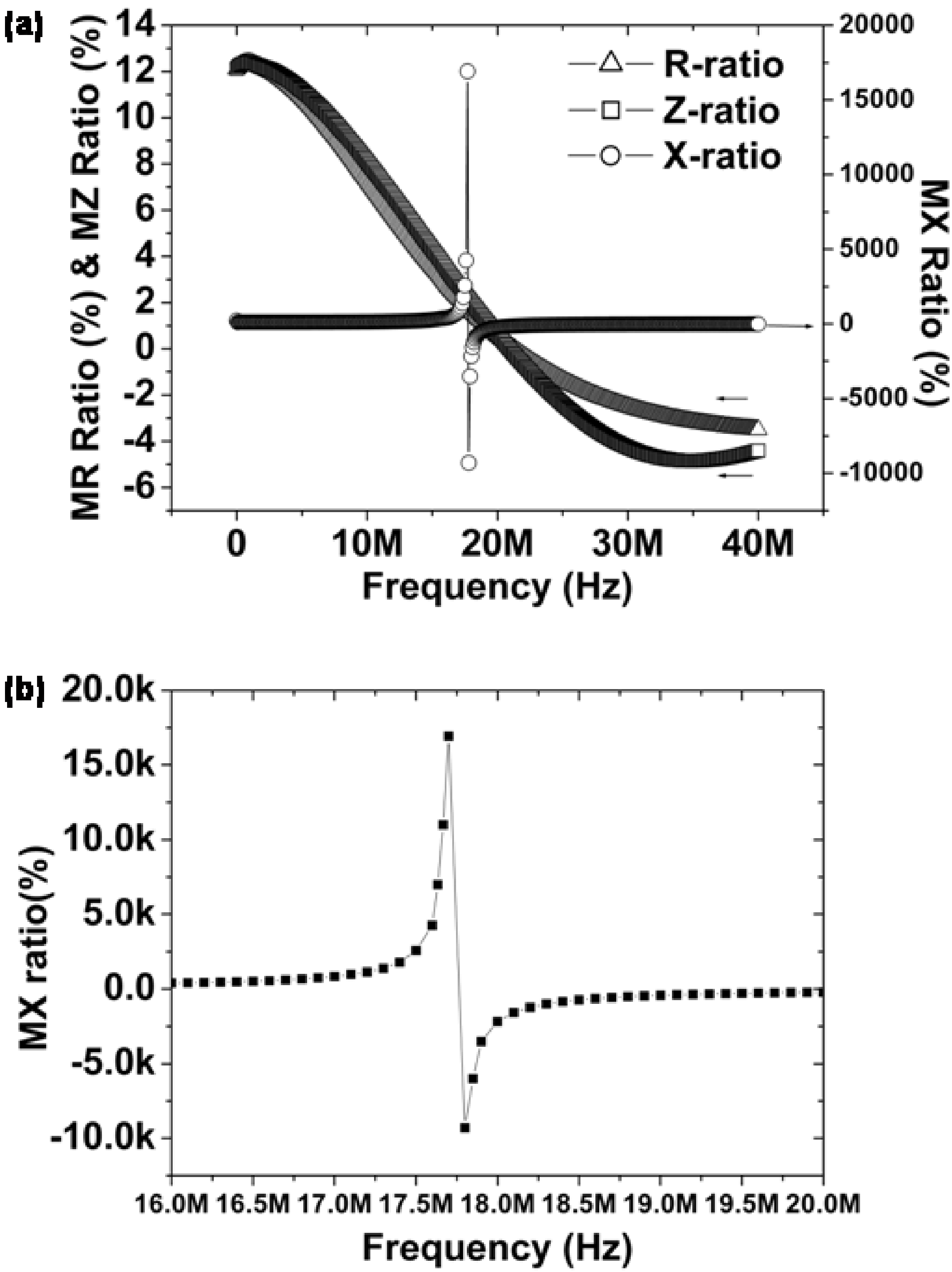


Fig. 4.4. (a) The frequency dependences of MR, MX, and MZ ratios. (b) The zoom in panel of the MX ratio changed; the frequency ranges from 16 to 20 MHz.

4.3.3 MR, MX, and MZ Ratios

The frequency dependences of the MZ, MR and MX ratios are shown in Fig. 4.4 (a). The ratios of MZ and MR at 100 Hz are close to 13%. As the frequency increases, the MZ and MR ratio decreases, approaching zero near 21.1 MHz. This is due to the difference between the parallel and anti-parallel states of Z and R being diminished as frequency increases. However, beyond the crossover frequency (21.1 MHz), the MZ and MR ratios change their signs and become negative values, as shown in Fig. 4.4 (a). The MX ratio shows a divergent behavior at the resonance frequency (17.7 MHz). The value of the MX ratio is small at frequencies father away from this resonance frequency, since the value of X_P is very close to zero and changes its sign at the resonance frequency. Therefore, a small change in X_{AP} would bring about a great change in the MX ratio (~ 17000% in the present sample). The MX ratio changes the sign near the resonance frequency as shown in Fig 4.4 (b).

4.3.4 Conclusion

In summary, the AC behavior in a magnetic tunneling junction has been studied. We observed a huge enhancement of magneto impedance and an inversed MZ loop in an MTJ system. The MTJ can be regarded as a combination of resistances ($R_{barrier}$, R_{int}, R_{wire}, R_{wire-1}), inductances (L_{wire}), and capacitances ($C_{barrier}$, C_{int}, C_{wire}), and equivalent circuit theory can be used to analysis the AC behaviors of this system. The vanishing-point of X_P was found near the resonance frequency f_r 17.7 MHz. The MX ratio changes its sign from negative at $f < f_r$ to positive at $f > f_r$ of the frequency dependence behavior. A huge change of more than ± 17,000% has been observed in the imaginary part of the impedance between the magnetically parallel and anti-parallel states of the MTJ. Furthermore, the inverse behavior of the magneto impedance loop occurs near 21.1 MHz, which is due to the crossover effect of the magneto capacitance between magnetically parallel and anti-parallel states. Our study suggests that MTJ is potentially a sensitive sensor for high frequencies.

4.4 Oscillating voltage dependence of high frequency impedance in Magnetic Tunneling Junctions

4.4.1 Oscillating Voltage Versus Effective Capacitance

Fig. 4.5 shows the resistance and capacitance reduced by barrier effect at parallel and anti-parallel states are functions of the V_{Os}. Obviously, the trends of the $R_{barrier}$ or $C_{barrier}$ at parallel and anti-parallel states are the same. However, the $R_{barrier}$ decreases as the V_{Os} increases and $C_{barrier}$ increases as the V_{Os} increases. With the V_{Os} increasing causes the electrons to get the higher energy over the barrier potential. Therefore, the $R_{barrier}$ decreases as the V_{Os} increases. The capacitance $C_{barrier}$ is inverse proportion to effective thickness of the barrier which is thin as $R_{barrier}$ is small. Therefore, the $R_{barrier}$ and $C_{barrier}$ have opposite results with increasing V_{Os}. Fig. 4.6 shows the resistance and capacitance reduced by interface effect at parallel and anti-parallel states to be functions of the V_{Os}. The trends of the R_{int} or C_{int} at

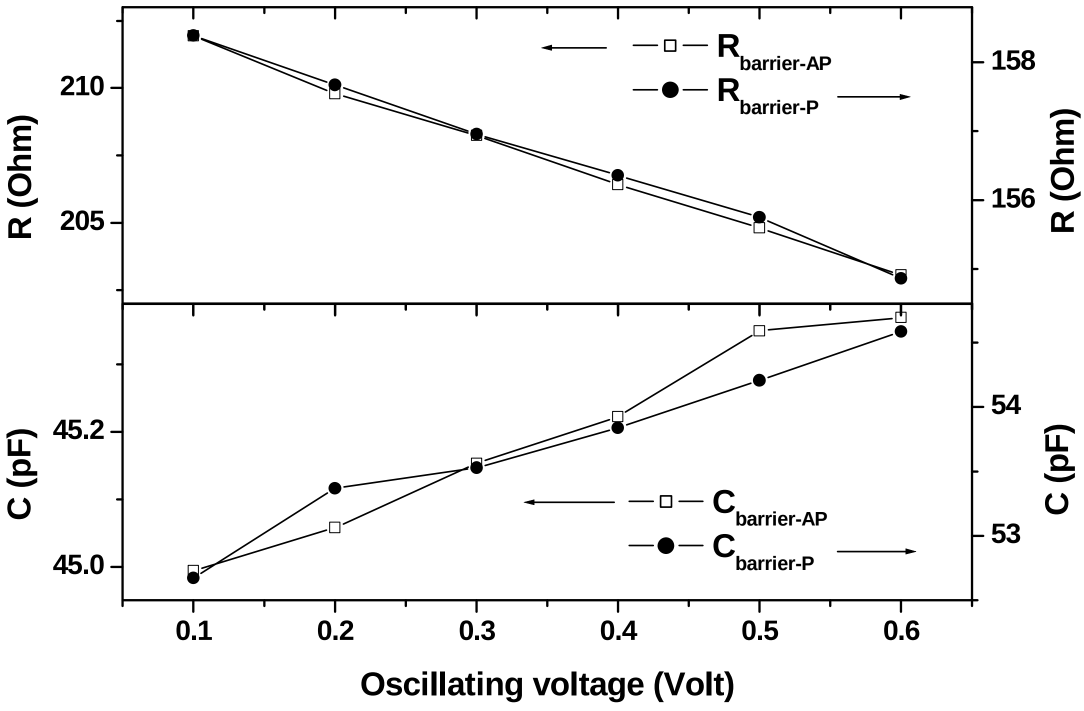


Fig. 4.5. The resistance and capacitance reduced by barrier effect at parallel and anti-parallel states are functions of the oscillating voltage.

parallel and anti-parallel states are similar as fig. 4.5. But the R_{int} increases as the V_{Os} increases and C_{int} decreases as the V_{Os} increases that the result is opposite to the barrier effect. The disorder and defects on the interface between metal and insulator are known with the ability to trap electrons. As the increasing of V_{Os}, the electrons become hard-trapped such that the capacitance effect of the interface part will decrease with the V_{Os} increases. According to the capacitance is inverse proportion to the resistance, the capacitance of the interface decreases cause the resistance of the interface increases with increasing V_{Os}.

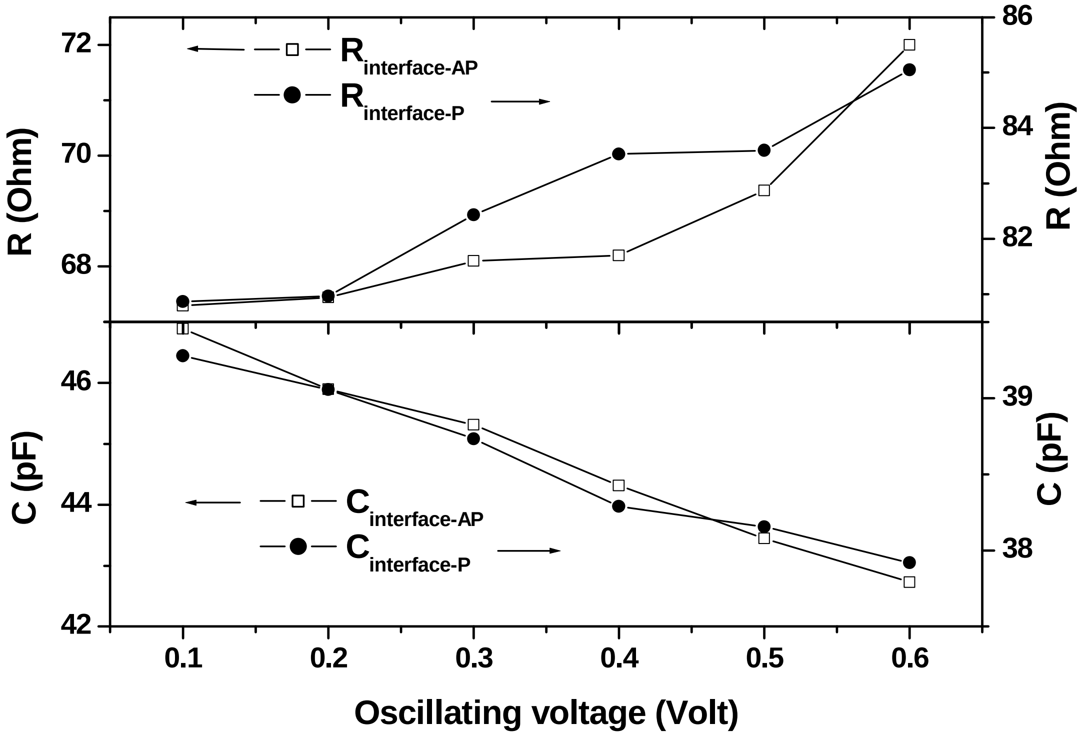


Fig. 4.6. The resistance and capacitance reduced by interface effect at parallel and anti-parallel states are functions of the oscillating voltage.

4.4.2 Oscillating Voltage Versus MI Ratio

Fig. 4.7 shows the frequency dependence of the MI ratio of the MTJ with different V_{Os} 0.1V, 0.2V, 0.3V, 0.4V, 0.5V, and 0.6V. At lower frequencies (below 22MHz), the MI ratio decreased gradually with increasing V_{Os} as shown in the inset panel in Fig. 4.7. This result accords with general cognition that the TMR ratio which is usually measured with DC circuit will decrease with DC bias increasing.

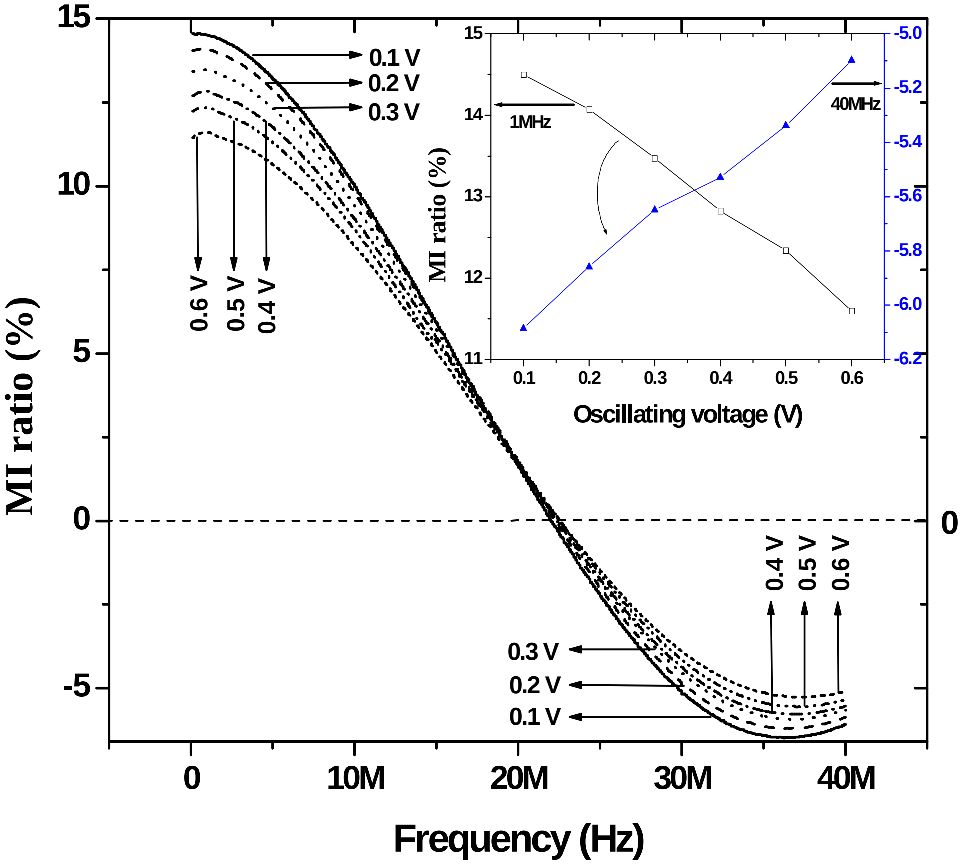


Fig. 4.7. The MI ratio of the MTJ with different oscillating voltage ranged from 100Hz to 40 MHz. The inset panel shows the MI ratio at 1MHz and 40MHz.

As disorder or defects in the tunnel barrier are known to increase the V_{Os} dependence through increased contribution from the spin independent parts of the two step tunneling or other spin flip processes [61]. When the frequency is over 22MHz (f_z), the MI ratio becomes negative from positive, which implied that the MI loop is reversed [51]. At higher frequency (over the f_z), the MI ratio increased gradually with increasing V_{Os} as shown in the inset panel in Fig. 4.7. This is due to the fact that the MI ratio is negative [51]. If using the absolute value of the MI ratio at high frequency, the result is the same as that in previous discussions.

4.4.3 Conclusion

In summary, the V_{Os} dependent of the magnetoimpedance effect of the magnetic tunneling junction has been studied. The MTJ can be regarded as a combination of resistances ($R_{barrier}$, R_{int}, R_{wire}, R_{wire-1}), inductances (L_{wire}), and capacitances ($C_{barrier}$, C_{int}, C_{wire}), and equivalent circuit theory can be used to analysis the barrier and interface behaviors of this system. We find the V_{Os} (AC bias) behavior of the MTJ that the behavior is similar to that of DC bias. The MI ratio decreases as V_{Os} increases. However, it is very interesting to find the MI ratio becomes negative at higher frequency. Consequently, our study is useful for MTJ characterization research and for MRAM fabrication.

4.5 Magneto impedance study in magneto tunneling junctions with different thickness of its barrier layer

4.5.1 Magneto Impedance Study for Different Barrier Thickness

The MTJ structures of Ru(5) /Cu(10) /Ru(5) /IrMn(10) /CoFeB(4) /Al (x)-oxide /CoFeB(4) /Ru(5) were deposited on Si/SiO wafers using the Magnetron Sputtering System, where all thicknesses are given in nm, with the junction area 6um x 6um. The thickness of the barrier layer Al-oxide is changed to 0.8, 1.1, and 1.2 nm.

Fig. 4.8 shows the hysterisis behavior of the MTJ with the barrier layer AlOx 0.8nm at the frequencies 100Hz and 40MHz, respectively. At low frequency 100Hz, the MR ratio is 3.08% that closes to the DC MR ratio 3.15%. At high frequency 40MHz, the both inverse MR ratio and MX ratio occurs [51]. Fig. 4.9 shows the frequency dependence of the real part of impedance (R_{AP}, R_P), and the imaginary part of impedance (X_{AP}, X_P) for the MTJ in the parallel and anti-parallel states. The R_{AP} and R_P curves decrease with increasing frequency, which indicates that the MTJ includes a significant capacitance effect as shown in Fig. 4.9(a), (c). Therefore, a Maxwell-Wagner (M-W) model capacitor consisting of dielectric material with the equivalent circuit (EC) theory could be used to analyze our sample. The EC consists of two parts, the MTJ and the sensing circuit as sketched in Fig. 4.1. In the MTJ part, the circuit contains not only the resistance ($R_{barrier}$) and capacitance ($C_{barrier}$) from

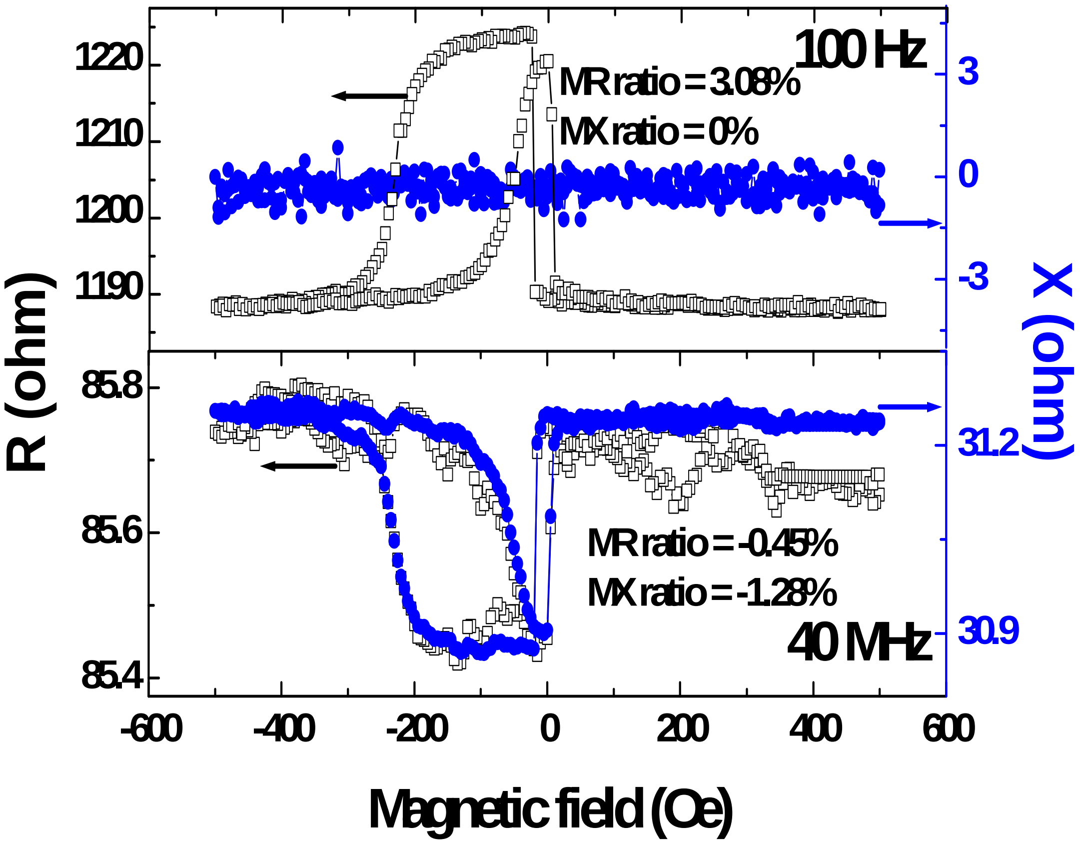


Fig. 4.8. It shows the hysteresis behavior of the MTJ Ru(5) /Cu(10) /Ru(5) /IrMn(10) /CoFeB(4) /Al (0.8)-oxide /CoFeB(4) /Ru(5) at frequencies 100Hz, and 40MHz, respectively.

the barrier but also has contributions from the interface, R_{int} and C_{int}, respectively. In the other part, the circuit components contain a resistor, a capacitor, and an ignorable inductor however, this part does not respond to the variation of the magnetic field. According to the EC theory, Z = $R_{eff} + iX_{eff}$ can be expressed as follows:

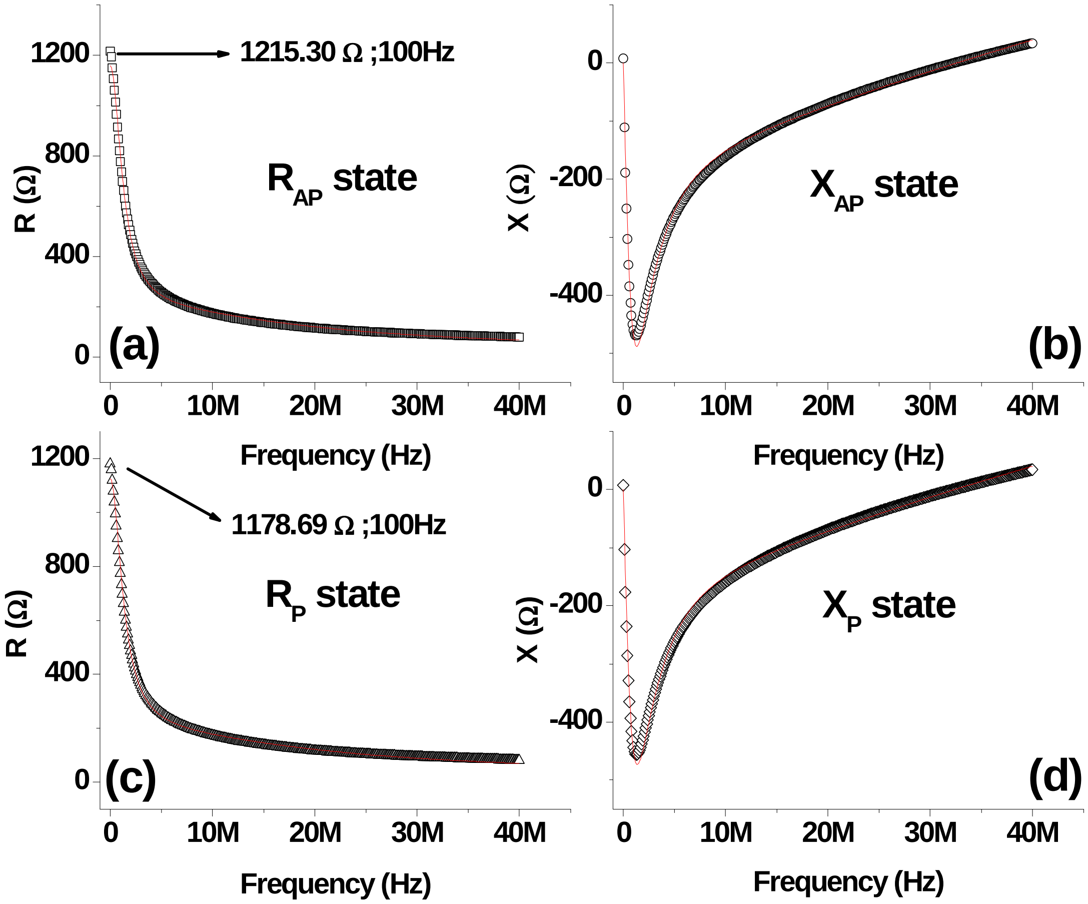


Fig. 4.9. The frequency dependences of the real part of the impedance (R) and the imaginary part of the impedance (X) for the magneto tunneling junctions in the anti-parallel (a), (b), and parallel states (c), (d).

$$R_{eff} = \mathrm{R_{barrier}} / \{[1 + (2\pi f\, \mathrm{C_{barrier}\, R_{barrier}})^2]\} + \mathrm{R_{int}} / \{[1 + (2\pi f\, \mathrm{C_{int}\, R_{int}})^2]\} + \mathrm{R_{wire}} + \mathrm{R_{wire\text{-}1}} / \{[1 + (2\pi f\, \mathrm{C_{wire}\, R_{wire\text{-}1}})^2]\} \quad (4.5.1)$$

$$X_{eff} = 2\pi f\, \{\mathrm{L_{wire}} - (\mathrm{C_{barrier}\, R_{barrier}}^2 / [1 + (2\pi f\, \mathrm{C_{barrier}\, R_{barrier}})^2] + \mathrm{C_{int}\, R_{int}}^2 / [1 + (2\pi f\, \mathrm{C_{int}\, R_{int}})^2] + \mathrm{C_{wire}\, R_{wire\text{-}1}}^2 / [1 + (2\pi f\, \mathrm{C_{wire} R_{wire\text{-}1}})^2]\} \quad (4.5.2)$$

The solid line (red line) of these equations as a function of frequency is displayed in Fig. 4.9, which shows good agreement with experimental results (dot). The simulated values of $\mathrm{R_{barrier}}$, $\mathrm{R_{int}}$, $\mathrm{C_{barrier}}$, and $\mathrm{C_{int}}$ in the parallel state are found to be 936.55 Ω, 154.94 Ω, 125 pF, and 47.1 pF, respectively, and those of $\mathrm{R_{barrier}}$, $\mathrm{R_{int}}$, $\mathrm{C_{barrier}}$, and $\mathrm{C_{int}}$ in the anti-parallel state are 964.95 Ω, 159.86 Ω, 126 pF, and 47.1 pF, respectively. The $\mathrm{R_{AP}}$ is the 1215.30 Ω at 100 Hz in anti-parallel state, and 1178.69 Ω at 100 Hz in parallel state as shown in Fig. 4.9(a), (c). It is obvious to see that the low frequency behavior is the same to DC behavior.

For the Fig. 4.10 (a)~(c), it demonstrates the frequency dependences of the MR, MX, and MI ratios at the barrier layer thickness 1.2nm, respectively. The ratios of MR and MI at 100 Hz are close to 13%. As the frequency increases, the MR and MI ratios decrease, approaching zero near 21.1 MHz. This is due to the difference between the parallel and anti-parallel states of R and Z being diminished as the frequency increases. However beyond the crossover frequency (21.1 MHz), the MR and MI ratios change their signs and become negative values, that mean the inverse hysterisis behaviors occurs as shown in Fig. 4.10(a), and (c). The MX ratio shows the divergent behavior at the resonance frequency ($\mathrm{F_r}$) 17.7 MHz as shown in Fig. 4.10(b). The value of the MX ratio is small at the frequencies farther away from this resonance frequency, since the value of $\mathrm{X_P}$ is very close to zero and changes its sign at the $\mathrm{F_r}$. Therefore, a small changes in $\mathrm{X_{AP}}$ would bring about a big change in the MX ratio (~17000%). For the Fig. 4.10 (d)~(f), it demonstrates the frequency dependences of the MR, MX, and MI ratios at the barrier layer thickness 1.1nm, respectively. The trend of the MX ratio is the same to the barrier layer thickness 1.2nm sample, but the F_r changes to 25.5 MHz as shown in Fig. 4.10(e). However, it is very interesting to notice the MR and MI behaviors of the barrier layer thickness 1.1nm sample as shown in Fig. 4.10(d), and (f). The value of the MR and MI ratios also decrease, approaching zero near crossover frequency 1.6 MHz, and change the sign beyond the crossover frequency.

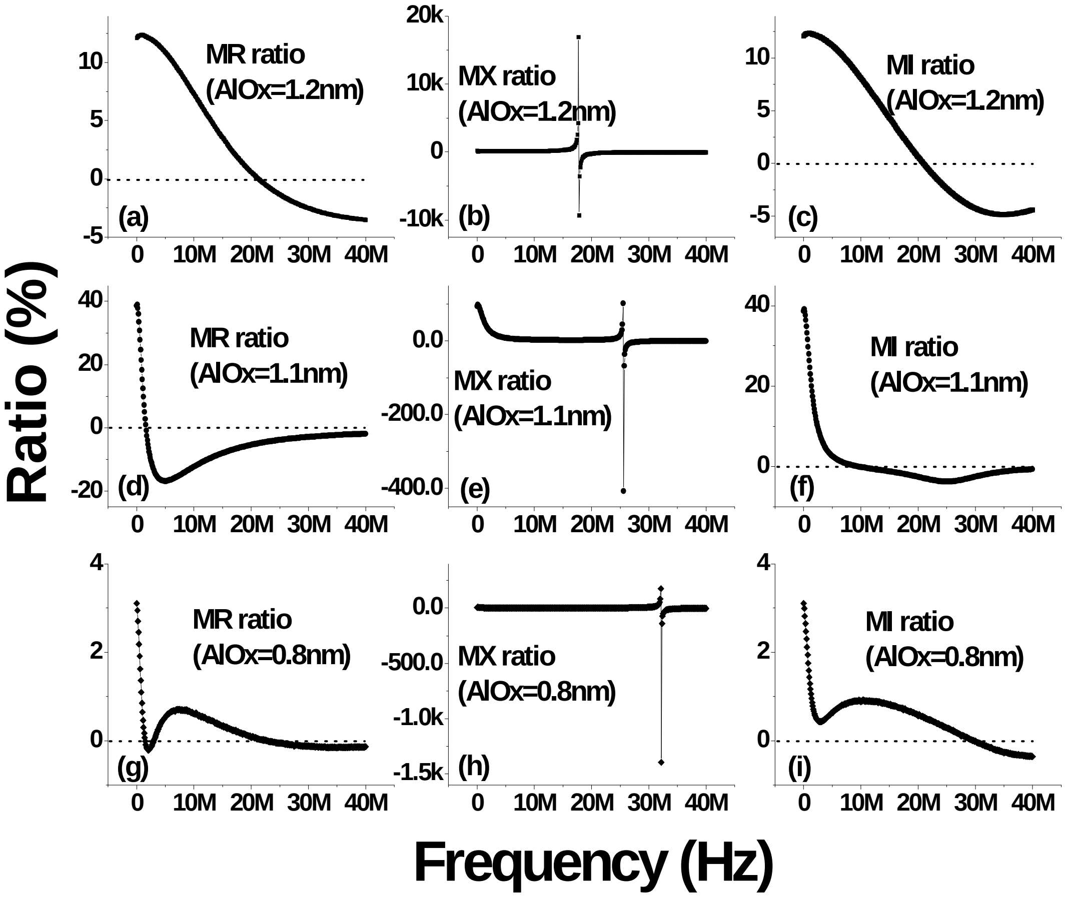


Fig. 4.10. shows the frequency dependence of the MR, MX, and MI ratio behaviors with different barrier layer AlOx thickness 0.8, 1.1, 1.2nm.

But at higher frequencies the MR and MI ratios change the trend, approaching the zero again as the frequency increases. In order to investigate these behaviors, we manufacture the thin barrier layer 0.8nm sample. It is obvious to find that the trend of the MX ratio behavior is equal to others sample as shown in Fig. 4.10(h). The F_r is 32.1 MHz. Furthermore; the Fig. 4.10(g) shows the trends of the MR and MI ratios are a little different to the barrier layer 1.1nm sample. The curve of MR ratio passes through the zero three times, which means that the there are three crossover frequencies in the barrier layer 0.8nm sample. The crossover frequencies are 1.5, 3, and 22.8 MHz, respectively. The trend of the MI ratio behavior is the same to MR ratio, but it just passes through the zero one time as shown in Fig. 4.10(i).

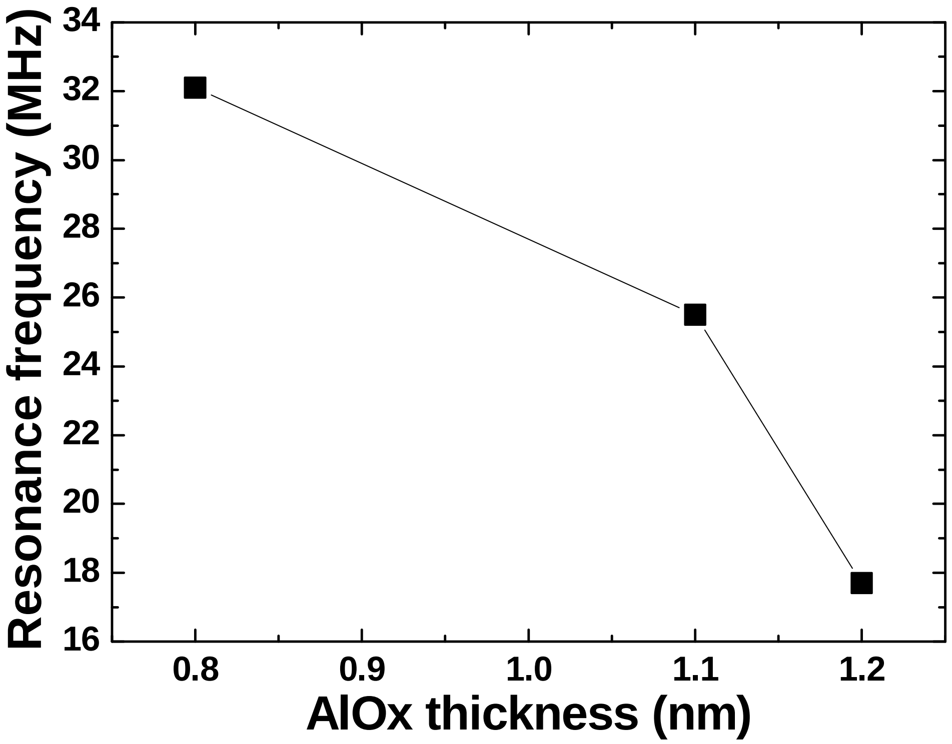


Fig. 4.11. The resonance frequency (F_r) of the MTJ is a function of the thickness of barrier layer.

The Fig. 4.11 shows the comparison with the resonance frequency (F_r) and the different barrier thickness 0.8, 1.1, and 1.2 nm. From the frequency dependence of the imaginary part of impedance ratio (MX ratio) for the MTJ, the F_r decreases from 32.1 to 25.5 and 17.7 MHz as the barrier thickness increases from 0.8 to 1.1 and 1.2 nm. Further, the roll-off frequency ($F_{roll\text{-}off}$) that defined as the minimum value of magneto impedance (Z) of the MTJ has been investigated. The $F_{roll\text{-}off}$ increases from 1.3 to 1.9 to 10.9 MHz as the barrier thickness increases from 0.8 to 1.1 and 1.2 nm. According to the effective capacitance calculation, $F_{roll\text{-}off}$ can be shown as:

$$F_{roll\text{-}off} = 1 / (2\pi R_{eff} C_{eff}) \qquad (4.5.3)$$

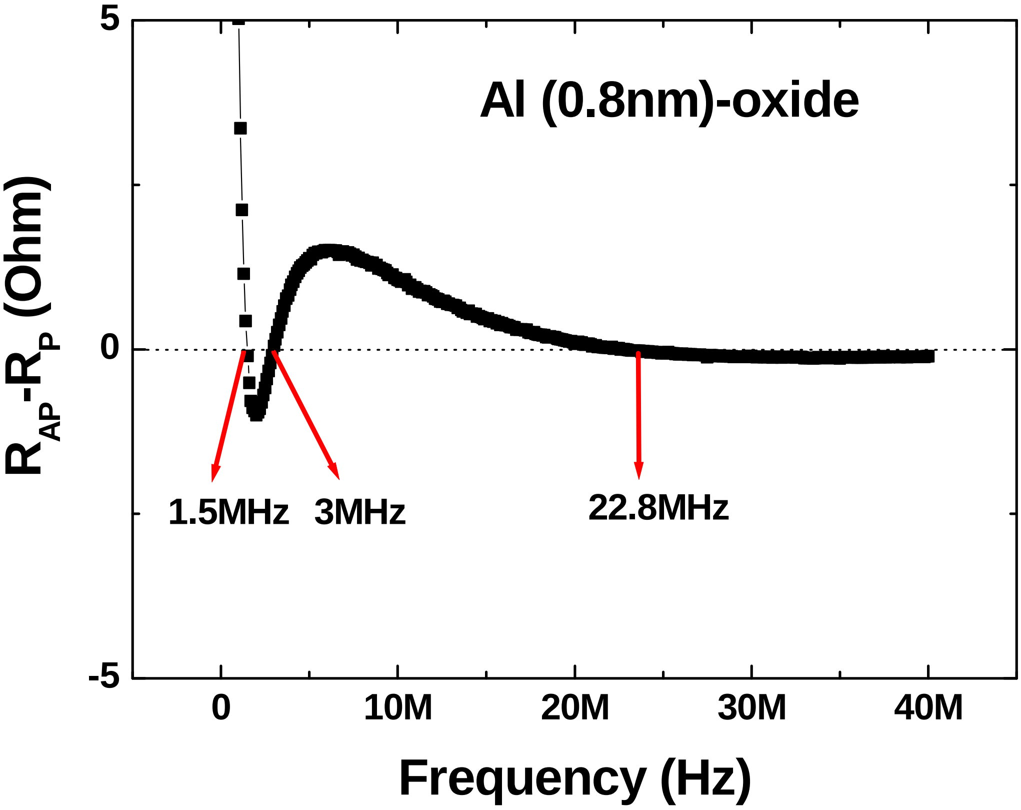


Fig. 4.12. The resistance difference between the anti-parallel state and the parallel state (R_{AP}-R_P) as a function of the frequency between 100Hz to 40MHz for sample with x = 0.8 nm.

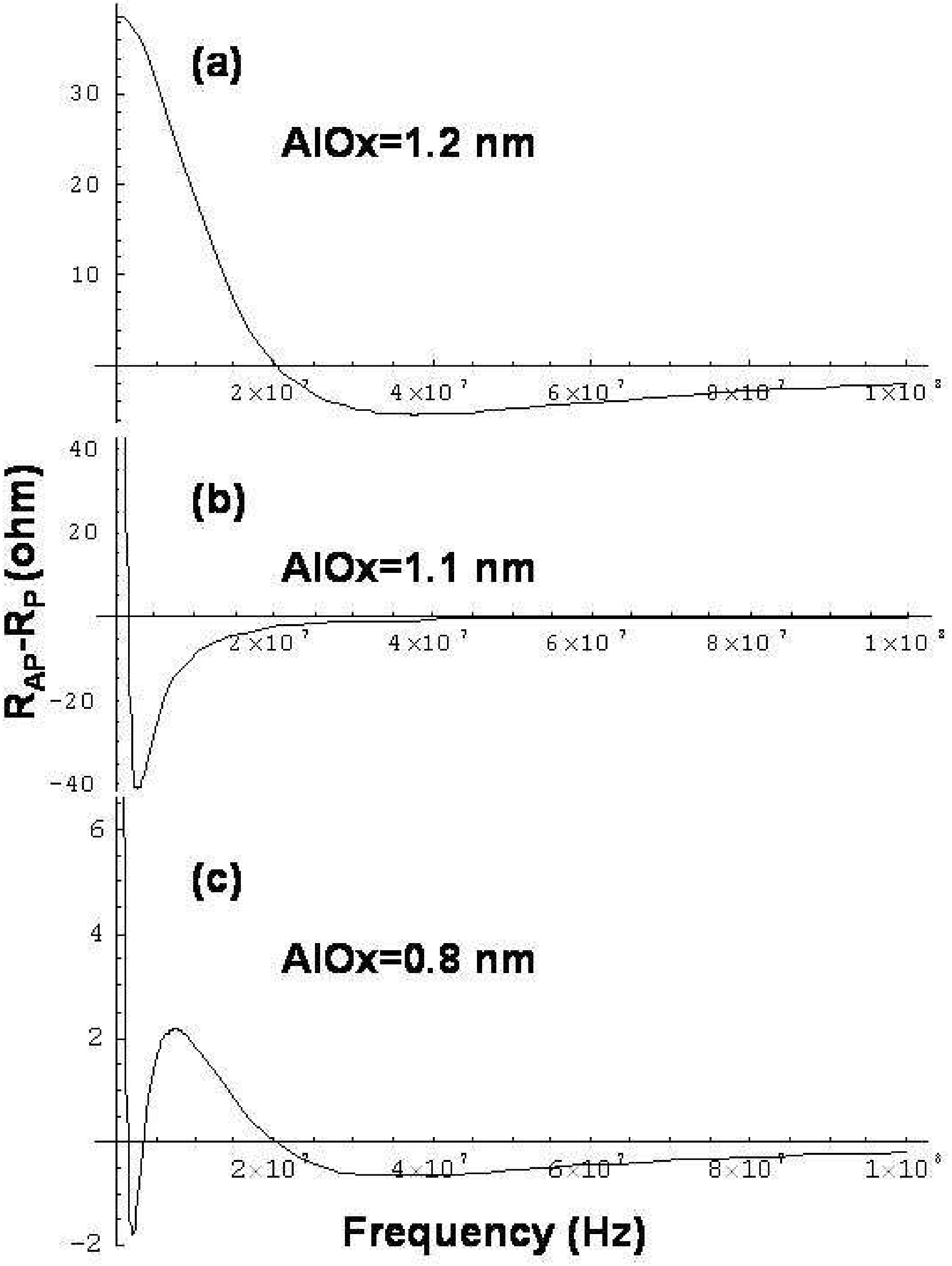


Fig. 4.13. Simulation results for R_{AP}-R_P with different barrier thickness 0.8, 1.1, and 1.2nm at the frequency ranging from 100Hz to 100MHz.

The effective capacitance is reverse proportion to the $F_{roll\text{-}off}$ and estimative values, and it varies from 184.9 to 168.81 and 64.1 pF as the barrier thickness increases from 0.8 to 1.1 and 1.2 nm, respectively. This means that the effective thickness of barrier increases which cause the effective capacitance decreases.

On closer inspection the relation between the values of the different of the real part of impedance R_{AP}-R_P and frequencies dependence ranging from 100Hz to 40MHz as shown in Fig. 4.12. Interestingly, it shows behaviors like a damping oscillating, and its amplitude decreases as frequency increases, which is quite consistent with the calculated value based on the Maxwell-Wagner model due to the reduction of the barrier thickness.

The simulation results following to Eq. (1) for R_{AP}-R_P with different barrier thickness 0.8, 1.1, and 1.2nm are demonstrated in Fig. 4.13. The driving frequency is simulated to high frequency 100MHz. All samples show the damping oscillating behaviors. For thin barrier thickness 0.8nm, it shows the obvious damping oscillating behavior corresponding to our experiment result as shown in Fig. 4.12. The depth physics for this oscillating behavior is still need to further study.

4.5.2 Conclusion

In summary, the AC behavior in a magnetic tunneling junction with different barrier layer thickness has been studied. The MTJ can be regarded as a combination of resistances ($R_{barrier}$, R_{int}, R_{wire}, $R_{wire\text{-}1}$) inductances (L_{wire}) and capacitances ($C_{barrier}$, C_{int}, C_{wire}), and equivalent circuit theory can be used to analysis the AC behaviors of this system. We observed a huge MX ratio at the resonance frequency, and it decreases from 32.1 to 25.5 and 17.7 MHz as the barrier thickness increases from 0.8 to 1.1 and 1.2 nm. We also found the inverse hysterisis behaviors due to the negative MR and MI ratio beyond the crossover frequency. For the thin barrier layer thickness, the trend of the frequency dependence of MR and MI ratio like a damping oscillating, and its amplitude decreases as frequency increases. The $F_{roll\text{-}off}$ increases as the barrier thickness increases, which means the effective capacitance decreases. Consequently, our study is useful for MTJ characterization research and for MRAM fabrication.

4.6 Summary

The magnetoimpedance effect was employed to study magnetotunneling junction (MTJ) with the structure of Ru(5 nm)/Cu(10 nm)/Ru(5 nm)/IrMn(10 nm)/CoFeB(4 nm)/Al2 O3/CoFeB(4 nm)/Ru(5 nm). A huge change of more than ±17 000% was observed in the imaginary part of the impedance between the magnetically parallel and antiparallel states of the MTJ. The inverse behavior of the magnetoimpedance (MI) loop occurs beyond 21.1 MHz; however, the normal MI at low frequency and the inverse MI at high frequency exhibit the same magnetization reversal as checked by the Kerr effect. The reversal in MI was due to the dominance of magnetocapacitance at high frequency.

Oscillating voltage (V_{Os}), which depends on the frequency dependence of the magnetoimpedance (MI) effect, was applied to study a magnetic tunneling junction (MTJ) at frequencies up to 40 MHz. The MI ratio decreased as the V_{Os} was increased. The MI ratio turned from positive to negative at a certain frequency. An equivalent circuit model was employed to analyze the results. The fact that MTJ can be regarded as the composition of a resistance component and two sets of parallel resistance (R) and capacitance (C) components in series has been utilized to describe the individual impedance contribution from the lead of cross pattern, barrier, and interface. The resistance ($R_{barrier}$) and capacitance ($C_{barrier}$) of the barrier effect are functions of V_{Os}. The $R_{barrier}$ decreases as the V_{Os} increases, However, $C_{barrier}$ behaves the opposite way. The tendency is for interfacial resistance $R_{interface}$ and interfacial capacitance $C_{interface}$ to have opposite results with increasing V_{Os}.

As the thickness of the barrier layer increases in the range of 0.8 to 1.2 nm, the F_r decreases from 32.1 to 17.7 MHz. The frequencies dependence of the MR and MI ratio show the damping oscillating behavior at thin barrier layer. The effective capacitance decreases as the barrier layer thickness increases. This work provides a detail investigation of frequency behavior with different barrier layer thickness, especially useful for MTJs characterization.

CHAPTER 5

WO_X RRAM Using Down Stream Plasma Oxidation

5.1 Introduction

Recently, resistance-based memory has attracted much attention for high-density applications because of its small cell size, simple structure, high speed, low power consumption, and potential for 3D stacking [62]. WO_X based RRAM requires only one extra mask, no new equipment and no new material from the standard CMOS process and is thus especially attractive [63]. In addition, WO_X devices have demonstrated the possibility for MLC operation [64]. However, past efforts had very little margin because the R-V curves were very steep and provided no operational plateau. We have improved the WO_X process significantly and thus have achieved an R-V curve with extended linear range. This has increased the resistance and voltage window by ~ 10X, thus allowing stable MLC operation.

In other region, memory with unipolar operation using a diode isolation device is an ideal way to achieve 3D high-density storage. However, data retention for unipolar operation of metal oxide RRAM is far worse than Flash memories and their cycling endurance is < 100 cycles [65-67]. Recently, we reported a self-aligned, graded oxidation WO_x RRAM that shows excellent performance and reliability under bipolar operation conditions. The characteristics of the WO_x RRAM suggest that the LRS and HRS are caused by different ability of hopping conduction behavior [63]. Previously, it was suggested that Joule heating effect may play a role for the unipolar switching of RRAM, noting the high current density passing through the interface [68]. However, no direct evidence for unipolar switching mechanism of the WO_x-based RRAM is understood up to now. In order to reduce the design complexity, we further improved the operation and process of the graded oxidation

WO_X.device.

5.2 Device Fabrication

Fig. 5.1 shows the cell structure and cross sectional TEM image of graded WO_X based resistive memory. The fabrication process flow was approximately the same as previously reported [63,64] but we have shrunk the plug from 0.5um to 0.17um and refined the W CMP and other processes. The down stream plasma oxidation was done in a mixture of nitrogen and oxygen at 265°C, for 1600s.

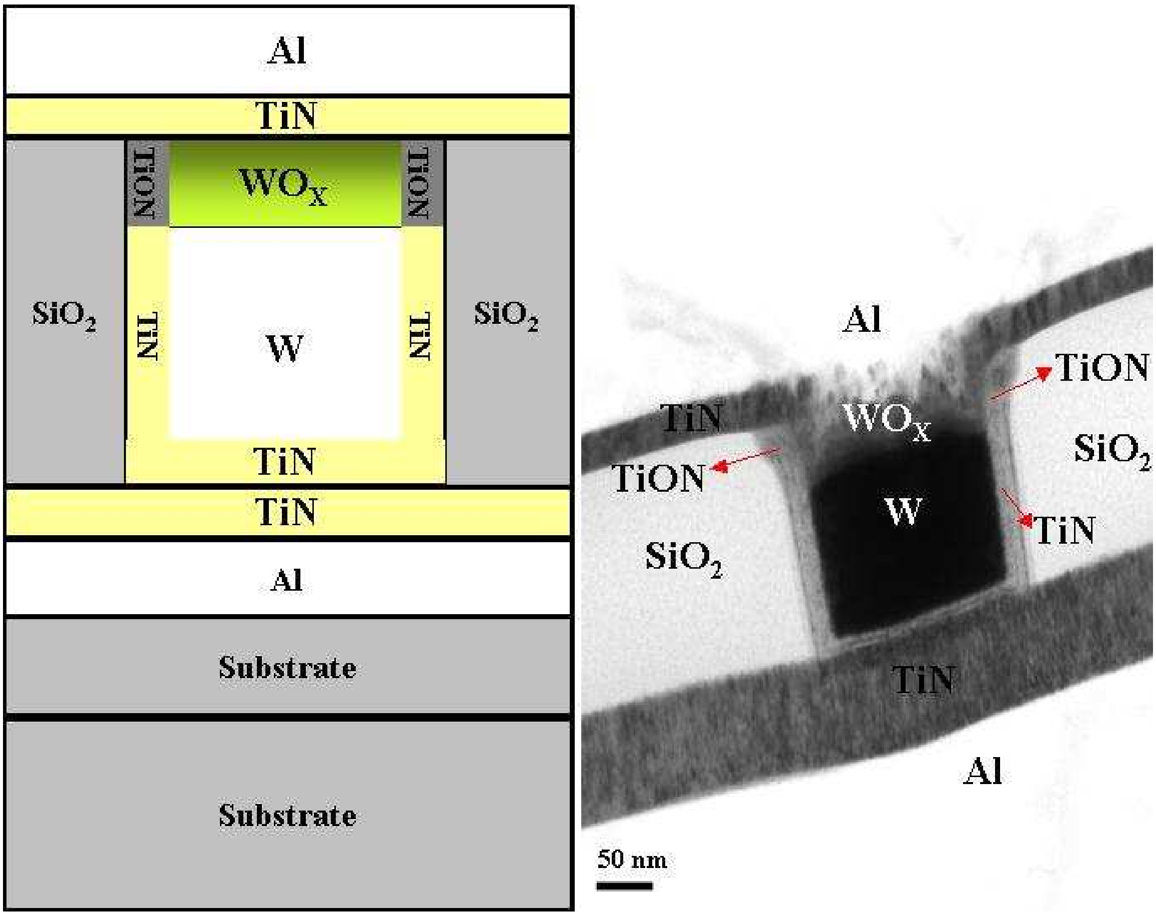


Fig. 5.1. Cell structure, cross-sectional TEM image and the process flow of the WO_X RRAM

5.3 Bipolar Switching Characteristics for Self-Aligned DSPO WO_x Resistance RAM (R-RAM) with Multi-Level Operation

5.3.1 Cell Operation

A modest forming step (4V 50ns) is used to reduce the programming voltage [69]. Before the forming step, relatively high voltage is needed to reset the device, but after the forming process the reset voltage is reduced (Fig. 5.2). The hysteresis loop after the forming step is shown in Fig. 5.3. The resistance is increased by applying a positive voltage, and is decreased by applying a negative voltage.

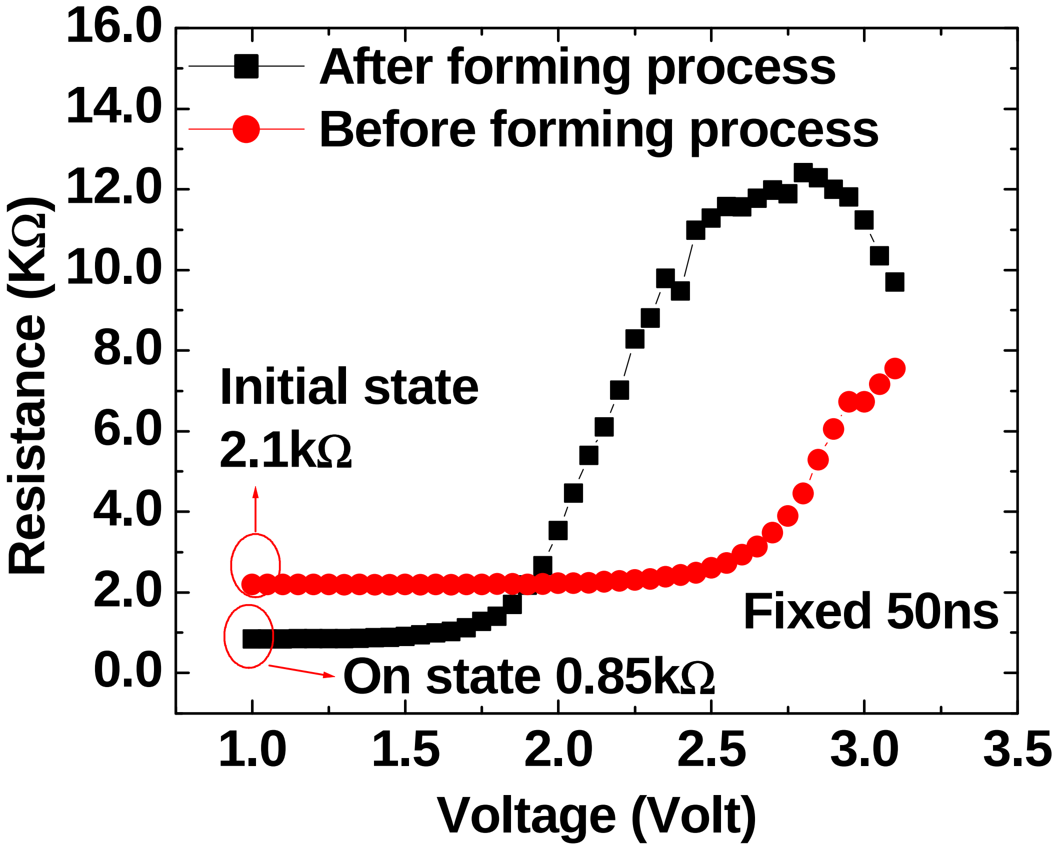


Fig. 5.2. R-V characteristics using fixed pulse width (50ns) before and after forming process. A forming process helps reducing the RESET voltage.

Fig. 5.4 shows the readout resistance at different programming voltages at 85°C. It is interesting to note that between 1.5V and 3V the resistance increases smoothly and linearly with the applied voltage both at room temperature and at 85°C. This represents an ideal characteristic for multi-level operation. Fig. 5.5 shows the operation algorithm used to achieve MLC. A simple verification routine helped achieving more than 1,000 cycles of P/E in 4 level MLC operation, as shown in Fig. 5.6. Fig. 5.7 shows distributions for 100 cells in four well-separated levels. Fig. 5.8 shows 8 distinguished levels after 40 cycles that show promise for 3-bit/cell storage if total window can be enlarged.

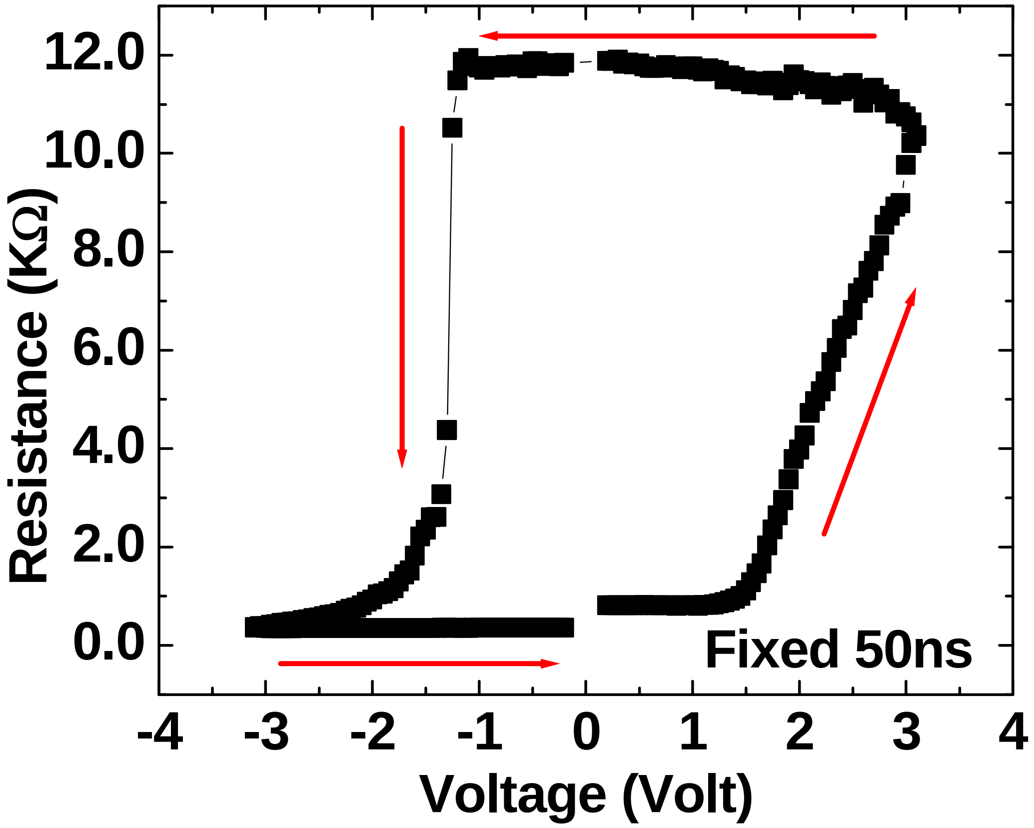


Fig. 5.3. Hysteresis loop between 3V and –3V with a fixed pulse width of 50ns. The resistance increases gradually and linearly from 1.5V to ~3V, but decreases suddenly at –1.2V.

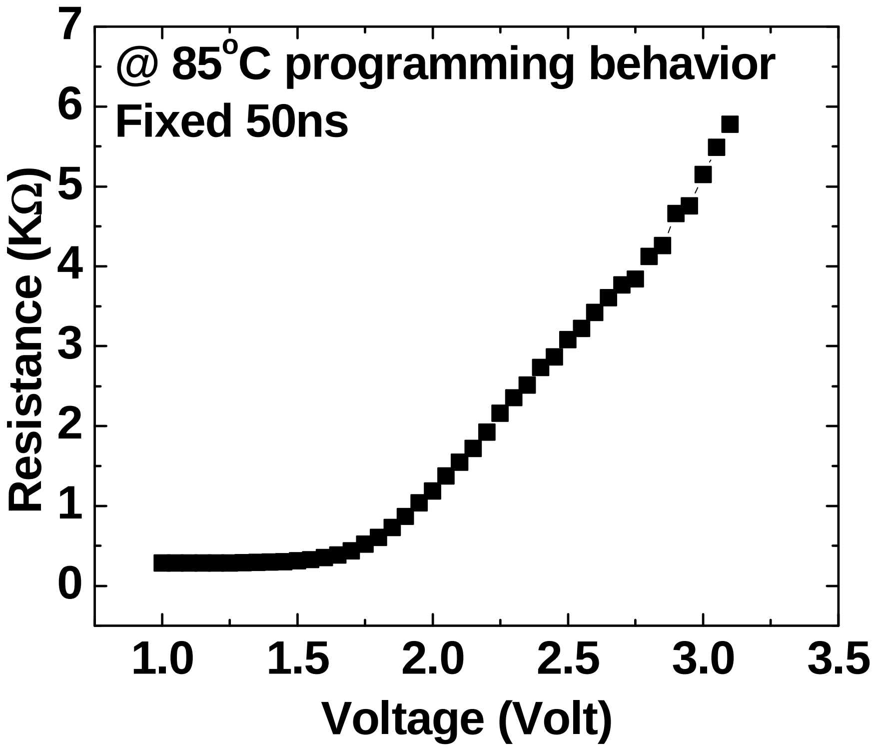


Fig.5.4. Resistance dependence on pulse voltage with fixed pulse width 50ns at 85°C. It again shows a well behaved linear region suitable for MLC programming.

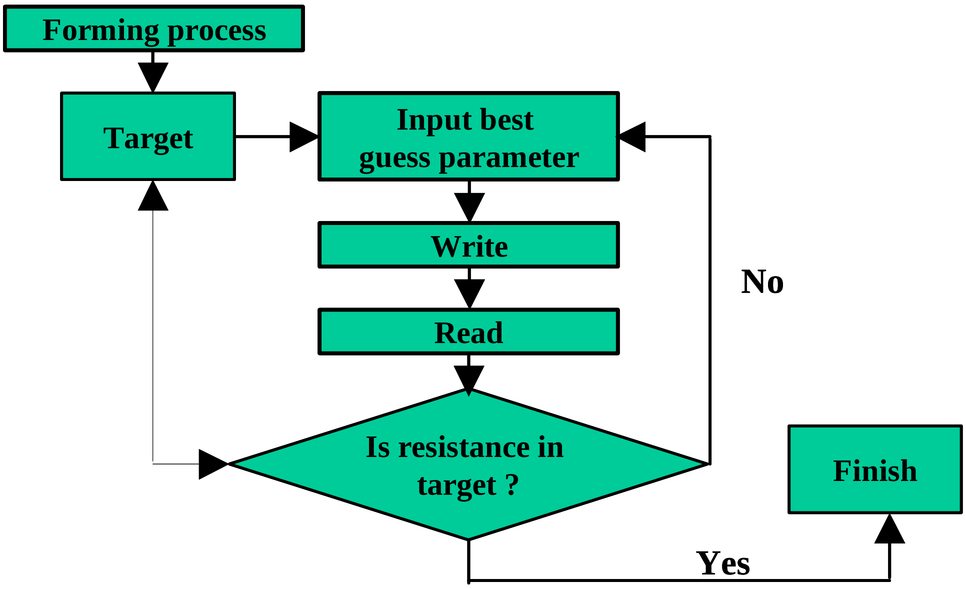


Fig. 5.5. The MLC operation algorithm. Two operation methods may be selected to control the resistance states of the WO_X RRAM: (1) varying the pulses voltage, (2) changing the pulse number. R-V plots (Fig. 4) are used to decide the initial parameters. If the resistance does not reach the target value, the programming voltage is increased.

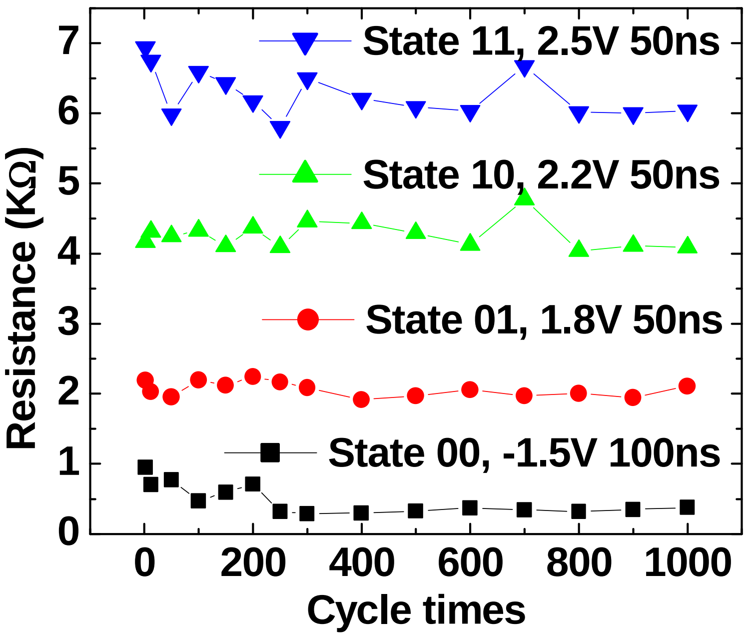


Fig. 5.6. 4-level cycling test of the WOx RRAM. 1,000 cycles are achieved. 3 RESET states (01,10,11) are programmed by different voltage positive pulses and the SET level (00) is programmed by a negative pulse.

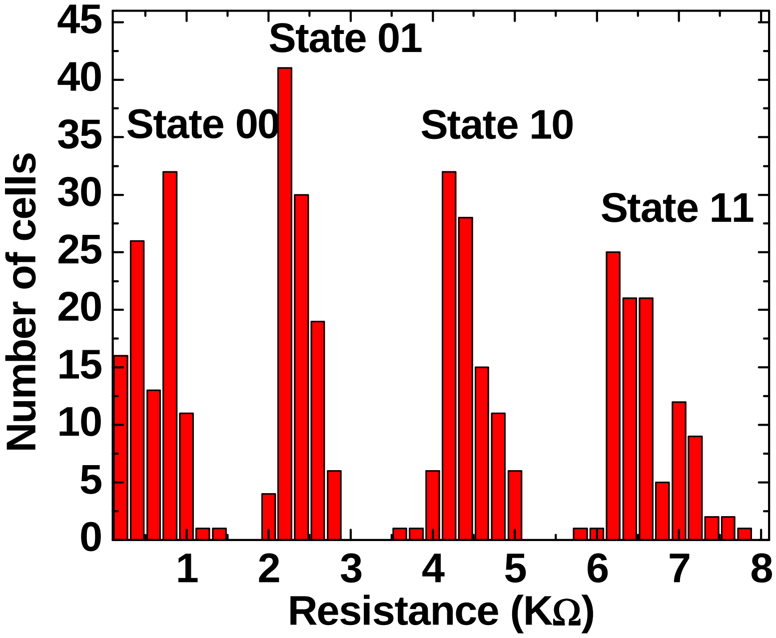


Fig. 5.7. 100 cells are programmed into 4 levels using the same programming conditions in Fig. 5.6. The levels are well distinguished.

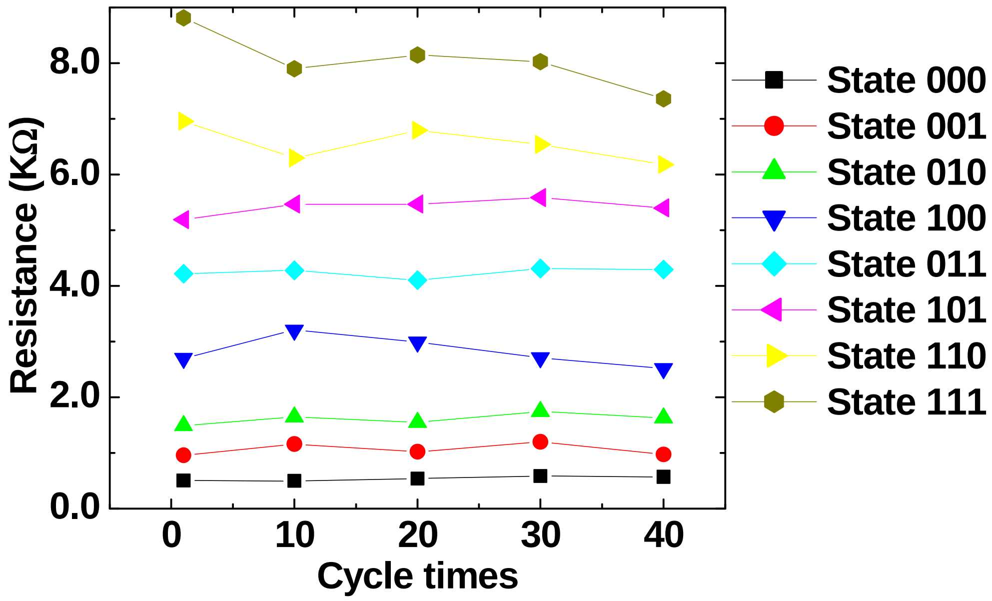


Fig. 5.8. Cycling test for 8 levels. Although there was no window closing after cycling, the window between adjacent logic levels is too narrow. For 3-bit/cell operation the total window needs to be further enlarged.

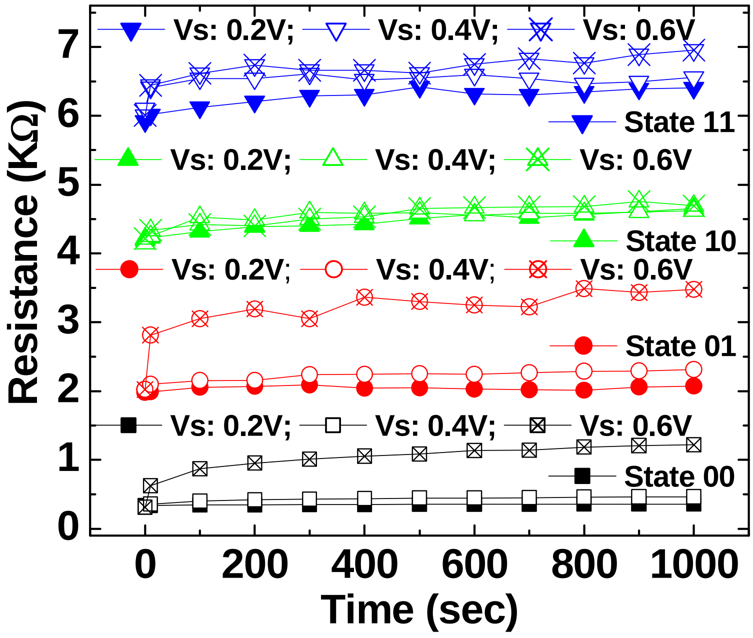


Fig. 5.9. Read disturb test for WO_X RRAM. The states 10, and 11 are not affected by the read bias ranging from 0.2V to 0.6V. The states 00, and 01 are immune to read disturb under 0.4V.

5.3.2 Device Reliability

Fig. 5.9 shows the read disturb behavior for applied voltages from 0.2V to 0.6V for all 4 states. The devices are immune to read disturb up to about 0.4V, adequate for all applications. The temperature dependence of resistance is shown in Fig. 5.10. High resistance states show significant temperature dependence while the low resistance state (00) is relatively insensitive to temperature. Below 100°C the four MLC levels are clearly separated. Although strong temperature dependence is undesirable, yet our results are well behaved and controllable and thus still leave sufficient margin for circuit design.

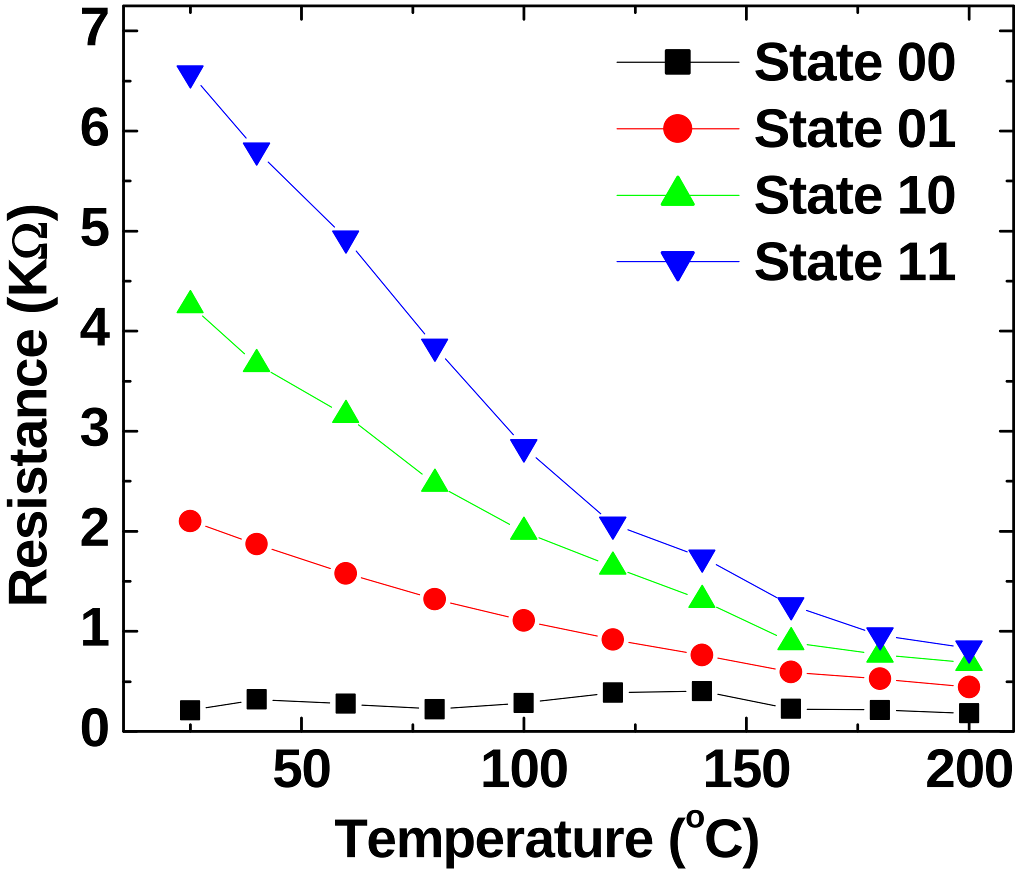


Fig. 5.10. Device resistance dependence on temperature from 25 to 200°C. The resistances of RESET states 01, 10, and 11 decrease with increasing temperature. The strong temperature dependence may limit application range.

Fig. 5.11 shows activation energies for higher resistance states 01, 10, and 11. Activation energies are not constant and tend to increase at higher temperature, as in previous literature [70]. Figs. 5.12 and 5.13 show data retention at room temperature and at 85^{o}C, respectively. At 85^{o}C the resistance window is reduced after heating but all states are stable with reasonable windows between levels. The original room temperature resistances for all states were restored after cooling down. Fig. 5.14 shows the excellent thermal stability for all MLC states at 150^{o}C. The resistance of state 00 increased slowly while the states 10, 01, and 11 remained almost constant. A 2k resistance window was maintained throughout the baking.

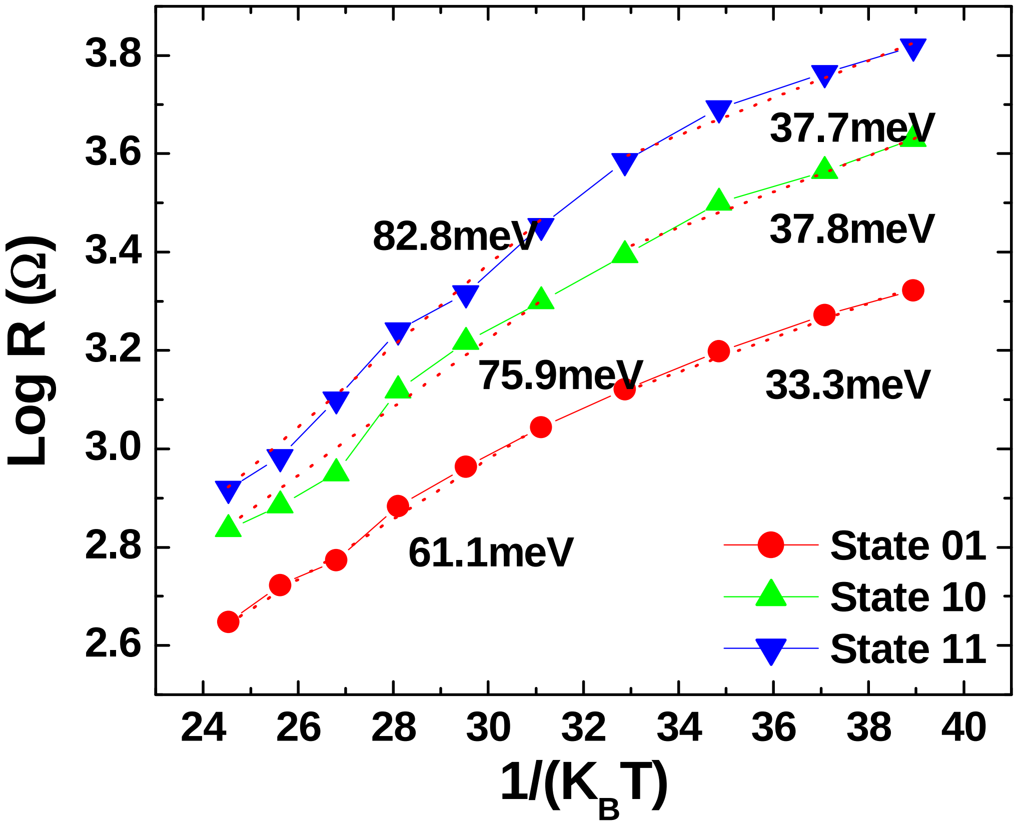


Fig. 5.11. The log R vs. 1/k_BT plot for states 01, 10, and 11. The activation energies are not constant but are similar for all states.

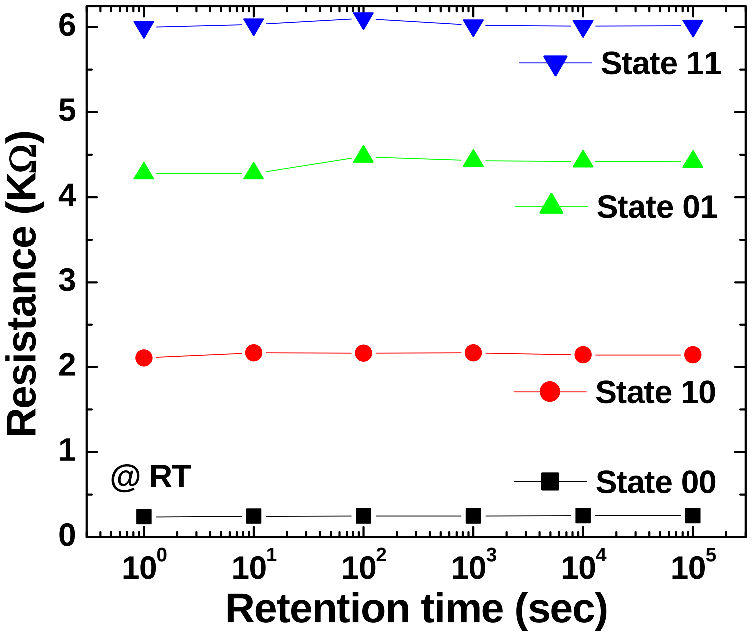


Fig. 5.12. Resistance stability of the WO$_X$ RRAM at room temperature. All 4 states show stable resistance.

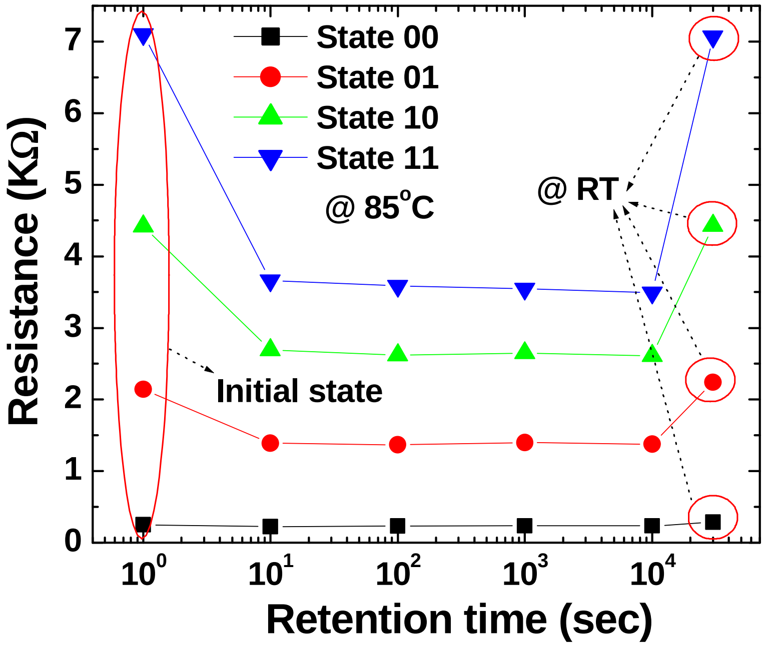


Fig. 5.13. The resistance stability at 85°C. The high resistance states maintain > 1kΩ of window after stressing.

5.3.3 Conclusion

By improving the characteristics of our WO_X device we have demonstrated stable MLC operation of 2-bit/cell (4 levels) RRAM. The reliability of the MLC operation has been examined in detail, showing good data retention, excellent thermal stability and so far the best cycling endurance reported for MLC operation. This work is the first demonstration of a promising MLC operation for RRAM.

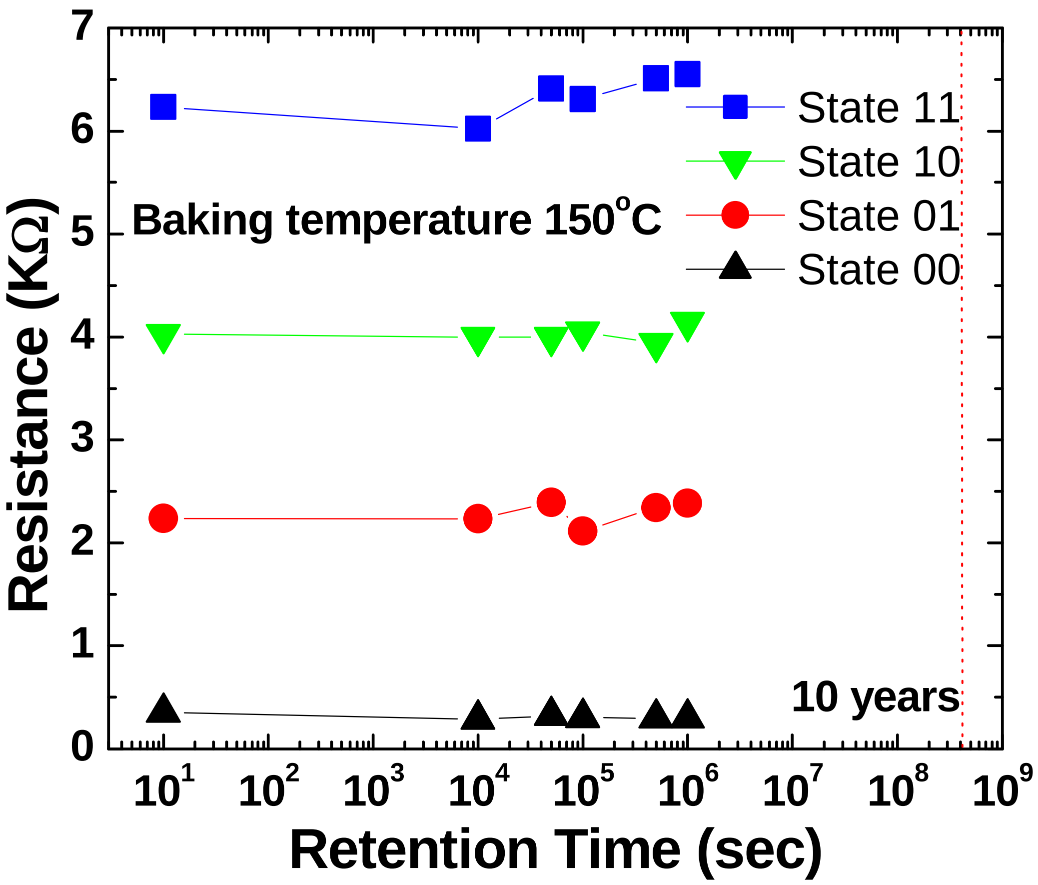


Fig. 5.14. Thermal stability test for WO_X RRAM at 150°C. Each state survives well beyond 106 sec.

5.4 Unipolar Switching Characteristics for Self-Aligned DSPO WO_x Resistance RAM (R-RAM)

5.4.1 Sample Preparation and Analysis

Fig. 5.15 shows the schematic process flow of a self aligned WO_x RRAM. The top surface of the W plug in a via after CMP is oxidized by downstream plasma oxidation for 1600s in a mixture of nitrogen and oxygen at 265℃. Only one added mask is required to remove the WO_X from the W plugs outside of the memory array. A standard metal TiN/AlCu/TiN stack is then deposited directly on top as the top electrode (TE).

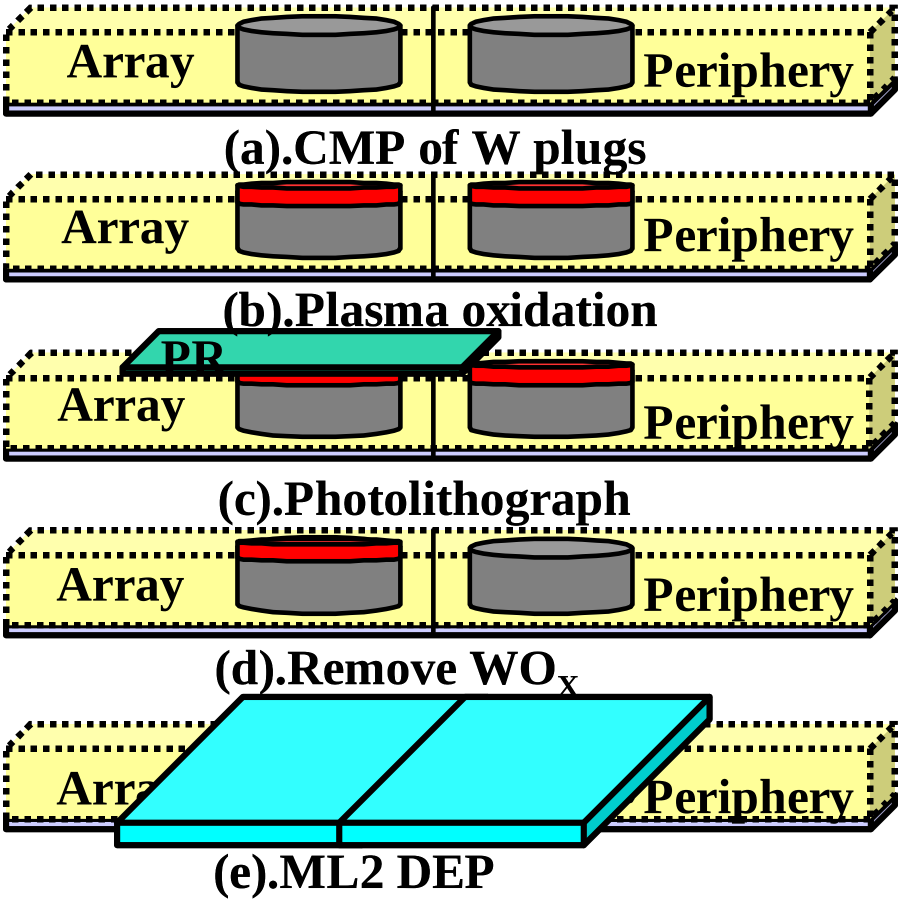


Fig. 5.15. Major processes for self-aligned WO_X RRAM: (a) CMP of W plugs, (b) plasma oxidation, (c) photolithography to expose peripheral circuits, (d) remove WO_X from W plugs in periphery, (e) top electrode deposition and patterning.

Fig. 5.16 shows the TEM image of the WO_x layer. Fig. 5.17 shows the binding energy change in XPS analysis. It shows that the tungsten oxide is composed of various valences of the WO_x and its structure is graded. Fig. 5.18 shows the WO_x thickness as a function of oxidation time. The total thickness of WO_x increases slowly with oxidation time, the composition of WO_x evolves with oxidation time. Fig. 5.19 shows that after 400s of oxidation, only the surface becomes WO_3 while after 1600s of oxidation the WO_3 layer penetrates into the bulk of the oxide layer.

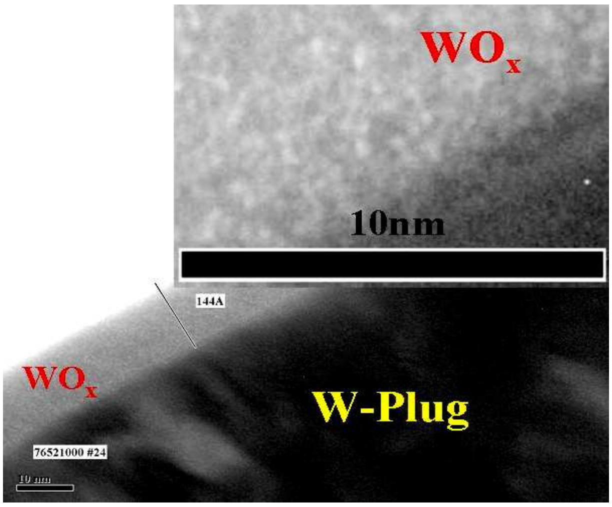


Fig. 5.16. Cross-sectional TEM for the WO_X RRAM cell. HR-TEM (inset) shows that the WO_X is amorphous.

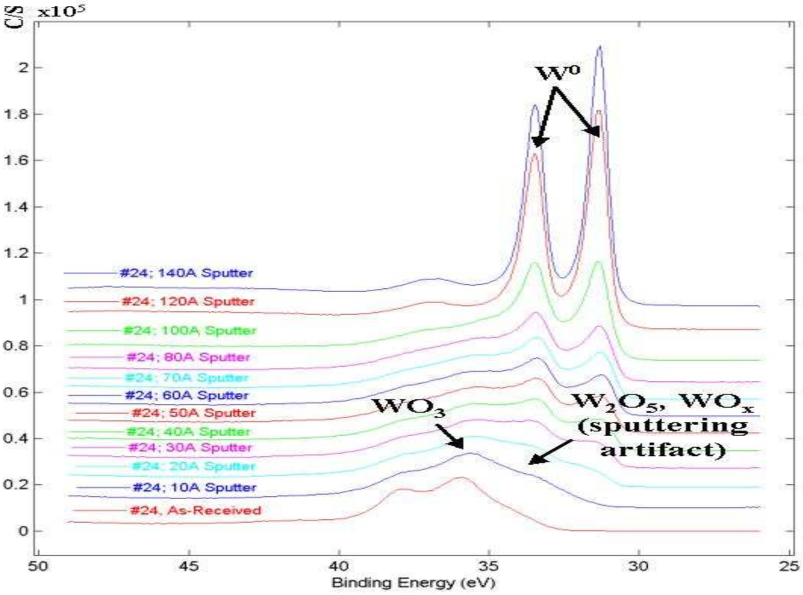


Fig.5.17 XPS spectra for WO_X fabricated by 1600s of oxidation. The film thickness is about 140Å.

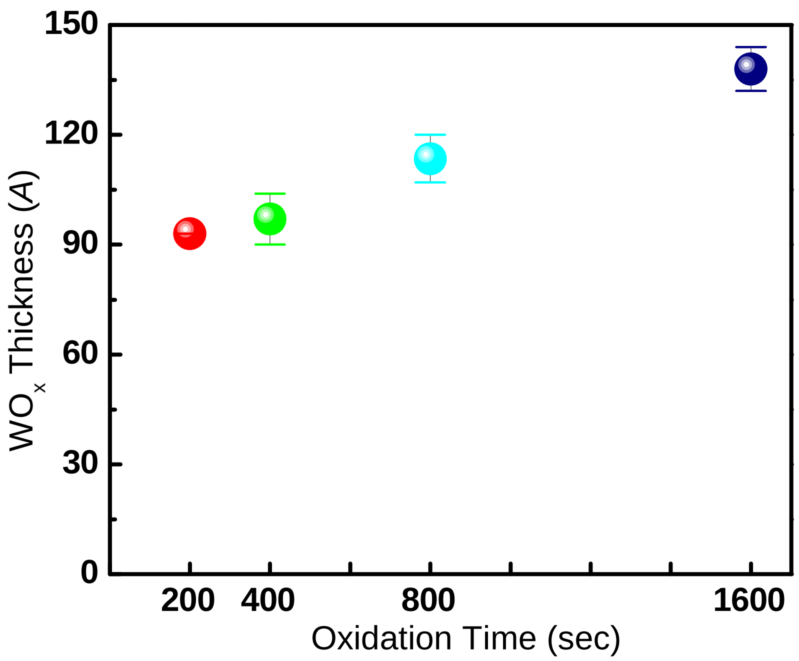


Fig. 5.18 Thickness of WO_X film as a function of oxidation time. The film thickness increases slowly after a fast initial growth. However, the film composition varies considerably with the oxidation time.

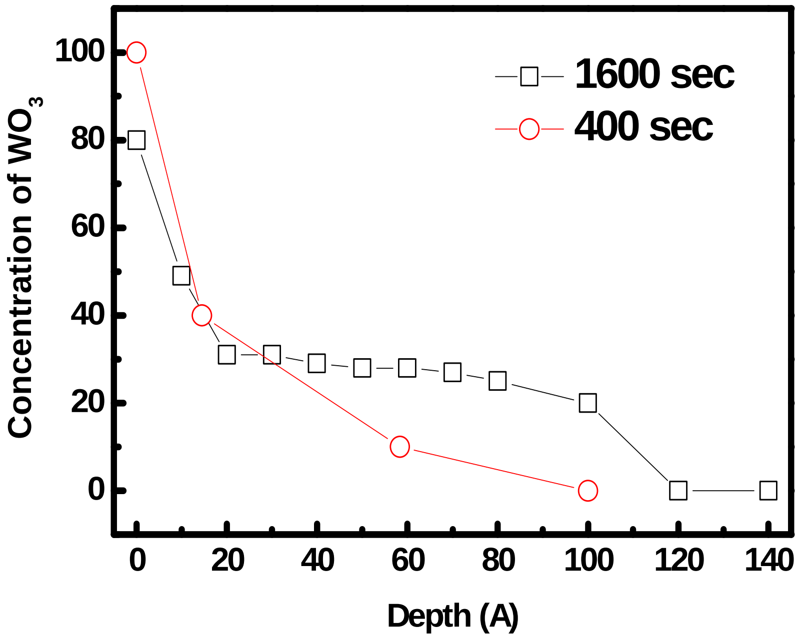


Fig. 5.19 Comparison of WO_X composition after short (400s) and long (1600s) oxidation. The 400s oxidation produces steeply graded WO_3 suitable for bipolar switching (Ref. 4). After 1600s of oxidation, the WO_3 penetrates through the oxide and film is suitable for unipolar switching (See Fig. 5.21).

5.4.2 Unpolar Switching Characteristics

Fig. 5.20 shows the initial switching behavior when a positive voltage is applied to the top electrode for various oxidation times. The ratio between HRS and LRS increases significantly as the oxidation time increases. Therefore, longer oxidation time is recommended for unipolar operation.

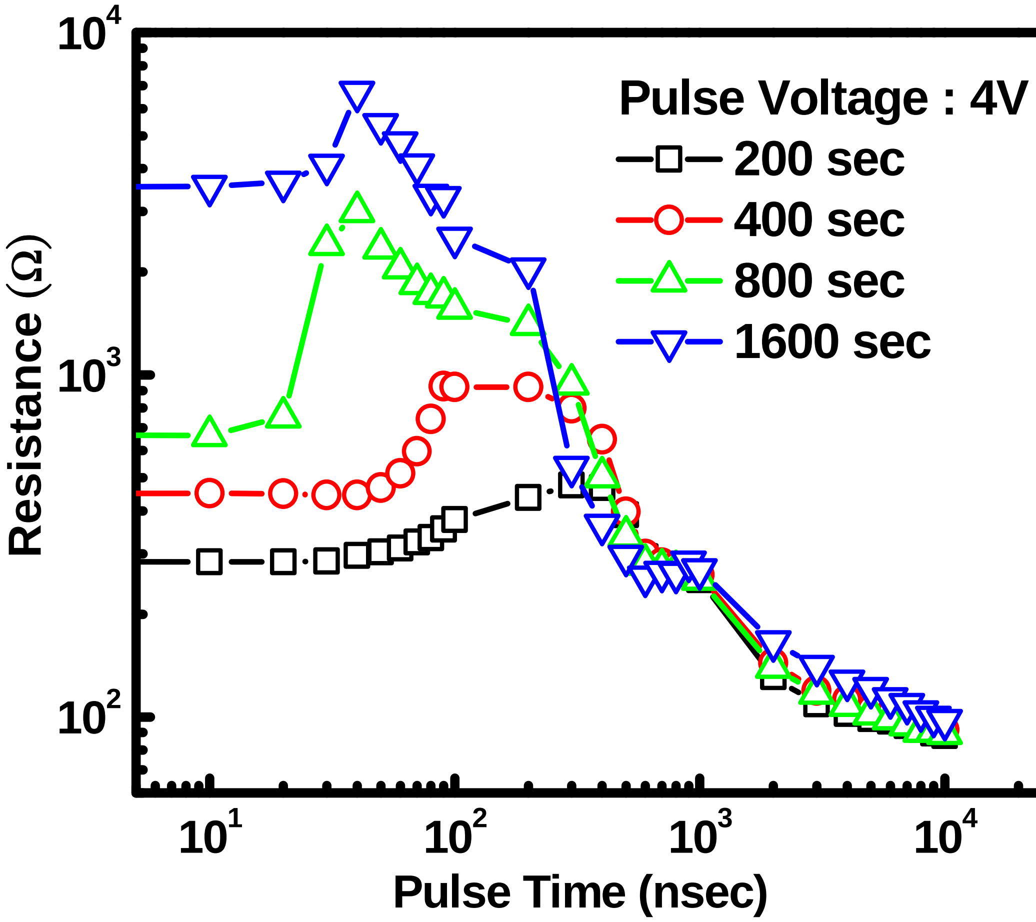


Fig. 5.20 Unipolar switching for fresh devices with various oxidation time. Short oxidation time gives poor unipolar switching capability, while long oxidation time produces films with good unipolar switching property.

Fig. 5.21 shows the switching behavior of 1600s WO_x from LRS to HRS and back to low resistivity state (LRS) by 3.3V unipolar pulses. Short pulses (20-50ns) increase the resistivity while longer pulses (200-500ns) decrease the resistivity. Fig. 5.22 shows the resistivity change when negative voltage pulses are applied to the top electrode. Although resistivity decreases after short pulses, it does not recover once switched. The temperature dependence of LRS and HRS states are shown in Fig. 5.23. The conductivity for both the LRS and HRS increases as temperature increases.

Fig. 5.23 is well described by the Fermi-Dirac distribution function for semiconductor $f(E)=1/\{1+exp[(E_C-E_F)/KT]\}\sim exp[-(E_C-E_F)/KT]$. This suggests that both LRS and HRS of the WOx RRAM obtained by unipolar switching are semiconducting in nature.

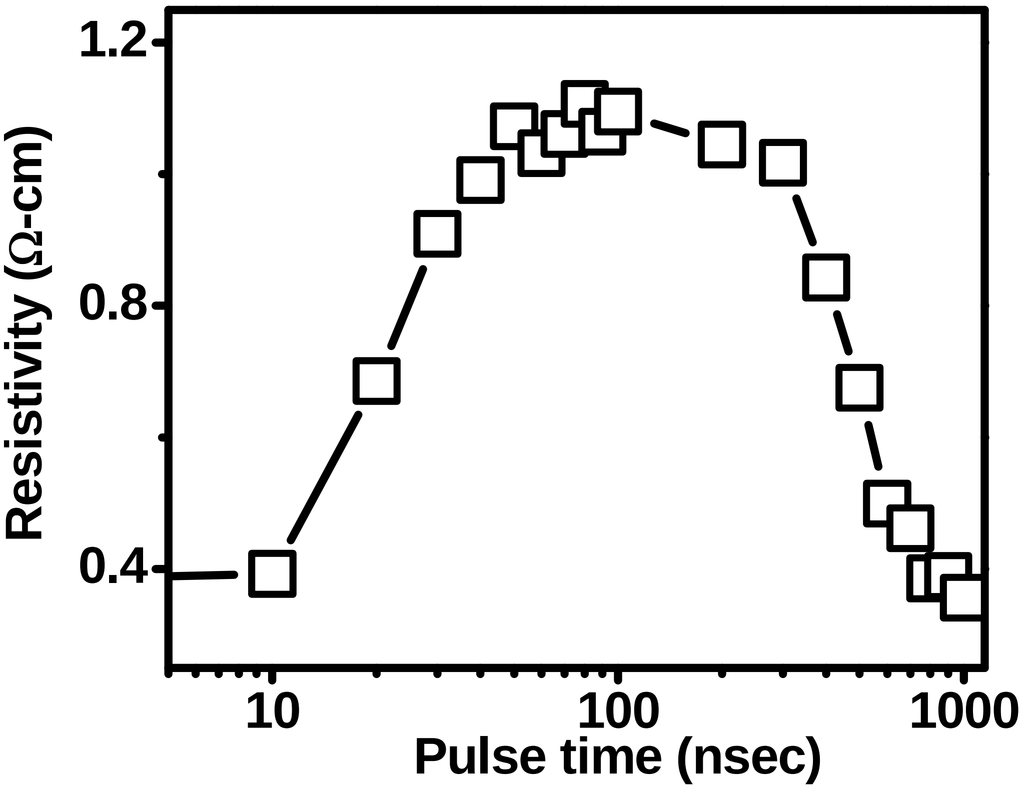


Fig. 5.21 Unipolar switching characteristics of a 1600s device. A short (20-50ns) positive pulse switches the resistivity from LRS to HRS, while long positive pulses (200-500ns) switch the resistivity from HRS back to LRS. Both operations are fully reversible.

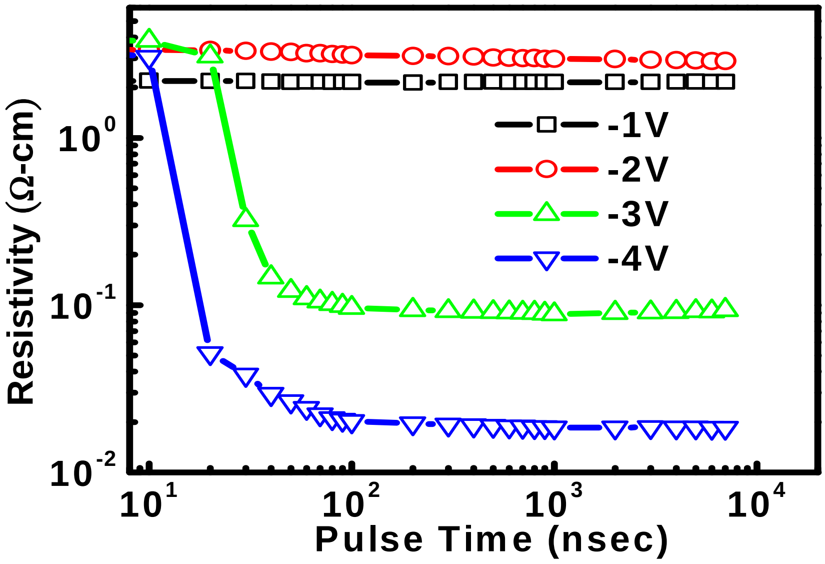


Fig. 5.22 Negative pulses, however, do not produce reversible unipolar switching on 1600s samples. At higher voltages, negative pulses can switch the WO$_X$ device from HRS to LRS once, but the device cannot be switched back to HRS anymore.

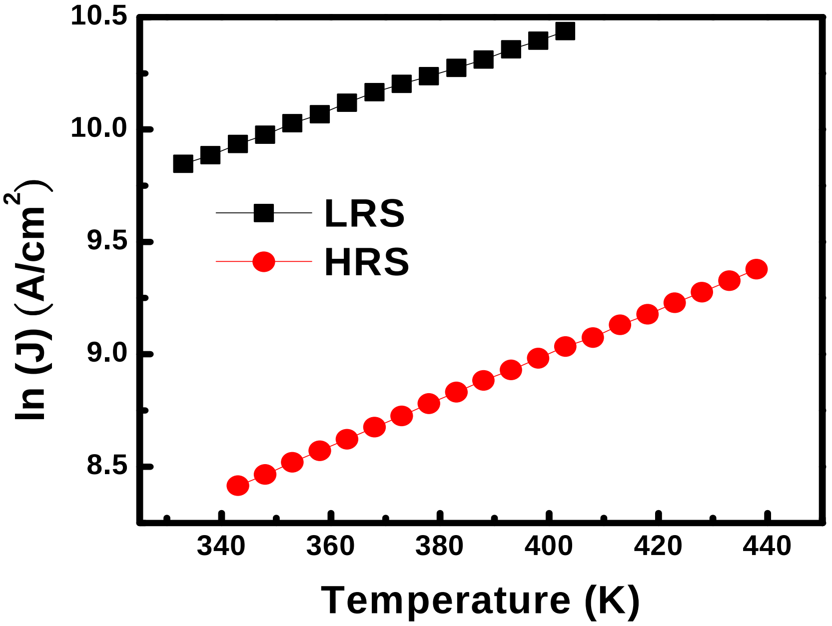


Fig. 5.23 Temperature dependence of the conduction currents for both the LRS and HRS indicating semiconducting behavior.

5.4.3 Device Reliability

Fig. 5.24 shows more than a thousand times cycling endurance with 10X resistance window. The RESET (LRS to HRS) condition is 3.3V, 20nsec and SET condition (HRS to LRS) is 3.3V, 500nsec. Fig. 5.25 shows excellent thermal stability at 150℃ over 2500 hours. Although there is an initial resistance drop, the resistivity decreases only slightly with time afterward. Fig. 5.26 shows the read disturb behavior between 0.2 to 0.6 V of applied voltage for both LRS and HRS. The HRS shows essentially no disturb and the LRS shows good immunity to read disturb up to 0.4V. These are by far the best performance and reliability demonstration for any unipolar resistance memory.

5.4.4 Conclusion

By engineering the WO$_x$ film and using variable pulse duration, we demonstrate a highly reliable WO$_x$ RRAM. This new device is promising for post-Flash era scaling of NVM and 3D storage.

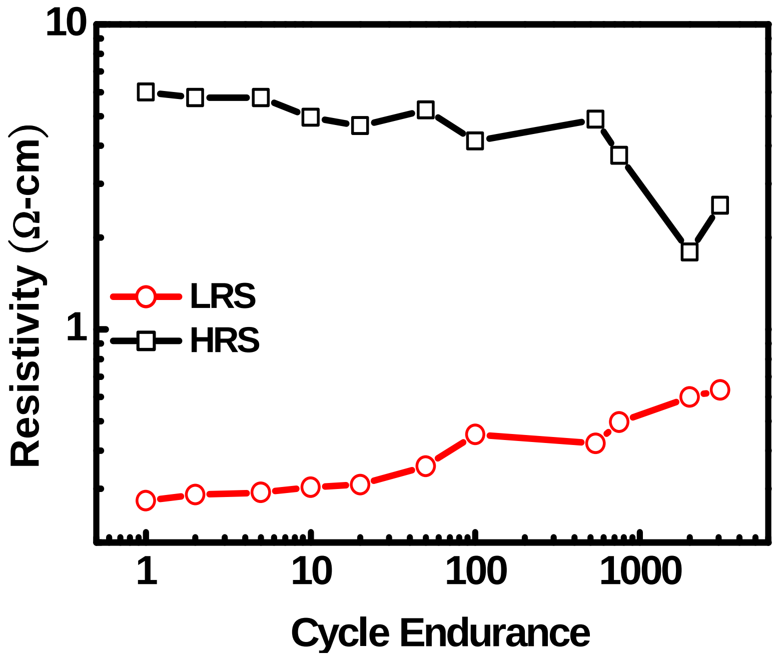


Fig. 5.24 Cycling characteristics of the WO$_X$ memory cell. RHS/LHS resistance window keeps well separated up to > 1000 cycles.

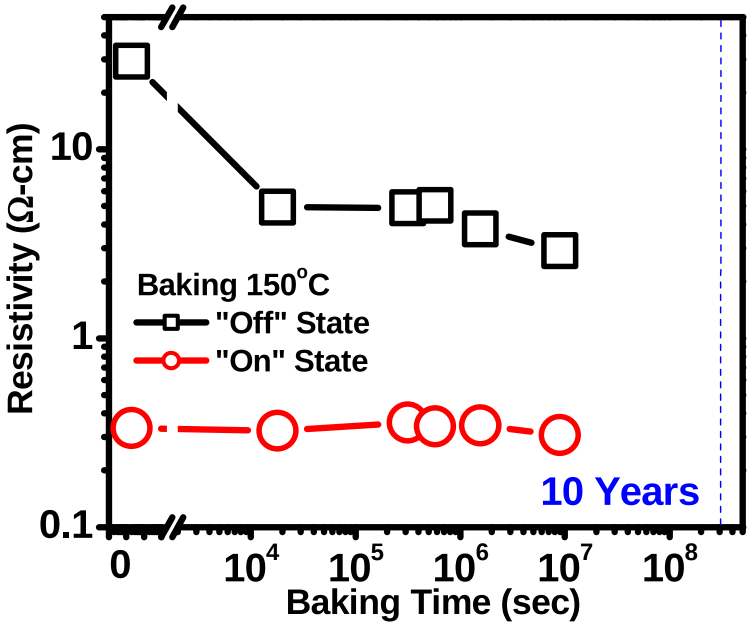


Fig. 5.25 Thermal stability test of WO$_X$ memory cell at 150^{0}C. The HRS decreases slowly while the LRS keeps almost constant. A 10X resistivity ratio is maintained up to 2500 hours of baking.

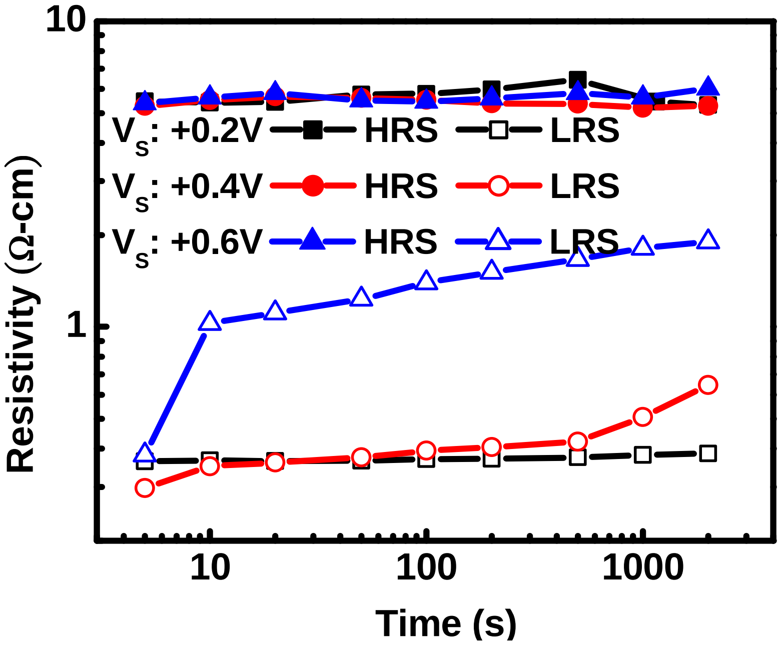


Fig. 5.26 Read disturb test on WO$_X$ devices. The HRS is not affected by the read bias of 0.2-0.6V. LRS is immune to read disturb under bias < 0.4V.

5.5 Summary

Both bipolar and unipolar operations for WO_X resistance memory with good performance and reliability are demonstrated. For bipolar operation, it demonstrated stable MLC operation of 2-bit/cell (4 levels) RRAM. The reliability of the MLC operation has been examined in detail, showing good data retention, excellent thermal stability and so far the best cycling endurance reported for MLC operation. For unipolar operation, a short (20-50ns) positive pulse switches the WOx film from low resistance state (LRS) to high resistance state (HRS), while a longer (200-500ns) positive pulse switches the film from HRS to LRS. Negative pulses, on the other hand, do not produce reversible resistivity changes. Despite the low energy switching, both LRS and HRS are very stable, capable of withstanding 2,500 hours of baking at up to 150^{o}C. Furthermore, the WOx R-RAM can withstand > 1,000 cycles of LRS/HRS switching, and the device is also highly immune to read disturb. This unipolar device is promising for future 3D high-density NVM storage.

CHAPTER 6

WO_X RRAM Using Rapid Thermal Oxidation

6.1 Introduction

Resistance-based memory [85-103] has attracted much attention for high-density memory applications because of its simple structure, small cell size, high speed, low power consumption, and potential for 3D stacking [71]. Resistance switching memories including transition metal oxides (TMO) and programmable metallization cell (PMC), such as TiO_X [72], NiO_X [67], MoO_X [73], CuO_X, TaO_X, CoO_X [74], and Cu/WO_X [75] have been investigated extensively and significant improvements have been reported. Compatibility with the CMOS process is a major criterion in selecting the metal oxide for RRAM design. WO_X-based RRAM is attractive because it requires only one extra mask without new equipment or new material to the standard CMOS process [63]. We applied a new RTO (rapid thermal oxidation) process to form the WO_X layer [76]. By replacing the down stream plasma oxidation (DSPO) with this RTO process, a larger resistance window (RESET/SET, 50kΩ/10kΩ for RTO device; RESET/SET, 8kΩ/1kΩ for DSPO device) and lower switching voltage (RESET/SET, 1.4V/-1.2V for RTO device; RESET/SET, 2.4V/-1.2V for DSPO device) have been achieved by bipolar operation for the WO_X RRAM devices [76,77]. Morover, bipolar operation, however, is complex in a CMOS circuit. Thus, we also demonstrates the unipolar operation behavior suitable for 3D application with a diode access device [78]. RTO RRAM devices by using unipolar operation show good cycling endurance up to 10^7 times, and operation as 2bit/cell up to 9,000 times.

6.2 Device Fabrication

The fabrication process follows the conventional back-end-of-line W-plug process and the active area is located between the W bottom electrode and the TiN top electrode. The WO_X was prepared by RTO for 60 seconds in oxygen ambient at 500^oC. The temperature ramping rate is 10^oC/sec and the cooling rate is 15^oC/sec. To implement the device in the CMOS process, only a high throughput RTO process and an extra mask are needed.

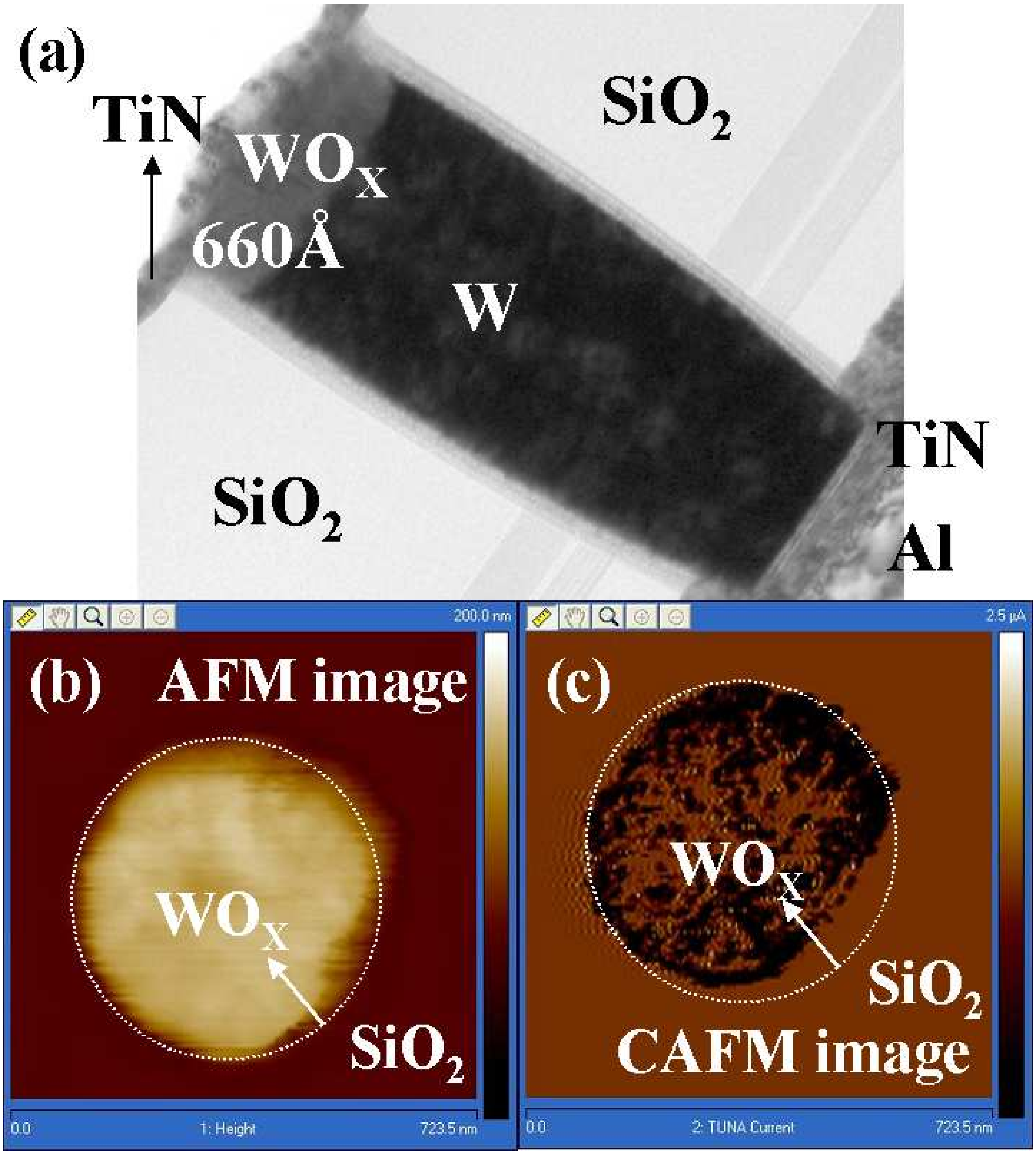


Fig. 6.1. (a). Cross-sectional TEM image for WO_X RRAM. (b) and (c). AFM and Conductive-AFM images of WO_X cell surface.

Figure 6.1 (a) shows the cross sectional TEM image of the WO_X resistive memory with 0.18μm diameter. The thickness of WO_X by RTO is about 660Å that is thick than by DSPO (140 Å). The AFM image of the fresh WO_X plug without the top electrode with 0.5μm diameter is shown in Figure 6.1 (b). A conductive AFM mapping is achieved by applying a 0.1V bias, as shown in Fig. 6.1 (c). The dark area represents the local conducting paths detected by Conductive-AFM (C-AFM). The existence of these conductive paths explains the low initial resistance (500Ω) of as-processed WO_X devices.

6.3 High-Speed Multilevel Resistive RAM Using RTO WO_X

6.3.1 Basic Electrical Characteristics

Figures 6.2 and 6.3 show the intrinsic pulse R-V characteristics by positive and negative pulses. Positive pulses reset the device to high resistance states, and negative pulses set the device to a low resistance state. However, the required pulse amplitudes are relatively high. Similar to the WO_X fabricated by plasma oxidation [63], after applying a forming step (3.5V/50ns) to the cells, the programming voltages are dramatically reduced (Fig. 6.4), and the cells are stable for normal operations. The cell resistance is then checked after different 50ns programming pulses. The resistance increases from the low resistance state (LRS) to the high resistance state (HRS) as the pulse amplitude increases. The resistance window of our RTO WO_X is 10X of the plasma-oxidized sample [69]; this indicates the performance of WO_X RRAM is strongly dependent on the oxidation process.

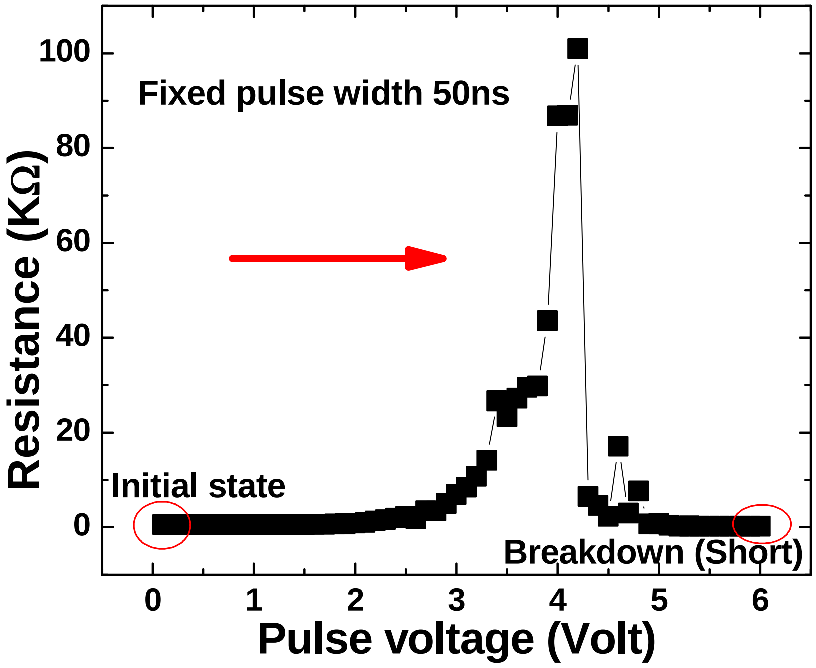


Fig. 6.2. The resistance state can be enhanced by positive pulse. At high voltage, the device becomes shorted.

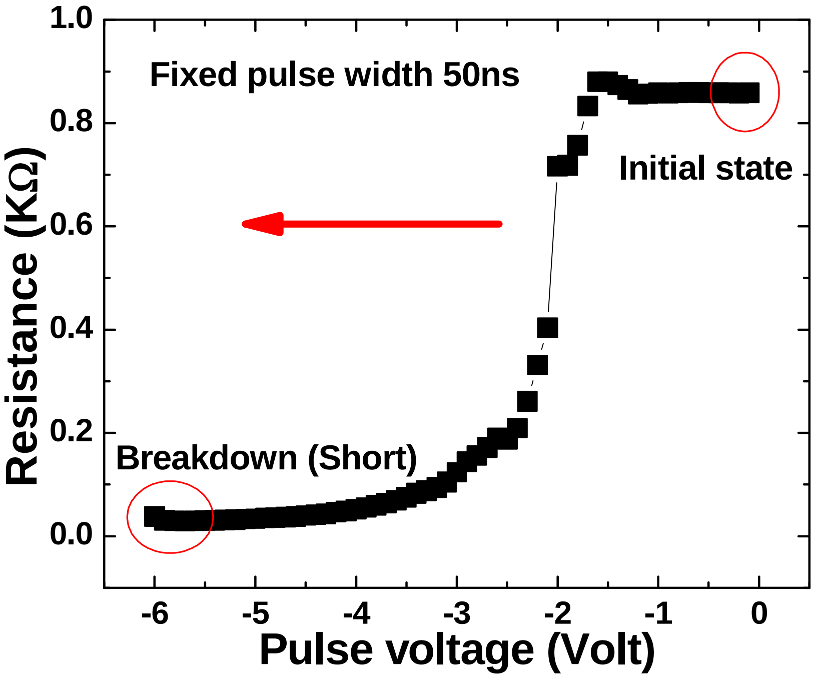


Fig. 6.3. Negative pulses, even at higher voltages, do not reset the device.

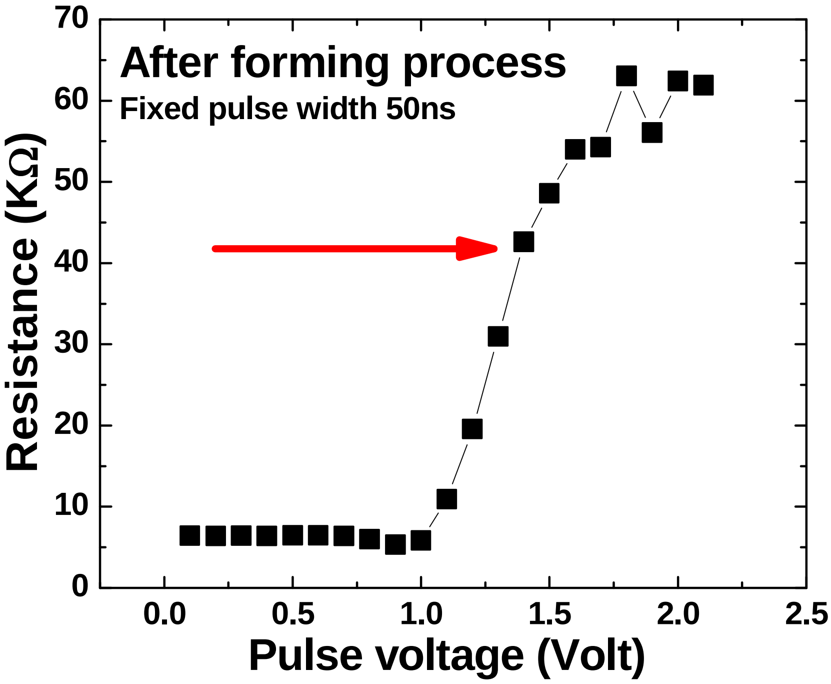


Fig. 6.4. R-V characteristics after the forming process. Forming process is useful to reduce the switching voltage.

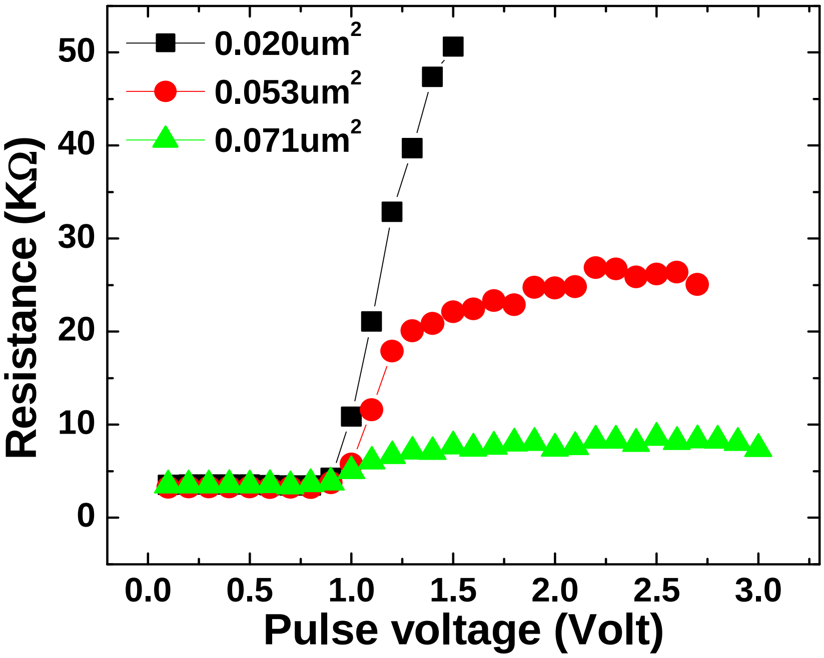


Fig. 6.5. The resistance window increases for smaller contact area. The devices are treated with a forming process using a 4V/ 50ns pulse first.

6.3.2 Device Performance

Figure 6.5 shows the R-V curves from cells with different contact sizes after forming. With a smaller contact, the cell shows a lager resistance window, which is beneficial for scaling. Figure 6.6 shows programming voltages required for successful SET and RESET operations for 50 cells. The tight distributions mean the contact size and the RTO WO$_X$ are both uniform. More interesting is that the RTO WO$_X$ device presents excellent cycling endurance—a resistance window (from 10KΩ to 50KΩ) is maintained very well even after 10^8 cycles (1.4V, 50ns for RESET and -1.2V, 50ns for SET), as shown in figure 6.7.

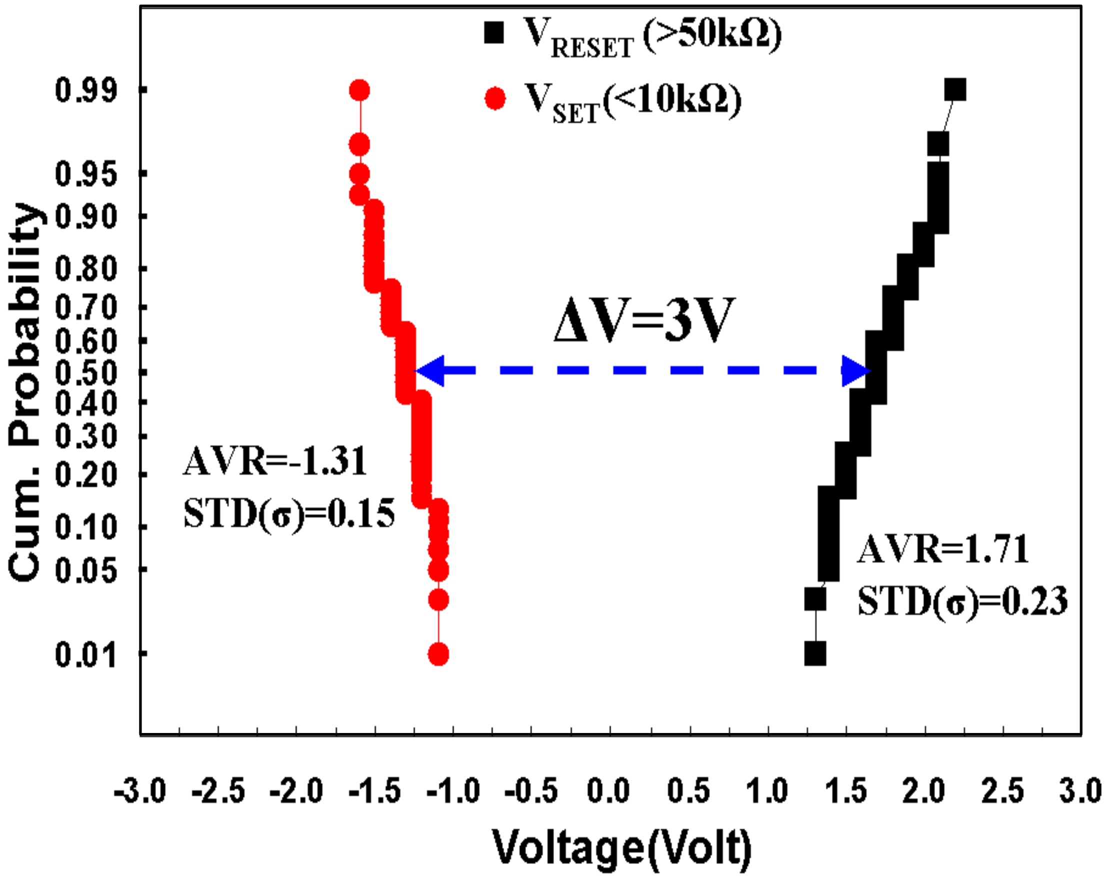


Fig. 6.6. Voltage distribution for HRS and LRS of 50 memory cells.

6.3.3 Transient Effect

For high speed testing, the pulse IV characteristics of the RTO sample are collected through a customized high-speed tester [81]. The transient I-V characteristics for both RESET and SET operations are shown in figures 6.8 and 6.9. The RESET pulse width is only 2ns, and the equivalent current density is about 3.4x10^6A/cm^2. Successful SET is achieved by a 2ns pulse with an equivalent current density of 3.3x10^6A/cm^2. The transient currents for RESET and SET operations with different pulse widths ranging from 2ns to 100ns are shown in Fig. 6.10. Both SET and RESET currents show slight pulse width dependence. Short pulse width can reduce the SET and RESET currents. Figure 6.11 shows the cell resistance after programming pulses with different pulse widths. Compared to Fig. 6.10, the RESET resistance remains at the same level but the SET resistance decreases as the pulse width increases.

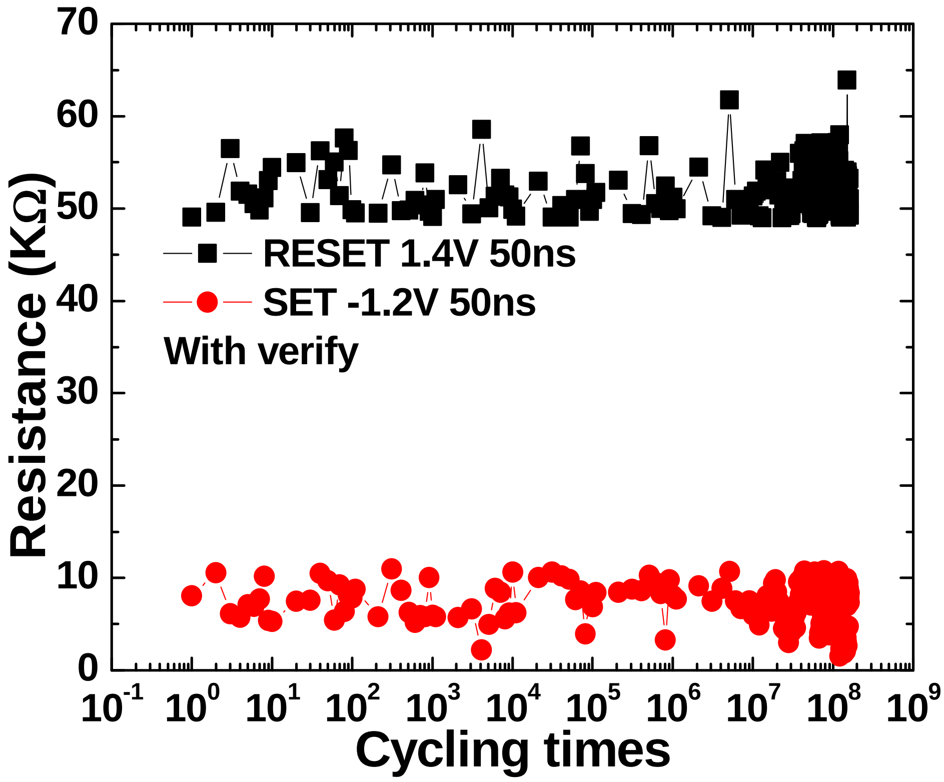


Fig. 6.7. Cycling characteristics of the WO_X memory cell. RHS/LHS resistance window is well separated at 50k Ω /10k Ω up to > 10^8 cycles.

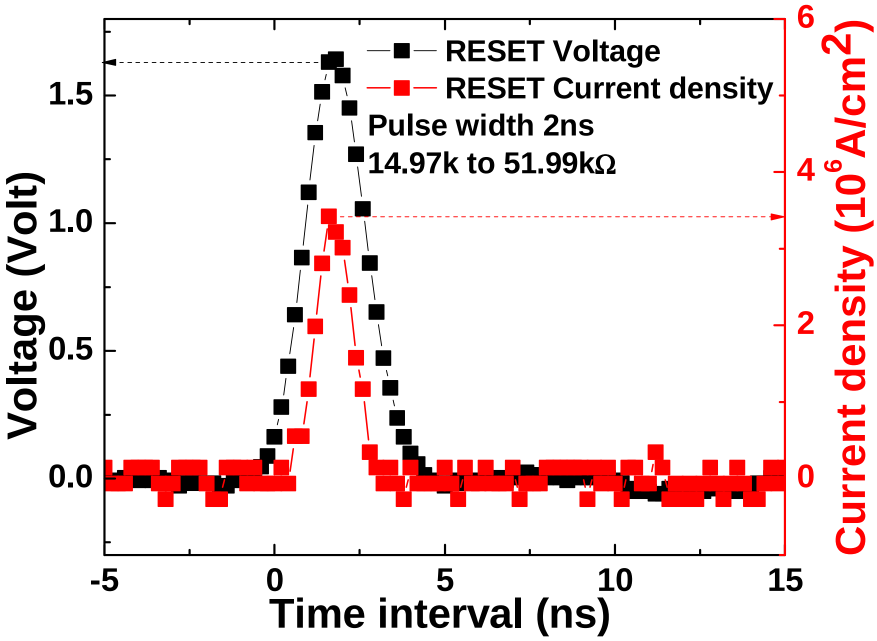


Fig. 6.8. Time resolved voltage and current traces of RESET operation. The input pulse width is 2ns. The RESET current density is about 3.4x10^6 A/cm^2.

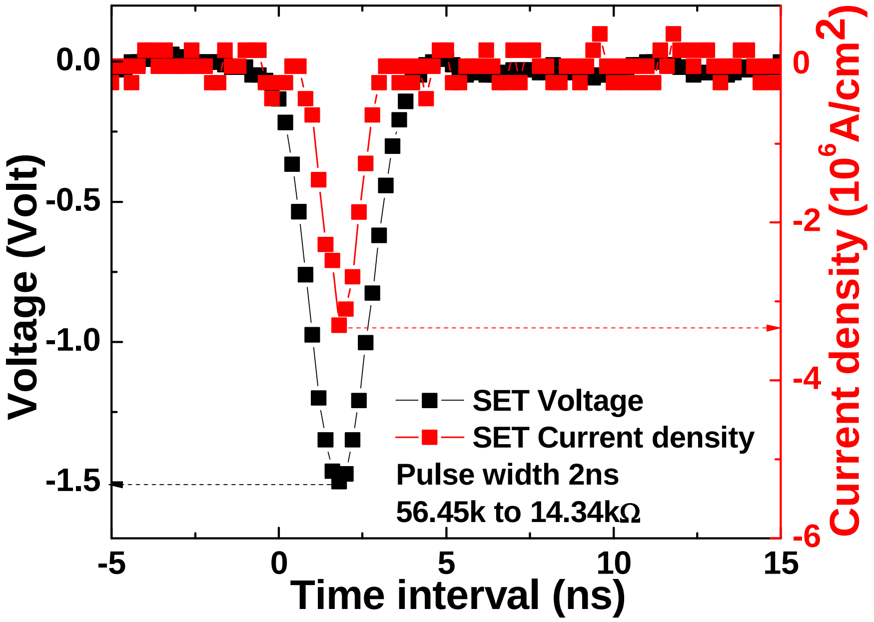


Fig. 6.9. J-t and V-t curves of SET operation. It also shows high speed erase capability (~2ns). The SET current density is about 3.3x10^6 A/cm^2.

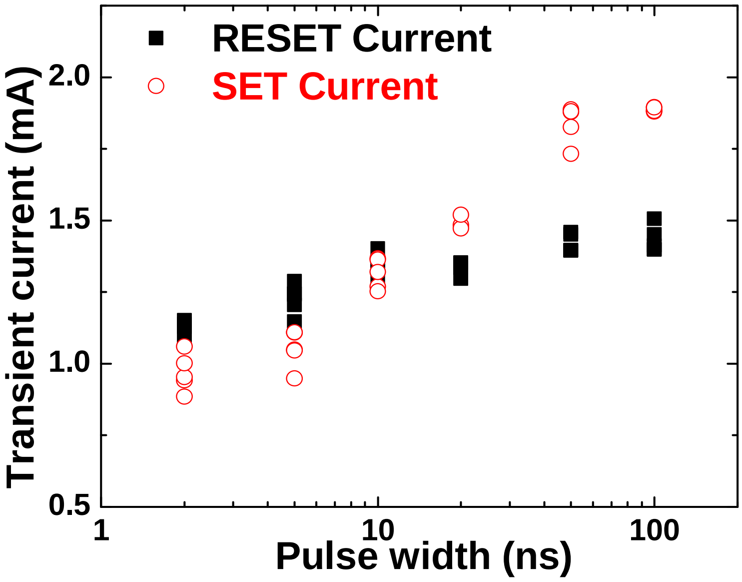


Fig. 6.10. Transient currents for RESET and SET using various pulse widths.

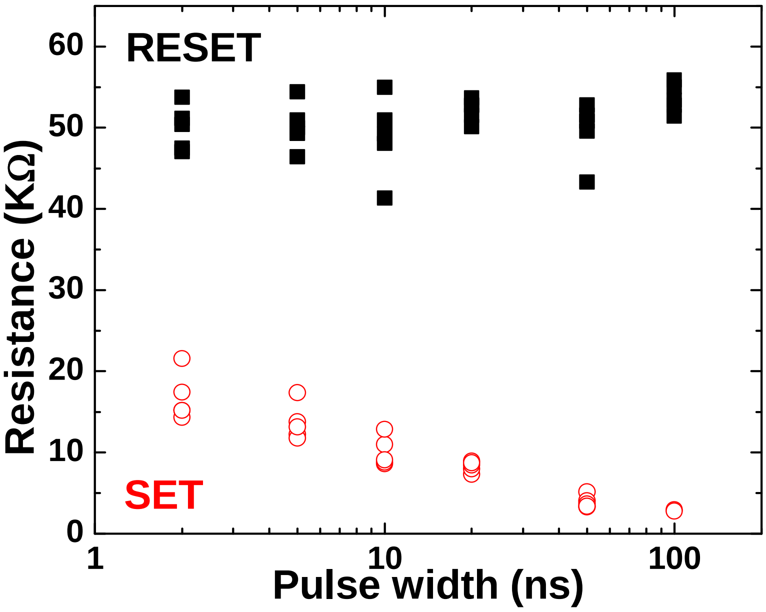


Fig. 6.11. Corresponding RESET and SET states for various pulse widths.

6.3.4 Multi-Level Operation

Excellent 2-bit/cell operation to more than 10^4 cycles is shown in Fig. 6.12. A 10KΩ resistance window is maintained for all adjacent states. The state 00, which is the LRS, is achieved by a –1.2V, 50ns SET pulse. The HRS 01, 10, and 11 are obtained by applying 50ns of 1V, 1.2V, and 1.4V pulses, respectively.

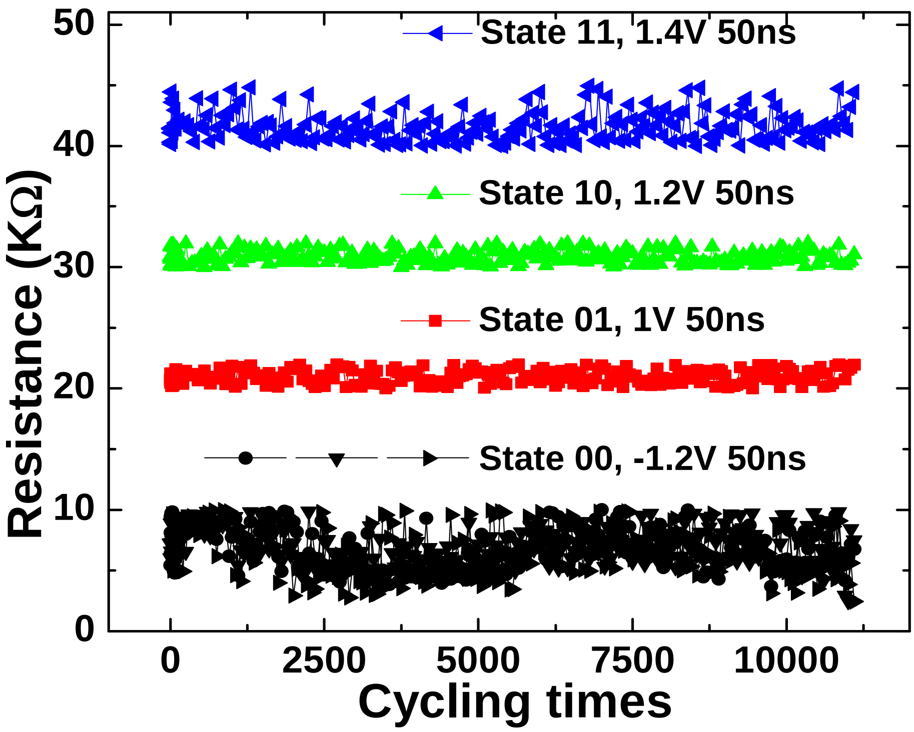


Fig. 6.12. 4-level cycling test beyond 10^4 cycles with verification. Three RESET states (01,10,11) are programmed by different voltage positive pulses and the SET level (00) is programmed by a negative pulse.

Figure 6.13 shows good immunity to read disturb for all states up to 0.5V. Figure 6.14 illustrates a 3-bit/cell operation RTO WO_X RRAM using a carefully designed P-V (program-verify) algorithm. The resistance window is more than 3KΩ for all adjacent states while cycling endurance is more than 8,000 times.

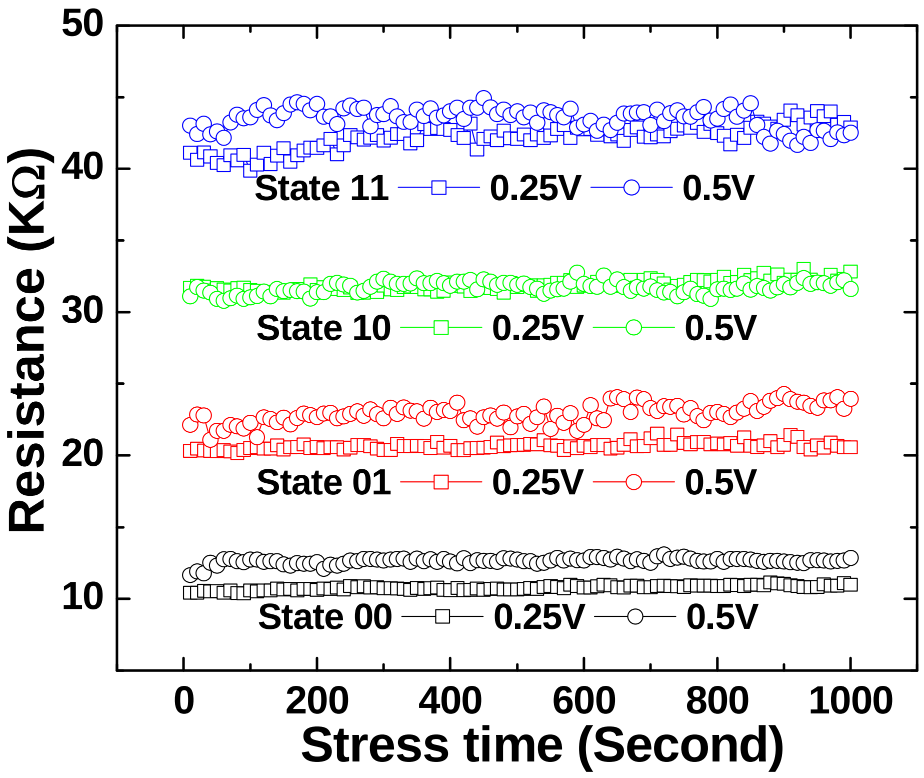


Fig. 6.13. Read disturb test. All states show acceptable read disturb up to 0.5V.

6.3.5 Switching Mechanism Supposition

The forming and switching behavior can be understood by oxygen vacancy diffusion near the interface, as shown in Fig. 6.15. After RTO the WO$_X$ has low resistance due to oxygen vacancy Vo$^+$ near the interface between the top electrode and the transition layer as shown in Fig. 6.15(a). Electrons can hop easily through the bottom to the top electrode. After the forming operation, oxygen is attracted by the positive voltage and fills the vacancies, as in Fig. 6.15(b). This breaks the conduction chain and is equivalent to filament rupture. During the SET operation, a negative voltage is applied and oxygen is repelled again and the vacancies are resumed, forming the conductive path again, as shown in Fig. 6.15(c). But this SET process just repels a small amount of oxygen from the vacancies with lower energy barrier. As shown in Fig. 6.15(d), these "shallow" vacancies can be readily filled by applying a low positive RESET voltage.

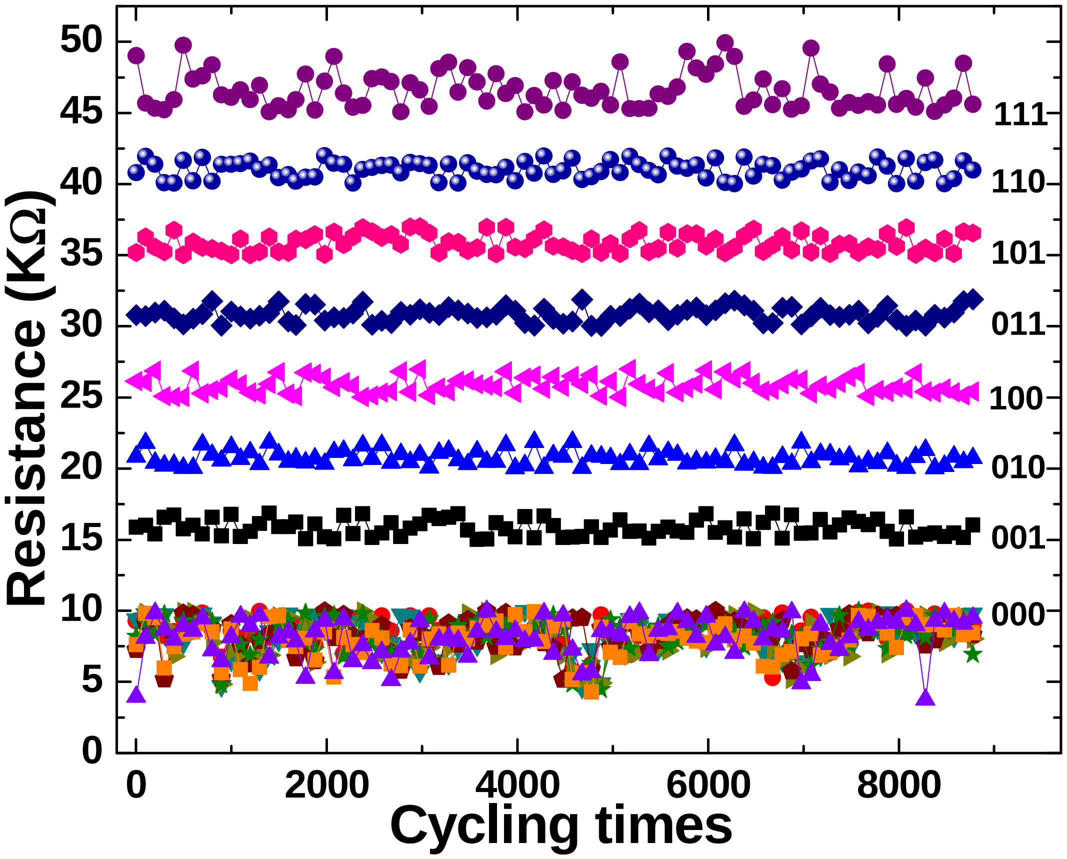


Fig. 6.14. 8-level cycling test of more than 8k cycles with verification. Well distinguishable resistance windows are maintained for each states.

In order to understand the switching mechanism of RTO WO_X RRAM, the conductive AFM (C-AFM) mapping is utilized as shown in Fig. 6.16(a). The dark area represents the local conducting paths detected by Conductive-AFM (C-AFM) with 0.1V bias as shown in Fig. 6.16(b). The existence of these conductive paths explains the low initial resistance (500Ω) of typical WO_X devices. After bias 1.5V, the dark area is eliminated which means the RESET process as shown in Fig. 6.16(c). The possible reason is that the oxygen ion generating from air by local high electrical field penetrates to RTO WO_X film and transfers to WO_3 with low conductivity. Figure 6.16(d), and (e) show the SET process. In contrast to RESET process, the dark area could be recovered by negative pulse -2.5V, 50ns. Meanwhile the reduction behavior of WO_3 occurs and transfers to WO_X with high conductivity. According to this result, the switching mechanism of RTO WO_X RRAM is proposed to the redox behavior of tungsten oxide.

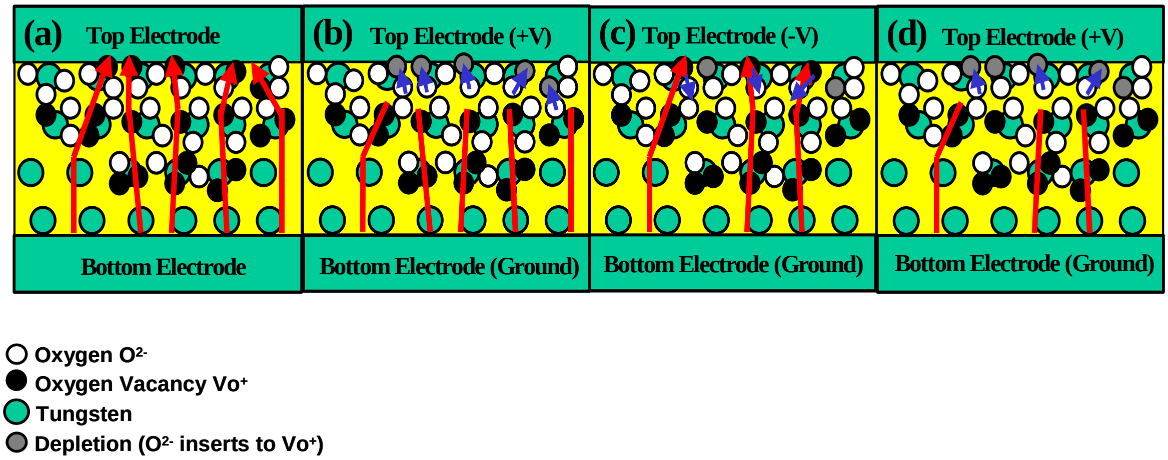
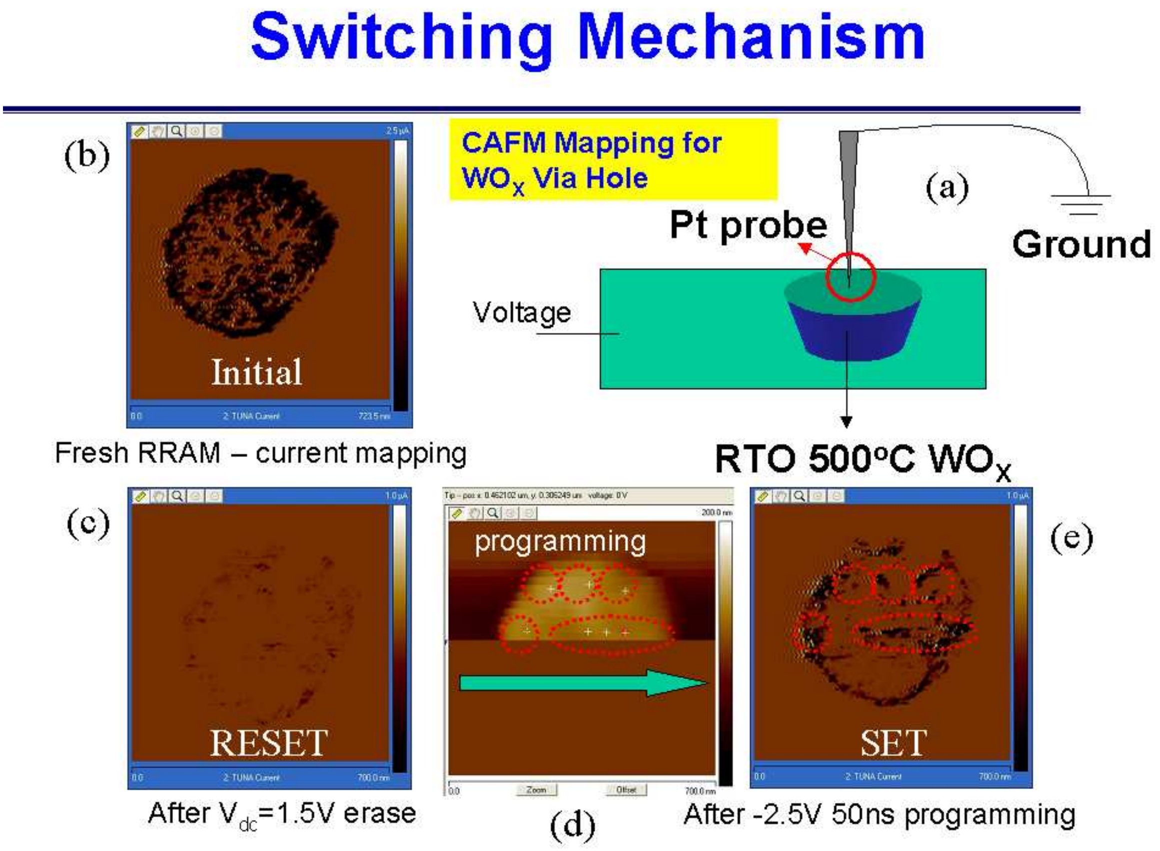


Fig. 6.15. Schematics for proposed WO_X RRAM switching mechanism. (a) Right after the RTO WO_X formation and top electrode process, many oxygen vacancies are present in the WO_X film leaving easy electron hopping paths. The initial resistance is below 1kΩ due to these conduction paths (sometimes referred to as filaments). (b) During the forming process, the positive voltage drives oxygen into vacancies near the top electrode. This cuts off the conduction paths and the resistance increases dramatically. (c) When a large enough negative voltage is applied, oxygen is separated from shallow vacancy traps. Thus some of the conduction paths are reconnected and the resistance drops (SET). (d) A positive voltage drives oxygen back into shallow vacancies and disrupt the conduction paths (RESET).

6.3.6 Conclusion

Excellent cycling endurance (up to 10^8 times) and low voltage (1.4V) operation are demonstrated by RTO WO_X RRAM. The new device exhibits a 10X larger resistance window than plasma oxidized device and provides a better base for MLC operation. The switching speed is extremely fast (~2ns), and the equivalent programming current density is ~$3x10^6$A/cm^2. Two-bit/cell operation with 10K cycle endurance and 3-bit/cell operation with more than 8K cycle endurance are demonstrated. This RTO WO_X RRAM is promising for high-density memory applications.



Switching Mechanism

CAFM Mapping for WO_X Via Hole

RTO 500°C WO_X

Fresh RRAM – current mapping

After V_{dc}=1.5V erase

After -2.5V 50ns programming

Fig. 6.16. C-AFM images of the WO_X cell surface.

6.4 Unipolar Switching Behaviors of RTO WO_X RRAM

6.4.1 Pulse Voltage and Pulse Width Dependence

Figure 6.17(a) shows the pulse R-V curves for forming [76] and RESET processes (All electrical results are measured on 0.18μm diameter devices). The program voltage ramps up with a fixed pulse width of 50ns. The SET voltage is fixed at 3V while varying the pulse width (Fig. 6.17 (b)). The resistance value is measured with a read voltage of 0.25V after programming. The resistance is increased from the initial (~500Ω) to the RESET state (≧ 40kΩ) by applying a positive voltage for the forming process, similar to the behavior of the DSPO devices [69]. The resistance is then decreased to SET state (≦10kΩ) by applying an electrical field of the same polarity with a long pulse width (300ns) in the SET process. The SET state is controlled at about 10kΩ, much higher than the SET state we published before [63, 69, 77]. It is because once the device is over-SET to below 1kΩ, the programming current is high and the endurance is sacrificed. After the SET process, the resistance is increased to the RESET state by applying a positive voltage. It is interesting to note that for unipolar operation, both forming and RESET voltage are comparable, whereas the forming and RESET voltages for bipolar operation are quite different [76]. This discrepancy suggests that the mechanism of unipolar programming is different from that of bipolar programming. The current density and relative power of unipolar operation are very high, ~ 1×10^8 A/cm^2 and ~ 75mW, respectively, thereby indicating a thermal-chemical effect where conducting paths in the top electrode and WO_X interface are formed and ruptured during operation [71, 79]. Reproducibility of unipolar operation is demonstrated by three test rounds of the same RTO sample.

The resistance dependence on the pulse width using square pulse (2.25V to 3V) is shown in Figure 6.17 (c). The resistance decreases as the pulse width increases. The SET pulse width can be reduced to 300ns with a voltage of 3V. The resistance as a function of voltage with pulse width ranging from 50ns to 250ns is shown in Figure 6.15 (d). With the

50ns pulse, the resistance increases to the RESET state at 3.3V. However, it is difficult to increase the resistance to the RESET state with long pulse width (150ns and 250ns), because such long pulse is operating the device in the unipolar thermal-chemical SET regime.

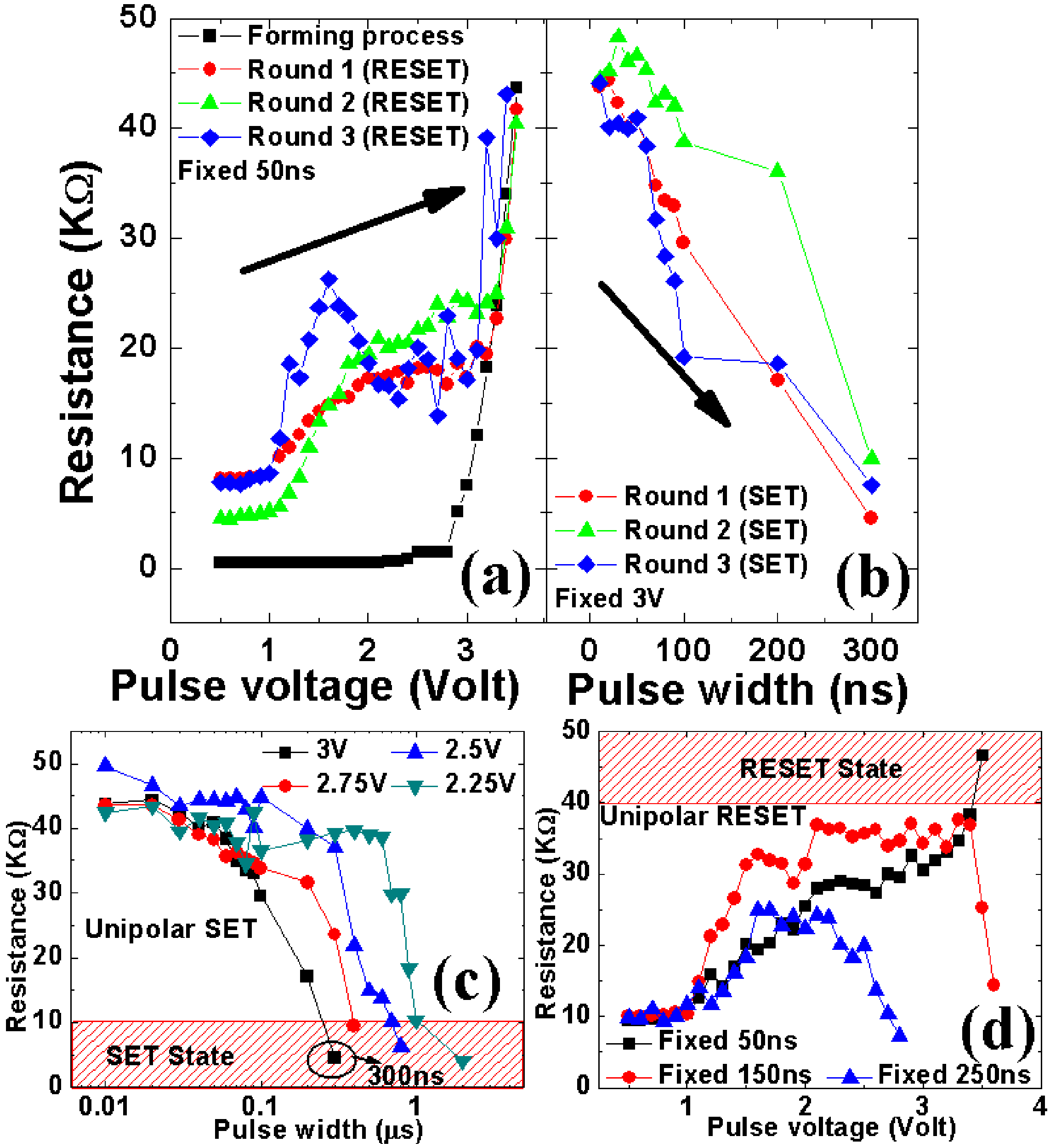


Fig. 6.17 (a). Unipolar RESET for pulse R-V curves and (b) SET for pulse R-t curves. (c) Pulse width dependence of unipolar SET with varied positive voltage and (d) voltage dependence of unipolar RESET with varied pulse width.

6.4.2 IV Characteristics

In addition to the programming properties, the read characteristics are also investigated. Figure 6.18 (a) shows the IV characteristics and fitting results for SET and RESET states. Non-linear behaviors for both SET and RESET states are observed.

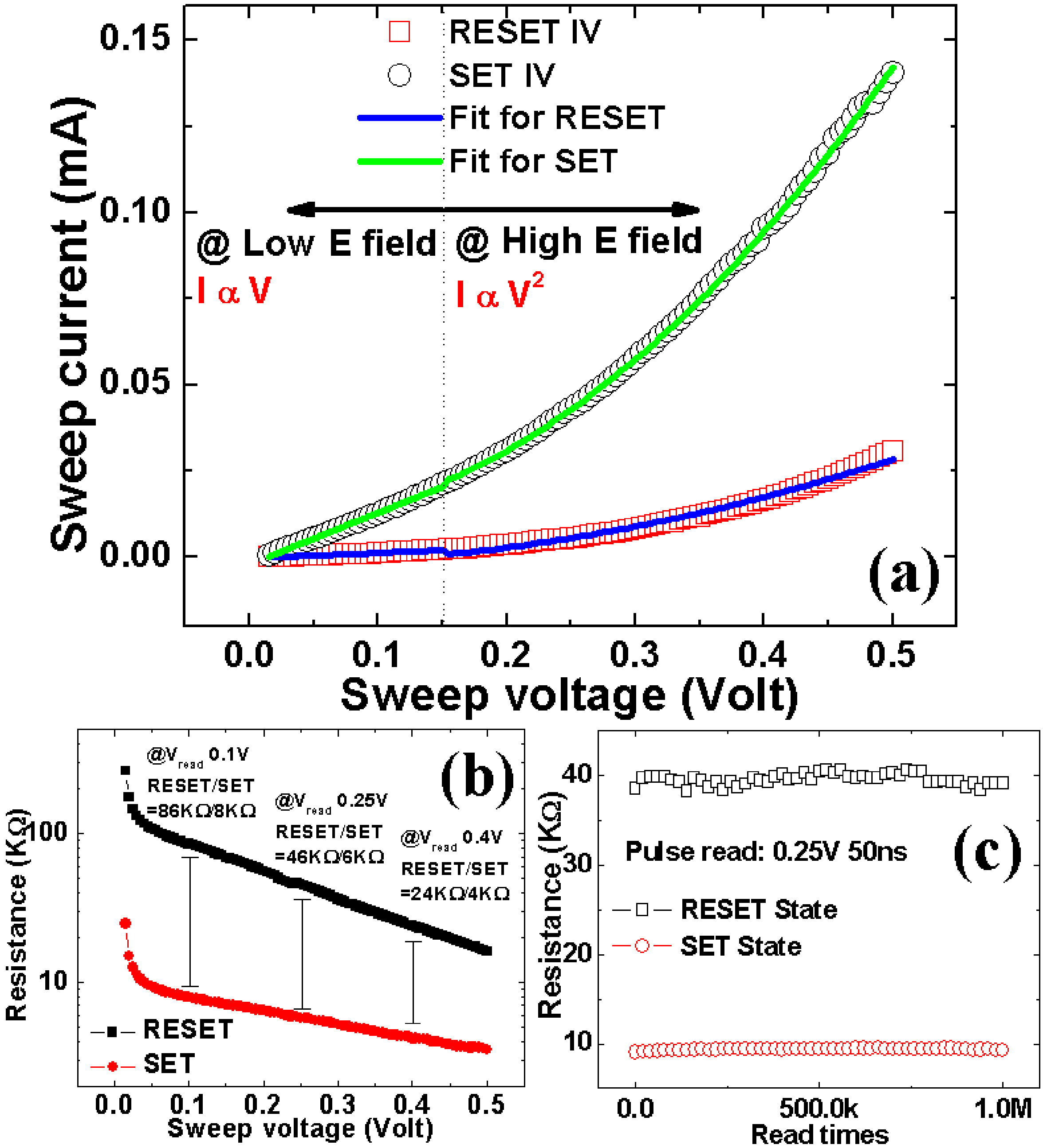


Fig. 6.18 (a). The IV curves and fitting results for SET and RESET states. (b) Read dependence for RESET and SET states. (c). 1 M read times for 0.25V pulse read voltage.

For both RESET and SET operations, the current is proportional to the electrical field for voltage below 0.15V, indicating Ohmic conduction mechanism. For voltage between 0.15V and 0.5V, the current is proportional to the square of the applied voltage, suggesting that the SCLC (space charge limited current, $J = 9\varepsilon\mu V^2 / 8d^3$) is the dominant conducting mechanism. The fitting is divided into two regions because a decent E field is needed to generate the uncompensated electrons near the interface between TiN and WO_X to perform the SCLC mechanism.

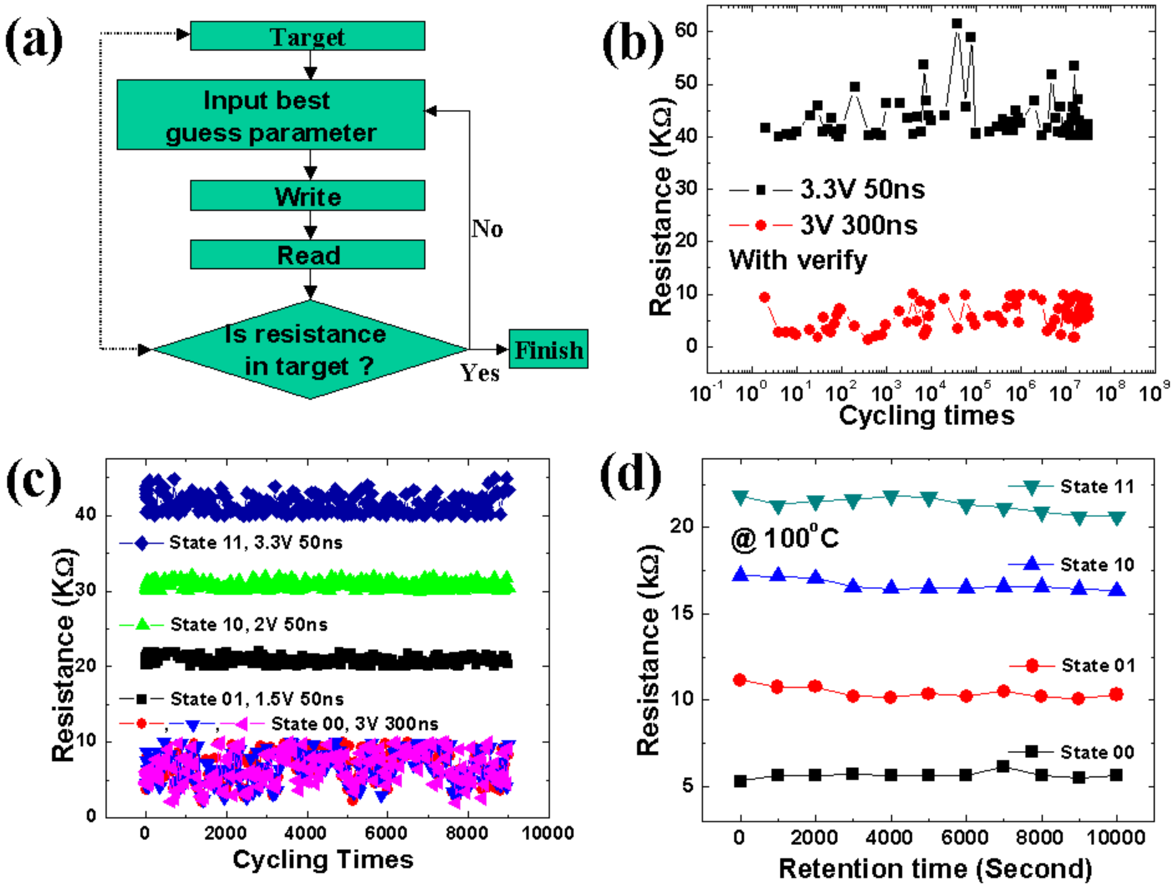


Fig. 6.19 (a). Program-verify algorithm for cycling test of RTO WO_X RRAM (b). Cycling characteristics of the RTO WO_X RRAM cell with unipolar operation. RESET/SET resistance window of 40kΩ/10kΩ is well maintained up to 10^7 cycles. (c). 4-levels cycling test for 9000 cycles. Three RESET states (01,10,11) are programmed by positive pulses of different voltage and the SET level (00) is programmed by a positive pulse with long pulse width. (d). Retention test for RTO WO_X RRAM with 100°C baking. The resistance values are lower indicating the semiconductor behaviors.

On the other hand, below the critical bias the IV curve is Ohmic [80]. Figure 6.18 (b) demonstrates the strong read voltage dependence of the device resistance. As shown by the non-linear behaviors of the RESET and SET I-V curves, the read voltage affects the resistance window for RTO samples. Therefore, a low read voltage improves the resistance window. A read disturb test is performed using 0.25V/50ns read pulses up to 1 million times for both the SET and RESET states (Fig. 6.18 (c)). Both the SET and RESET states show good immunity to read disturb without observable degradation after 1M read pulses at 0.25V.

6.4.3 Performance

Figure 6.19 demonstrates good cycling endurance and MLC (Multi-Level Cell) results of the device. To obtain tight resistance distribution, program-verify algorithm is used (Fig. 6.19 (a)) [77]. There are two parameters to control the resistance states of the RTO WO_X RRAM. Pulse voltage is varied to tune the RESET value while the pulse width is varied to adjust the SET value. A resistance window of 10kΩ to 40kΩ with RESET condition of 3.3V and 50ns, and SET condition of 3V and 300ns is maintained up to 10^7 cycles (Fig. 6.19 (b)). Furthermore, an excellent 2-bit/cell operation with a 10kΩ resistance window between states with > 9,000 cycles is shown in Fig. 6.19 (c). Figure 6.19 (d) is the further retention test of the four states at 100^oC. It shows stable resistance during 10000 seconds of baking.

6.4.4 Conclusion

Unipolar behavior of RTO WO_X RRAM is studied. The RESET and SET resistance can be manipulated by varying the pulse voltage and width, respectively. With the program-verify algorithm, cycling endurance up to 10^7 cycles and 2bit/cell operation over 9,000 cycles are demonstrated. With its robust unipolar behaviors, the RTO WO_X RRAM is a promising candidate for future memory applications.

6.5 A Study of Top Electrodes Effect for WO_X RRAM

6.5.1 Conduction Mechanism

Figure 6.20 shows the structure and the process flow of the WO_X cell. The contact size is 0.18μm and a 500°C RTO (Rapid thermal oxidation) process is used for forming the WO_X [76]. Different top electrodes (TEs) are formed by PVD deposition.

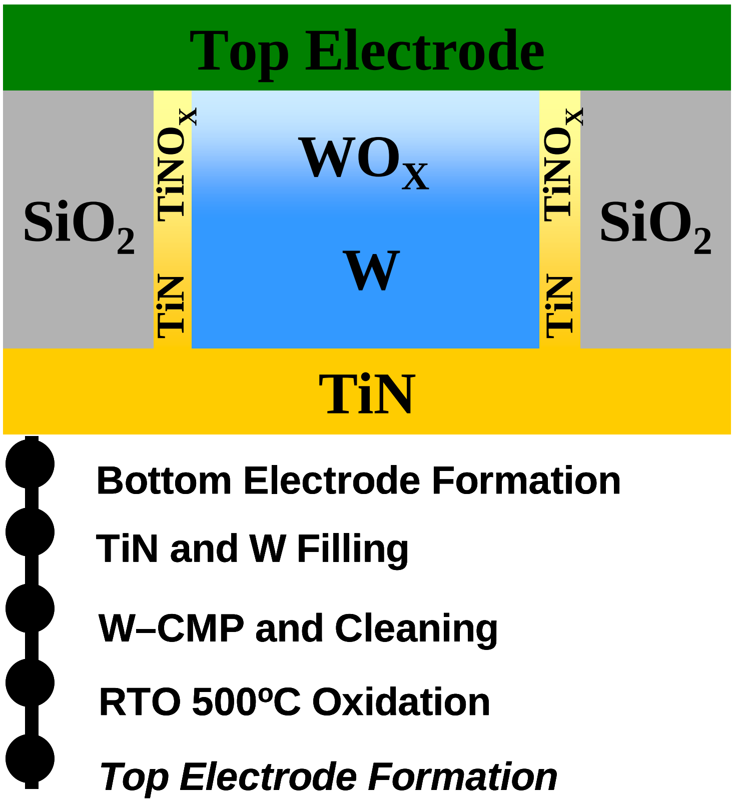


Fig. 6.20. WO_X RRAM structure and process flow.

As shown in Fig. 6.22, the initial resistance of WO_X devices strongly depends on the WF of the TE material. A low WF TE has low initial resistance, and a high current is needed during forming to bring the resistance from low to high (type I) [76]. In contrast, a high WF TE results in high initial resistance and in this case the forming process (type II) brings the resistance from high to low.

SCLC equation:

$$J = \frac{9}{8}\mu_n \varepsilon \frac{V^2}{d^3} \text{...Eq.(1)}$$

Thermionic emission:

$$J = (A^*) * T^2 \exp\left(\frac{q\sqrt{qE/4\pi\varepsilon_i}}{k_B T} - \frac{q\Phi_B}{k_B T}\right)$$

$$J = 1.08\text{E}7 * \exp(a\sqrt{V} - b)\text{...Eq.(2)}$$

A^* =Effective Richardson constant

= $120\,\text{Acm}^{-2}\text{K}^{-2}$

T = Absolute temperature

Φ_B = Barrier height $= b * \frac{k_B T}{q}$...Eq.(3)

ε_i =Insulator dynamic permittivity

Fig. 6.21. Formulas for SCLC and thermionic emission.

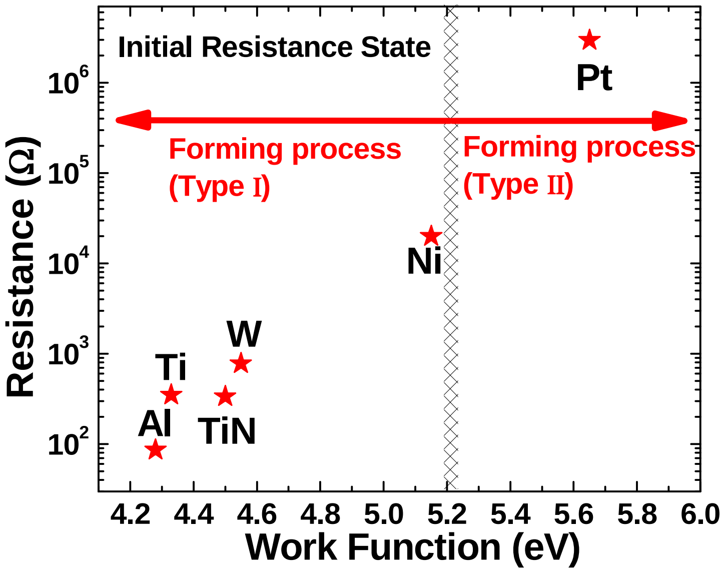


Fig. 6.22. The initial resistance increases with the WF of the TE. Two types of forming process (I and II) are observed.

Furthermore, the conduction mechanism of TiN, Ni, and Pt top electrodes WO_X RRAMs is studied. For a low WF TE, TiN, the IV curve of the initial state follows the SCLC mechanism [Figure 6.21, Eq.(1)]. For high WF TEs, Ni and Pt, both of the I-V curves are well matched with thermionic emission [Figure 6.21, Eq.(2)] as shown in Fig. 6.23. The barrier heights of Ni device, 0.18eV and Pt device, 0.44eV are obtained [Figure 6.21, Eq.(3)].

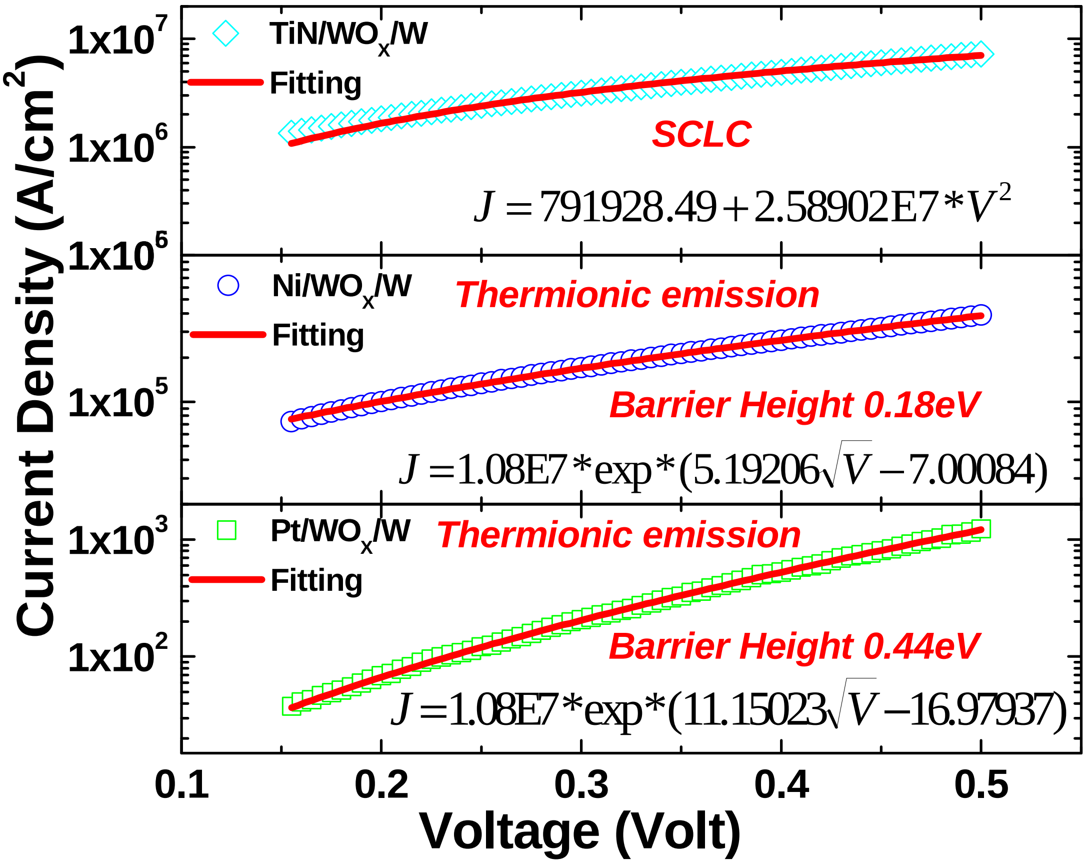


Fig. 6.23. IV curves and fitting results for initial states of Pt/WO_X/W, Ni/WO_X/W, and TiN/WO_X/W. Thermionic emission describes the behaviors for Pt and Ni/WO_X/W well, but not TiN TE.

Figure 6.24 demonstrates slight temperature dependence of the initial state for TiN/WO_X/W device from room temperature (RT) to 80°C. The current versus square of voltage is further plotted, that the linear trend indicates the SCLC mechanism. Temperature dependence of initial states for Ni/WO_X/W and Pt/WO_X/W from RT to 80°C are shown in Fig. 6.25 and Fig. 6.26, respectively. The IV curves can be described by the thermionic emission. Figure 6.27 further supports the thermionic emission mechanism for Ni/WO_X/W and Pt/WO_X/W cells [83]. The schematics of conduction mechanism of WO_X RRAM with Pt, Ni, and TiN are shown in Fig. 6.28.

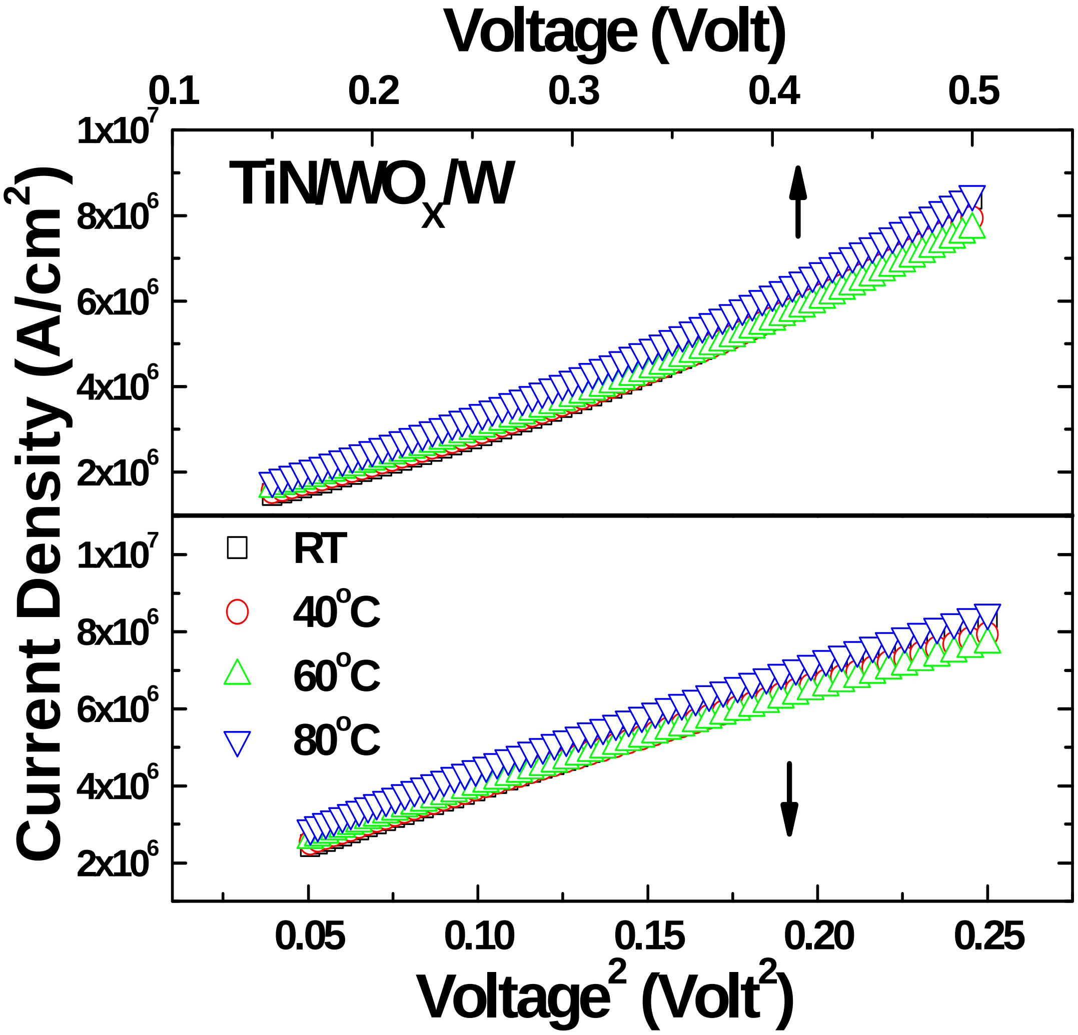


Fig. 6.24. IV curves and J versus V^2 curves for TiN/WO_X/W at different temperatures RT, 40, 60, and 80°C. J is proportional to V^2 indicating the SCLC behaviors.

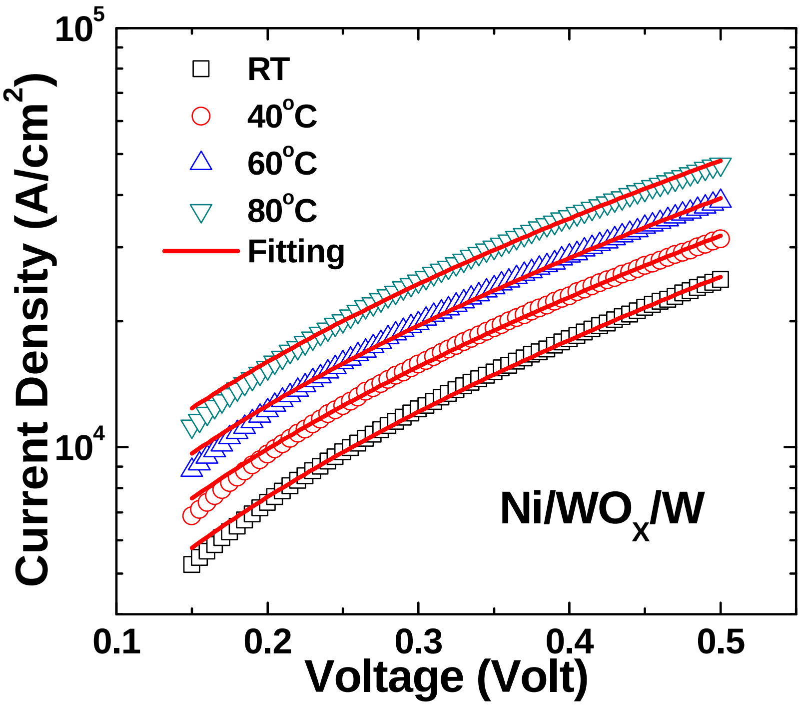


Fig. 6.25. IV curves and thermionic emission fitting results for initial state of Ni/WO$_X$/W at different temperatures RT, 40, 60, and 80^{o}C.

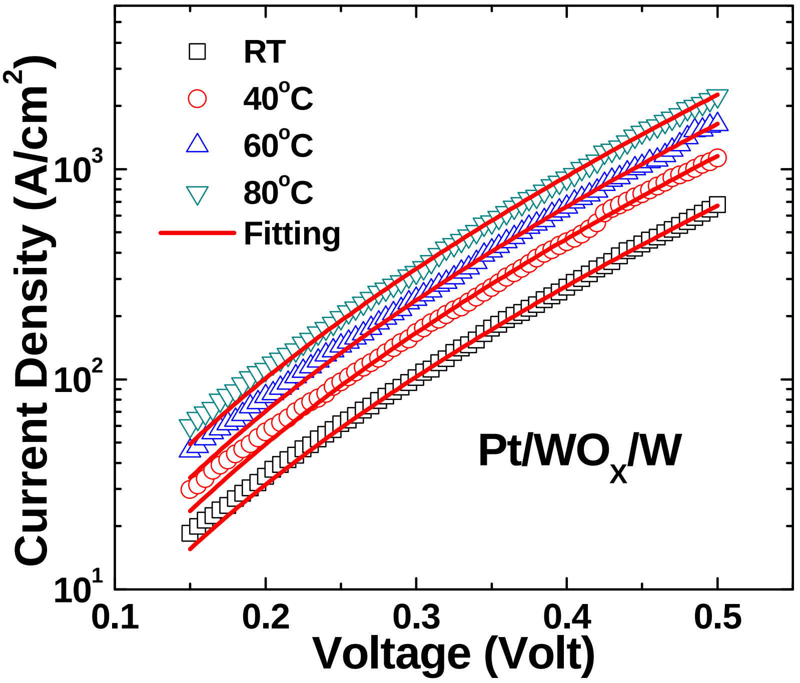


Fig. 6.26. IV curves and thermionic emission fitting results for initial state of Pt/WO$_X$/W at different temperatures RT, 40, 60, and 80^{o}C.

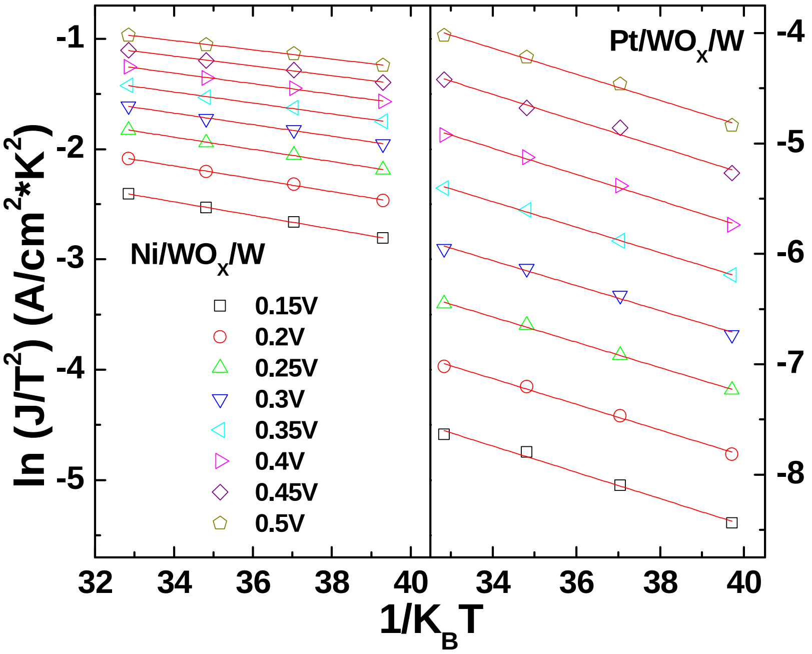


Fig. 6.27. ln (J/T^2) versus $1/k_BT$ curves for Ni/WO_X/W and Pt/WO_X/W with bias between 0.15V to 0.5V. The linear trend indicates the thermionic emission behaviors

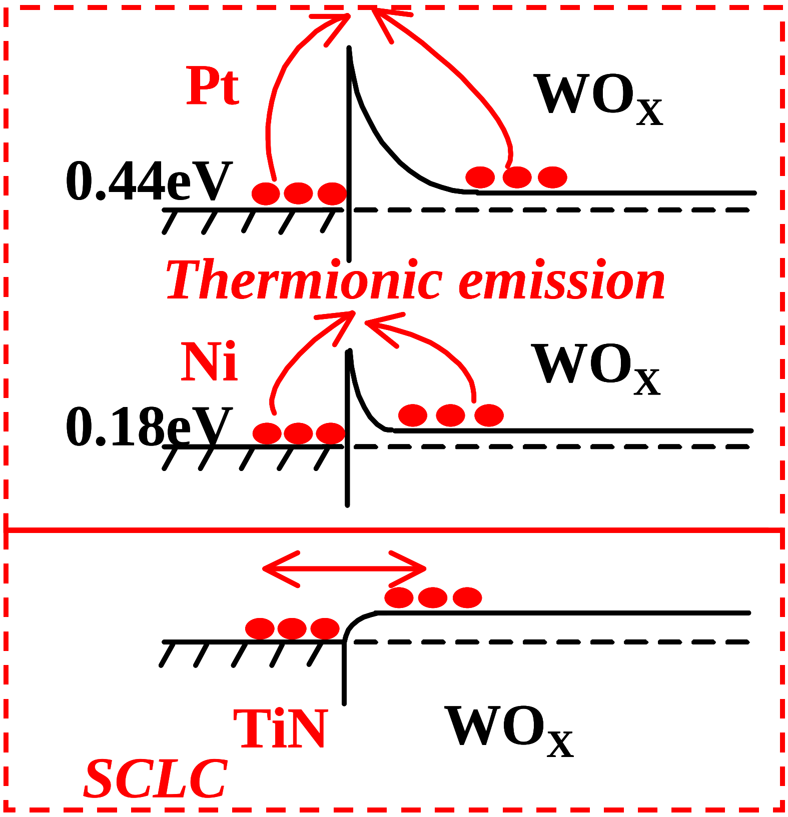


Fig. 6.28. Schematics for conduction mechanism for Pt, Ni, and TiN/WO_X/W.

The resistance window is important to memory application, thus the impact of WF is further studied. Figure 6.29 shows the resistance window as a function of the WF of the TE. The devices with Ni and/or Pt TEs show good resistance windows larger than 2 orders of magnitude, indicating that TE plays an important role for electrical properties. From the experiments above, we may conclude that a high WF electrode such as Ni and Pt is needed to get a large resistance window. However, Pt electrode is difficult to process and expensive. Therefore, we choose the Ni/WO_X/W RRAM for further investigation.

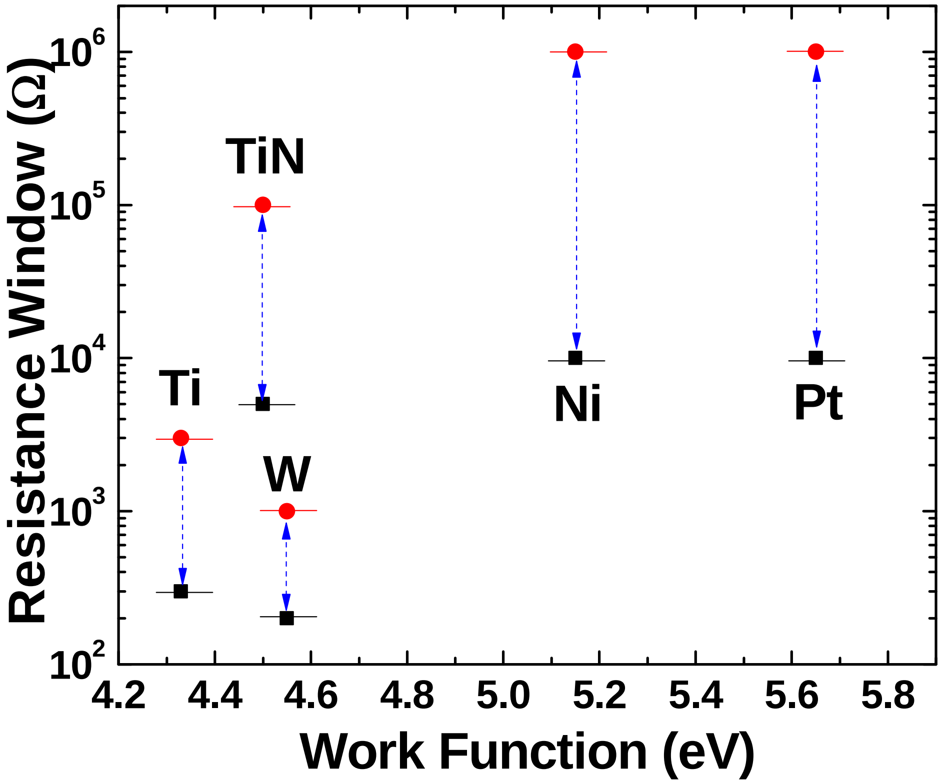


Fig. 6.29. High WF TE produces large resistance window. Both Pt/WO_X/W and Ni/WO_X/W show 100X window and higher RESET resistance.

6.5.2 Device Performance

Figure 6.30 shows the cross-sectional TEM of the Ni(200nm)/WO_X(70nm)/W cell. For bipolar switching of Ni/WO_X/W RRAM, positive pulses are used to RESET the device, and negative pulses are used to SET the device as shown in Fig. 6.31. The transient I-t curves for RESET and SET processes are shown in Fig. 6.32. The RESET (2V/50ns) current is about 180uA, and SET (-1.8V/ 50ns) current is about 150uA. Figure 6.33 demonstrates the cycling endurance for 10k times. To obtain tight resistance distribution, a program-verify algorithm is used [76]. Both the SET and RESET states show good immunity to read disturb without observable degradation after 0.6V stressing for 1,000 seconds, as shown in Fig. 6.34. The retention results after baking at 150°C are shown in Fig. 6.35. Both RESET and SET are well separated after two weeks of baking, and the devices continue to function normally after baking. Further retention studies are shown in Fig. 6.36. An activation energy of 1.34eV is deduced from the Arrhenius plot, and retention time extrapolated predicts > 10 years at 115°C and > 300 years at 85°C.

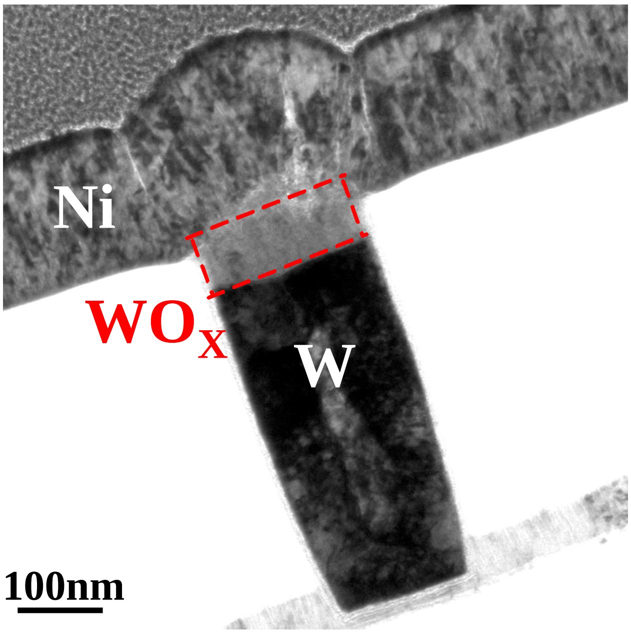


Fig. 6.30. Cross sectional TEM image of Ni/WO_X/W RRAM.

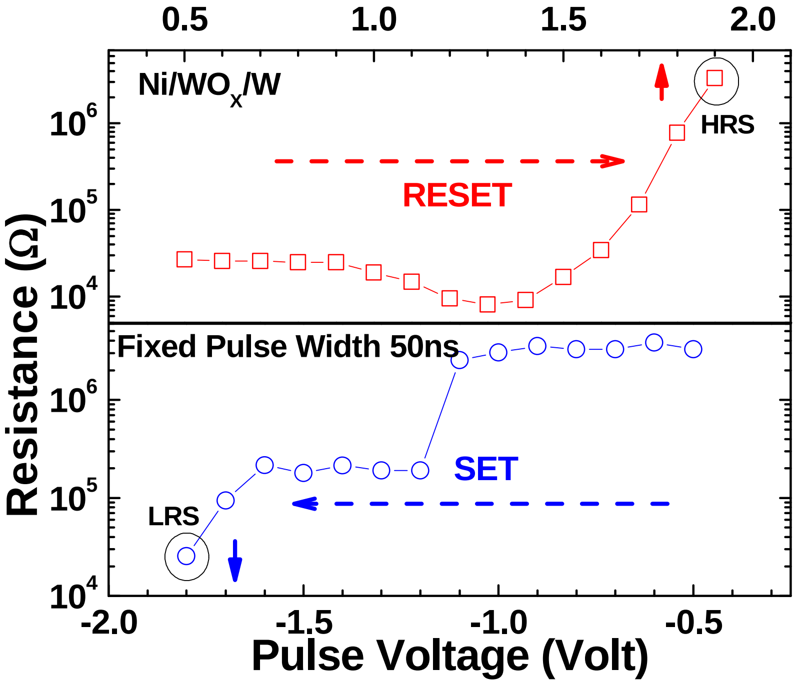


Fig. 6.31. RESET and SET pulse R-V curves for Ni/WO$_X$/W after reverse forming process.

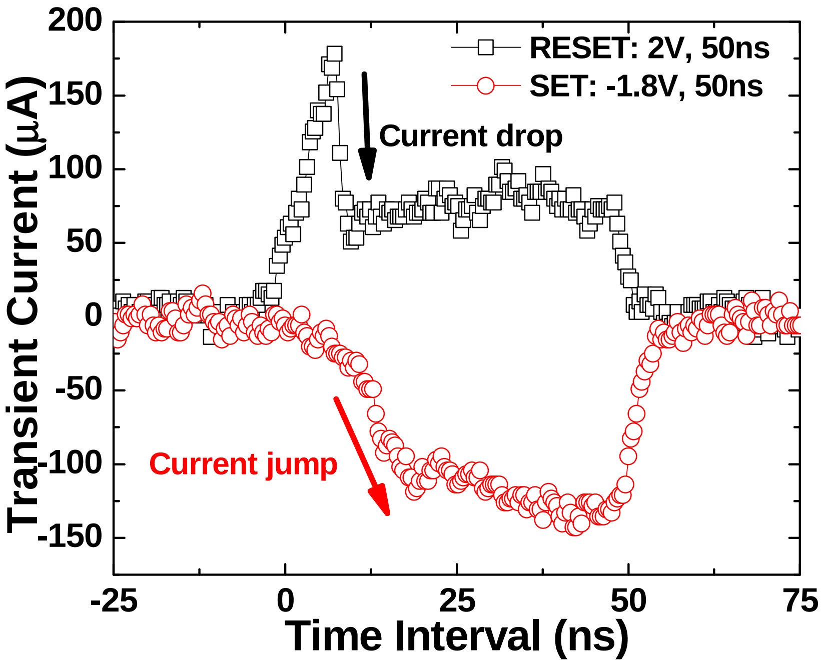


Fig. 6.32. Transient I-t curves of RESET and SET operation of Ni/WO$_X$/W cell. The RESET current is about 180uA, and SET current is about 150uA.

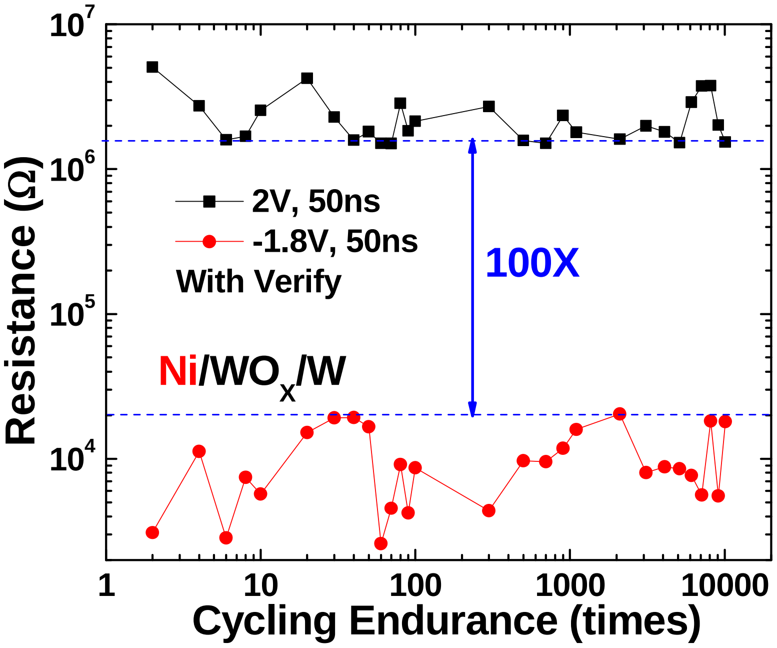


Fig. 6.33. Cycling characteristics of the Ni/WO_X/W cell. RESET/SET resistance window is well separated at 1MΩ /10kΩ for > 10k cycles.

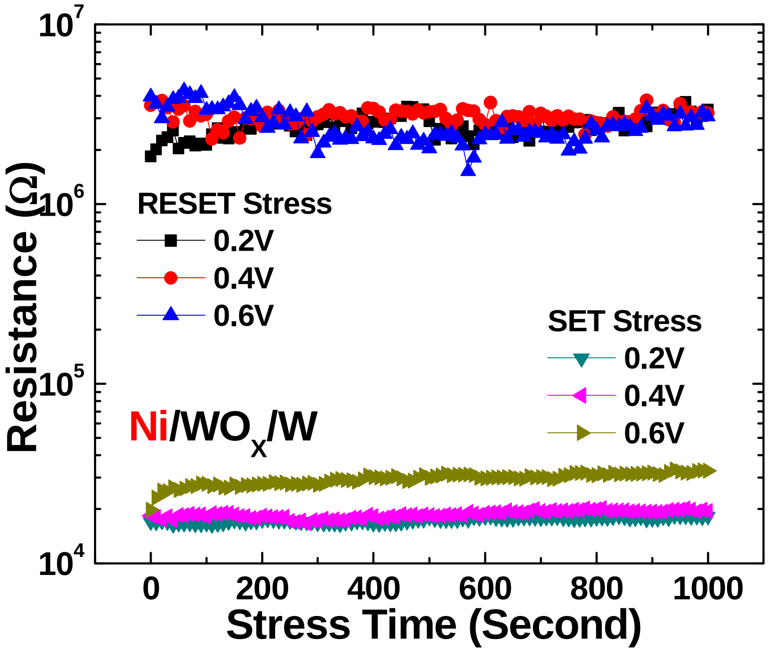


Fig. 6.34. Read disturb test. Both RESET and SET states show good read disturb resistance up to 0.6V.

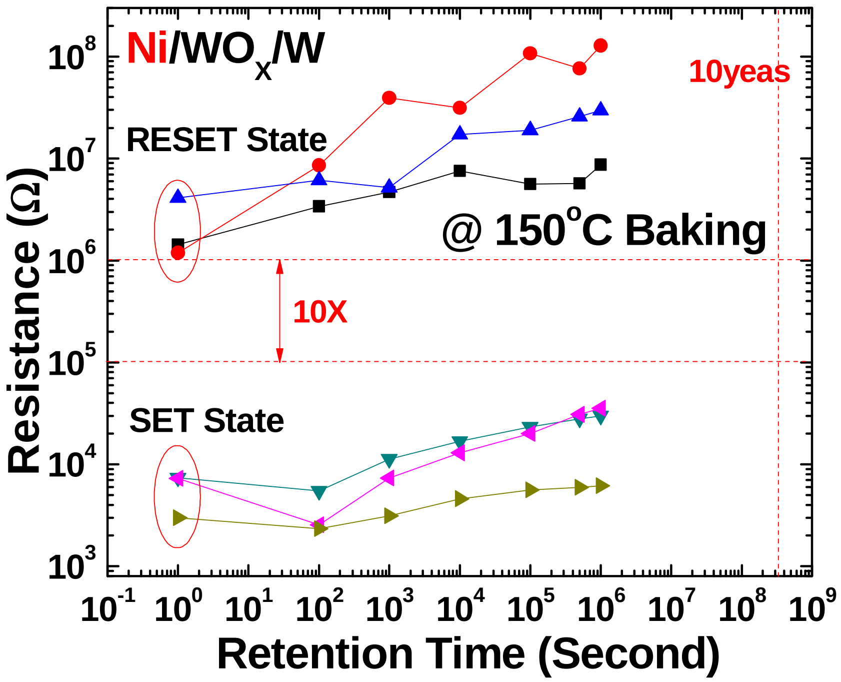


Fig. 6.35. Thermal stability test for Ni/WO$_X$/W cell at 150^{0}C. Both RESET and SET states survive well beyond 10^6 sec with at least 10X resistance window.

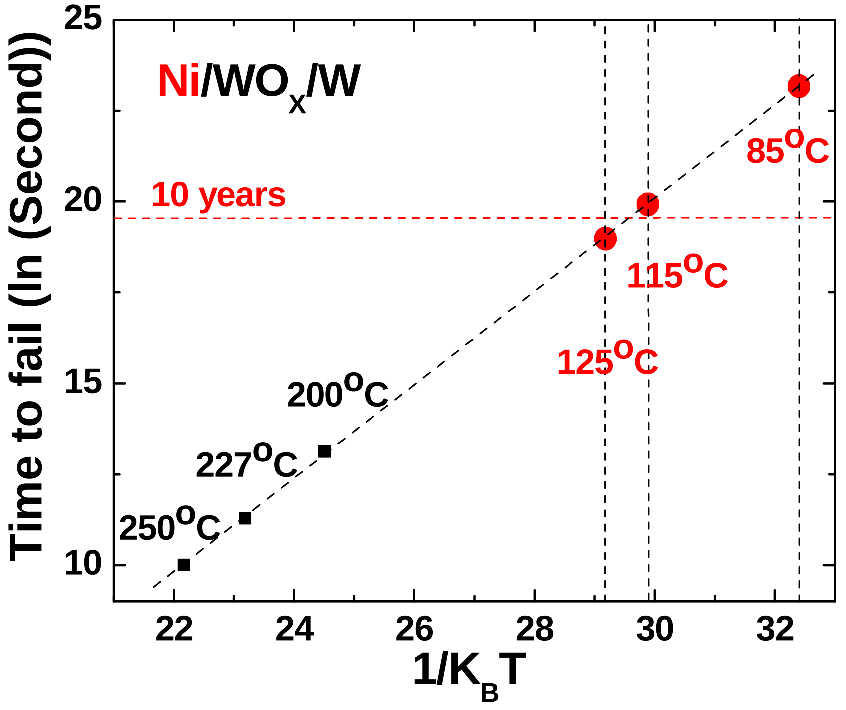


Fig. 6.36. Arrhenius plot for retention test of Ni/WO$_X$/W cell. Ea is ~ 1.34eV. The reten-tion time is 10years @115°C, and 300 years @ 85°C. The retention criteria is <100kΩ for SET .

A comparison of different electrodes is shown in Fig. 6.37. Both Ni and Pt TEs reduce the operation current from the previously proposed TiN/WO_X/W device. The Ni/WO_X/W cell shows excellent thermal stability with large resistance window. The reason for good thermal stability may be due to that the free energies of formation of W (-2.7eV) and Ni (-2.6eV) oxides are similar [82,84] therefore the driving force for degradation is low.

6.5.3 Conclusion

The WF of TE plays an important role for WO_X RRAM. The high WF Ni/WO_X/W structure shows low operation current, large resistance window, suitable endurance, good read disturbance, and excellent thermal stability.

	Forming Type	Forming current (A/cm^2)	RESET current (A/cm^2)	SET current (A/cm^2)	Resistance window	Endurance (times)	Thermal stability
TiN/WO_X /W (dia. 0.18um)	**Forming (Type I)**	**$1*10^8$**	**$3.4*10^6$**	**$3.3*10^6$**	**10k/100k (10X)**	**10^5**	**Fair, 85°C Years**
Ni/WO_X/ W(dia. 0.18um)	**Forming (Type I)**	**$7*10^6$ (reduce 10X)**	**$7*10^5$**	**$5.6*10^5$**	**10k/1M (100X)**	**10^4**	**Excellent, 85°C Centuries**
Pt/WO_X/ W(dia. 0.18um)	**Forming (Type II)**	**$1.2*10^6$ (reduce 100X)**	**$3.5*10^6$**	**$1.6*10^6$**	**10k/1M (100X)**	**10^5**	**Poor, 85°C Months**

Fig. 6.37. Comparison for TiN, Pt, and Ni/WO_X/W cells. Ni/WO_X/W cell shows promising performance for memory application with low operation current, large resistance window, and excellent thermal stability.

6.6 Summary

The microstructure and electrical properties of the WO_X based RRAM are investigated in this work. The WO_X layer is formed by converting the surface of the W plug with a CMOS-compatible rapid thermal oxidation (RTO) process. The conductive atomic force microscopy (C-AFM) result indicates that nano-scale conducting channels exist in the WO_X layer and result in a low initial resistance. Both of bipolar and unipolar operations are observed for WO_X RRAM. For bipolar operation, it shows excellent cycling endurance (up to 10^8 times) and low voltage (1.4V) with a 10X larger resistance window. The switching speed is extremely fast (~2ns), and the equivalent programming current density is ~$3x10^6$A/cm^2. Two-bit/cell operation with 10k cycle endurance and 3-bit/cell operation with more than 8k cycle endurance are demonstrated. For unipolar operation, the low programming voltage for RESET (3.3V/50ns) and fast SET speed (3V/ 300ns) are achieved along with cycling endurance greater than 10^7 times. In addition, the device is immune to read disturb. 2-bit/cell operation is also demonstrated for high density applications.

Furthermore, the electrode effects for WO_X RRAM are studied. In WO_X–base ReRAM, top electrode (TE) materials control the conduction mechanism and the forming process. In devices with a low work function (WF) top electrode, space charge limit current (SCLC) dominates the conduction mechanism, and the forming process changes the low initial resistance to high resistance. On the other hand, the conduction mechanism shifts to thermionic emission for a high WF TE, and the corresponding forming process reversely alters the high initial resistance back to low one. Based on the findings, we proposed using Ni as TE material for the WO_X ReRAM and found the new Ni/WO_X/W device has <200uA switching current, a 100X resistance window, and extremely good retention at high temperatures. The novel Ni/WO_X/W ReRAM is very promising when comparing to other ReRAMs.

CHAPTER 7

Conclusions

7.1 Summary of Findings and Contributions

The first part, the magneto impedance behaviors of pseudo spin valve and magneto tunneling junction are studied. The equivalent circuit theory can be used to analysis the AC behaviors of both PSV and MTJ. The imaginary part of magneto impedance ratio shows the huge value in the resonance frequency in PSV device 1700% at 476kHz, and MTJ device 17000% at 17.7MHz, respectively. The nano oxide layer plays a role to enhance the resistance ratio of PSV device. Thus the magneto impedance behavior for PSV device with different NOL thickness is investigated. By using this impedance analysis, the NOL property could be predicted. So, the impedance analysis is a useful technique to do non-destructive analysis for PSV device. Moreover, the bias dependence of MTJ is observed. The bias is strong affecting the resistance ratio of MTJ. Our study suggests that MTJ is potentially a sensitive sensor for high frequencies.

Tungsten oxide resistive memory had been studied, extensively. WO_X-based RRAM is attractive because it requires only one extra mask without new equipment or new material to the standard CMOS process. We applied a new RTO (rapid thermal oxidation) process to form the WO_X layer. By replacing the down stream plasma oxidation (DSPO) with this RTO process, a larger resistance window, high endurance, fast programming time and lower switching voltage have been achieved by bipolar operation for the RTO WO_X RRAM devices. Moreover, RTO WO_X RRAM is controlled not only by bipolar operation but also by unipolar operation. Using unipolar operation behavior of RTO WO_X RRAM is suitable for 3D application with a diode access device, and it also show good performance with good cycling endurance up to 10^7 times, and operation as 2bit/cell up to 9,000 times.

Besides, the study of top electrodes effect for RTO WO_X RRAM is investigated. We found that the behavior of WO_X ReRAM is a strong function of the top electrode (TE) material. The work function (WF) of the top electrode determines both the conduction mechanism and the behavior of the forming process. For a low WF electrode conduction is space charge limited (SCL), while current from a high WF electrode is dominated by thermionic emission. Thermionic emission is indicative of an interface potential barrier, and this subsequently reduces the switching and forming currents, as well as providing a larger resistance ratio. Based on these insights we have proposed and characterized a novel Ni top electrode WO_X ReRAM. The new Ni/WO_X/W device operates at <200uA switching current, a 100X resistance ratio window, and extremely good data retention of > 300 years at 85 ^{o}C.

7.2 Suggestions for Future Works

Although the WO_X RRAM shows the acceptable performance for memory application, the switching mechanism of WO_X RRAM is still unclear. Therefore, study and finding the switching mechanism is more important thing in order to further improve the RRAM technology. The switching mechanism should be divided three parts. According to the WO_X RRAM could be controlled by both bipolar operation and unipolar operation, thus it may not only one face of the switching mechanism for WO_X RRAM. What is the switching mechanism for bipolar operation, and what is the switching mechanism for unipolar operation should be considered. In last part, keep studying the top electrode effect for WO_X RRAM is useful to further clear of the conduction and switching behaviors of the WO_X RRAM. The end of the target of WO_X RRAM is finding the very good performance that could be utilized as universal memory. At the present, the performance of the WO_X RRAM is required to further improved.

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Publication List of Wei-Chih Chien

Journal papers

[1]. **“Tungsten Oxide (WO_X) Resistive Memory Using Rapid Thermal Oxidation (RTO) of Tungsten Plugs”**, Erh-Kun Lai, ***Wei-Chih Chien***, Yi-Chou Chen, Tian-Jue Hong, Yu-Yu Lin, Kuo-Pin Chang, Yeong-Der Yao, Pang Lin, Sheng-Fu Horng, Jeng Gong, Shih-Chang Tsai, Ching-Hsiung Lee, Sheng-Hui Hsieh, Chun-Fu Chen, Yen-Hao Shih, Kuang-Yeu Hsieh, Rich Liu, and Chih-Yuan Lu, **JJAP, vol. , p., (2010) (Accepted)**(SCI paper)

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