國 立 交 通 大 學

電子物理學系

碩 士 論 文

利用多層閘極之增強型應力記憶技術製作在n型金氧半場效電晶體之研究

Enhancement of Stress Memorization Technique on nMOSFETs by Multiple Strain-Gate Engineering

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摘要

在本篇論文的研究中，我們利用控制電子通道中殘留應力的技術來製作n 型金氧半場效應電晶體，電子通道中應力的主要來源是利用元件尚未定義出閘極前覆蓋一層Si_3N_4 薄膜，接著快速退火，然後去除Si_3N_4 薄膜(SPFT technique)，利用Si_3N_4薄膜本身具有的高應力特性及多晶矽內部結構改變，產生殘留的應變，進而達到改善電子遷移率的目的。此外，我們利用非晶矽及複晶矽兩種堆疊的結構加上SPFT技術製作元件，這種結構的優點主要是可以增加電子通道中應力的大小，使電子遷移率的增加幅度能夠更加顯著，我們發現同時利用閘極堆疊結構及這種方式可以有效提昇元件的電導達24%。以上所有的元件部份，最後皆有附加一層接觸孔蝕刻停止層(CESL)，使得這項技術可以廣泛的使用在製程內而不會有應力減小的效果。我們相信利用控制電子通道中應力的大小來改善電流驅動能力在未來CMOS 元件技術的發展上將扮演非常重要的角色。

Enhancement of Stress Memorization Technique on nMOSFETs by Multiple Strain-Gate Engineering

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Abstract

An enhanced stress memorization technique (SMT) has been demonstrated by multiple strain-gate engineering that utilizes strain proximity free technique (SPFT) and a stacked a-Si/poly-Si gate structure. It is found that the transconductance (G_M) of nMOFETs with SPFT exhibits an 18% increase compared to that of counterparts. The SPFT can prevent the limitation of stressor volume for performance improvement in high density CMOS circuits. We also found that the optimization of stacked a-Si/poly-Si gate structure and combine with the SPFT can improve the G_M further to 24% more than the single-poly-Si gate structure without SPFT.

誌謝

首先我要特別感謝指導教授趙天生博士的指導與教誨，受教於趙教授這兩年期間，讓我在獨立思考及專業知識上都有所成長，期間有好幾次遇到挫折，幸好有老師的鼓勵讓我更能勇敢面對問題，謝謝老師對我的細心指導與鼓勵，在此致上我最高的敬意。

此外，我也非常感謝呂宗宜學長在專業知識給我的一切協助與指導，同時也感謝陳建豪、郭伯儀、吳偉成、馬鳴汶、羅文政、楊宗諭、高國興、邱德馨、劉美君、猴子、妍心、阿壘等學長姐在這段期間給我的關懷與協助，在我論文及實驗上有疑惑時常常給予解惑，在此表達我的感激。特別感謝與我一起走過這段日子的研究夥伴，宗育、冠迪、威良、廖俊、翊鴻、榮家以及實驗室的學弟妹們，感謝他們這段時間的陪伴與鼓勵，有了你們讓我感到實驗室時常充滿歡笑聲，使我更有動力邁向研究的動力，別忘了以後有空時候在一起打球及唱歌。

特別感謝心頤小姐在這些年來對我的關懷與扶持，謝謝她一路陪我走過漫長的求學生涯並陪我渡過重重難關，最後僅以此論文獻給我敬愛的母親以及家人，感謝他們在我一度迷失人生方向時扶持我繼續向前，支持與鼓勵我順利完成學業。

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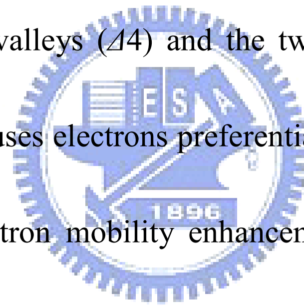
Chapter 1

Introduction

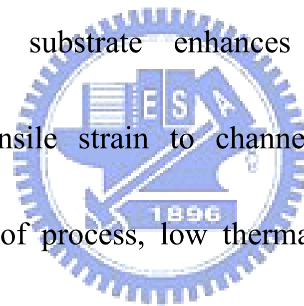
1-1 General Background

In order to realize higher speed, lower power and higher packing density metal oxide semiconductor field effect transistor (MOSFET) integrated circuit, the semiconductor device manufacturing process technique has already exceeded into nano-generation. As the devices gate length geometric scaling down, the short channel effect will be serious and increases the gate leakage current, and would also increase the Sub-threshold Swing (S.S) etc. To solve this problem, the higher dielectric constant (High-K) material [1-3] is used to replace traditional silicon dioxide to become MOSFET gate layer. By using high-k material as a dielectric layer, we can make thickness several times of silicon dioxide and make gate leakage current smaller. However, these high-k materials have many problems in traditional CMOS processes. Therefore, some possible solutions for solving CMOSFET scaling limits have been developed. The strain technique, for enhancements of electron- and hole-mobility, is the most popular one among these solutions. In brief, the strain technique is using manufacturing processes and materials to make stress in silicon channel. It has been reported that the carrier mobility in CMOS can be improved by using strain technology on the strain silicon [4-5].

Theoretical calculations indicate that Si strained in biaxial tension possesses higher mobility than bulk silicon [6-10]. The electron transport in strained Si will be explained following. For electron transport in bulk Si, the conduction band is comprised of six degenerate valleys, as shown in Fig. 1-1(a). For unstressed bulk Si, the total electron conductivity mass, *m**, is obtained by adding the contributions of degenerate six degenerate valleys and is given by $m^* = [1/6\ (2/m_l) + (4/m_t)]^{-1}$, where m_l is the longitudinal mass = 0.98 m_0, and m_t is the transverse mass = 0.19 m_0.With the application of strain, the tensile strain in nMOSFETs induced the valence band splits into the four in-plane valleys ($\Delta 4$) and the two out-of-plane valleys ($\Delta 2$), as shown in Fig. 1-1(b). This causes electrons preferentially populate the $\Delta 2$ band which is lower in energy. The electron mobility enhancement due to intervalley phonon scattering between the $\Delta 2$ and $\Delta 4$ valleys can be reduced and in-plane effect mass in the band can be reduced too. For holes, the valence-band structure of Si is more complex than the conduction-band. For unstrained Si at room temperature, holes occupy the top two bands, the heavy- and light-hole bands. With the application of strain, the hole effective mass becomes highly anisotropic due to band warping, and the energy levels become mixtures of the pure heavy, light, and split-off bands. In order to get higher hole-mobility, the biaxial tensile stress provides a low in-plane conductivity mass and reduces inter-band scattering, as shown in Fig. 1-2.

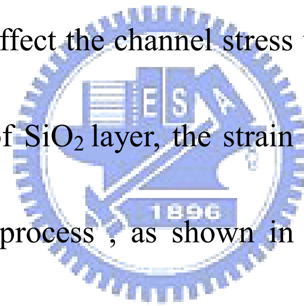


By using strain technology, many methods can be used to improve electron and hole mobility, such as Ge or SiGe epitaxy in channel [11-12]，different substrate orientation (110) or (111) [13-15], and process induced strain [17-21]. For example, Si and Ge are miscible and lattice mismatch of about 4.2%, which can effectively provide strain in local channel region. When a thin film with a large constant ($Si_{1-x}Ge_x$) grown on a substrate of silicon, the film retains the in-plane lattice constant of the substrate and is under a biaxially compressive strain. On the contrary, with epitaxy a Si thin film on Ge or $Si_{1-x}Ge_x$ substrate [16], the film can get a biaxially tensile strain. Biaxial compressive strain substrate enhances hole-mobility, but degrades electron-mobility. Biaxial tensile strain to channel enhances electron and hole mobility. However, the cost of process, low thermal budget and some production problems still need to be solved appropriately.



Process induced strain has been used to produce uniaxial strain. Several approaches such as silicon nitride (Si_3N_4) capping layer [17], shallow-trench isolation(STI) [18], silicidation processes [19], and embedded SiGe S/D [20] or SiC S/D [21] have been utilized to realize the local strain. Recently, stress memorization technique (SMT) has been reported to enhance electron-mobility on nMOSFETs and widely studied by different methods [22-24]. This process induced strain technique has been developed to use the polycrystalline silicon gate as a stressor to generate

tensile strain in the nMOSFETs silicon channel. Ota et al. reported significant strain-related nMOSFETs performance improvement from residual stress [25], as shown in Fig. 1-3. The strain process was executed after arsenic implantation at source/drain regions. This implantation step could change the polysilicon gate and S/D Si into amorphous silicon. Then, a tensile SiO_2 layer (PECVD) was deposited on the polysilicon gate and S/D regions. Wafers were then annealed the device at a high temperature and stripped the stressed film. The observed performance improvement of devices was attributed to the channel strain. The stress effect was found to be enhanced and memorized to affect the channel stress underneath the re-crystallization poly-Si gate. After removal of SiO_2 layer, the strain was memorized in place by the polysilicon re-crystallization process , as shown in Fig. 1-4. A new strain booster named as Dopant Confinement Layer technique (DCL) that is novel Stress Memorization Technique has been reported [26], which is added on the conventional CMOSFET structure, as shown in Fig. 1-5. Gate electrode is fabricated as follows: 1st Si deposition, implantation to pMOSFETs, implantation to nMOSFETs, 2st Si deposition, and gate etching. After S/D regions were implanted, dopants were activated by using a spike annealing. After this process, a strong residual strain was added to the channel region at the same time.



1-2 Motivation

As the scaling of design rule such as poly-pitch is shrunk for high density logic circuits, mobility enhancement will be limited by stressor volume and process integration issues. One of the critical challenges in the integration of dual-stressed overlayers into a logic CMOS technology is the patterning and dedicated removal of the stressed material. Optimized layer stacks and dedicated etch processes have to be used to avoid patterning problems [27], as shown in Fig. 1-6. Another problem we meet is the longitudinal tensile stress will be limited as the stressor volume reaches its saturation point (as shown in Fig. 1-7), and even caused the performance degradation [28]. In this work, we propose a novel strain proximity free technique (SPFT) to prevent the limitation of stressor volume for performance improvement in high density CMOS circuits. Stacked a-Si/poly-Si gate structure has been reported to enhance channel stress and electron mobility. We also demonstrated that the stacked gate structure with optimization of a-Si/poly-Si thickness can further improve the performance on nMOSFETs.

1-3 Thesis Organization

This dissertation is divided into four chapters as follows:

In chapter 1, a brief general background of strained Si devices is introduced to describe the various characteristics. Then we discuss recent studies in local strained

channel devices with stress memorization technique (SMT) and motivation of our study.

In chapter 2, we report the process strain proximity free technique (SPFT) and stacked a-Si/poly-Si gate structure for fabricating n-channel metal oxide semiconductor field effect transistors.

In chapter 3, we demonstrate the characteristics of strain proximity free technique devices and Si_3N_4 capping layer. The improvement of electron mobility is turn out by elevating strain in the channel region. Moreover, we found that the strain dependence of mobility enhancement will become significant by using both SPFT and stack of *a*-Si gate structures. Then we discuss the important issue while we attempt to enhance carrier mobility by introducing strain in the channel region on device fabrication.

In chapter 4, we summary our experimental results and give a brief conclusion. Recommendations are also given for further study.

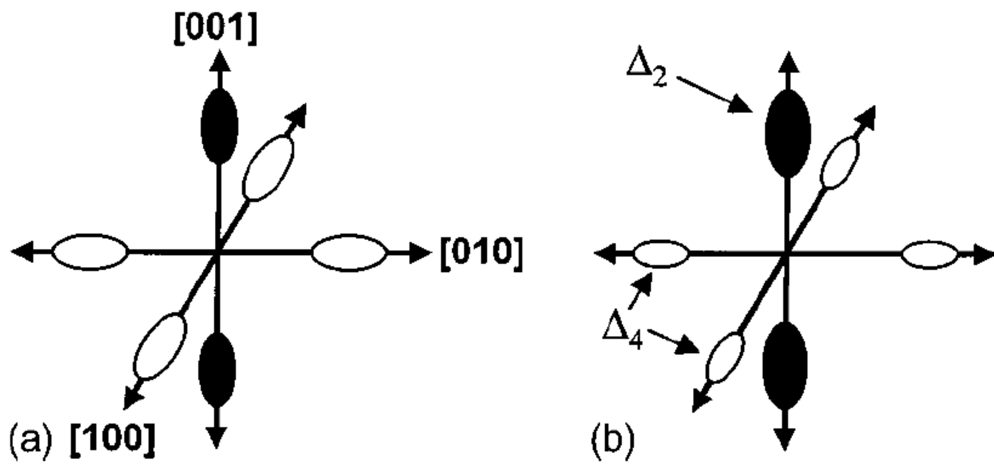


Fig. 1-1 Conduction-band structure of (a) bulk Si and (b) strained-Si.[10]

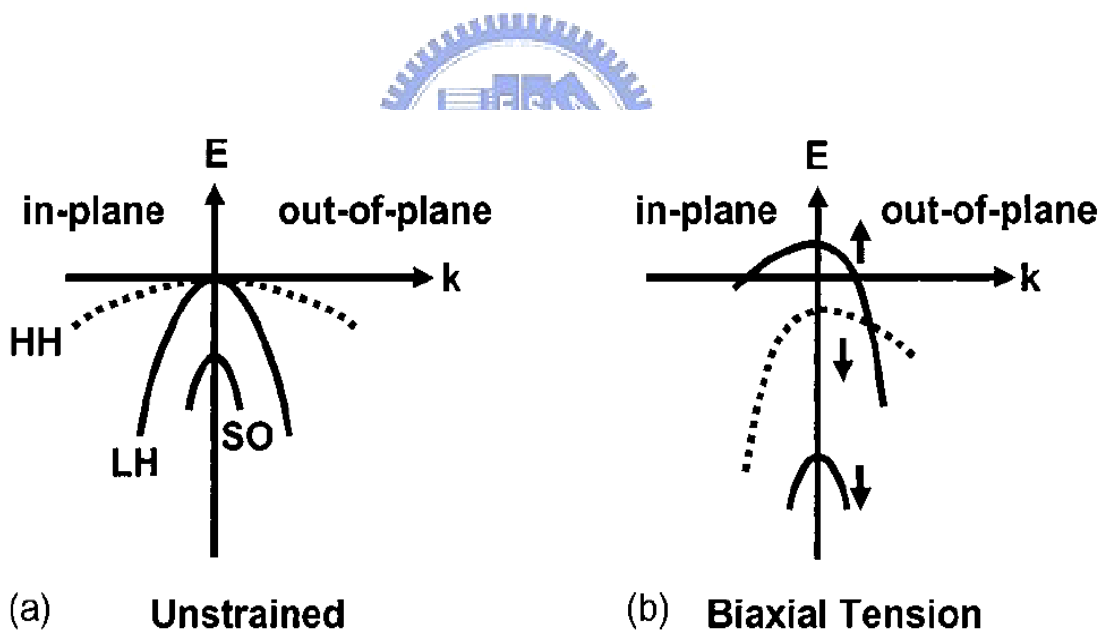


FIG. 1-2 Valence band of (a) bulk Si and (b) Si under biaxial tension.[10]

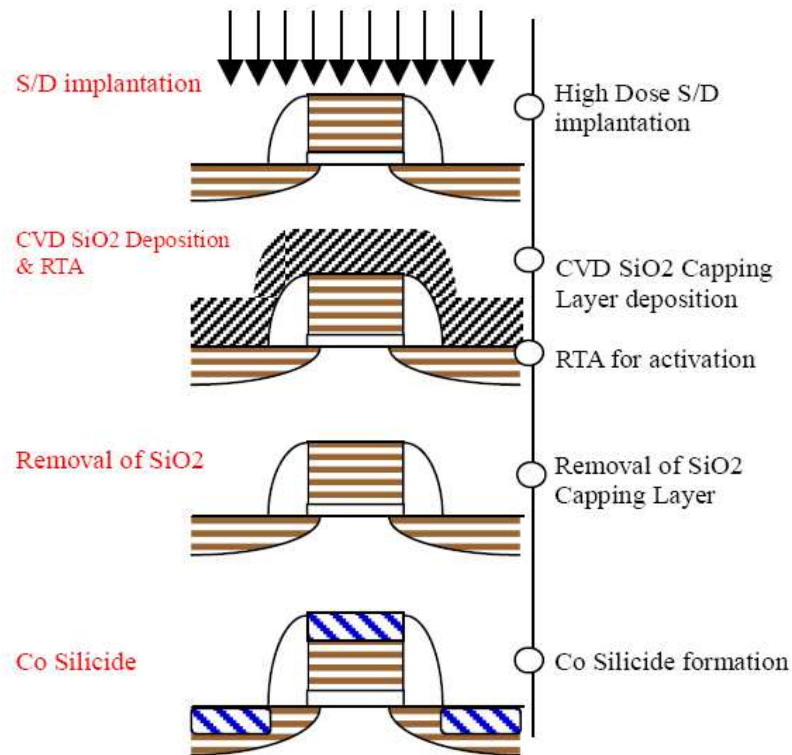


Fig. 1-3 Fabrication process for locally strained channel transistor.[25]

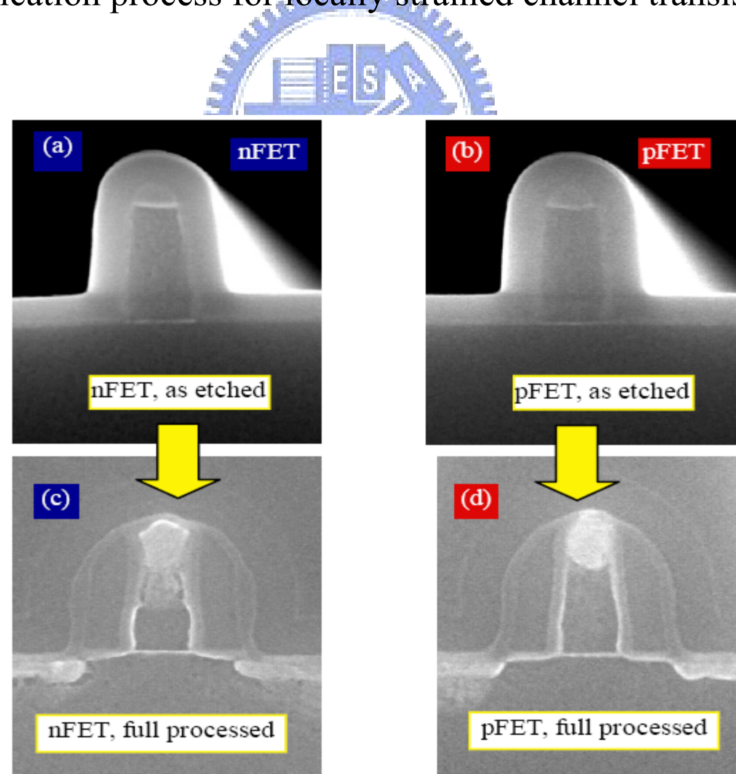


Fig. 1-4 The cross sectional SEM images and stress distributions of nFET and pFET. [25]

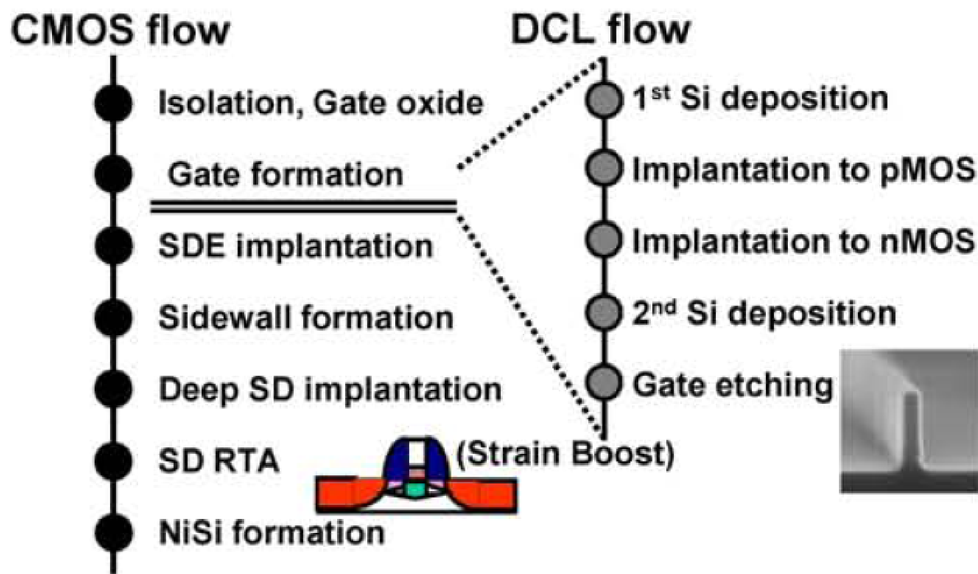


Fig. 1-5 (a)Schematic illustration of process flow of CMOSFET with DCL technique.[26]

E S A

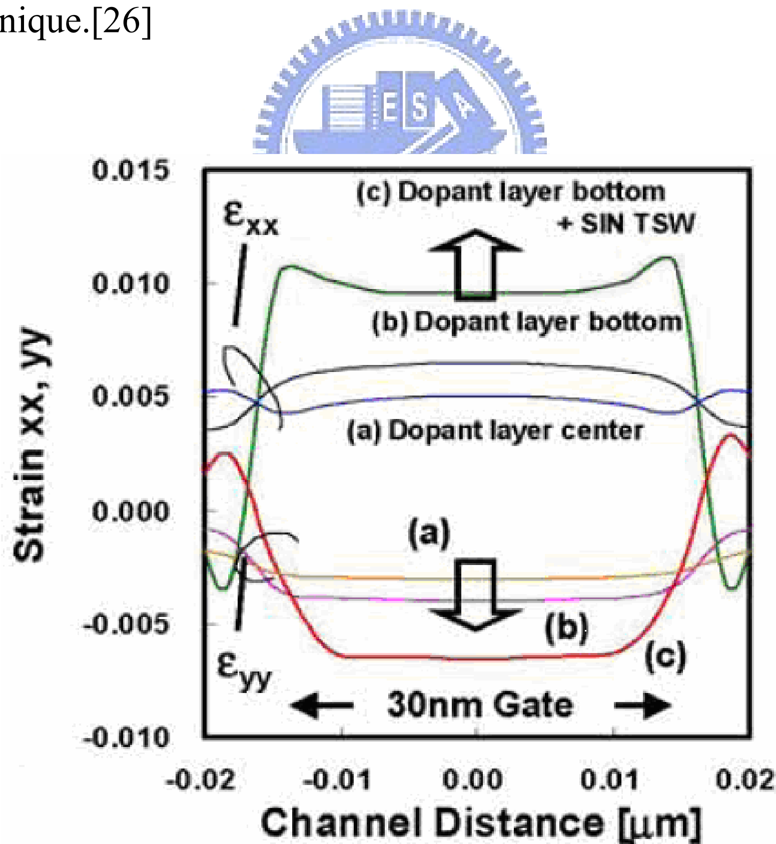


Fig.1-5 (b)Stress simulation results (vertical strain yy) of nMOSFETs .[26]

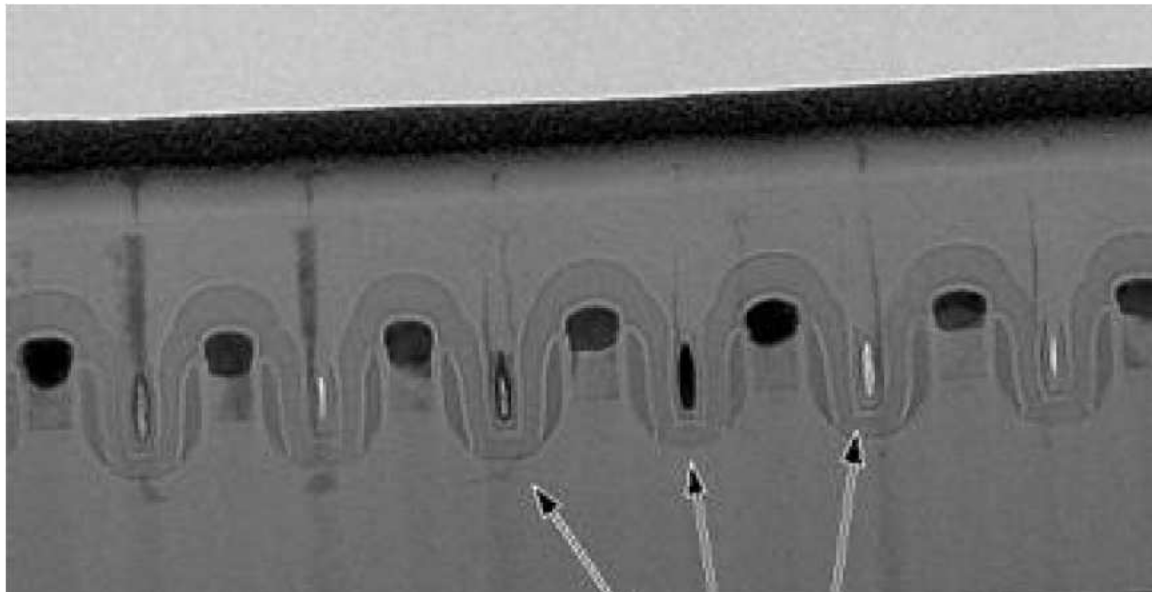


Fig. 1-6 Voids in the dense poly regions on STI can lead to shorts in the circuitry, when filled with tungsten contact material.[27]

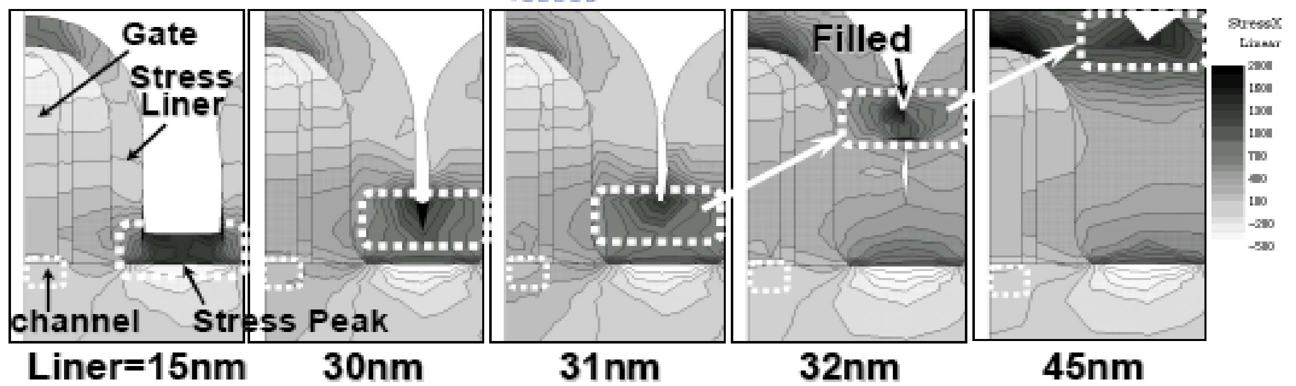


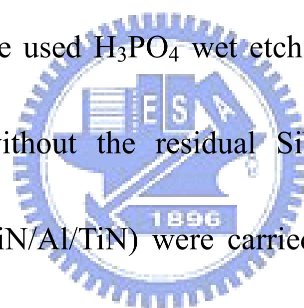
Fig. 1-7 Sxx distribution dependence on stress liner thickness. Stress peak position goes up once gate space is filled and channel region stress is decreased rapidly.[28]

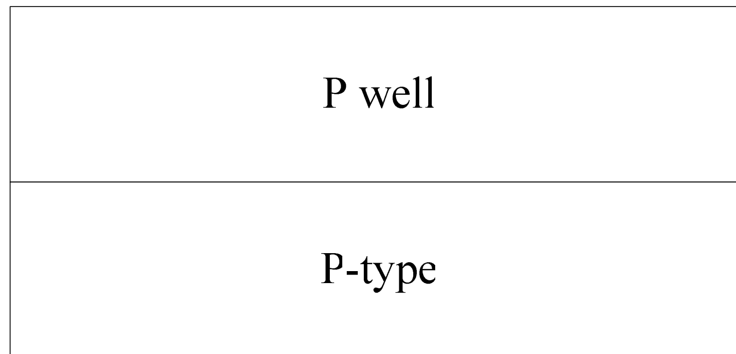
Chapter2

Device fabrication

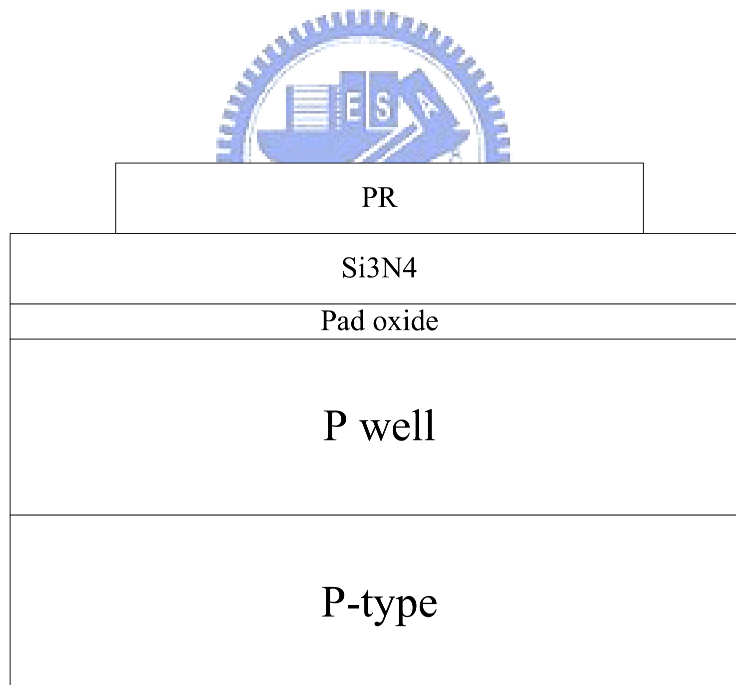
The process flow is illustrated in (1) ~ (13). After BF_2 implantation for p-well region, CVD SiO_2 for oxidation enhanced diffusion (OED) in well drive-in process. Active region alignment followed pad oxide and Si_3N_4 deposition. After Si_3N_4 was etched, BF_2 implantation for the stack of channel stopped. Then, field oxidation was carried out in the high temperature ambient for LOCOS isolation. Two sacrificial oxide deposition followed Si_3N_4 removal process was executed to eliminate Kooi effect. Then, threshold voltage adjustment from arsenic implantation and phosphorus implantation was performed in order to anti-punch through. After RCA cleaning process, 25Å gate oxide was carried out in vertical furnace (800°C,O_2 ambient). Amorphous silicon (a-Si 550 ^{o}C,500-700Å) and in-situ doped n^+ poly-Si were deposited in the same ambient followed by gate oxide. The total thickness of poly-gate for all samples is 2000Å. The process flow of SPET is included by high tensile stressor deposition (Si_3N_4 1500Å), rapid thermal annealing 1050 ^{o}C and remove Si_3N_4. Then, poly-Si and a-Si etch followed gate alignment process. After sidewall polymer removal, source/drain extension implantation, sidewall spacer and S/D (As, 15kev, 5E15) formation are processed. Rapid thermal annealing was carried out in nitrogen ambient at 1050 ^{o}C for 10 seconds followed p+-substrate implantation

(BF_2, 50 kev, 2.5E15). Thermal CVD Si_3N_4 layer (at 780 °C) with 1000Å was directly on all the transistor and followed by TEOS (at 700 °C,4000Å) deposition. After contact alignment, TEOS and Si_3N_4 etch were carried out in the same system. This step is the key to this experiment. First, we used the dry etching process to remove the upper TEOS and dipped in BOE solution to confirm that the remnant TEOS was completely removed. Then, we used another recipe to etch the lower Si_3N_4 layer in the same system. In order to protect the Si surface without plasma etching damage, Si_3N_4 layer was etched in two-step. We calculated the Si_3N_4 etching rate and kept 200Å after dry etching process. Then, we used H_3PO_4 wet etch solution over-etching (20%) to confirm the contact hole without the residual SiN layer. After this processes, four-level metallization (Ti/TiN/Al/TiN) were carried out in PVD system and final alignment was followed this step. Etching metal process, annealing in a H_2 / N_2 ambient at 400 °C for 30 minutes was performed in order to mend dangling bonds and reduce interface state density in oxide/Si interface.

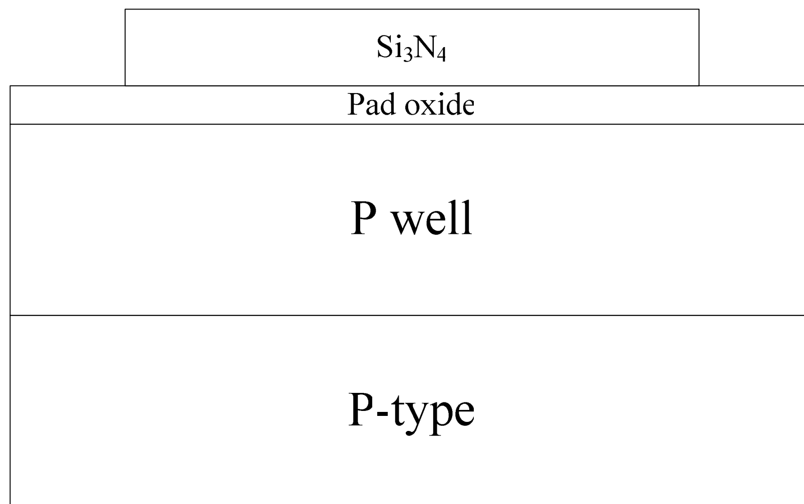




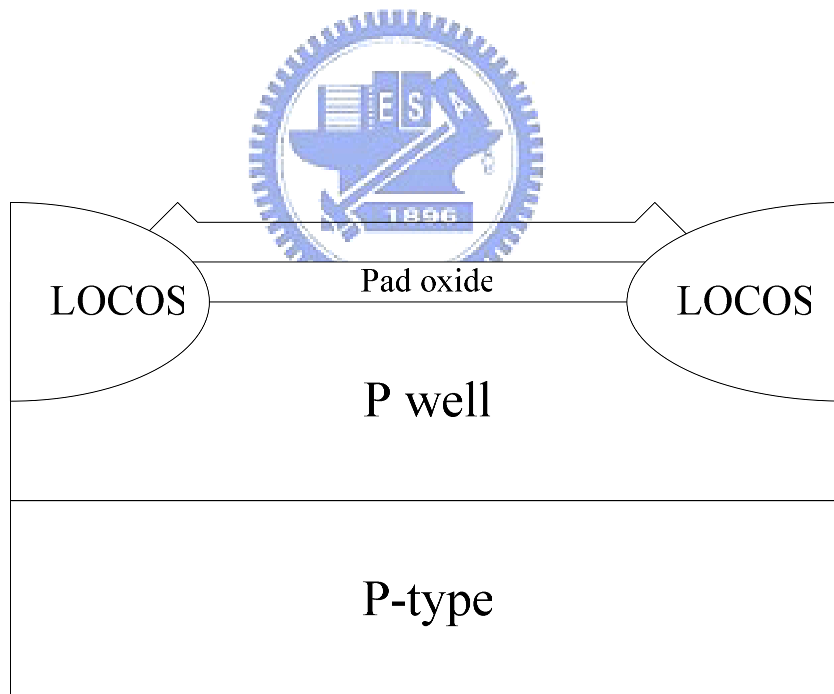
(1) P-well implant (S:BF_2 / E:70kev /D:1.2E13) and APCVD SiO_2 for well drive in.



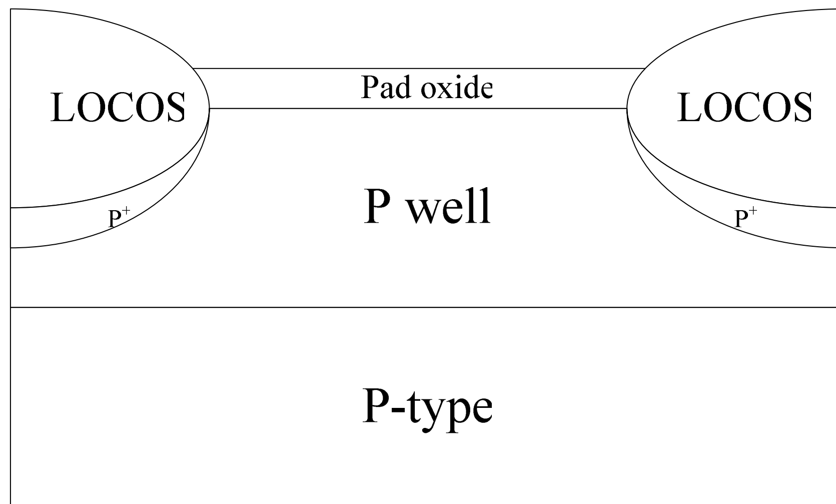
(2) Active region alignment after pad oxide and nitride deposition.



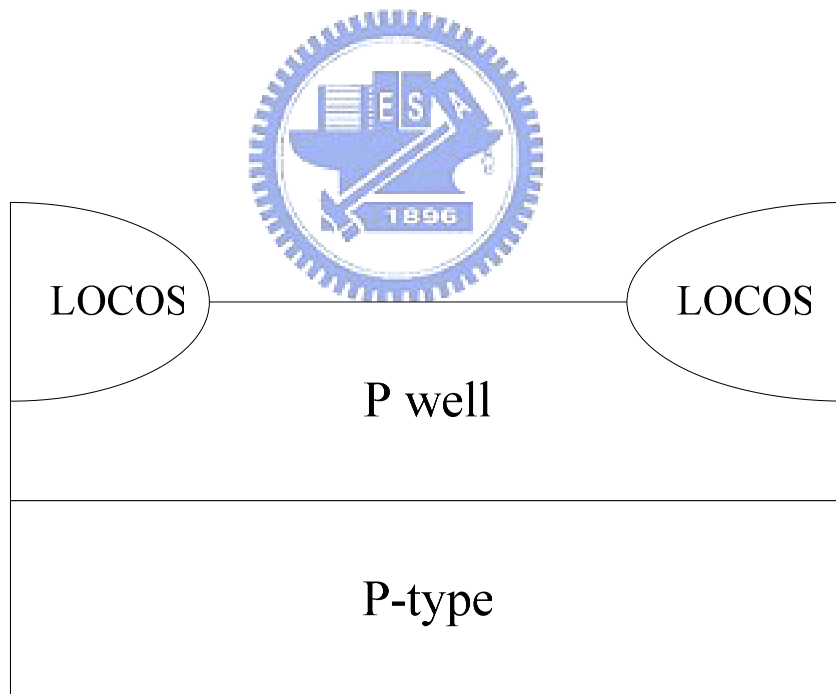
(3) Si_3N_4 etch.



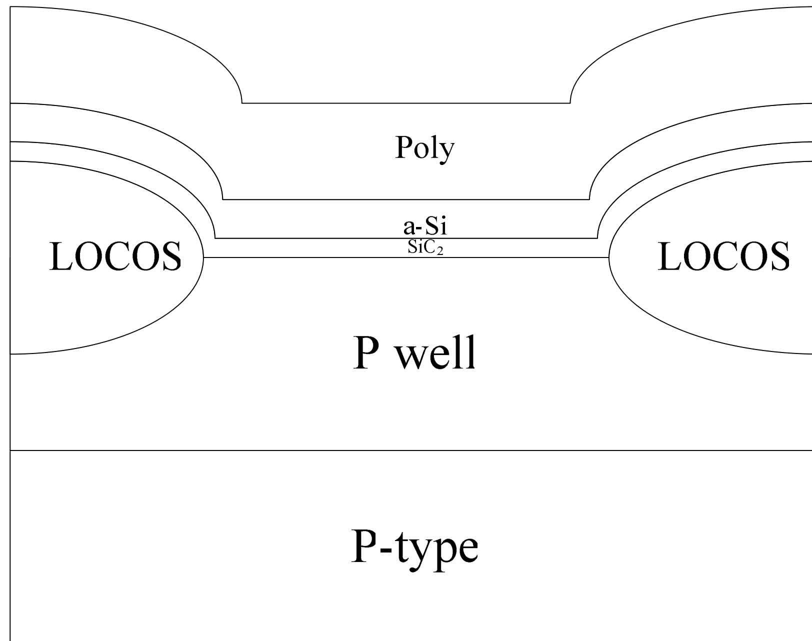
(4) Field oxide grow 5500A with 980°C and channel stop implant (S:BF_2 / E:120kev /D:4E13).



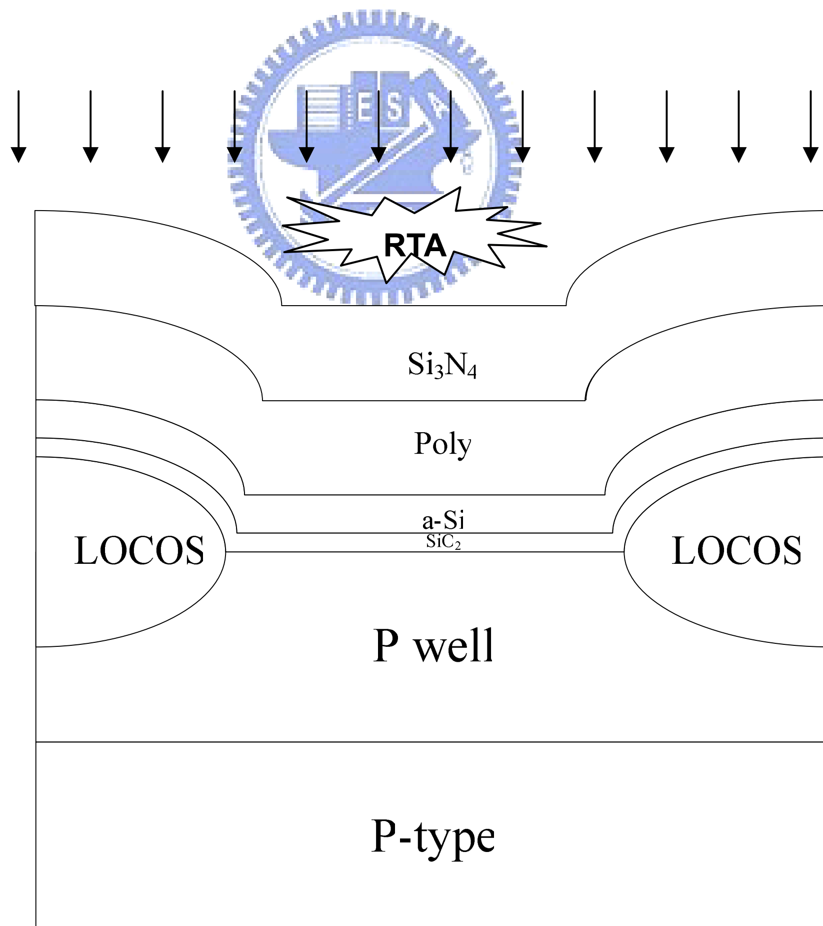
(5) Sac. Oxide (wet oxide 925 °C 300Å) for eliminating Whit Ribbon effect.



(6) Nitride remove, Vt implant (S:BF_2 / E:80kev / D:1E13) and P-APT implant (S:B / E:45kev /D:4E12).

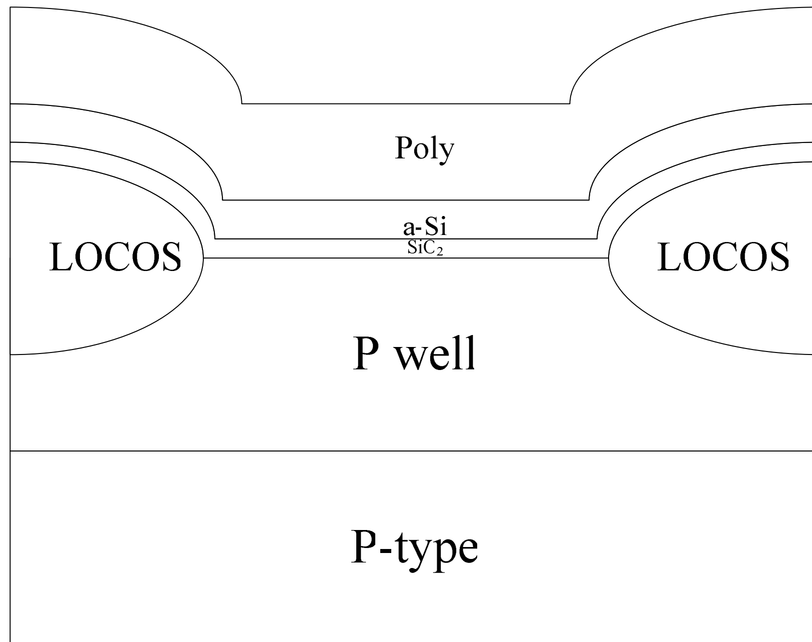


(7) SiO_2 (25Å), gate deposition (split:poly-2000Å /a-Si-500Å +poly-1500Å / a-Si-700Å +poly-1300Å).

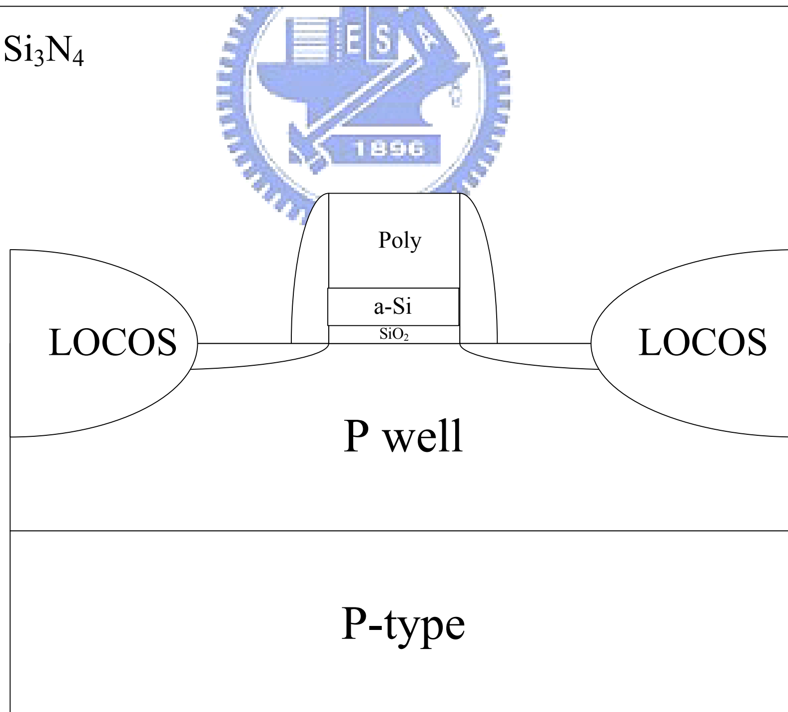


(8) Split for SPFT process: Poly Amorphorization Implant (S:As / E:10kev / D:1E15) + Si_3N_4 1500Å +RTA 1050°C.

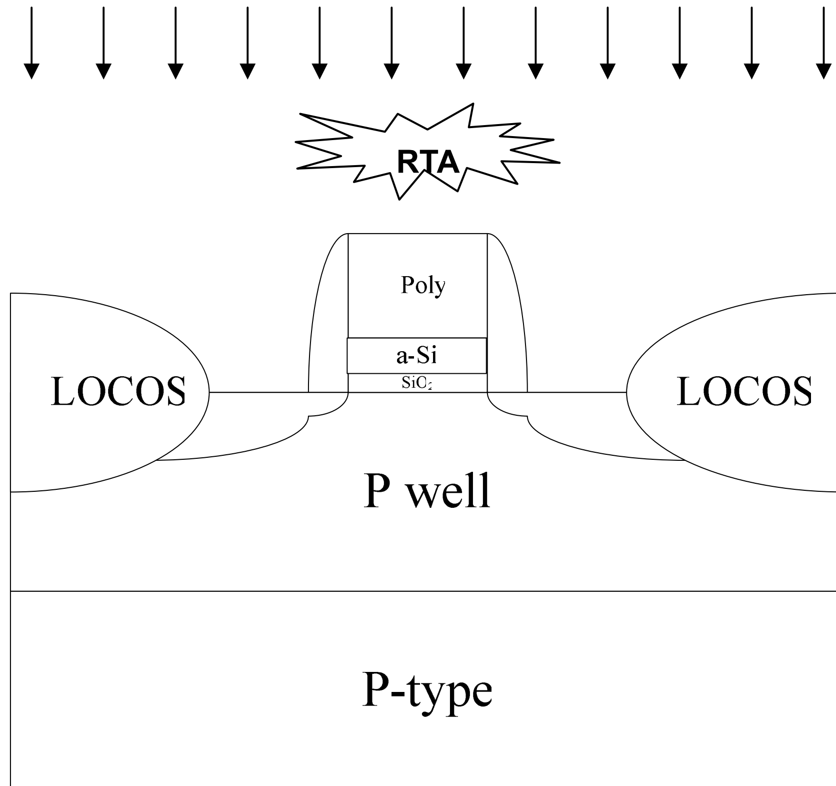
(9)



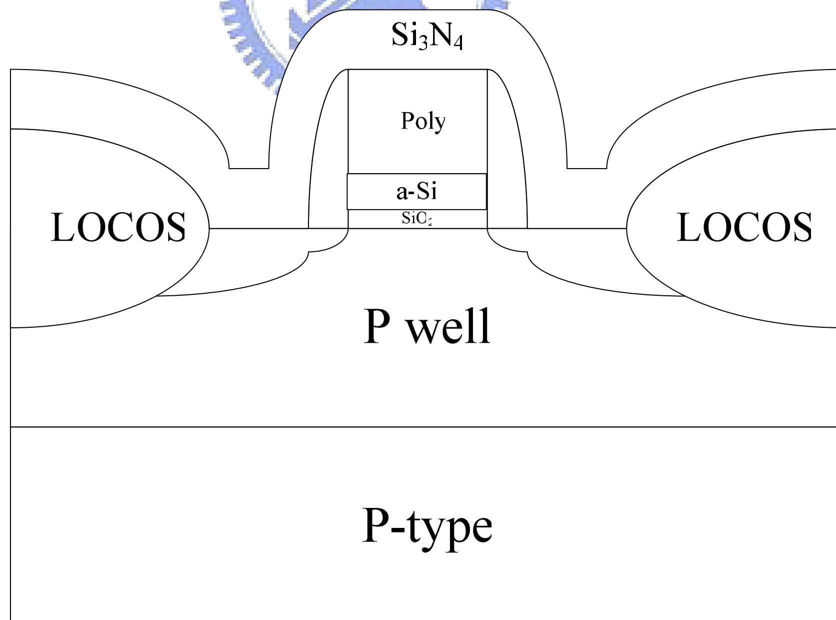
(9) Remove Si_3N_4



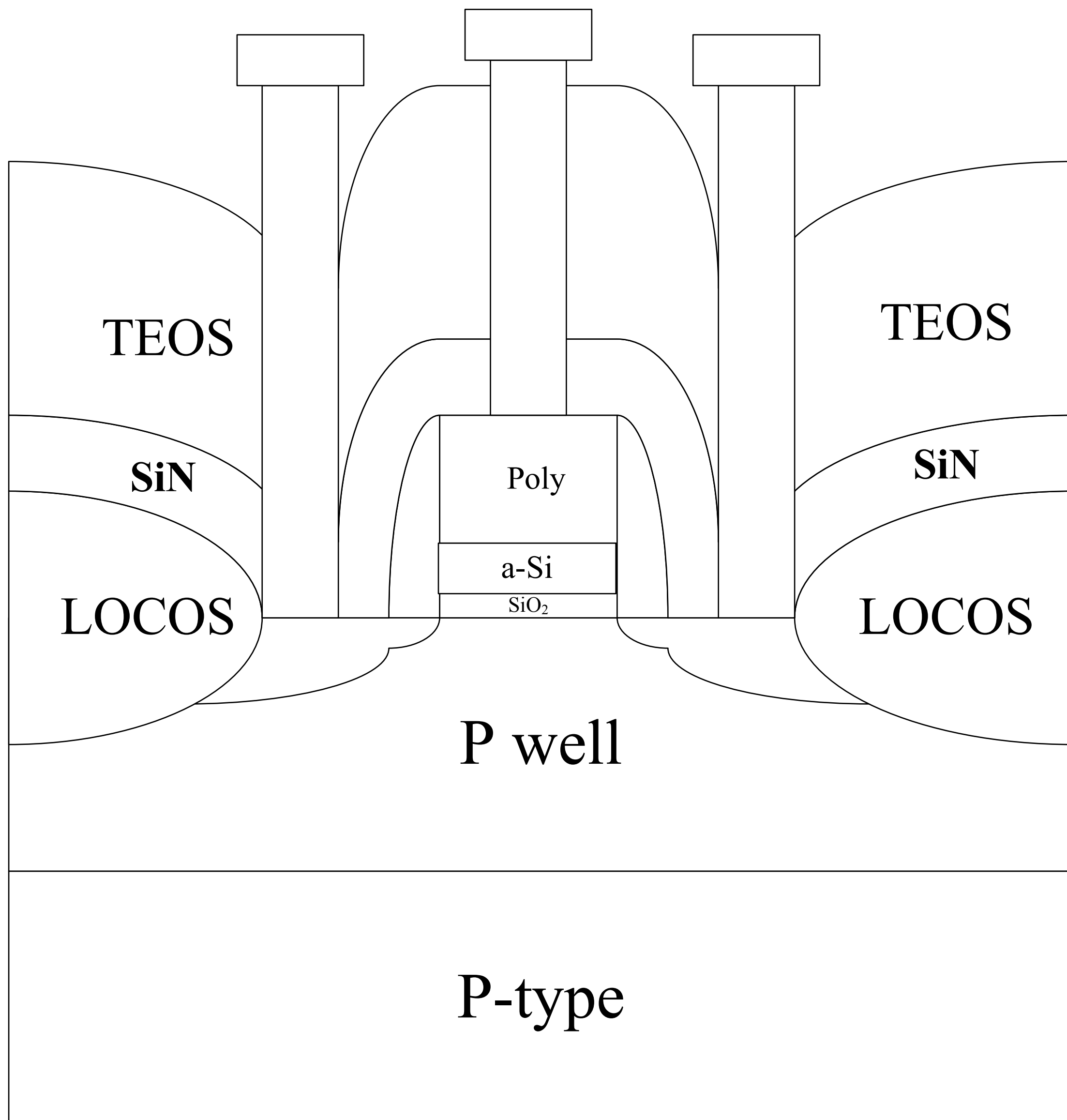
(10) Spacer and LDD implant (S:As / E:10kev / D:1E15).



(11) S/D implant (S:As / E:15kev / D:5E15), RTA anneal (1050°C 10sec).



(12) Contact Etch Stop Layer (LP Si_3N_4 1000Å).



(13) Passvation deposit (TEOS 4000Å) and four-level metallization.

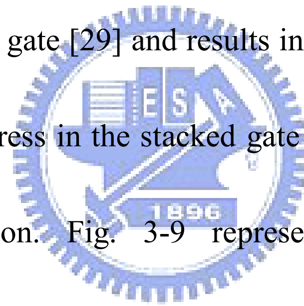
Chapter 3

Results and Discussion

3-1 Summary of stacked a-Si/poly-Si gate structure

In this section, we would introduce the strain effect of the stack of a-Si and poly-Si gate structure. nMOSFETs with three different structures has been fabricated as shown in Table I and Fig. 3-1. In Fig 3-2 illustrates a measured C-V profile with different gate structures with fixed thickness of Si_3N_4 capping layer (CESL 1000Å). The accumulation capacitances in long channel devices (100 μm) are almost the same as that of the conventional devices and the EOT is about 26.5Å. The dependence of Id-Vg characteristics was measured at Vd = 0.1V on different thickness of amorphous (a-Si) layer are shown in Fig. 3-3. The dependence of Id-Vg characteristics is measured at Vd = 1V on different thickness of a-Si layer is shown in Fig. 3-4. The improvement of current (linear curve) drivability is in proportion to thickness of a-Si and would not decrease Ioff current in all samples. Fig. 3-5 and Fig. 3-6 show the threshold voltages (measured at Vd = 0.1V or Vd = 1V) of the device with a-Si layers of different thicknesses. The threshold voltage is proportional to the thickness of a-Si layer. The a-Si stack layers increasing that Vth is small than control sample. We conjecture this is related to the bandgap narrowing effect caused by the channel strain [39]. Fig 3-7 indicates there are no significant differences of DIBL (Drain Induced

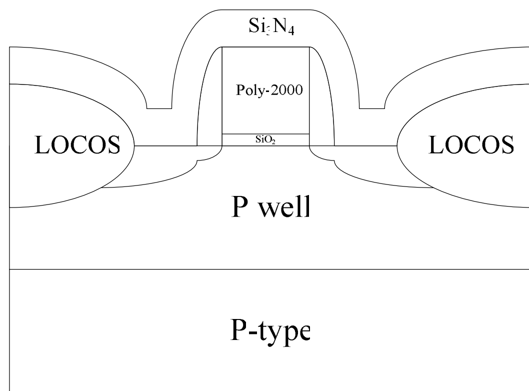
Barrier Lowing) effect among all samples. Fig. 3-8 shows the transconductance (Gm) increases with the increase of thickness of a-Si layer. The a-Si-700/poly-Si sample can improve 14.5% compare to control sample in the channel length at 0.4μm. This result implies that the strain dependence on mobility enhancement by stack of a-Si gate structure. The mechanism of the stress elevation could be as follows: before the dopant activation process, the stacked gate is in amorphous phase due to the bottom a-Si and high dose implantation of arsenic on top of poly-Si. The recrystallization of amorphous region during the rapid thermal annealing step leads to the shrinkage of total thickness of stacked a-Si gate [29] and results in the residual compressive stress. Therefore, the compressive stress in the stacked gate provides additional high-tensile strain to the channel region. Fig. 3-9 represents the a-Si-500/poly-Si and a-Si-700/poly-Si samples compare to the control sample Poly-2000 that the Gm enhancement percentage with different channel length. We can see that the Gm enhancement reaches 8 ~ 12% at the channel length between 1um to 0.4μm in the a-Si-500/poly-Si sample. For the a-Si-700/poly-Si split, it is seen that the Gm enhancement reaches 14 ~ 17.5%. The dependence of output characteristics on different thickness of a-Si layer is shown in Fig. 3-10. The drain current of nMOSFETs with a-Si-700/poly-Si showed 12% and a-Si-500/poly-Si shows 6% increased compare to the poly-Si at a channel length of 0.4 μm. Fig. 3-11 represents



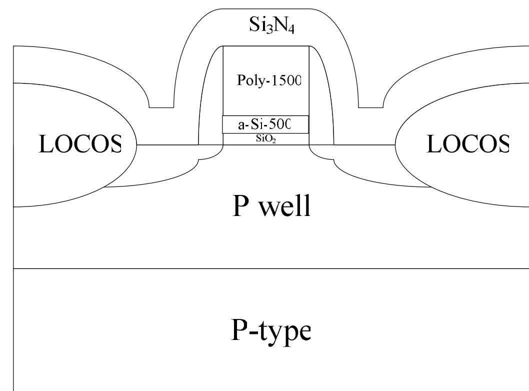
a-Si-700/poly-Si sample that the drive current enhancement reaches 10~15% and a-Si-500/poly-Si enhancement reaches 5~9% compared to the control sample at the channel length between 1um to 0.4 μm. It is very interesting since the improvement of current drivability and Gm increase as thickness on a-Si layer is increased. This may be due to the thicker a-Si layer when re-crystallization during rapid thermal annealing provides more residual tensile strain than thin a-Si layer in the channel region.

Si_3N_4-capping layer / Gate structure	Si_3N_4 1000Å
Poly-2000	**V**
a-Si-500/Poly-1500	**V**
a-Si-700/Poly-1300	**V**

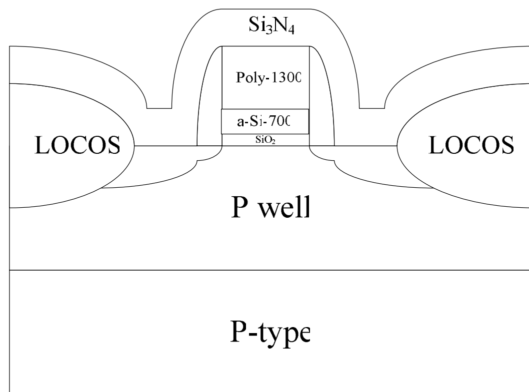
Table. I Gate structure with fixed Si_3N_4 for local strained channel devices.



(a)Poly 2000



(b)a-Si-500/Poly1500



(c) a-Si-700/Poly1300.

Fig. 3-1 Gate structure with different condition (a)Poly 2000 (b)a-Si-500/Poly1500 (c) a-Si-700/Poly1300.

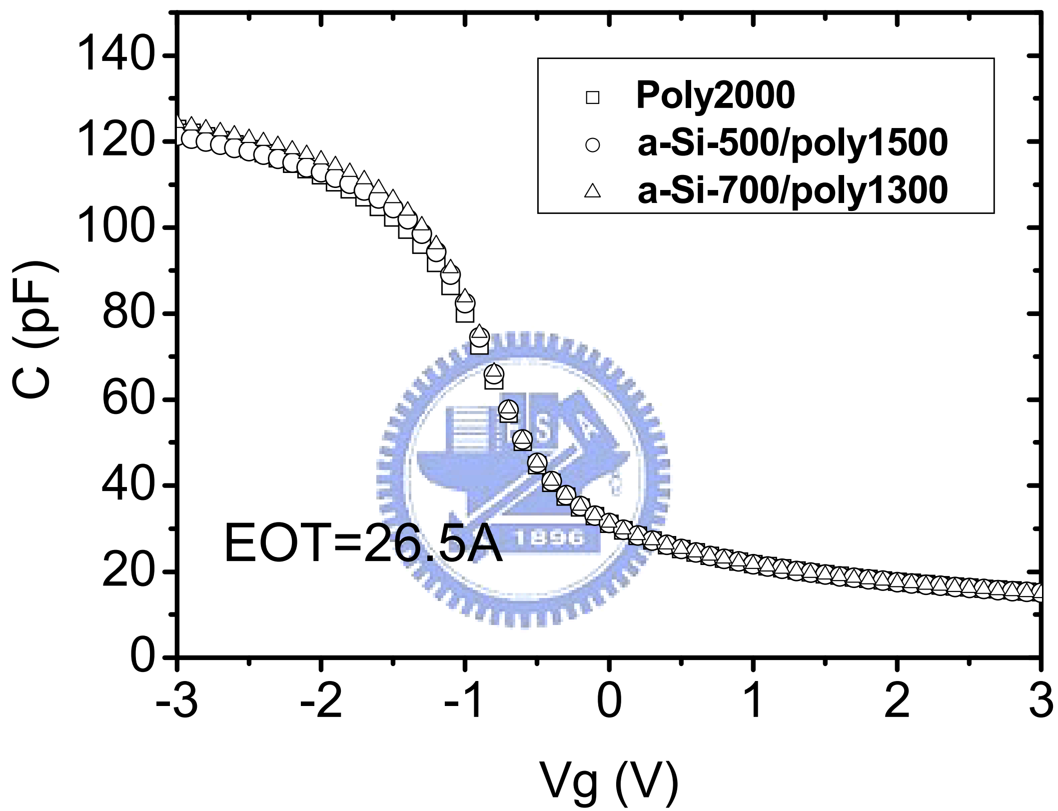


Fig. 3-2 C-V characteristics for different thickness of a-Si layer.

Id-Vg (measured at Vd = 0.1 V) for length = 0.4 μm

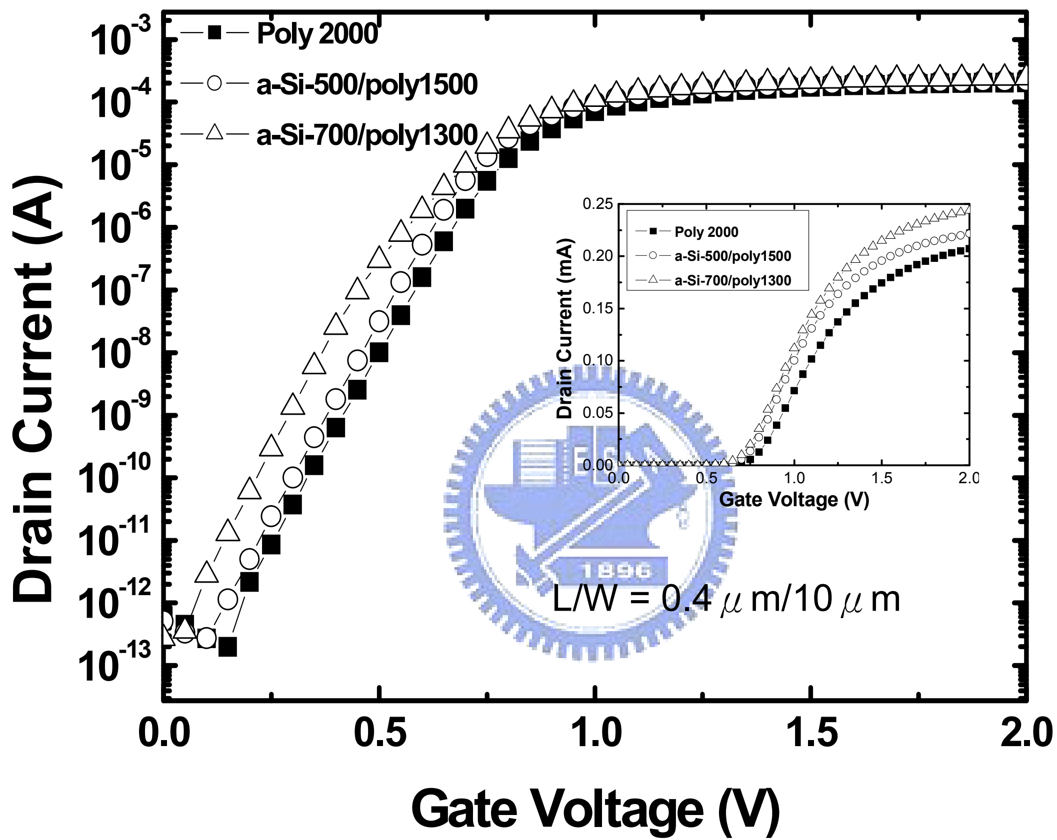


Fig. 3-3 I_d-V_g characteristics for different thickness of a-Si layer.

Id-Vg (measured at Vd = 1 V) for length = 0.4 μm

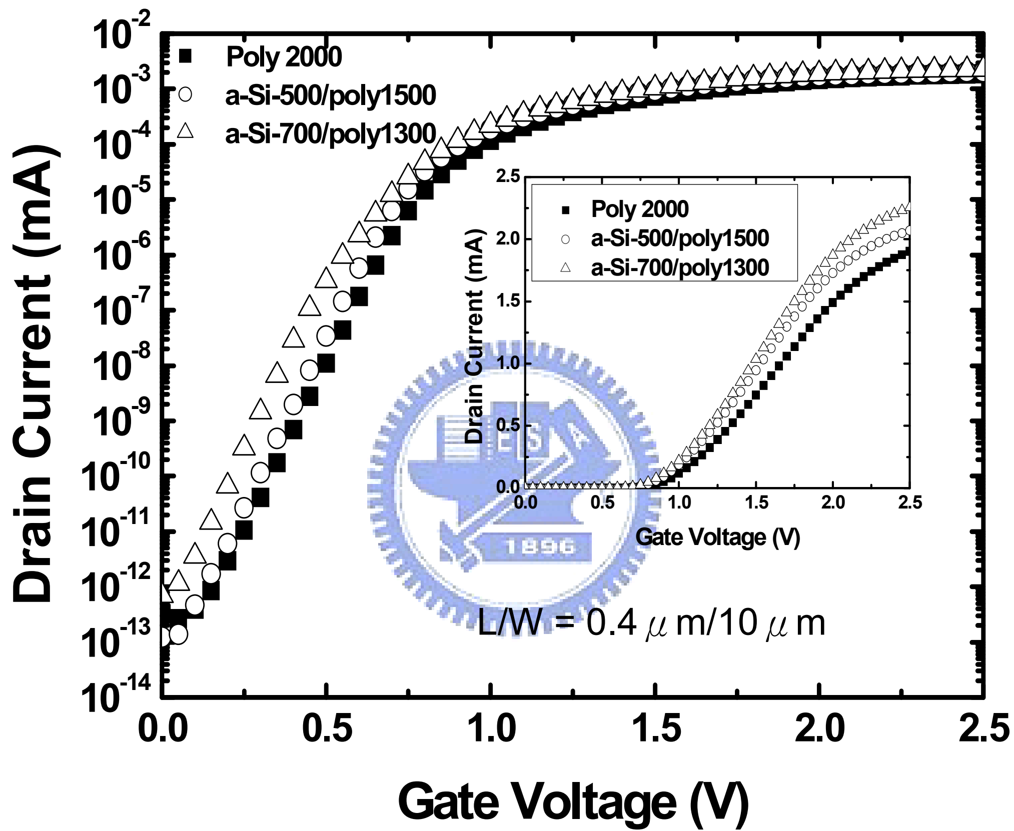


Fig. 3-4 I_d-V_g characteristics for different thickness of a-Si layer.

Vt (lin) measured at Vd = 0.1 V

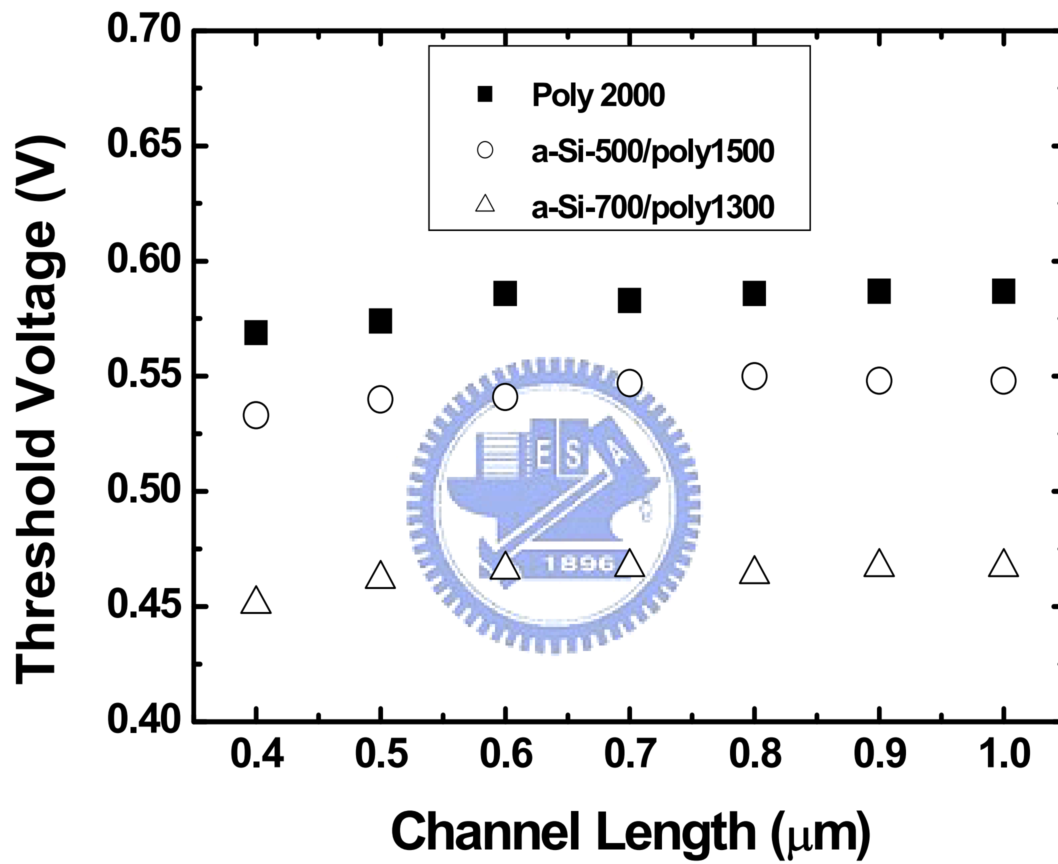


Fig. 3-5 Threshold voltage for different thickness of a-Si layer.

Vt (sat) measured at Vd = 1 V

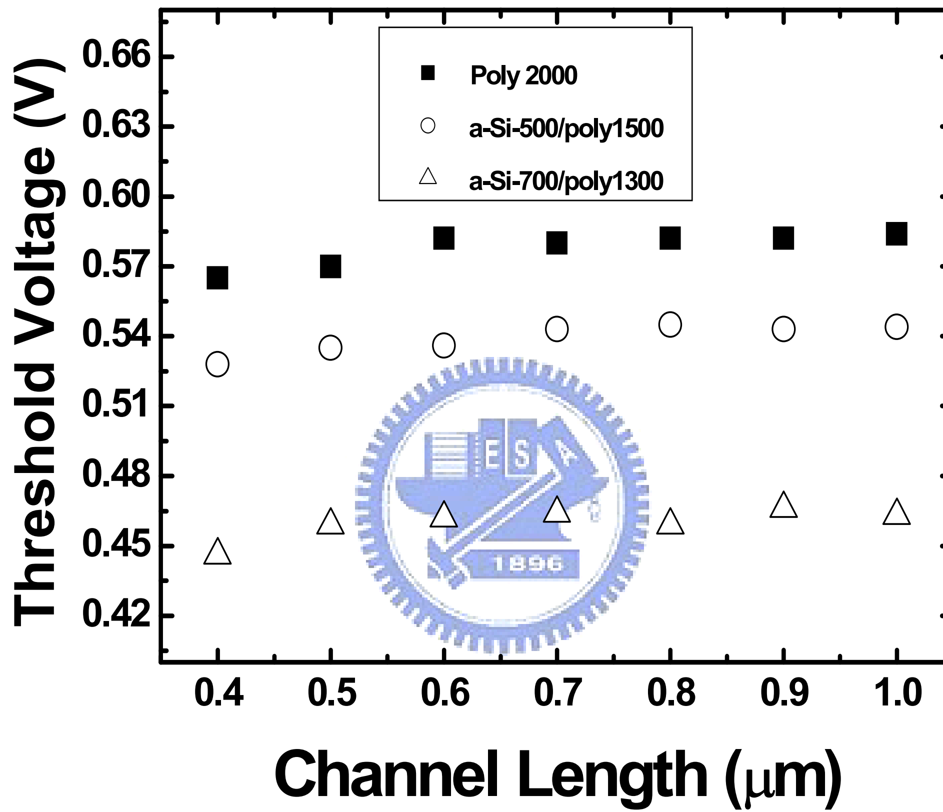


Fig. 3-6 Threshold voltage for different thickness of a-Si layer.

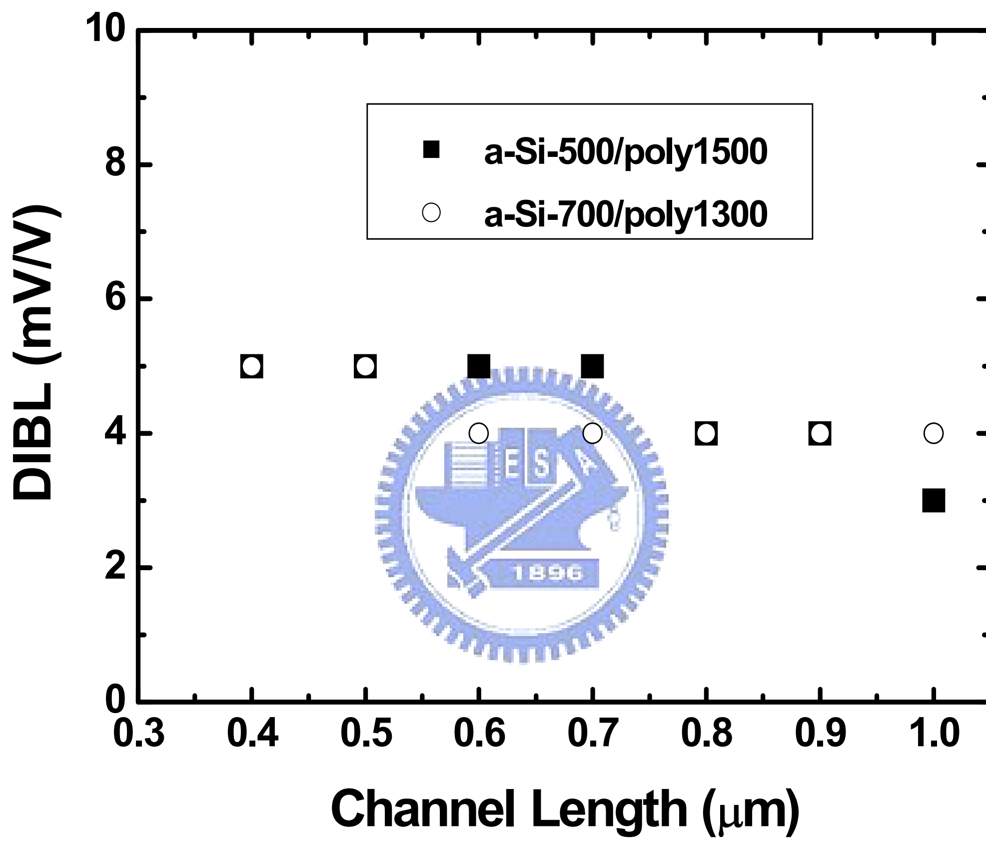


Fig. 3-7 DIBL for a-Si layer with different channel length.

a-Si split+Si_3N_4-1000--Gm,length-0.4 μm

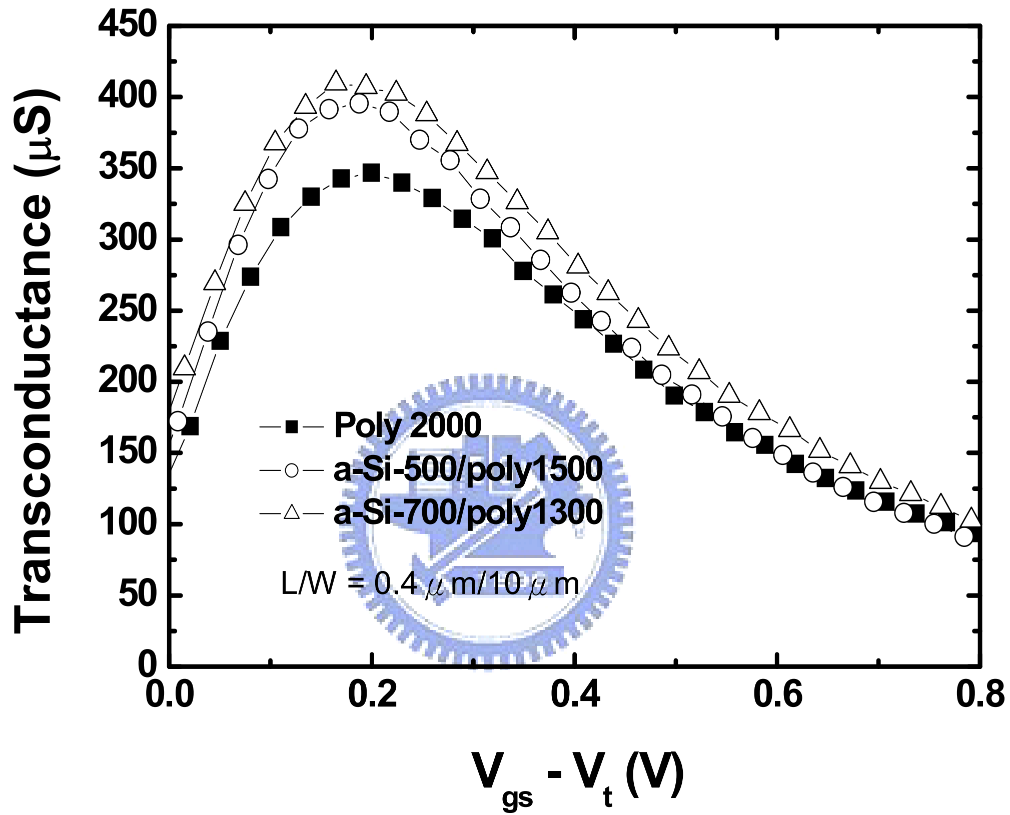


Fig. 3-8 Transconductance for different thickness of a-Si layer.

Δ Gm / Gm, $_{control_Poly\ 2000}$(%)

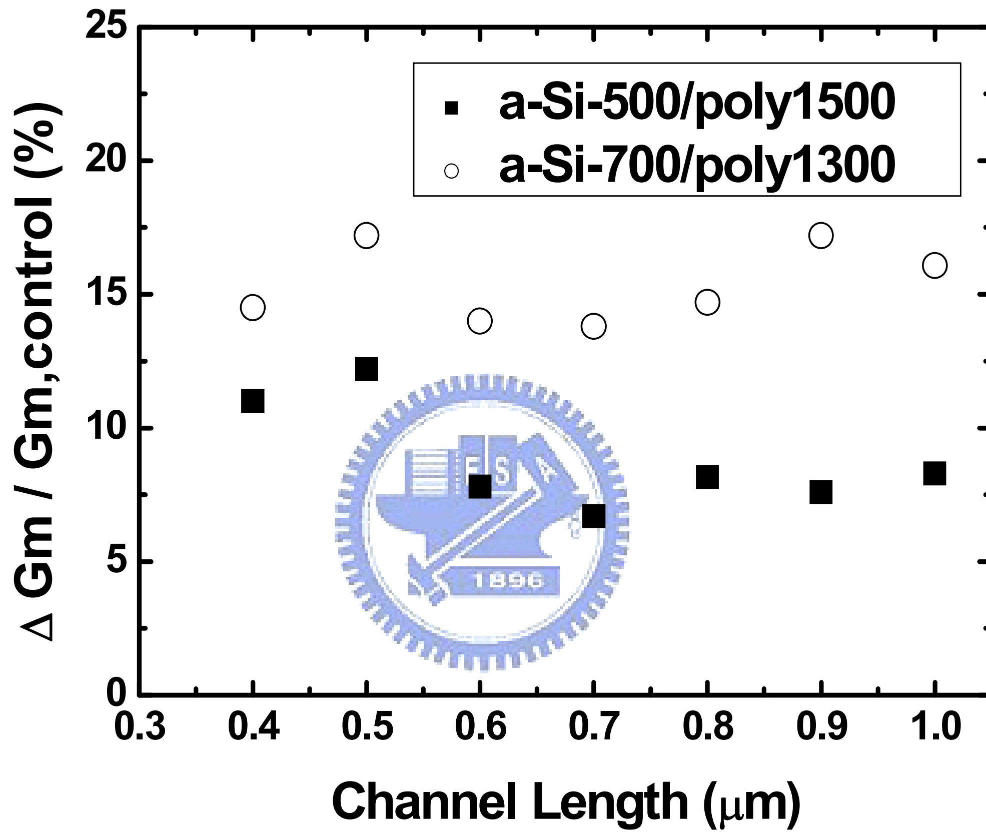


Fig. 3-9 Transconductance increase versus channel length with different thickness of a-Si layer.

a-Si split+Si_3N_4-1000—I_d-V_d,length-0.4 μm

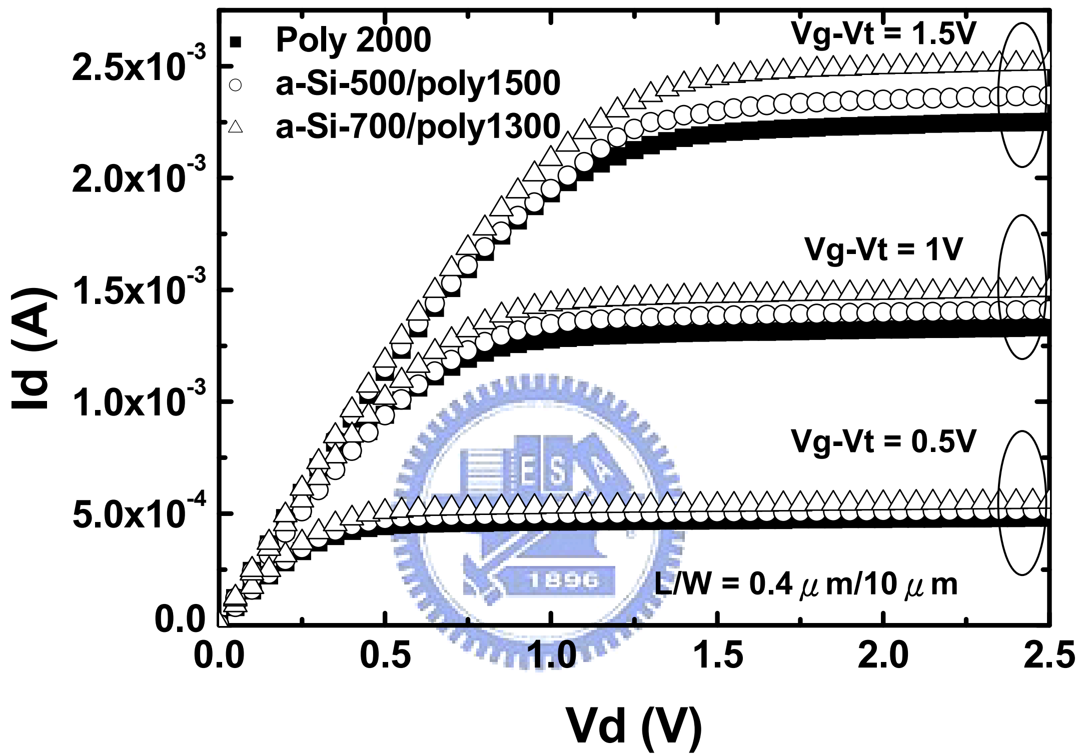


Fig. 3-10 I_d-V_d characteristics for different thickness of a-Si layer.

$\Delta I_D / I_{D,control_Poly\ 2000}$ (%)

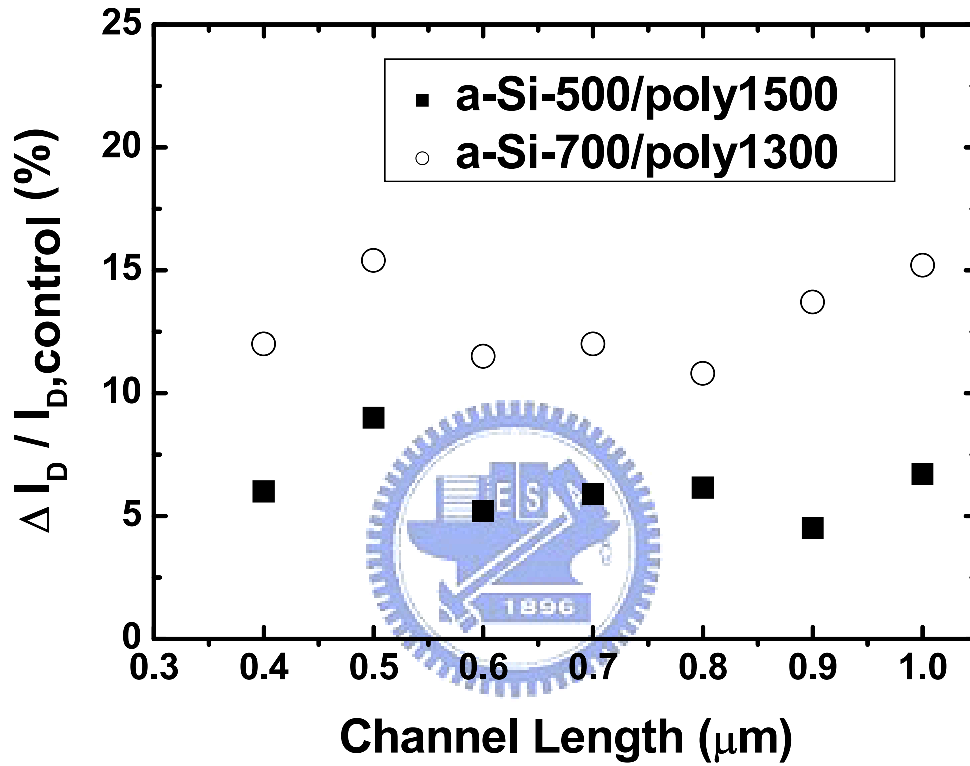


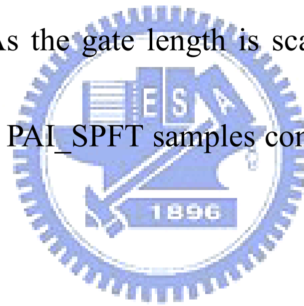
Fig. 3-11 Saturation current increase versus channel length with different thickness of a-Si layer. The saturation current was defined at V_G-V_{th} =1.5 V and V_{DS} = 2.5 V.

Chapter 3-2 Summary of strain proximity free technique (SPFT)

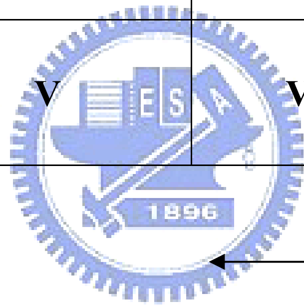
Now, we would describe the strain effect by using Strain Proximity Free Technique (SPFT). The poly-Si gate with two different technique of the SPFT (Strain Proximity Free Technique) and PAI (Poly Amorphous Implantation) with fixed thickness of Si_3N_4 capping layer has been fabricated as shown in Table II and Fig3-12. Fig 3-13 illustrates measured C-V profile that the accumulation capacitance in long channel devices (100 μm) is almost the same as that of the conventional devices and the EOT is about 26.5 Å. The dependence of Id-Vg characteristics with Vd = 0.1V with different technique of poly gate is shown in Fig. 3-14. The dependence of Id-Vg characteristics was measured at Vd = 1V on different technique of poly gate is shown in Fig. 3-15. The improvement of current (linear curve) drivability by using SPFT and PAI_SPFT technique was enhanced. In Fig. 3-16 and Fig. 3-17 show the threshold voltages were measured at Vd = 0.1V and Vd = 1V with different techniques. It found the threshold voltage has slight roll-off characteristics among the devices and the control sample describes a pronounced reverse short channel effect (RSCE). By using SPFT and PAI _SPFT technique, the Vth are smaller than control sample. This is related to the bandgap narrowing effect caused by the channel strain. Fig 3-18 indicates there are no significant differences of DIBL (Drain Induced Barrier Lowing) effect among all samples. Fig. 3-19 shows the Gm increases with the SPFT and

PAI_SPFT technique. The SPFT sample improves 19% and the PAI_SPFT sample improves 21% compare to control sample in the channel length as 0.35 μm. A simple model is presented to explain the mechanism of PAI_SPFT technique. As in Ref. [30-31], it was reported that the vertical compressive stress is the major part of stress in SMT process. However, SPFT process and conventional SMT technique are different as the implant process. From the report [28] that it is very interesting in SMT2 sample which was fabricated with high temperature stress memorization during the final RTA-requires differential process, but not necessarily S/D amorphization. It found the SMT2 sample in NMOS saturated drive current improve 20%. The SMT2 sample process is similar to the SPFT technique. We advance simple model to explain the mechanism of SPFT technique. The polysilicon film is a temperature dependent elastic-plastic material [31]. When increasing temperature the polysilicon is elastic upto the yielding point and then is plastic beyond the yielding point [32]. The polysilicon in plastic region will cause residual strain and deformation, as showed in Fig. 3-20. During the RTA process, the changes in the poly silicon film microstructure re-crystallization and grain change can account for some of the stress variation [33-34]. In our sample the poly-silicon grain size with SPET process and without SPFT is compared by AFM and SEM in Fig. 3-21 and Fig. 3-22. Mean grain size for poly silicon without SPFT is 94nm, while the size with SPET becomes smaller down

to 72nm. There is possibility that grain size changes during SPET process may induce tensile stress memorization phenomena in the channel region [35]. It will provide a high vertical compressive strain on poly-Si after RTA process and a residual strain will be induced in poly-Si. This mechanism could be explained the stress elevation by using SPFT to enhance electron mobility. In Fig. 3-23, as the gate length is scaling the percentage increase of Gm with the SPFT and PAI_SPFT samples compared to the control sample. Fig. 3-24 shows the drain current enhancement reaches 13% in the SPFT samples and 15% in the PAI_SPFT samples compare to the control samples at a channel length of 0.35 μm. As the gate length is scaling the percentage increase of drive current of the SPFT and PAI_SPFT samples compared to the controls sample in Fig. 3-25.

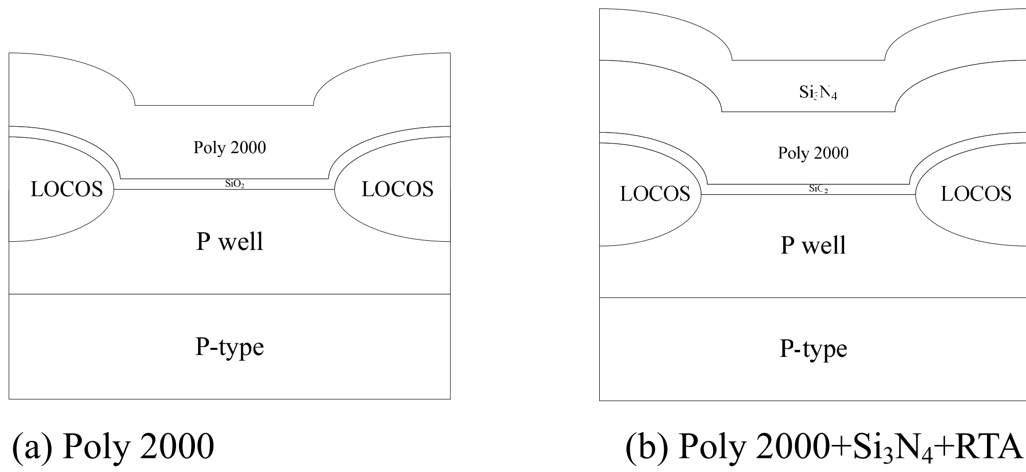


split / Gate structure	PAI (S:As / E:10kev / D:1E15)	Si_3N_4 (1500 Å)	RTA (1050°C)	Remove Si_3N_4
Poly 2000				
Poly 2000		**V**	**V**	**V**
Poly 2000	**V**	**V**	**V**	**V**

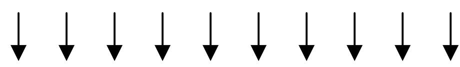


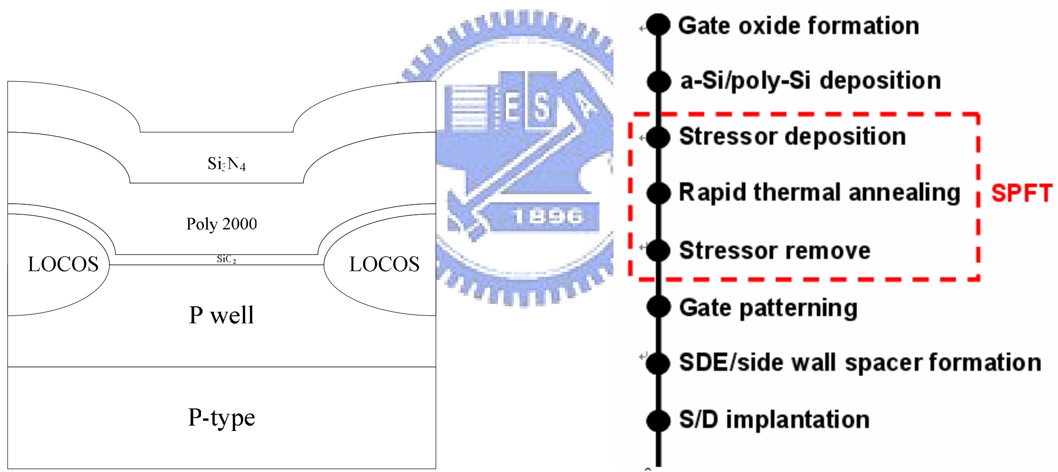
SPFT process

Table. II Poly gate with SPFT and PAI_SPFT technique.



(a) Poly 2000　　　　(b) Poly 2000+Si_3N_4+RTA





(c) Poly 2000+PAI+Si_3N_4+RTA　　　　(d) process flow

Fig. 3-12 Poly gate with SPFT and PAI_SPFT technique (a) Poly 2000 (b) Poly 2000+Si_3N_4+RTA (c) Poly 2000+PAI+Si_3N_4+RTA (d) process flow

W/L= 100/100 μm

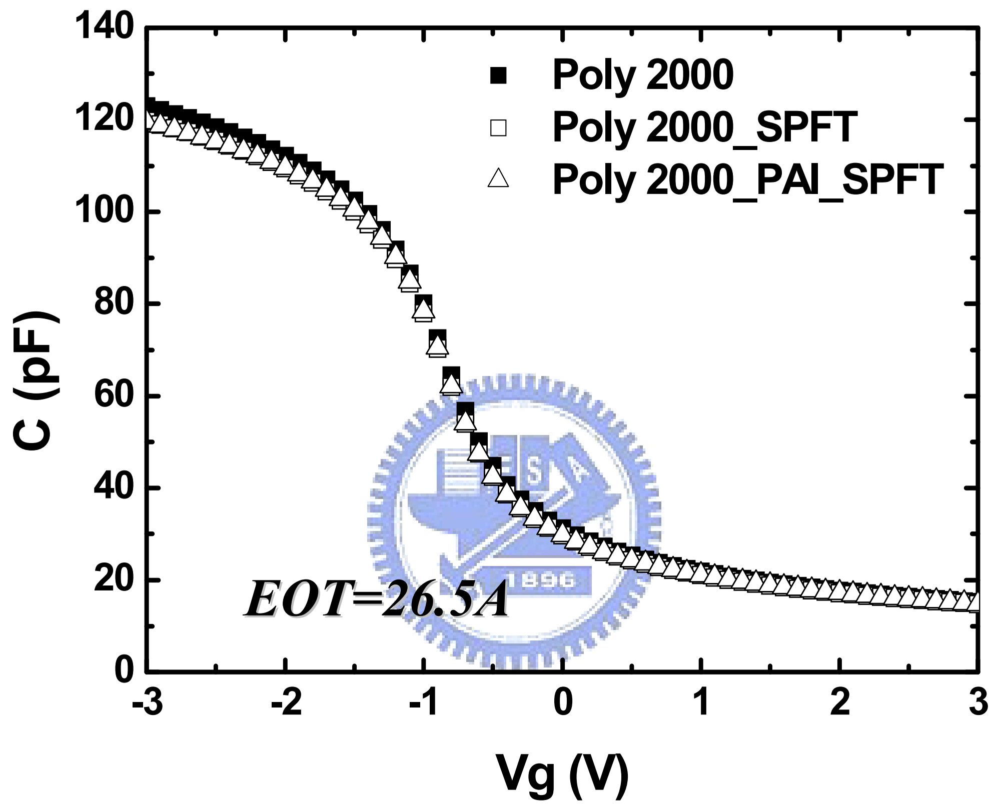


Fig. 3-13 C-V characteristics for SPFT and PAI_SPFT technique.

Id-Vg (measured at Vd=0.1 V) for length = 0.35 μm

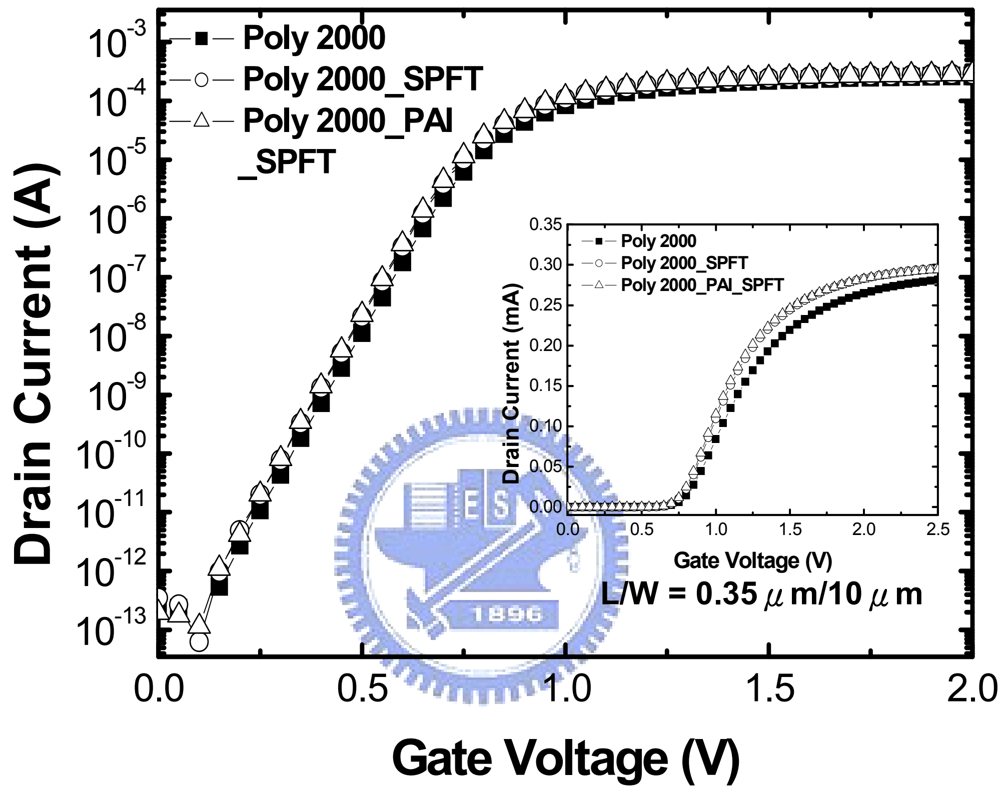


Fig. 3-14 I_d-V_g characteristics for SPFT and PAI_SPFT technique.

Id-Vg (measured at Vd=1 V) for length=0.35 μm

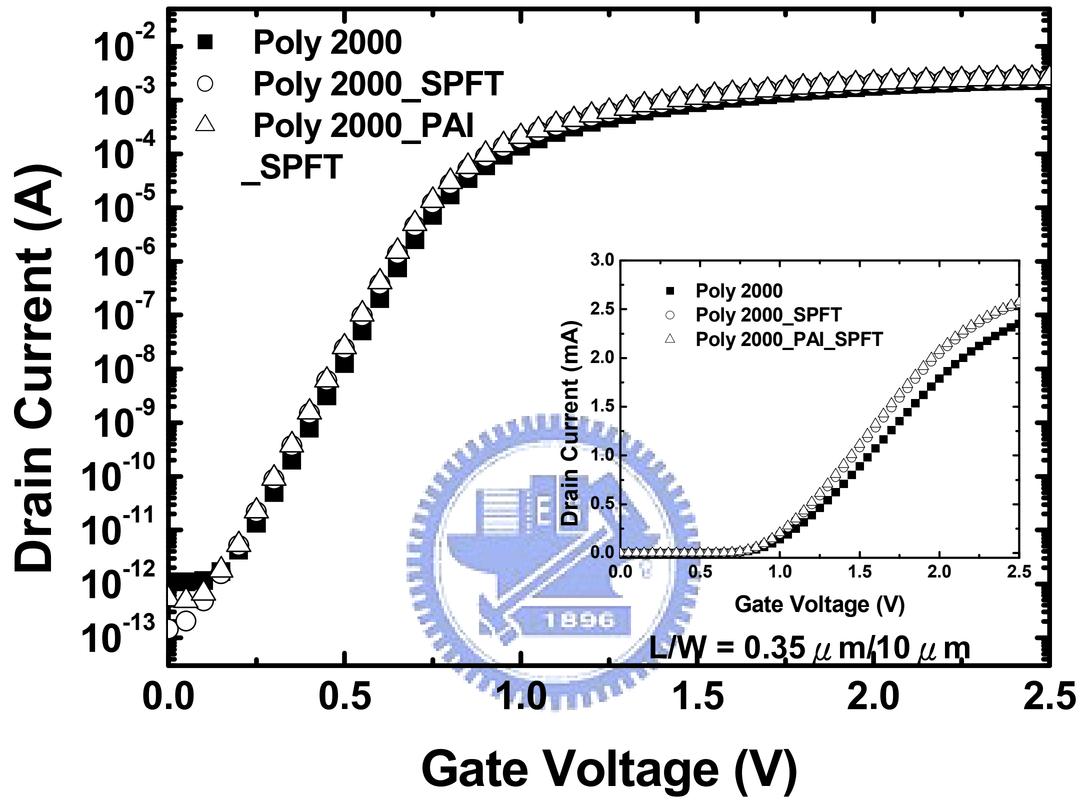


Fig. 3-15 I_d-V_g characteristics for SPFT and PAI_SPFT technique.

Vt (lin) measured at Vd=0.1 V

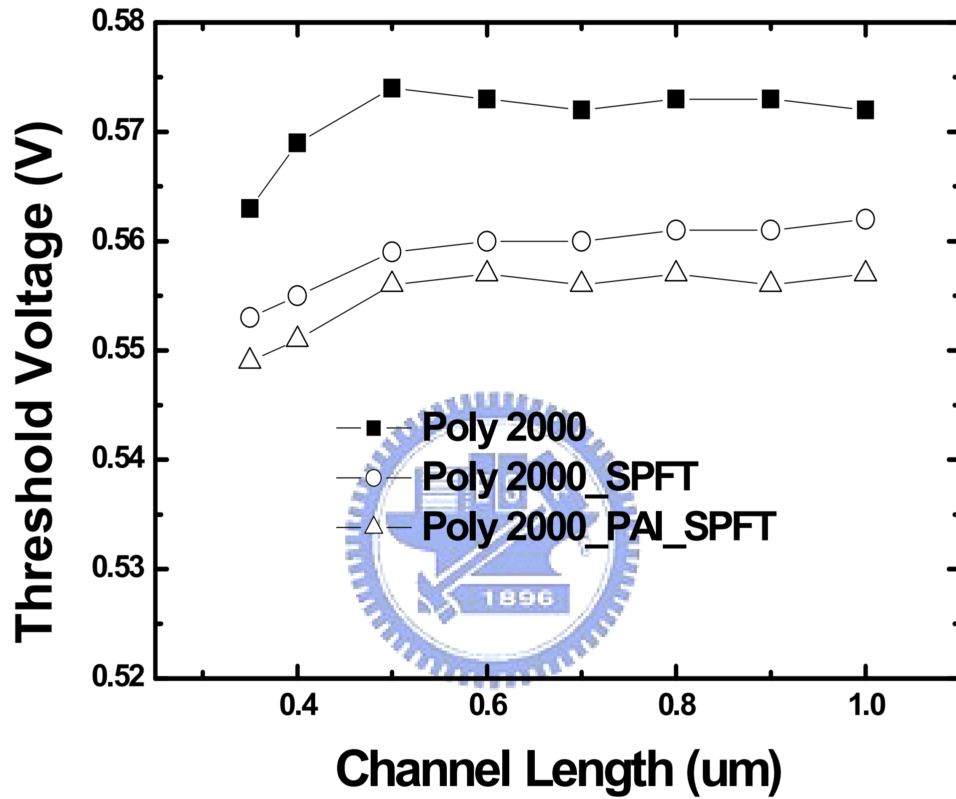


Fig. 3-16 Threshold voltage for SPFT and PAI_SPFT technique.

Vt (sat) measured at Vd=1 V

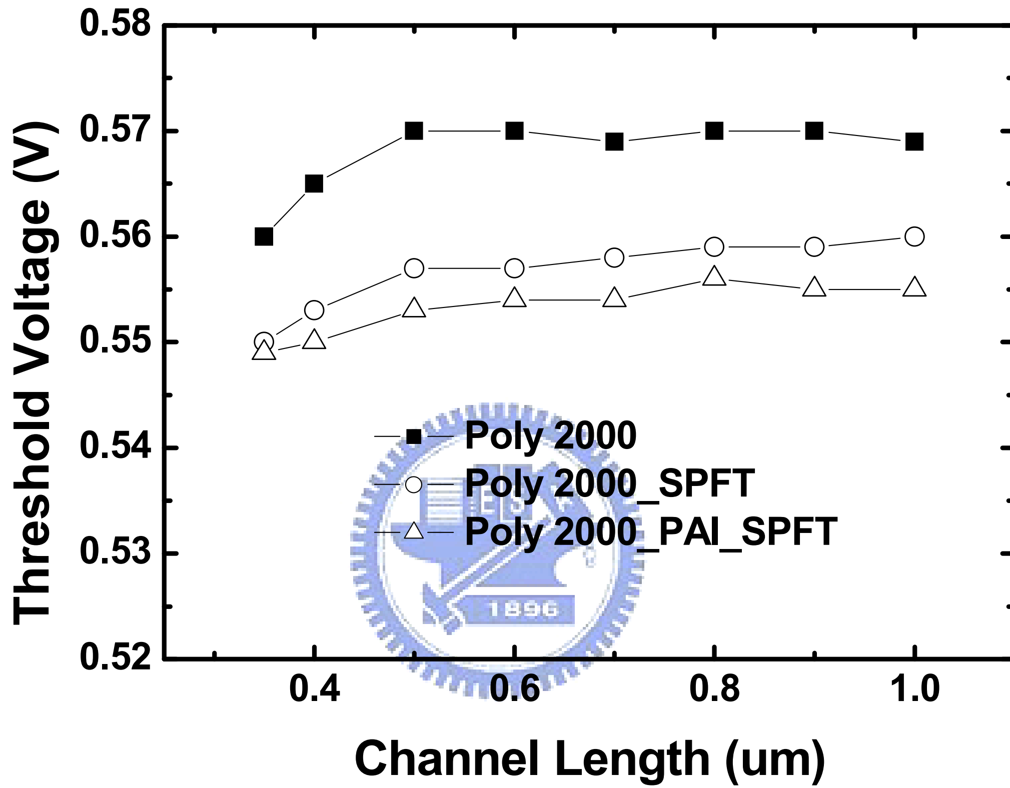
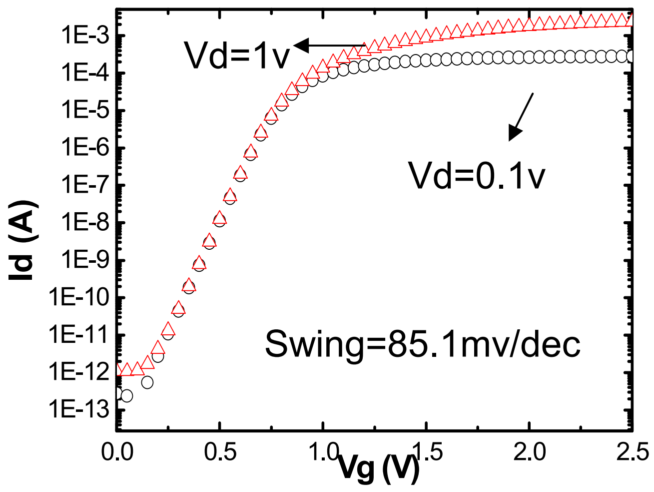
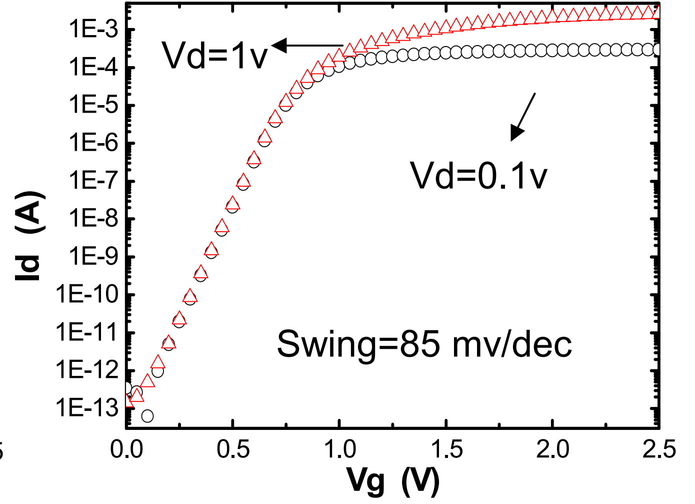


Fig. 3-17 Threshold voltage for SPFT and PAI_SPFT technique.

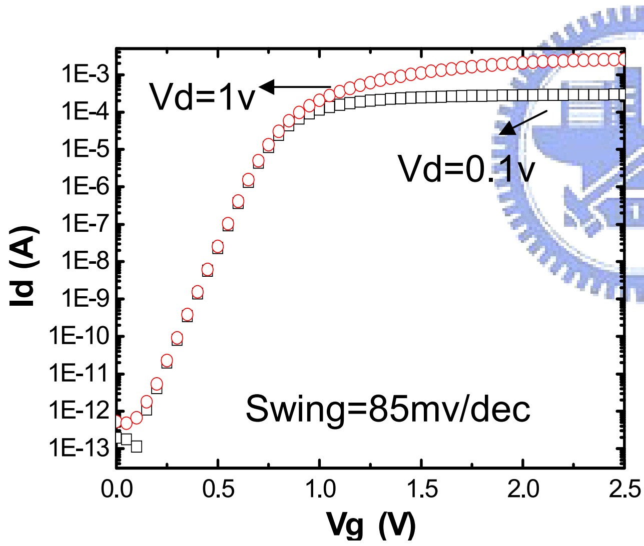
L/W = 0.35 μm/10 μm



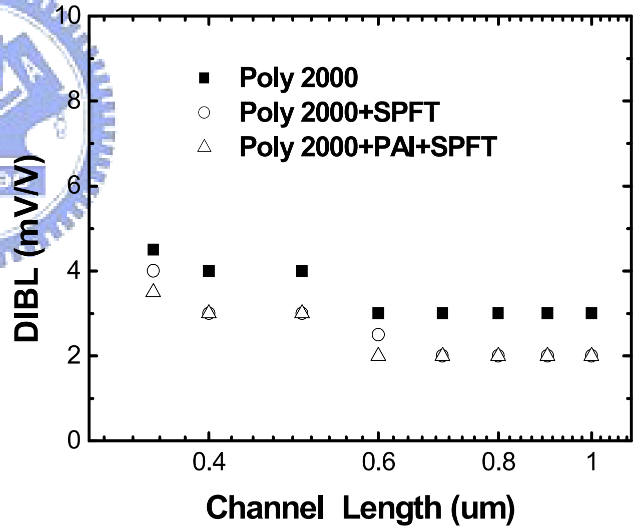
(a) Poly 2000



(b) Poly 2000_SPFT



(c) Poly 2000_PAI_SPFT



(d) DIBL for SPFT and PAI_SPFT.

Fig. 3-18 DIBL for SPFT and PAI_SPFT technique.

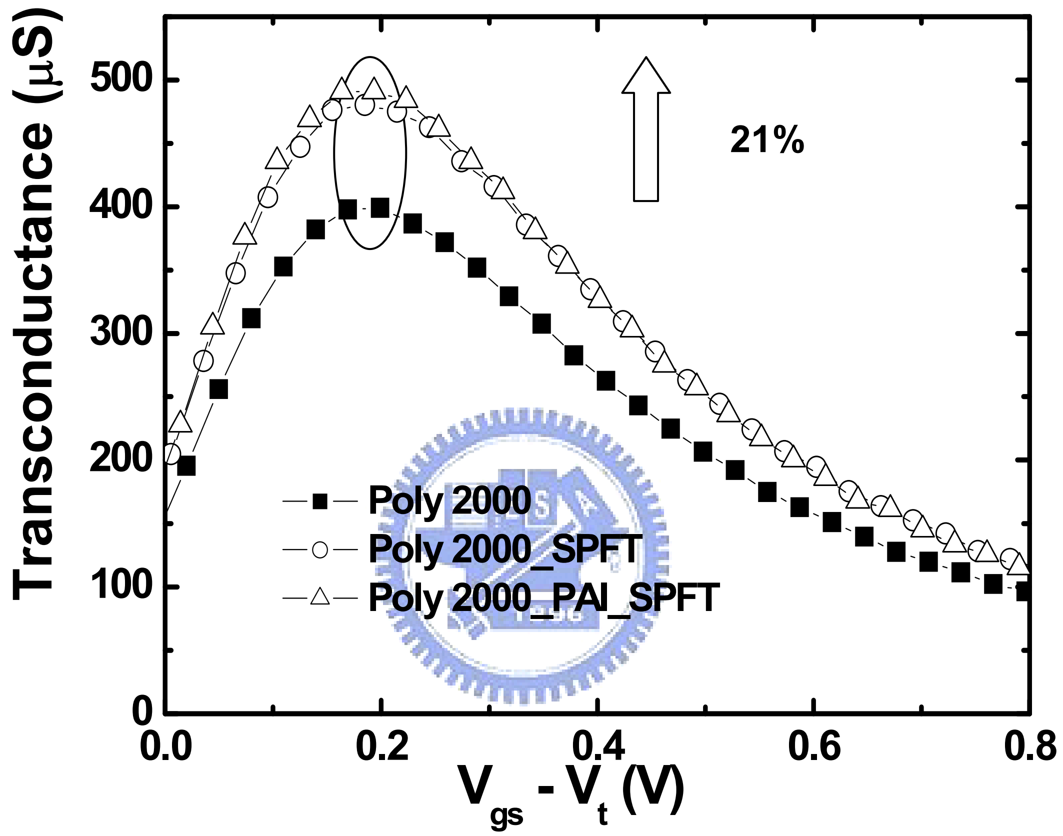


Fig. 3-19 Transconductance for SPFT and PAI_SPFT technique.

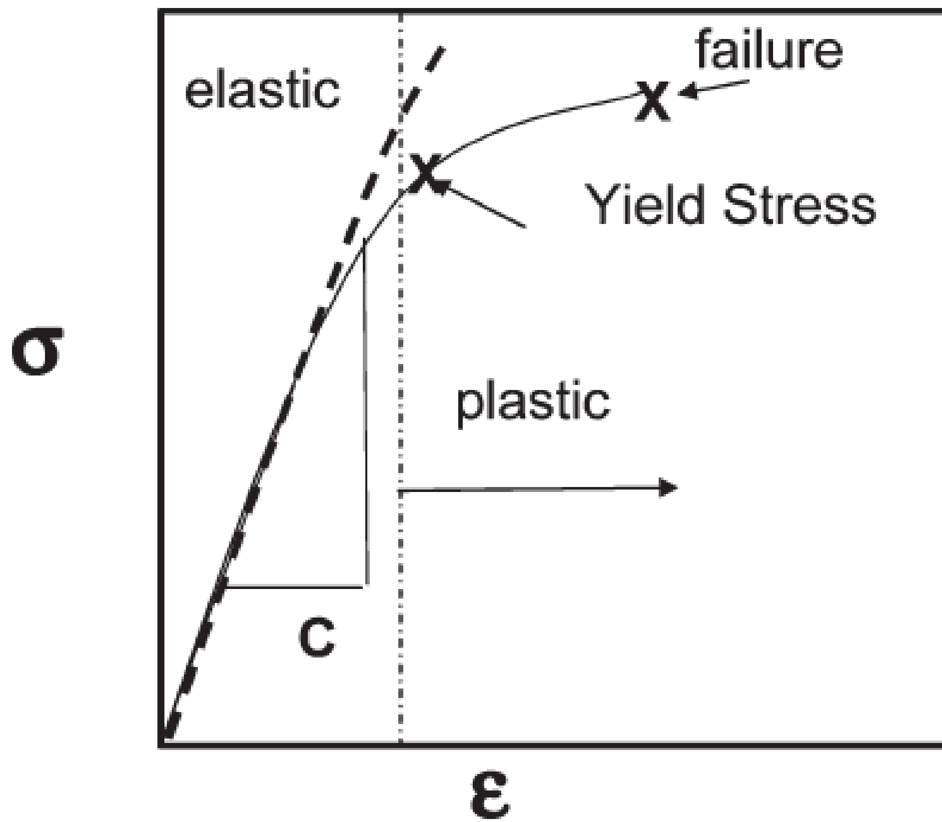
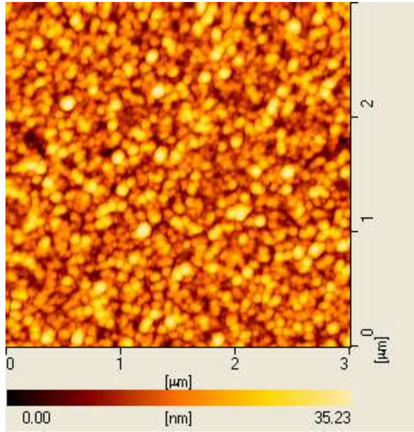
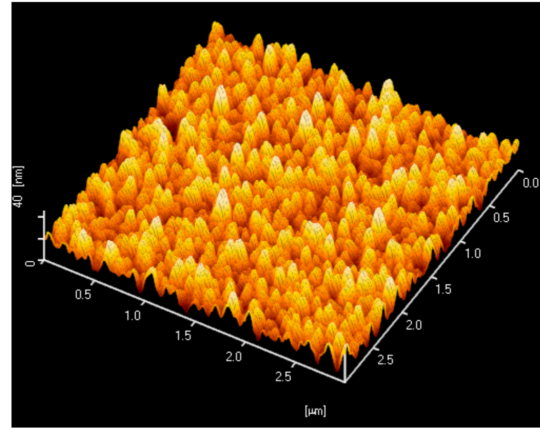
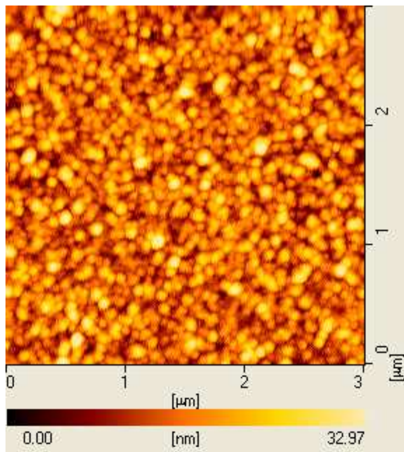


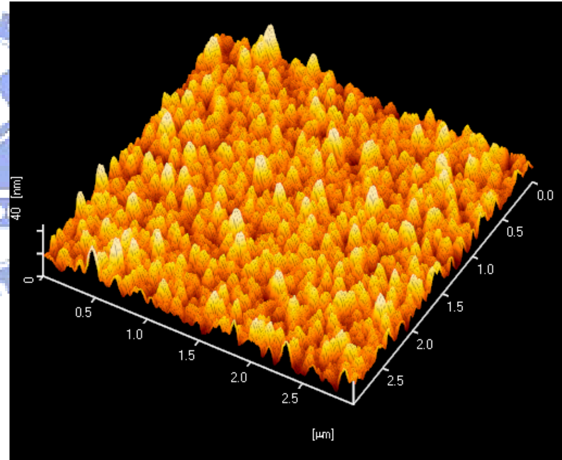
Fig. 3-20 Stress–strain curve showing the elastic and plastic regimes.[32]





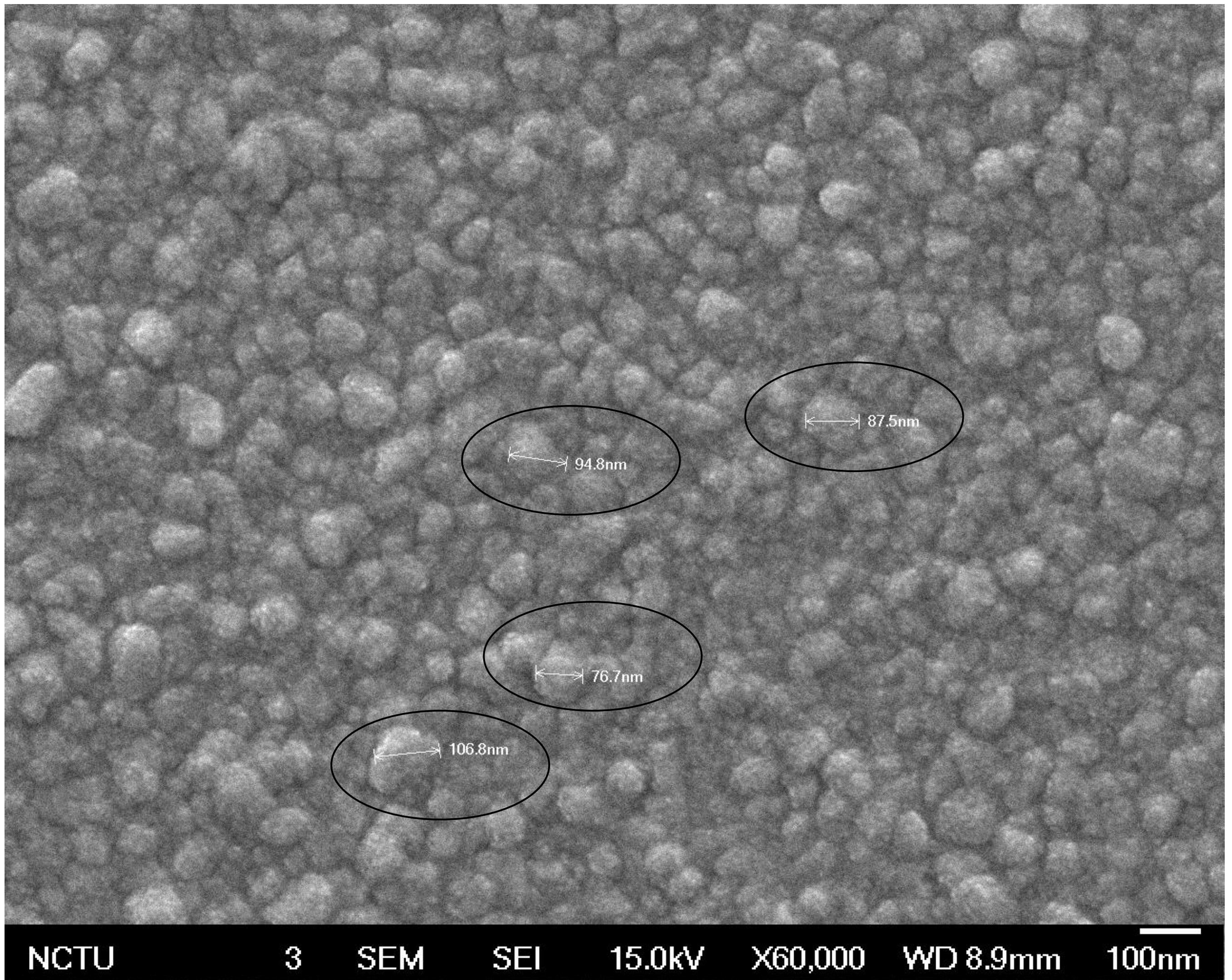
(a) AFM image for Poly 2000 sample. (b) 3-D AFM image for Poly 2000 sample.



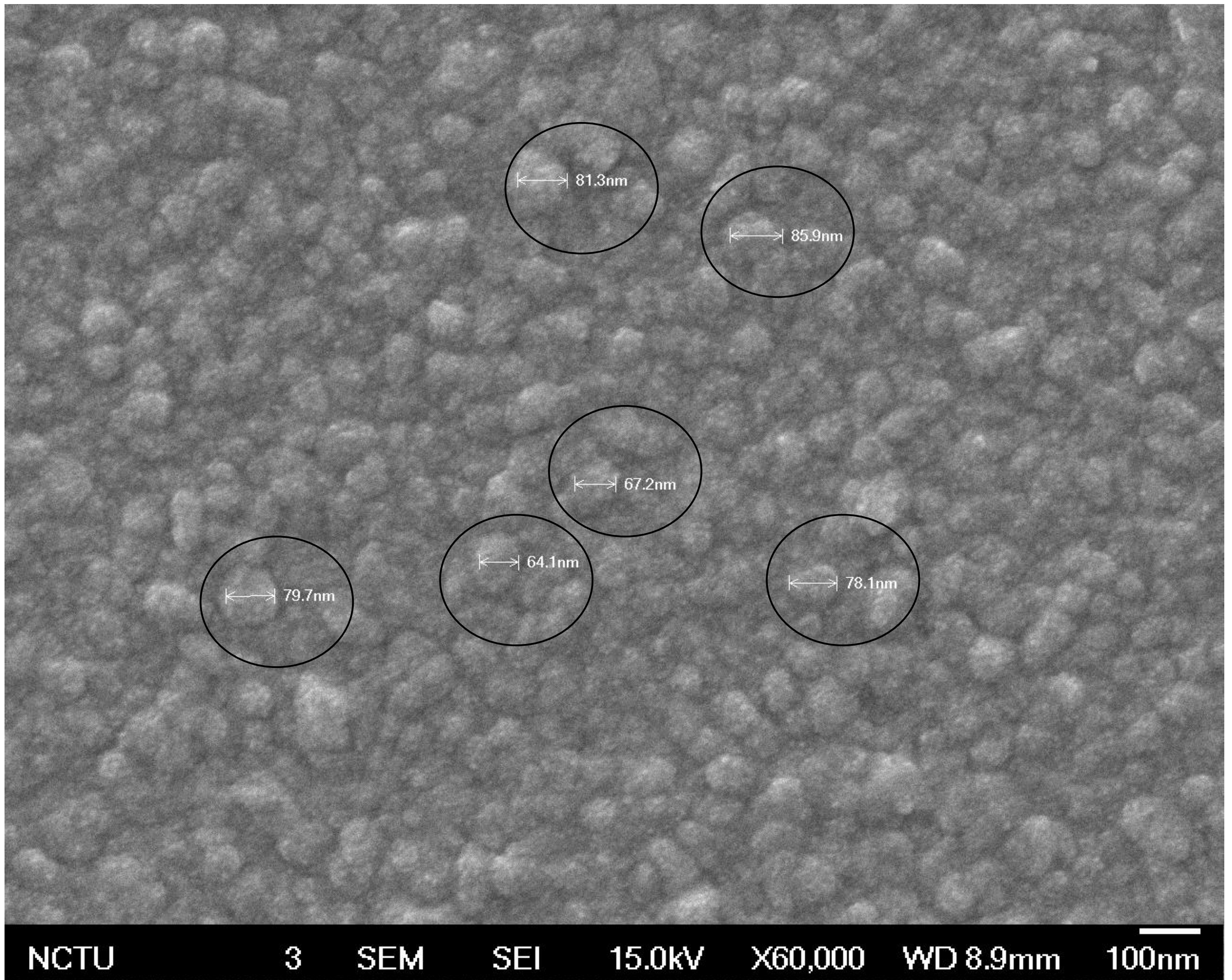


(c) AFM image for Poly 2000_SPFT sample (d) 3-D AFM image for Poly 2000_SPFT sample.

Fig. 3-21 AFM image for Poly 2000 sample and Poly 2000_SPFT sample. Poly 2000 sample mean grain size is 94 nm and Poly 2000_SPFT sample mean grain size is 72 nm.



(a) SEM image for Poly 2000 sample.



(b) SEM image for Poly 2000_SPFTsample.

Fig. 3-22 SEM image for Poly 2000 and Poly 2000_SPFT samples. The grain size is between 77 nm and 106 nm in Poly 2000 sample and grain size is between 64 nm and 79 nm in Poly 2000_SPFT sample.

Δ Gm / Gm, $_{control_Poly\ 2000}$ (%)

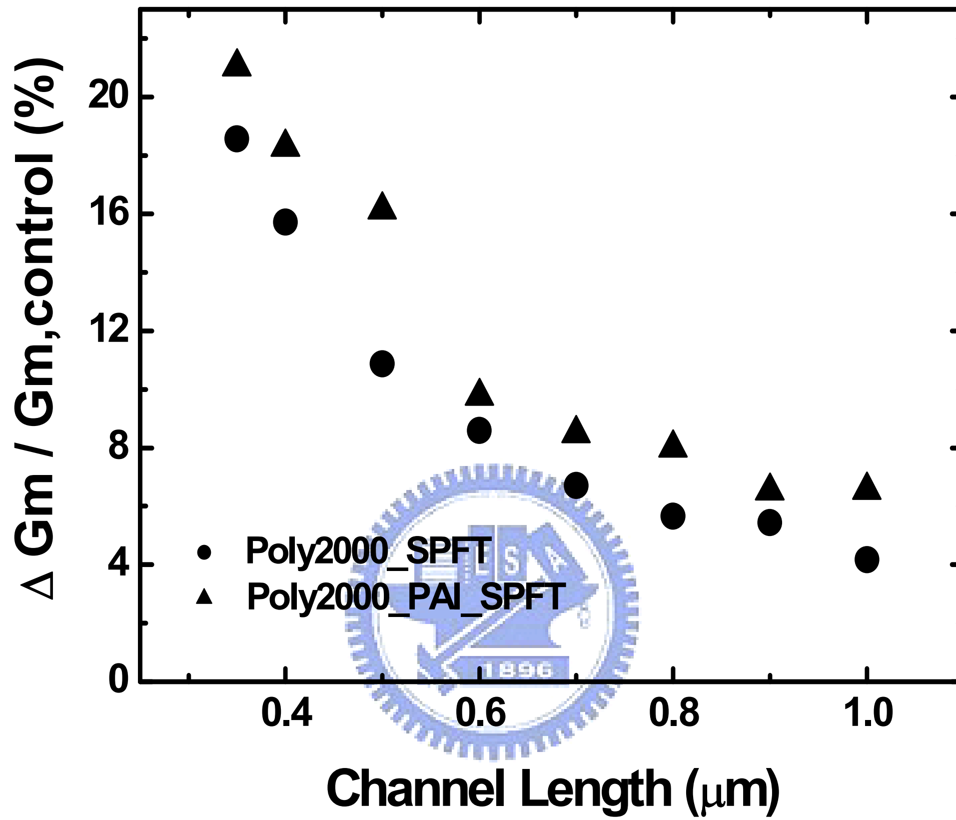


Fig. 3-23 Transconductance increase versus channel length with SPFT and PAI_SPFT technique.

Poly 2000 split_Si_3N_4-1000—I_d-V_d,length-0.35 μm

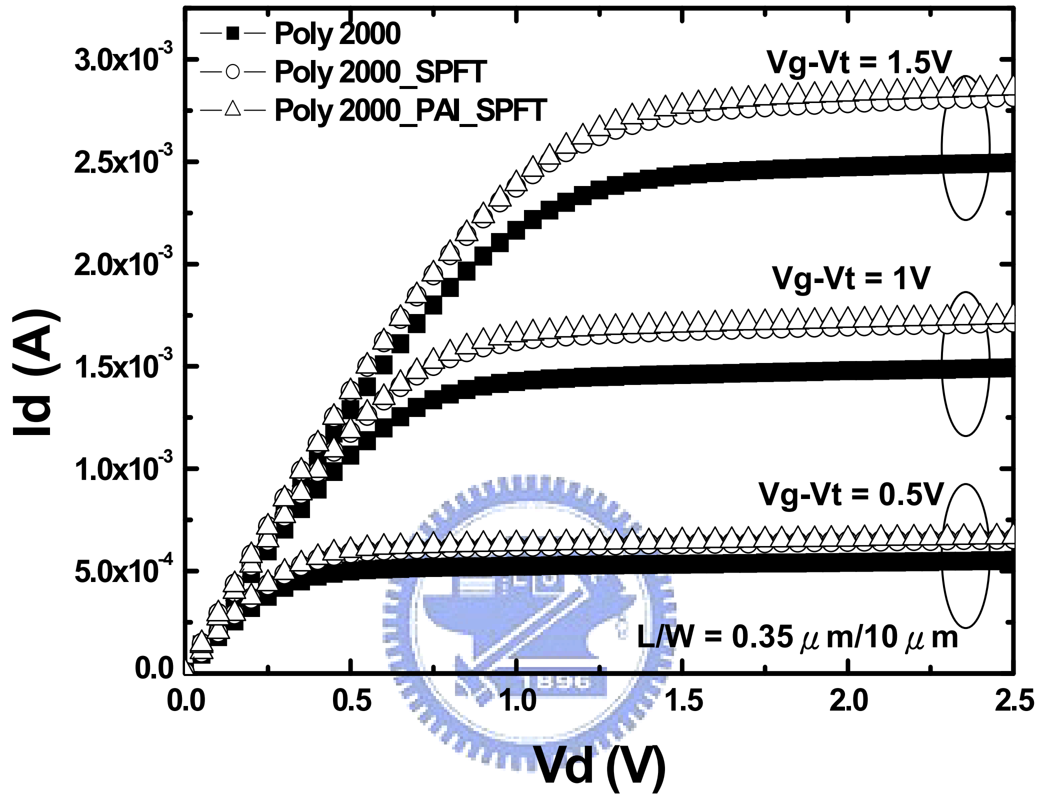


Fig. 3-24 I_d-V_d characteristics for SPFT and PAI_SPFT technique.

$\Delta I_D / I_{D,control_Poly\ 2000}$ (%)

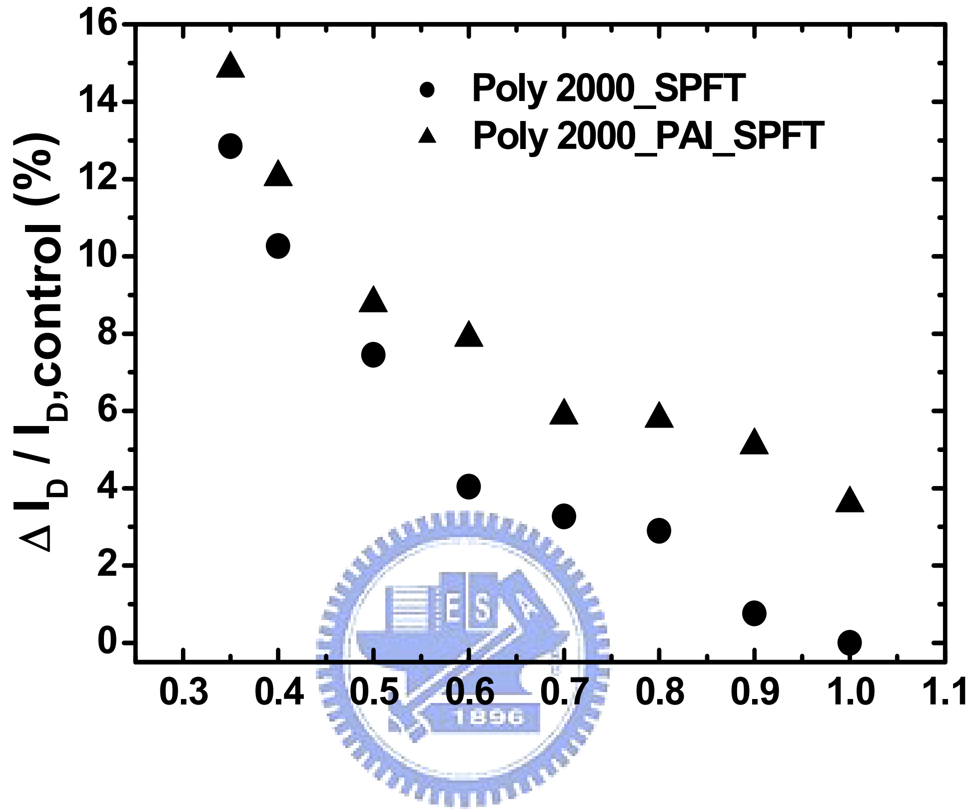


Fig. 3-25 Saturation current increase versus channel length with SPFT and PAI_SPFT technique. The saturation current was defined at V_G-V_{th} =1.5 V and V_{DS} = 2.5 V.

Chapter 3-3 Summary of stacked a-Si gate structure with SPFT

In this section we would describe the local strained technique by using stacked a-Si gate structure with SPFT. The dependence of Id-Vg and transconductance characteristics with SPFT and a-Si-700/poly1300_SPFT gate structure technique are shown in Fig. 3-26. It found that the SPFT can further increase Gm 16% compare to the control sample. Moreover, the Gm increases 23% could be achieved when a-Si-700/poly1300_SPFT gate structure. The mechanism of the stress enhancement in stacked a-Si-700/poly1300 gate could be as follows: the re-crystallization of amorphous region during SPFT process leads to shrinkage of total thickness of stacked a-Si/poly-Si gate and results in the residual tensile strain to channel. The stacked gate structure with optimization of a-Si/poly-Si thickness will provide more vertical compressive stress and longitudinal tensile stress into channel region. By using SPFT process and a-Si-700/poly1300_SPFT gate structure that the Vth is small than the control sample, as showed in Fig. 3-27. The shift of Vth may cause to the bandgap narrowing effect caused by the channel strain. In Fig. 3-28, as the gate length is scaling the percentage increase of transconductance of the SPFT and a-Si-700/poly1300_SPFT gate structure compared to the control sample. Fig. 3-29 shows the drain current enhancement reaches 11% in the SPFT and 16% in a-Si-700/poly1300_SPFT samples compare to the control sample at a channel length

of 0.4 μm. As the gate length is scaling the percentage increase of drive current of the SPFT and a-Si-700/poly1300_SPFT gate structure samples compared to the control sample in Fig. 3-30.

Id-Vg (measured at Vd=0.1 V) for length=0.4 μm

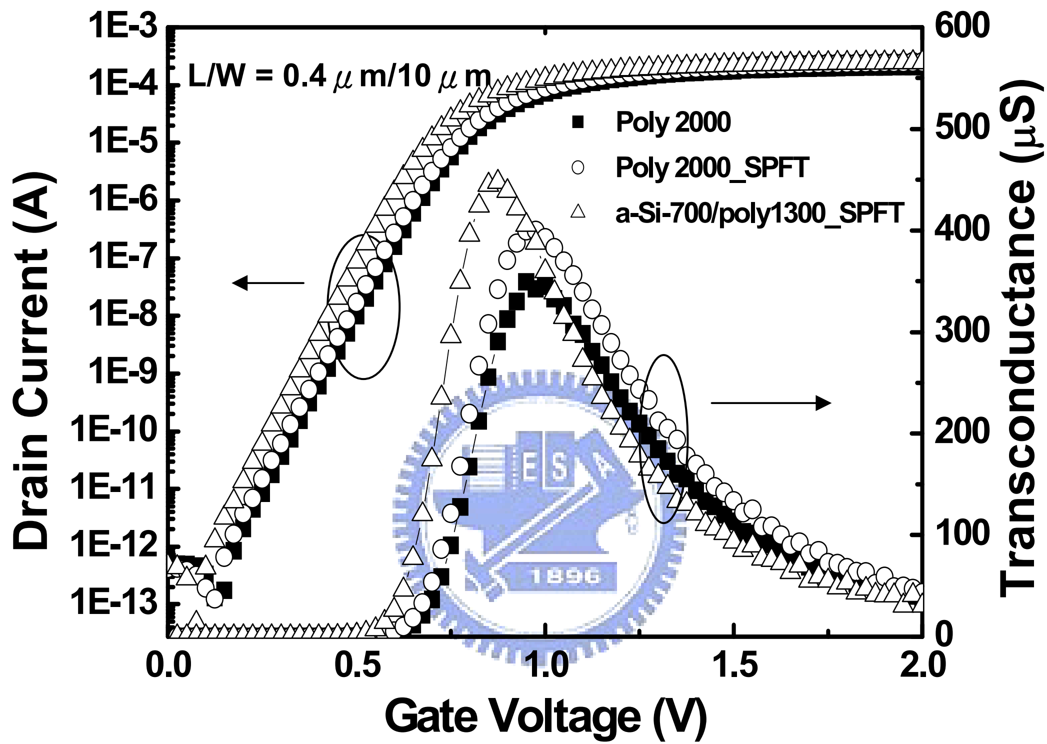


Fig. 3-26 Id-Vg and transconductance characteristics with SPFT and a-Si-700/poly1300_SPFT gate structure.

Vt (linear) measured at Vd=0.1 V

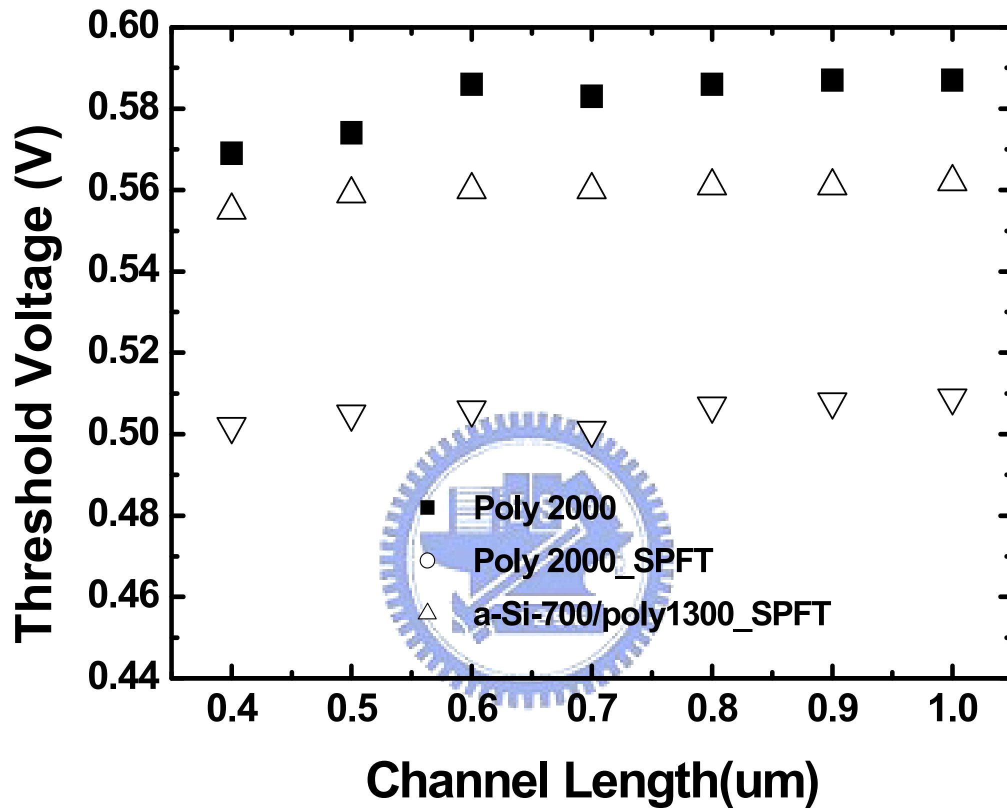


Fig. 3-27 Threshold voltage for SPFT and a-Si-700/poly1300_SPFT gate structure .

Δ Gm / Gm, $_{control_Poly\ 2000}$(%)

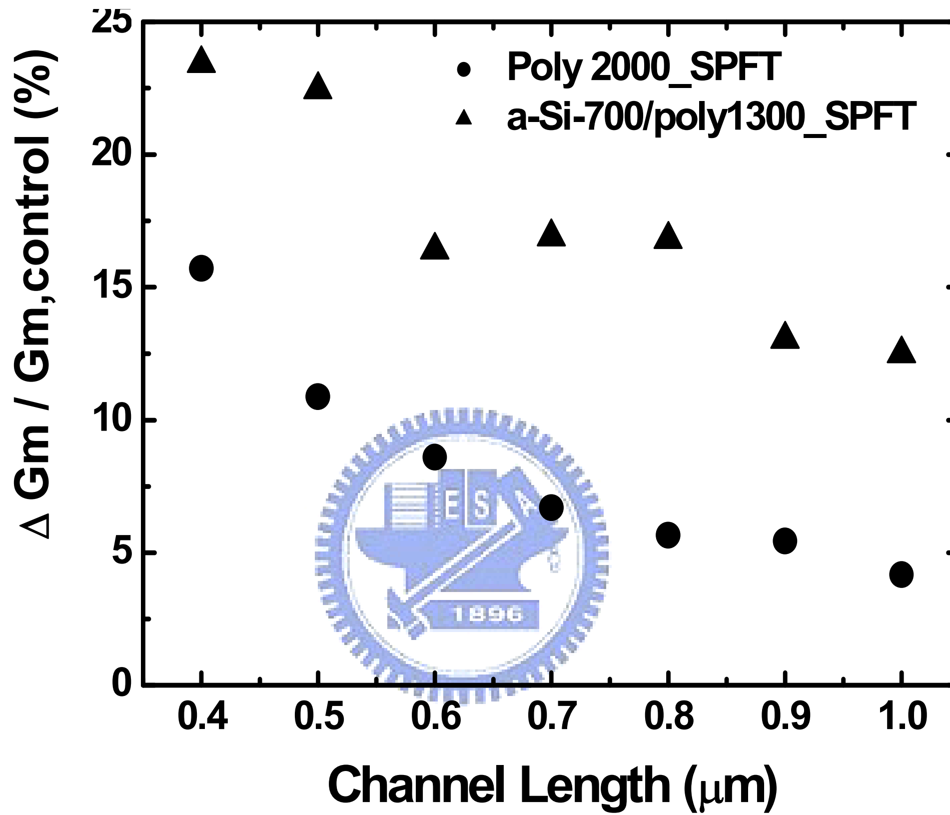


Fig. 3-28 Transconductance increase versus channel length with SPFT and a-Si-700/poly1300_SPFT gate structure.

Gate split_Si_3N_4-1000—I_d-V_d,length-0.4 μm

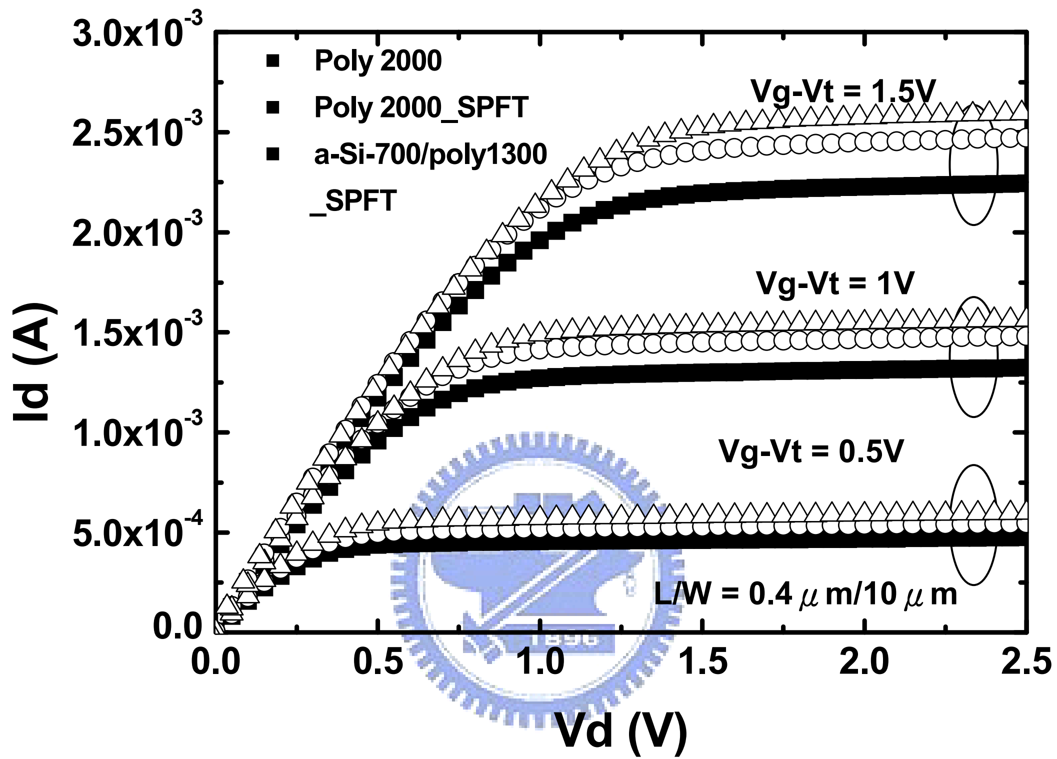


Fig. 3-29 I_d-V_d characteristics for SPFT and a-Si-700/poly1300_SPFT gate structure.

$\Delta I_D / I_{D,control_Poly\ 2000}$ (%)

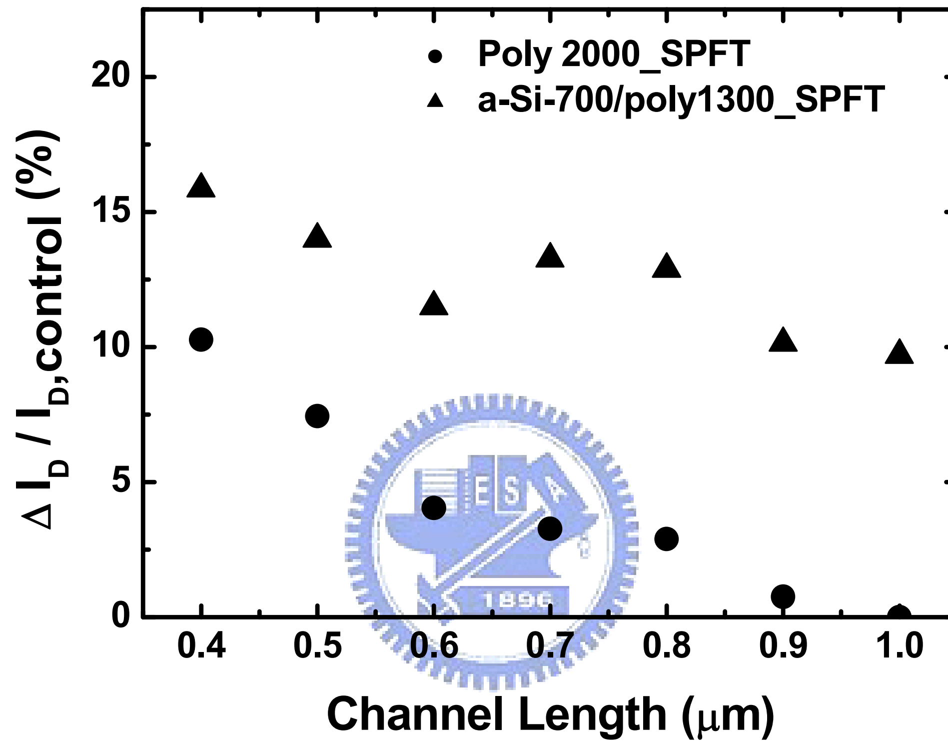


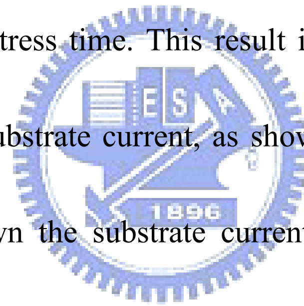
Fig. 3-30 Saturation current increase versus channel length with SPFT and a-Si-700/poly1300 _ SPFT gate structure. The saturation current was defined at V_G-V_{th} =1.5 V and V_{DS} = 2.5 V.

3-4 Hot carrier reliability

One of the serious reliability problems posed by continued shrinking of MOSFETs into the submicron regime is the hot-carrier effect . If device channel length in scaling and the power-supply voltage remains constant, the internal lateral electric field is increasing so much. This would cause the inversion layer charge acquire energy (or a high effective temperature, thus called hot carriers) enough to impact ionization that generates electron-hole pairs in silicon (as shown in Fig. 3-31), and leads to a number of harmful devices phenomena. The most important hot carrier effect is the damage inflicted to the gate oxide and Si/SiO2 interface. This causes a time dependent degradation of various MOSFET characteristics, for example, threshold voltage, linear region transconductance, subthreshold slope (swing), and saturation current.

The substrate current of the SPFT and PAI_ SPFT samples with various channel lengths are shown in Fig. 3-32. It significant seen the SPFT sample substrate current is much larger than the control sample with reducing channel length. And PAI_SPFT sample substrate current has slightly larger than SPFT sample at the same channel length. In Fig. 3-33, the a-Si-700/poly1300_SPFT sample substrate current is larger than the other splits with reducing channel. The results indicates that the channel strain enhance mobility and impact ionization rate [36-37]. An empirical expression for substrate current is I_{sub} α exp $(-\varphi_i / q\lambda E)$, where λ is the mean-free path of electrons and E is the electric field. φ_i is the minimum energy for impact ionization,

which is shown to be about the magnitude of the bandgap [38-39]. Therefore, the bandgap narrowing will act on substrate current. In Fig. 3-34 shown the substrate current with three splits of samples at Vds = 3.5 V and channel length is 0.35um. The devices were stressed at Vds = 3.5 V and V_{GS} at maximum substrate current. The Id-Vg and transconductance characteristics with three samples at Vds=0.1 V were measured before and after stress 5000 seconds as shown in Fig. 3-35. The stress degradation caused by the hot electrons. We found that the shift of threshold voltage (ΔV_{th}) and degraded peak transconductance (ΔGm) are slightly higher in SPFT sample as a function of the stress time. This result is attributed by improving drain current and induced higher substrate current, as shown in the inset in Fig. 3-36 and Fig. 3-37. In Fig. 3-38 shown the substrate current with another three splits, hot carrier were stressed at Vds = 3.5 V and V_{GS} at $I_{sub\ max}$, the Id-Vg and transconductance characteristics were measured at Vds = 0.1V before and after stress 5000 seconds. We found that the shift of threshold voltage (ΔV_{th}) higher in SPFT sample as a function of the stress time (shown in Fig. 3-39). But degraded peak transconductance (ΔGm) higher in a-Si-700/poly1300 _ SPFT sample as shown in Fig. 3-40.



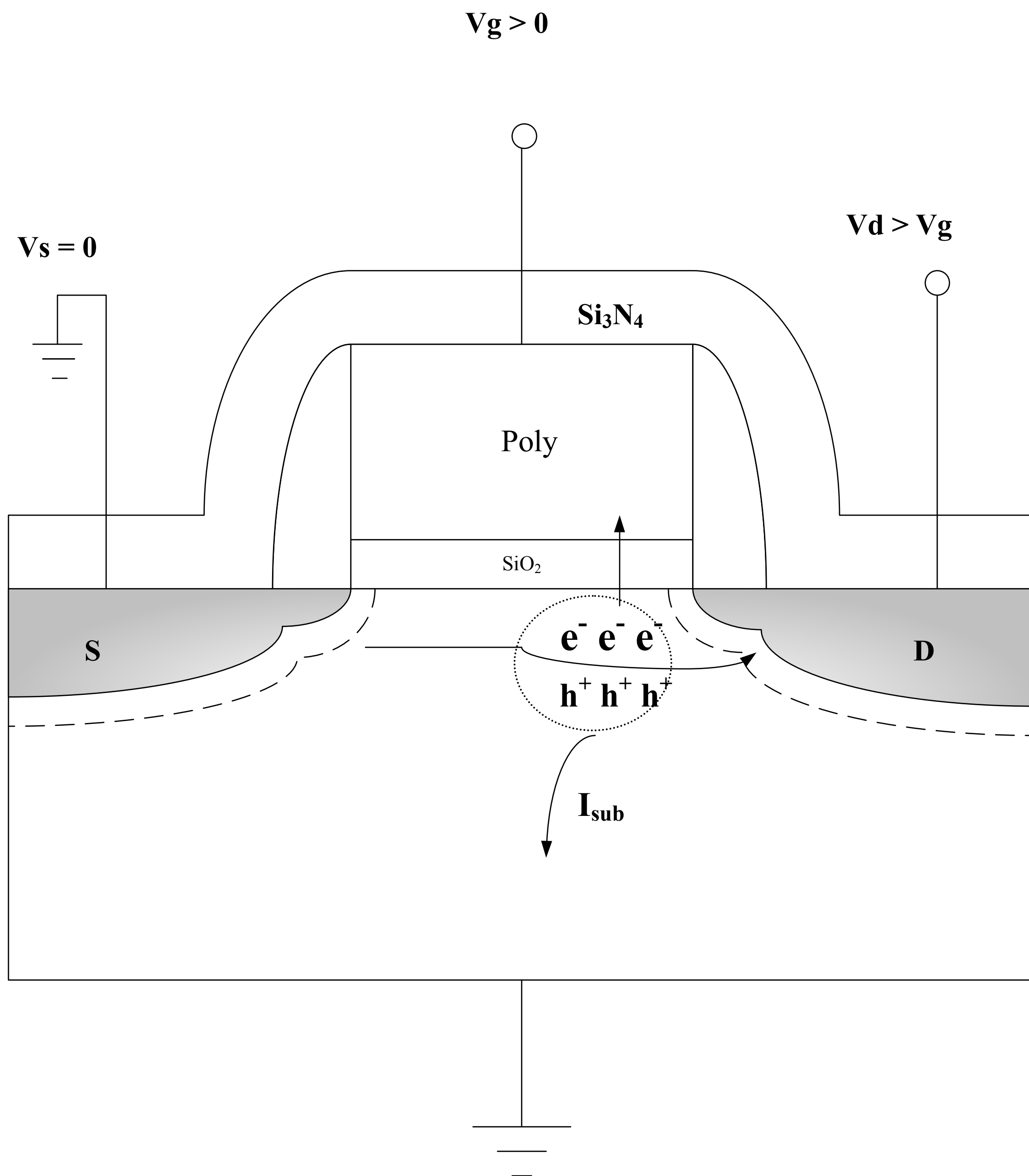


Fig. 3-31 Schematic showing electron-hole pairs generation by impact ionization due to hot electrons.

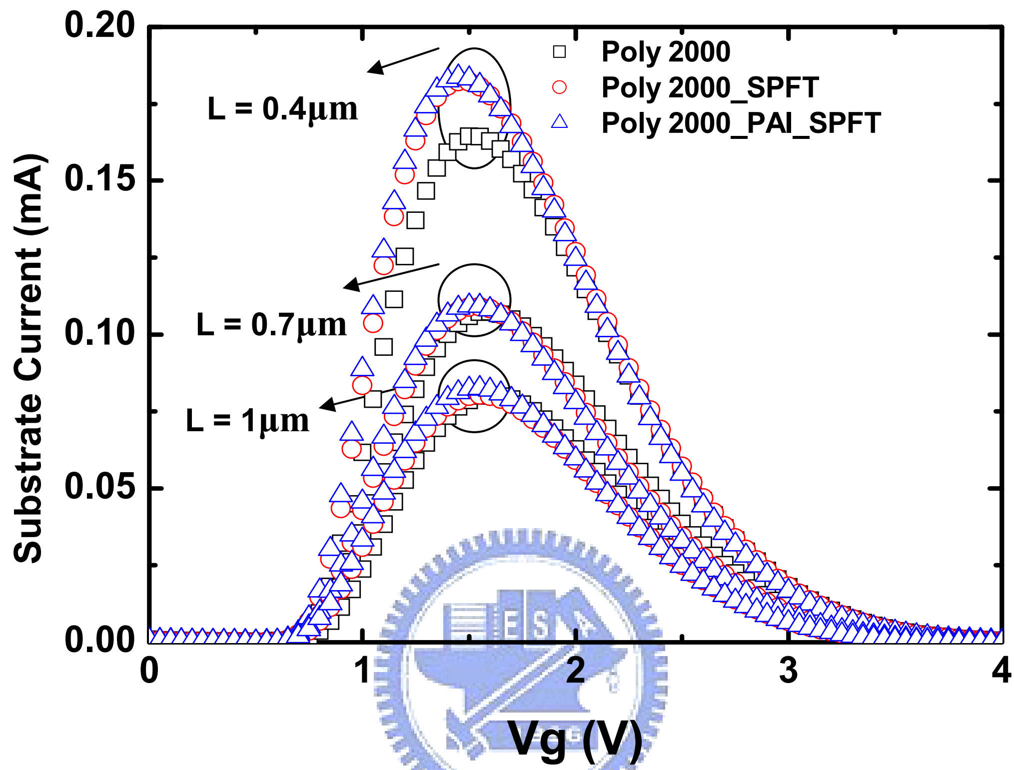


Fig. 3-32 Substrate current versus gate voltage with the three splits in different channel lengths of 0.4, 0.7, 1.0 μm.

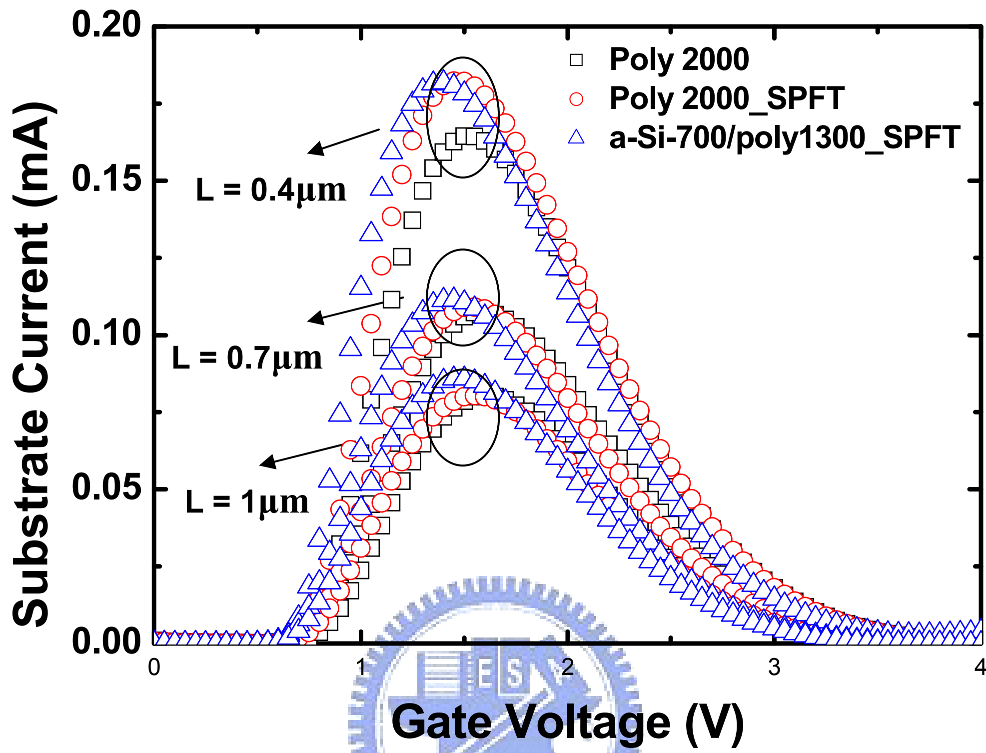
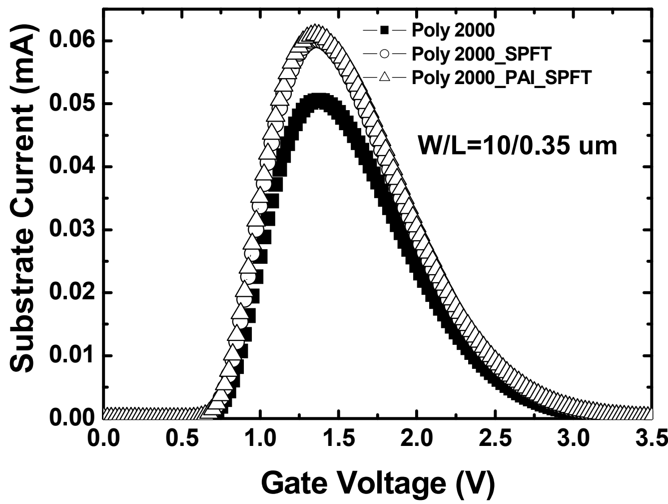
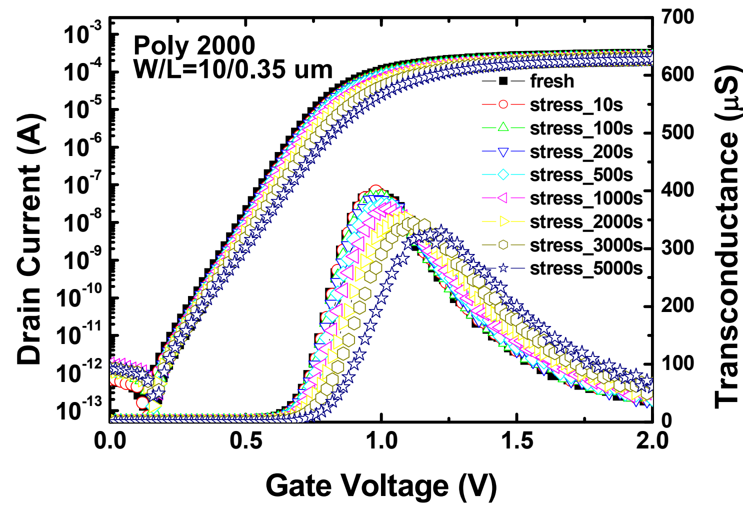


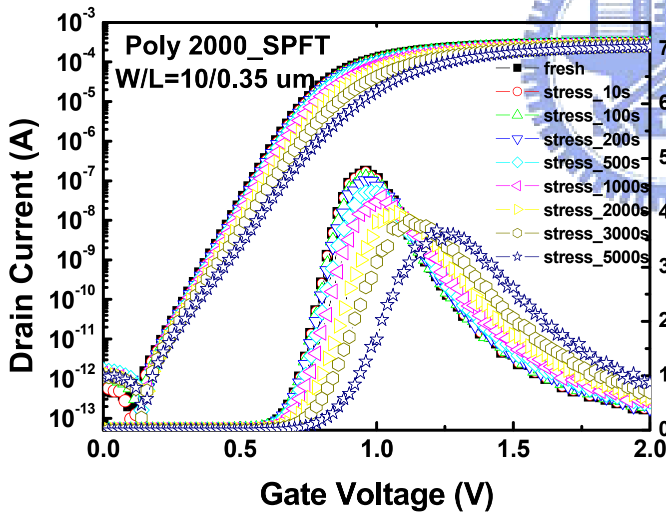
Fig. 3-33 Substrate current versus gate voltage with SPFT and a-Si/poly1000_SPFT splits in different channel lengths of 0.4, 0.7, 1.0 µm.



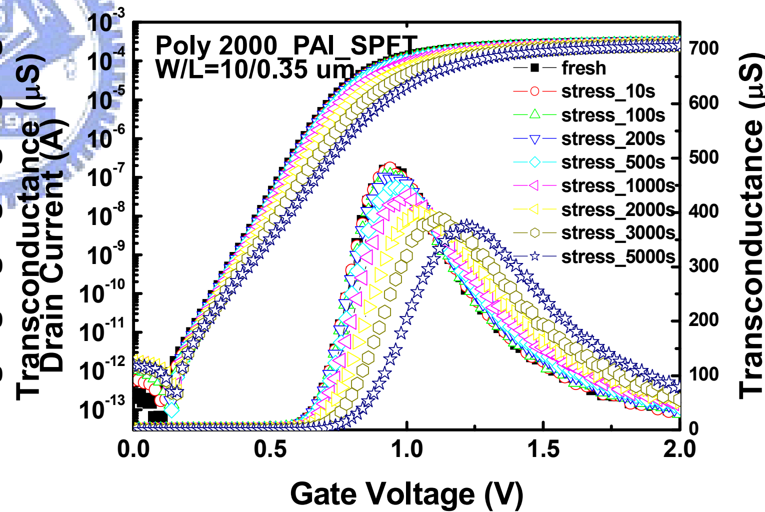
(a) Substrate current



(b) Before and after 5000s hot electron stress for the control sample.



(c) Before and after 5000s hot electron stress hot electron stress for the SPFT sample.



(d)Before and after stress 5000s stress hot electron stress for the PAI_SPFT sample.

Fig. 3-34 Hot carrier stress for the three splits at Vds=3.5v & Vg=Isub_max .

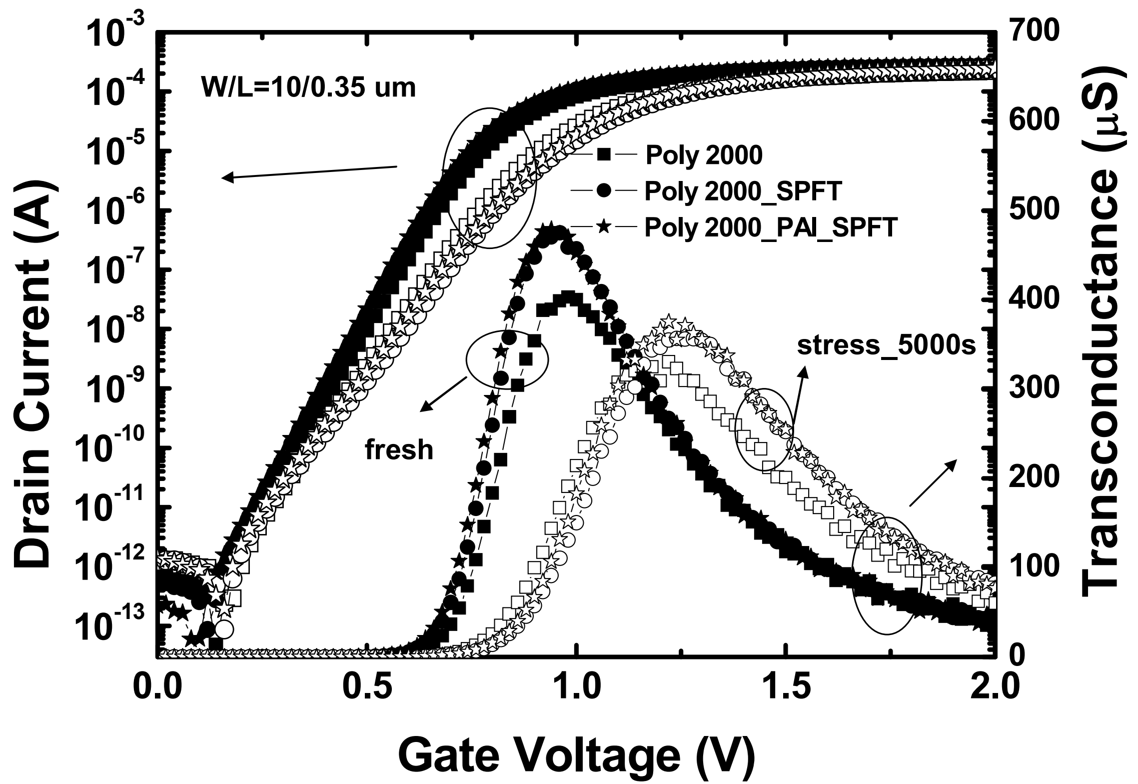


Fig. 3-35 Subthreshold and transconductance characteristics for the SPFT and PAI_SPFT samples before and after stress 5000 sec.

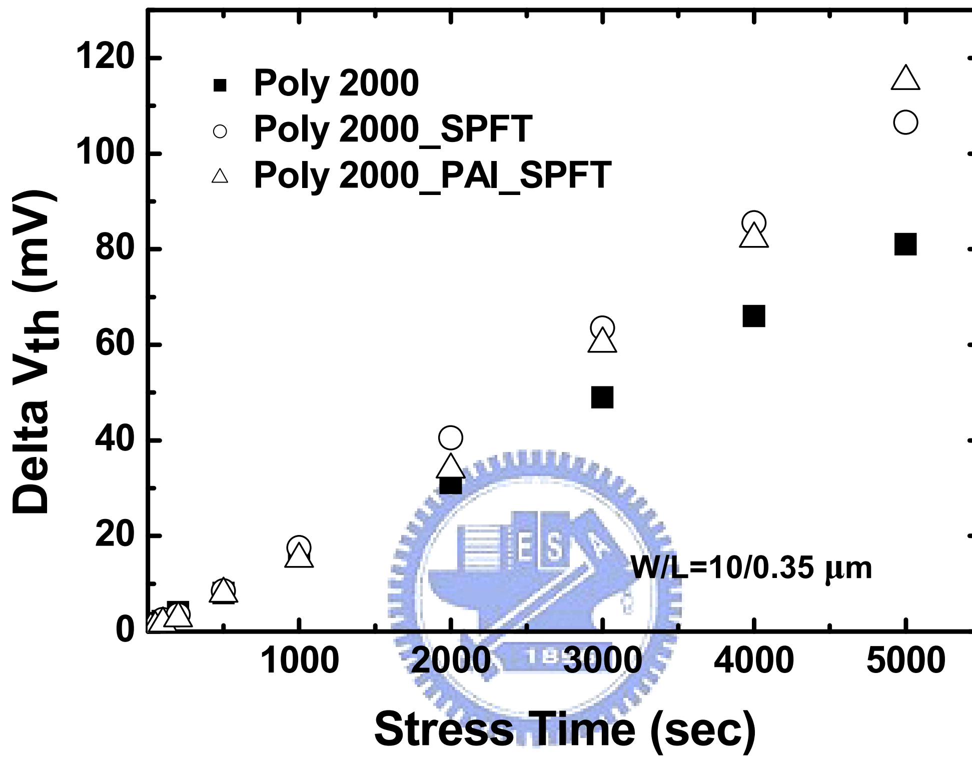


Fig. 3-36 Channel hot carrier characteristics for SPFT and PAI_SPFT samples.

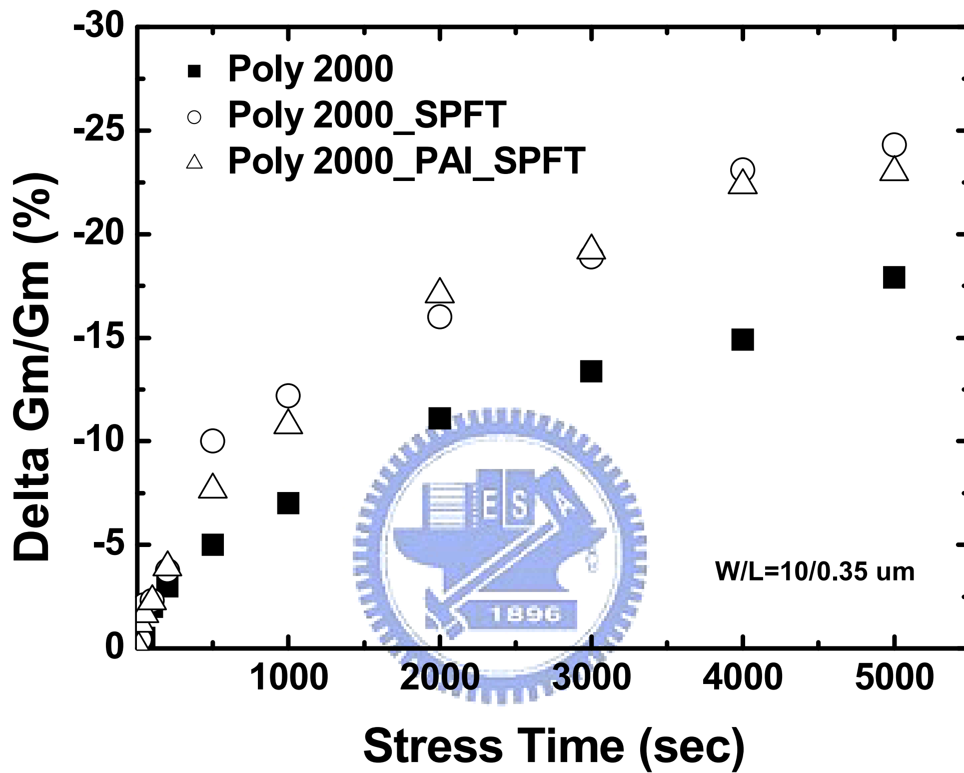
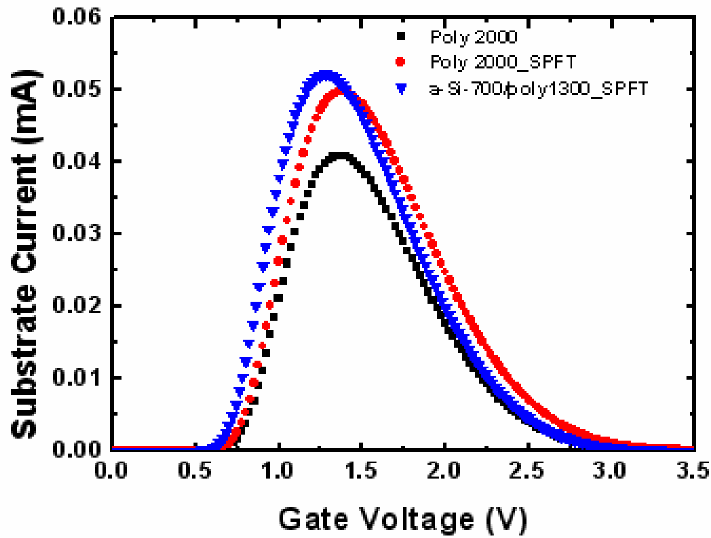
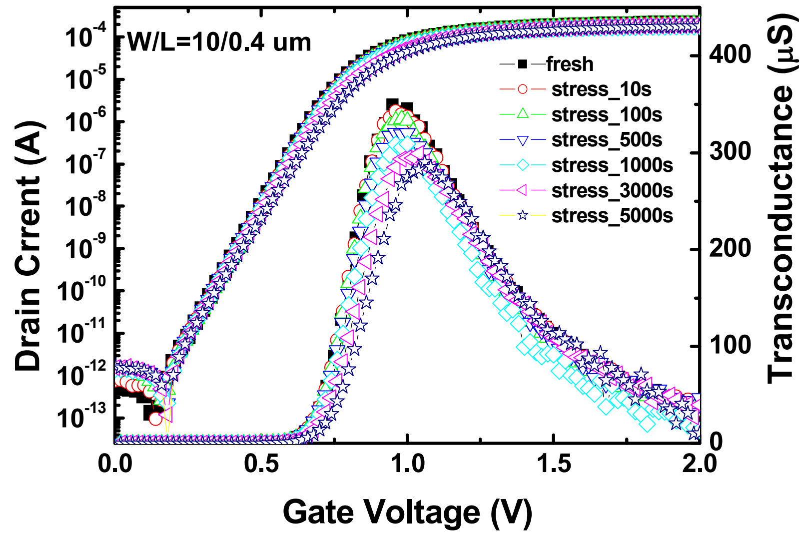


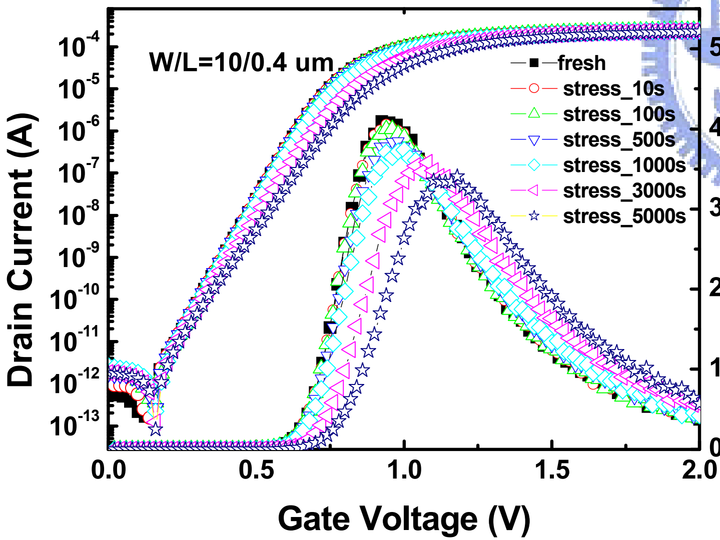
Fig. 3-37 Channel hot carrier characteristics for SPFT and PAI_SPFT samples.



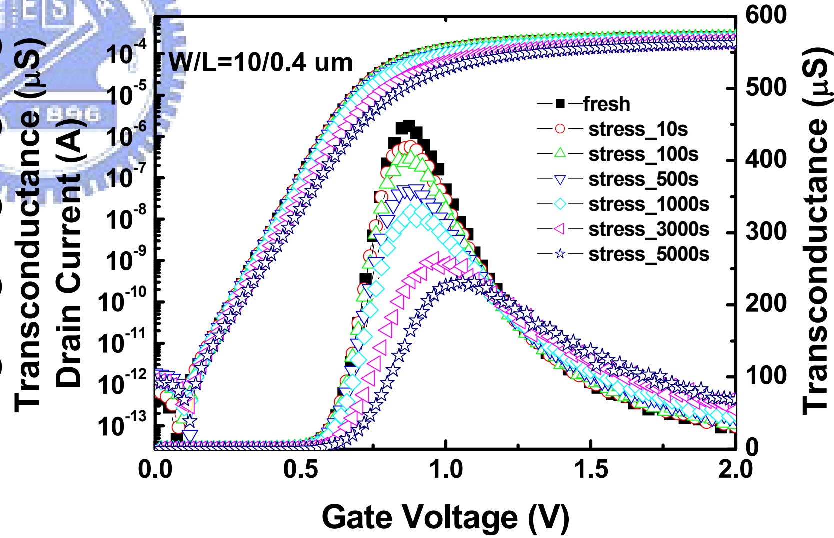
(a)



(b)



(c)



(d)

Fig. 3-38 Before and after hot carrier stress 5000 sec for the three splits at Vds=3.5v & Vg=Isub_max .(a) Substrate current (b) Poly 2000 sample (c) Poly 2000_SPFT sample (d) a-Si-700/poly1300_SPFT sample.

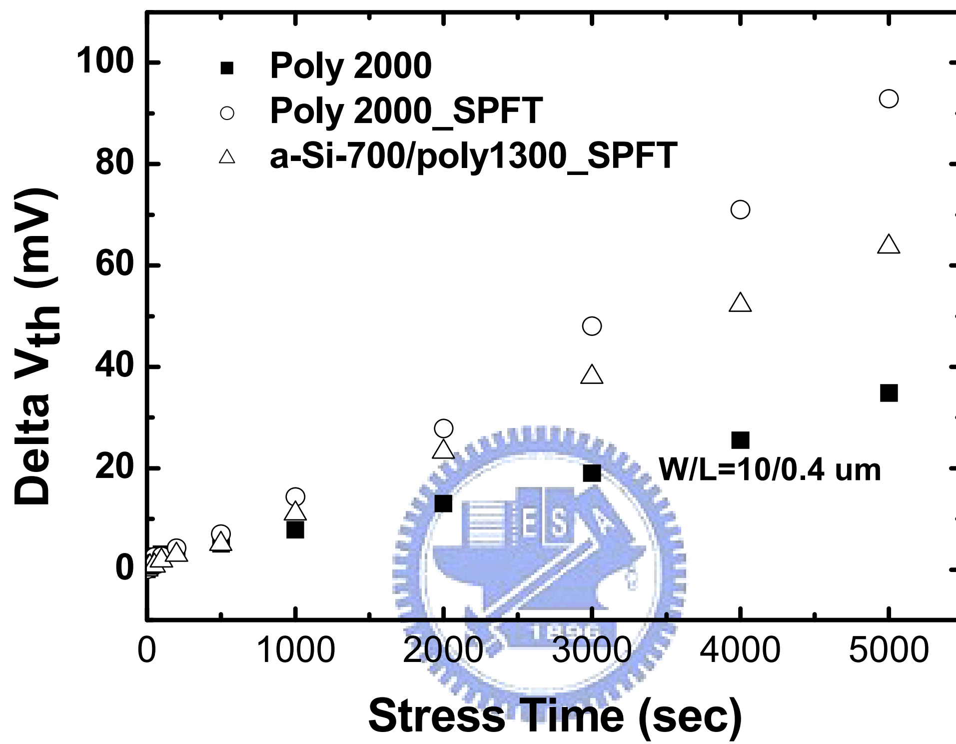


Fig. 3-39 Channel hot carrier characteristics for SPFT and a-Si-700/poly1300 _ SPFT samples.

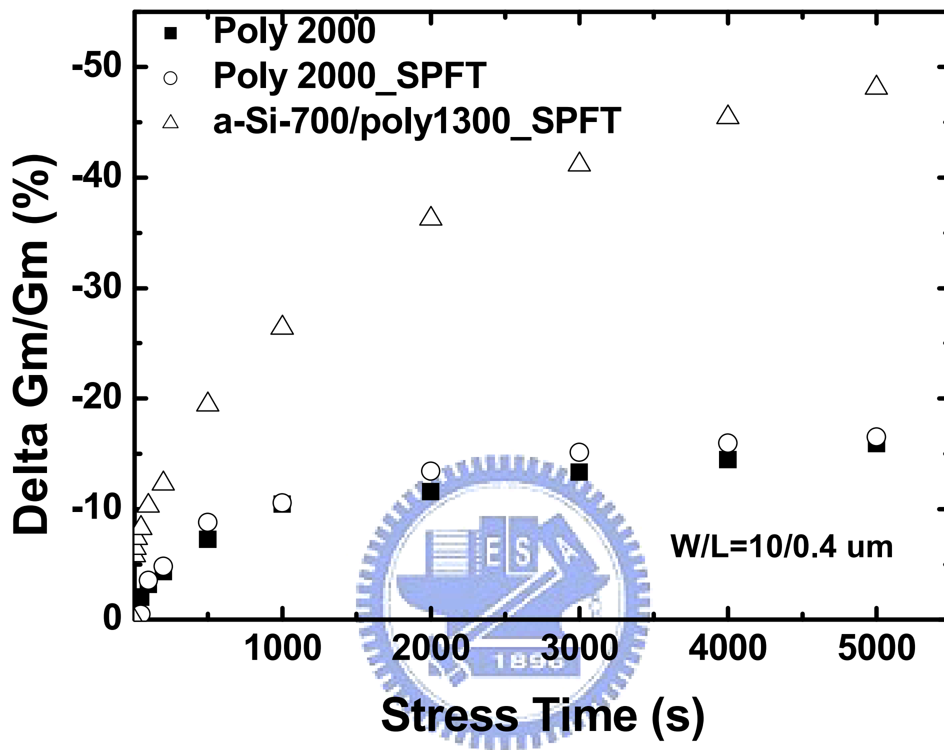
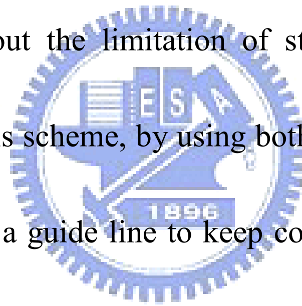


Fig. 3-40 Channel hot carrier characteristics for SPFT and a-Si-700/poly1300 _ SPFT samples.

Summary and Conclusion

In summary, we have proposed strain proximity free technique (SPFT) in nMOSETs, it could be solve etch processes problems with dense structure in logic CMOS circuit. We found that the transconductance (G_M) exhibits an 16% increase and drain current improve 10% at channel length 0.4 μm of nMOFETs with SPFT and the hot carrier stress would not serious damage. A multiple strain-gate engineering that utilizes the SPFT and a stacked a-Si/poly-Si gate structure. The G_M and current drivability could be improved by controlling the SPFT process and the thickness of stacked gate structure. Without the limitation of stressor volume in high density CMOS circuits, we believe this scheme, by using both SPFT and stacked a-Si/poly-Si gate structure will provide us a guide line to keep continuous improvement in future CMOS technology.



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