國　立　交　通　大　學

電子物理研究所

碩　士　論　文

閘極介電質氧化鉿與氮氧矽鉿之可靠度研究

Study on the Reliability of HfO_2 and HfSiON Gate Dielectric

研究生 ： 林威良

指導教授 ： 趙天生 博士

中華民國 九十七年

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中華民國 九十七 年

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Student：Wei-Liang Lin **Advisors：Dr. Tien-Sheng Chao**

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Abstract

In this thesis, PBTI degradation for HfO2 and HfSiON NMOSFETs has been demonstrated. The generated oxide trap dominated the PBTI characteristics for Hf-based gate dielectrics. In addition, the reduction of V_{TH} shift and oxide trap generation under PBTI stress indicates that the HfSiON is better than HfO2. On the other hand, the electron trapping/de-trapping effect has been investigated. As compared to HfO_2 dielectrics, the HfSiON has shallower charge trapping level due to elimination of deep dielectric vacancies, and the temperature effects are quite different between the HfSiON and HfO2 gate dielectrics. DNBTI stress on HfO_2 and HfSiON PMOSFETs has been investigated. The DNBTI model of hole trapping under NBTI stress and the electrons trapping under passivated stress have been proposed. In addition, the characteristics of the V_{TH} shift and charge pumping current under DNBTI stress indicate that the interface states are not recovered during the passivated period.

閘極介電質氧化鉿與氮氧矽鉿之可靠度研究

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摘要

在這篇論文裡,我們展示 HfO_2 和 HfSiON 介電質的 PBTI 退化特性,氧化層中生成的捕捉電荷主導了Hf-base 介電質得PBTI特性,另外,再PBTI stress中,較少的臨界電壓飄移與氧化層捕捉電荷的生成證實了HfSiON相較於HfO_2有較好的特性.另一方面,我們也討論了電子的 trapping/de-trapping 效應,與HfO_2介電質相比,由於消除了較深層的介電質缺陷HfSiON有較淺的捕捉能階,而在不同溫度下的表現,HfO2介電質與HfSiON介電質有相當程度的不同.HfO_2與HfSiON P 型場效電晶體在動態的 NBTI stress 也再論文中一併討論,我們提出在 NBTI stress與passivated stress下,電洞捕捉模型.同時,我們由臨界電壓的改變與 charge pumping current 的特性得知,因為 stress 所造成的表面狀態在鈍化的過程中將不會有回復的現象.

誌 謝

趙天生老師是學生第一個要感謝的人。謝謝老師給學生這個機會在實驗室裡學習，再我無處可歸的時候收留我, 並且指導與充實學生在專業知識上的本質學能。

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此論文獻給以上諸位!

林威良

誌於 新竹交大

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Chapter 1

Introduction

1-1 General Background

Reliability issues, such as negative-bias temperature instability (NBTI) [1-2] positive-bias temperature instability(PBTI) and hot-carrier injection (HCI) [3-4], that could induce threshold voltage shift and performance degradation in MOSFETs become a serious concern for realizing highly reliable integrated CMOS devices. Threshold voltage shift and performance degradation in MOSFETs are dominated by oxide trap and interface trap [5-6], high-*k* dielectric materials are especially advantageous for low-power application and for thickness uniformity control owing to the thicker physical thickness. Among high-k gate dielectric materials, Hf-based gate dielectric including HfO_2 and Hf-silicate are the attractive materials because they have good device characteristics and compatible with the conventional polysilicon gate process [7-10]. However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be better identified. Bias temperature instability (BTI) has been recognized as one of the critical concern in the reliability of modern CMOS devices.

In conventional SiO_2 gate oxides, NMOS under PBTI stress shows little threshold voltage degradation and hence is not a reliability concern while PMOS under NBTI

stress has a continued reliability issue as the gate oxide thickness is scaled thinner[11]. On the contrary, unlike conventional SiO_2 gate dielectrics, NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics [12].

Negative-bias temperature instability (NBTI) occurs in PMOS device which stresses with negative gate voltages at elevated temperature. In MOS circuits, it occurs most commonly during the "high" state of *p*-channel MOSFETs inverter operation. It also leads to timing shift and potential circuit failure due to increased spreads in signal arrival in logic circuits.

1-2 Motivation

The aggressive CMOS device scaling has been reaching the physical limit of conventional SiO2 MOSFETs as a result of significant direct tunneling current through ultrathin oxides. The resultant intolerable standby power consumption has made further oxide scaling impractical. High-k gate dielectric and metal gate expected to replace the conventional SiO2 /polysilicon gate stack to meet aggressive gate leakage current specification for advanced CMOS technologies. Replacement of SiO2 gate dielectric by high-k materials with larger physical thickness will reduce gate leakage current. Among the candidates, Hf-based materials are most promising, and considerable efforts have been devoted to their film compositions, process

optimization, as well as reliability assessment and analysis. Recently, HfSiON and HfO2 have been successfully integrated into CMOS devices as gate dielectric for low-power applications with good reliability, comparable mobility (as SiO2), and greatly reduced gate leakage. Threshold voltage Vt of a field effect transistor (FET) is observed to shift with stressing time and this stress induced Vt shift is an important transistor reliability issue. Vt shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping.

1-3 Bias temperature instability stress mechanisms

One of the main constraints for scaling down MOSFET's dimensions is the device instability. Degradation of MOSFET's can be caused by hot carrier stressing, Fowler–Nordheim tunnelling injection and the bias temperature stressing (BTS). The former two have been investigated extensively, while the latter has received relatively less attention, although it is one of the earliest identified reliability problems. This is not because the bias temperature instability (BTI) has been fully understood, but because the BTI in modern MOS integrated circuit has been greatly reduced empirically. However, recent experimental results have shown that the BTI can still make a considerable contribution to the degradation of small size MOSFET's. Further efforts have to be made, therefore, to understand the BTI phenomenon.

Positive bias temperature instability (PBTI) is often reported to be one of the

primary reliability concerns in high-k gate stacks. It is generally agreed that PBTI in these gate stacks occurs due to reversible electron trapping in existing trap sites. Several groups have reported different techniques to mitigate the PBTI issues in high-k gate stacks, such as reducing the thickness of the dielectric. During PBTI stress, gate will be biased at positive voltage which induce electrons from inversion layer trapped in gate dielectric and damage the interface between gate dielectric and silicon substrate. Fig.1 shows the charge trapping behavior during PBTI stress.

Negative bias temperature instability (NBTI) has been known since the very early days of MOS device development. NBTI, occurring in p-channel MOS devices stressed with negative gate voltage at elevated temperatures, manifests itself as absolute drain current and transconductance decrease, and absolute threshold voltage increase. In digital circuits fig.2, it occurs most commonly during the “high” state of p-channel MOSFETs inverter operation. It also leads to timing shifts and potential circuit failure due to increased spreads in signal arrival in logic circuits. During NBTI stress, the injected holes will induce interface state generation, and the holes also trap in gate dielectric. Fig.3 shows the charge trapping behavior during NBTI stress.

1-4 Thesis Organization

This thesis divided into four chapters. In chapter 2, shows the NMOS with high-k gate dielectric fabrication and electrical measurements. The experimental

measurement include effective electron mobility, charge pumping current, threshold voltage shift. In chapter 3, we demonstrated Negative-bias temperature instability (NBTI) characteristics on PMOS with high-k gate dielectric , and compare the various charge pumping current and different appearance of Trapping/De-Trapping at different stress voltage and different temperature.

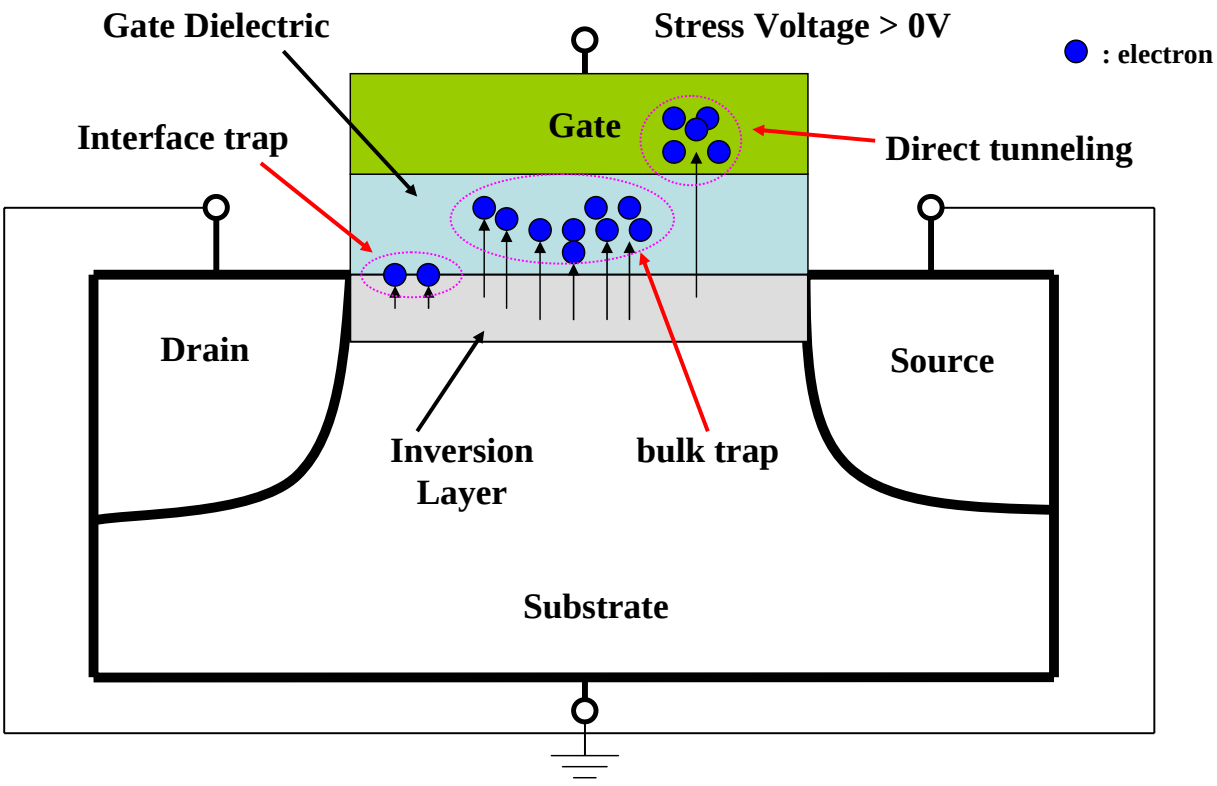


Figure 1.1 The charge trapping behavior during PBTI stress

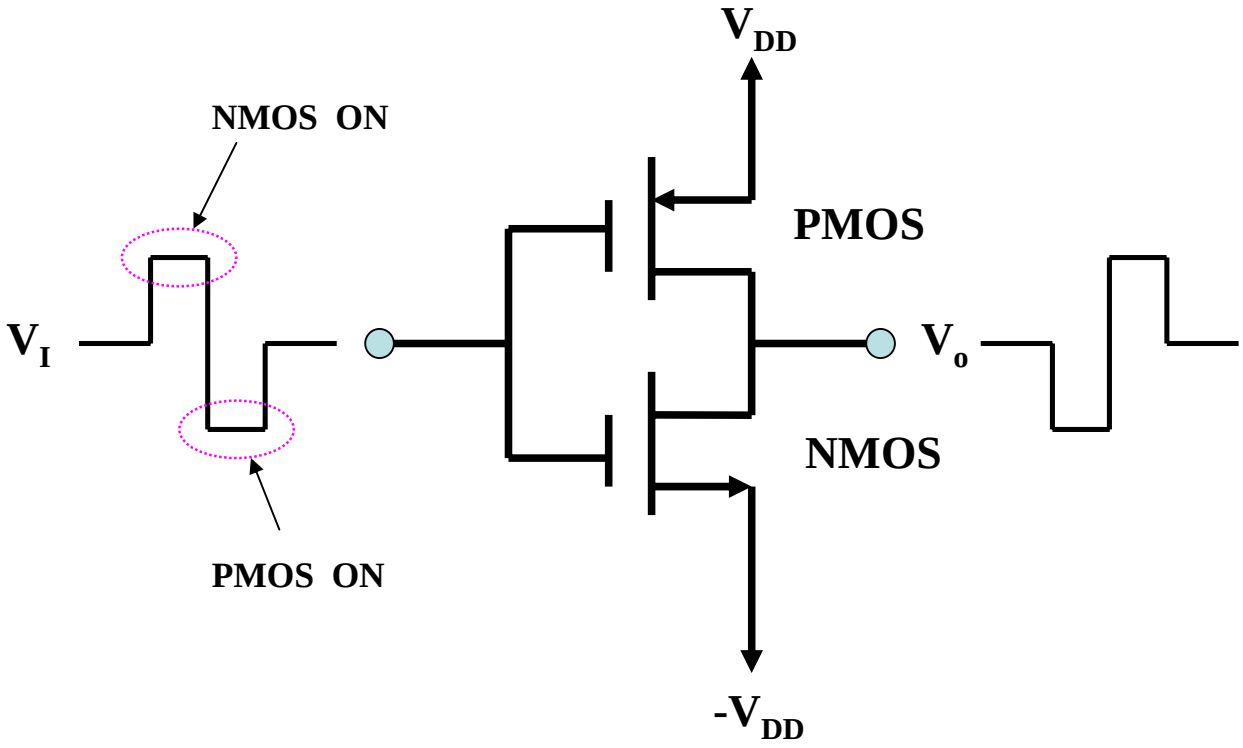


Figure 1.2 Illustration of inverter operation

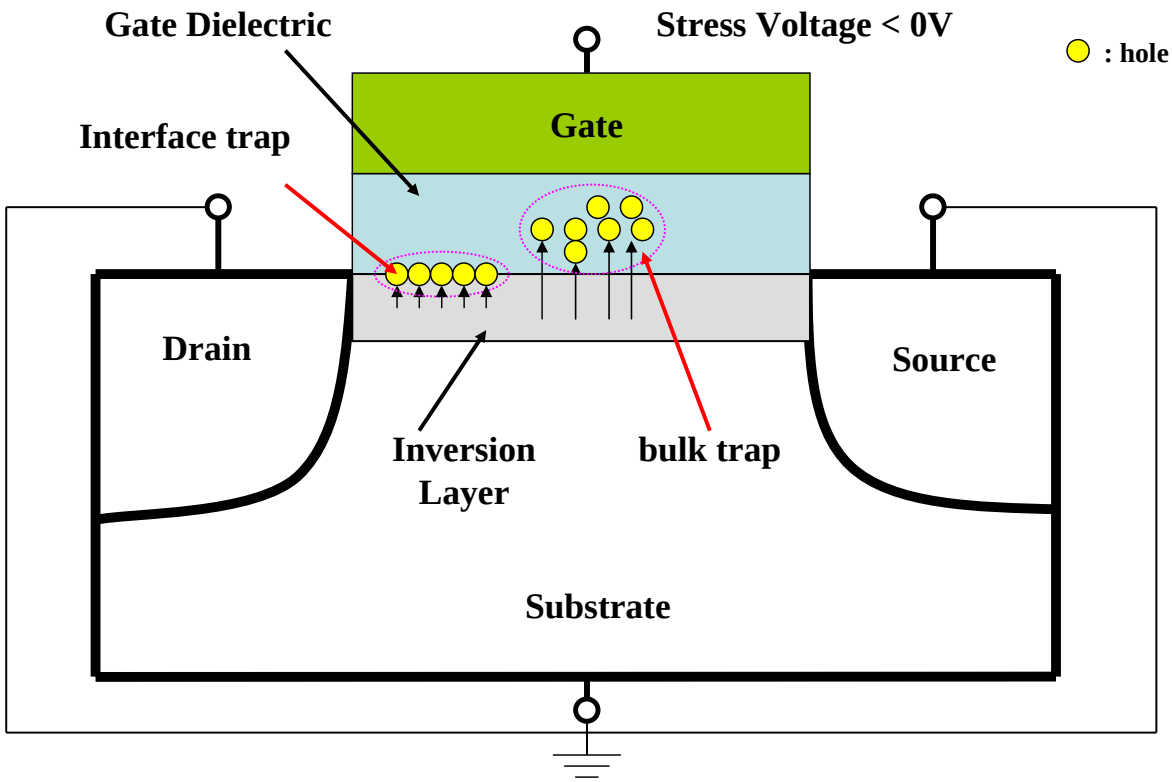


Figure 1.3 The charge trapping behavior during PBTI stress

Chapter 2

Trapping and De-trapping Characteristics in PBTI and Dynamic PBTI between HfO_2 and HfSiON Gate Dielectrics

2-1 Introduction

High-k dielectrics are especially advantageous for low-power application. Among high-k gate dielectric materials, Hf-based gate dielectric including HfO_2 and Hf-silicate are the attractive materials because they have good device characteristics. However, before Hf-based gate dielectrics being successfully integrated into future technologies, their reliability characteristics still need to be better identified. NMOS positive bias temperature instability (PBTI) could be a potential scaling limit of CMOS technology with Hf-based gate dielectrics[13-16]. Most of the previous studies showed a significant positive threshold voltage shift for the high-k gate stack under PBTI stress, which was attributed to the preexisting traps in the high-k layer or the holes induced oxygen vacancy traps[17-21]. In addition, one of the main issues for high-k gate dielectrics is the charge trapping/de-trapping characteristics during reliability test. Since electrons can be trapped and de-trapped in the high-k dielectrics with a minimal residual damage to its atomic structure, a threshold voltage instability associated with electron trapping/detrapping in high-k layer can significantly affect

the transistor performance[22].

2-2 Device Fabrication

NMOS devices were fabricated by state-of-the-art 300 mm wafer foundry technology. Shallow trench isolation (STI) was performed for devices isolation followed by super-steep retrograde well formation. The high-K dielectric including HfO_2 and Hf-silicate were deposited by atomic-layer deposition (ALD). Chemical oxide was used as the interfacial layer unless it is specifically mentioned. The nitridation of HfSiO with Hf/(Hf+Si) ratio of 50% was carried by NH_3 annealing in the ambient. After shallow source/drain extensions and pocket implantation, tetraethoxysilane (TEOS) liner and low-temperature silicon nitride were processed in sequence to form a sidewall spacer. Modified S/D implants were adopted to improve activation and junction capacitance while maintaining good SCE. The fabrication of a heavily doped source/drain junction by implantation was followed by a rapid thermal annealing (RTA) of 1000 ^{o}C for 5s for S/D activation and thermal stability of HfSiON

2-3 Results and Discussion

2-3-1Device Performance

Figure 2-1 shows the high-frequency C-V characteristics at 100 kHz for HfO_2 and HfSiON gate dielectrics, respectively. The well C-V characteristics under accumulation, depletion and inversion regions can be observed in this work for both HfO_2 and HfSiON gate dielectrics. The effective oxide thickness was also extract

from these C-V curves under accumulation without considering quantum effects. Since the EOT were almost the same (1.3 nm) for HfO_2 and HfSiON gate dielectrics as shown in Fig. 2-1, therefore, the reliability test can be analyzed by biasing the same gate voltage in this work.

At a higher field (>1 MV/cm), the mobility of HfSiON gate dielectric is large than HfO_2 gate dielectrics as shown in Fig. 2-2. We speculate that the Si-O and Si-N bodings were formed for the HfSiON gate dielectrics resulting in annihilation of oxygen vacancies to offer mobility enhancement at high electric field.

2-3-2 PBTI Degradation for HfO_2 and HfSiON Gate Dielectrics

In order to understand the mechanism of PBTI in our high-k dielectrics, Figure 2-3 shows the threshold voltage degradation (ΔV_{th}) of HfO_2 and HfSiON gate dielectrics under PBTI stress at room temperature. Figures 2-4 show the charge pumping current (I_{CP}) before and after PBTI stressing. Contrast to ΔV_{th} , the HfO_2 gate dielectrics have better HfO_2/Si interface due to its less initial I_{CP}. However, the Icp of HfSiON dielectrics is larger than HfO_2, but the increase in I_{CP} during PBTI stress is almost identical for HfO_2 and HfSiON gate dielectrics, as shown in Fig. 2-5. From Fig. 2-5 & 2-6, it is noted that the N_{it} increase is quite low ($< 2\times10^9$ cm^{-2}) in this work[11]. Figure 2-7 shows the N_{ot} increase for both of HfO_2 and HfSiON dielectrics during PBTI stress, respectively[12].

Therefore, the charge trapping model for Hf-based gate dielectrics under PBTI stress was illustrated in Fig.2-8.

2.3.3 Temperature-Dependent De-trapping Characteristics for HfO_2 and HfSiON Gate Dielectrics

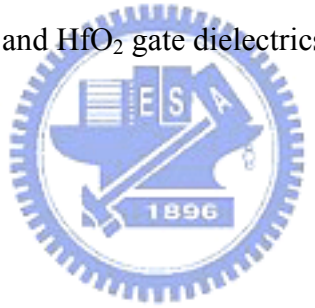
The temperature-dependent trapping and de-trapping characteristics for both HfO_2 and HfSiON splits are also investigate in this study. In Figs. 2-9, we compare the HfO_2 and HfSiON gate dielectrics under PBTI stress (Vg = +2.5 V) w/ and w/o hold time at different temperatures, including 25, 75 and 100 ^{o}C. The obvious improvement in PBTI characteristics was observed for HfSiON gate dielectrics while the hold time is 100 s as indicated in Fig. 2-9(b). This result indicates that the electron de-trapping will be easily occurred in HfSiON gate dielectrics. It means that the extra Si-O and Si-N bodings effectively removed the dielectric vacancies to have a lower trapping cross section and a lower concentration of generated traps, and reduce some trapping levels. This implies that some deep electron traps are effectively eliminated for HfSiON gate dielectrics, resulting in the characteristics as shown in Figs. 2-10(a) & (b). In Fig.2-10 (a), it indicates that the HfO_2 gate dielectric generated deeper charge trap during PBTI stress and trapped electrons need higher thermal energy to de-trap from HfO_2 film. In Fig.2-9 (b), because of some deeper trap were effectively eliminated; the ΔV_{TH} in PBTI stress with 0 s hold time is larger than ΔV_{TH} with 100 s

hold time at different temperatures. Figures 2-11(a) & (b) illustrate the charge trapping/de-trapping models for HfO_2 and HfSiON gate dielectrics under PBTI stress respectively. As compared to HfO_2 dielectrics, the HfSiON dielectrics has deep charge trapping level under PBTI stress as illustrated in Fig. 2-11(b).

In Figs. 2-12, we also compare the HfO_2 and HfSiON gate dielectrics under dynamic positive bias temperature instability (DPBTI) stress (Vg = +2.5V under stress, while Vg=0V under passivation) at 25°C, 75°C, 100°C, respectively. In Fig. 2-12(a), the ΔV_{TH} of HfSiON is lower than that of HfO_2 at 25°C due to the annihilation of oxygen vacancies removed by the Si-O and Si-N bonding. From the results under higher temperature DPBTI stress in Figs. 2-12(b) and (c), we speculate that electrons need higher thermal energy to trap in deep level in HfSiON gate dielectric. In addition, the recovery amplitudes at different stress temperature during passivation periods are almost identical for both HfO_2 and HfSiON splits. Finally, we extracted the coefficient n and K from DPBTI stress and summarized in Table I , where n stands for trapping /de-trapping ability and K is the amplitude which is function of stress voltage Vg, temperature, dimension size, and process conditions. From the n and K values in Table I , the temperature effects are quite different between the HfSiON and HfO_2 gate dielectrics.

2-4 Summary

The generated oxide trap during PBTI stress will dominate the PBTI characteristics for Hf-based gate dielectrics. In addition, the degree of threshold voltage degradation and oxide trap generation under PBTI stress indicates that the HfSiON thin film quality is better than HfO_2 attributed to HfSiON gate dielectrics had the extra Si-O and Si-N bodings resulting in annihilation of oxygen vacancies. As compared to HfO_2 dielectrics, the HfSiON has shallower charge trapping level under PBTI stress due to elimination of deep dielectric vacancies. Finally, the temperature effects are quite different between the HfSiON and HfO_2 gate dielectrics.



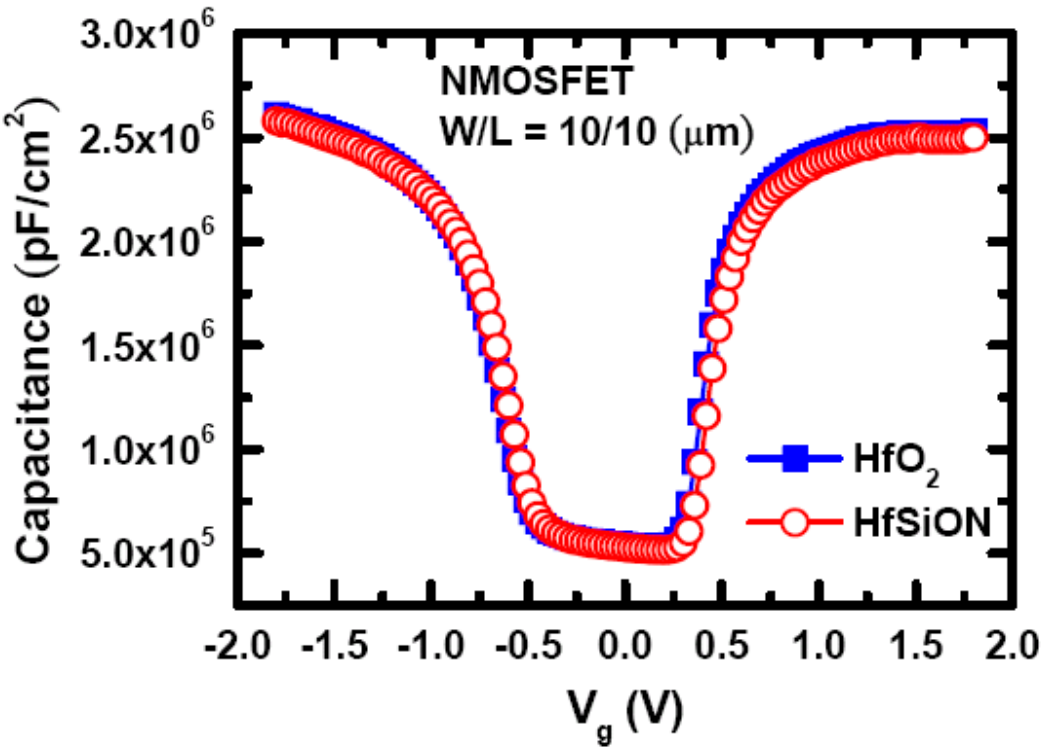


Fig. 2-1 High-frequency C-V characteristics at 100 kHz for NMOSFET with HfO_2 and HfSiON gate dielectrics, respectively.

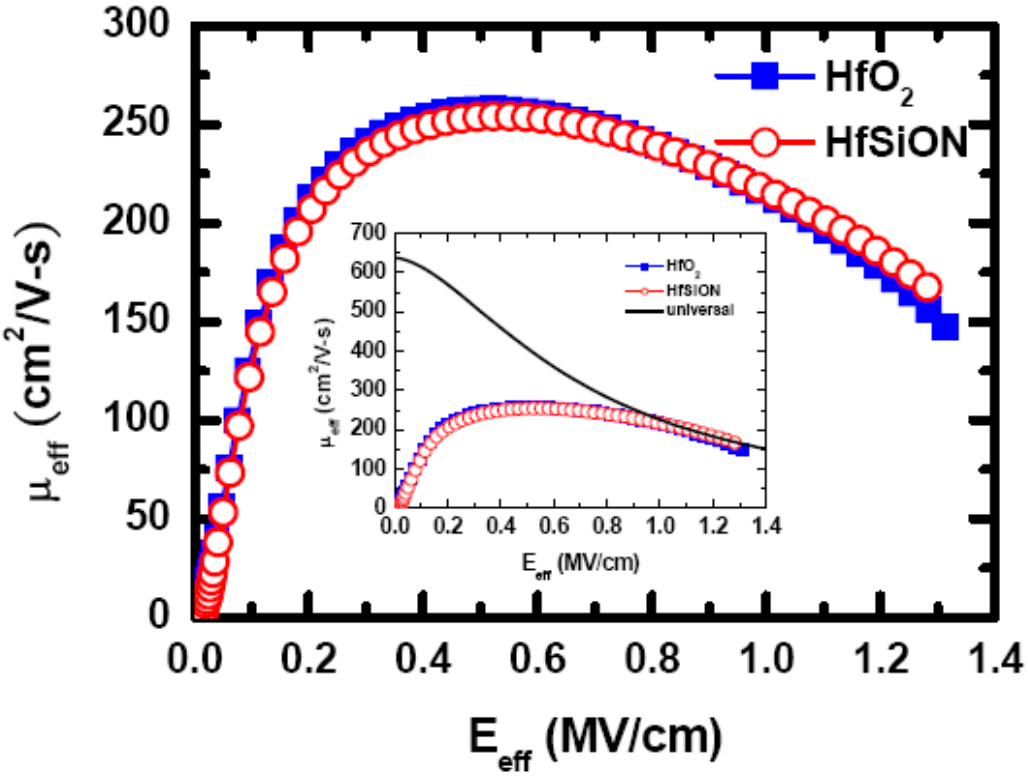


Fig. 2-2 The effective electron mobility measured on HfO_2 and HfSiON gate dielectrics using split CV method.

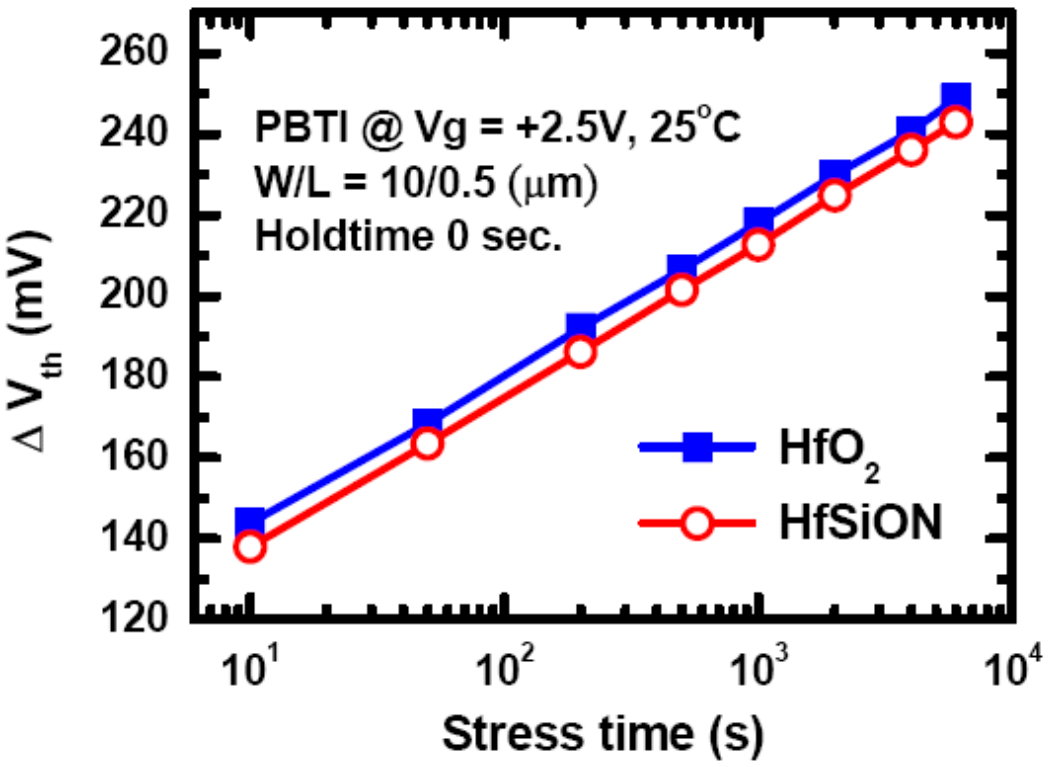


Fig. 2-3 ΔV_{th} of HfO_2 and HfSiON gate dielectrics under the same PBTI stress (Vg = +2.5 V) at room temperature.

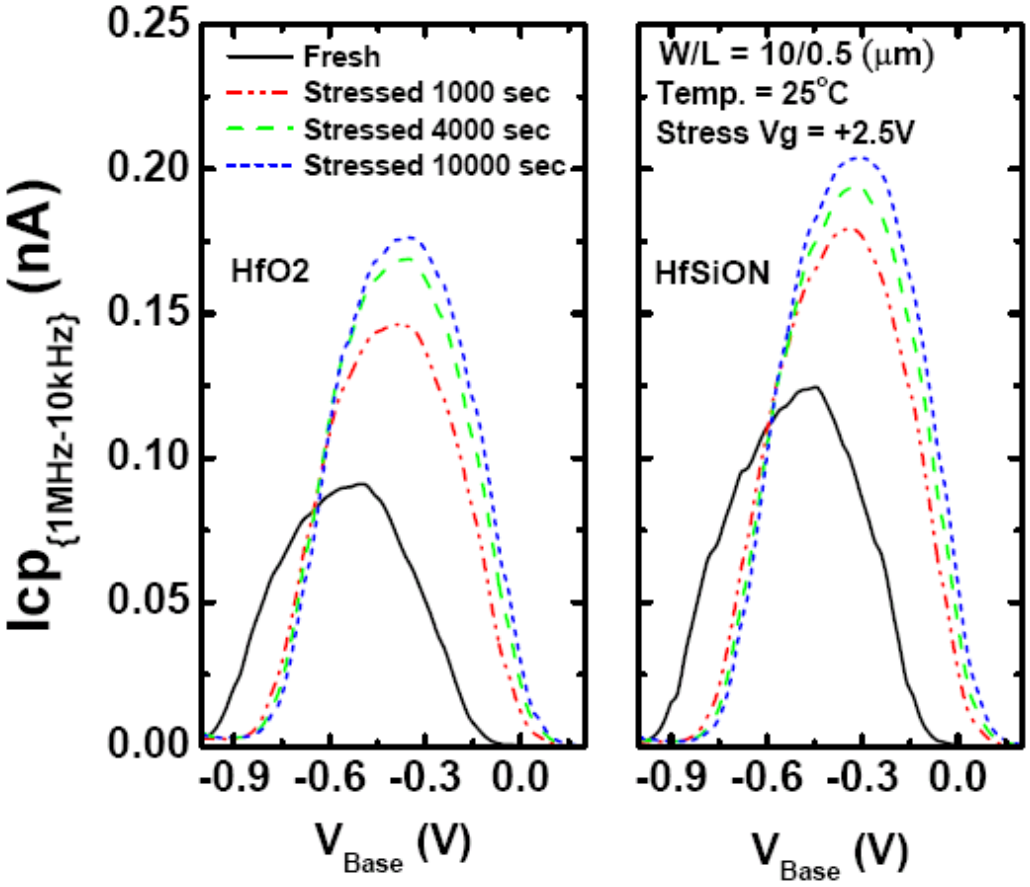


Fig. 2-4 Charge pumping current (I_{CP}) before and after PBTI stressing at +2.5V for HfO_2 and HfSiON dielectrics, respectively

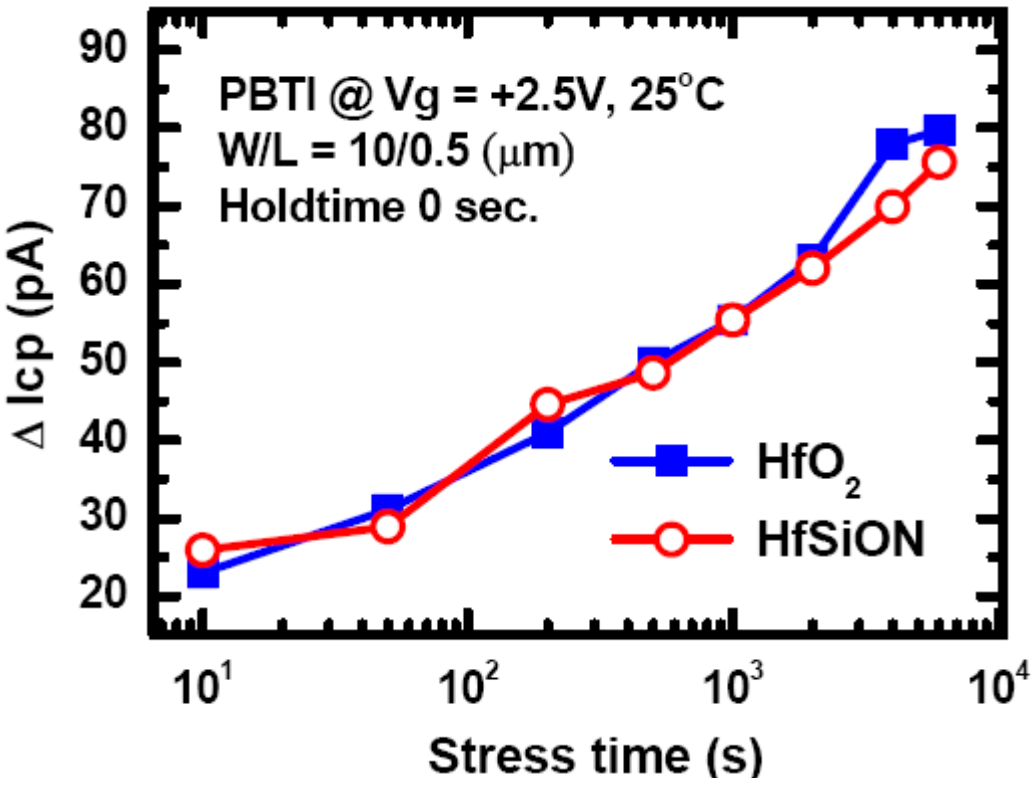


Fig. 2-5 Charging pumping increase (ΔI_{CP}) of HfO_2 and HfSiON gate dielectrics during the same PBTI stress bias (Vg = +2.5 V) at room temperature.

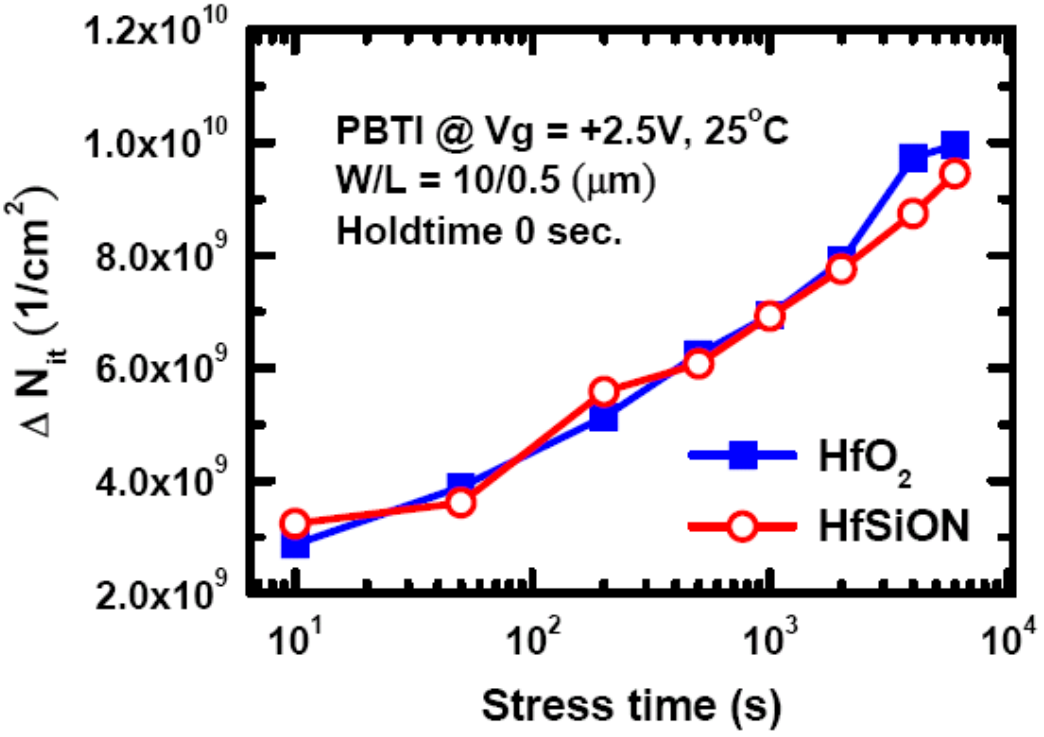


Fig. 2-6 Interface trap increase (ΔN_{it}) which extracted from ΔI_{CP} of HfO_2 and HfSiON gate dielectrics during the same PBTI stress bias (Vg = +2.5 V) at room temperature.

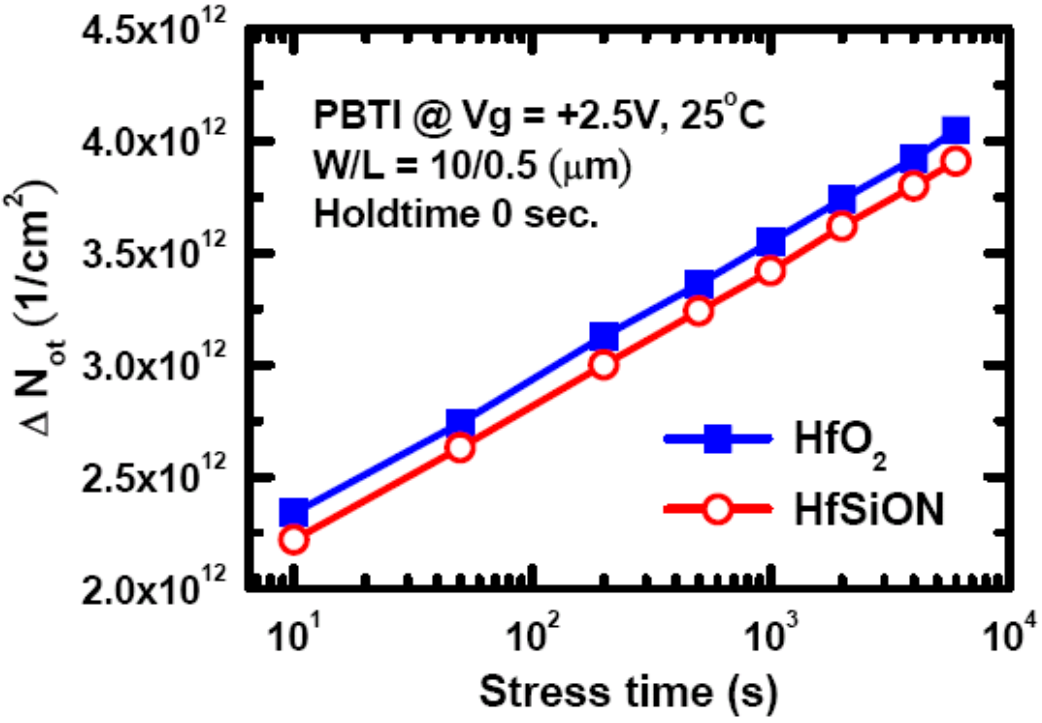


Fig. 2-7 Generated oxide trap (ΔN_{ot}) in the bulk of higk-k film during PBTI stress for both of HfO_2 and HfSiON dielectrics, respectively

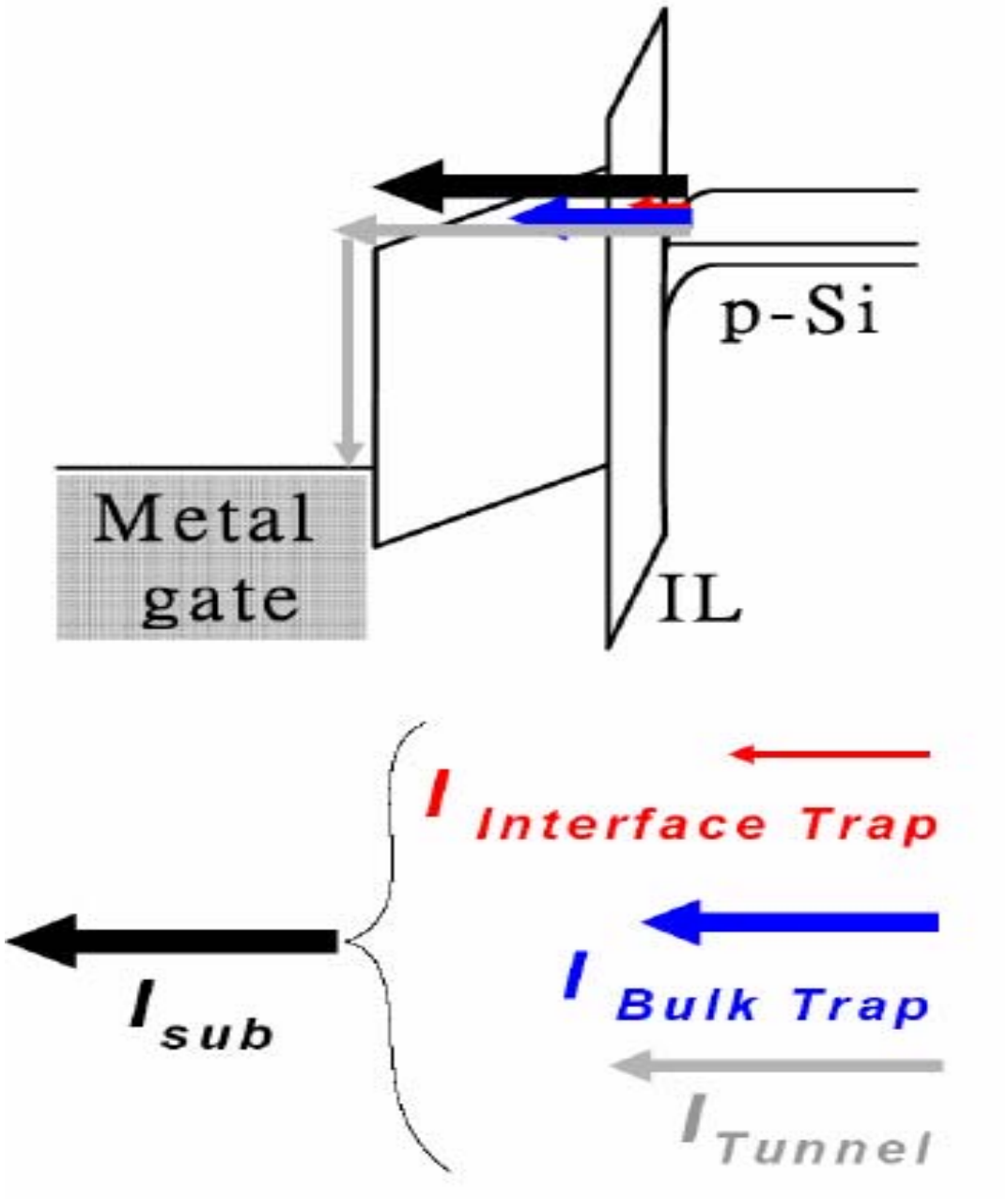


Fig. 2-8 Illustration of electron trapping model for Hf-based gate dielectrics under PBTI stress.

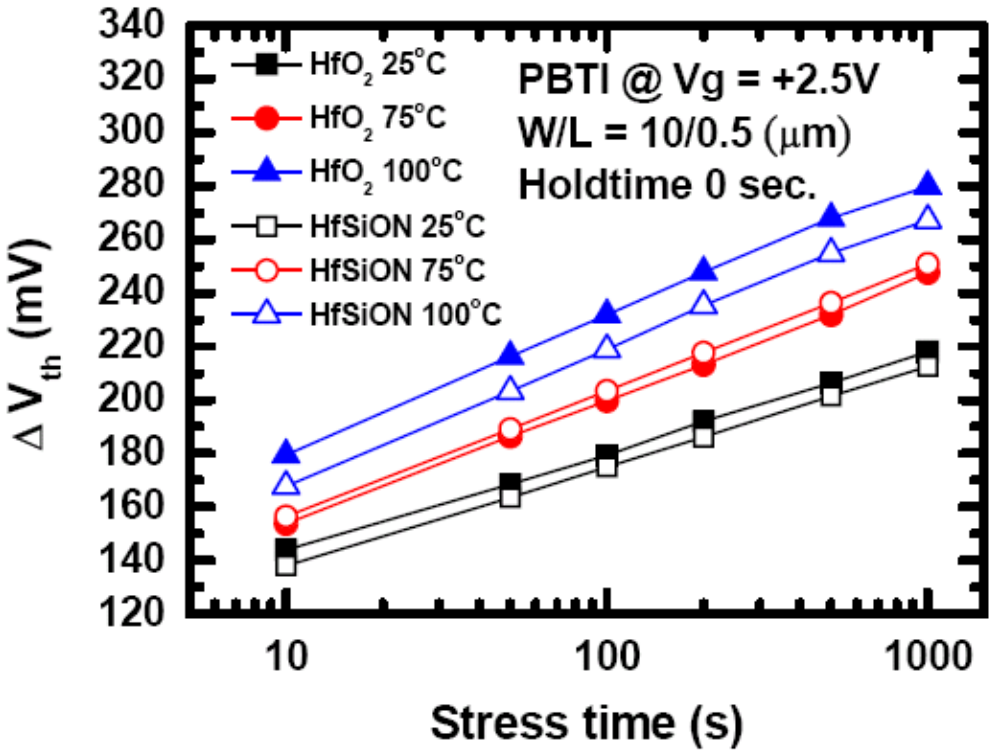


Fig. 2-9(a) ΔV_{th} of HfO_2 and HfSiON gate dielectrics during PBTI stress (Vg = +2.5 V) with no hold time at different temperatures, including 25, 75 and 100 ^{o}C.

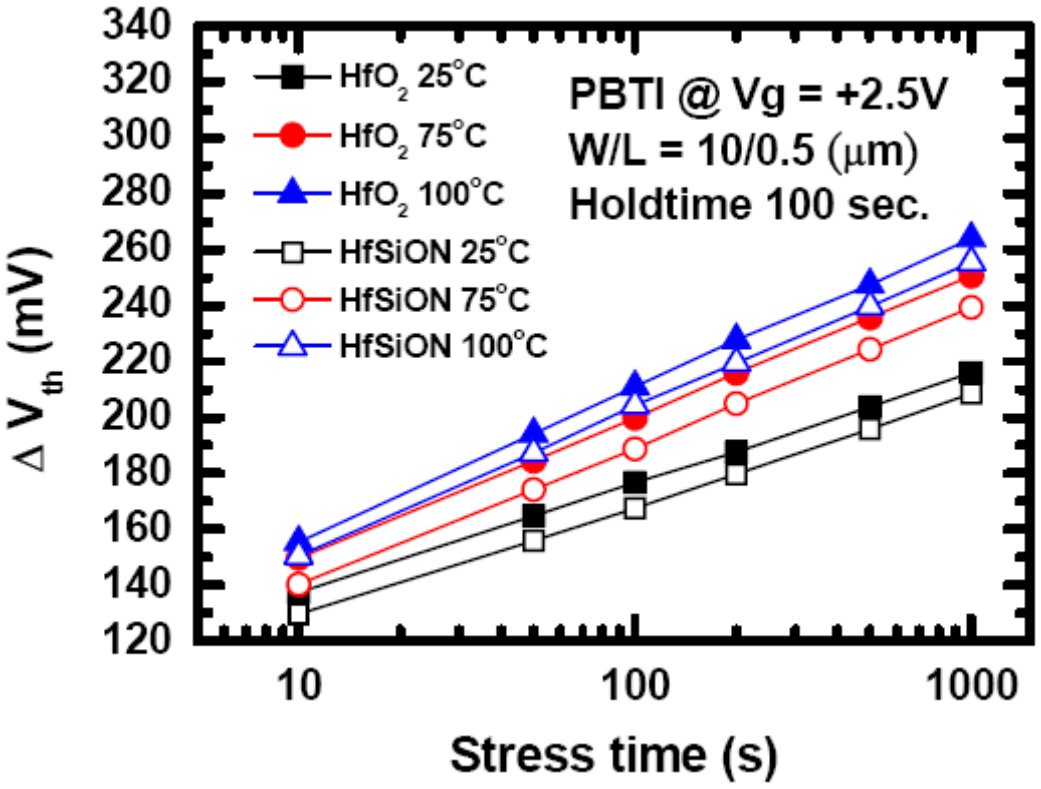


Fig. 2-9(b) ΔV_{th} of HfO_2 and HfSiON gate dielectrics during PBTI stress (Vg = +2.5 V) with hold time 100 s at different temperatures, including 25, 75 and 100

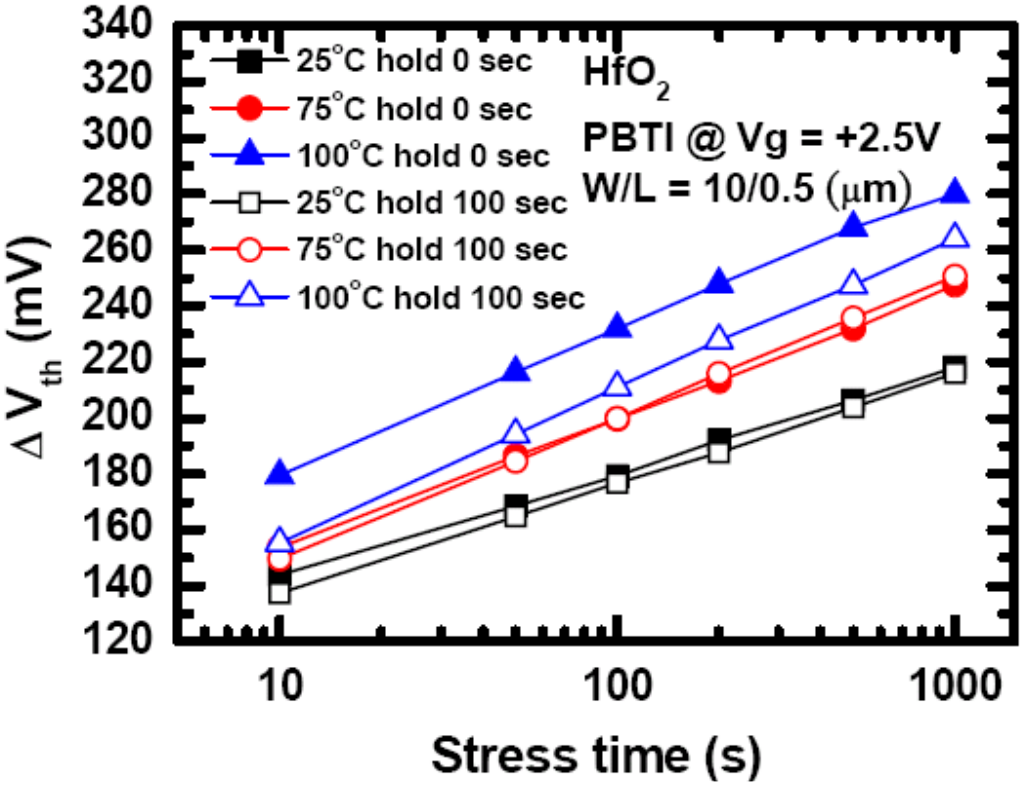


Fig. 2-10(a) Comparison of different hold time (0 & 100 s) under PBTI stress (Vg = +2.5V) at different temperatures, including 25, 75 and 100 ^{o}C for HfO_2 gate

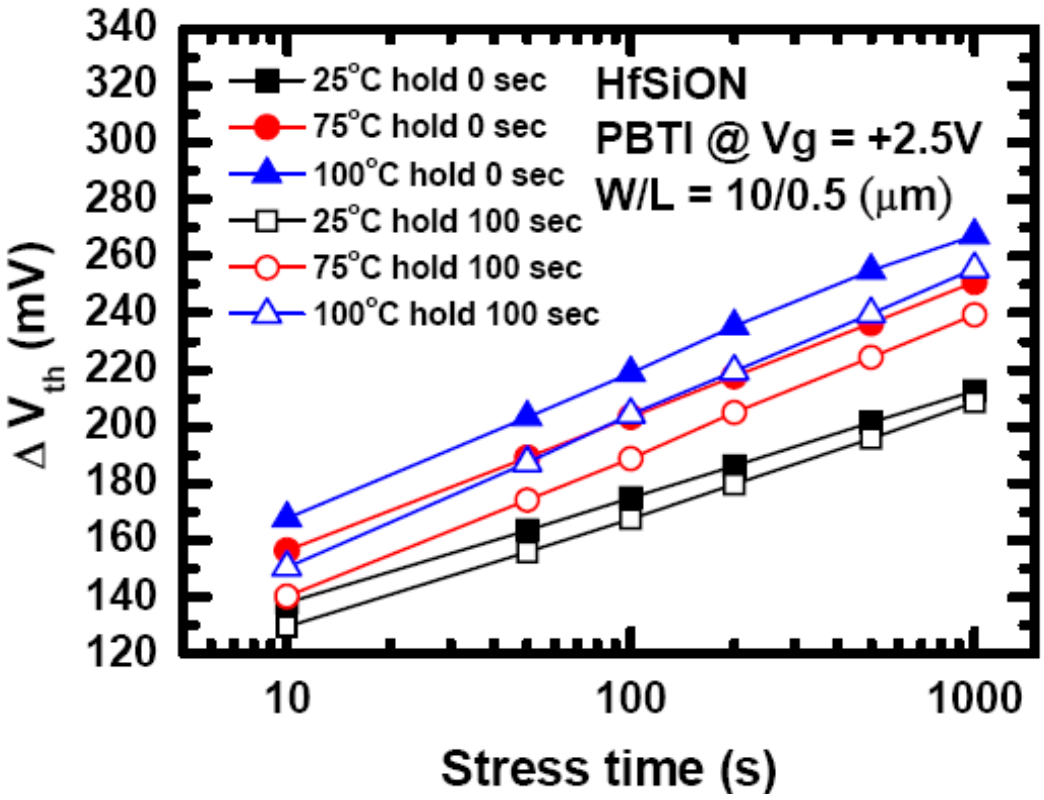


Fig. 2-10(b) Comparison of different hold time (0 & 100 s) under PBTI stress (Vg = +2.5V) at different temperatures, including 25, 75 and 100 ^{o}C for HfSiON gate dielectrics.

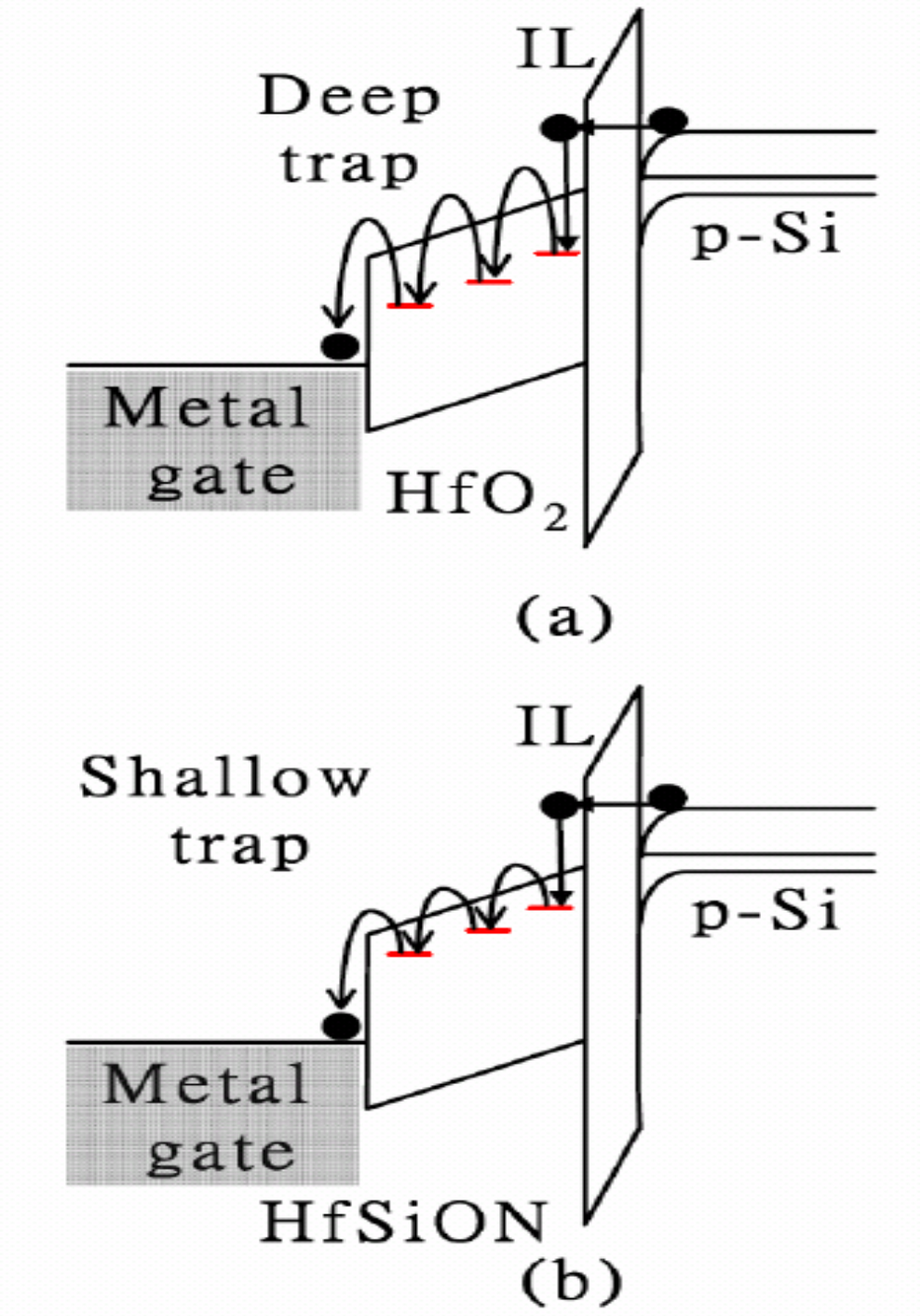


Fig. 2-11 Illustration of the charge trapping/de-trapping models for (a) HfO_2 and (b) HfSiON gate dielectrics under PBTI stress respectively.

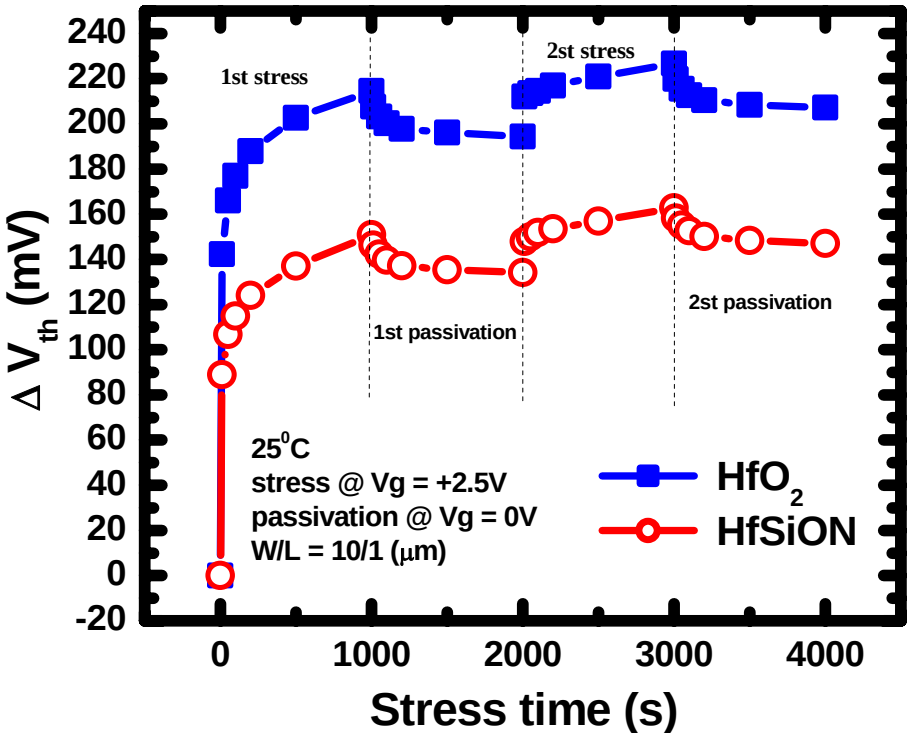


Fig. 2-12(a) ΔV_{th} of DPBTI stress versus stress/passivation at different temperature 25 °C

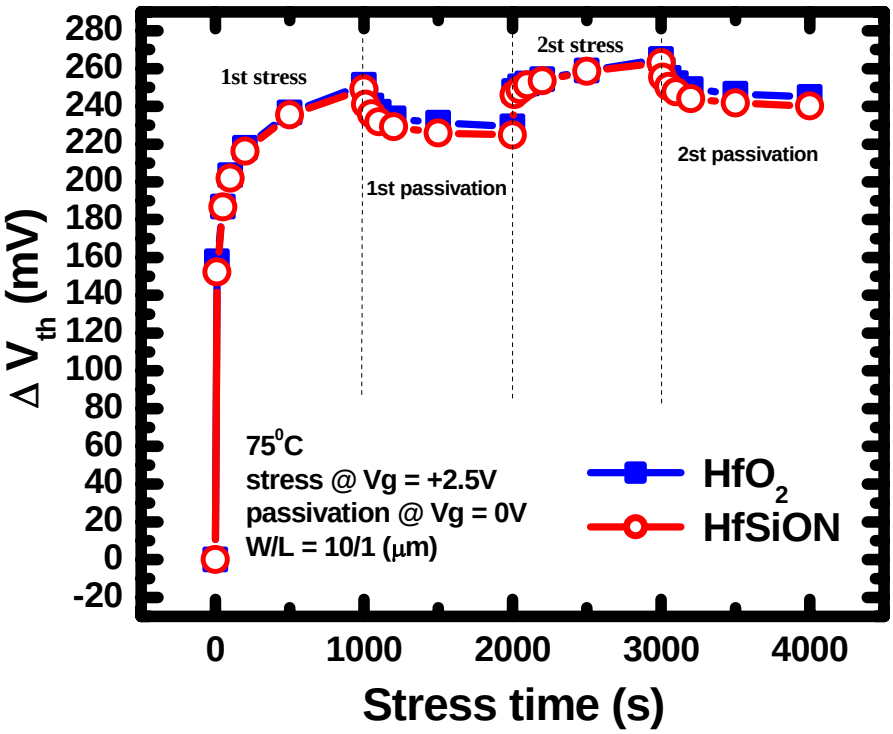


Fig. 2-12(b) ΔV_{th} of DPBTI stress versus stress/passivation at different temperature 75 ^{o}C

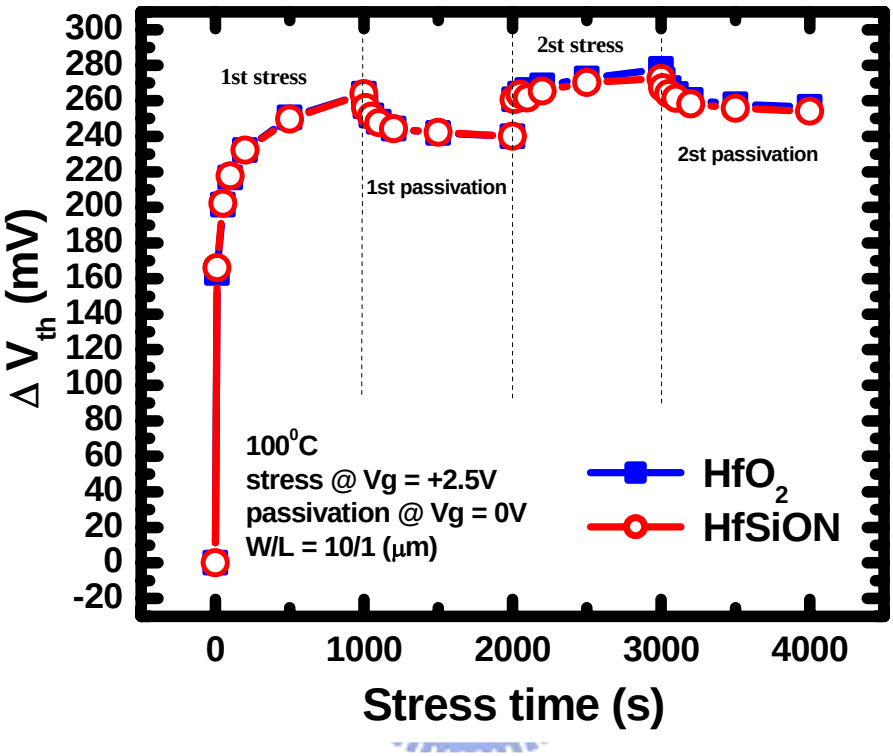


Fig. 2-12(c) ΔV_{th} of DPBTI stress versus stress/passivation at different temperature 100 ^{o}C

		1st stress		1st passivation		2nd stress		2nd passivation	
		HfSiON	HfO_2	HfSiON	HfO_2	HfSiON	HfO_2	HfSiON	HfO_2
25°C	K	68.429	116.75	152.95	214.69	139.69	203.27	164.79	226.59
	n	0.113	0.089	-0.0194	-0.0146	0.0197	0.0138	-0.0167	-0.0116
75°C	k	121.63	125.94	250.11	253.7	236.32	238.26	263.96	276.88
	n	0.1065	0.1016	-0.016	-0.0148	0.0144	0.0137	-0.014	-0.0132
100°C	k	134.98	131.85	265.17	266.38	253.18	251.33	275.16	280.46
	n	0.0998	0.1039	-0.0147	-0.0154	0.0098	0.0134	-0.0116	-0.0132

Table Ⅰ

Extracted Coefficients n and k after stress/passivation: $\Delta V_{th} = K*t^n$

Chapter 3

Trapping Characteristics of Electrons and Holes under Dynamic NBTI Stress between HfO_2 and HfSiON Gate Dielectrics

3-1 Introduction

As CMOS devices are scaling down aggressively, high-*k* gate dielectrics have become very important[21.25]. However, there are still a number of fundamental issues[26-29], such as fixed charge, reduced channel mobility, trapped charge, and reliability characteristics, which have to be understood and solved for successful high-*k* integration into the silicon CMOS technology. Reliability of high-k gate dielectric is an important issue in integral circuit performance. The quality of high-k gate dielectric, including high-k bulk pre-exist charge trap, stress-induced charge trap and high-k/SiO_2/Si interface are greatly influence the performance and lifetime of the devices.

Negative bias temperature instability (NBTI) represents one of the major concerns for the reliability of MOSFETs. In references[30-31], the NBTI was considered due to the interface states between dielectric and silicon bulk(e.g., Reaction and Diffusion model). In this study, we would discuss the characteristics in dynamic negative bias temperature instability (DNBTI) stress between HfO_2 and HfSiON gate dielectrics at

different temperature and passivated voltage. The relationships between threshold voltage and charge trapping /de-trapping and the behavior of charge pumping current under stress and passivated phase are investigated[32-33].

3-2 Device Fabrication

PMOS devices were fabricated by state-of-the-art 300 mm wafer foundry technology. STI was performed for devices isolation followed by super-steep retrograde well formation. The high-K dielectric including HfO_2 and Hf-silicate were deposited by ALD. Chemical oxide was used as the interfacial layer unless it is specifically mentioned. The nitridation of HfSiO with Hf/(Hf+Si) ratio of 50% was carried by NH_3 annealing in the ambient. After shallow source/drain extensions and pocket implantation, TEOS liner and low-temperature silicon nitride were processed in sequence to form a sidewall spacer. Modified S/D implants were adopted to improve activation and junction capacitance while maintaining good SCE. The fabrication of a heavily doped source/drain junction by implantation was followed by a RTA of 1000 ^{o}C for 5 s for S/D activation and thermal stability of HfSiON. Device parameters, including drive current and threshold voltage, were measured using a Keithley 4200 papameter analyzer before and after reliability stressing.

3-3 Results and Discussion

In this study, DNBTI on HfO_2 and HfSiON PMOSFETs has been investigated. The DNBTI model of hole trapping under NBTI stress and the electrons trapping under passivated stress have been proposed. In addition, the characteristics of the ΔV_{TH} and charge pumping current under DNBTI stress indicate that the interface states are not recovered during the passivated period.

3-3-1 Temperature instability

Figure 3-1 show the temperature dependence of (a)HfO_2 and (b)HfSiON dielectrics. The change of threshold voltage is due to hole trapping/de-trapping and interface state generation/passivation. Although the high temperature enhance the hole trapping and interface state generation, but it also have better behavior under passivation state.

3-3-2 The characteristics of carriers trapping/de-trapping

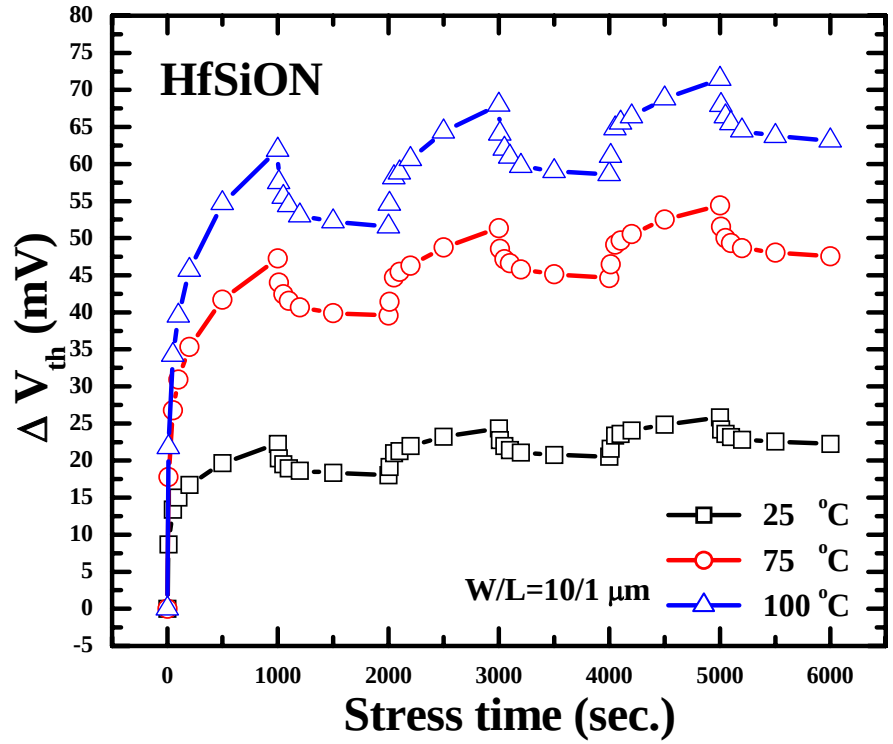
Figures 3-2 show the comparisons of the threshold voltage shift (ΔV_{th}) for (a) HfSiON and (b) HfO_2 under DNBTI stress with respect to stress time. Each cycle time is 1000 seconds and the stress temperature is kept at 100 ^{o}C. The gate voltage V_G is -2.5 V under NBTI stress, and V_G is 0, 1, 1.5V under passivated stress, respectively. Furthermore, the terminals (source, drain, and substrate) are grounded under both conditions during the DNBTI stress. It is worth noting that the ΔV_{th} is almost recovered at V_G=1.5V. Figures 3-3 show the comparisons of the ΔV_{th} on log scale for

(a) HfSiON and (b) HfO_2 under first passivated stress. From the extraction of power law, one finds that there is only one power-law exponent value for the splits of V_G=0 and 1V, but there are two distinct power-law exponent values for the split of V_G=1.5V. For the split of HfSiON, the n of power-law exponent value is from -0.173 to -0.456, and that of HfO_2 is from -0.280 to -1.746. The decreasing magnitude of HfO_2 is larger than that of HfSiON, and we suppose that the defects in HfO_2 one more than that in HfSiON for electron trapping. Figures 3-4 show the comparison of that under second passivated period. For the split of HfSiON, Fig. 3-4(a), the n value of power-law exponent value is from -0.146 to -0.318, and that of HfO_2 Fig. 3-4(b) is from -0.205 to -0.829. The decreasing magnitude of second passivated period is less than that of first passivated period, and the n value of third passivated period Fig. 3-5 is the smallest in these passivated states. In order to compare the difference recovered behaviors between different passivated and stress state, we extracted the coefficient n and summarized in Table I and Table II. In the first passivated cycle, one can observe two different passivated behaviors for the split of V_G=1.5V. In first stage, we speculate that the hole de-trapping from high-k dielectric to the substrate with small amount electrons trapping into high-k dielectric, which results in smaller n value. Then, the coefficient n decreases in second stage, because of a great amount of electrons trapped into dielectric. Furthermore, in the second passivated cycle, the absolute n values are

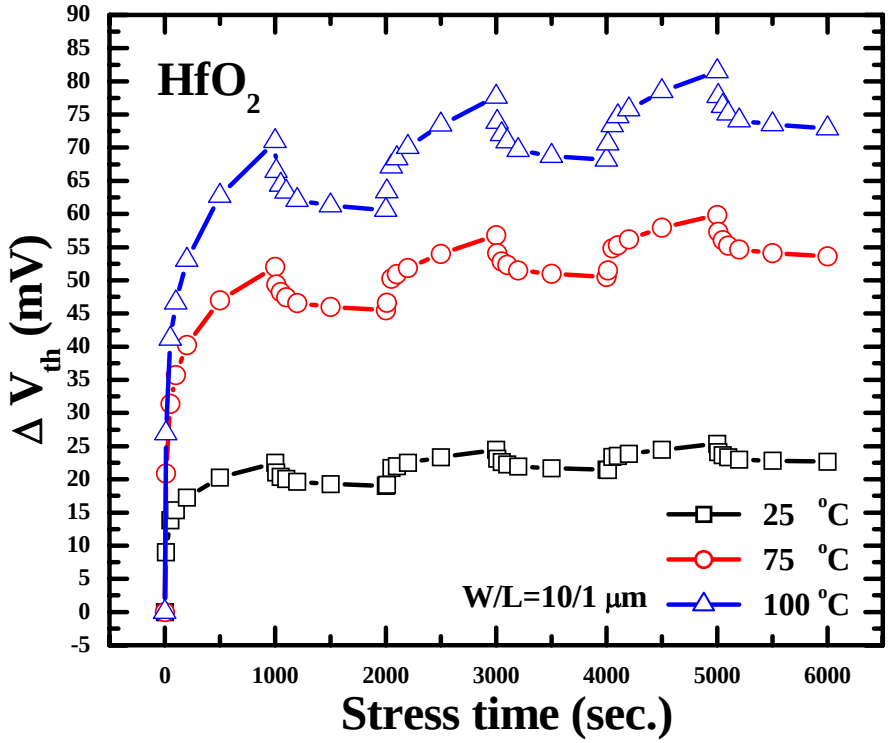
smaller than that in the first passivated cycle. Figures 3-6 depict the charge pumping current under the first NBTI stress cycle for (a) HfSiON and (b) HfO_2 dielectrics, respectively. The charge pumping current increases during the first NBTI stress cycle. However, during the first passivated stress cycle, the charge pumping current decreases slightly, as shown in Figs. 3-7. As compared with Figs. 3-2, the ΔV_{th} would be almost recovered, especially for the split of V_G=1.5V, but the charge pumping current isn't recovered any more. Therefore, the recovery behavior isn't due to the passivation of interface states, but due to the electrons trapping. Figures 3-8 depict the charge pumping current under the second NBTI stress cycle for (a) HfSiON and (b) HfO_2 dielectrics, respectively. It is interesting that the charge pumping current doesn't change, which is different from that during the first NBTI stress cycle. This means that the interface states increasing is close to saturation after the first NBTI cycle. In the second and third passivated/stress cycles of Figs. 3-8 to Figs. 3-11, the charge pumping current also decreases slightly. It turns out that, the recovery of ΔV_{TH} is not dominant by the passivated behavior of interface states. Figures. 3-12 show the schematic of gate stack band diagram under (a) stress and (b) passivated cycle. Under NBTI stress state, holes in the inversion are injected into the gate dielectric layer. Under passivated states, the electrons are injected into the gate dielectric layer, and the holes are slightly escaping from the gate dielectric at the same moment.

3-4 Summary

The threshold voltage shift was almost recovered at V_G=1.5V, and there are two distinct power-law exponent values for the split of V_G=1.5V. In addition, the charge pumping current increases only in the first NBTI cycle, and it almost has not any variation in other cycles due to the saturation of interface states generation. Therefore, we conclude that the interface states are generated at the first NBTI stress state, and they are not recovered anymore at passivation cycles. Under passivated stated, the recovery of ΔV_{TH} is only due to the electrons/holes trapping/de-trapping.

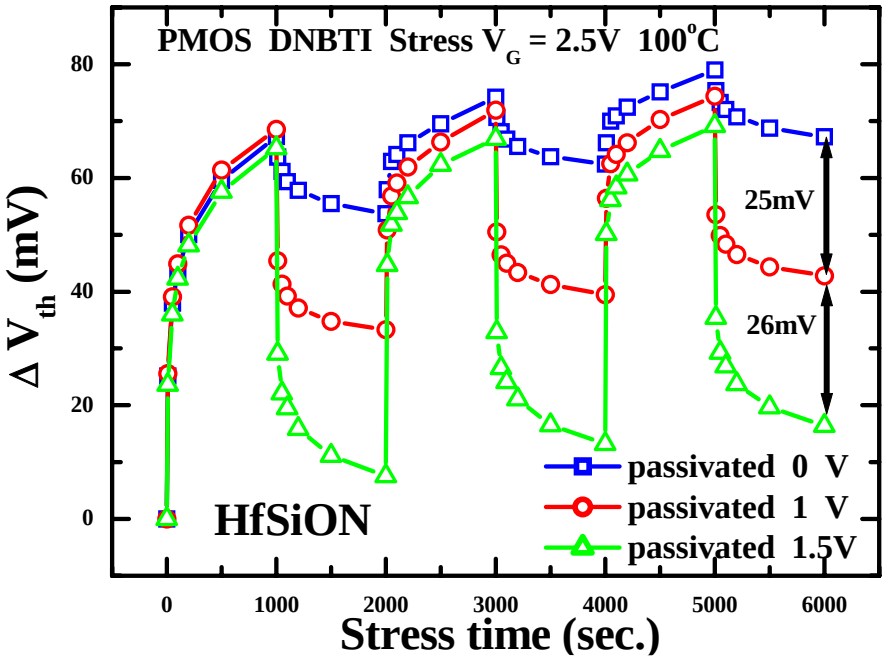


(a)

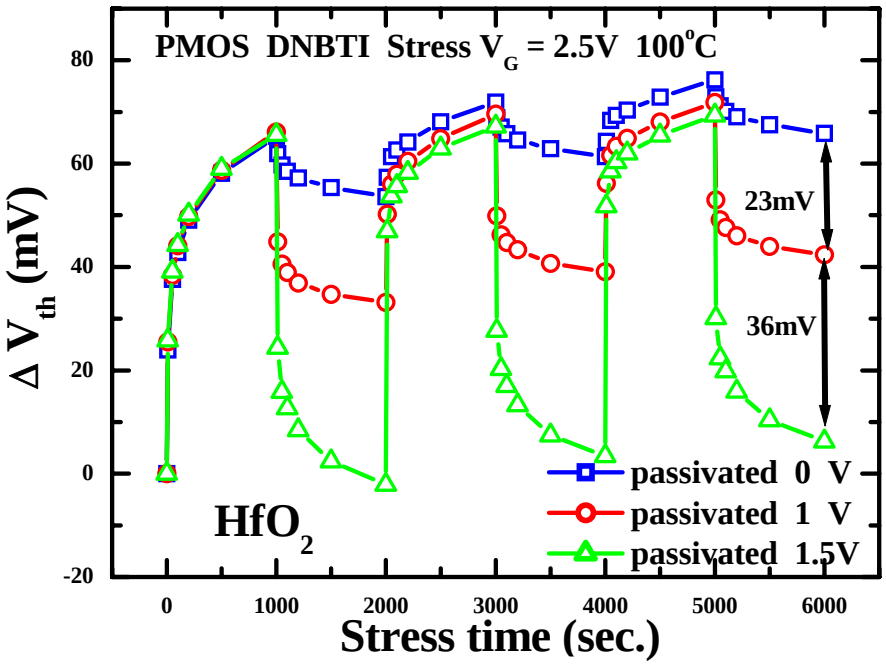


(b)

Figure 3-1 show the temperature dependence of (a)HfO_2 and (b)HfSiON dielectrics.

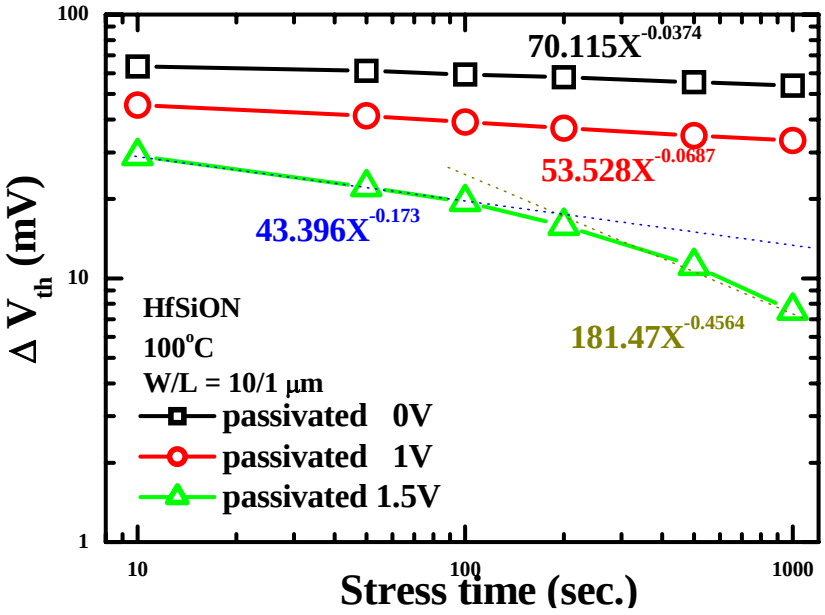


(a)

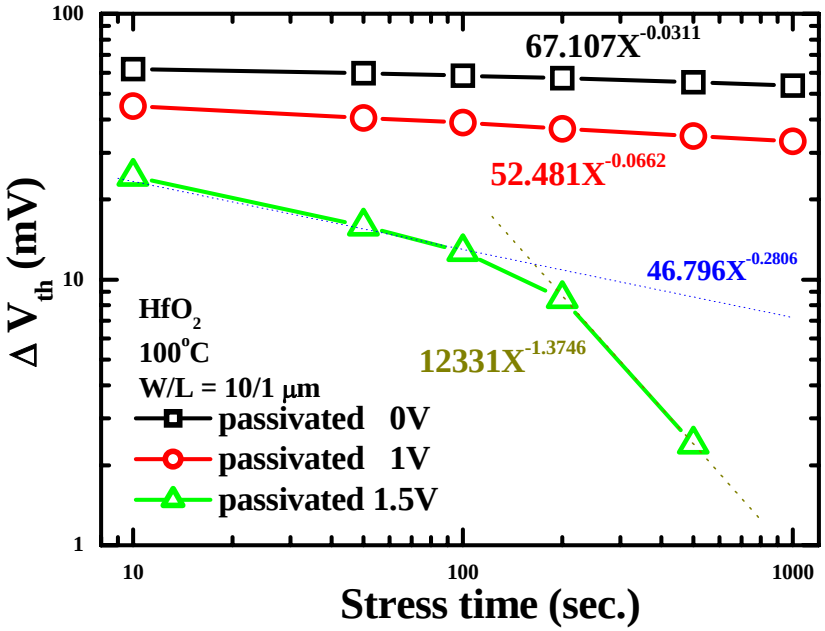


(b)

Figure 3-2 Threshold voltage shift during DNBTI stress (-2.5V)/passivated(0V, 1V, 1.5V) 1000s cycles at T=100°C on (a) HfSiON (b) HfO_2 devices.

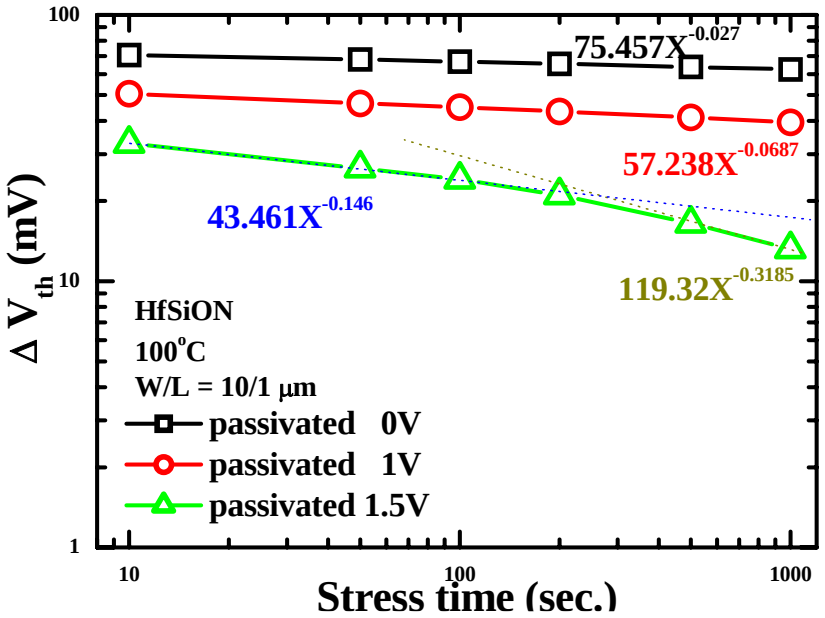


(a)



(b)

Figure 3-3 Comparison of threshold voltage shift for (a) HfSiON and (b) HfO_2 under first passivated period, and V_G=0, 1, 1.5V, respectively.



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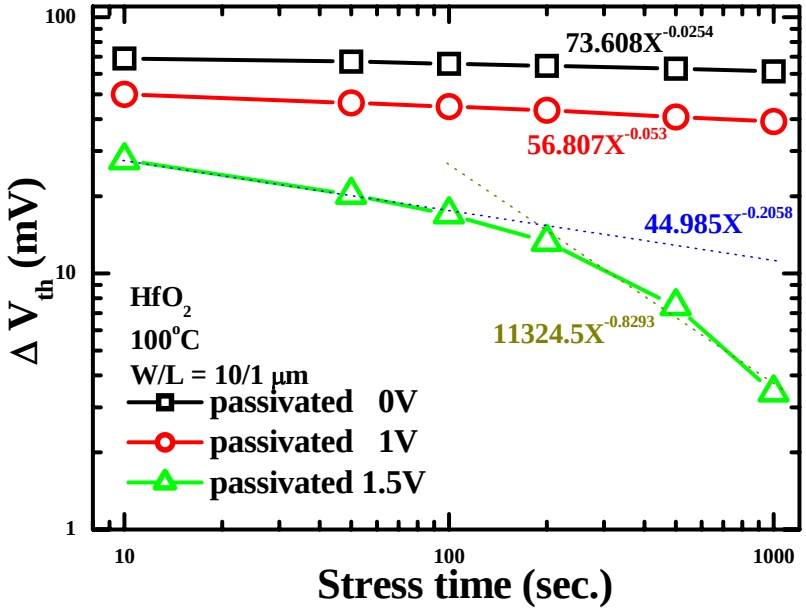
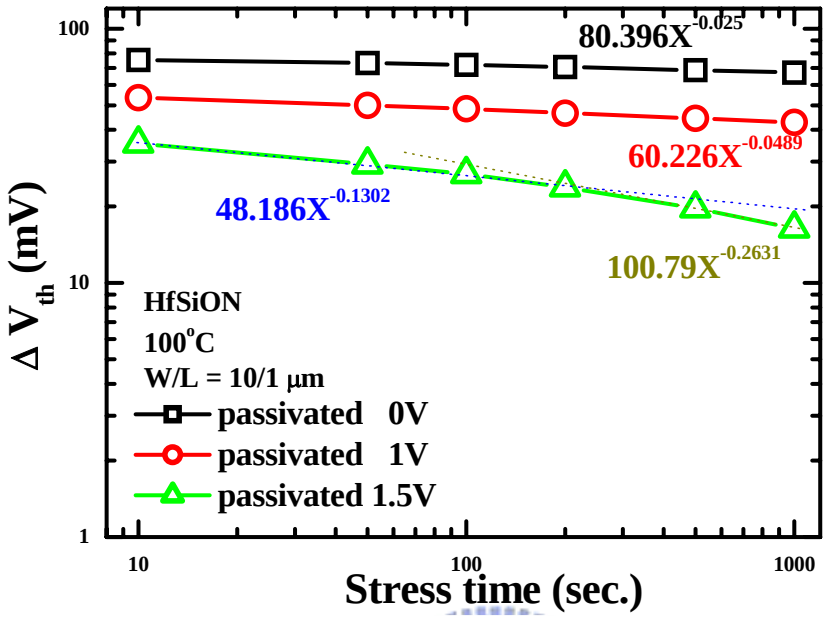
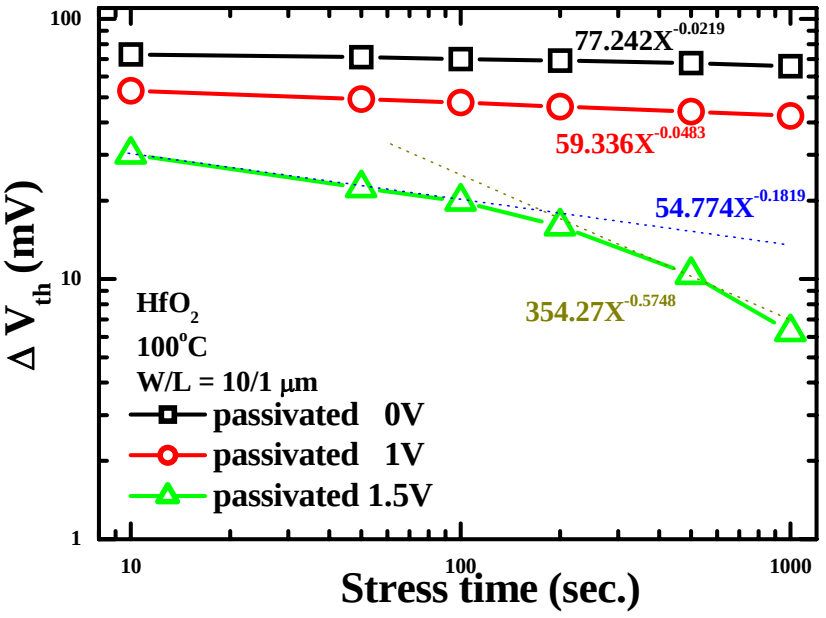


(b)

Figure 3-4 Comparison of threshold voltage shift for (a) HfSiON and (b) HfO_2 under second passivated period, and V_G=0, 1, 1.5V, respectively.

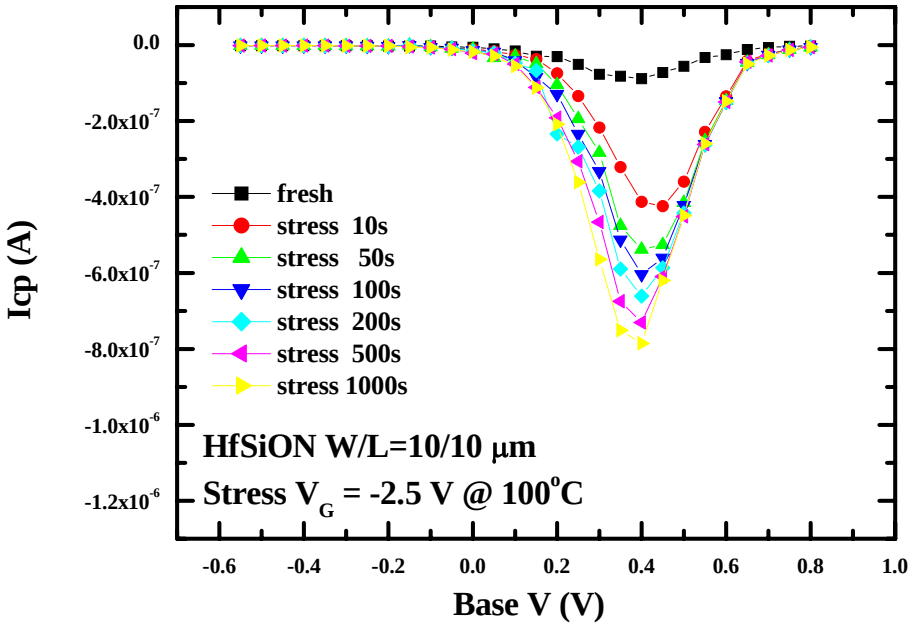


(a)



(b)

Figure 3-5 Comparison of threshold voltage shift for (a) HfSiON and (b) HfO_2 under the third passivated period, and V_G=0, 1, 1.5V, respectively.



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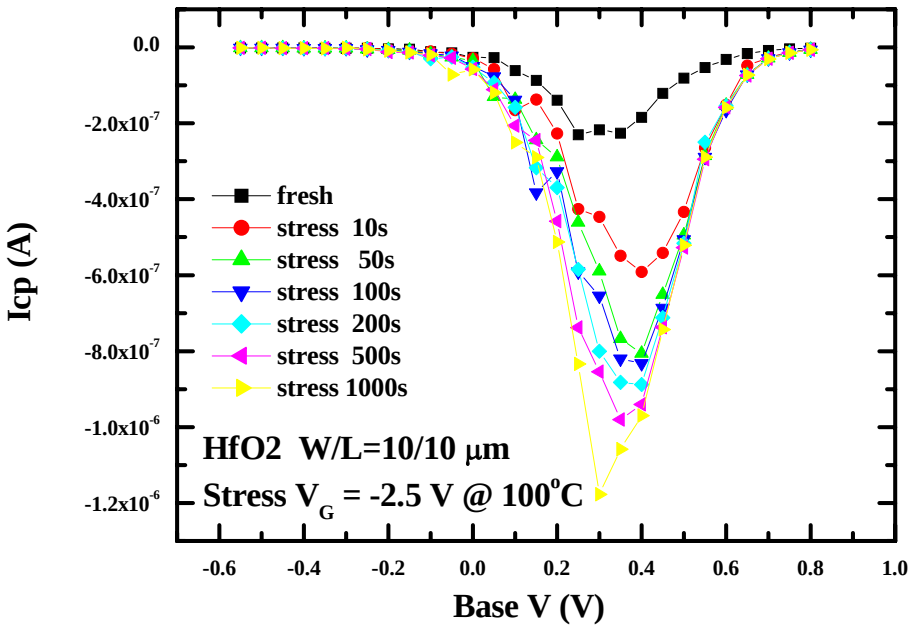
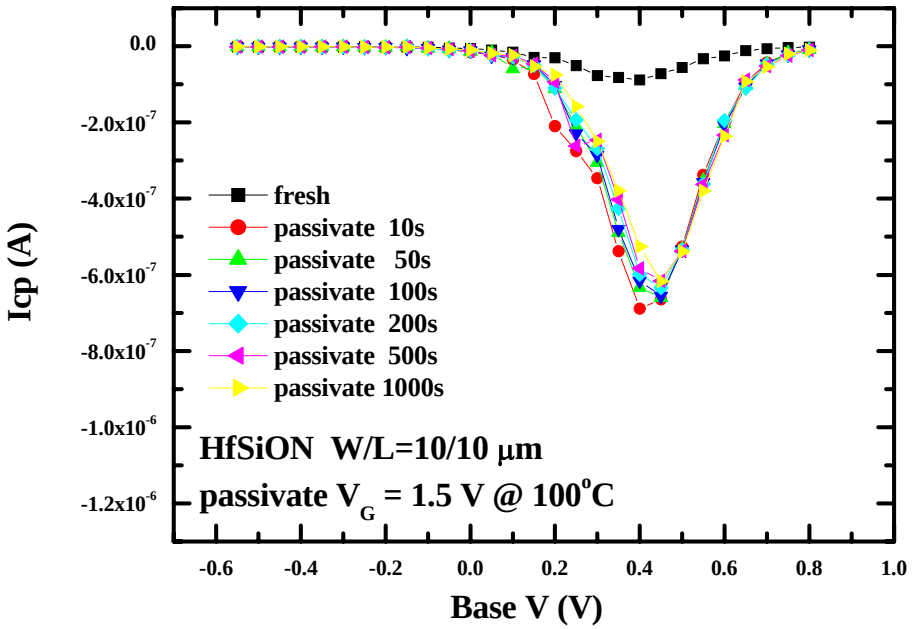


(b)

Figure 3-6 Charge pumping current under the first NBTI cycle for (a) HfSiON and (b) HfO_2 dielectrics, respectively



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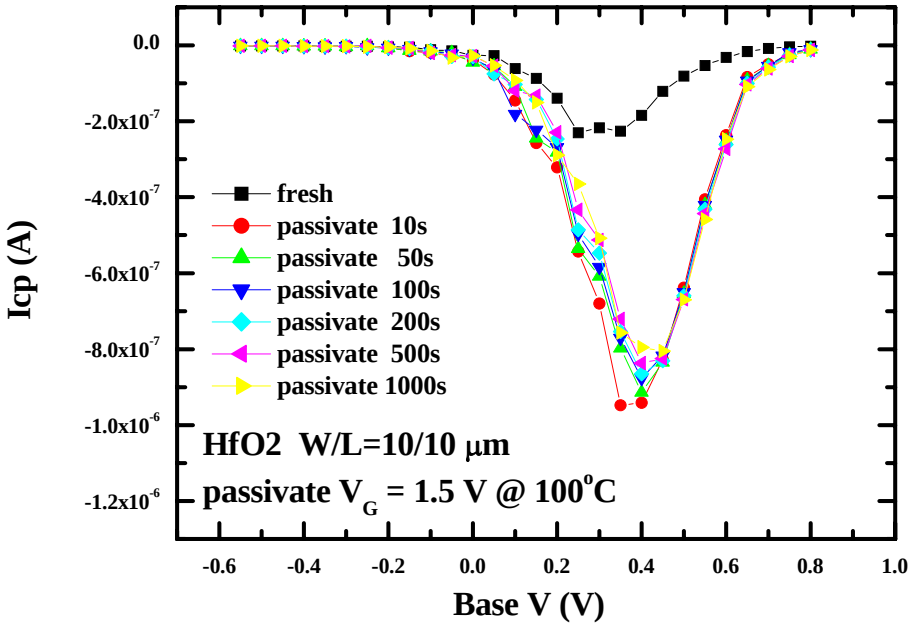
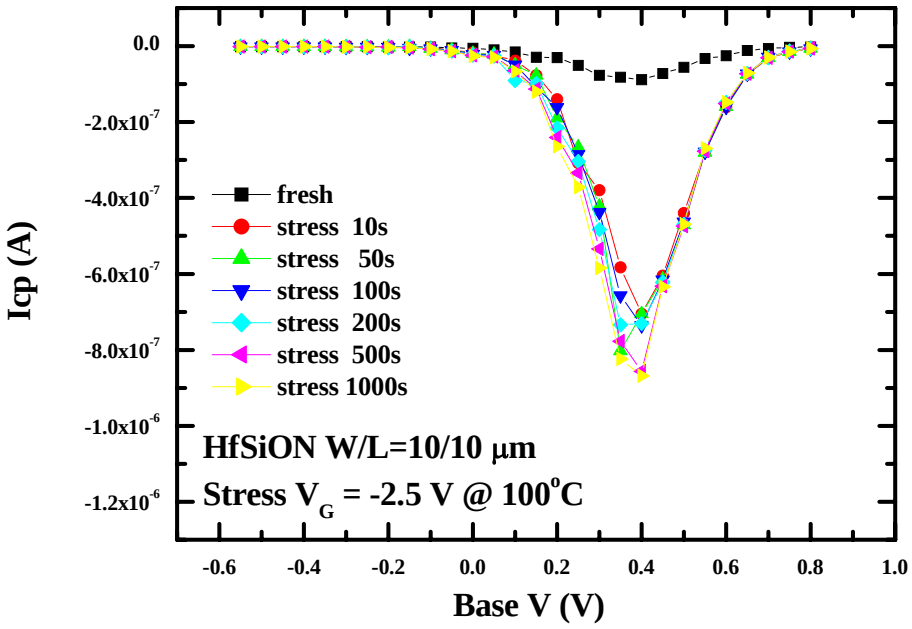
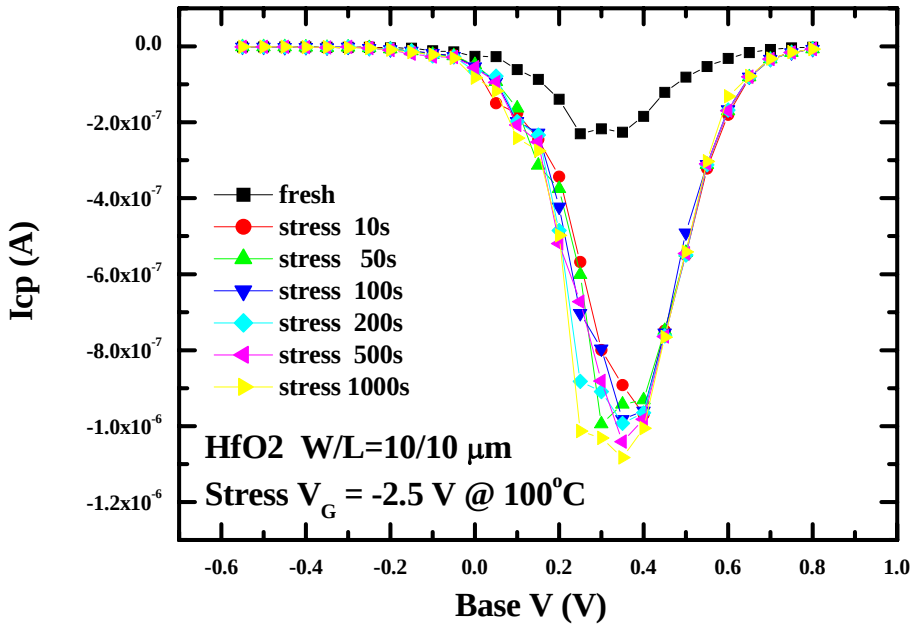


(b)

Figure 3-7 Charge pumping current under the first passivated state at 1.5V for (a) HfSiON and (b) HfO_2 dielectrics, and the appearances of recovery are not obviously.

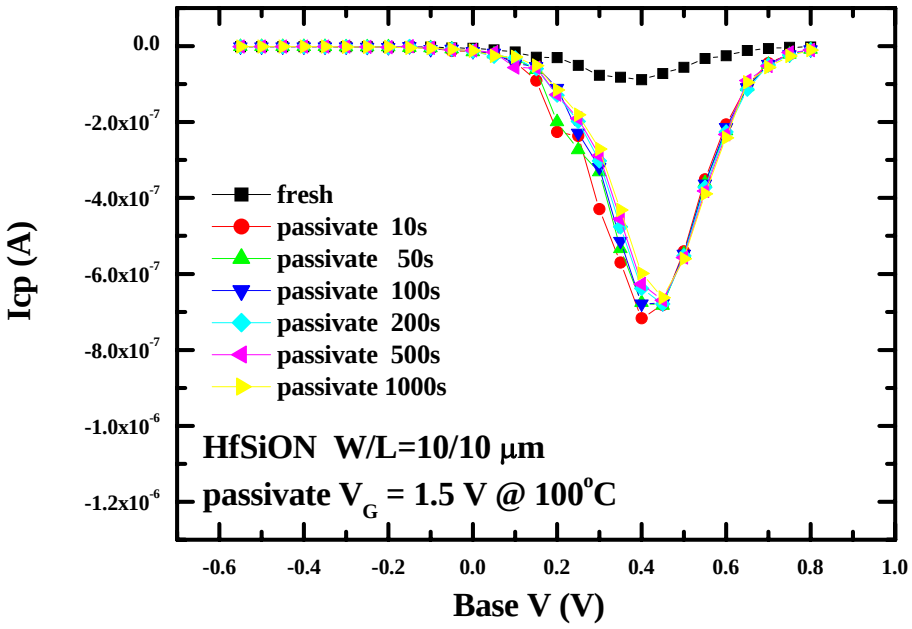


(a)

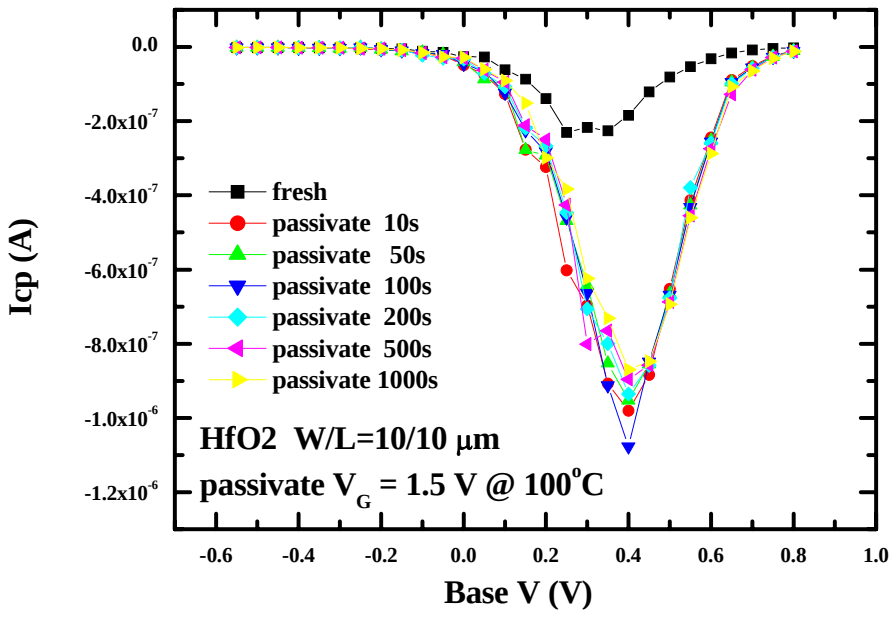


(b)

Figure 3-8 Charge pumping current under the second stressed state at -2.5V for (a) HfSiON and (b) HfO_2 dielectrics, and the increase of charge pumping current are also not obviously.

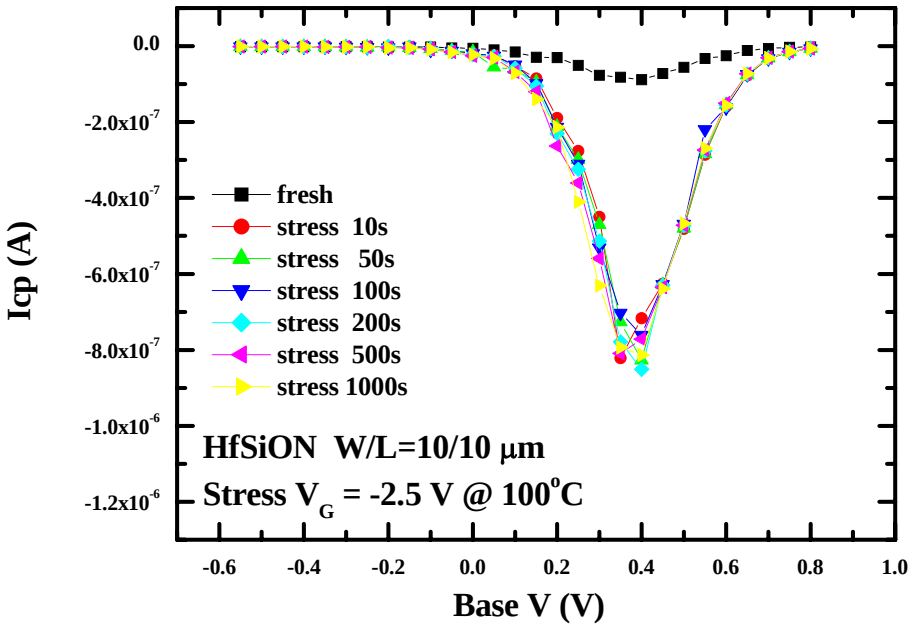


(a)



(b)

Figure 3-9 Charge pumping current under the second passivated state at 1.5V for a) HfSiON and b) HfO_2 dielectrics, and the recovered phenomenon almost can be ignored.



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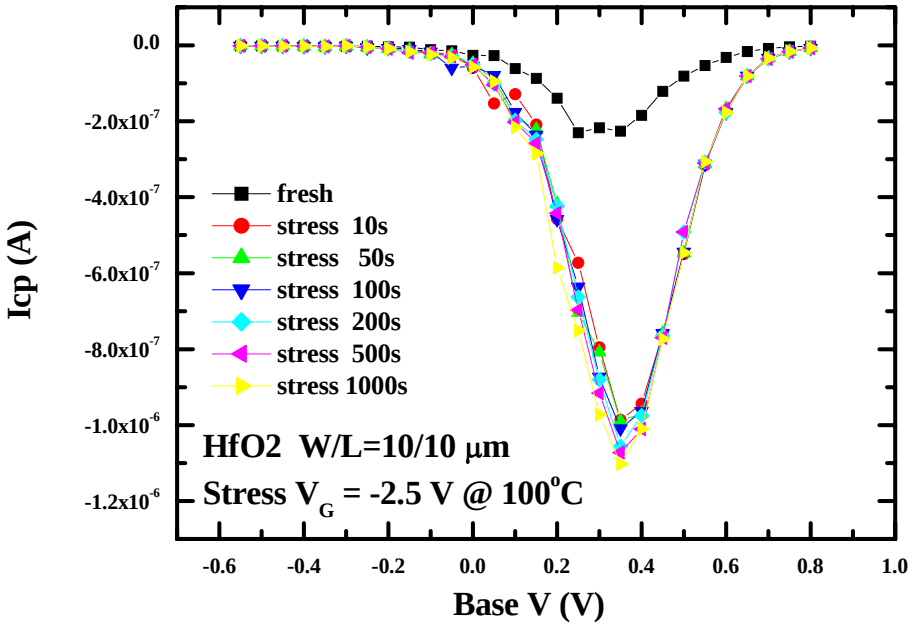
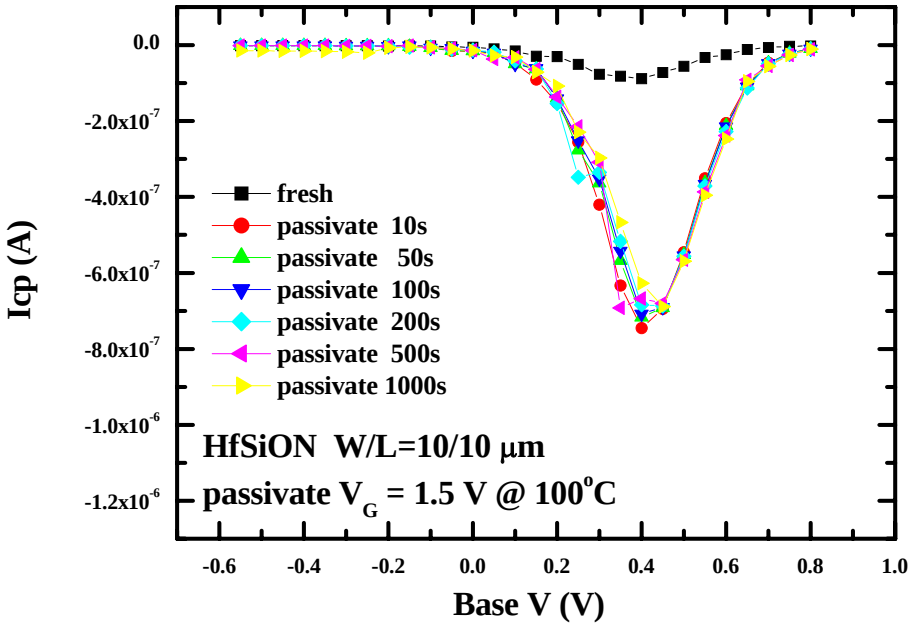
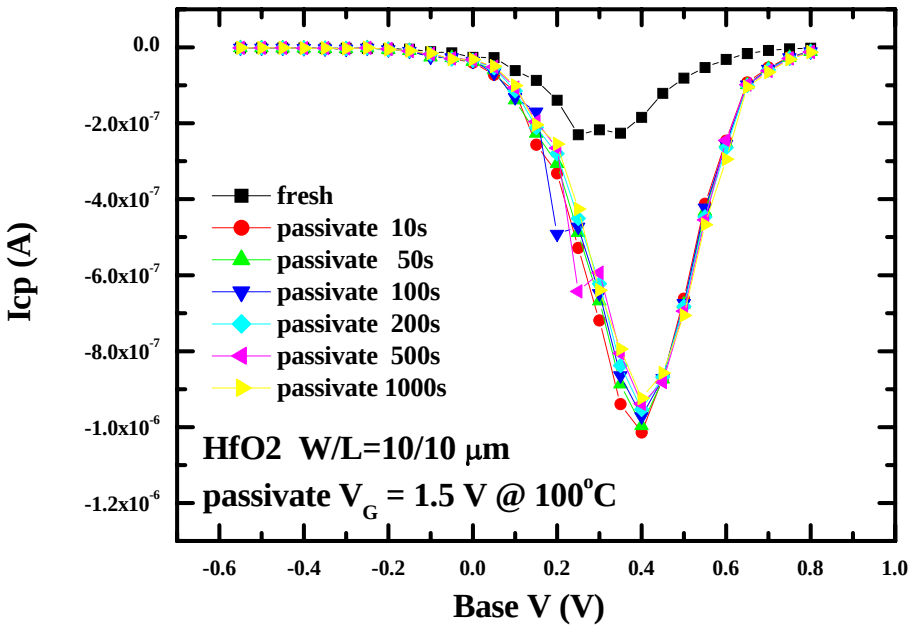


(b)

Figure 3-10 Charge pumping current under the third stressed state at -2.5V for (a) HfSiON and (b) HfO_2 dielectrics, and the increase of charge pumping current are also not obviously.

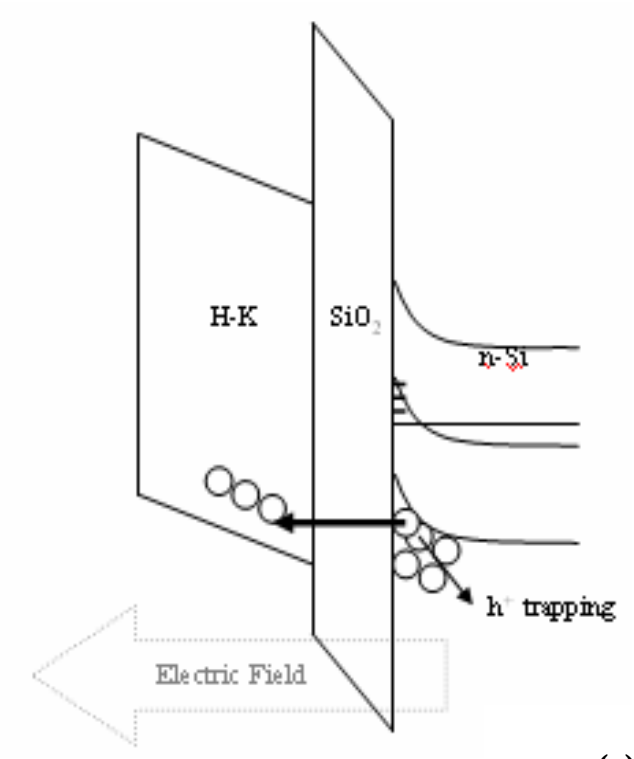


(a)



(b)

Figure 3-11 Charge pumping current under the third passivated state at 1.5V for a) HfSiON and b) HfO_2 dielectrics, and the recovered phenomenon almost can be ignored.



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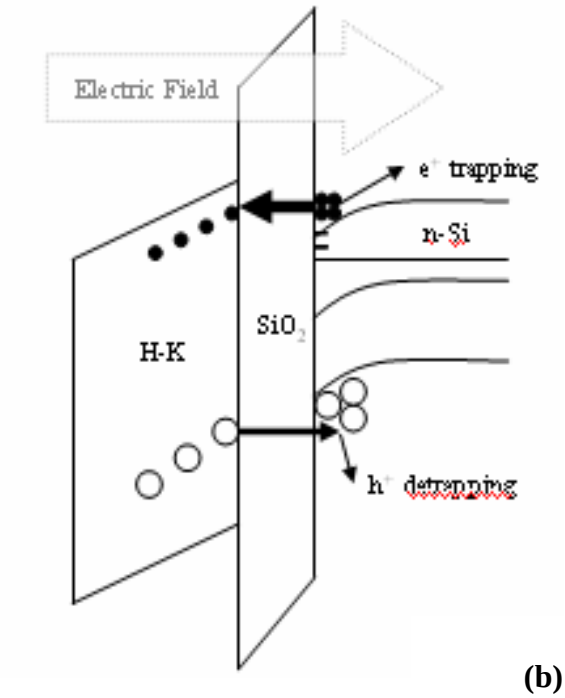

(b)

Figure 3-12 Schematic of gate stack band diagram under (a) stress and (b) passivated

Table Ⅰ Extracted Coefficient n during NBTI stress and $\Delta V_{th} = K*t^n$. The NBTI stress voltage V_G=-2.5V and the temperature T=100 ^oC.

		1st stress		2nd stress		3rd stress	
		HfSiON	HfO_2	HfSiON	HfO_2	HfSiON	HfO_2
Passivated 0V	n	0.2117	0.2145	0.0509	0.0473	0.0362	0.0344
Passivated 1V	n	0.2129	0.2039	0.0728	0.0685	0.0576	0.0509
Passivated 1.5V	n	0.2188	0.1998	0.0855	0.0759	0.0678	0.0603

Table Ⅱ Extracted Coefficient n during passivated oeriod, and $\Delta V_{th} = K*t^n$. The NBTI stress voltage V_G=-2.5V and the temperature T=100 ^oC.

		1st passivation				2nd passivation				3rd passivation			
		HfSiON		HfO_2		HfSiON		HfO_2		HfSiON		HfO_2	
Passivated 0V	n	-0.0374		-0.0311		-0.027		-0.0254		-0.025		-0.0219	
Passivated 1V	n	-0.0687		-0.0662		-0.0687		-0.053		-0.0489		-0.0483	
Passivated 1.5V	n	-0.173	-0.4564	-0,2806	-1.3746	-0.146	-0.3185	-0.2058	-0.8293	-0.1302	-0.2631	-0.1819	-0.5748

Chapter 4

Conclusion

In this studying, the PBTI and NBTI degradation for HfO_2 and HfSiON NMOSFETs with the metal gate electrode has been successfully demonstrated.

The pre-exist/generated oxide trap during PBTI stress will dominate the PBTI characteristics for Hf-based gate dielectrics. In addition, the better behaviors of threshold voltage degradation and oxide trap generation under PBTI stress indicates that the HfSiON thin film quality is better than HfO_2 attributed to HfSiON gate dielectrics had the extra Si-O and Si-N bodings resulting in annihilation of oxygen vacancies. On the other hand, the electron trapping/de-trapping effect has been investigated in both HfO_2 and HfSiON NMOSFETs with constant voltage stress. As compared with HfO_2 dielectrics, the HfSiON has shallower charge trapping level under PBTI stress due to elimination of deep dielectric vacancies.

During the NBTI stress, the threshold voltage shift was almost recovered at V_G=1.5V, and there are two distinct power-law exponent values for the split of V_G=1.5V. In addition, the charge pumping current increases only in the first NBTI cycle, and it almost has not any variation in other cycles due to the saturation of interface states generation. Therefore, we conclude that the interface states are generated at the first NBTI stress state, and they are not recovered at any situation.

Under passivated stated, the recovery of ΔV_{th} is only due to the electrons/holes trapping/de-trapping.

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Publication List

International Conference Paper：

[C-1] ***Wei-Liang Lin***, Yao-Jen Lee, Wen-Cheng Lo, King-Sheng Chen, Y. T. Hou[4], K. C. Lin[4], and Tien-Sheng Chao"Trapping and De-trapping Characteristics in PBTI and Dynamic PBTI between HfO_2 and HfSiON Gate Dielectrics" 2008 INTERNATIONAL SYMPOSIUM ON THE PHYSICAL AND FAILURE ANALYSIS OF INTEGRATED CIRCUITS

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