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電機學院光電工程學系
光電工程研究所

碩 士 論 文

低溫複晶矽薄膜電晶體製作於可

撓式基板之研究

Investigation of Low Temperature

Polycrystalline Silicon TFT Fabricated on Steel

Foil

研 究 生：陳思維

指導教授：劉柏村　博士

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摘要

可撓式薄膜電晶體研究是現今最受矚目之一的一項技術,擁有輕薄、可撓曲、容易隨身攜帶等特性。目前大多數可撓式元件都由多晶矽薄膜電晶體為主基礎應用;然而複晶矽薄膜電晶體技術相對於多晶矽薄膜電晶體有更佳的傳輸電流和更快的開關速度。對於可撓式顯示器的應用上,顯示器面板被要求能承受某種程度的撓曲。因此希望在不同撓曲情況下,能夠研究平行通道方向的撓曲對於不同通道長度之複晶矽薄膜電晶體電性在不銹鋼基板上所產生的效應。

首先研究複晶矽薄膜電晶體在不銹鋼基板上撓曲多次前後電性是否有劣化或穩定趨勢。接下來研究不同撓曲程度對元件電性上的影響,並且配合變溫量測和不同通道長度量測萃取源/汲極寄生電阻和缺陷密度來分析去除寄生電阻後載子遷移率的特性變化並且探討原因。最後研究在不同撓曲情況下,P型複晶矽薄膜電晶體在直流電壓操作下可靠度問題。實驗結果發現在撓曲的情況下,不論是張應力或壓應力起始電壓偏移均較平面情況下為嚴重,然而壓應力下經由長時間直流電壓操作後,載子遷移率較張應力下長時間直流電壓操作為佳,也顯示壓應力下對於元件的可靠度較張應力下更優。

Investigation of Low Temperature Polycrystalline Silicon TFT Fabricated on Steel Foil

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Department of Photonics and Display Institute

Abstract

In recent years, flexible display technology has been investigated significantly. They have characteristic of light、thin、bendy and portable! Much of recent flexible research on thin-film electronics has been focused on amorphous silicon TFT. But poly silicon thin film transistor technology provides a better alternative since it offers higher current and faster switching speed. And TFT based on metal foil has the advantage of cheap and softly. For application
 of flexible display, display panels are required to sustain a certain degree of bending. Bending would induce strain in the electronic circuits and may affect TFT device characteristics. So we investigate the effects of different radius of bending parallel the channel length on p-type poly silicon TFT on metal foil base.

First, we investigate the trends after hundreds of bending parallel the channel length on p-type poly silicon TFT on metal foil base to make sure

the electronic characteristics stable or not. Then extraction the parasitic

resistance 、 flat band voltage and trap density 、 threshold voltage、

subthreshold slope and mobility. That's help discuss the reasons of

mobility and current changing under bending condition. Another

consideration we also study the reliability of p-type polycrystalline

silicon thin film transistors on metal foil fabricated by the ELC method

under bending condition. We utilize DC stress to simulate the operation

of P-type poly-Si TFTs and observe the degradation degree under

bending condition. The result indicates that threshold voltage shift more

worse in bending situation no matter under compressive or tensile

condition than in plan situation. It also indicates that mobility under

compressive bending drain bias DC stress better than tensile bending

drain bias DC stress.
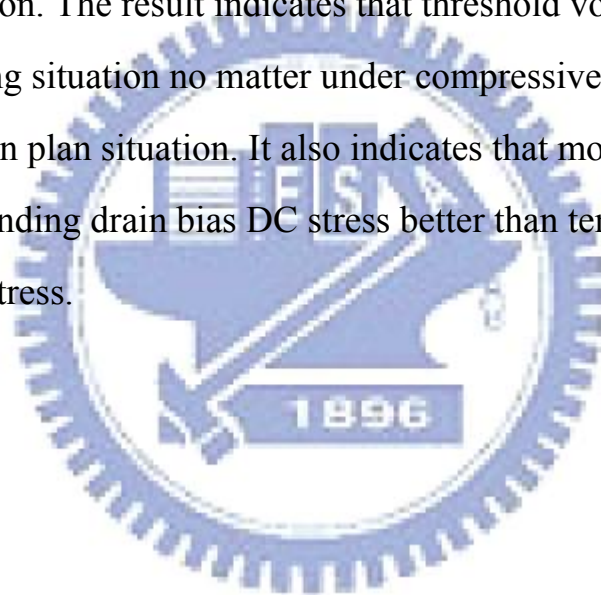
致謝

在這兩年的碩士研究生涯中，有許多人令我心存感激。首先誠摯的感謝指導教授劉柏村博士，劉老師細心且認真的指導使在下在學術研究、知識累積、人格養成上不斷的教誨和提攜，使我收穫良多並且順利的完成碩士學位。在此至上內心最誠摯的敬意和謝意。諸位口試委員的指導和建議，在下也在此謹申謝意。

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謹以此文獻給我摯愛的家人以及朋友們。

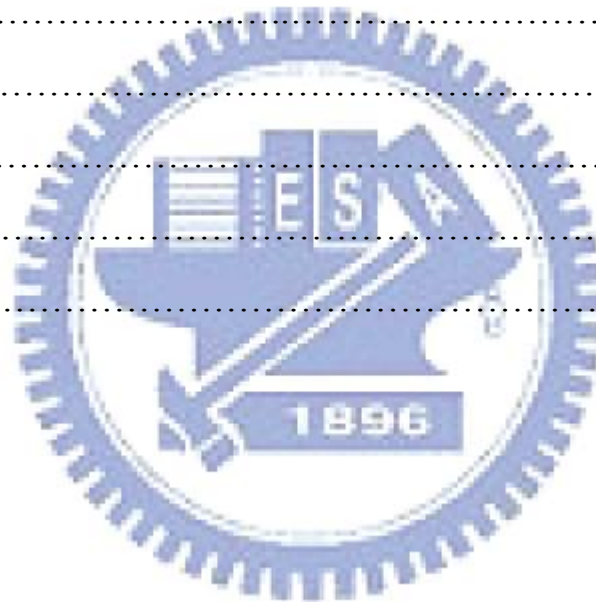
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Chapter 1   Introduction

1.1 General Background

Recently, electronic paper、smart labels and personal digital assistant (PDA) are fields of rapidly growing interest. Lightweight, thin and rugged flexible flat panel display is of great interest for application in portable instruments. Most of the reported flexible electronics so far are based on amorphous silicon thin-film transistor (a-Si:H TFT) technology. For these applications, the traditional glass substrate of large-area electronics must be replaced with a flexible and lightweight substrate like plastic substrate or steel foil substrate. The electrical instability is also a critical issue for a-Si:H TFTs, as it can degrade the electrical characteristics and affects the lifetime of devices.

So for large area display and flexible application, poly-Si TFTs can be used for both pixel switching and for the integrated display driver circuitry **[1.1]** since it offers higher current and faster switching speed. Additionally, poly-Si TFTs also play the role of light shutters in projection display. The higher durability against luminance and heat is needed since those devices are put adjacent to a high-power lamp. But the relatively large leakage current is one of the most important issues of poly-Si TFTs under OFF-state operation **[1.2]**, **[1.3]**. The dominant mechanism of the leakage current in poly-Si TFTs is field emission via grain boundary traps due to the high electric field near the drain junction **[1.3]**-**[1.6]**. Consequently, there are two ways to reduce leakage current:

one is to reduce grain-boundary trap density and the other is to alleviate the electric field near the drain side. To overcome this inherent disadvantage of poly-Si films, many of researches have been focused on modifying or eliminating these grain boundary traps. Hydrogenation is a method for reducing the trap density in poly-Si films [1.7]-[1.9]. As the number of trapped carriers decreases, the potential barrier associated with the grain boundary also decreases. We choose the way of Hydrogenation by SiNx preservation annealing to repair grain-boundary trap density. In this way we can measure better current-voltage curve and lower leakage currents. And for portable devices, steel foil substrate is more attractive due to its lightweight, thin, flexible, low price and rugged characteristics [1.10]-[1.16]. As compared with plastic substrates, steel foil is compatible with the traditional TFT process because of its higher melting point and is a better candidate on blocking water vapor and oxygen permeability. In order to obtain higher display quality and lower power consumption, the LTPS-TFT technology is necessary [1.14]-[1.16].

In summary, it is expected that poly-Si TFTs on metal foil will become more and more important in near future technologies. The researchers indicate the market of flexible display will achieve 9.7billion U.S dollars in 2010.The portable flexible electronics technology would bring us more convenient and comfortable life. They believe that the market of flexible display would more and more large. So there are distant prospects to make this flexible display's dreams come true.

1.2 Motivation

Now, the large area electronics or the flat-panel displays comprised of poly-Si TFTs such as a switch device of AM-LCD are used by people in the world. And flexible products are applied in many ways nowadays. But a-Si:H TFTs under flexible substrates have the problems of many trap densities and charge trapping effects and state creation effects **[1.17]-[1.18]**. So if we bending so many times or stress too long will cause serious irreversible damages in a-Si:H TFTs under flexible substrates. Conversely, polycrystalline silicon TFTs because of the crystalline ways different from a-Si:H TFTs, so they have better currents and stable characteristics.

Flexible technology and poly-Si TFTs technology are more and more interested by people at the globe. So to combine two technologies is a very original and proactive study. But how do we know the flexible instruments endurable or how much temperature they could endure? So the instability of study is emphasis important. There are extensive studies over *a*-Si:H TFTs on flexible substrate under mechanical strain **[1.19]-[1.20]**. From bending measurement、change Temperature measurement to DC,AC stress under bending condition for *a*-Si:H TFTs on flexible substrate. However, very few relevant investigations were reported for poly-Si TFT in the past. Especially for p-type poly-Si TFTs on flexible substrate study, there is no relevant investigation to be reported in the past. Therefore my experiments focus on p-type poly-Si TFTs on flexible substrate study.

In flexible substrate material, Metal foil (like steel) and plastic

(like polymer film) are most common than others because of lightweight, thin and easy to obtainment. Two substrates have their own advantages and disadvantages. Plastic has advantages like flatness、lucent able and no substrate capacitance effects (like back-gate effect[1.21]). Because of high transmission in the visible range, we can use background emission device applied to plastic substrates. Plastic substrates are usually used in light penetrative elements. Metal foil substrates are usually applied to light reflective elements. In this way, metal foil substrate possible products usually assembled outdoor or under strong light source condition. But it also has disadvantages like high price、low temperature process endurable(critical temperature about$225^{o}C$)、water absorption and high Coefficient of Thermal Expansion(CTE) **[Table1]**. Conversely, metal foil has advantages of low cost、high temperature process endurable(SS304 steel foil critical temperature about $1300^{o}C$)、no water absorption and low Coefficient of Thermal Expansion(CTE) **[Table1]**.So after compared this two substrates material advantages and disadvantages, we choose metal foil (SS304 steel foil) to be poly-Si TFTs substrate in our study and investigate their flexible characteristics (different from inward: Rn and outward: Rp**[1.22]**) and instability analysis.

1.3Review of studies on poly-TFT under DC stress

In order to make LTPS TFTs suitable for advanced circuits, besides the improvement of performance of LTPS TFTs, the improvement of reliability is also significant. Therefore, reliability testing and

understanding of reliability mechanisms become more and more necessary. In LTPS TFTs, several DC stress degradation mechanisms have been reported. In 2002 Satoshi Inoue paper brought up the stress voltage dependence of the V_{th} shift in poly-Si TFTs, as shown in **Figure 1-2**. Thus, in 2003 Satoshi Inoue's paper classified the degenerated phenomena. **Figure 1-3** shows the effect of stress voltage on the I_{on} variation in TFTs. This result indicates two main degradation regions, the stress voltage of region A and region B. At first, hot carrier degradation is considered to originate from the damage of the metal-oxide-semiconductor (MOS) interface and of the channel poly-Si layer near the drain of TFTs. On the other hand, self-heating degradation is thought to originate in breaking of Si-H bonds and regeneration of dangling bonds in the MOS interface and channel poly-Si layers. In region A, the dominant degradation mechanism is self-heating, both the drain and gate voltages are high, typically over 10V. In region B, the dominant degradation mechanism is hot carrier, only the stress drain voltage is high, typically over 10V, and gate voltage is low, typically from 2V to 5V.

1.4 Organization of this thesis

This thesis is organized as followed: in **Chapter 2,** introduction of poly-Si crystallization methods and fabrication process of poly-Si TFTs on metal foil substrate. Simultaneously, the instruments for bending system and current-voltage (I-V) measurement will be introduced. Then we describe the methods of device parameter extraction. In **Chapter 3,**

the experiment processes and conditions will be illustrated. The content includes the current-voltage (I-V) measurement under bending/ flat condition and use X-ray diffraction measurement (XRD) to measure grain boundary orientation and material characteristics. Then we study the reliability of p-channel polycrystalline silicon (poly-Si) thin film transistors (TFTs) on steel foil substrates under drain bias instability stress. We use strain molds which are different form tensile (outward, Rp) and compressive (inward, Rn) **[see Fig1.1]**. There have radius of curvature (R) from 50 millimeter to 10 millimeter in our bending molds.

Then in **Chapter 4,** we try to explain the results of our experiment. After bending several times and then flattens, the threshold voltage (Vth) shift and sub threshold swim (S.S) degradation, but after hundreds of times bending the current-voltage properties would be stable. Then we discuss the electronic properties' variation under strain condition. Under compressive condition the hole mobility is better than flat and in flat condition the hole mobility is better than tensile condition. And we also find out threshold voltage shift and threshold slope degradation no matter what kind of bending status. At last we utilize the DC drain bias stress the elements under bending condition. Although the on current and sub threshold swim degradation, we find out electronic properties under compressive status after stress is better than plan and tensile status. In order to explain the phenomenon, used amorphous silicon and MOS TFTs mechanism to accounts of our experiments is necessary. Finally in **Chapter 5,** we conclude our results and integrate my thesis. And put my future work and poly-Si TFTs technology future application inside.

Chapter 2   Fabrication and Characterization:

2.1 Fabrication process of poly-Si on metal foil

In this research, our TFT process developed for the LCD active-matrix backplanes is a low temperature poly-silicon process (LTPS). The TFTs were fabricated on a SS304 stainless steel foil (thickness=70μm, area=10cm×10cm) by conventional LTPS process, where a-Si is crystallized using a XeCl excimer laser. All of the fabrication of poly-Si on metal foil, we different this part of process flow paths for four parts as follow:

2.1.1 Metal polishing

After degreasing and cleaning, metal foils are polished by mechanical polishing process [2.1], which provides a drastic reduction of roughness. Propose of mechanical polishing process is flatten our substrate less than 2 nm. Average roughness (Ra) was reduced from 95 nm before polishing down to 0.75 nm [Fig 2.1] after polishing which gives finally mirror-like surface [Fig 2.2].

2.1.2 Thick insulator

After that, the buffer layer was coated on the polished steel foil in order to obtain a smooth and pinhole free surface. This insulator can be inorganic, such as PECVD SiNx, but organic materials such as spin coated polymer are also being evaluated. This buffer layer should exhibit

high adhesion to the flexible metal. The buffer layer not only reduced the surface roughness of steel foil but also prevented contamination from steel substrate during the heating processes that a smoother steel foil surface was critical in TFTs process and could improve the TFT alignment in photolithography process. So we spin coating silicon on glass 2um as buffer layer in order to reduce the pin hole and roughness. See this **Figure 2.3** of AFM, before buffer layer process the roughness is about 0.891nm and after buffer layer process the roughness is about 0.499nm. Then we deposited SiNx 3000A as smooth layer. After fabrication of the inorganic SiNx layers, TFT were islanded to release the stress. Therefore, the substrate was flat, indicating no global stress. So PECVD SiNx was preferred to polymer and chosen as insulator layer for the present LTPS process on metal **[Fig. 2.4(a)(b)]**.

2.1.3 LTPS process

After pre-treatment of steel foils, it was glued onto glass for the subsequent LTPS-TFT processes. Figure 2.3 illustrates the conventional LTPS-TFT structure where M1 represents the gate metal and M2 represents the source and drain metal of TFT. The Cr is used as gate, source and drain metal as shown in **[Fig. 2.5]**. The maximum process temperature was 200°C in the CVD processes, including a-Si (50nm), gate oxide (100nm) and inter layer dielectric (ILD) oxide (300nm) deposition. The pulse excimer laser with 308nm wavelength was used to induce the poly-Si crystallization. The crystallized poly-silicon sample was etched by seco-etching solution, and scanning electron microscope

(SEM) was utilized to observe the surface image of poly-Si layer, as showed in **[Fig. 2.6]**. The grain size of poly Si showed in SEM about 0.4 micro meters. The electrical characteristics of p-type LTPS-TFTs were measured by HP4156 parametric analyzer. We used top gate, self-alignment polycrystalline Si TFT, adopting an organic layer as the first gate insulator on metal foil. The self-aligned ion doping technology was used to produce p-type LTPS TFT. The activation process was performed at 450℃ to reduce the resistance of P^+ ion doping area by the rapid thermal process (RTP). At last we use SiNx 1000A as preservation layer and then anneal 2 hours to Hydrogenate by Atmospheric Anneal Furnace. The bus line metals are exposed to high stress during the plasma enhanced chemical vapor deposition (PECVD) process at 200°C because the CTE was mismatched between substrate and metal line. Therefore, the ductility of the bus line metal is important for the electronic device on metal foil substrate. **[Fig. 2.7]**

2.1.4 Introduction of Instruments for C-V Measurement

The electrical test setup of HP4156C semiconductor parameter analyzer is utilized in this experiment, illustrated in **Figure 2.8**, a probe station is situated inside a dark box. The ground probe station is furnished with an electrically isolated, water-cooled thermal chuck. The chuck is controlled by Temptronic TPO315A thermal controller, which can operate temperature from 25°C to 200°C. An Agilent 4156C precision semiconductor parameter analyzer can provide I-V measurement, bias for BTS, and quasi C-V measurement, etc. We employ the ICS (Interactive Characterization Software) to obtain the output and transfer

characteristics, like V_D-I_D, V_G-I_D (Linear), V_G-I_D (saturation), and extract the typical semiconductor parameters.

In order to investigate the effect of the DC gate-bias stress under bending condition (i.e., the gate was given a constant voltage while the source and the drain were grounded) on the electrical parameters of excimer laser annealing (ELA) low temperature poly-silicon TFTs, the p-type poly Si structure on metal foil setup is shown in **Figure 2.7.**

2.2 Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameter extraction such as threshold voltage V_T, subthreshold swing (S.S), field-effect mobility μ_{FE}, flat band voltage V_{FB}, trap density N_t, activate energy Ea, parasitic series resistance R_{pa}, field-effect mobility without the effect of series resistance μ_{FE0} and the strain of the surface $\varepsilon_{surface}$. We will show it as follow.

2.2.1 Determination of the Threshold Voltage (Vth)

Several methods are used determinate the threshold voltage (Vth), which is the most important parameter of semiconductor device. The method we determinate in this thesis is the constant drain current method, the voltage at a specific normalized drain current NI_D is taken as the threshold voltage. This technology is easy to extract and adopted in most TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the specific normalized current $NI_D = I_D/(W/L)$ is defined at 10nA for V_D operated in linear

region and 100nA for V_D operated in saturation region in poly Si TFTs devices, to extract the threshold voltage of TFTs in most papers.

2.2.2 Determination of the Subthreshold Swing (S.S)

Subthreshold swing (V/dec) is a significant parameter to describe the control ability of gate bias toward drain current and the efficiency of the switch turning on and off. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. It should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to the short-channel effects such as charge sharing, avalanche multiplication, and punch through-like effects. It is also related to the gate voltage due to some undesirable factors such as serial resistance and interface state. It is defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude. The formula can be shown that the expression for S.S is given by

$$ SS = \frac{\partial V_g}{\partial (\log I_d)} $$

In general, many researchers use the way to evaluate S.S as follow:

S.S.= [Vg(NId=10nA)- Vg(NId=100pA)] / 2

The threshold current is specified to be the drain current when the gate voltage is equal to the threshold voltage **[Fig2.9]**.

2.2.3 Determination of the field-effect mobility μ_{FE}

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The **field-effect mobility** (μ_{FE}) is determined from the transconductance g_m at low drain voltage (linear region). The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, ignoring any other non-ideal effect and assuming the electric field in the channel is uniform, so the first order I-V relationship in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_T)V_D - \frac{1}{2}V_D^2] \qquad (2\text{-}1)$$

Where C_{ox} is the gate oxide capacitance per unit area

W is channel width

L is channel length

V_T is the threshold voltage.

If V_D is much smaller than (V_G-V_T) (i.e., $V_D \ll V_G$-V_T) and $V_G > V_T$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_T)V_D \qquad (2\text{-}2)$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\bigg|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \qquad (2\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_D} g_m \qquad (2\text{-}4)$$

The mobility value was taken from Equation (2-4) with maximum μ_{FE} .

2.2.4 Determination of the trap density N_t

The extraction method of trap density Nt is as follow. From Seto's

model, we know there are the relationship with grain boundary potential barrier height V_B and doping concentration N_D. When doping concentration N_D [cm^{-3}] increase more than Nt/L We can express the grain boundary potential barrier height VB as follow equation:

$$V_B = \frac{qn}{2\varepsilon_s}\left(\frac{N_t}{2n}\right)^2 = \frac{qN_t^2}{8\varepsilon_s n}$$

Where Nt[cm^{-2}] is density of acceptor-like traps at grain boundary

$\quad\quad$ V_B is the grain boundary potential barrier height

$\quad\quad$ n [cm^{-3}] is the carrier concentration

Based on this consideration, the amount of trap state density N_t can be extracted from the current-voltage characteristics of poly-Si TFTs. As proposed by Levinson *et al.* **[2.2]**, the I-V characteristics including the trap density can be obtained by the following equation

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{TH})V_D \exp\left(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{TH})}\right)$$

This equation had been further corrected by Proano *et al.* by considering the mobility under low gate bias **[2.3]**. It is found that the behavior of carrier mobility under low gate bias can be expressed more correctly by using the flat-band voltage V_{FB} instead of the threshold voltage V_{TH}. Moreover, a better approximation for channel thickness t_{ch} in an undoped material is given by defining the channel thickness as the thickness at which 80 percent of the total charge resides. Therefore, by solving the Poisson's equation, the channel thickness is given by

$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})}$$

(2-7)

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The drain current of poly-Si TFTs then should be expressed as

$$I_D = \mu_0 C_{ox} \frac{W}{L}(V_G - V_{FB})V_D \exp\left(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^2(V_G - V_{FB})^2}\right)$$

(2-8)

The effective trap state density then can be obtained from the slope of the curve $\ln\left[I_D/(V_G - V_{FB})\right]$ versus $(V_G - V_{FB})^{-2}$ as in **Figure 2.10** and we can calculate the slope from it. The grain boundary trap-state density can be determined from the square root of the slope directly, expressed by the simplified equation below.

$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|Slope|}$$

(2-9)

2.2.5 Determination of the parasitic series resistance R_{pa}:

In this section, we want to get the parasitic series resistance. Because there are resistances of any materials, in source/drain parts we called the resistance as parasitic series resistance (R_{pa}) and in channel part we called the resistance as channel resistance (R_{ch}). They can be extracted by well-known transmission line method (TLM) **[2.4-5]** using a series of TFTs with different channel lengths measured at a low source/drain voltage, so we can neglect the space-charge-limited currents (SCLC) effect. The total TFT ON-resistance is as follow:

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch} L + 2R_{S/D}$$

(2-10)

Where r_{ch} is the channel length resistance per channel-length unit and $2R_{S/D}$ is total (source+drain) series resistances. Using equations (2-10)

and (2-2), we can express the total ON-resistance RT as function of μ_{FE} and threshold voltage:

$$R_T = \frac{L}{\mu_{FE}\ C_i W(V_{GS} - V_T)}$$

(2.11)

The same equation applied to the ideal TFT lets us express the channel resistance as a function of the intrinsic mobility (μ_{FEi}) and threshold voltage (V_{Ti}), which are representative of the conduction channel material, without the influence of the TFT series resistance:

$$r_{ch} = \frac{1}{\mu_{FEi}\ C_i W(V_{GS} - V_{Ti})}$$

(2.12)

The extraction of the TFT source and drain series resistance and intrinsic field-effect mobility and threshold voltage is rather straightforward using a series of TFTs with different channel lengths. So we use different L and RT to plot the total ON-resistance as a function of the TFT channel length for different gate voltage. Ensuring that the TFT is in accumulation layer, and then we fit the experimental data to linear curves. We show in **Figure2.11**. In the cross-point of fitting linear curve, we can obtain $2R_{S/D}$ from the y-intercepts. And then we can express field- effect mobility without series resistance as follow **[2.6-7]**:

$$\frac{1}{\mu} = \frac{1}{\mu_i} + R_p\left(\frac{W}{L}\right)C_G(V_G - V_T)$$

(2-13)

Where μ is the carrier field-effect mobility with series resistance

   μ_i is the carrier field-effect mobility without series resistance

   R_p ($R_{S/D}$) is the series resistance

   C_G is the gate oxide capacitance

2.2.6 Determination of the strain of the surface:

In order to define the strain percentage to our investigation, we must find out the respective Young's modulus of steel foil (Ys) and substrates (Y$_f$). In our cases, Young's modulus of film and substrate for both Y$_f$ and Y$_s$ are 200 GPa **[2.8-10]**. The strain of surface function is given by:

$$\varepsilon_{surface} = \left(\frac{d_f + d_s}{2R}\right)\frac{\left(1 + 2\eta + x\eta^2\right)}{\left(1 + \eta\right)\left(1 + x\eta\right)}$$

(2-14)

Where $\eta = d_f/d_s$ and $x = Y_f/Y_s$, here, $d_f = 0.8\mu m$ and $d_s = 80\mu m$. There is compressive or tensile strain with radius R $= \infty$, ± 50, ± 40, ± 30 and ± 10 mm. So after transforming with strain equation, we can get the equivalent strain quantity shown in **Table 2**.

2.3 Experimental Procedures of Flexible characterization of P-type poly-Si on metal foil

2.3.1 Experiment of flexibility test for p-type poly-Si on metal foil:

After fabrication of p channel polycrystalline silicon TFTs on metal foil, we measure electronic property by semiconductor parameter analyzer 4156. It exhibits superior characteristics such as field-effect mobility of 92 cm^2/Vs, a threshold voltage of -5.4 V, and an on/off current ratio of more than 10^7 and substhreshold slope of 0.82 V/dec **[Fig.2.12]**. But how could we know if the electronic property be affected after bending several times. So we must use the flexibility test first before bending experiment. The device picture is shown in Figure 2.2. The

length and width is 10 x 10cm. we inflict the tensile stress (outward) to 6 cm parallel source/drain channel and then flat. We repeat to have back and forth bending 1~100times to the condition of test and then flat to measure the electronic characteristic of ID-VG and ID-VD. Then we repeat to have back and forth bending 400times (500times bending) to test and then flat to measure the electronic characteristic of ID-VG and ID-VD. Last we repeat again to have back and forth bending 500times (total 1000times bending) and then flat to measure the electronic characteristic of ID-VG and ID-VD. The model is shown in **Figure2.13**.besides outward flexibility test we also inflict inward bending tests in another new device. The radius of flexible curvature is 20 millimeter and transform to surface strain is about 0.281%. Then we measure and take pictures by optic microscope Charge Coupled Device (CCD) shown in **Figure2.14**.

2.3.2 Experiment of electronic property variation under bending status:

In this part, we use models of bending radius of curvature (R) from 50 millimeter to 10 millimeter in our bending molds. That's different into compressive and tensile two parts **[Fig. 1.1]. [2.11]-[2.12]**. After the test of flexible device stability, we make sure the electronic property stable. Then we start the experiment of electronic properties variation under bending status by these devices. The bending molds are shown in **Figure 2.15** that the radius of curvature from 10 millimeter to 50 millimeter. We defined the bending direction shown in **Figure 2.16**.The strain force which device suffered defined for uniaxial strain

and biaxial strain. Because of different channel devices in the same substrates, the strain force is the same in different channel position or there exhibits two direction strain forces in three dimensional spaces; we call biaxial strain (global strain). There is different strain force in different channel position in the same device; this kind of strain is one dimensional strain force in three dimensional spaces which we called uniaxial strain (local strain). In our investigation the strain force is uniaxial strain and parallels the source/drain current channel. We measure the drain current virus gate voltage curve and drain current virus drain voltage curve under bending status by HP4156 parametric analyzer. In order to make sure of the increase of state in polycrystalline Si channel material under the inwardly and outwardly bent situation, the activation energy (E_a) of polycrystalline TFTs with different bending situation was extracted from varied temperature measurement in the temperature range from room to 150°C.

2.3.3 Experiment of DC bias stress under bending condition:

After measurement under bending status, we flat again and make sure the property return. Then we start the experiment of instability under bending condition. First, find out two different test keys but same length/width in one sample. Then measure the electronic property in one test key; supply -20 voltage drain bias stress and -20 voltage gate bias stresses as **Figure 2.17** in order to see the self heating effect in 10, 100, 1000 and 2000 seconds. The TFT length/width is 30 over 10 micrometers. Second, we repeat the drain and gate bias stress measurement in another test key of the same sample under tensile status in 10, 100, 1000 and 2000

seconds and then flatten again to mature the electronic properties. Last we repeat the drain and gate bias stress measurement in the same length/width test key of another sample under compressive sample in10, 100, 1000 and 2000 seconds and flatten to mature the electronic properties again.

Chapter 3 Results and discussion:

3.1 Electrical Performance after Flexibility Test of P-type Poly-Si on Metal Foil

3.1.1 Electrical Performance after First-time and multi-times Flexibility Tests:

After the flexibility tests, we extracted the Gm maximum, mobility and threshold voltage to compare with the electronic properties after many times flexibility. It is shown in **Table 2**. We find out the mobility changes very small after 1, 10, 100,500 and 1000 flexibility tests. But threshold voltage shift during 100 times bending tests then become stable. In **Figure 3.1(a)-(b)**, there are all serious threshold voltage shifts at first bending test about 0.2 voltage shifts. Then after first bending test, the property becomes stable little by little. Finally 500 times bending create 0.004 voltage shifts and we think it almost in error value ranges. There is more serious shift on inward bending test. But mobility is not change very much under inward or outward flexibility test. We transform rate of mobility change after 1000 times test; it is less than 0.9%. In this way we consider the mobility is very stable after 1000times inward and outward test.

For the results, we assume when we bend first times create mass broken bonds by bending strain. Because there is also density of states in poly silicon **[Fig.3.2]**, deep states near mid-gap are associated with broken bonds and shallow tail states are associated with strained bonds. We consider the flexible action will account broken bonds increase at first 100 times. Then the weak bonds in deep states broken but other

strong bonds did not be effected so after 100 times tests the characteristics become stable. In order to verify our think, we try to extract the trap density.

3.1.2 Analysis of trap density Extraction:

In **Figure3.3-4**, we extracted the trap density clouding flat to 1000 times flexibility tests. The variation rate of trap density from first 100 times tests is about 5.357% and last 900 times tests is about 0.068% of inward test. And variation rate of trap density from first 100 times tests is about 5.31% and last 900 times tests is about 0.084% of outward test. So this results show no mater outward or inward bending will account broken bonds increase after first 100 times bending tests. And inward test create more damage than outward test. We assume compressive strain cause more serious damage than tensile strain in our case. Then we believe the device characteristic become stable step by step.

3.2 Electrical Performance under Different Mechanical Strain
3.2.1 Electrical Property Variation under Different Bending Status:

Before the mechanical stress applied, we make sure the device property already pass flexibility test and characteristic becomes stable. In this way we can use mechanical bending molds to bend our sample several times and the device keeps the characteristics. The p-channel LTPS TFTs we measure before mechanical bending exhibited superior characteristics such as field-effect mobility of 92 cm^2/Vs, a threshold voltage of -5.7 V, and an on/off current ratio higher than 10^7 and substhreshold slope of 0.85 V/dec. However, a slight increase of

subthreshold slope (SS) from 0.85(R= ∞) to 1.02 V/dec(R_n=-10mm) was observed in the case of compressive stressing(the insert of **Fig3.5(a)**) while SS increased from 0.85(R= ∞) to 0.97 V/dec(R_p=10mm) with the increase of tensile strain, shown in **Fig3.5(b)**. It also was observed that the threshold voltage of poly-Si TFT devices, applied at V_D= -10 V, increased as a function of either compressive or tensile strain with radius R= ∞, ±50, ±40, ±30 and ±10 mm. We enlarge the I-V curve on the upper right corner of the figures. Then transformed the strain of the surface **[Table3]**, we draw the threshold voltage virus strain percentage in **Figure 3.6**. The creation of the dangling bonds in the polycrystalline silicon is mainly due to the breakage of weak Si-Si bonds during mechanical strain measurements **[Fig3.2]**. The bond strength can be affected by the strain and thus the creation of dangling bonds will depend on the curvature **[3.1-2]**. Therefore, this could cause the enlargement of threshold voltage with increasing mechanical strains. The compressive strain (inward) create more dangling bonds in the polycrystalline silicon than tensile strain; the results agree with the flexibility tests which showed inward test threshold voltage shift more serious than outward test. **Figure 3.7** shows the normalized mobility virus strain percentage. An abnormal results that mobility increase under compressive bending condition but decrease under tensile bending condition. For this normalized results, we try to analyze activation energy and trap density to find out the reason.

3.2.2 Analysis of Activation Energy and trap density Extraction:

We utilize varied temperature measurement in the temperature range from room to 120℃ to extract the activation energy (E_a) of

polycrystalline TFTs with different bending situation showing as follow **Figure3.8 [3.3]**. The energy barrier of tensile is higher than flat curve, and compressive curve is lowest. So there is the lowest energy barrier in compressive curve. This result matches our experiment. For more intimate investigation, we try to find many kinds of models in poly crystalline silicon strain effect. We extracted the trap density under different bending condition to investigate the trap density variation in **Figure 3.9 (a)-(b)**. Then we calculate the trap density variation rate. In 0.08% strain(R=50mm), the variation rate is about 0.9% in tensile status but in 0.1347% strain(R=30mm) it is about 2.68 % until 0.404% strain(R=10mm) means after 0.1347% strain the trap increase slightly. The same phenomenon appeared in compressive status, in 0.08% strain, the variation rate is about 1.15 % in tensile status but in 0.1347% strain it is about 4.21 % until 0.404% strain. Once we mature in bending status no matter what compressive or tensile condition, the trap densities increase. So we explain the bending action measurement would act trap densities and under compressive status more serious. But generally the electric characteristic is still very will. But in the other way, we don't know which mechanisms affected the drain current variation, so it is necessary to clarify our results step by step. One of conditions is the effect of parasitic series resistance.

3.2.3 Analysis of Parasitical Series Resistance Extraction:

To make sure if parasitic series resistance affects the mobility under bending status. The way we use is to measure the different channel length I-V curve on another device under flat, compressive and tensile

status. And then extracted the parasitic series resistance and field effected mobility except parasitic series resistance to discuss the difference of mobility. The channel length we measure from 2 to 50 micro meters and width length 10 micro meters and strain percentage from -4.04% (Rn=10mm) to 4.04% (Rp=10mm). The **figure 3.10(a)-(b)** illustration of the transmission line methods used to extract the S/D series resistance. The total ON resistance R_m*W has been plotted as a function of the TFT channel length for different gate voltage. The cross-point equal two times of R_{pa} is about 7.7 kΩ. So R_{pa} in flat status is about 3.85 kΩ. Different radiuses of curvatures have different R_{pa} **[Fig 3.11].** We extracted five times and calculate arithmetic mean in our error bar. In figure 3.11 the parasitical series resistances are almost straight in different bending status. After calculation of every bending status, we draw the normalized mobility except parasitic series resistance virus strain percentage in **Figure 3.12 [3.4]** and we also draw different channel length normalized mobility except parasitic series resistance virus strain percentage to see the integral trends **[Fig 3.13]**. In these two figures we can see even except parasitic series resistance the compressive condition still has high mobility than flat and tensile condition has lowest mobility from channel length 2 to 50 micro meters. So we can find out the mobility still affected by strain percentage even the mobility already rejected parasitic series resistance effects. This means parasitic series resistance is not the main reason affected mobility change. Even under different strain percentage the series resistance change very little and we think this is not for mobility increase reason under compressive condition. So we try to find other possibility to explain our results. These characteristics are similar to

those in the single crystalline metal oxide semiconductor devices, due to the strain-induced band splitting effects **[3.5]**.

3.2.3-1 Factor affects single crystalline Si mobility:

We utilize p-channel metal oxide semiconductor devices strain mechanism **[3.5-6]** to explain our results. Recently many researches for biaxial (uniaxial) strain effects of p-channel and n-channel MOSFET improve the drain current **[3.6-10]**. The **table 4** arranges the biaxial (uniaxial) strain effects to PMOS and NMOS drain current. We can find out biaxial tensile strain could improve PMOS and NMOS drain current simultaneously, but uniaxial strain effects improve one device instead of depraving another device [example: tensile (compressive) modify NMOS (PMOS) but deprave PMOS (NMOS)]. These devices characteristics attribute to changing of mobility in drain current equation by strain effects. If it examine carrier mobility change by band structure related parameter, the carrier distributed rate in valley band、scattering rate and effect mass are the most direct reasons of these three parameters. There are three factors affect single crystalline silicon mobility: silicon thickness、surface orientation and strain. First, all of our samples have the same silicon thickness about 500Å so this factor is constant. Second, the surface orientation relationship graph is in **figure 3.14[3.10-11]** and because our samples under the same crop of TFT devices, so the surface orientation are the same. In PMOS device, there is the highest hole mobility in (110) direction parallel the source/drain current path because of carrier repopulation **[3.11].** It also indicates that (110) surface

orientation provides the higher drain current in compressive status than flat status. Because our samples are poly silicon TFT device, there is not only one surface orientation in our samples. The strain direction is dependant of mobility of gain for (110). In (110) surface for example, mobility of gain is overwhelmingly larger than those in the other channel direction. When the bending direction parallel the surface orientation (110), the tensile condition get low mobility of gain and compressive condition get higher mobility of gain. In our case, we must know the surface orientation so we sand a material sample to take XRD measurement. We use X-ray diffract meter (XRD) to analyze our sample surface structure in **figure 3.15 (a)-(b)**. In order to make sure the XRD pulse of poly film is not affected by substrate material, we scan x-ray diffraction in positive and negative way simultaneously. We analyze the structure in **Figure3.16 (a)-(b)**. The pulse *FeCr0.29Ni0.16C0.06* is also existed in both positive and negative. We indicated that is our substrate material pulse. So off with *FeCr0.29Ni0.16C0.06* pulse, we can indicate (111) (110) (100) in our poly silicon samples. (4,0,0) pulse is the same orientation with (1,0,0) but in other views, so (2,2,0) pulse is the same orientation with (1,1,0) but in other views and (2,2,2) pulse is the same orientation with (1,1,0) but in other views. We know as long as it exhibited (1,1,0) pulse, we can get higher drain current in compressive condition and worse drain current in tensile condition.

3.2.3-2 Single crystalline strain effect:

Figure 3.17 showed that silicon structure conduction band and valence band varied illustration before unstrained and after uniaxial

(biaxial) tensile and compressive strain. These characteristics are similar to our poly silicon device on metal foil! Before strain effect, the six valley bands of silicon conduction band energy degenerated, and heavy hole (HH) and light hole (LH) of valence bands are also energy degenerated. When biaxial tensile strain inflicted, the in-of-plane lattices are stretched and out-of-plane lattices compressed **[3.5] [3.13]**. It corresponded kx and ky direction fourfold degenerate (Δ4) energy band upgrade and kz direction twofold degenerate (Δ2) energy band downgrade. So most electrons distributed in twofold degenerate (Δ2) energy band because of lower energy band, the effect mass decrease. Besides this, the biaxial strain leaded to strain-induced band splitting then another way degrade inter-valley scattering rate and effect density of states of conduction band. In this way lower effect mass and inter-valley lower scattering rate leaded to electron mobility increase and improved drain current. The same reason as uni-axial strain, **figure 3.18 [3.11]** uppers are schematic illustrations of strain induced carrier repopulation among six valleys in silicon conduction band. Applied strains are uni-axial tensile and uni-axial compressive strain along <110> which is Si single crystal surface orientations. The change of six valleys in silicon conduction band is dependent on surface orientation, strain and silicon thickness as the above-mentioned **[3.11]**. Because all of our devices are follow one thickness of silicon layer, 50 nanometers, so the susceptible factors of six valleys in silicon conduction band are surface orientation and strain. **Figure 3.19** showed the surface orientation and current flow directions. The in-plane channel direction (θ) is defined as an angle between the channel and the notch orientation. The bottoms are schematic

representations of the qui-energy lines of conduction band and valence band **[3.14] [3.15]** for each surface. So we can know the qui-energy lines of conduction band and valence band are different in different surface orientation. In our case, the effected factors of uniaxial tensile and compressive strain:

1. Cause of light hole and heavy hole separation then reduce scattering effect, so τ(mean free time) increase.

2. Cause of apparent band warping, then hole effect mass reduce (Mn).

Because mobility is equal electron quantity multiply mean free time over hole effect mass, so uniaxial compressive could increase μ.

3.3 Reliability Analysis of poly-Si TFT under Bending Condition
3.3.1 Gate DC Bias Stress Reliability Investigations:

In this section, we use three the same length/width (10/30micro meters) but different test keys to measure the I-V curve. First one we stress 10 seconds to 2000 seconds DC bias stress in flat status in Figure 3.20 as comparison. There are obvious on current degrade after 1000 seconds stress. After 2000 seconds stress, the threshold voltage shift about 0.17 volt and mobility variation rate is about 49.4% but S.S degraded unobvious. Then we measure another two test keys for DC drain bias stress from 10 to 2000 seconds under compressive (Rn=10) and tensile (Rp=10) status **[Fig 3.21 (a)-(b)]**. There are also on current degradation after 1000 seconds DC stress and obvious S.S degradation. In order to compare with the stress effect under different bending status, we draw the threshold voltage shift and normalized mobility virus strain

percentages in **figure 3.22-3.23**. In these figures, threshold voltage and mobility decrease slightly after 1000 seconds DC bias stress but they are still decrease seriously after 1000 seconds DC bias stress in bending status.

3.3.2 Comparison of Electrical Property under Different Condition

There is superior characteristic in compressive status than tensile status after stress, and more than this, we calculate mobility variation rate comparison before and after stress in **figure 3.24**. Under three different status, there are still damaged after 1000 seconds in bending status. After 2000 seconds stress, compressive status has better characteristics than flat status and the worst is under tensile status. We explain the mobility affected by strain so silicon six valley bands separated and band warping in compressive condition. In bending status there are electron accumulations in silicon lattice surface so the mobility decreased slowly. But after 1000 seconds the accumulated electrons affected so the mobility continued degradation. Because of six valley bands warping, the DC bias stress damaged slightly than flat status. And there is the worst mobility performance because of light hole and heavy hole keep near to each other in tensile condition. There is more than one effect exhibit in the DC bias stress experiments.

Chapter 4 Conclusions and Future Work:

4.1 Conclusion:

In this thesis, we fabricated P- channel polycrystalline thin film transistors on metal foil and it exhibited superior characteristics such as a field-effect mobility of 92.45 cm2/Vs, a threshold voltage of -5.7V, the subthreshold slope of 0.85V/dec at VD=-10V, the I_{on}/I_{off} ratio greater than 10^7. Then we make these samples in flexibility tests in order to conform if flexible action influences the electric property. We find out first 100 times bending tests make most serious damages and trap densities then become stable step by step. After this, we measured the electric properties under different radius of curvature bending status and fund out the threshold voltage degraded following the strain percentage. And it has greater mobility in compressive condition than flat and tensile conditions. After extracted parasitical resistances and activation energy and trap densities, we assumed this effect is because of silicon lattices warping and light hole and heavy hole separated so the effect field mobility changed. Last in DC drain bias stress under bending status, threshold voltage shift and on current degraded slightly after 1000 seconds stress in flat condition but it still damaged silicon lattices even after 1000 seconds under bending status. But no matter stress or flexibility tests or mechanical bending measurement, inward (compressive) status has serious internal damage than outward (tensile) and greater mobility performance. We believe these researches will improve the development of poly TFTs on metal foil technology. E-book and e-labels and flexible signage industry may become practical.

4.2 Future work:

After these researches, we will investigate poly-Si TFT AC bias stress under bending status to discuss protracted alternating current influence. For life's application, we will sustain to research poly-Si TFT stress in sun's rays under bending status and compared with our results. Last for electric labels application, we will research with small size poly-TFT on metal foil under sun's ray's illumination.

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Table:

Table1: Comparion of different substrates characteristics

	Metal Foil				Plastic	μ-Glass	Glass
Substrate	Ti	SS304	Fe/Ni	Al	PES	Eagle 2000TM	Corning 1737
Tg (°C)	1668	>1300	N/A	660	225	725	666
CTE(ppm/°C)	8.6	17.3	1.7-2.0	23.5	55	3	3.76
Water Absorption	0	0	0	0	1.4	0	0
Density(g/cm^3)	4.507	7.86	8.0	2.7	1.37	2.36	2.54
Weight g/cm^2		0.04/0.024			0.03		0.18
Thickness(mm)	0.1	0.05/0.03	0.1	0.2	0.2	0.1	0.7
Cost (NTD/cm^2)		0.27 (30*30)			0.33 (30*40)	5 (10*10)	0.458 (37*47)

Table2: the electric properties of inward and outward flexibility tests

10/50	Flat	inward100	Inward500	Inward1000
Gm	5.2E-8	5.24E-8	5.236E-8	5.24E-8
Vth	-7.435	-7.63	-7.701	-7.705
Mobility	123.4	123.3	123.22	123.3
10/30	flat	outward100	outward500	outward1000
Gm	1.37E-7	1.366E-7	1.36E-7	1.358E-7
Vth	-6.13	-6.32	6.327	6.33
Mobility	64.5	64.31	64.01	63.93

Table3: transform from radius of curvature to surface strain percentage

R (mm)	Strain (%)
10	0.404
20	0.35
30	0.1347
40	0.101
50	0.0808
flat	0
50	-0.0808
40	-0.101
30	-0.1347
20	-0.35
10	-0.404

Table 4: the relationship between biaxial (uniaxial) strain and NMOS (PMOS) drain current

Compared with Ctrl	NMOS I_{dsat}	PMOS I_{dsat}	Example
Biaxial tensile	↑	↑	Strained Si/ relaxed SiGe
Biaxial compressive	↓	↑	Strained SiGe on insulator
Uniaxial tensile	↑	↓	CESL (100)/<110>
Uniaxial compressive	↓	↑	SiGe SD (100)/<110>

Figures:

Figure1.1 illustration of mechanical bending measurement
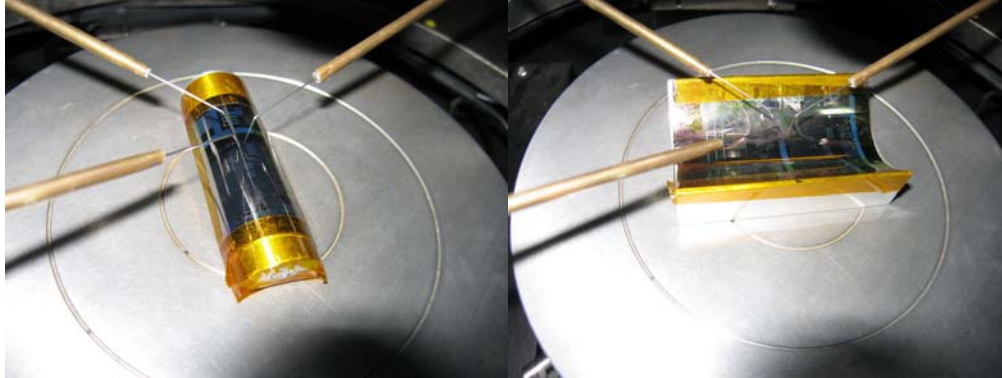
Figure1.2: Stress voltage dependence of the V_T shift of the TFTs
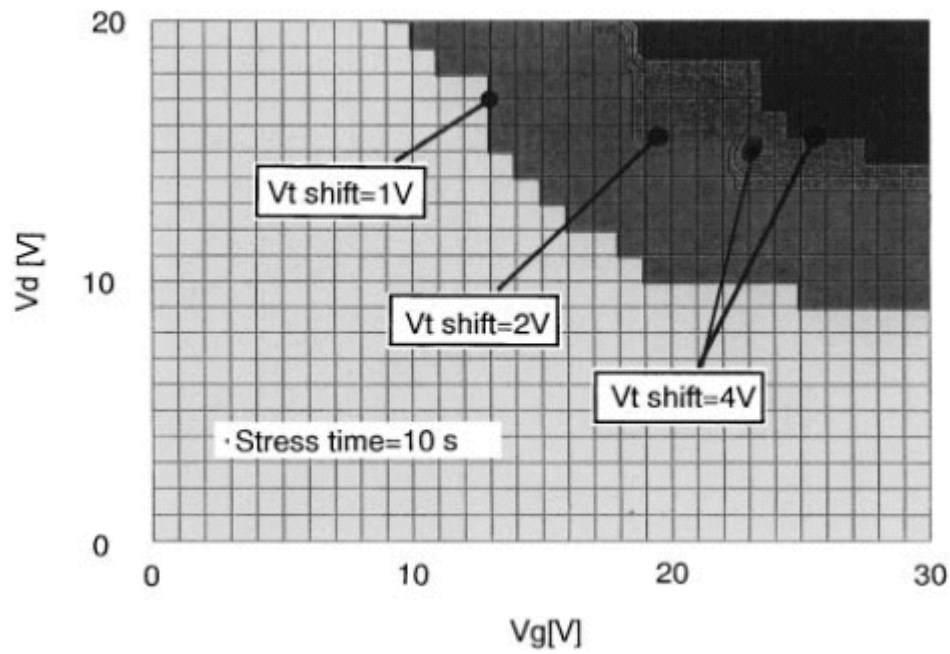
Figure 1.3: Dependence of stress voltage on the I_{on} variation in the TFTs
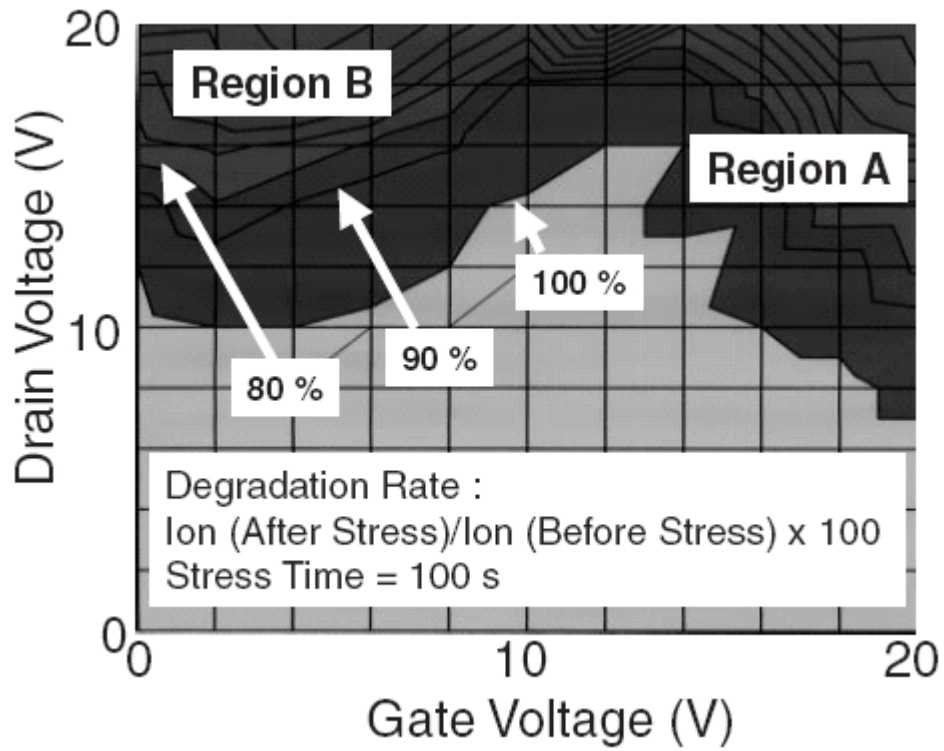
Figer2.1 comparison of roughness before and after mechanical polish

Before polish   After polish
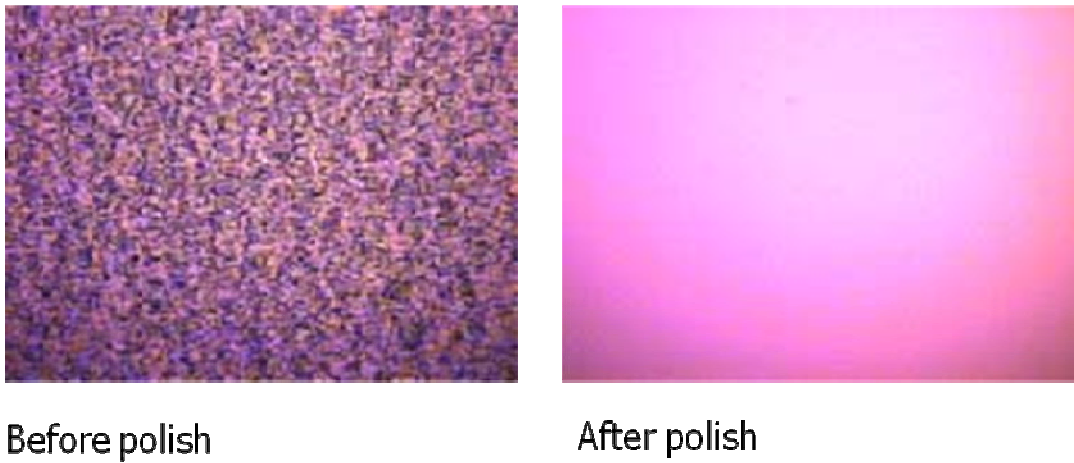
Figure2.2: mirror-like surface poly-Si TFT on metal foil

Figure 2.3:AFM of before and after buffer layer (SoG) process.
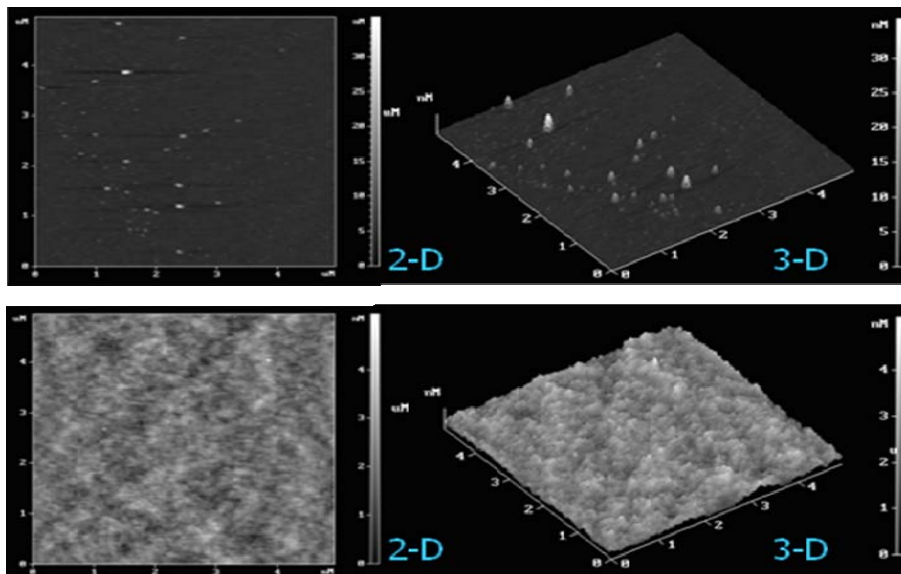
Figure 2.4

(a)No SiNx on buffer layer as flatten layer. There are many particles and defects.
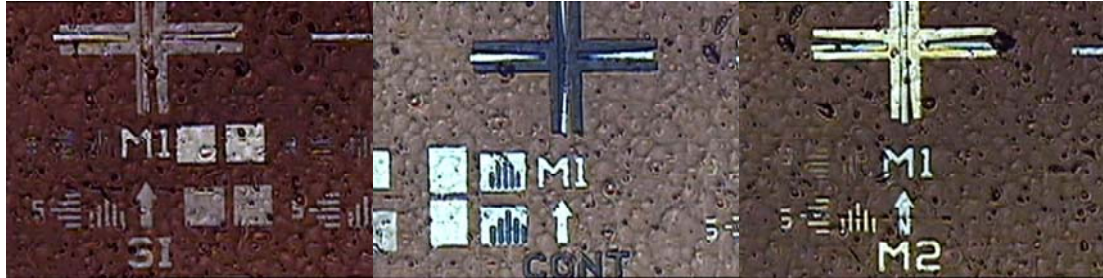
(b)Have SiNx as buffer layer.
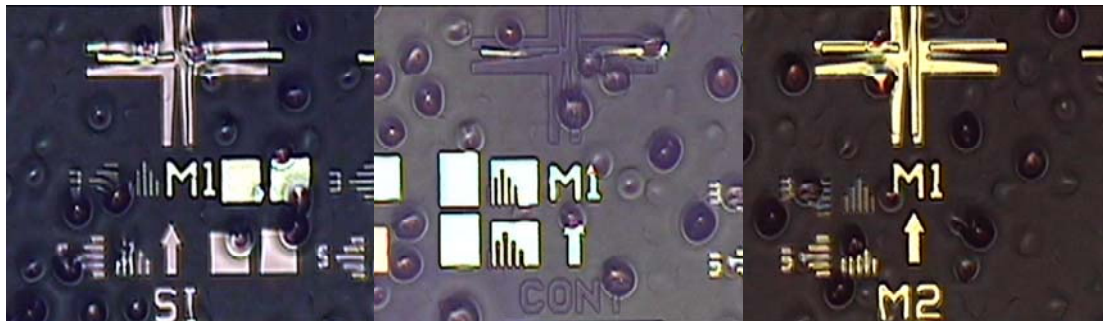
Figure 2.5 the illustration of poly silicon TFT on metal foil
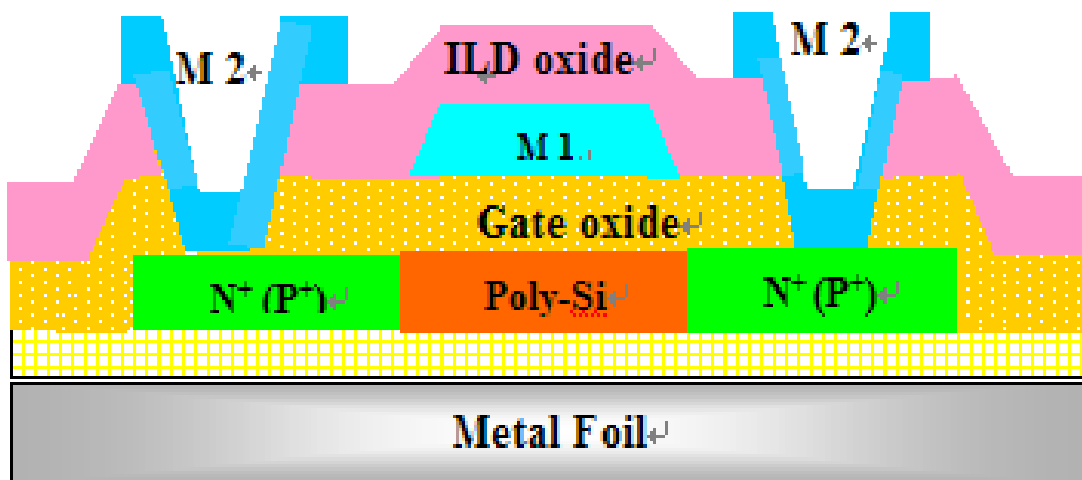
Figure 2.6: the surface illustration of SEM. Grain boundary of poly-Si is about 400 nanometers.
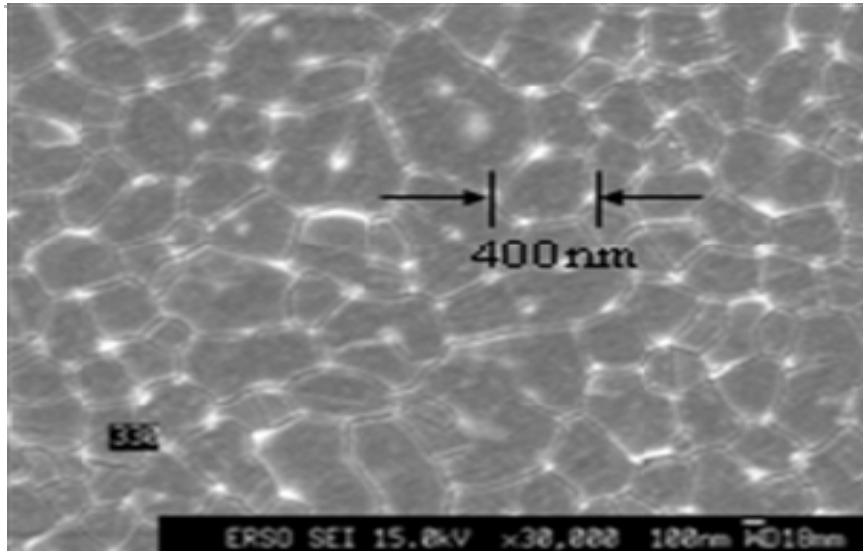
Figure 2.7 after P-channel LTPS-TFTs fabricated on metal foil
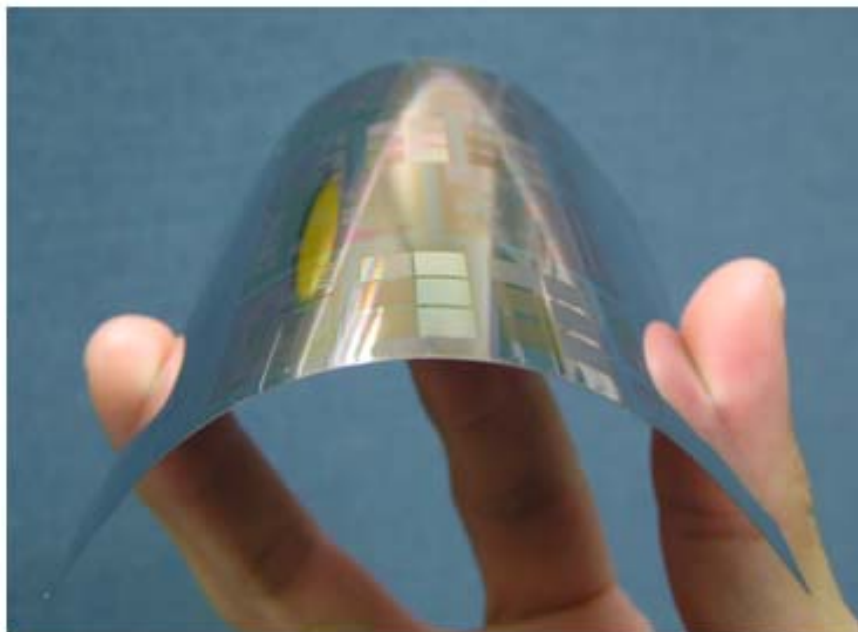
PMOS LTPS-TFTs fabricated on metal foil

Figure 2.8 I-V/C-V instruments set up in the laboratory.

4284A

C-V
measurement

Probe switch connect

E5250A

substrate connection

ground

heat

connect

TPO 315A

Thermal controller

4156C

I-V 1896

measurement
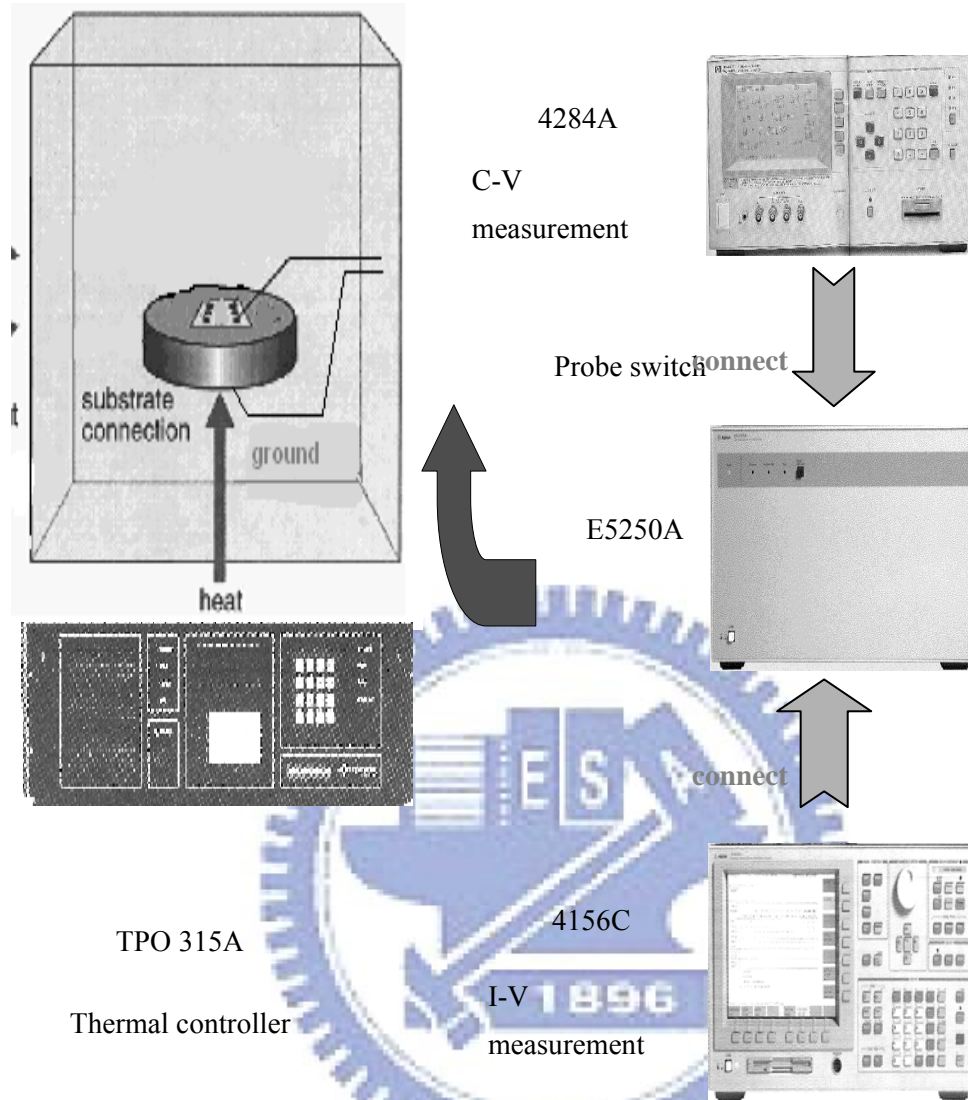
Figure 2.9: the way to extract subthreshold swing

$\log(I_D)$

$\Delta\log(I_D)$

ΔV_G

V_G
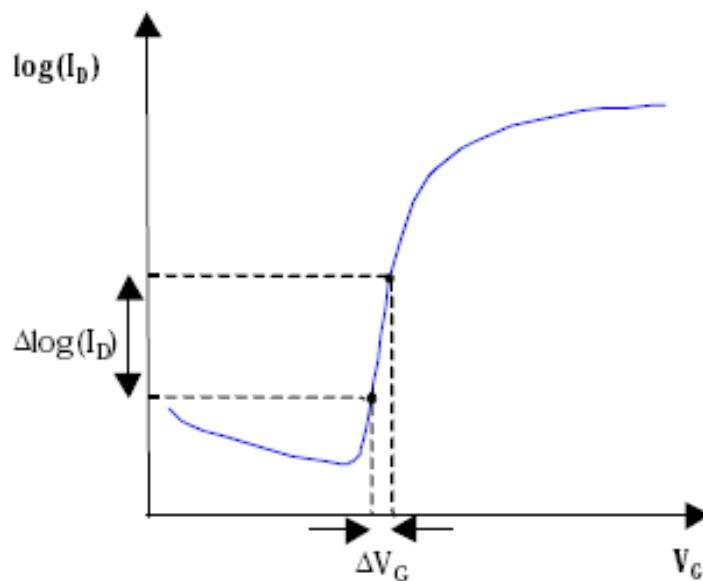
Figure 2.10   Plotting of $\ln\left(\dfrac{I_D}{(V_G - V_{FB})}\right)$ versus $(V_G - V_{FB})^{-2}$.
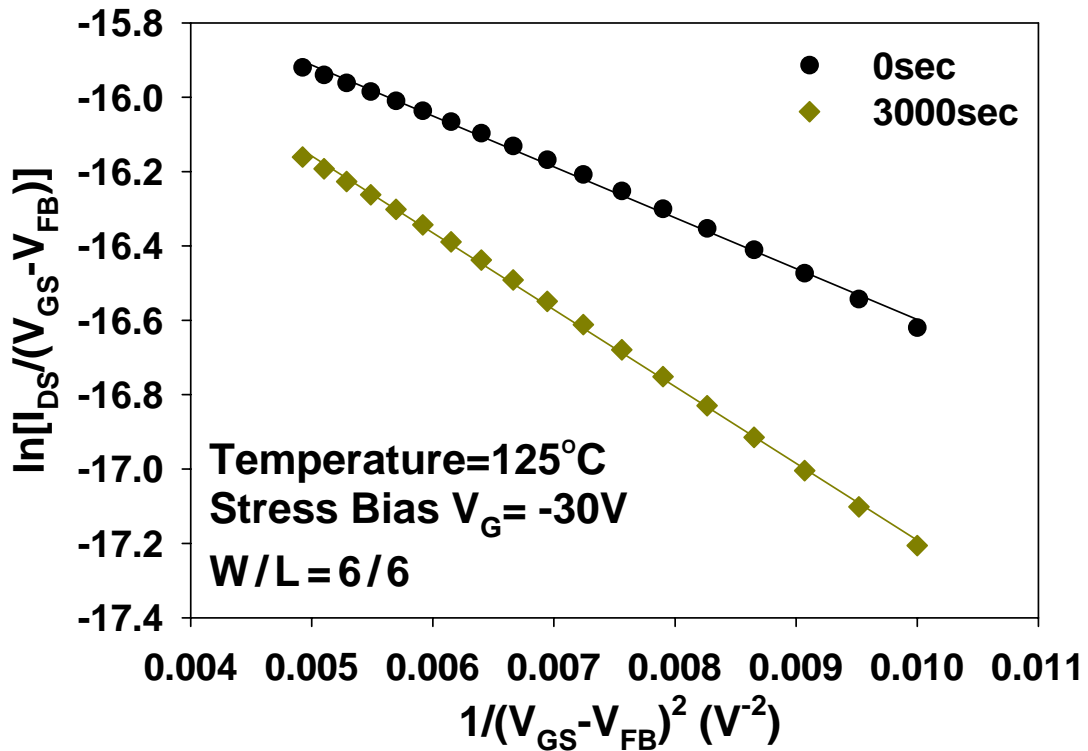
Figure 2.11: the extraction of parasitical resistance
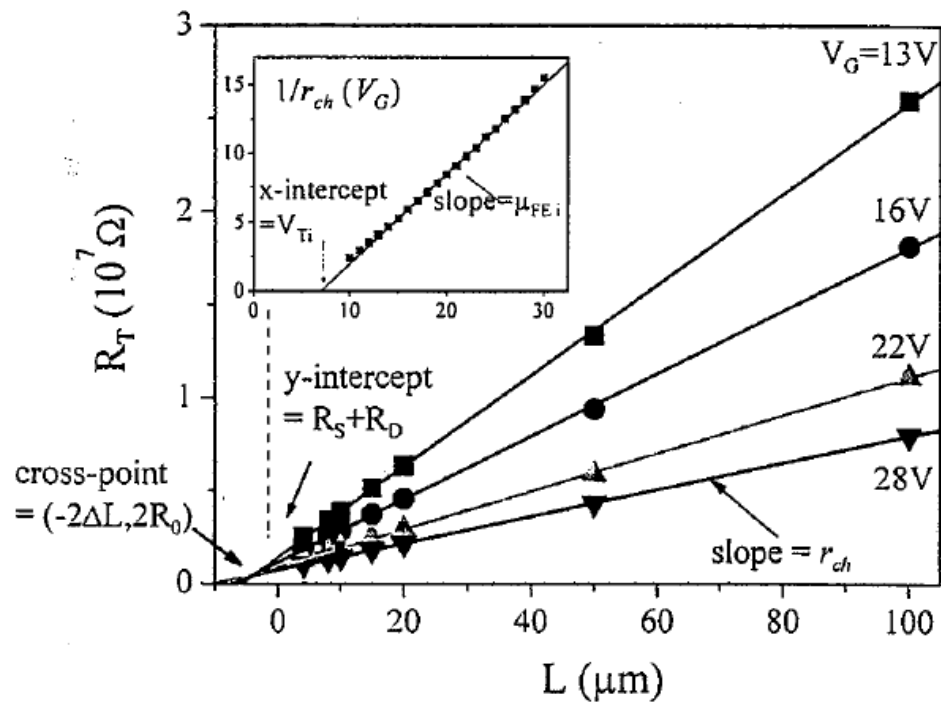
Figure 2.12: the superior characteristics of I-V curve after P-channel

poly-Si fabricated on metal foil
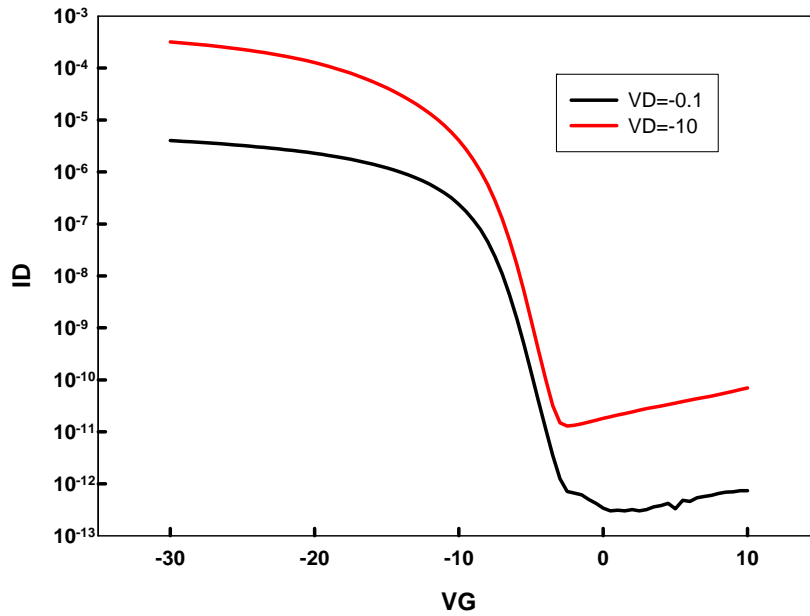
Figure 2.13 illustration of inward and outward flexibility test
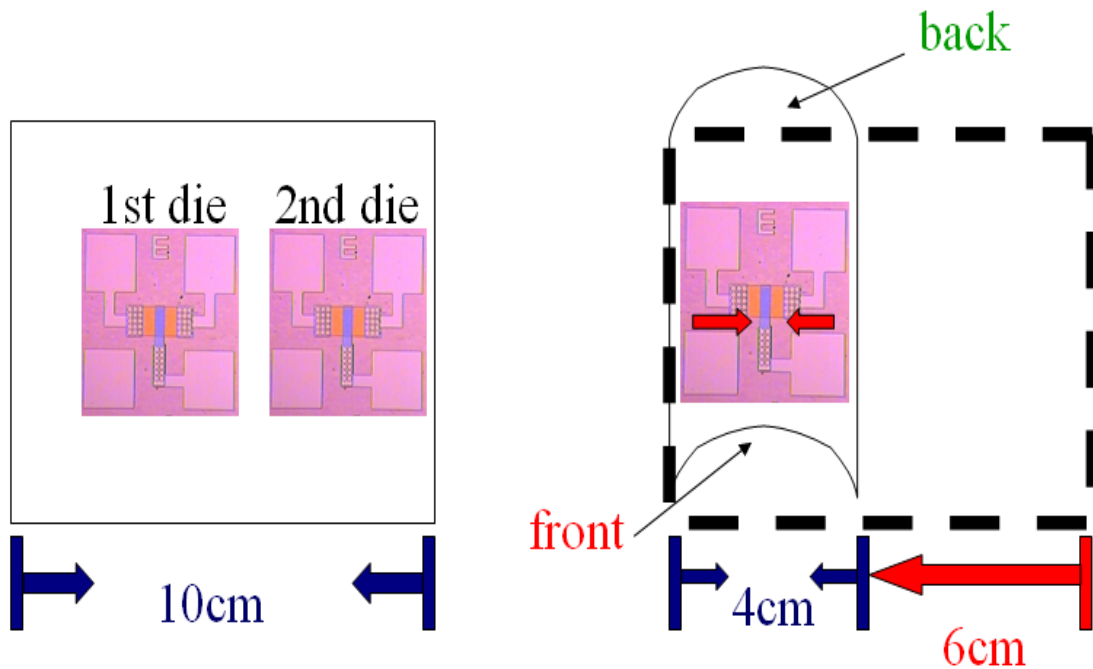
Figure2.14 (a)no outward flexibility test

(b) after 1000 times outward bending test
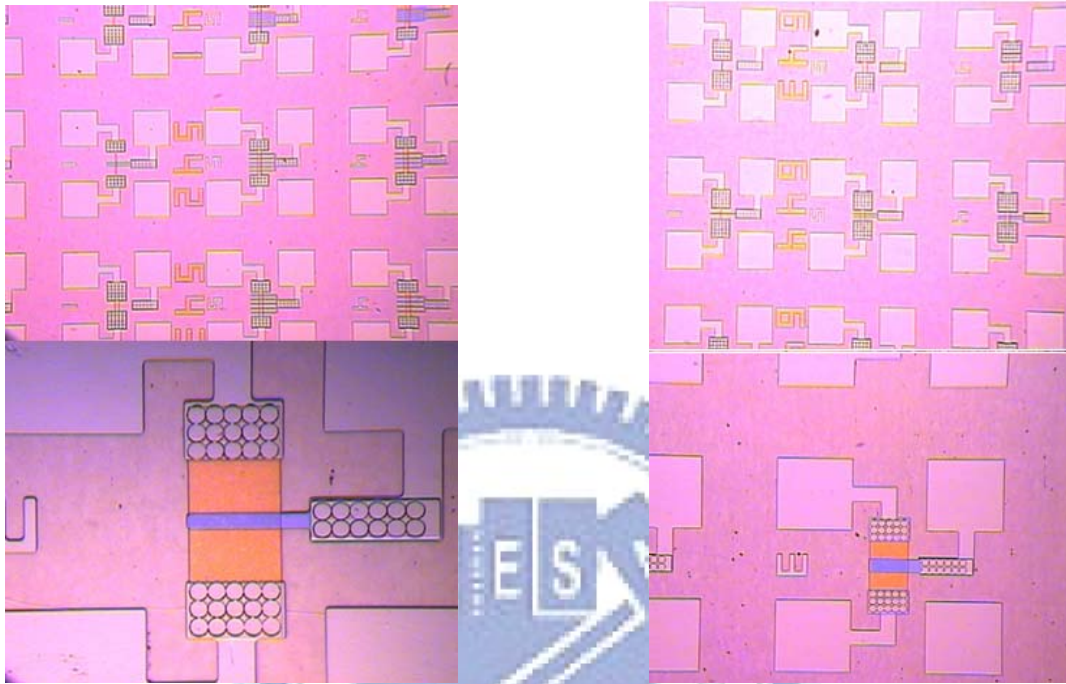
Figure 2.15 the photos of bending molds

Figure 2.16 definition of bending direction. Our direction is parallel to
source/drain current path.
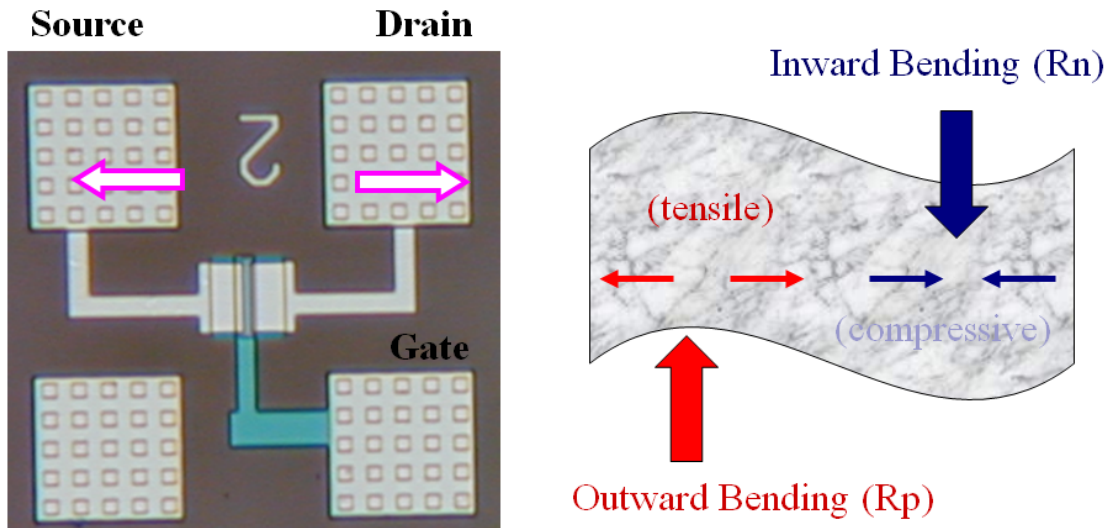
Figure 2.17 model of DC bias stress condition.
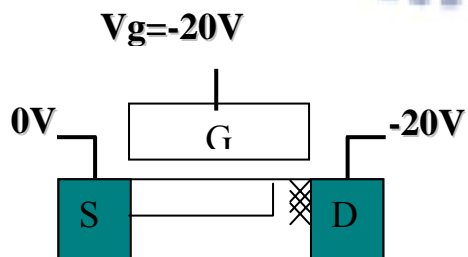
Figure 3.1 (a): illustration of threshold voltage shift after 1000 times of

inward (outward) flexibility tests
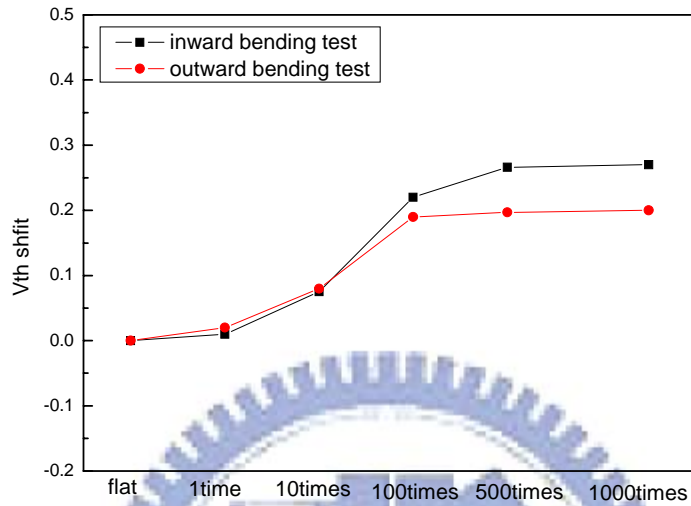
Figure 3.1 (b): illustration of normalized mobility change after 1000

times of inward (outward) flexibility tests
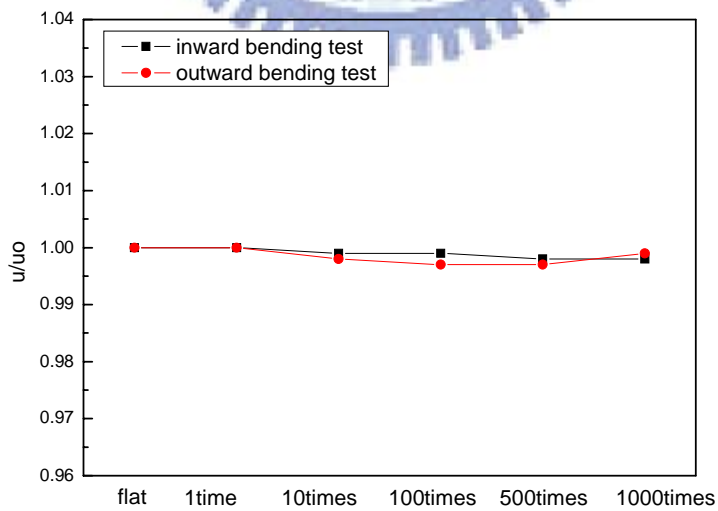
Figure 3.2 Poly-Si Density of States Distribution
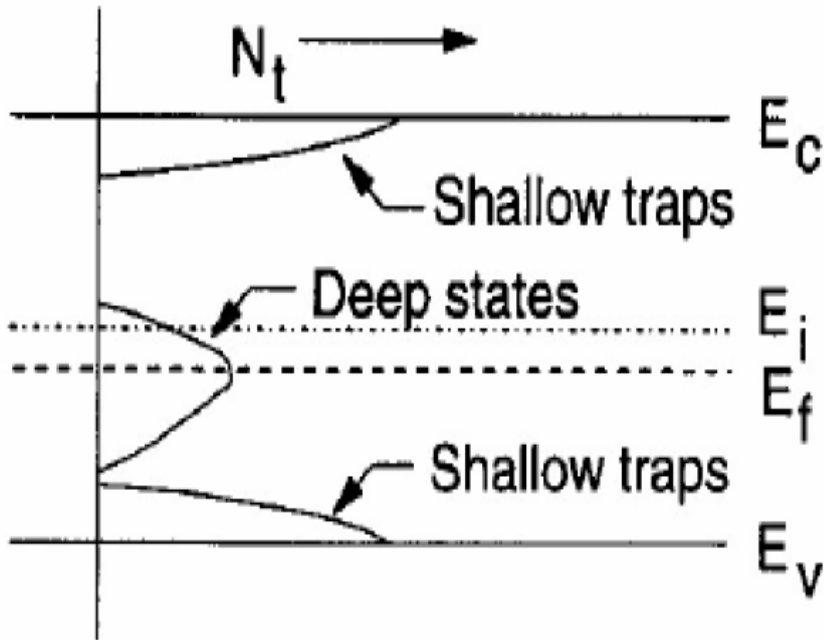
Figure 3.3 extracted trap density of inward flexibility test
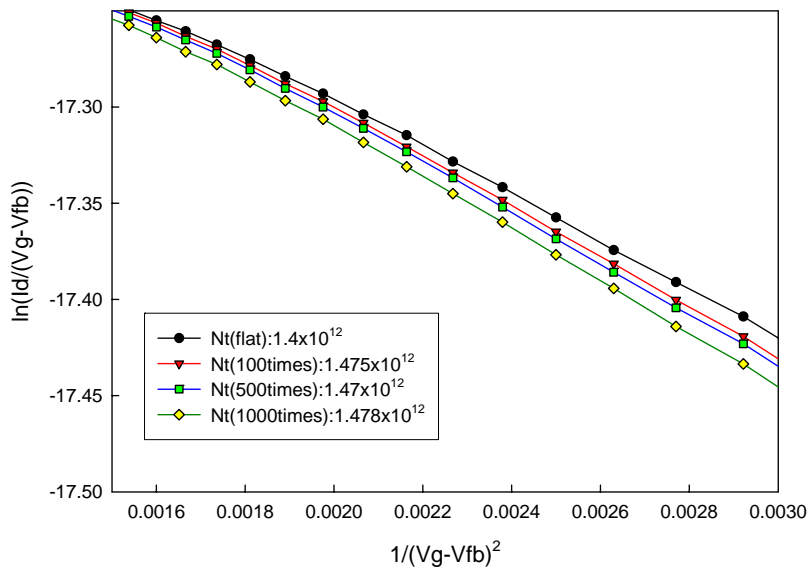
Figure 3.4 extracted trap density of outward flexibility test
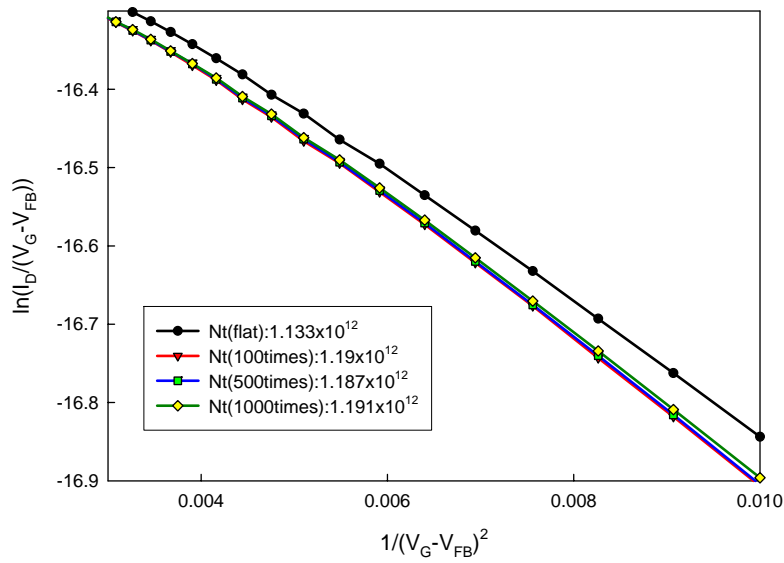
Figure 3.5: drawing of drain current virus gate voltage under different
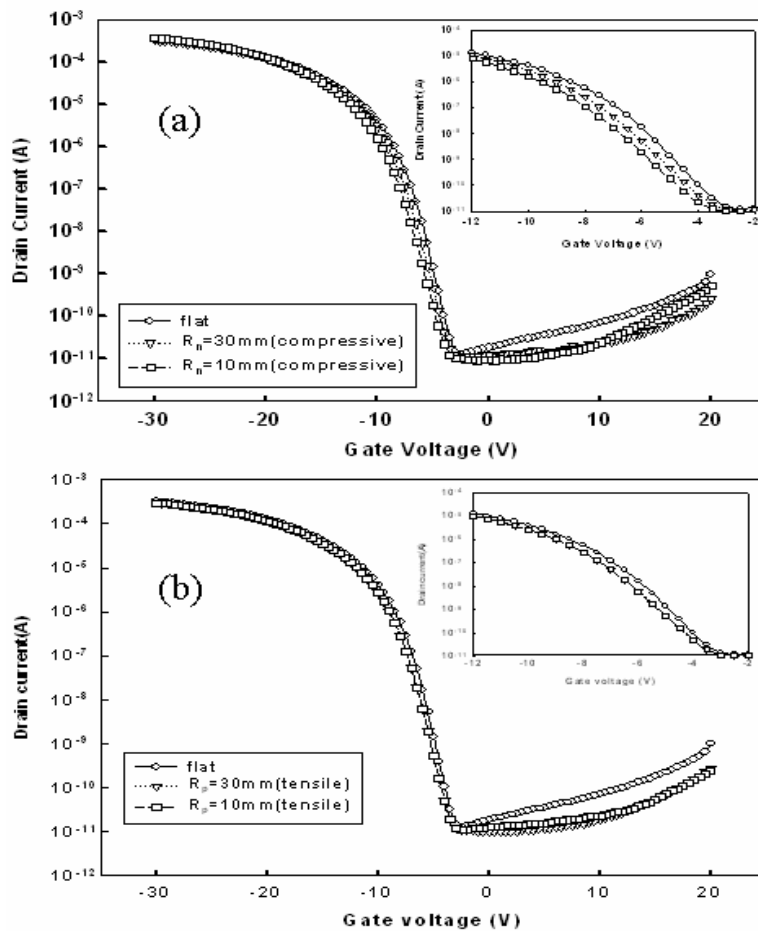
status

Figure 3.6: drawing of threshold voltage virus strain percentage under
bending status.
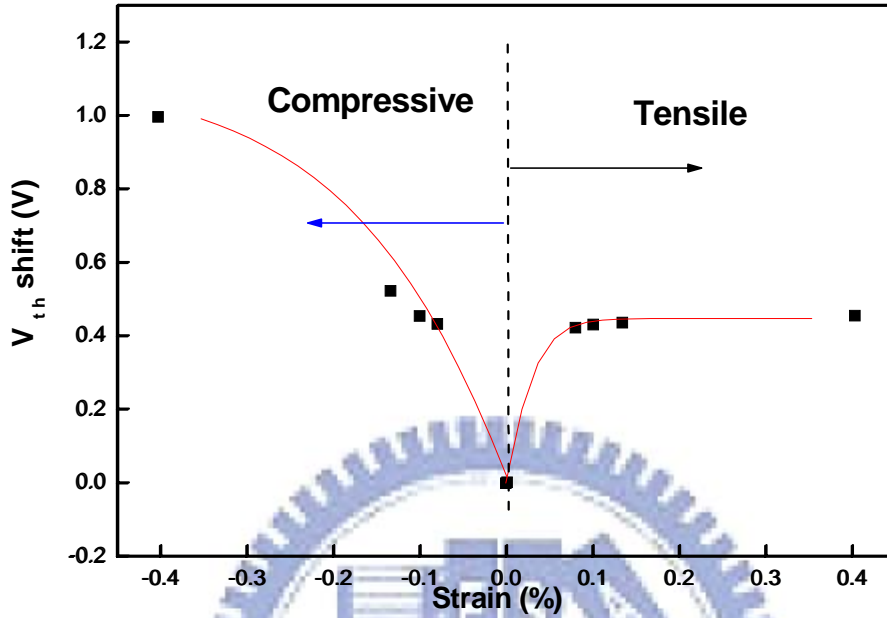
Figure 3.7: drawing of normalized mobility virus strain percentage under
bending status.
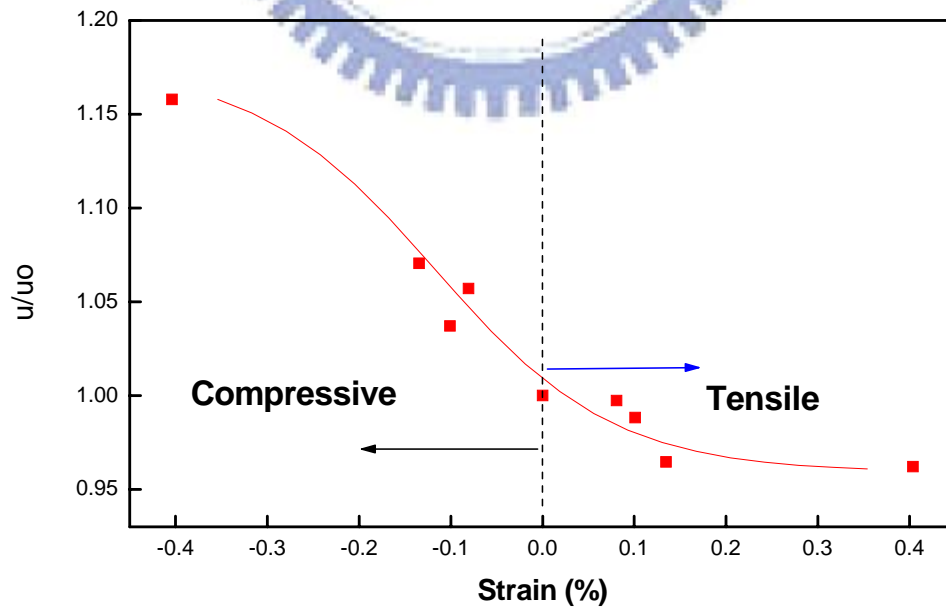
Figure 3.8: activation energy extracted under different status.
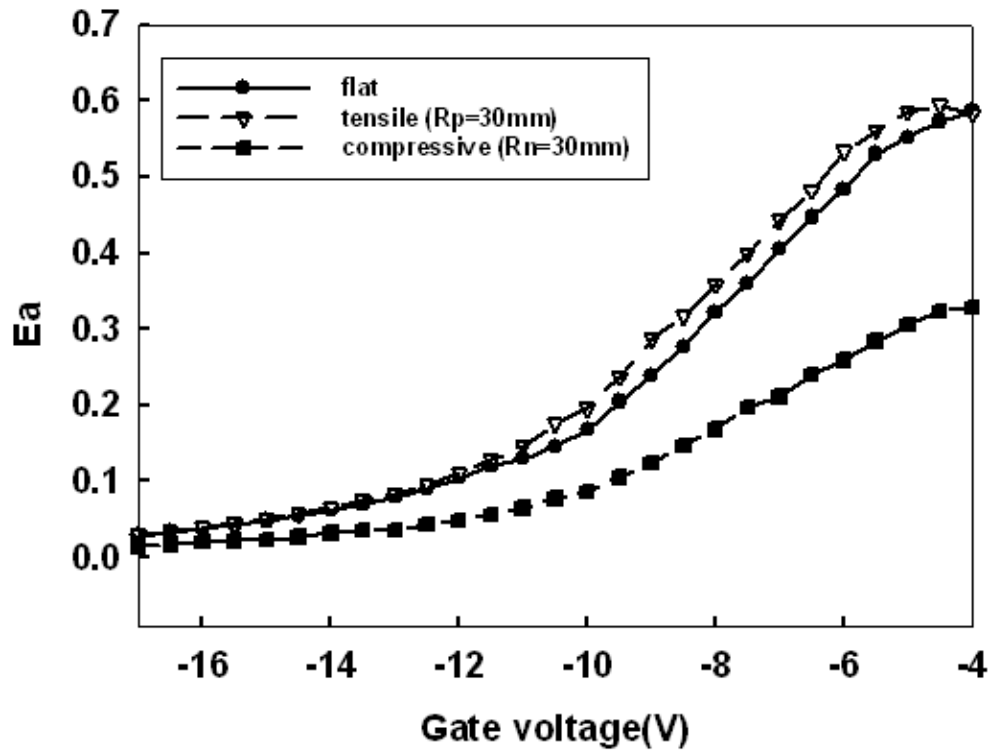
Figure 3.9 (a): extracted trap density under tensile bending status.

127-5 tensile trap density
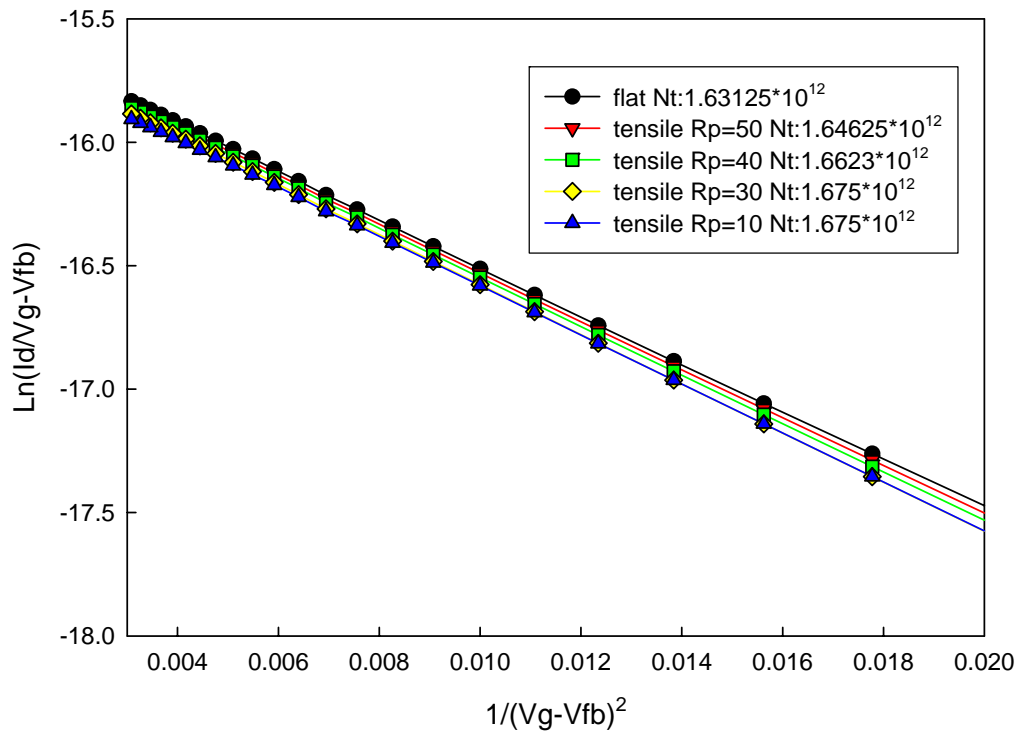
Figure 3.9 (b): extracted trap density under compressive bending status.

127-5 compressive trap density
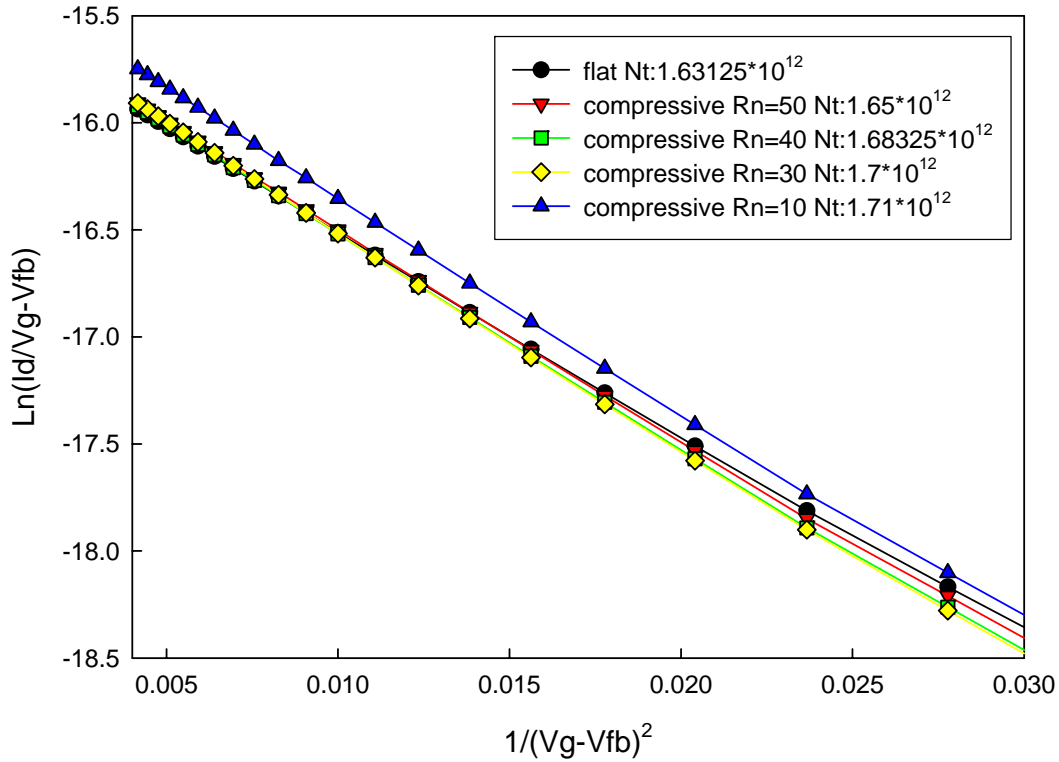
Figure3.10 (a): illustration of extracted parasitical resistance in flat status.
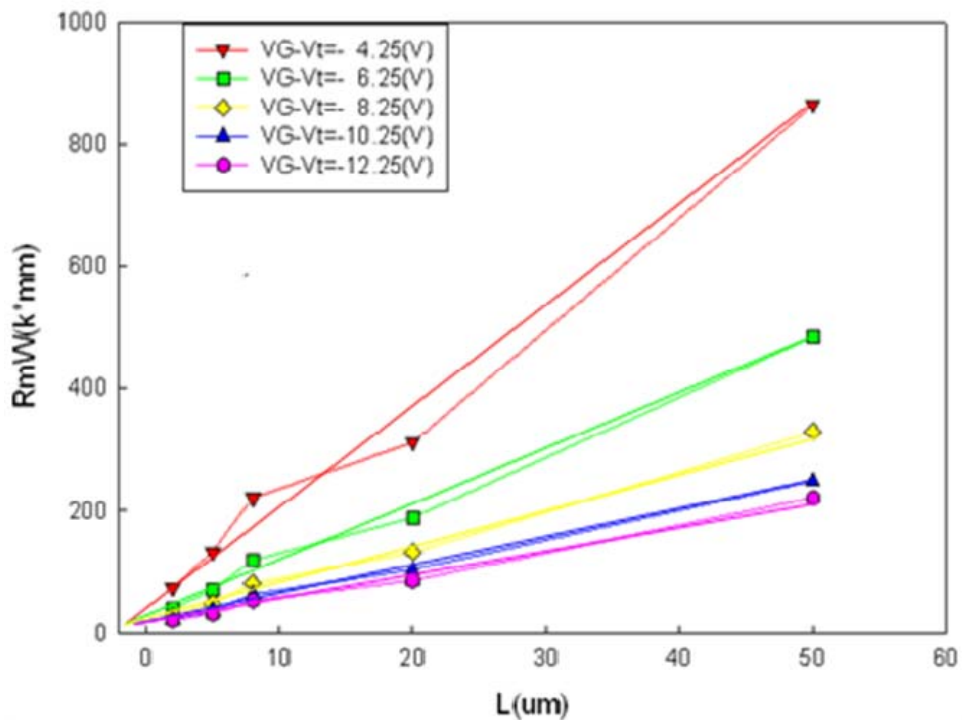
Figure3.10 (b): illustration of extracted parasitical resistance by original

in flat status.
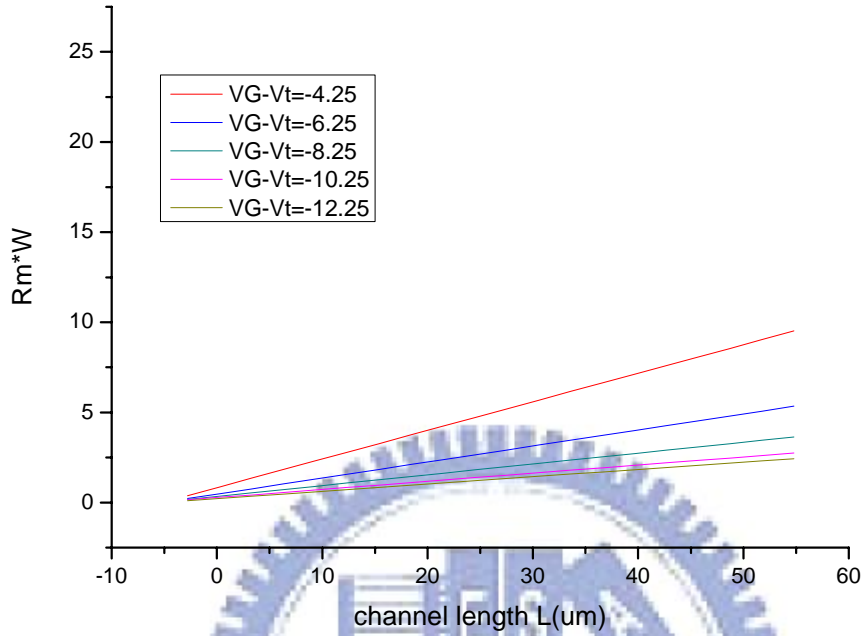
Figure3.11: illustration of parasitical resistance under different strain
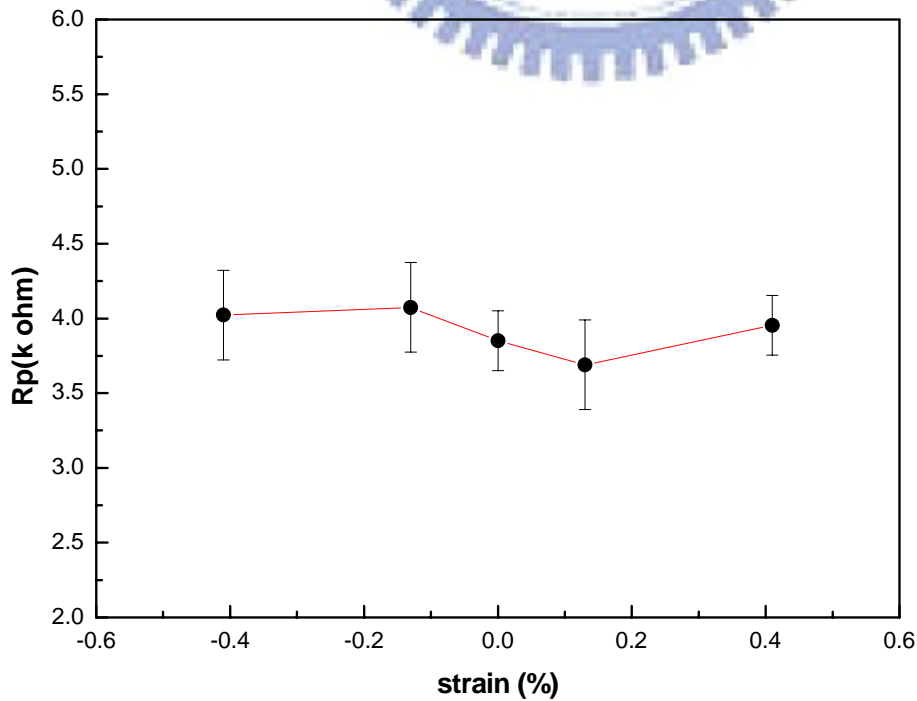
percentage.

Figure 3.12: the mobility excluding parasitical resistance change virus
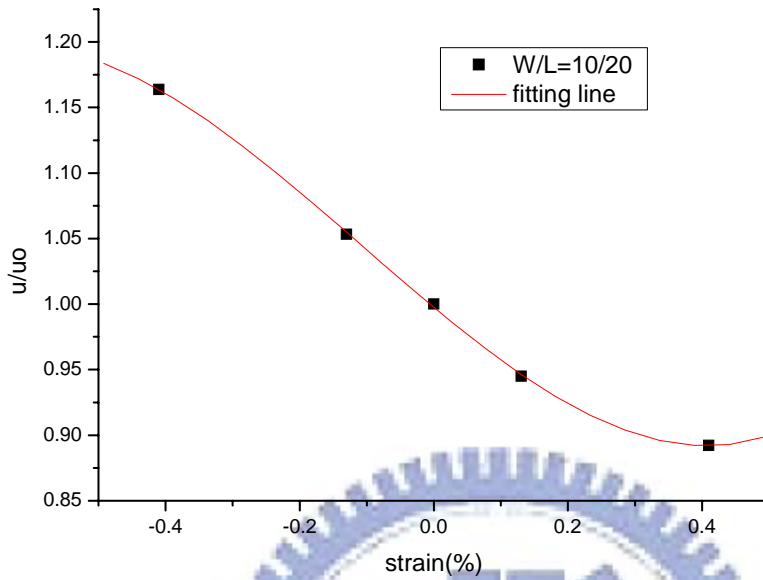
strain percentage.

Figure 3.13: different length/width the mobility excluding parasitical

resistance change virus strain percentage.
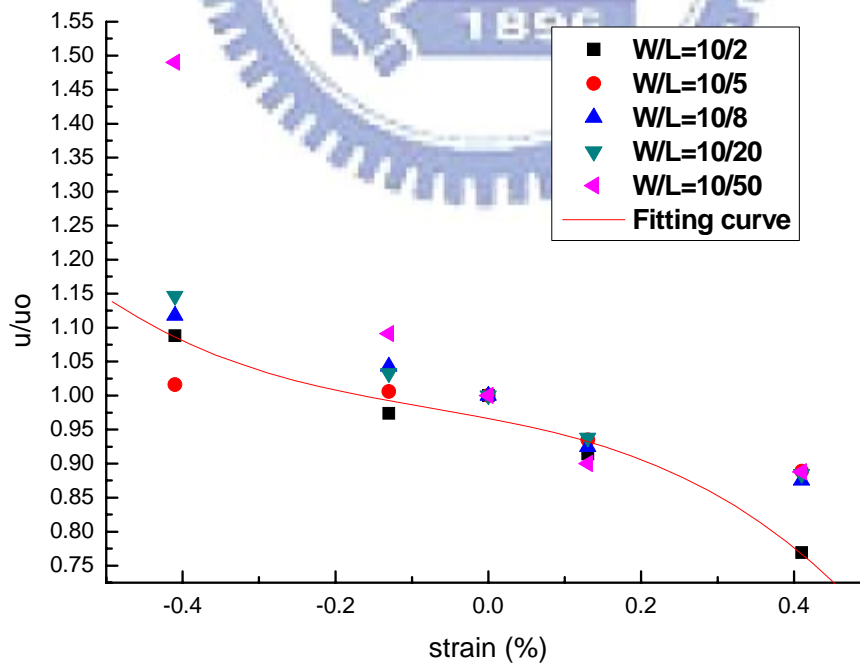
Figure 3.14: the relationship graph with surface orientation and bending

status
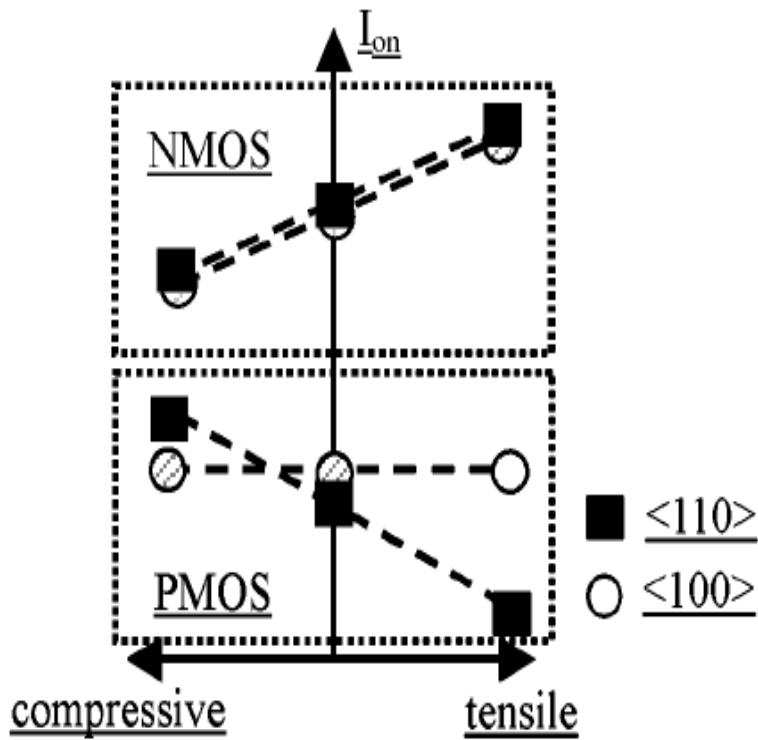
Figure 3.15 (a): XRD graph in positive surface (b): negative surface
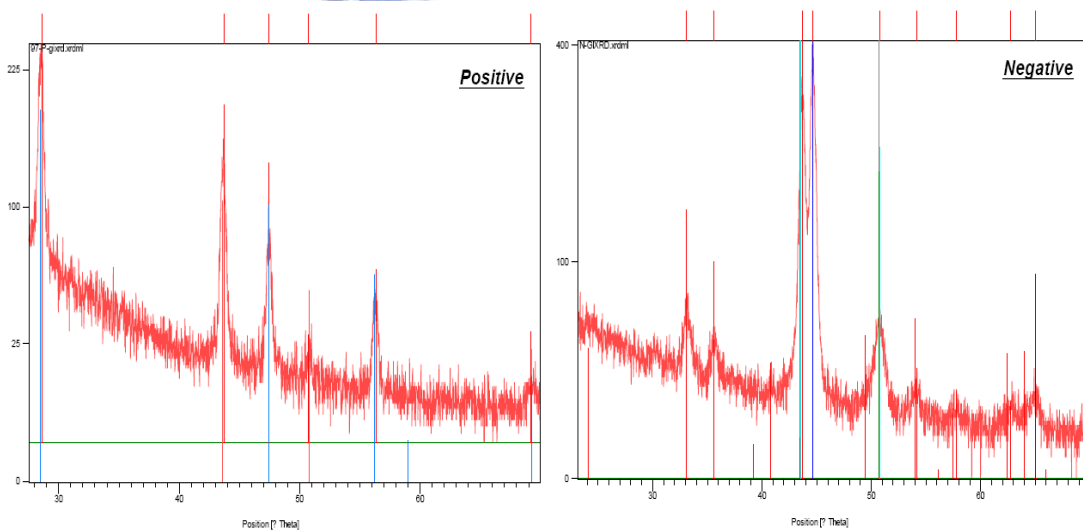
Figure 3.16 (a): XRD analysis in positive facade
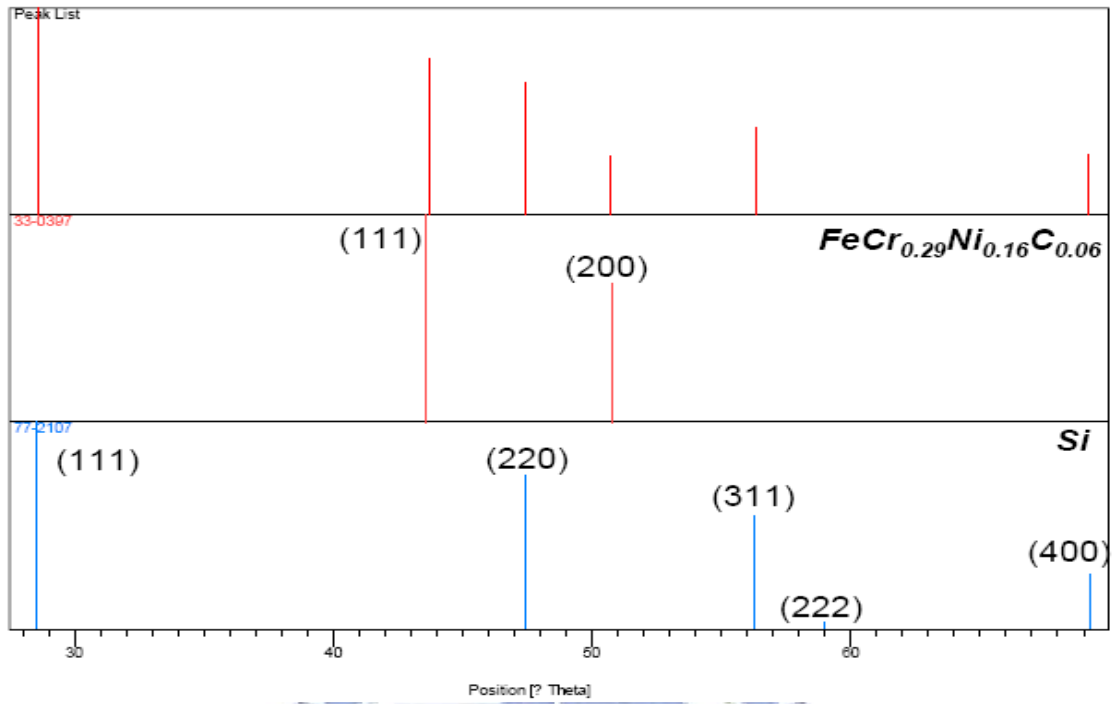
Figure 3.16 (b): XRD analysis in negative facade
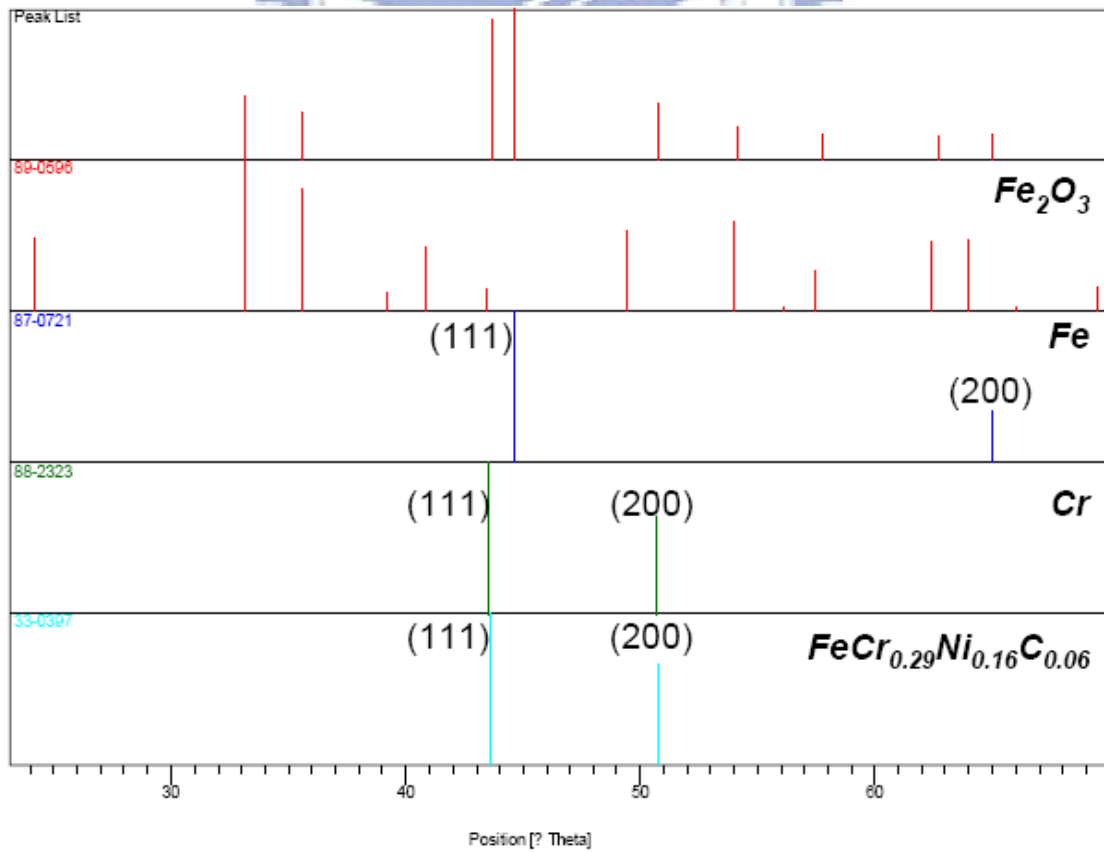
Figure3.17: the six valleys in silicon conduction band under different

status
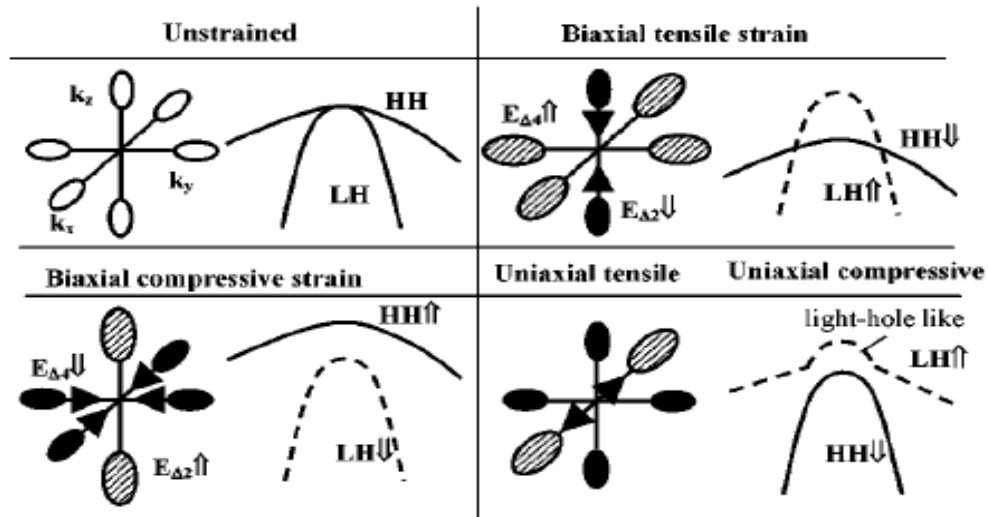
Figure 3.18: the illustration of the six valleys in silicon conduction band

change and different surface orientation.
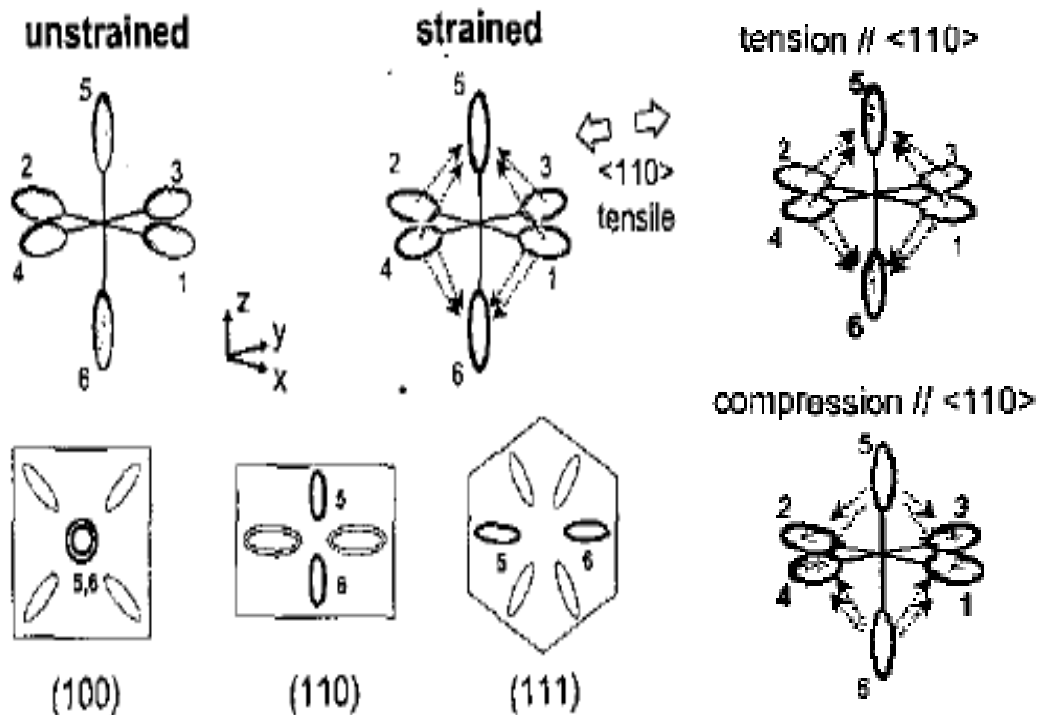
Figure 3.19: light hole and heavy hole variation under different surface orientation.
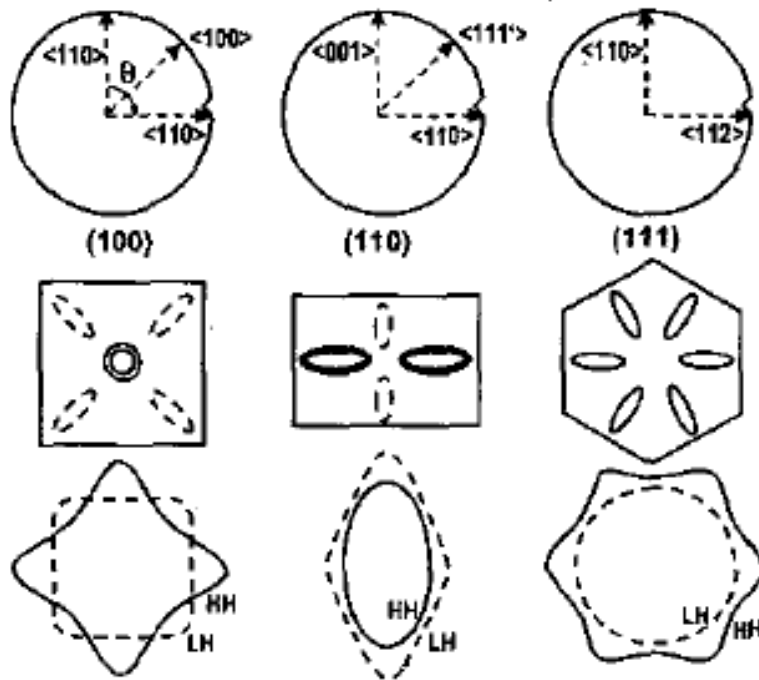
Figure 3.20: the I-V curve of DC bias stress in flat status
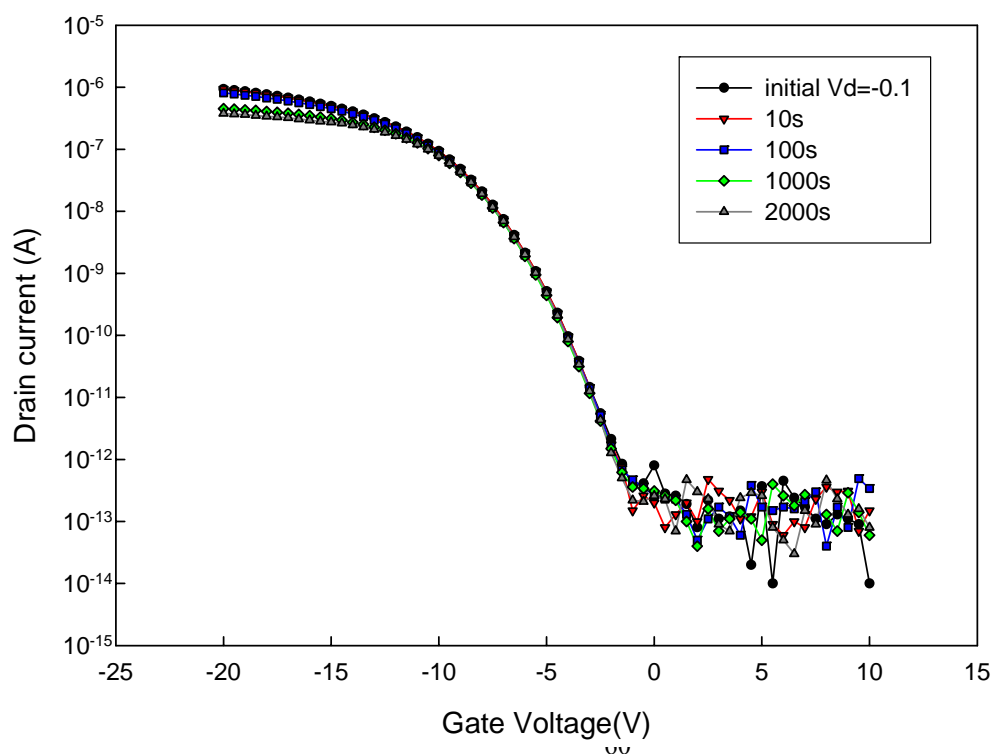
Figure3.21 (a): the I-V curve of DC bias stress in compressive status
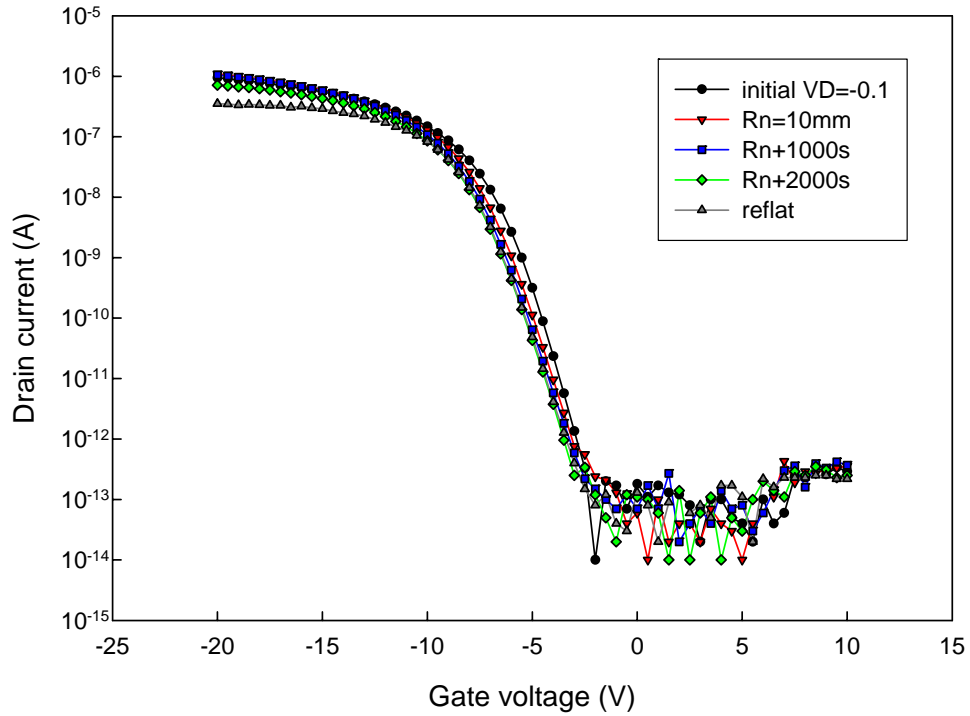
10/30 compressive DC bias stress

Figure3.21 (b): the I-V curve of DC bias stress in tensile status
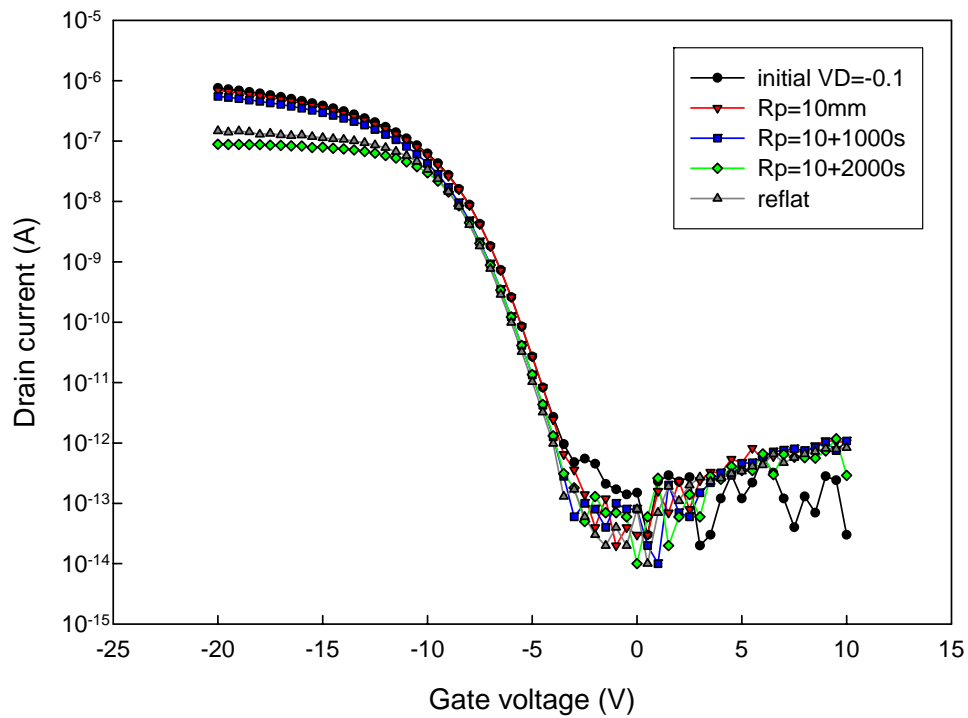10/30 tensile DC bias stress

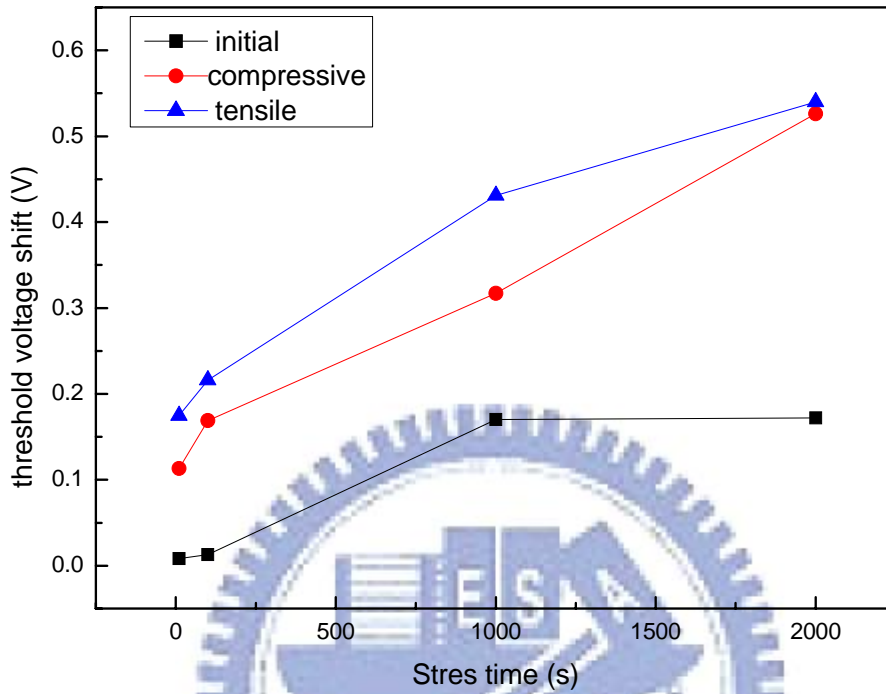Figure3.22: the threshold voltage shift virus stress time under different

bending status (Rp=Rn=10mm)

Figure 3.23: the mobility change before and after DC stress variation
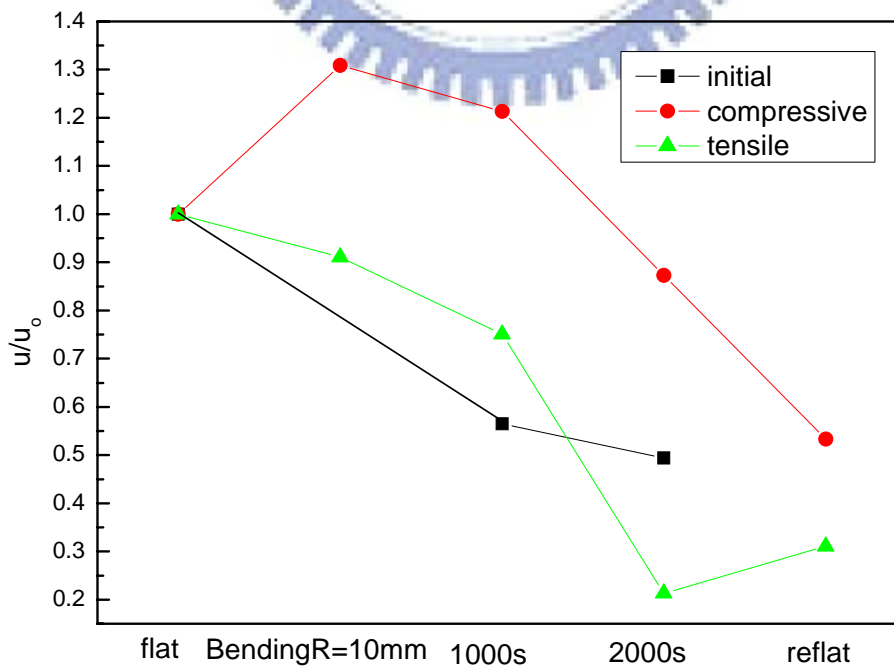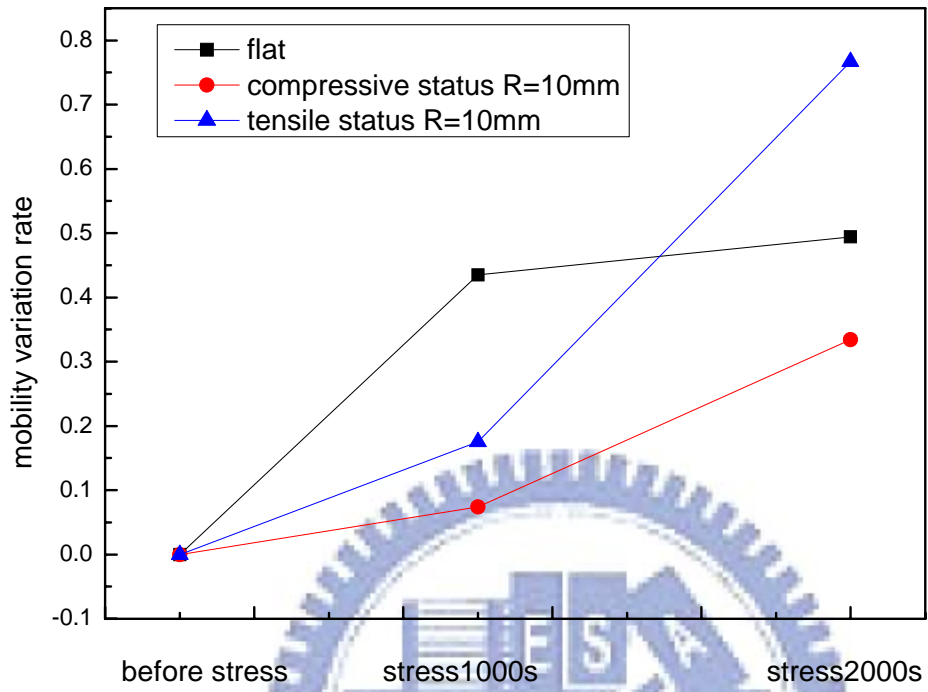
under different bending status (Rp=Rn=10mm)

Figure3.24: the mobility variation rate under different bending status

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發表論文: 1.I-Hsuan Peng, Po-Tsun Liu, **Szu-Wei Chen**, Tai-Bor Wu

「Mechanically strained low-temperature polycrystalline silicon thin film

transistor on metal foil substrate 」EMRS, 2008,5,27

2. I-Hsuan Peng, Po-Tsun Liu, **Szu-Wei Chen**, Tai-Bor Wu

「Mechanically Reliability of low-temperature polycrystalline silicon

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