國立交通大學

光電工程研究所

碩士論文

含自組裝矽量子點之奈米孔洞氧化矽複合材料閘極之非揮發記憶體

Nonvolatile memory with gate of self-assembled nanostructures of silicon quantum-dots in mesoporos silica

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摘要

在本篇論文中,利用將零維度矽奈米微晶埋藏於自我組裝奈米孔洞氧化矽模版中,展示了新型態的人工製造類鐵電材料,我們將量測到的極化場歸因於奈米晶粒與二氧化矽模板間非對稱介面鍵結感應電子極矩所產生。我們也將此種材料替換金-氧-半場效電晶體的閘極介電層,展示了高度的潛力應用在矽基非揮發鐵電記憶體。

Nonvolatile memory with gate of self-assembled nanostructures of silicon quantum-dots in mesoporos silica

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Abstract

In this thesis, a new class of artificially engineered ferroelectric-like materials synthesized by embedding three-dimensional arrays of Si nanocrystals in mesoporous silica matrix was reported. We attribute the measured polarization switching to polar layers lying at the interfaces between one-side bonded Si nanocrystals and mesoporous silica matrix. A metal-oxide-semiconductor field-effect transistor with the ferroelectric-like material in place of the gate dielectrics was fabricated to demonstrate its high potential for the silicon-based nonvolatile random-access memories.

誌謝

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Chapter 1 Introduction

1.1 The general background of nonvolatile memory

With development of the information industry and provision of more applications of the information media, various kinds of memory have increasingly become important. Among them, the electronic memory is undoubtedly the most important one. The electronic memories may be functionally categorized into two types. (**Fig. 1.1**) One is random access memory (RAM), which possesses an access time down to below 100 ns. However, the RAM does not provide a permanent memory function. The other one is non-volatile memory, such as flash memory, which has a permanent memory function, but has an access time greater than 1 ms.

Floating-gate memory (**Fig**. **1.2**) can be the most commonly used non-volatile memory and has been utilized in a variety of electronic products. However, as the semiconductor process is developed down to below 70 nanometer, the scalability of the floating-gate memory has met a challenge. It is because that the floating-gate memory can not has superior charging capability and high memory performance any more in case that the dimension of the floating-gate memory is manufactured down to the nano-level.

To solve the above-mentioned problems, a nano quantum dot memory(**Fig. 1.3**) [1]device has been suggested, in which the nano quantum dots existing in a thin film, instead of the poly-silicon floating gate, is used as the floating gate for charge storage. Although many quantum dot memories are made from silicon-based materials and are compatible with the semiconductor processes, the processes of nano quantum dot memory devices are not easy to be controlled, which limits their developments. Furthermore, since the quantum dot memory device is operated in a similar manner with the conventional floating-gate memory, i.e. operated by moving charges, it has

the disadvantages of relatively large power consumption, long access time and reduced lifetime.

For solving this problem, a novel ferroelectric memory has been set forth. Since the ferroelectric memory is not involved with any charge motion and collision during the access process, it has a relatively fast access time (approximately 10^{-9} sec), a prolonged retention time and a relatively low power consumption, compared with that of the conventional floating-gate memory.(**Table 1.1**) Further, the ferroelectric memory can have theoretically limitless operation cycles. In spite of the above-mentioned advantages, the ferroelectric memory has encountered with the process compatibility problem for a long time.

1.2 Motivation

The spontaneous polarization of a ferroelectric material is mainly due to dipoles that can switch directions under the influence of an electric field. The nonvanishing electrical polarization is a result of the non-centrosymmetric crystal structure. Bulk silicon does not possess ferroelectric properties because it is of the diamond structure with centrosymmetry. No net dipolar polarization is produced by the displacement of lattice ions in the crystal. Therefore, tremendous efforts have been made to integrate non-silicon-based ferroelectric films, such as lead zirconate titanate (PZT)[2][3], with the mature silicon-based memory technology to realize FeRAM. However, the interface reactions between PZT and the Si substrate, which results in mobile ions and low data retention time[4][5][6] make it difficult to obtain a good ferroelectric/Si interface. Contamination of the Si integrated circuit (IC) fabrication line by metal ions in a non-Si based ferroelectric is also a major concern.[2][7] The development of silicon-based ferroelectric-like thin films will realize an IC-compatible FeRAM technology.

At the nanometer scale, the ratio of the numbers of atoms on the surface and in the bulk of a material increases rapidly. Interfacial properties of a nanostructured material could, therefore, enable new functional devices.[8][9] In this regard, self-assembled mesoporous silica (MS)[10][11] is attractive for its extremely large internal surface area and controllable nanoporous structure. There is provided a silicon-based ferroelectric memory material comprising a mesoporous silica (MS) with a plurality of nanopores thereon, and the arrays of nanocrystalline (nc) silicon (or germanium) quantum dots attached to the inner walls of the nanopores of the mesoporous silica by the surface bonds contributing to ferroelectricity.

In this thesis, we report that interface of *nc*-Si/MS exhibits a novel ferroelectric-like polarization switching effect which could potentially be developed into a fully silicon-based FeRAM technology.
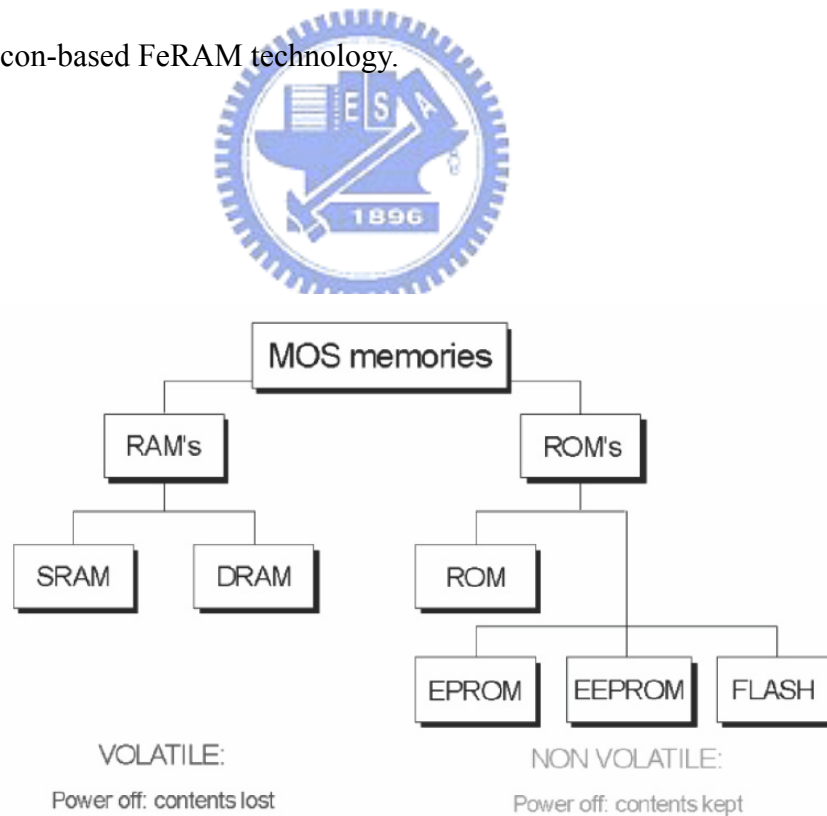
Fig 1.1 MOS memory tree
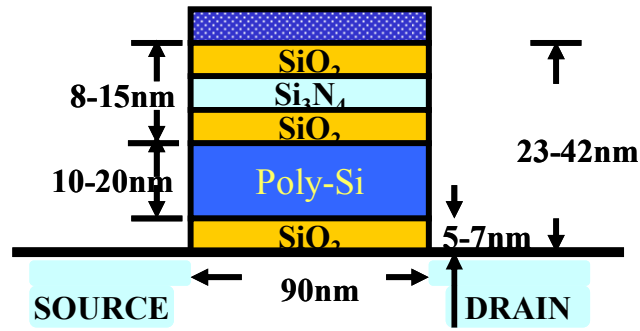
Fig. 1.2 Conventional flash memory
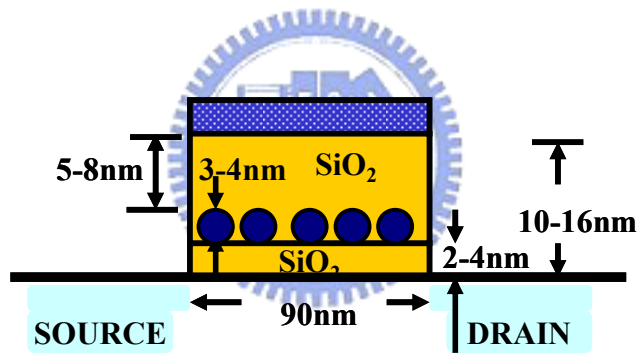
Fig. 1.3 Nanocrystal memory

Memory type	DRAM	SRAM	Flash-NOR	Flash-NAND	FRAM	MRAM	Phase change memory
Cell size factor (F^2)	6~12	90~150	**8~10**	**4**	18	10~20	5~8
Largest array built (Mb)			**256**	**2Gb**	64	1	4
Volatile/Non-volatile	Volatile	Volatile	NV	NV	NV	NV	NV
Endurance write/read	∞ / ∞	∞ / ∞	$10^6 / \infty$	$10^6 / \infty$	$10^{12} / 10^{12}$	$10^{14} / \infty$	$10^{12} / \infty$
Read	Destructive	Partially-destructive	**Non-destructive**	**Non-destructive**	Destructive	Non-destructive	Non-destructive
Read/Program voltage (V)	~1	~1	2/10	2/18	1.5/1.5	3.3/3.3	**0.4/1**
Program/Erase/Read speed, ns	50/50/8	**8/8/8**	1us/1-100ms (block)/60ns	1ms/1-100ms/60 ns	80/80/80	30/30/30	50/50/50
Direct over-write	Yes	Yes	**No**	**No**	Yes	Yes	Yes
Bit/byte Write/Erase	Yes	Yes	Yes	Block erase	Yes	Yes	Yes
Read dynamic range (margin)	100-200mV	100-200mV	**Delta current**	**Delta current**	100-200mV	20-40% R	10X-100XR
Programming energy	*Medium*	*Medium*	*High*	*Low*	*Medium*	*Medium*	Low
Transistors	Low performance	High performance	High voltage	High voltage	Low performance	High performance	High performance
CMOS logic compatibility	Bad	Good	Ok, but Hi V needed	Ok, but Hi V needed	Ok, but Hi V needed		Good
New materials	Yes	No	No	No	Yes	Yes	Yes
Scalability limit	Capacitor	6T (4T possible)	Tunnel oxide/HV	Tunnel oxide/HV	Polarizable capacitor	Current density	Lithography
Multi-bit storage	No	No	**Yes**	**Yes**	No	No	No
3D potential	No	No	Possible	Possible	?	?	No
SER susceptibility	Yes	Yes	No	No	Yes	No	No
Relative cost per bit	Low	High	Medium	Medium	High	?	Low
Extra mask needed for embedded memory			6-8		2	4	3-4
In production	Yes	yes	Yes	Yes	Yes	2004	N/A

Table. 1.1 Performance comparison between volatile memory (DRAM & SRAM) and nonvolatile memory (Flash, FRAM, and PCM) devices. Flash memory exhibits the best performance except the disadvantages of high programming voltage and slow program/erase speed.

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Chapter 2 Basic Theory about ferroelectric memory

2.1 Ferroelectric theory

2.1.1 Ferroelectricity

Ferroelectricity only occurs in some noncentrosymmetric crystal structures. Ferroelectric crystals exhibit electric dipole moments even in the absence of an external electric field. This spontaneous polarization is caused by the two thermodynamically stable positions of constituent ions in the crystal and its direction can be changed by applying an external field. In the ferroelectric state, the center of the positive charge of the crystal does not coincide with the center of negative charge, as shown in the **Fig. 2-1.**

Many perovskite type (ABO_3) materials are the commonly used ferroelectrics. The crystal structure of the perovskite such as $BaTiO_3$ (BTO) is shown in **Fig. 2-2.** The Ti^{+4} ion is displaced at the center of the cubic, while the Ba^{+2} located at the corner of the cube, and the O^{-2} is at the face center.

The obvious feature of ferroelectric materials is the response of the polarization (P) to external electric field (E). The plot of polarization versus electric field ($P–E$) for the ferroelectric state is referred to the hysteresis loop, as illustrated in **Fig.2-3**. However, the polarization can not increase without limit, it will reach a saturation polarization Ps,which corresponds to the maximum degree of domain orientation possible for that material. The coercive field E_c is the reverse field to remove the polarization to zero and further increases in the reverse field lead to saturation of P in the opposite direction. At $E= 0$, some of the polarization will be lost, but the remnant polarization Pr is retained. The ferroelectric materials would undergo a crystallographic phase transformation from higher temperature paraelectric phase into a lower temperature

ferroelectric phase. The temperature of the cubic to tetragonal or orthorhombic to rhombohedral transformation is known as the Curie point or Curie temperature, T_c. Ferroelectric materials that possess a low Curie temperatures close to the range of device operation are undesirable in reliability issues than those with high Curie temperatures, because ferroelectric materials with high T_c are less susceptible to P_r and E_c degradation. Since the response time of the ferroelectric dipole moment is the order of nanoseconds, non-volatile random access memory called 1T-1C type FeRAM (ferroelectric random access memory) can be realized using ferroelectric capacitors, in which two states of "0" and "1" in the binary logic are represented by the direction of the spontaneous polarization. As shown in **Fig2-4**[1].
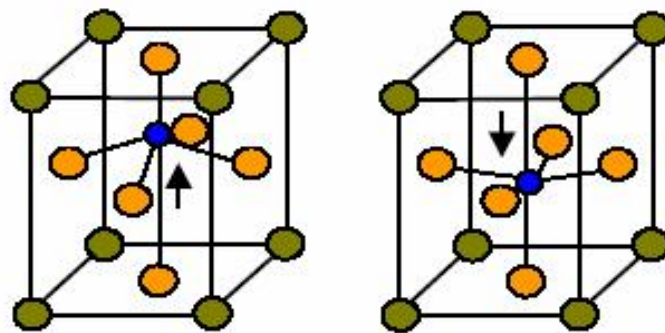
Fig. 2.1 The origin of ferroelectricity of perovskite materials: Dipole created by the relative displacement of the sublattices of the cations and oxygen.

● Ba (A)
• Ti (B)
○ O
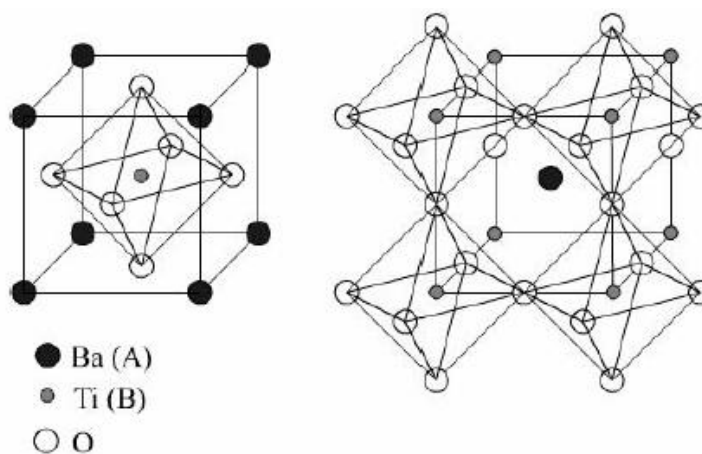
Fig. 2.2 The perovskite structure of $BaTiO_3$.
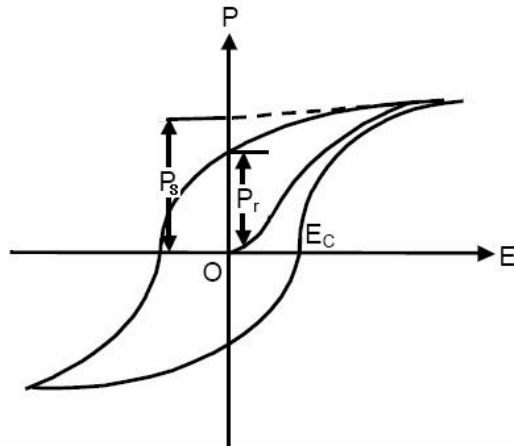
Fig. 2.3 The typical hysteresis loop (polarization to electric field) of ferroelectric
materials.
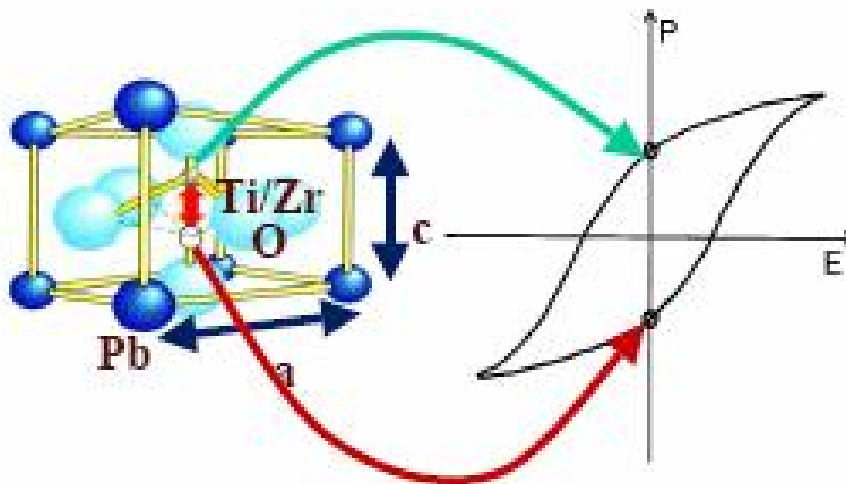
Fig. 2.4 The two stable polarization state of ferroelectric materials like PZT can

be defined as "0" and "1" for 1T-1C type FeRAM.

2.1.2 Ferroelectric Field Effect Transistors

For the current progress of emerging nonvolatile memories such as CRAM(chalcogenide random access memory), FeRAM and MRAM(magnetic random access memory), FeRAM is the first one in production into the electronic market. The commercialized 1T-1C FeRAM needs the ferroelectric material of the capacitor to have larger remnant polarization, which is required to produce devices with higher density. However, to maintain the minimum switching charge in the scaling ferroelectric capacitoris still the most serious problem for this type of FeRAM to survive in the future. Besides, the disadvantage of its destructive read out is undesirable for unlimited read/write cycles and ultra fast operation speed (< 20 ns). The other type FeRAM consists of a ferroelectric gate dielectric in the transistor, therefore, no additional capacitor layer is needed **(Fig 2-5 (a))**. The basic unit of this type FeRAM is only one transistor, which is much smaller than the capacitor type FeRAM. In this metal/ferroelectric/semiconductor field effect transistor (MFS-FET), the surface potential is dependent on the remnant polarization of ferroelectrics. The data of this device are read by sensing the variation of surface conductivity of the silicon rather than the switching polarization state, which is seen in the1T-1C type FeRAM. The 1-T FeRAM has the following advantages compared to the 1T-1C type FeRAM:

1. Nondestructive readout

2. Lower power consumption

3. Scaling rule is more adaptive and very high integration density

4. Simpler integration process and lower cost

2.1.3 Type of 1-T type FeRAM

The first concept of MFS-FET was proposed from Bell Lab in 1957[2]. However, no such devices have been commercialized, because it is very difficult to obtain the excellent ferroelectric/semiconductor interface. As ferroelectric materials like PZT , SBT were directly deposited on silicon substrates, the chemical reaction and inter-diffusion of Pb, Bi, and Si led to very high density of surface traps in the ferroelectric/Si interface .The charge trapping and charge injection effect would degrade the data retention performance of MFS-FET seriously.

In order to solve the problems of poor interface between ferroelectric and silicon substrate, many solutions have been proposed so far:

1. MFIS FET (Fig 2-5 (b)):

The insulator buffer layer would be inserted between ferroelectric and Si to form a metal/ ferroelectric/insulator/semiconductor (MFIS) gate structure. It is believed that an insulator layer can prevent the problems caused by ferroelectric-semiconductor interface However, this structure causes series capacitance effect so it is difficult to apply sufficient voltage on the ferroelectric thin film to switch its saturation polarization state because part of the gate bias drops on the insulator layer.

2. MFMIS FET (Fig 2-5 (c)):

Another structure of ferroelectric-gate FETs is the metal-ferroelectric-metal-insulator-semiconductor (MFMIS) structure. This concept was first proposed by Katoh/NEC in 1996[3], where metal was additionally inserted between the ferroelectric and insulator layers as a floating gate. In contrast to MFS- and MFIS-FET, the ferroelectric MFM capacitor size and MIS capacitor size can be independently designed in MFMIS-FET. It is able to adjust the area ratio of

ferroelectric capacitor and insulator capacitor in order to use the saturation polarization of the ferroelectric film effectively (i.e., make the ferroelectric capacitor area small). However, the additional lithography process makes the integration more complicated, and the larger insulator capacitor area violates the semiconductor scaling-down rule.

3. All Epitaxial Perovskite FET [4][5] **(Fig 2-6)**:

The use of a perovskite semiconductive oxide such as $La_{0.7}Ca_{0.3}MnO_3$(LCMO), $SrRuO_3$ (SRO) rather than Si ,which are more compatible with common ferroelectrics. To reduce the trap density under the gate, use of an epitaxial heterostructure is inevitable. Due to the excellent interface condition, the retention time of this type FeRAM is largely improved. However, the material complexity and the epitaxial process largely raise the fabrication cost.
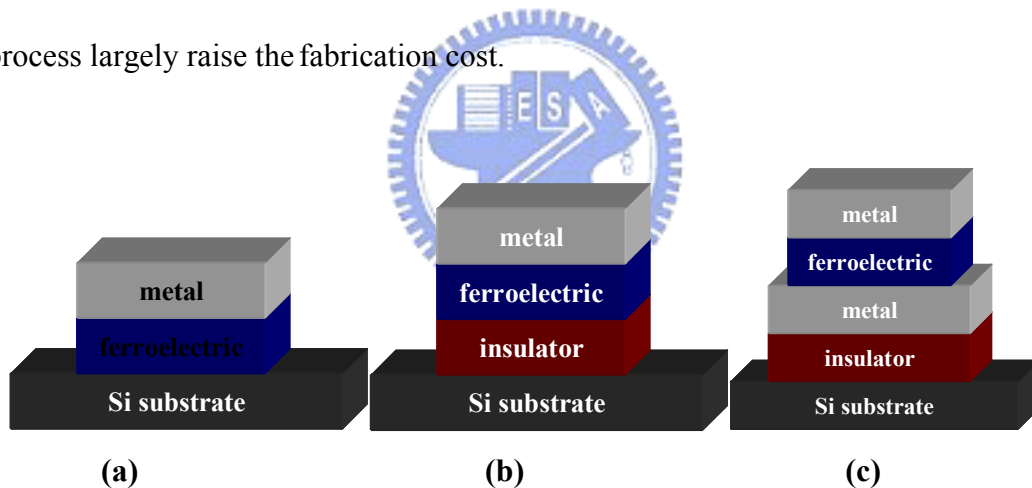
Fig. 2.5 Type of 1T-FeRAM: (a) MFS-FET (b) MFIS-FET (c) MFMIS-FET
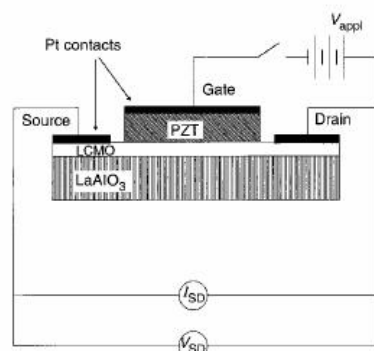
Fig. 2.6 Schematic diagram of an all-perovskite ferroelectric FET and measurement circuit.

2.2 Ferroelectric memory mesurement

The basic operation mechanism of ferroelectric-gate-controlled devices, such as the metal-ferroelectric-insulator-silicon (MFIS) or metal-ferroelectric-metal-oxide-silicon (MFMIS) field-effect transistors (FETs), is depicted in **Fig. 2.7**.[6][7] When the ferroelectric material is poled towards the gate electrode, positive charges are induced at the channel.   The threshold voltage of the transistor is very large.   The transistor is programmed to the "off" state.   On the other hand, negative charges are induced at the channel when the ferroelectric material is poled toward the channel.   The threshold voltage of the transistor is low and the device is programmed to the "on" state.   During read operation, the sense amplifier detects the state of the MFMISFET.   If there is a large drain current, it is on state; if there is a small drain current, it is off state.

In the previous work, we reported that interface of nc-Si/MS exhibits a novel ferroelectric-like polarization switching effect. The existence of electrical polarization in the nc-Si embedded MS structures can be revealed with polarization-electric field (P-E) measurements (See **Fig. 2.8**).   The remnant polarization (P_r) of Si-O nanostructured layers in the metal-insulator-metal (MIM) configuration were found to be 3.0 $\mu C/cm^2$ and is much larger than the reported values for iron-passivated porous silicon.[8] The memory window of devices is equal to $2P_r/C_{FE}$, where P_r and C_{FE} are

the remnant polarization and capacitance of ferroelectric capacitor, respectively. According to the theoretical work by Miller and McWhorter[9], an electrical polarization higher than 0.1 $\mu C/cm^2$ is sufficient to switch the Si surface potential from depletion to inversion. Ferroelectricity-induced capacitance-voltage (C-V) memory window (ΔV) can be determined from the coercive field (E_c) by $\Delta V=2E_c.d$ [10], where d denotes the thickness of ferroelectric films. The coercive field of 700 kV/cm yields C-V hysteresis width of 9 V theoretically for Si-O nanostructured ferroelectrics of 65 nm in thickness, in accordance with measured values of 8 V (See **Fig. 2.9**). It preliminary manifests the feasibility of our materials in memory applications.
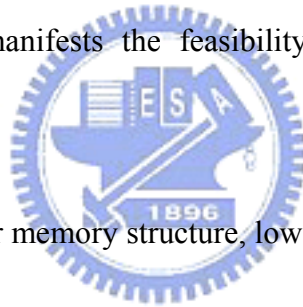
In general, in transistor memory structure, low P_r can ensure positive threshold voltage at the on state and, therefore, low standby currents.[6][7] Moreover, increasing (decreasing) the capacitance of gate insulator capacitors (ferroelectric capacitors) increases voltage drop across ferroelectrics, while reducing the polarization filed decreases the depolarization field.[6][7] Our Si-O nanostructured ferroelectric thin films have smaller polarization (3 $\mu C/cm^2$), a relatively large coercive field (~600 kV/cm), and lower dielectric constant (~4) in comparison with conventional perovskite ferroelectrics. Notably, the leakage current in Si-O nanostructured ferroelectrics was quite low (See **Fig. 2.10**). Therefore, the Si-O

nanostructured ferroelectric material was suitable for one-transistor memory application.

At high V$_{th}$ state **At low V$_{th}$ state**
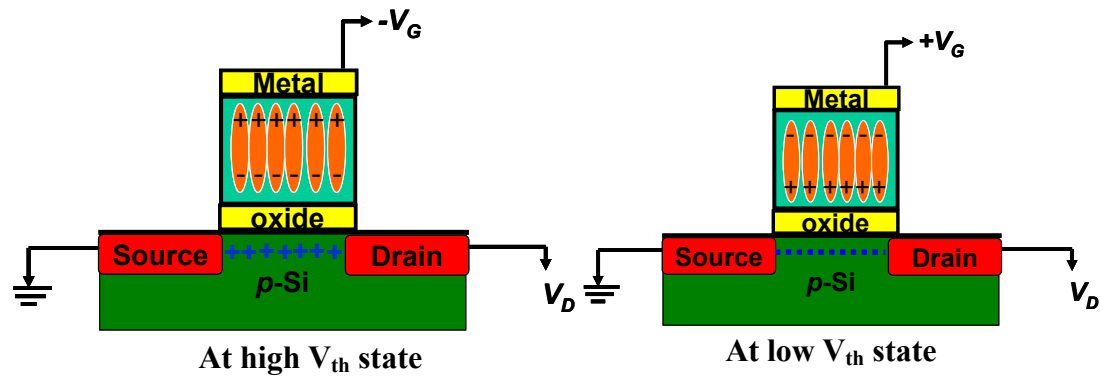
Fig. 2.7 Operation mechanism for MFMISFET (or MFISFET).
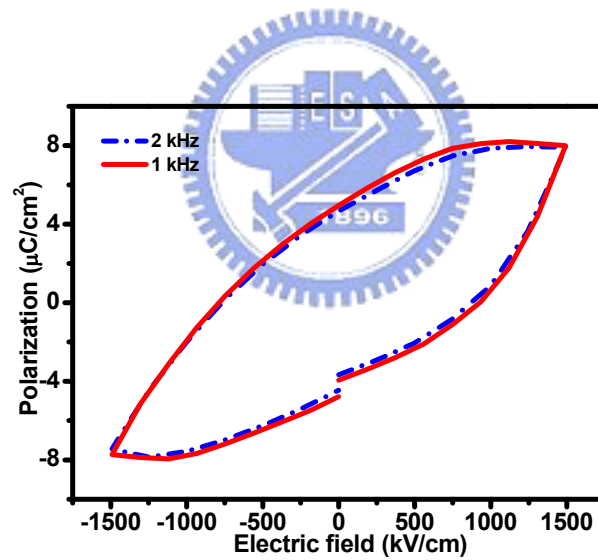
Fig. 2.8 The existence of electrical polarization in the nc-Si embedded MS structures

can be revealed with polarization-electric field
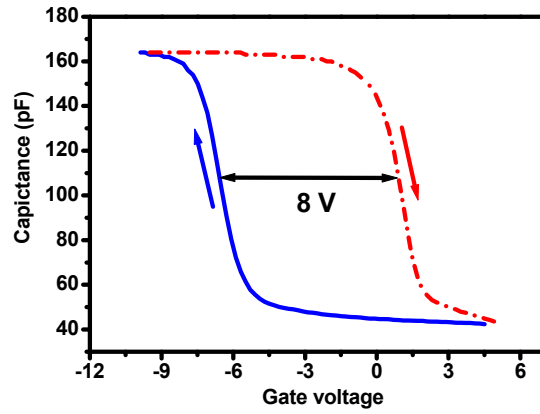
Fig. 2.9 C-V hysteresis feature of Si-O nanostructured ferroelectric metal-oxide-silicon capacitors.
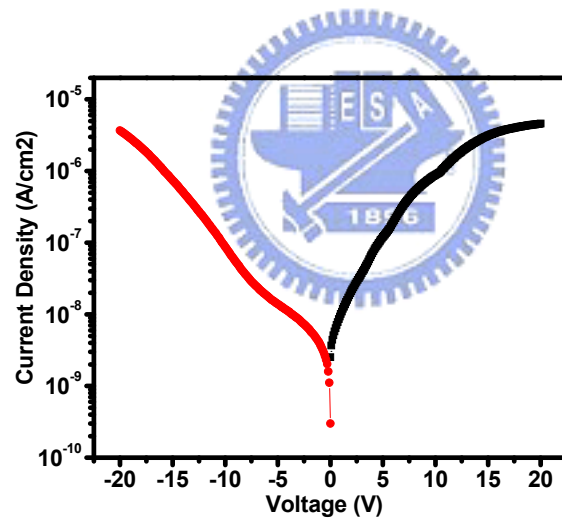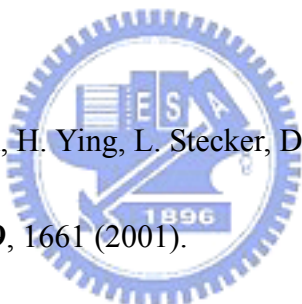
Fig. 2.10 Leakage currents of Si-O nanostructured ferroelectric metal-insulator-metal

capacitors.

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Chapter 3 Experimental Details

3.1 Preparation of mesoporous silica template

The films of mesoporous silica (MS) [1] were deposited on *p*-type silicon substrates by spin-coating.　To prepare the spin-coating solution, we first produced an acid-catalyzed silica sol-gel by refluxing a mixture of tetraethylorthosilicate (TEOS), H_2O, HCl, and ethanol with a molar ratio of 1: 0.008-0.03:3.5-5.0:0.003-0.03:40 (TEOS/P123/H_2O/HCl/Ethanol) at 70°C for 90 minutes. A precursor solution was then made by adding an ethanol solution of triblock copolymer Pluronic P-123 (P123) to the acid-catalyzed silica sol-gel. After the precursor solution was aged at room temperature for 3-6 hours under ambient conditions, it was spin-coated onto the substrates at 3000 rpm for 30 seconds.　The film was dried at 40-60 °C for 4-6 hours, and then baked at 100-120°C for 3 hours. The resulting mesoporous silica film was used as the nanotemplate to synthesize three-dimensional array of Si nanocrystals (nc-Si). The flowchart of mesoporous silica nanotemplate films preparing is shown in **Fig. 3.1**.

MS template preparing flowchart

Precursor sol : P123/H2o/HCl 70℃ , 90 min

↓

Addition of triblock copolymer template

↓

Aging for 3-6 hours, RT

↓

Spin coating on Si Wafer

↓

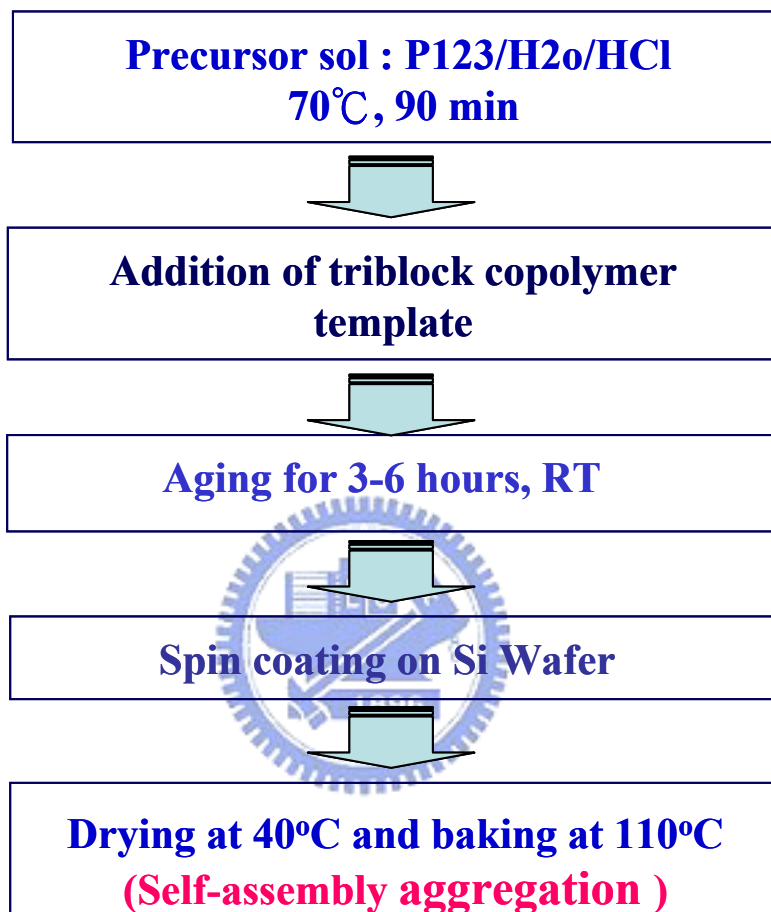| Drying at 40ºC and baking at 110ºC (Self-assembly aggregation) |
|---|

Fig. 3.1 Flowchart of sol-gel procedure for preparing mesoporous silica nanotemplate films.

3.2 Synthesis of Si (or Ge) nanocrystals

nc-Si was grown with a cluster-level inductively coupled plasma chemical vapor deposition **(ICPCVD)**[2][3] system at a base pressure as low as 10^{-6} torr. After loading MS-coated wafers into the chamber, the plasma was formed by exciting a SiH_4+H_2/H_2 mixture with a radio-frequency electrical power of 500 W. The gas mixture was kept below 10 mtorr and the substrate temperature maintained at 250 °C during the entire process. Small size (~4 nm) and large size (~6 nm) nc-Si can be synthesized by using twelve and fifteen cycles of pulsed ICP, with a duty cycle of 1 second and 3 seconds, respectively. The corresponding cross-sectional transmission electron microscopy (TEM) images of pure MS film and the MS films embedded with the small- and large-size nc-Si are presented in **Fig. 3.2** with the detailed growth parameters summarized in **Table 3.1.**

The formation of high quality nc-Si inside the nanopores of the MS with pulsed plasma involves several critical steps. First of all, the pure-H_2 ICP shall be used to remove organic templates of MS matrices lightly to form nucleation sites of Si-OH on the surfaces of nanopores[4] needed for a self-limiting growth reaction (SLR). The SLR is the key for atomic layer deposition.[5] Subsequently, ICP-excited SiH_n species in the form of nanoclusters diffuse into the nanopores of MS, and then absorb on the pore surfaces. The adsorbed species eventually react with the nucleation sites of Si-OH via hydrogen-elimination reaction (HER),[4] as illustrated in **Fig 3.3**. SLR in cooperation with HER precisely governs the conversion of ICP-excited species bound in MS into nc-Si. The number density of nc-Si (or nc-Ge) grown by pulsed plasma can be as high as $2.5\times10^{18}cm^{-3}$. The resulting number density is about 5-10 times higher than that grown by steady-state plasma, where only HER is involved during the growth of nc-Si.

The organic contents of MS can be removed *in situ* by calcinatiion with H_2 plasma at a flow rate of 200 sccm for 10 minutes. For device applications, a 15-nm thick SiO_2 film[2] was deposited with ICP CVD underneath and above the nc-Si/MS film. Since all sample preparation processes were conducted sequentially in the high-vacuum environment, the quality and characteristics of the interfaces between nc-Si and MS matrix can be accurately controlled and reproducible.
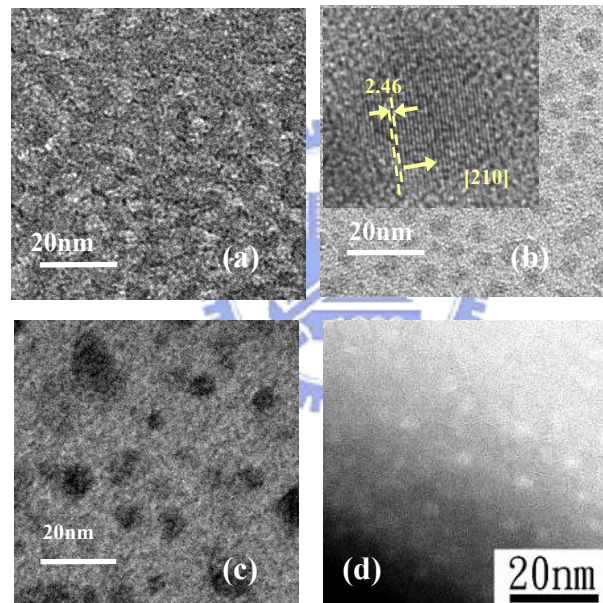
Fig 3.2 The cross-sectional TEM images of (a): pure MS film, and nc-Si/MS films with high-density of (b): small-size nc-Si, (c): large-size nc-Si prepared with twelve and fifteen cycles of pulse plasma, respectively. The inset shown in (b) reveals the lattice fringes of nc-Si. For comparison, the TEM image of nc-Si/MS film grown with steady-state plasma is also shown in (d).

	Conditions of Gas Supply	ICP sequence
		H₂ step (·····) SiH₄+ H₂ step (———)
steady-state plasma	steady-state SiH$_4$(1 sccm) + H$_2$(200 sccm) for 15 seconds	⟶ 15 sec
Pulsed plasma	twelve (fifteen) cycles of pulsed SiH$_4$(1 sccm) + H$_2$(200 sccm)/ H$_2$(200 sccm) with a duty cycle of 1 second/3 seconds	3S 1 3S 1 ⟶

Table 3.1 Flow rate and sequence of the ICP deposition cycles used for the preparation of nc-Si/MS film.
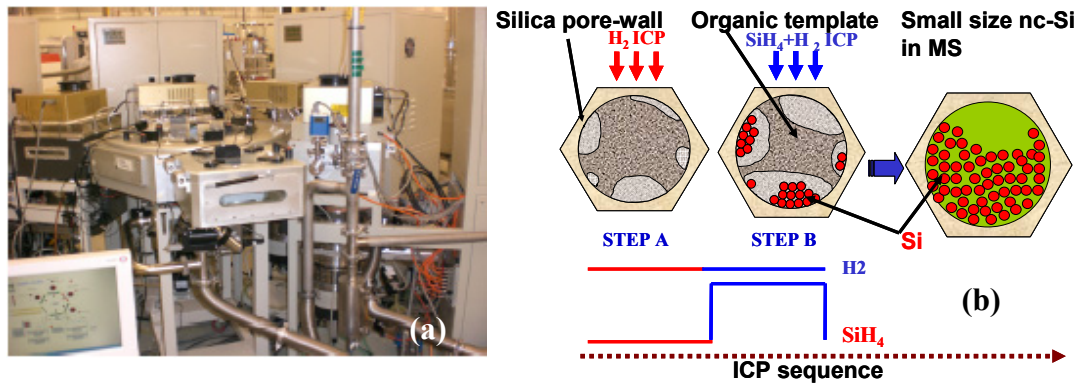
Fig 3.3 (a)The ICP CVD system which synthesize of nc-Si (nc-Ge) in MS matrices by

either pulsed or steady-state ICP and deposit of SiO_2 layers by stead-state ICP.

(b) Schematic mechanism of 3D Si nanodots formed by pulse ICP process.

3.3 Device fabrication

3.3.1 Capacitance fabrication

Current-voltage (I-V), capacitance-voltage (C-V) characteristics of nc-Si/MS nanostructured films were studied using a metal-oxide-semiconductor (MOS) capacitor structure. The testing devices involve a composite oxide (O) layer of SiO_2/nanostructured film/SiO_2 stack **(See Fig. 3.4)**.The top electrode pad of the MOS capacitor was made of an aluminum film, 250 nm in thickness and 400-μm in diameter. The back-side of the semiconductor substrate S was coated with a blanket aluminum film.
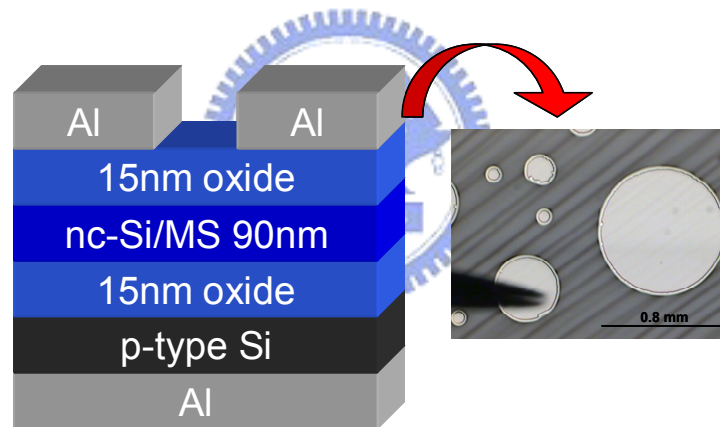
Fig. 3.4 The MOS structure with *nc*-Si/MS films

3.3.2 The fabrication of nc-Si/MS MOSFET

To test the feasibility of nc-Si/MS for FeRAM technology, a MOS field-effect transistor (MOSFET) was fabricated with a 70-nm nc-Si/MS layer was used in place of the gate dielectrics. A 15-nm thick oxide buffer layer underneath and above the nc-Si/MS film was introduced to inhibit charge transport through the gate dielectric structure. Poly-Si channels on quartz substrates were formed by the green CW laser-crystallization (**CLC**) of amorphous silicon islands with thicknesses of 100nm, which were deposited by low pressure chemical vapor deposition (**LPCVD**). Gate dielectrics of nc-Si/MS with a thickness of 100 nm together with thermally deposited poly-Si gates with a thickness of 200 nm, are applied to form self-aligned transistors. Poly-Si gates and S/D regions were doped with PH_3 ($5.0 \times 10^{15} cm^{-2}$ and 35 keV) and activated by furnace thermal annealing (**FA**) for 12 h at 580 ^{0}C.[6] **Fig. 3.5** shows the procedures and key facilities used for the fabrication of the test devices and the pictures of the fabricated devices.
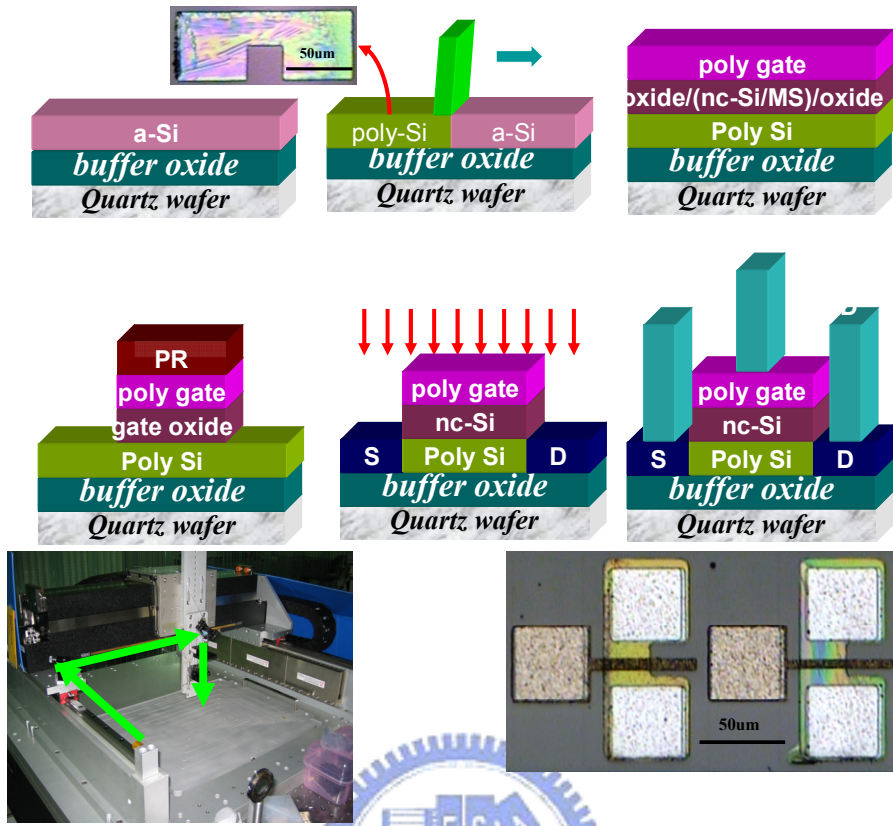
Fig. 3.5 The green laser-annealing system is formed of epi-like Si layers on quartz substrates and the transistor with poly Si/ SiO2/nc-Si-in-MS/SiO2 gate structure on the epi-like Si layers

3.4 Experiment Setup

The system we used to measure the high ferquence capacitance is **Bias Temperature Stress measurement system (BTS):** Keithley 590 CV analyzer 、 Keithley 595 Quasistatic CV meter、Keithley 230 programmable voltage source、 Keithley 5951 remote input coupler and computer with ICS software installed and the I-V measurement we used HP 4156A. **Fig 3.6** shows the schematic diagram of C-V measurement system.
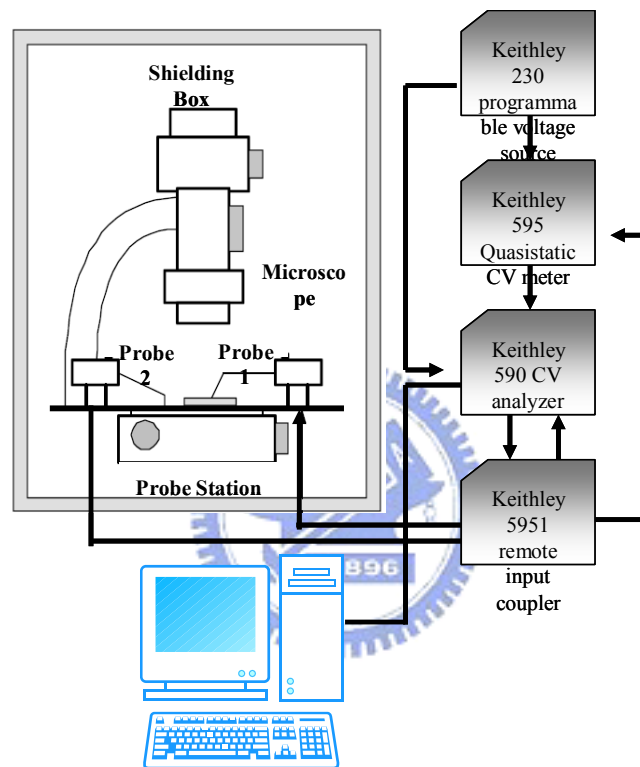
Fig. 3.6 The schematic diagram of C-V measurement system.

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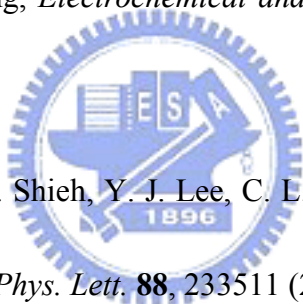
Chapter 4   Results and Discussions

4.1 C-V measurement

The capacitor test samples were prepared by spin coating a 90-nm thick MS nanotemplate layer on *p*-type silicon substrate. Si nanocrystals were thereafter synthesized in the MS templates by using the high-density inductively coupled plasma (ICP) method.[1][2] During the synthesis, we applied a negative voltage of 40 V at 300 kHz on the substrate. This creates preferential growth of *nc*-Si on the bottom of the pore-channels with schematic shown in **Fig. 4.1**. The resulting one-side bonded silicon nanocrystals yield polar oriented layers of Si-O bonds.

Typical capacitance-voltage (**C-V**) characteristic of an metal-oxide-semiconductor (**MOS**) structure with a SiO$_2$/*nc*-Si-in-MS/SiO$_2$ stack on a *p*-type silicon substrate and with a top circular Al pad, 400 μm in diameter, is presented in **Fig. 4.2.** The thickness of the *nc*-Si-in-MS and one oxide buffer layer is about 90 nm and 15 nm, respectively. We found two key features in this C-V measurement. First, a clockwise hysteretic loop (see the red-colored hysteretic curve in **Fig. 4.2**) appears in the MOS capacitor.[3][4] Note that charging (discharging) of QDs by electrons (holes) via a tunneling process can shift the flat-band voltage to a more (less) positive value.[5] This shall leads to a counter-clockwise[6] C-V loop

when a positive-to-negative-to-positive voltage sweep is carried out, which contradicts with what we had observed. Secondly, the leakage current through the SiO_2/nc-Si-in-MS/SiO_2 stack of our samples is extremely low with a magnitude of $1.0 \times 10^{-7} A/cm^2$ at 1×10^6 V/cm, indicating a very low tunneling current in our samples. The ferroelectric-like nature of the clockwise C-V hysteretic loop on p-type Si substrate distinguishes clearly from that was observed with larger Si quantum dots in the same size of nanoporous MS shown by the blue-colored curves in **Fig. 4.2.** By growing larger Si nanodots to completely fill the cross sections of pore channels, a centrosymmetric bonding structure is achieved. The resulting C-V characteristic reveals a counter-clockwise loop. Therefore we attribute the observed clockwise C-V hysteretic curve of our MOS capacitor with one-side bonded nc-Si/MS to an electrical polarization layer.[7] Depending on the direction of the applied electric field, the built-in dipole field of the sample would either enhance or screen the external field, resulting in the observed C-V hysteretic loop with red-color shown in **Fig. 4.2.** A polarization-induced C-V memory window (ΔV) as large as 11.5 V was obtained.

According to the theoretical work by Miller and McWhorter,[8] an electrical polarization higher than 0.1 C/cm^2 is sufficient to switch the Si surface potential from depletion to inversion. Ferroelectricity-induced C-V memory window (ΔV) can be related to the coercive field (E_c) with $\Delta V = 2E_c.d$,[7] where d denotes the thickness of

ferroelectric films. The C-V memory window was calculated to be about 12.6 V with

a measured coercive field[9][10] of 700 kV/cm (see **Fig. 2.8)**. This agrees reasonably

well with the result shown in **Fig. 4.2.**

4.2 I-V characteristics of the ferroelectric memory

To test the feasibility of *nc*-Si/MS for FeRAM technology, a MOS field-effect

transistor (MOSFET) with a 70-nm *nc*-Si/MS layer in place of the gate dielectrics was

fabricated as illustrated on **Fig. 4.1**. A 15-nm thick oxide buffer layer underneath and

above the *nc*-Si/MS film was introduced to inhibit charge transportation through the

gate structure. The MOSFET with a channel length (L) of 10 μm and a channel width

(W) of 10 μm was fabricated on a laser-crystallized layer of 100 nm in thickness[11]

on quartz substrate. **Fig. 4.3** shows the drain currents I_d as a function of gate voltage

V_g. The V_g was varied from -17 V to 17 V with an increment of 0.1 V while the drain

voltage V_D was kept constant at 0.1 V. As the V_g changed from −17 V to +17 V, the

device switches from the "off" state to the "on" state with the turn-on threshold

voltage at 2.2 V. On the contrary, as the V_g changed from +17 V to −17 V, the device

switched from the "on" state to the "off" state with a turn-off threshold voltage of -5.2

V, yielding a memory window of about 7.4 V.[4][12] Notice that after writing the

"off" state, the drain current I_d is about $2.5×10^{-13}$ A at V_g=0 V. In the "on" state, the I_D

is about $1.34×10^{-5}$ A with a gate voltage of 0 V. The contrast ratio of the "on" to the

"off" state is larger than 7 orders.

Fig. 4.4 shows I_d versus V_d characteristics of a 10μm* 10 μm memory device after writing to the "on" state and "off" states using a gate voltage of 17 V and -17 V, respectively. Small gate voltages of -2, -1.5, -1, and -0.5 V and a drain voltage of 0.1 V were applied to prevent any unwanted writing during reading. Drain currents of 0.36 pA, 0.19 pA, 0.14pA and 0.43 pA were measured at V_g of -2 V, -1.5 V, -1V and -0.5 V, respectively, after the device has been written to the "off" state. In contrast, drain currents of 1μA, 2μA, 4μA and 6μA were measured at of -2V, -1.5V,-1V and -0.5V, respectively, after the device was written to the "on" state. Clearly, the "on" to "off" state current ratios differ in magnitude by 7 orders, which is consistent to the versus measurement shown in **Fig. 4.3. Fig. 4.5** shows the retention properties of transistors. The threshold voltage is measured as a function of time after applying writing of +17 and −17 V, respectively. The threshold voltage was measured by sweeping gate voltage from -6 to 6 V. As illustrated in **Fig. 4.6.**

4.3 Discussion

Two major causes of the short data retention time in FeRAM are: 1) depolarization field and 2) finite gate leakage current.[12][13]

1. Depolarization field

The depolarization field is intrinsic in the ferroelectric layer. That is, the direction

of the electric field in the ferroelectric film is opposite to that of the polarization.

For the gate stack of a MFIS structure shown in **Fig4.7** [13], a depolarization field

always exists due to the finite compensating charge of the insulator and

semiconductor. The relationship between depolarization field and the oxide

capacitance can be expressed as following equation:

$$E_{dp} = PC_F / [\varepsilon(C_{IS} + C_F)]$$

The C_{IS} is the capacitance of the insulator layer, and the C_F and P is the

capacitance and the polarization of the ferroelectrics. From the equation we can see

that C_{IS} is not infinity. There is always a finite depolarization field. This

depolarization field is in the direction of reducing the polarization in the ferroelectric

and tends to reduce the memory retention time. So it is suggested that in order to get a

smaller depolarization field, the larger ratio of C_{IF}/C_F is necessary. Since our

nc-Si/MS nanostructured material intrinsically has a low dielectric constant, the

depolarization field shall not be a problem.

2. Gate leakage current and charge trapping

The gate leakage current and trapping of carriers through the MFIS gate dielectric

stack is another major cause of the reduced retention time. **Fig. 4.8** [13] illustrates the

situation where the MFIS gate stack has just been programmed such that the

ferroelectric polarization induces Si-channel to inversion in the p-type semiconductor.

Therefore the MFIS-FET is "on" state. This ferroelectric polarization attracts electron

injection from both the gate electrode and the semiconductor side. This electron

injection is followed by trapping in the gate dielectric stack, leading to local charge

compensation and gradually diminished the effect of polarization. Thus, the memory

retention is no longer observed after a long time.

The retention time of a FeRAM device, in which the remnant polarization is P_r,

leakage current I, and a trapping probability of α, can be estimated with

$\tau = P_r / I\alpha$.[12] **Figure 4.3** shows a very low leakage current with applied voltages of

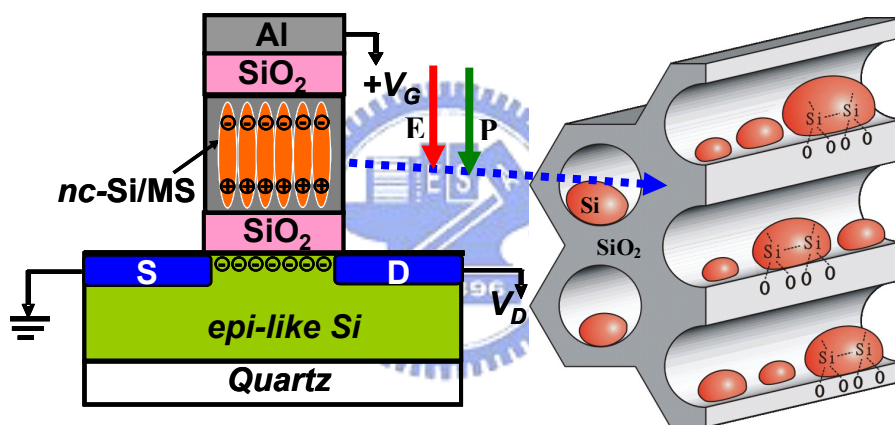17 V. The leakage current may not affect the retention property seriously.

Fig. 4.1 Schematic drawing illustrating the one-side bonding geometry of Si
nanocrystals in porechannels prepared by applying an electric field during
the synthesis process (right plot). A transistor with Al/
SiO_2/nc-Si-in-MS/SiO_2 gate structure on the epi-like Si layers that was
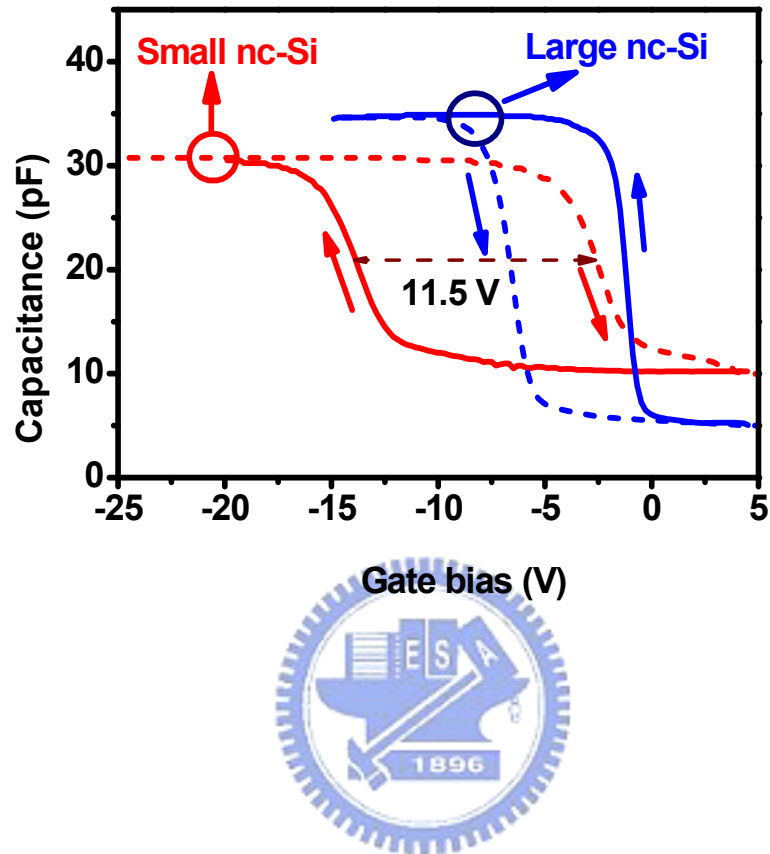activated by green laser irradiation was illustrated on the left plot.

Fig. 4.2 C-V hysteresis characteristics of a MOS capacitor containing the Si-O polar layer of *nc*-Si/MS capped with a 15-nm thick SiO_2 buffer layer on the top and bottom (red-colored curves). For comparison, C-V hysteresis for a MOS capacitor with larger *nc*-Si to completely fill the porechannels of MS (solid and dashed curves in blue) is also presented. Solid and dashed curves indicate the C-V obtained with a voltage sweep from positive to negative and from negative to positive, respectively.
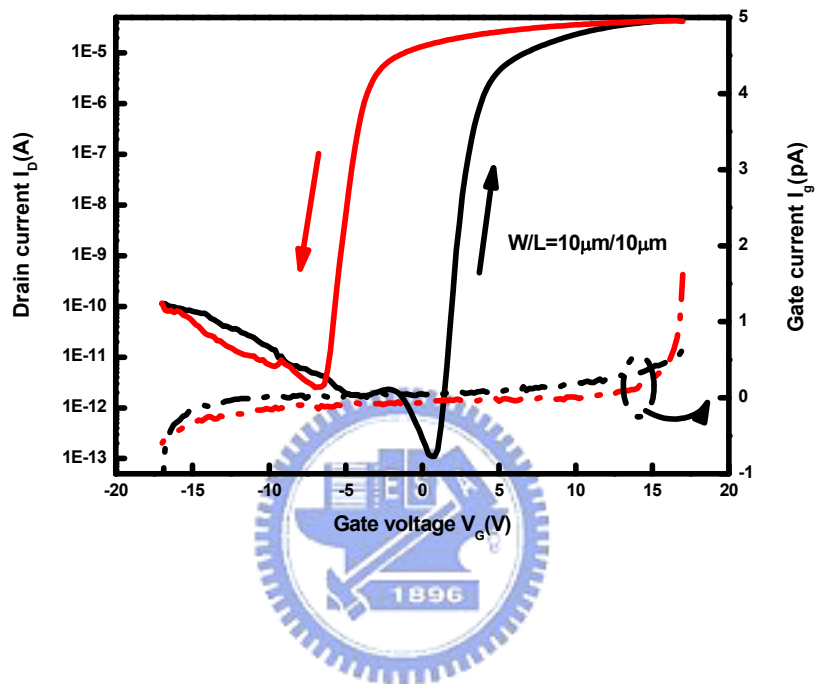
Fig. 4.3 A ferroelectric-like switching with ultralow gate current was demonstrated

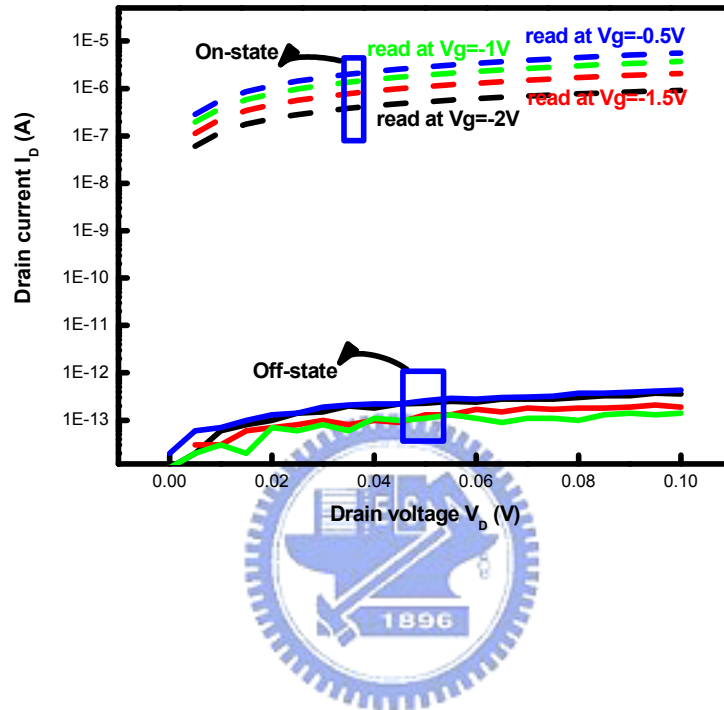with a MOSFET structure depicted in Fig. 4.1.

Fig. 4.4 I_d versus V_d characteristics of a 10μm* 10 μm memory device after writing to

the "on" state and "off" states using a gate voltage of 17 V and -17 V,
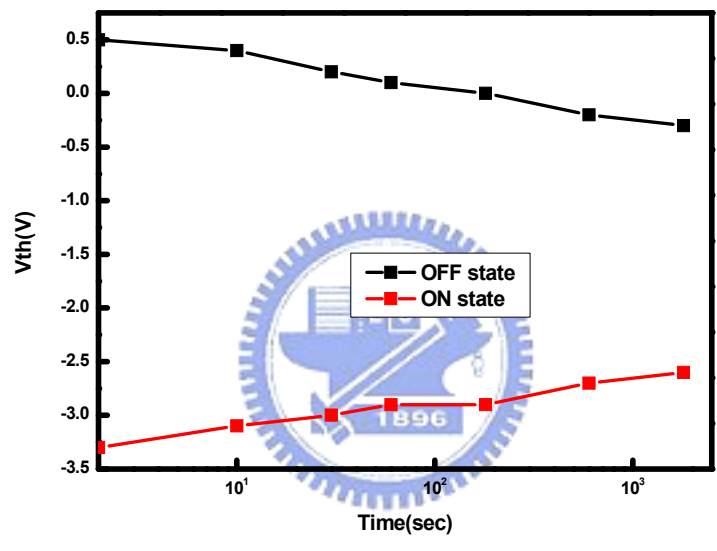
respectively.

Fig. 4.5 The retention properties of transistors. The threshold voltage is measured as a

function of time after applying writing of +17 and −17 V, respectively. The

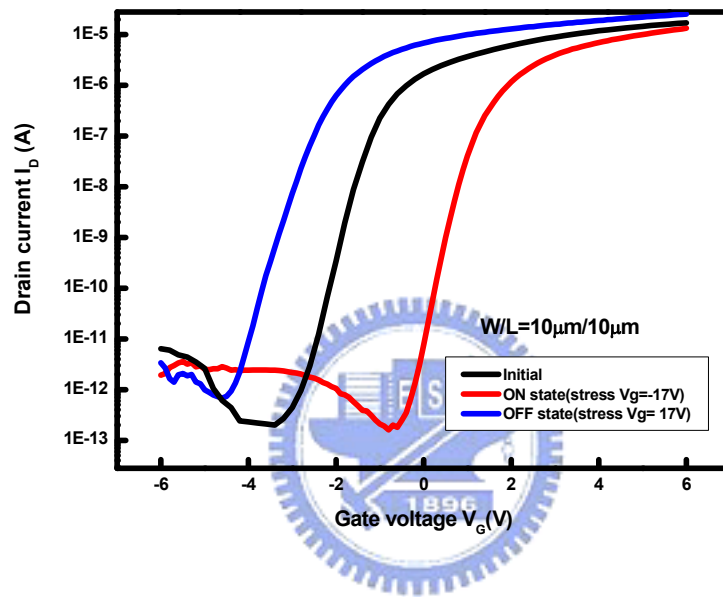threshold voltage was measured by sweeping gate voltage from -6 to 6 V.

Fig. 4.6 The initial state and the device after writing to the "on" state and "off"

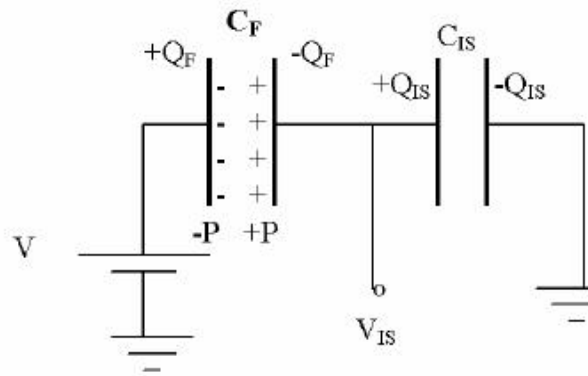states using a gate voltage of 17 V and -17 V, respectively.

Fig. 4.7 Gate stack of the 1T-FeRAM is modeled by a ferroelectric capacitance (C_F) in series with the semiconductor capacitance C_{IS} , where C may be generalized to represent the series combination of an insulating buffer on top of the semiconductor. A gate voltage V induces a polarization P and a voltage V_{IS} across C_{IS}
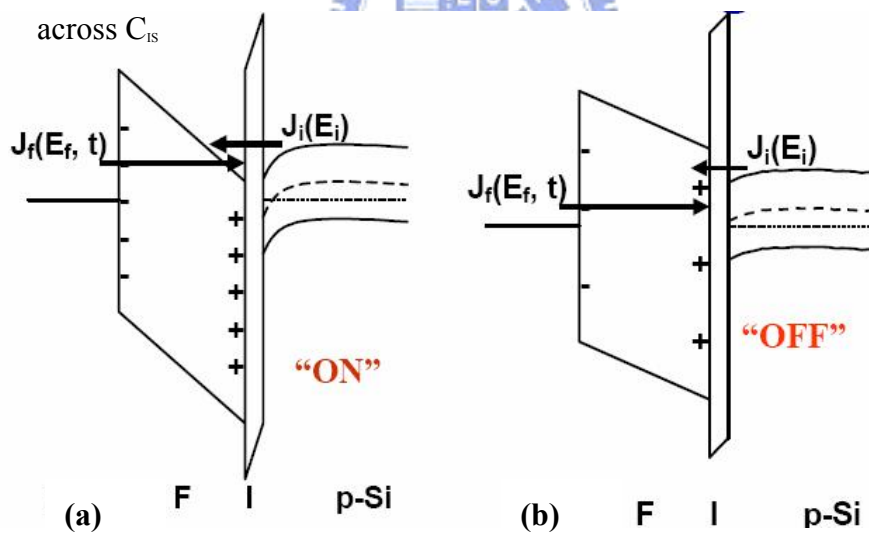

Fig. 4.8 (a) The MFIS-FET is in its "on" state and the electric field distribution favors electron injection toward the ferroelectric/buffer interface where some electrons are trapped in the dielectric stack and (b) sufficient electron trapping has taken place that results in diminished polarization effect ,the MFIS-FET is in its "off" state.

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Chapter 5   Conclusions and future work

5.1 Conclusion

By inductively coupled plasma chemical vapor deposition **(ICPCVD)**, we dispersed three-dimensional dispersed Si nanocrystals (NCs) within the mesoporous silica films. ICP makes reactive species own highly mobile and bond with pore-wall well, therefore, efficiently construct 3D Si NCs/silica arrays. Material characterizations indicated that the nanocrystals formed non-centrosymmetric bonding with the host silica matrix with highly stable interface structures, which exhibited the dipole effect at one-side bonded surfaces of Si nanocrystals with mesoporous silica matrix. The polar structure is verified by optical sum-frequency generation and P-E measurement. A remnant polarization of $P_r = 5\,\mu C/cm^2$ (saturated polarization $P_s = 8\,\mu C/cm^2$) and a polarization-induced C-V memory window (ΔV) of 15V were achieved. A MOS field-effect transistor was fabricated with a *nc*-Si/MS layer in place of the metal gate. Our device shows a clear polarization-induced memory window of 7.4V with very low gate leakage and high ratio of the "on" state to the "off" state, thus promises for better FeRAM nonvolatile memory devices.

5.2 Future works

In this thesis, the gate structure was poly Si, the activation temperature may be cause the ferroelectric-like structure some damage. Therefore, we could use the Al gate and use the green laser activation. These process are low temperature so that preventing thermal damage about the ferroelectric-like structure.