國立交通大學

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碩 士 論 文

複晶矽薄膜電晶體之光特性研究

Study on Photo Characteristics of Polycrystalline Silicon Thin-Film Transistors

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Chinese Abstract

在此論文裡，我們將分為兩個主題，第一個主題針對光漏電機制做探討，第二個主題是對具有橫向身體端的薄膜電晶體元件做光特性方面的研究。在第一個主題部分，從文獻中可以瞭解光漏電與通道底部及主動層厚度有關，因此我們對元件的通道做摻雜處理，試圖抑制光漏電。照光後的電子電洞對會有部分被我們創造的複合中心所捕獲，而使到達源極與汲極端的電子電洞對減少而降低光漏電流。經由不同深度的通道摻雜，我們發現摻雜於通道底部對抑制光漏電最為有效。我們並且改變主動層的厚度，對於有無通道底部摻雜的元件做進一步的研究。

在第二個主題部分，我們設計了不同尺寸不同身體端位置的薄膜電晶體元件，並對於元件做基本特性的量測，而確定了身體端收集到的電流是來自衝擊離子效應所產生的電洞。而在照光實驗中，發現了具有身體端的薄膜電晶體元件可以偵測光電流，因此對光特性方面做進一步的研究。對於量測的結果，我們提出了能帶圖來解釋其電性。

English Abstract

In this thesis, we investigate two subjects. First is the study on the mechanism of photo leakage current. Secondly, the study on photo characteristics of polycrystalline silicon Thin-Film Transistors with lateral body terminal (LBT TFTs). In first subject, we implanted the channel of TFTs in order to reduce the photo leakage current. From reference, the photo leakage current is dependent on the channel and the thickness of active layer. The part of electron-hole pairs which generate by backlight could recombine by the trap which we create. The photo current becomes lower because both the electrons which reach the drain terminal and the holes which reach the source terminal become lower. By different depth of channel implanted, we could observe the TFTs with implanted the bottom of channel have least photo current. Then we change the thickness of active layer in order to research further.

In second subject, we designed the LBT TFTs with varied LBT position and size. We measured the device characteristics. The body current comes from the holes which generate by impact ionization. In light experiment, we found the LBT TFTs could sense light. So we measured the LBT poly-Si TFTs in dark and irradiated illuminance to analyze the device behavior. We thought that the device behavior is come from the L shape p/i/n in LBT TFT. In LBT TFT, source and drain is n+ region, channel is intrinsic region, and LBT is p+ region. In order to explain the device behavior, the energy band of the p/i/n in LBT TFTs is proposed.

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Chapter 1 Introduction

1.1 Overview of Low Temperature Poly-Si Thin-Film Transistors

In recent years, the polycrystalline silicon thin-film transistors (poly-si TFTs) have been widely used in active matrix liquid crystal display (AMLCDs) **[1.1]-[1.3]** ,active matrix organic light emitting displays (AMOLEDs) **[1.4]-[1.6]**. Except large area displays, poly-Si TFTs also have been applied into some memory devices such as dynamic random access memories (DRAMs) **[1.7]**, static random access memories (SRAMs) **[1.8]**, electrical programming read only memories (EPROM) **[1.9]**, electrical erasable programming read only memories (EEPROMs) **[1.10]**, linear image sensors **[1.11]**, thermal printer heads **[1.12]**, photo-detector amplifier **[1.13]**, scanner **[1.14]**, neutral networks **[1.14]**. The major attraction of applying polycrystalline silicon thin-film transistors (poly-Si TFTs) is in active matrix liquid crystal display (AMLCDs) lies in the greatly improved carrier mobility in poly-Si film and the capability of integrating the pixel switching elements and the capability to integrate sophisticated digital and analog driving circuit on the glass substrates**[1.15]-[1.17]**. For the poly-Si active layer, carrier mobility larger than 10 cm^2/Vs can be easily achieved, that is enough to use as peripheral driving circuit including n-and p-channel devices (or p-channel only). Such performance brings the era of system-on-panel (SOP) technology. The process complexity can be greatly simplified to lower the cost (which save the IC and FPC BOM cost). In addition, the mobility of poly-Si TFTs much better than that of amorphous ones, the dimension of the poly-Si TFTs can be made smaller compared to that of amorphous Si TFTs for high driving current and high resolution AMLCDs, and the aperture ratio in TFT array can be significantly improved by using poly-Si TFTs as pixel switching elements. This is because that device channel width can be scaled down while meeting the same pixel driving requirements as in α-Si TFT AMLCDs.

The manufacture of polycrystalline silicon thin film transistors (poly-Si TFTs) embraces

numerous steps commonly encountered in MOSFET fabrication for integrated circuits. Despite the similarities, however, a number of key differences exist. These differences emerge primarily from the fact that the substrate of TFTs is no longer a single-crystal silicon wafer, but rather a heat-sensitive material such as glass. In MOSFET fabrication, poly-silicon is usually prepared by LPCVD and then annealed above 900°C, namely, SPC (Solid Phase Crystallization) method. Unlike MOSFET devices, the TFT active layer needs to be formed on such amorphous host material and the temperature of all associated process has to be districted within the allowable range prescribed by the materials characteristics of the substrate. For current display-glass substrates, maximum processing temperature needs to be kept below 650°C. Even after considering possible exceptions to this maximum temperature such as RTA, the temperature range for fabrication on glass is severely constrained with respect to that on silicon. This limitation affects critical process steps, such as the gate-insulator formation and the activation of the doped regions of the device. These processes have to be reconsidered and optimized for TFT fabrication on glass. Hence, low temperature polysilicon (LTPS) technology is the novel technology specific for the flat panel display manufacture. Now, there are several ways to prepare the LTPS film on glass or plastic substrate: Metal-Induced Crystallization (MIC), Excimer Laser Crystallization (ELC), and Sequential Lateral Solidification (SLS), etc. Because of the methods mentioned above, the manufacturing technologies of poly-Si TFTs can lower the maximum process temperature enabling the use of low-quality glass and therefore reduce production cost **[1.10]**.

Enhancing the performance of poly-Si thin-film transistors, as well as improve their reliability to realize various applications mentioned above. Recently, the performance gap between poly-Si TFTs and single-crystalline silicon devices has become smaller as a result of the advancement in poly-Si crystallization techniques. In comparing poly-silicon devices with their single-crystal counterparts, the major difference arises because of the presence of grain boundaries in the poly-Si. There are high density trap states in the grains and along the

grain boundaries, and the electrical activity of the charge-trapping centers profoundly affects the electrical characteristics of poly-Si TFTs. Large amount of defects serving as trap states locate in the disordered grain boundary regions to degrade the ON current seriously **[1.17]**. In short, the grain boundary influences the TFT characteristics, and the typical device characteristics of TFTs will be poor compared with the devices fabricated on single crystal silicon film.

Moreover, the relatively large leakage current is one of the most important issues of poly-Si TFTs under OFF-state operation **[1.18]**, **[1.19]**. The dominant mechanism of the leakage current in poly-Si TFTs is field emission via grain boundary traps due to the high electric field near the drain junction **[1.19]**-**[1.22]**. Consequently, there are two ways to reduce leakage current: one is to reduce grain-boundary trap density and the other is to alleviate the electric field near the drain side.

To overcome this inherent disadvantage of poly-Si films, many researches have been focused on modifying or eliminating these grain boundary traps. Hydrogenation is a method for reducing the trap density in poly-Si films **[1.23]**-**[1.25]**. As the number of trapped carriers decreases, the potential barrier associated with the grain boundary also decreases. The defect-state density can also reduced by improving the crystallinity of poly-Si film with techniques such as laser annealing **[1.26]**-**[1.27]** and solid-phase crystallization **[1.28]**, **[1.29]** to enlarge the grain size. For devices with smaller dimensions, the number of grain boundaries decreases since there are fewer grains within the channel region. Because the drain voltage drops on the depletion regions located at grain boundaries, a large electric field will exist in small dimension TFTs and make the drain current increase dramatically due to the impact ionization. Hence, a drain offset region or lightly-doped drain region is used to suppress leakage current by decreasing drain electric field.

The substrate dissimilarity, however, has an even more immediate impact on the process flow of TFTs. Unlike MOSFETs, Where the device active layer is part of the substrate, in the

case of TFTs the active layer needs to be separately formed on the host substrate. The common way of doing that, for poly-Si TFTs, is by deposition of an amorphous Si (a-Si) film on host substrate and the annealing step. Both of these steps affect the micro-structural quality of the result critically affected by the selection of techniques and operating parameters for the deposition and crystallization of the thin Si film. It should be further noted that these steps are also constrained, as far maximum temperature, per our earlier discussion.

1.2 Motivation

The market for liquid crystal displays has been rapidly expanding in recent years. The demand for a high luminance and a high contrast ratio in liquid crystal displays (LCDs), such as small-medium LCDs for projection device, mobile displays and displays for cars, is continuing to grow and seems insatiable. However, high luminance would increase photo leakage current (PLC) in the TFTs, which diminishes the voltages that are held across the pixel electrodes or affect the gray level controlling, which in turn, would cause a low contrast ratio and error color display. For instance, the off current of poly-Si TFTs exposure at the 3000nits backlight is higher than in the dark, which is about higher one order, shows as the Fig.1.1 and Fig.1.2. Not only low drain voltage but also high ones. It is suffer the On/Off ratio of device and will affect the TFTs operating. It goes without saying for the application of brightness about 8000nits in car. Consequently, it is necessary to suppress the PLC in LCDs with high luminosity.

Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film. It follows that the excess holes flow to the drain under the negative drain bias for p-channel devices, generating the photo leakage current. And the photo leak current depends linearly on the thickness of active layer while the electron-hole pairs are insensitive to the thickness [1.30]. Because the implant can increase trap density, the electron-hole pairs

can recombine by the trap. To reduce photo leakage current I_{PLC}, we designed poly-Si TFTs with different depth of implant and various dose of boron. As the key condition of photo leakage current are the bottom and thickness of active layer. We designed poly-Si TFTs with different thickness and two kind depth of implant. One is the poly-Si TFTs with two-thirds implanted depth of active layer and five thicknesses. Second is poly-Si TFTs with implanted the bottom of active layer and three thicknesses. In chapter 3, we canvassed our research in poly-Si TFTs with different active layer.

Low-temperature polysilicon thin film transistors (TFTs) employing excimer laser annealing (ELA) may be promising devices for high resolution active matrix liquid crystal display (AMLCD) owing to their high mobility and low thermal budget [1.31]. However, a critical problem of polysilicon TFTs is the kink effect caused by inherent floating body effect structure [1.32]. The TFT employing a counter-doped lateral body terminal is proposed to suppress the kink effect by collecting the counter-polarity carriers [1.33]. Because the TFTs with lateral body terminal (LBT) can collect the counter-polarity carriers, we designed TFTs with small LBT size and varied LBT position and varied channel length to make a study of the floating body effect and the photo characteristic of TFTs. In chapter 4, we canvassed our research in photo characteristics of Poly-Si TFT with counter-doped lateral body terminal.

Chapter 2 Device Fabrication and Experiment

Second, detailed poly-Si TFTs fabrication processes and experimental procedure were described.

2.1 Fabrication Process of Poly-Si TFTs

The top gate p-channel and self align light drain doping (LDD) TFTs were fabricated on Corning1737 glass substrate [1]. First, the buffer SiNx/oxide layer and 50 nm thickness a-Si:H film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380℃, we dehydrogenated aSi:H film in a furnace at 450℃. Then the poly silicon channel was formed by 308nm XeCl excimer laser irradiation at 350mJ/cm2. In this work, 95% laser overlap ratio was adopted to obtain large grain size and better uniformity of active layer. As the SEM Fig2.1, the average grain size of polycrystalline silicon was found to be 280~300nm [3]. The island was patterned by plasma dry etching Fig2.2. The 100nm thickness gate insulator was deposited by TEOS (Tetra-Ethyl-Ortho-Silicate)-base oxide. The source/drain and LDD region were formed by the mass-separated ion implanter technique. The doping activation was performed at 530℃/1hr thermal furnace and RTA irradiation Fig2.3~Fig2.5. Finally, the interlayer oxide and inter-connection metal were deposited and pattern. The H2 plasma hydrogenation was performed in a commercial RF parallel-plate plasma reactor at 100W, 480℃ 15min in H2 and Argon gas mixture. The SiO2/SiNx with 300nm and 100nm interlayer film and source/drain contact holes etching and S/D metal patterning Fig2.6. Finally, the planer layer (UHA2) and ITO were employed on our device Fig2.7 [4-6]. The fabrication process of n channel Poly-Si TFTs with lateral body terminal (LBT) are almost the same as n channel LTPS Poly-Si TFTs, The p-doped lateral body terminal is the only different. The fabrication process of LBT TFTs needs no additional mask step. The body terminal was formed by the mass-separated ion implanter technique. The device electrical measurements were finished by HP4156C and Keithley

4200-SCS.The data of chapter3 were measured by HP4156P, and the data of chapter4 were measured by Keithley 4200.

2.2 Introduction of Instruments

In this thesis, all of the electrical characteristics of proposed poly-Si TFTs were measured by HP 4156B-Precision and Keithley 4200-SCS Semiconductor Parameter Analyzer , illustrated in Fig2.8, a probe station is situated inside a dark box. Many methods have been proposed to extract the characteristic parameters of poly-Si TFTs.The photo leakage current was measured as we putted the device up on back-light. We can change the applied current of back-light to control the brightness. The ground probe station is furnished with an electrically isolated, water-cooled thermal chuck. The chuck is controlled by Temptronic TPO315A thermal controller, which can operate temperature from 25°C to 75°C. An Agilent 4156C precision semiconductor parameter analyzer can provide I-V measurement, bias for BTS, and quasi C-V measurement, etc. We employ the ICS (Interactive Characterization Software) to obtain the output and transfer characteristics, like V_D-I_D, V_G-I_D (Linear), V_G-I_D (saturation), and extract the typical semiconductor parameters. An analyzer Keithley 4200-SCS can do the same analyze like HP4156C.

2.3 Electrical Characterization Measurement and Analysis

2.3.1 Output Characteristics

The typical TFT output characteristics are shown in Fig.2.12. They represent the dependence of the Drain-Source current (I_{DS}) on the Drain-Source voltage (V_{DS}) at different gate voltage (V_{GS}). The Drain-Source current increase linearly at low Drain-Source voltage (Linear regime/operation) and saturates at high Drain-Source voltage (Saturation regime /operation). The saturation values of I_{DS} depend on the applied gate voltage. When the low gate voltage is applied, the thickness of the induced channel is small and current is low. On

the other hand, thicker channel is induced at high gate voltage and the saturation current is higher. Well-separated output characteristics are an indication of good ohmic contact at drain and source. The transistor enters in saturation regime when $V_{DS} > V_{SAT}$, where $V_{SAT}=V_{GS}-V_T$. In Id_Vd curve, the points corresponding to $V_{DS} = V_{SAT}$ are connect the blue line described the following equation:

$$I_{DS} = \frac{1}{2} \times \mu_{fe} \times Cox \times \frac{W}{L} \times \left[(V_{GS} - V_T)^2 \right] \quad (2\text{-}1)$$

When W and L are the width and length of the transistor channel, μ_{fe} is the field-effect electron mobility and C_{ox} is the gate insulator capacitance. The threshold voltage and the field mobility effect mobility can be determined from measuring the saturation current, plotting the square root of the measured I_{DS} vs. V_{GS} in saturation ($V_{DS} \geqq V_{GS}-V_T$).

Of course, the poly-Si TFTs are not perfect device as the single crystalline; it is since the grain boundary [10]. The region of operation in poly-Si TFT roughly:

A. Cut-off : Current is due to reverse-bias drain junction leakage trap-assisted mechanisms.
B. Subthreshold : Current is due to carrier diffusion. Limited by source junction potential barrier.
C. Pseudo-subthreshold : Current is due to carrier drift. Inversion-charge density Q_{inv} increases ~linearly with V_G-V_T. The field mobility μ_{fe} increases ~ exponentially with V_G → I_D increases ~ exponentially with V_G.
D. Above threshold : Current is due to carrier drift, Qinv V_G-V_T; μ_{fe} ~ constant → I_D increases linearly with V_G

Refer to the Fig2.9.

2.3.2 Methods of Device Parameter Extraction

In this section, we will introduce the methods of typical parameter extraction such as the threshold voltage V_T, subthreshold swing S.S, field-effect mobility μ_{FE} from the device

characteristics.

Several methods are used to determinate the threshold voltage, V_T, which is the most important parameter of the semiconductor devices. The method to determinate the threshold voltage in this thesis is the constant drain current method, the voltage at a specific normalized drain current NI_D is taken as the threshold voltage. This technique is adopted in most studies of TFTs. It can give a threshold voltage close to that obtained by the complex linear extrapolation method. Typically, the specific normalized current $NI_D = I_D/(W/L)$ is defined at 10nA for V_D operated in linear region and 100nA for V_D operated in saturation region, to extract the threshold voltage of TFTs in most papers.

The subthreshold swing S.S (V/dec) is a significant parameter to describe the control ability of gate bias toward drain current and the efficiency of the switch turning on and off. It is defined as the amount of gate voltage required to increase/decrease drain current by one order of magnitude. It should be independent of drain voltage and gate voltage. However, in reality, the subthreshold swing might increase with drain voltage due to the short-channel effects such as charge sharing, avalanche multiplication, and punch through-like effects. It is also related to the gate voltage due to some undesirable factors such as serial resistance and interface state. In this experiment, the subthreshold swing is defined as one-second of the gate voltage required to decrease the threshold current by two orders of magnitude. The threshold current is specified to be the drain current when the gate voltage is equal to the threshold voltage.

The field-effect mobility (μ_{FE}) is determined from the transconductance g_m at low drain voltage (linear region). The transfer characteristics of poly-Si TFTs are similar to those of conventional MOSFETs, ignoring any other non-ideal effect and assuming the electric field in the channel is uniform, so the first order I-V relationship in the bulk Si MOSFETs can be applied to the poly-Si TFTs, which can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_T)V_D - \frac{1}{2}V_D{}^2] \quad (2\text{-}1)$$

where C_{ox} is the gate oxide capacitance per unit area

W is channel width

L is channel length

V_T is the threshold voltage.

If V_D is much smaller than (V_G-V_T) (i.e., $V_D << V_G$-V_T) and $V_G > V_T$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_T)V_D \quad (2\text{-}2)$$

The transconductance is defined as

$$g_m = \frac{\partial I_D}{\partial V_G}\Big|_{V_D=const.} = \frac{WC_{ox}\mu_{FE}}{L}V_D \quad (2\text{-}3)$$

Therefore, the field-effect mobility can be obtained by

$$\mu_{FE} = \frac{L}{C_{ox}WV_D}\mathrm{g_m} \quad (2\text{-}4)$$

The mobility value was taken from Equation (2-4) with maximum μ_{FE} .

Chapter 3 Polycrystalline Thin Film Transistor with different active layer

In this chapter, the research is into the TFTs active layer which influences the device behavior. We have regard to the thickness of the semiconductor layer and the channel implant. In following section, we had expanded on the measurement of the TFTs with implanted active layer, various poly-Si thicknesses, and implanted the bottom of active layer.

3.1 Results of TFTs with Implanted Channel

Figure 3.1 shows the I_D-V_G transfer curves of conventional p-channel poly-Si TFT operated in linear region under the dark and photo states. The brightness of back-light for photo state measurement is set as 3100nits. As the gate bias is swept from 12 to 0 V, the leakage current of poly-Si TFTs in the dark state was about 10^{-13} A. With the same range of gate bias, the leakage current of poly-Si TFT under illumination is as high as two orders of magnitude, around 10^{-11}A. In addition, the sub-threshold swing is increased under illumination, about 0.45 V/dec, as the initial value in dark is 0.29 V/dec. The variation of sub-threshold swing is about 55%. The on/off current ratio of poly-Si TFTs was substantially reduced due to the high photo leakage current, so that the function of TFTs used as the pixel switch under illumination would be affected seriously.

Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film. Furthermore, the energy-band structure of Si material is indirect bandgap. The excess electron-hole pairs induced by the absorption of light would not be recombined from band to band directly due to the momentum conservation principle. The numerous electron-hole pairs are accumulated in the bottom of poly-Si layer. It follows that the excess

holes flow to the drain under the negative drain bias for p-channel devices, generating the photo leakage current. These electron-hole pairs either recombine at the glass/poly-Si interface or diffuse to the gate SiO2/poIy-Si interface and recombine there. Because the implant can increase trap density, the electron-hole pairs can recombine by the trap. To reduce photo leakage current I_{PLC}, we designed poly-Si TFTs with different depth of implant and with various dose of boron. Four kind poly-Si TFTs as follows, in Fig.3.2 and Fig.3.3.

1. No implant：The conventional poly-Si TFTs without channel doping.
2. 200A,8E11；200A,9E11；200A,2E12：The depth of implant is about 200A with various doses 8E11, 9E11, and 2E12. Because the thickness of active layer is 500A, the depth of implant 200A is above half of active layer.
3. 550A,2.8E12：Depth of implant is 550 A and dose of implant is 2.8E12. Because the thickness of active layer is 500A, the depth of implant 550A is below the bottom of active layer.
4. CD STD：Depth of implant is 375A and dose of implant is 1E12. Because the thickness of active layer is 500A, the depth of implant 375A is below the half of active layer.

The photo leakage current of the conventional and the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is -0.1V, with the increasing brightness of back-light (2160, 3100, 4110, 5620 nit) are illustrated in Fig.3.4. The photo leakage current of conventional poly-Si TFTs increases substantially with increasing brightness of back-light. In contrast, for TFTs with channel doping, the leakage current under illumination is slightly increased and remain a weak dependence of the brightness of back-light. For TFTs with the depth of implant is about 200A, photo leakage current increases as the implant dose increases. But as the depth of implant is below 375A, the photo leakage current is very low even the implant dose is high. As the depth of implant is 550A, the photo leakage current reduces most even the implant dose is 2.8E12. The photo leakage current of

the conventional and the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 7V as V_D is -9V, with the increasing brightness of back-light (2160, 3100, 4110, 5620 nit) are illustrated in Fig.3.5. We could observe that the current of TFT with implant depth 200A and highest implant dose 2E12 is higher than the conventional poly-Si TFT. Table3.1 shows the common TFTs characteristic (V_{th}, mobility, SS, leakage current) with different channel doping. We could observe that the implant dose influence device characteristic as the implant depth is 200A. As the implant dose increases, the V_{th} increases, the mobility decreases, and S.S increases. The TFTs with channel doping can reduce the photo leakage current. But as the implant depth is 200A, overdose influence device characteristic especially for high V_D and high illumination. We may say that the implant damage the channel as the implant depth is 200A. So the device characteristic is become bad. From Fig.3.6, the sub-threshold swing of TFT with implant depth 550A is better than implant depth 375A in dark. From Fig.3.7, we could observe that the device characteristic of TFT with implant depth 550A is better than implant depth 375A. Fig.3.8 shows the comparison of sub-threshold swing in the TFTs with implant depth 375A and 550A under illumination with increasing brightness. The increasing ratio of sub-threshold swing ΔS.S is defined as (S.SPHOTO/S.SDARK −1), where S.SPHOTO and S.SDARK is the sub-threshold swing of devices at drain voltage of -0.1V and -9V under photo and dark states, respectively. As the brightness of back-light is 5610 nit, the maximum ΔS.S of the TFTs with implant depth 375A and 550A are 74.3% and 43.0% at drain voltage of -0.1V, respectively. As the brightness of back-light is 5610 nit, the maximum ΔS.S of the TFTs with implant depth 375A and 550A are 55.5% and 9.4% at drain voltage of -9V. As the implant depth increase to 550A, there is improvement of variation in sub-threshold swing of poly-Si TFT under illumination is confirmed. The implant dose and implant depth are two conditions for reduce photo leakage current. We found that the depth of implant is the key condition for reduce photo leakage current.

3.2 Results of TFTs with Various Poly-Si Thicknesses

Fig.3.9 shows the top gate Poly TFTs with lightly drain doping (LDD). The channel length of poly-Si TFTs is 6um. The thickness of active layer is 300A, 360A, 430A, 490A, and 550A. These devices were treated by the ion-implant. The implant dose is the same for those TFTs, but the depth of implant dependent on the thickness of active layer. The doping site lies on two-thirds of semiconductor layer. The depth of implant is below half of semiconductor layer.

We measured the dependence of the normalized drain current (NI_D) on the gate voltage (V_G) of poly-Si TFTs with lightly doped drain (LDD) structure as V_D is -0.1 Volt, -5 Volt, -9 Volt, and -15 Volt. And we measured the NI_D-V_G in dark and increasing brightness of back-light (2160, 3100, 4110, 5620 nit). Fig.3.10 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in dark. The thickness of the semiconductor layer affects the threshold voltage (V_{TH}), but has no influence to ON/OFF ratio, ON current, and OFF current. We could observe that as V_D increase from -0.1V to -15V. The TFTs with thin channel also has better threshold voltage. The V_{TH} shifts with thickness of semiconductor layer increases. So we extracted the current at a voltage $|V_G-V_{TH}|$ of 5V in order to compare those TFTs. The dark current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V, are illustrated in Fig.3.11. We could observe that the thickness of semiconductor layer has no influence on OFF current, even operated in linear region or saturation region.

Fig.3.12 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in the brightness of 2160nit. The thickness of the semiconductor layer affects the threshold voltage (V_{TH}), S.S and OFF current. The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 2160nit, are illustrated in Fig.3.13. We could observe that the OFF current is

dependent on thickness of the semiconductor layer. The photo current increases as the thickness of the semiconductor layer increases, and the photo current increases rapidly as V_D is -15V. Because the thickness has influence on S.S, we extracted the increasing ratio of sub-threshold swing ΔS.S. Fig.3.14 shows the comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer. The ΔS.S of the TFTs with the 300A thickness of active layer is 63% and the ΔS.S of the TFTs with the 550A thickness of active layer is 113%.We could observe that ΔS.S increases as the thickness of the semiconductor layer increases. Fig.3.15 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in the brightness of 5620nit. The thickness of the semiconductor layer affects the threshold voltage (V_{TH}), S.S and OFF current. The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 5620nit, are illustrated in Fig.3.16. The photo current increases as the thickness of the semiconductor layer increases. Fig.3.17 shows the comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer. The ΔS.S of the TFTs with the 300A thickness of active layer is 67% and the ΔS.S of the TFTs with the 550A thickness of active layer is 143%. We could observe that ΔS.S increases as the thickness of the semiconductor layer increases.

The OFF current is independent of the active layer thickness in dark measurement. As the hole channel is formed, the current path from drain to source is only near gate. The active layer thickness is independent of current path. Even if the active layer thickness increases, the OFF current does not increase. But we could observe that the OFF current is dependent on thickness of the semiconductor layer in light. The photo current increases as the thickness of the semiconductor layer increases. The active layer is light absorption region. So the absorption region increase s as the thickness of semiconductor layer increases. The more light absorbs in active layer, the more electron-hole pairs generates. The photo current increases as the electron-hole pairs increases.

3.3 Results of TFTs with Implanted the Bottom of Channel

Fig.3.18 shows the top gate Poly TFTs with lightly drain doping (LDD). The channel length of poly-Si TFTs is 6um. The thickness of active layer is 430A, 490A, and 550A. These devices were treated by the ion-implant. The implant dose is 1E12 and the implant depth is 550A for these TFTs. The depth of implant reaches the bottom of semiconductor layer.

We measured the dependence of the normalized drain current (NI_D) on the gate voltage (V_G) of poly-Si TFTs with lightly doped drain (LDD) structure as V_D is -0.1 Volt, -5 Volt, -9 Volt, and -15 Volt. And we measured the NI_D-V_G in dark and increasing brightness of back-light (2160, 3100, 4110, 5620 nit). Fig.3.19 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in dark. The thickness of the semiconductor layer affects the threshold voltage (V_{TH}), but has no influence to ON/OFF ratio, ON current, and OFF current. We could observe that as V_D increase from -0.1V to -15V. The V_{TH} shifts with thickness of semiconductor layer increases. So we extracted the current at a voltage $|V_G-V_{TH}|$ of 5V in order to compare those TFTs. The dark current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V, are illustrated in Fig.3.20. We could observe that the thickness of semiconductor layer has no influence on OFF current, even operated in linear region or saturation region.

Fig.3.21 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in the brightness of 2160nit. The thickness of semiconductor layer has no influence on OFF current and S.S. The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 2160nit, are illustrated in Fig.3.22. We could observe that the photo current is independent on thickness of the semiconductor layer. Fig.3.23 shows the NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V and -15V in the brightness of 5620nit. As the brightness

increase to 5620nits, the thickness of semiconductor layer has no influence on OFF current and S.S either. The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 5620nit, are illustrated in Fig.3.24. We could observe that the photo current is independent on thickness of the semiconductor layer. Fig.3.25 shows the comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer (430A, 490A, 550A) and varied brightness of back-light (2160, 3100, 4110, 5620 nit). The ΔS.S of the TFTs is independent on thickness of the semiconductor layer. AS the brightness increases, the ΔS.S of the TFTs increases slightly. Even if the brightness increases to 5620nit, the ΔS.S of the TFTs with every thickness of active layer is below 60%.

The OFF current is independent of the active layer thickness, whether in dark or light measurement. As the hole channel is formed, the current path from drain to source is only near gate. The active layer thickness is independent of current path. Even if the active layer thickness increases, the OFF current does not increase. But we could observe that the OFF current is independent on thickness of the semiconductor layer in light. The photo current does not increase as the thickness of the semiconductor layer increases. As the back-light is into semiconductor layer, the electron-hole pairs generate most carrier concentration at the bottom of semiconductor layer. The carrier concentration decreases as the depth of the semiconductor layer decreases. There are traps at the bottom of semiconductor layer because the implant depth reaches the bottom of semiconductor layer. These electron-hole pairs can recombine at the glass/poly-Si interface by traps. The trap density of the bottom of active layer is the key condition of the photo leakage current. As more the trap density of the bottom is, the electron-hole pairs can recombine more at the glass/poly-Si interface.

Chapter 4 Poly-Si TFT with Counter-doped Lateral Body Terminal

In this chapter, the research is into the TFTs with lateral body terminal.

4.1 Measurement of Body Current of Poly-Si TFT with Lateral Body Terminal

The devices structures of the poly-Si TFTs with lateral body terminal (LBT TFTs) with varied LBT position are showed in Fig.4.1.There are two kinds of structures of LBT TFTs with varied LBT position. The distance from LBT to n+ region is 1um and 13um. That is to say, for change drain position, the LBT TFTs can be regarded as LBT near source, near drain, and LBT near the middle of channel. For forward bias is applied, the position of LBT is near drain. And for reverse bias is applied, the position of LBT is near source. We measured the dependence of the Drain current (I_D) and LBT current (ABSIB) on the gate voltage (V_G) of LBT poly-Si TFTs with lightly doped drain (LDD) structure in linear region and saturation region. From Fig.4.2, the ABSIB is independent of LBT position in linear region. From Fig4.3, there is a peak of ABSIB when LBT near drain in saturation region. As positive V_G increases, the ABSIB increase rapidly. As V_G increases more, ABSIB decrease rapidly. Fig.4.4 shows only ABSIB-V_G in saturation region, we could observe that there is no ABSIB peak as positive V_G is applied when LBT near source and middle of channel. As forward bias or reverse bias is applied, there is no ABSIB peak when LBT near middle of channel. The ABSIB peak is dependent of LBT position and drain voltage. As TFT operates in saturation region, the high drain voltage is applied. In Fig.4.5, as small V_G and high V_D are applied, there is high electric field in the junction of channel and drain. The excessive holes generated by impact ionization under high electric field of drain. If In conventional short channel polysilicon TFTs, the holes accumulate at the bottom of channel. We could observe that

ABSIB increase rapidly, because the excessive holes inject p+ region (LBT) in LBT TFTs. In Fig.4.6, as V_G increases, the ABSIB decrease rapidly, because of the electric field of drain becomes lower, and impact ionization becomes slightly. We know that the substrate current has direct proportion with electric field (E) and current density (J). As small V_G is applied, the current density is small, and as big V_G is applied, the eclectic field is small. So as V_G becomes half of V_D, the ABSIB is biggest in MOSFEF. Because the channel of TFT is poly-Si which structure is fragile than single crystal, the max ABSIB occurres as V_G is one-third V_D. The ABSIB peak is dependent of the electric field of drain. The peak of ABSIB only appears when LBT near drain in saturation region. This phenomenon can shows that the excessive holes generated by impact ionization under high electric field of drain. The holes accumulate at the bottom of channel near the drain when the size of TFT is big (channel length 30um).

From Fig.4.7, there are two dimensions of LBT TFTs. The width and length of channel of big size TFT are 30 um and 30 um (W/L=30/30). The width and length of channel of small size TFT are 30 um and 6 um (W/L=30/6). The LBT position of both sizes is near n+ region. For forward bias is applied, the position of LBT is near drain. And for reverse bias is applied, the position of LBT is near source. Fig.4.8 shows I_D-V_D of small size TFT which channel length is 6 um as forward bias and reverse bias is applied. We could observe that the on current which as forward bias is applied is lower than reverse bias is applied. This is because that when device turn on, a part of current injects into LBT. As forward bias is applied, the position of LBT is near drain, the electric field between LBT and drain is higher than LBT near source. As LBT near drain, the electric field between LBT and drain region is higher than LBT near source. More current injects into LBT as the position of LBT is near drain. From Fig.4.9 and 4.10, in linear region, there are no difference in NID and ABSIB between forward bias and reverse bias. From Fig.4.11, in saturation region, we could observe that there are ABSIB peak as forward bias and reverse bias is applied. The current which as reverse bias is applied is less than forward bias is applied. As the channel length is short, the holes which

generated by impact ionization under high electric field of drain can through channel to source region. Even LBT is near source, most holes can inject into LBT in short channel LBT TFT. Fig.4.12 shows I_D-V_D of big size TFT which channel length is 30 um as forward bias and reverse bias is applied. We could observe that the on current which as forward bias is applied is also lower than reverse bias is applied. This is the same as small size LBT TFT. From Fig.4.13 and Fig.4.14, in linear region, there are no difference in NID and ABSIB between forward bias and reverse bias. From Fig.4.15, in saturation region, we could observe that there are ABSIB peak only as forward bias is applied. As the channel length is long, the holes which generated by impact ionization cannot through channel to source region. We could see from different sizes LBT TFTs that as the excessive holes generated by impact ionization under high electric field of drain, the holes accumulate at the bottom of channel. As the channel is short, the holes accumulate at the bottom of channel, and holes decease away from drain by recombination. As the channel is long, the holes only accumulate at the bottom of channel near drain.

Even the LBT is not connect fully channel, the hole still inject p+ region. The ABSIB which we observed is truly come from the floating body effect. Then we measured LBT TFTs with forward bias and reverse bias in dark and light. The dependence of the LBT current (ABSIB) and normalize drain current (NID) on the gate voltage (V_G) in linear region and saturation region are shown in Fig.4.16 and Fig.4.17. We could observe that the ABSIB in light is higher than it in dark. From Fig.4.18 and Fig.4.19, the dark current of forward bias is less than reverse bias, but the current is the same in light. We found the LBT TFTs could sense light. In next section, we measured the LBT poly-Si TFTs in dark and irradiated illuminance to analyze the device behavior.

4.2 Photo Characteristics of Poly-Si TFT with Lateral Body Terminal

We measured the LBT poly-Si TFTs which the position of LBT near the n+ region with

no lightly doped drain (LDD) structure in dark and irradiated illuminance. The dependence of the LBT current (ABSIB) on the gate voltage (V_G) with fixed N+ region voltage (V_{SD}) and variations in the LBT voltage (V_B) is shown in Fig.4.20. And we could find that the position of LBT would not influence the tendency of device behavior in Fig.4.21 and Fig.4.22. In Fig.4.23, it is found that for high V_{SD} and high positive or negative V_G, the LBT current (ABSIB) is very high whatever in dark or light. As V_G is high, the LBT current (ABSIB) is independent of illumination, so the current is tunneling current. We could observe two things. First, as the positive V_G is high, the tunneling current is shift with V_B. Second, as the negative V_G is high, the tunneling current is independent of V_B. We thought that the device behavior is come from the L shape p/i/n in LBT TFT. In LBT TFT, source and drain is n+ region, channel is intrinsic region, and LBT is p+ region. In order to explain the device behavior, the energy band of the p/i/n in LBT TFTs is shown in Fig.4.24. In the energy band, we could know that the V_B effects on p+ region, the V_G effects on intrinsic region, and the V_{SD} effects on n+ region.

Fig.4.25 shows the ABSIB-V_G of LBT TFT with fixed V_{SD} and varied V_B in dark. We could explain the device behavior into four regions.

(1) From Fig.4.26, as high positive V_G is applied, almost V_G>10V, the tunneling current is occurred. And the current is shift with V_B. We could explain the device behavior by energy band. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As positive V_G is applied, the energy band of intrinsic region also becomes lower. And as negative V_B is applied, the energy band of p+ region becomes higher. The energy band of p+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the PI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of p+ region to the conduction band of intrinsic region. The tunneling current is shift with V_B, because the energy band of p+ region is controlled by

V_B.

(2) From Fig.4.27, as high negative V_G is applied, almost V_G<-10V, the tunneling current was occurred. And the current is independent of V_B. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As negative V_G is applied, the energy band of intrinsic region becomes higher. And as negative V_B is applied, the energy band of p+ region also becomes higher. The energy band of n+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the NI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of intrinsic region to the conduction band of n+ region. The tunneling current is independent of V_B. We could observe that the tunneling current at high negative V_G is higher than the current at high positive V_G. It is because intrinsic region has more electrons than p+ region.

(3) Fig.4.28 shows that the LBT current is independent of V_B, when small V_G is applied, almost -10V<V_G<5V. Because the current is independent of the energy band of p+ region, the current comes from the NI junction. We supposed that electrons through the NI junction by two mechanisms, trap assisted thermionic and trap assisted tunneling. We measured the device characteristics from 25℃ to 75℃, because the two mechanisms dependent with temperature. The LBT current horizontal increase from 25℃ to 75℃ as small V_G is applied in Fig.4.29. Therefore, this phenomenon can prove our assumption.

(4) From Fig.4.30, as high positive V_G increases, almost 5V<VG<10V, the current decreases rapidly. As positive V_{SD} and V_G are applied, the energy band of n+ region and intrinsic region become lower. When V_G>V_{SD}, the energy band of intrinsic region approach the energy band of p+ region, the electric field across the NI junction becomes lower. Then electrons can't reach n+ region from intrinsic region. Therefore, the electric field across the NI junction becomes lower cause the LBT current decrease rapidly.

Fig.4.31 shows the ABSIB-V_G of LBT TFT with fixed V_{SD} in light. We could explain

the device behavior into six regions.

(1) From Fig.4.32, as small positive V_G is applied, the photo current is like a flat-top. As negative V_B is applied, the energy band of p+ region becomes higher. As positive V_G is applied, the energy band of intrinsic region becomes lower. The photo current generated in the PI junction region, because the electric field was big enough to broke electron-hole pairs which generated by light. The electrons generated migrate toward the channel region, while the holes move toward the p+ region. Although the positive V_{SD} is applied, the energy band of n+ region also becomes lower. Because $V_{SD}>V_G$, the energy band of n+ region decrease more than the energy band of intrinsic region, the electric field in NI junction was big enough to broke electron-hole pairs which generated by light. The photo current also generated in the NI junction region, and the electrons generated migrate toward the n+ region, while the holes move toward the channel region. In brief, there are two junction regions generate photo current.

(2) From Fig.4.33, as positive V_G increase to $V_{SD}=V_G$, the LBT current decreases rapidly. As positive V_G and V_{SD} are applied, the energy band of intrinsic region and n+ region become lower. Because of $V_{SD}=V_G$, the of energy band of n+ region approach the energy band of intrinsic region. The small electric field in NI junction could not break electron-hole pairs which generated by light. The LBT current decreases rapidly, as only PI junction could generate photo current.

(3) From Fig.4.34, as high positive V_G is applied, the tunneling current is occurred. The current is shift with V_B, the same as it in dark. We could explain the device behavior by energy band. As positive V_G and V_{SD} are applied, the energy band of intrinsic region and n+ region become lower. And as negative V_B is applied, the energy band of p+ region becomes higher. The energy band of p+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the PI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very

steep. Therefore, electrons can tunnel from the valence band of p+ region to the conduction band of intrinsic region. The tunneling current is shift with V_B, because the energy band of p+ region is controlled by V_B.

(4) From Fig.4.35, as small negative V_G is applied, the same as small V_G positive is applied, photocurrent like a flat-top. As negative V_B and V_G are applied, the energy band of p+ region and intrinsic region become higher. Because $V_B<V_G$, the energy band of p+ region increases more than the energy band of intrinsic region, the electric field in PI junction was big enough to broke electron-hole pairs which generated by light. And as positive V_{SD} is applied, the energy band of n+ region also becomes lower. The photo current generated in the NI junction region. There are two junction regions generate photo current.

(5) From Fig.4.36, as negative V_G decreases to $V_B=V_G$, the current decreases rapidly. As positive V_B and V_G are applied, the energy band of intrinsic region and n+ region become lower. Because of $V_B=V_G$, the of energy band of p+ region approach the energy band of intrinsic region. The small electric field in PI junction could not break electron-hole pairs which generated by light. The LBT current decreases rapidly, as only NI junction could generate photo current.

(6) From Fig.4.37, as high negative V_G is applied, the tunneling current is occurred, and the current is independent of V_B. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As negative V_G and V_B are applied, the energy band of intrinsic region and p+ region become higher. The energy band of n+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the NI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of intrinsic region to the conduction band of n+ region. The tunneling current is independent of V_B. We could observe that the tunneling current at high negative V_G is higher than the current at high positive V_G. It is because intrinsic region has more electrons than p+ region.

Fig.4.38 shows the ABSIB-V_G of LBT TFT with fixed V_B and varied V_{SD} in Dark. We could explain the device behavior into four regions.

(1) From Fig.4.39, as high positive V_G is applied, the tunneling current is occurred. And the current is independent of V_{SD}. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As positive V_G is applied, the energy band of intrinsic region also becomes lower. And as negative V_B is applied, the energy band of p+ region becomes higher. The energy band of p+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the PI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of p+ region to the conduction band of intrinsic region. The tunneling current is independent of V_{SD}.

(2) From Fig.4.40, as high negative V_G is applied, the tunneling current is occurred. And the current is shift with V_{SD}. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As negative V_G is applied, the energy band of intrinsic region becomes higher. And as negative V_B is applied, the energy band of p+ region also becomes higher. The energy band of n+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the NI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of intrinsic region to the conduction band of n+ region. The tunneling current shifts with V_{SD}. We could observe that the tunneling current at high negative V_G is higher than the current at high positive V_G. It is because intrinsic region has more electrons than p+ region.

(3) Fig.4.41 shows that the LBT current has less increment as V_{SD} increases, when small V_G is applied. The electrons through the NI junction by two mechanisms, trap assisted thermionic and trap assisted tunneling. When V_{SD} increases, the electric field across NI junction becomes higher and the LBT current has less increment.

(4) From Fig.4.42, as positive V_G increases, the current decreases rapidly. And the current shifts with V_{SD}. As positive V_{SD} and V_G are applied, the energy band of n+ region and intrinsic region become lower. When $V_G > V_{SD}$, the energy band of intrinsic region approach the energy band of p+ region, the electric field across the NI junction becomes lower. Then electrons can't reach n+ region from intrinsic region. Therefore, the electric field across the NI junction becomes lower cause the LBT current decrease rapidly. As the smaller V_{SD} is applied, the smaller V_G of LBT current decrease rapidly.

Fig.4.43 shows the ABSIB-V_G of LBT TFT with fixed V_B and varied V_{SD} in light. We could explain the device behavior into five regions.

(1) From Fig.4.44, as small V_G is applied, the photo current likes a flat-top. The photo current generated in the PI and NI junction region, because the electric field was big enough to broke electron-hole pairs which generated by light. In PI junction, the electrons generated migrate toward the channel region, while the holes move toward the p+ region. In NI junction, the electrons generated migrate toward the n+ region, while the holes move toward the channel region. In brief, there are two junction regions generate photo current.

(2) From Fig.4.45, as positive V_G increase, the photo current decrease rapidly. And the current shifts with V_{SD}. As higher V_{SD} is applied, the current decrease rapidly by higher V_G. As positive V_G and V_{SD} are applied, the energy band of intrinsic region and n+ region become lower. Because of $V_{SD}=V_G$, the of energy band of n+ region approach the energy band of intrinsic region. The small electric field in NI junction could not break electron-hole pairs which generated by light. The LBT current decreases rapidly, as only PI junction could generate photo current.

(3) From Fig.4.46, as high positive V_G is applied, the tunneling current was occurred. And the current is independent of V_{SD}. As positive V_{SD} and V_G are applied, the energy band of n+ region and intrinsic region also become lower. And as negative V_B is applied, the energy band of p+ region becomes higher. The energy band of p+ region is apart from it of

intrinsic region, so the depletion region is formed in the vicinity of the PI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of p+ region to the conduction band of intrinsic region. The tunneling current is independent of V_{SD}.

(4) From Fig.4.47, as negative V_G increases, until $V_G=V_B$, the photo current decreases rapidly, and the current is independent of V_{SD}. As positive V_B and V_G are applied, the energy band of intrinsic region and n+ region become lower. Because of $V_B=V_G$, the of energy band of p+ region approach the energy band of intrinsic region. The small electric field in PI junction could not break electron-hole pairs which generated by light. The LBT current decreases rapidly, as only NI junction could generate photo current.

(5) From Fig.4.48, as high negative V_G is applied, the tunneling current is occurred. And the current is shift with V_{SD}. As positive V_{SD} is applied, the energy band of n+ region becomes lower. As negative V_G and V_B are applied, the energy band of intrinsic region and p+ region become higher. The energy band of n+ region is apart from it of intrinsic region, so the depletion region is formed in the vicinity of the NI junction. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of intrinsic region to the conduction band of n+ region. The tunneling current shifts with V_{SD} in light.

Then we measured the LBT poly-Si TFTs which the position of LBT near the n+ region with lightly doped drain (LDD) structure in dark and irradiated illuminance. The dependence of the LBT current (ABSIB) on the gate voltage (V_G) with fixed N+ region voltage (V_{SD}) and variations in the LBT voltage (V_B) is shown in Fig.4.49. From Fig.4.50, as high positive V_G is applied, the tunneling current was occurred. As the depletion layer is formed and the electric field is high, the energy band of depletion layer becomes very steep. Therefore, electrons can tunnel from the valence band of p+ region to the conduction band of intrinsic region. But as high negative V_G is applied, the tunneling current isn't occurred. This is because that the most

of high V_G is at LDD region. The electric field isn't big enough to cause the tunneling current.

Fig.4.51 shows that I_D-V_G of linear region of LBT TFT in dark and light. The drain current increases 2 order from dark to 5620nits. Fig.4.52 shows that ABSIB-V_G of LBT TFT in dark and light. As V_{SD}=0V, V_B=-2V, and small V_G is applied, the LBT current increases 3 order from dark to 5620nits. This new structure TFT can sense light, because there is PIN of L shape in LBT TFT. Since the device structure and layout are compatible with LTPS TFTs technology and no extra mask is needed. The LBT TFTs are good dual purpose TFTs.

Chapter 5 Conclusion

5.1 Polycrystalline Thin Film Transistor with Different Active Layer

The Polycrystalline TFT with different active layer has been demonstrated in this thesis. Since the light emitted from back-light is mainly absorbed at the interface between the poly-Si layer and the buffer layer, plenty of electron-hole pairs are generated in the bottom of poly-Si film. Furthermore, the energy-band structure of Si material is indirect bandgap. The excess electron-hole pairs induced by the absorption of light would not be recombined from band to band directly due to the momentum conservation principle. The numerous electron-hole pairs are accumulated in the bottom of poly-Si layer. It follows that the excess holes flow to the drain under the negative drain bias for p-channel devices, generating the photo leakage current. These electron-hole pairs either recombine at the glass/poly-Si interface or diffuse to the gate SiO_2/poly-Si interface and recombine there. Because the implant can increase trap density, the electron-hole pairs can recombine by the traps. The implant dose and implant depth are two conditions for reduce photo leakage current. The implantation damage the channel as the implant depth is above half of active layer. So the device characteristic is become badly. We found that the depth of implant is the key condition for reduce photo leakage current.

As the hole channel is formed, the current path from drain to source is only near gate. The active layer thickness is independent of current path. Even if the active layer thickness increases, the OFF current does not increase. The photo current increases as the thickness of the semiconductor layer increases. The active layer is light absorption region. So the absorption region increase s as the thickness of semiconductor layer increases. The more light absorbs in active layer, the more electron-hole pairs generates. The photo current increases as the electron-hole pairs increases.

The OFF current is independent on thickness of the semiconductor layer in light as the

TFTs are implanted channel bottom. As the back-light is into semiconductor layer, the electron-hole pairs generate most carrier concentration at the bottom of semiconductor layer. The carrier concentration decreases as the depth of the semiconductor layer decreases. There are traps at the bottom of semiconductor layer because the implant depth reaches the bottom of semiconductor layer. These electron-hole pairs can recombine at the glass/poly-Si interface by traps. The trap density of the bottom of active layer is the key condition of the photo leakage current. As more the trap density of the bottom is, the electron-hole pairs can recombine more at the glass/poly-Si interface.

5.2 Poly-Si TFT with Counter-doped Lateral Body Terminal

As we measured the LBT TFTs with different LBT position, we could observe that the ABSIB peak is dependent of LBT position and drain voltage. The peak of ABSIB only appears when LBT near drain in saturation region. This phenomenon can shows that the excessive holes generated by impact ionization under high electric field of drain. The holes accumulate at the bottom of channel near the drain. We could observe that ABSIB increase rapidly, because the excessive holes inject p+ region (LBT) in LBT TFTs. As V_G increases, the ABSIB decrease rapidly, because of the electric field of drain becomes lower, and impact ionization becomes slightly. We could see from LBT TFTs with different channel length that as the excessive holes generated by impact ionization under high electric field of drain, the holes accumulate at the bottom of channel. As the channel is short, the holes accumulate at the bottom of channel, and holes decease away from drain by recombination. As the channel is long, the holes only accumulate at the bottom of channel near drain.

We found the LBT TFTs could sense light, so we measured the LBT poly-Si TFTs in dark and irradiated illuminance to analyze the device behavior. We thought that the device behavior is come from the L shape p/i/n in LBT TFT. In LBT TFT, source and drain is n+ region, channel is intrinsic region, and LBT is p+ region. In order to explain the device

behavior, the energy band of the p/i/n in LBT TFTs is proposed. In the energy band, we could know that the V_B effects on p+ region, the V_G effects on intrinsic region, and the V_{SD} effects on n+ region. The energy band of the p/i/n could explain the device behavior in dark and light. As V_{SD}=0V, V_B=-2V, and small V_G is applied, the LBT current increases 3 order from dark to 5620nits. This new structure TFT can sense light, because there is PIN of L shape in LBT TFT. Since the device structure and layout are compatible with LTPS TFTs technology and no extra mask is needed. AS LBT TFTs using the same fabrication processes as LTPS-TFTs, the LBT TFTs are good dual purpose TFTs.

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Figure Caption

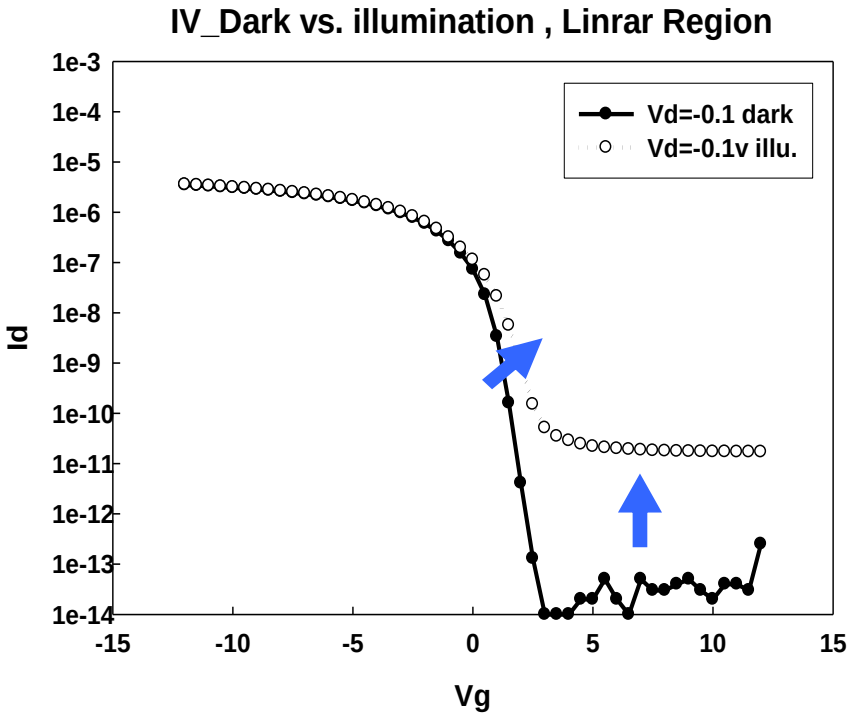


Fig.1. 1 Id_Vg Curve of Dark and Illuminated at linear region.

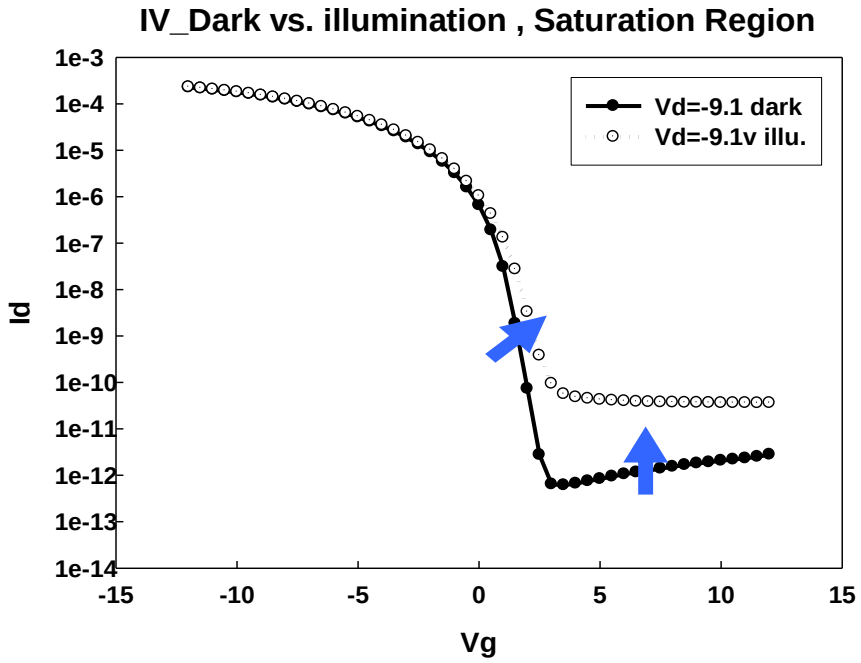


Fig.1. 2 Id_Vg Curve of Dark and Illuminated at saturation region.

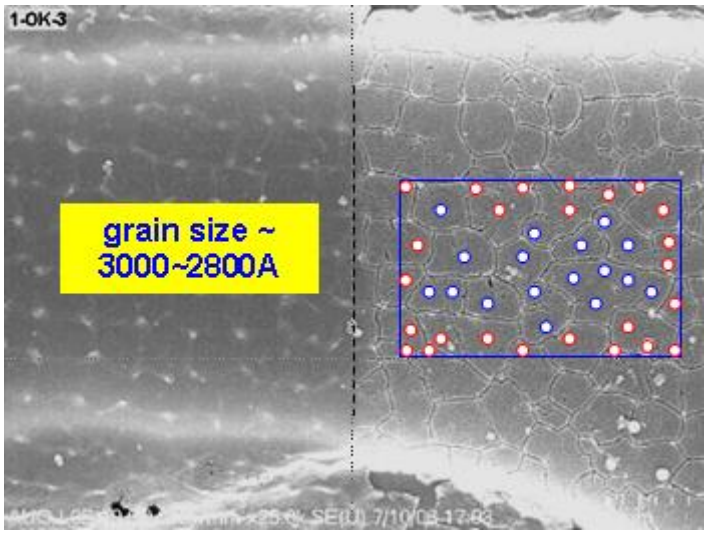


Fig.2. 1 SEM of Grain Size

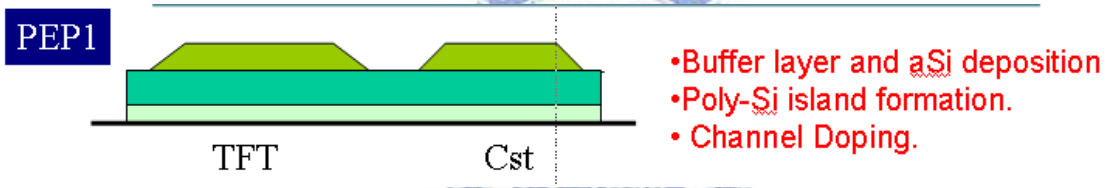


Fig.2. 2 Pep1 Process Flow of LTPS PMOS TFT

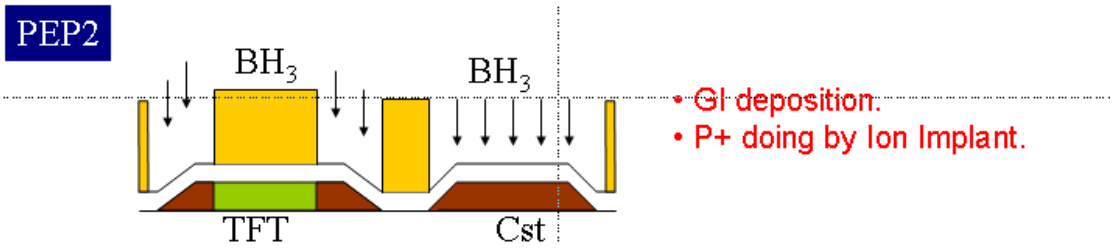


Fig.2. 3 Pep2 Process Flow of LTPS PMOS TFT

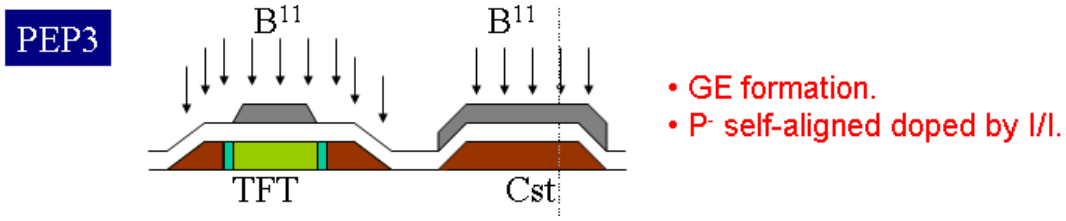


Fig.2. 4 Pep3 Process Flow of LTPS PMOS TFT

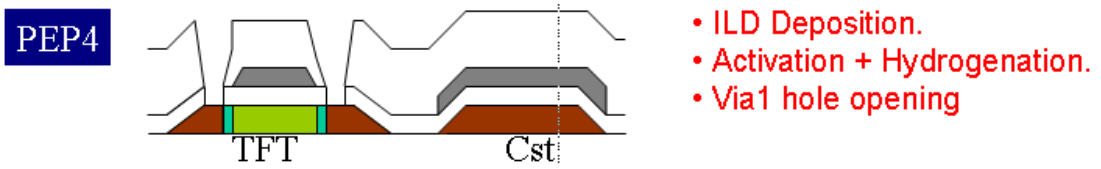


Fig.2. 5 Pep4 Process Flow of LTPS PMOS TFT

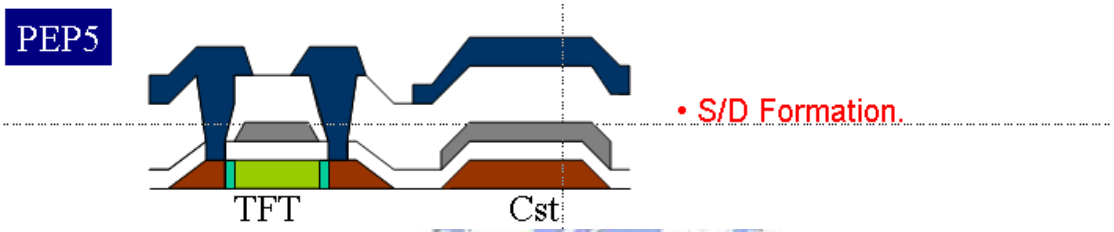


Fig.2. 6 Pep5 Process Flow of LTPS PMOS TFT

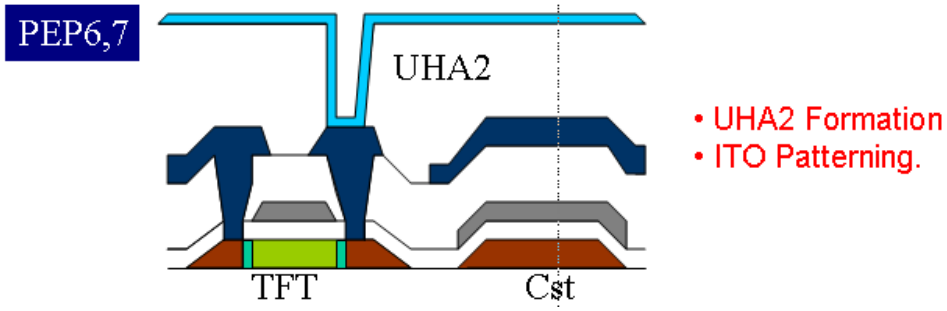


Fig.2. 7 Pep6,7 Process Flow of LTPS PMOS TFT

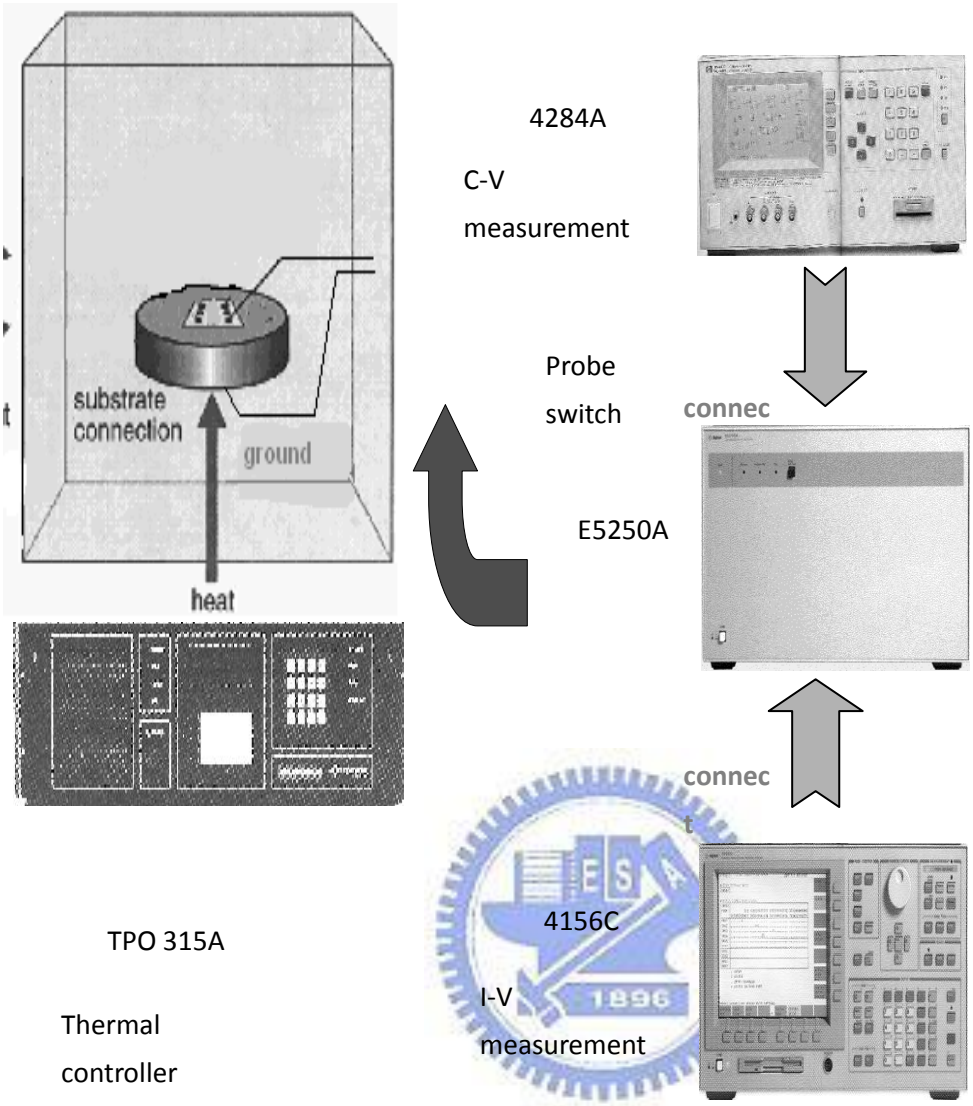


Fig.2. 8 I-V instruments set up in the laboratory.

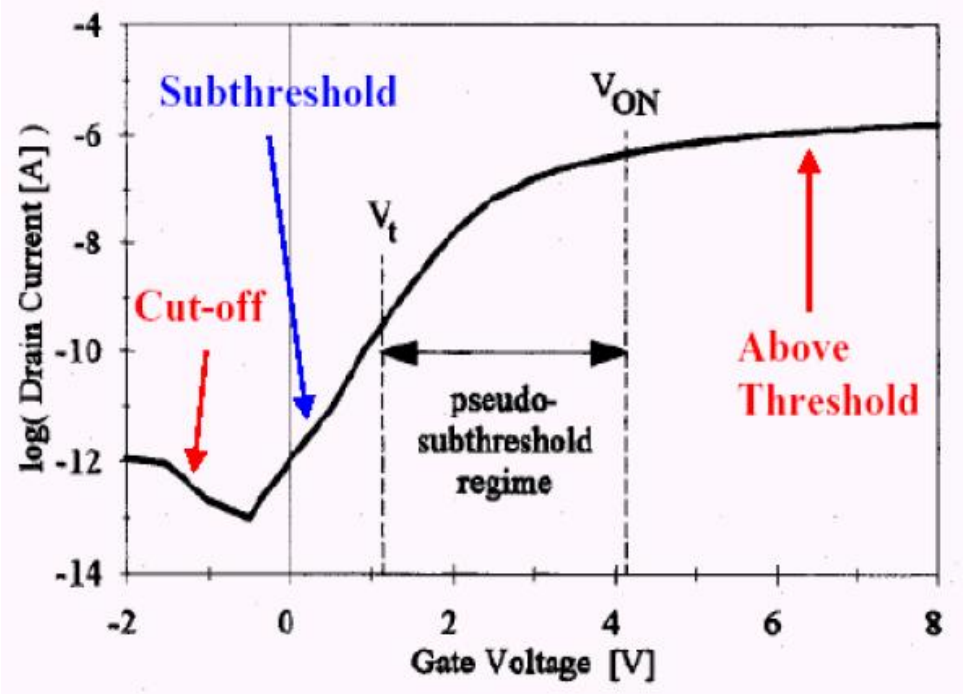


Fig.2. 9 Poly TFT Transfer Characteristics (Id_Vg Curve)

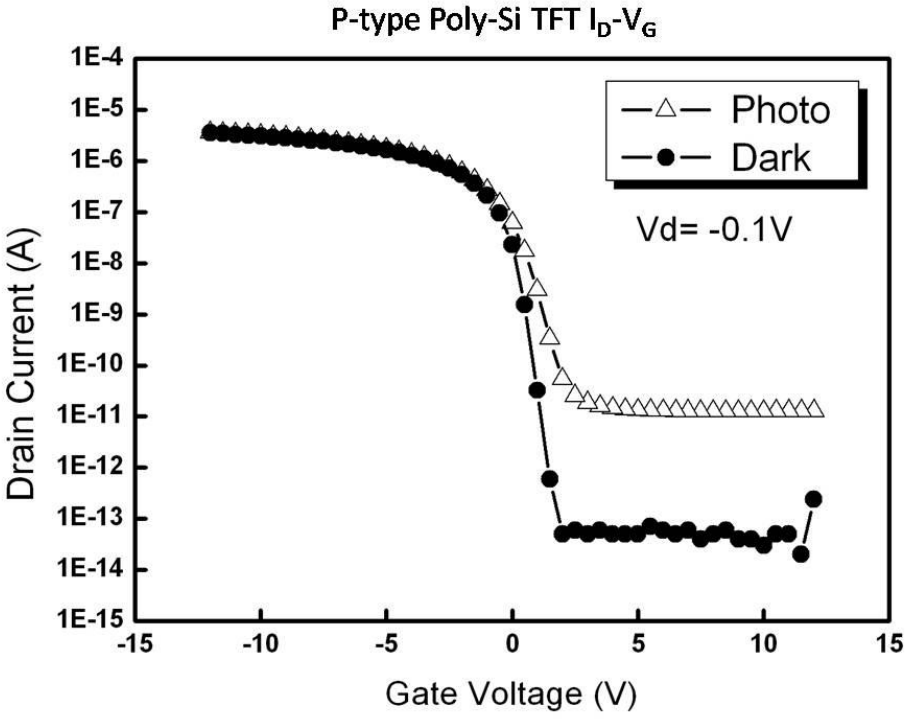


Fig.3. 1 The I_D-V_G of P-type TFT under dark state and light state.

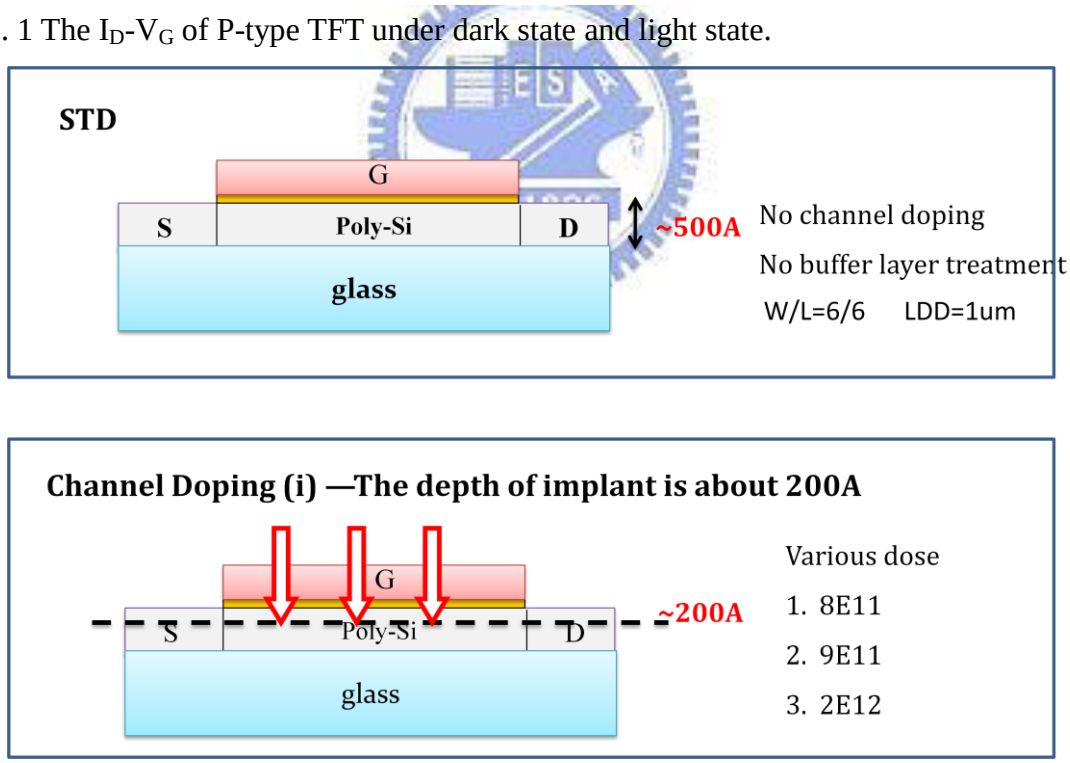


Fig.3. 2 The structure of TFT with implanted the active layer experiment. The STD is conventional TFT with LDD and no channel doping. The depth of implant of channel doping TFTs is about 200A with various doses 8E11, 9E11, and 2E12.

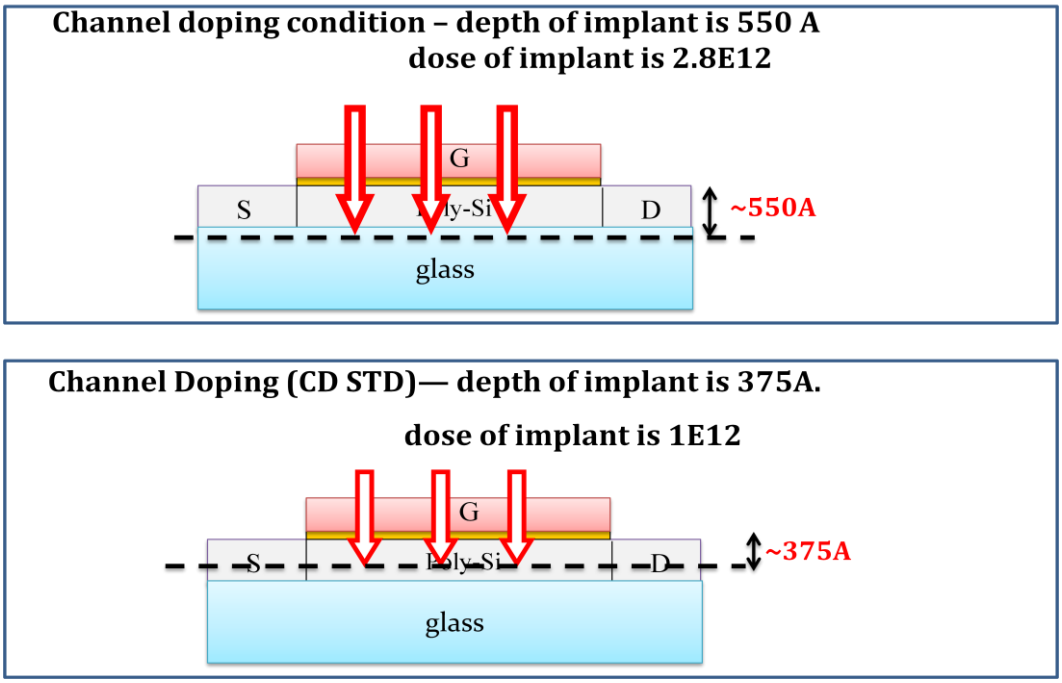


Fig.3. 3 The structure of TFT with implanted the active layer experiment. Depth of implant is 550 A and dose of implant is 2.8E12. Depth of implant is 375A and dose of implant is 1E12.

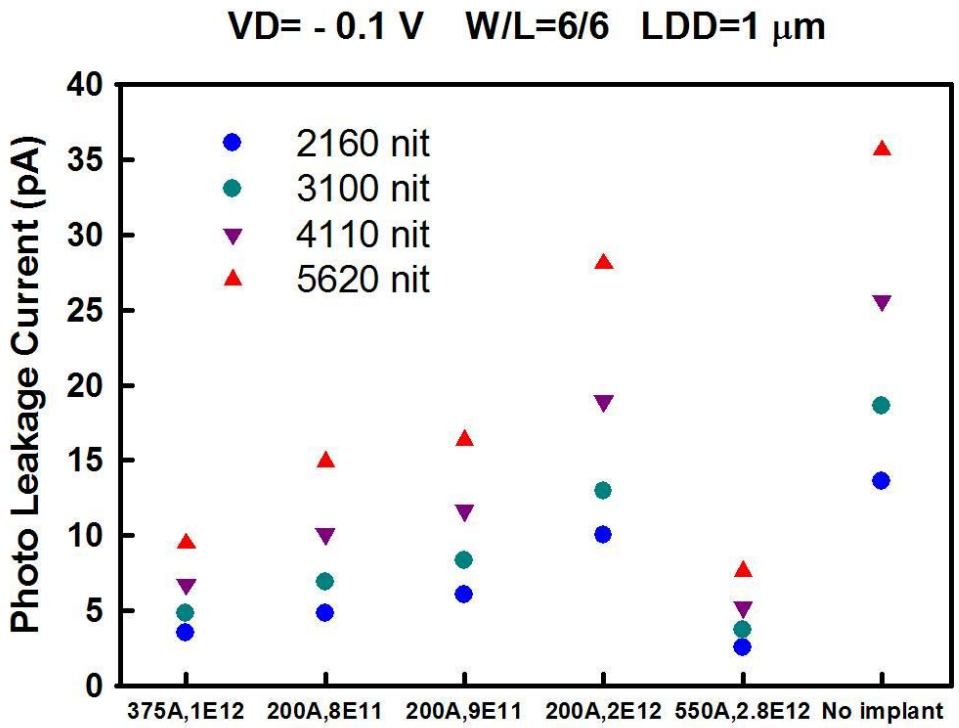


Fig.3. 4 The photo leakage current of TFT with implanted the active layer experiment as V_D=-0.1V. The photo leakage current is extracted as V_G-V_T=7V.

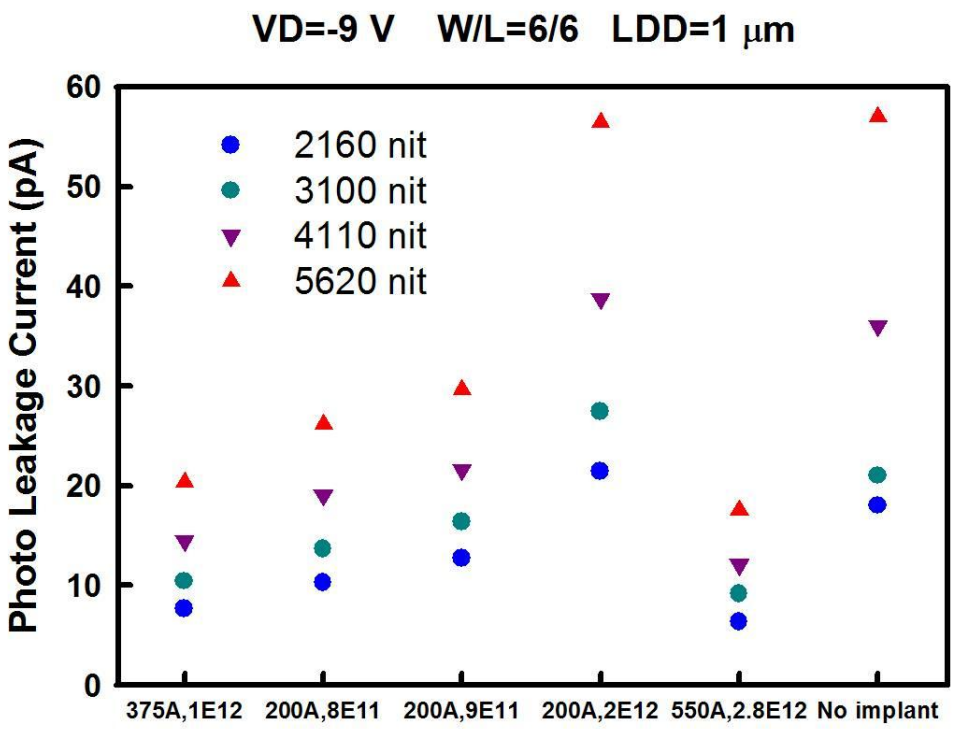


Fig.3. 5The photo leakage current of TFT with implanted t he active layer experiment as V_D=-9V.

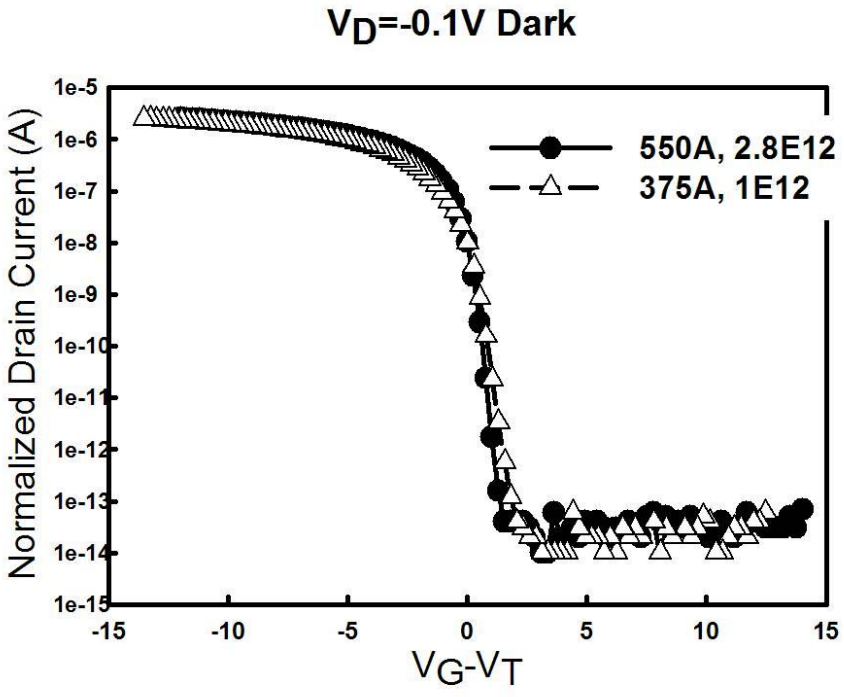
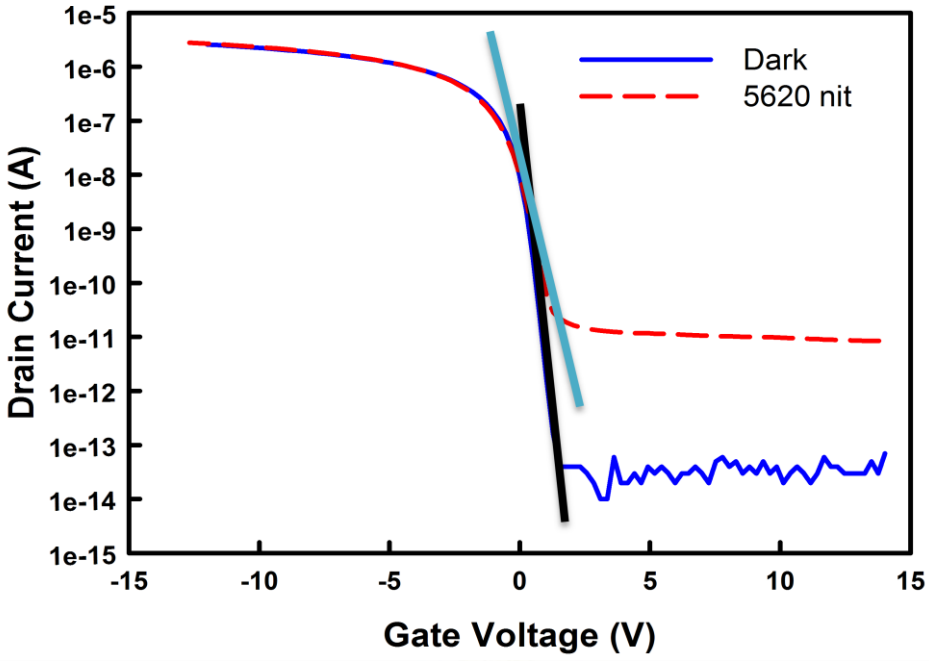
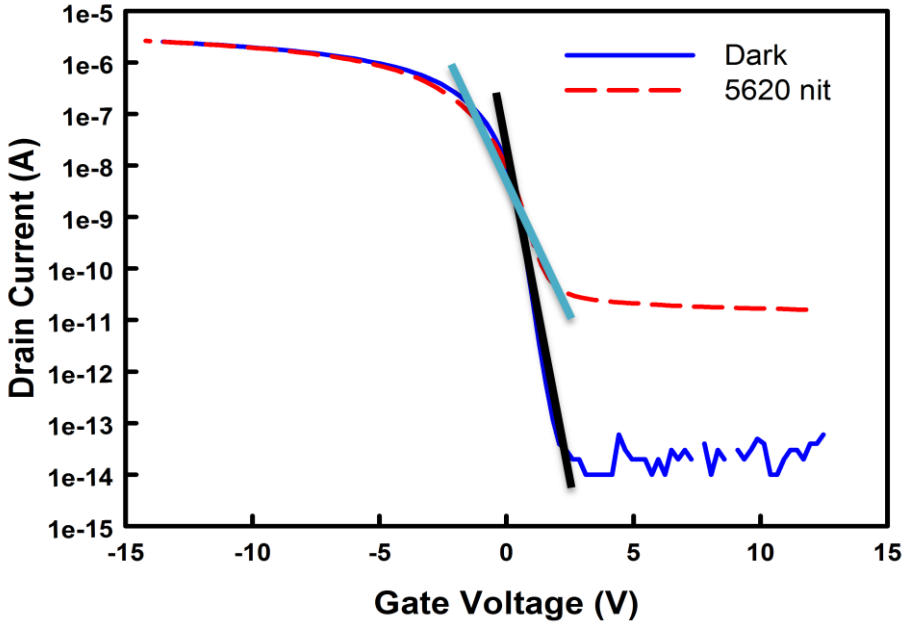


Fig.3. 6 The I_D-V_G of TFTs under dark state as V_D=-0.1V. The swing of TFT with implanted the bottom of active layer is better.

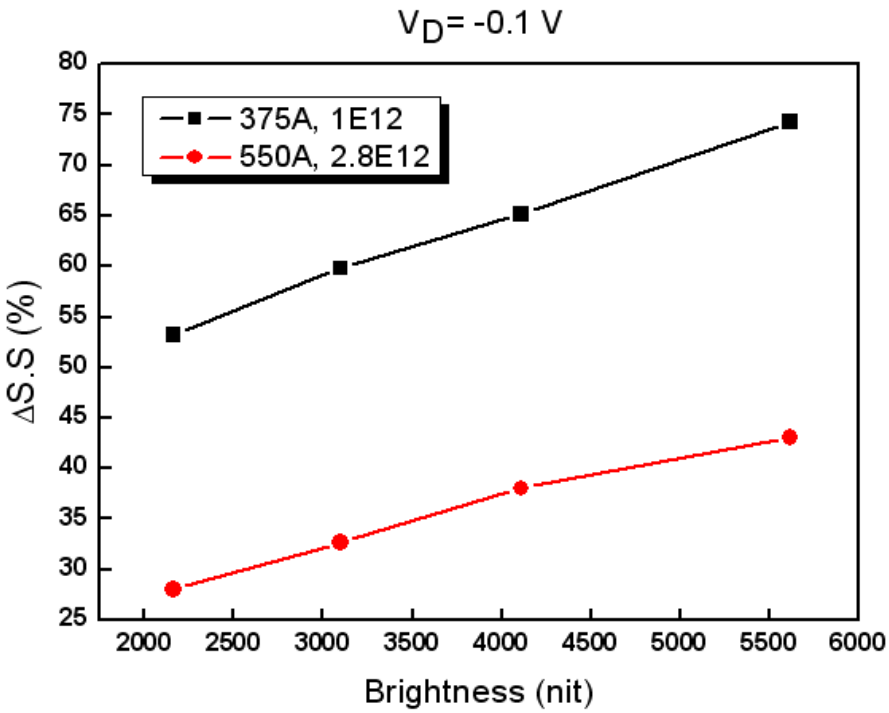


(a)

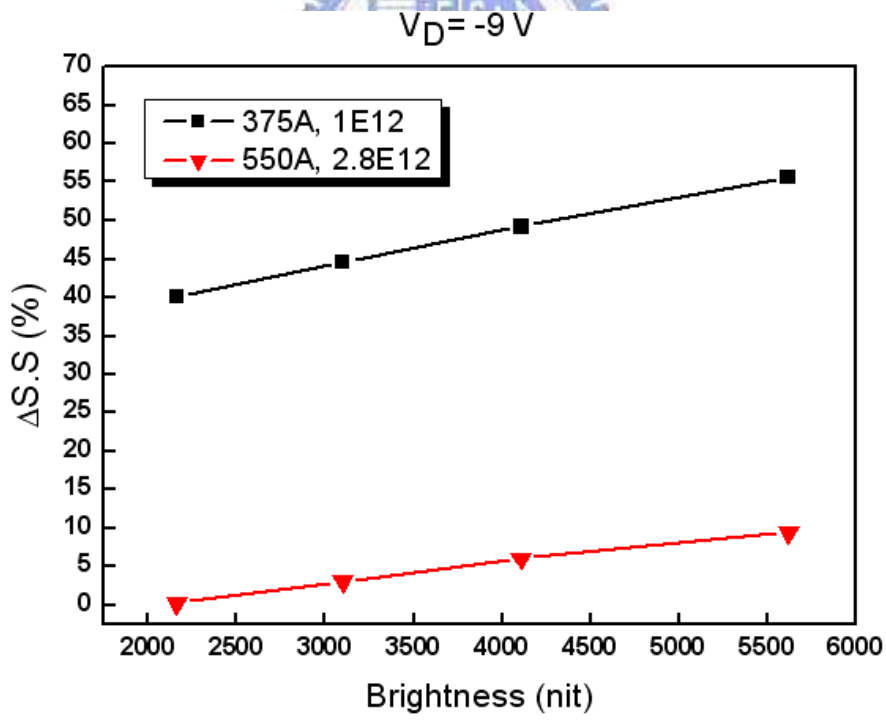


(b)

Fig.3. 7 (a) The I_D-V_G of TFT with channel doping STD. (b) The I_D-V_G of TFT with implanted the bottom of active layer. The ∆ SS of the TFT with implanted the bottom of active layer is better.



(a)



(b)

Fig.3. 8 (a)The ΔSS of TFTs with varied backlight brightness as drain voltage is -0.1V. (b) The ΔSS of TFTs with varied backlight brightness as drain voltage is -9V

.

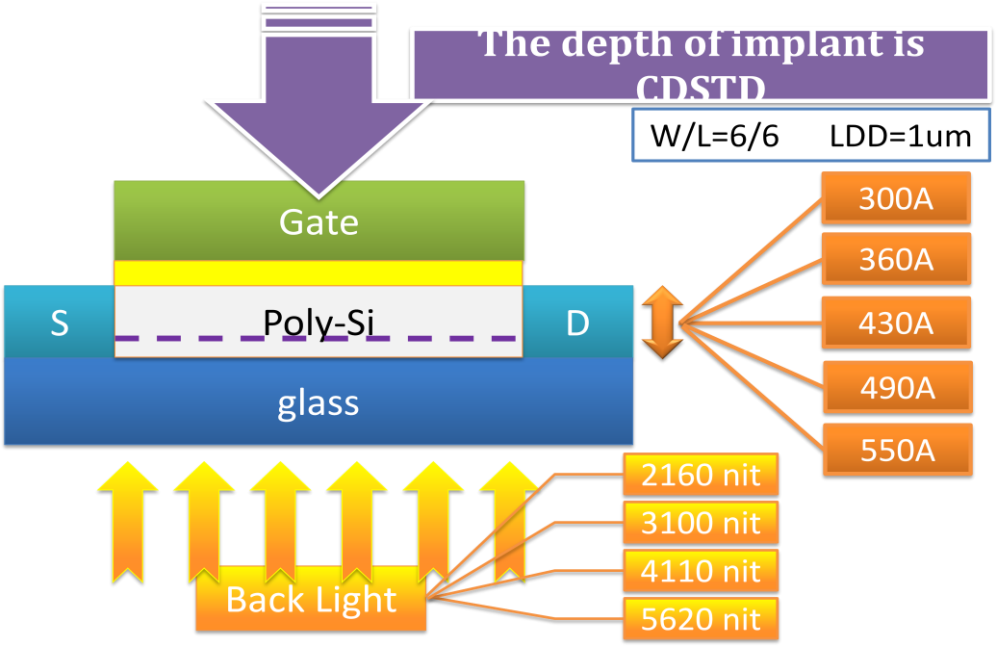
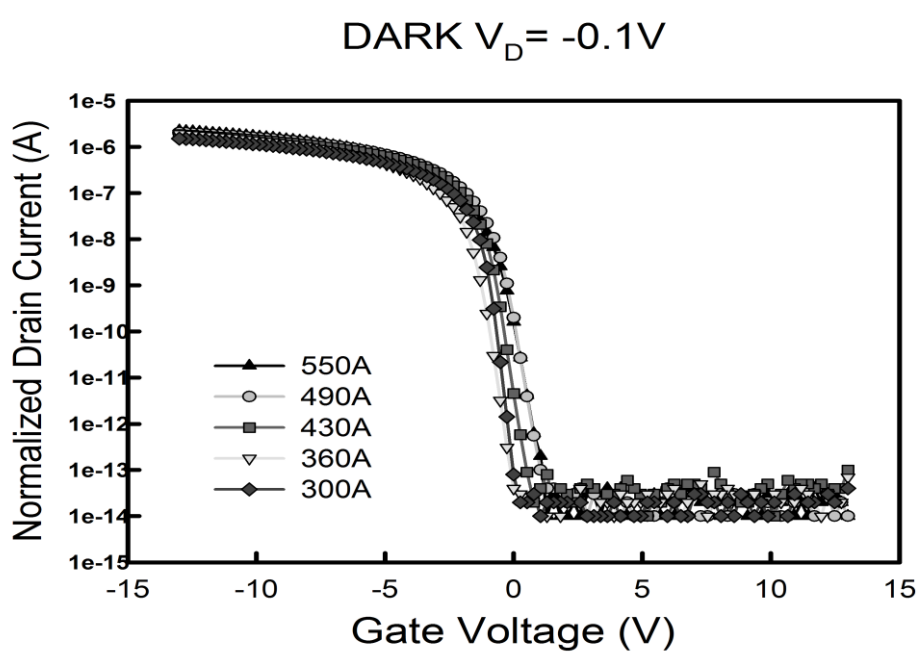
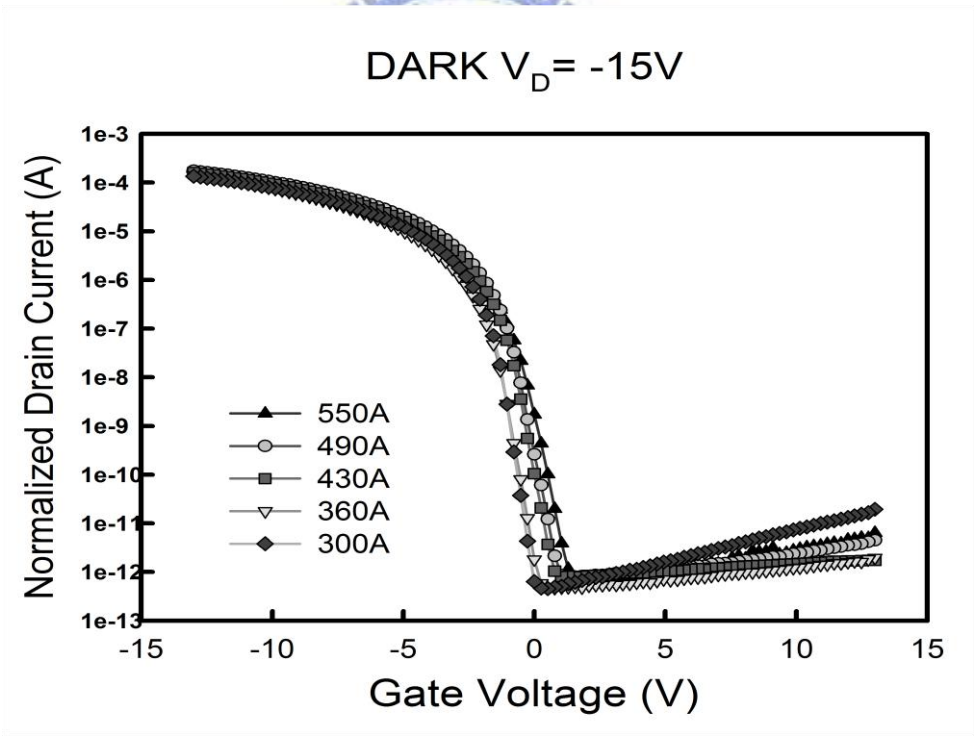


Fig.3. 9 The experiment of CDSTD TFTs with various Poly-Si Thicknesses. The thickness of active layer is 300A, 360A, 430A, 490A, and 550A. The doping site lies on two-thirds of semiconductor layer. The depth of implant is below half of semiconductor layer.



(a)



(b)

Fig.3. 10 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in dark. (b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in dark.

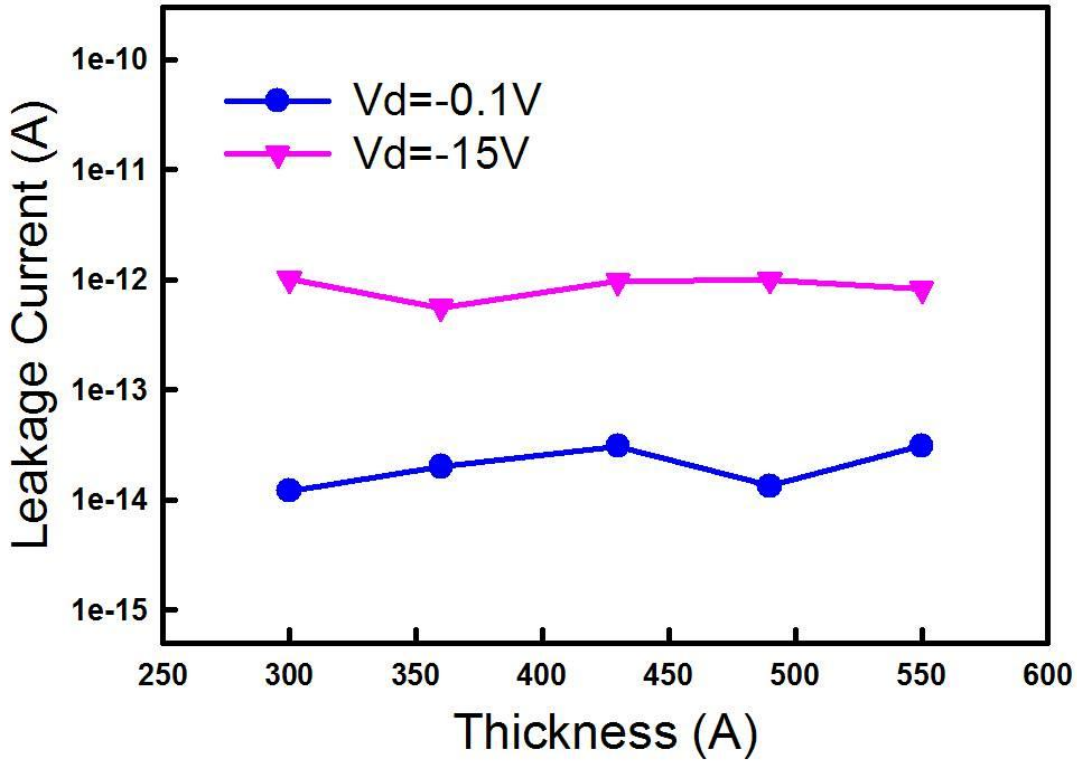
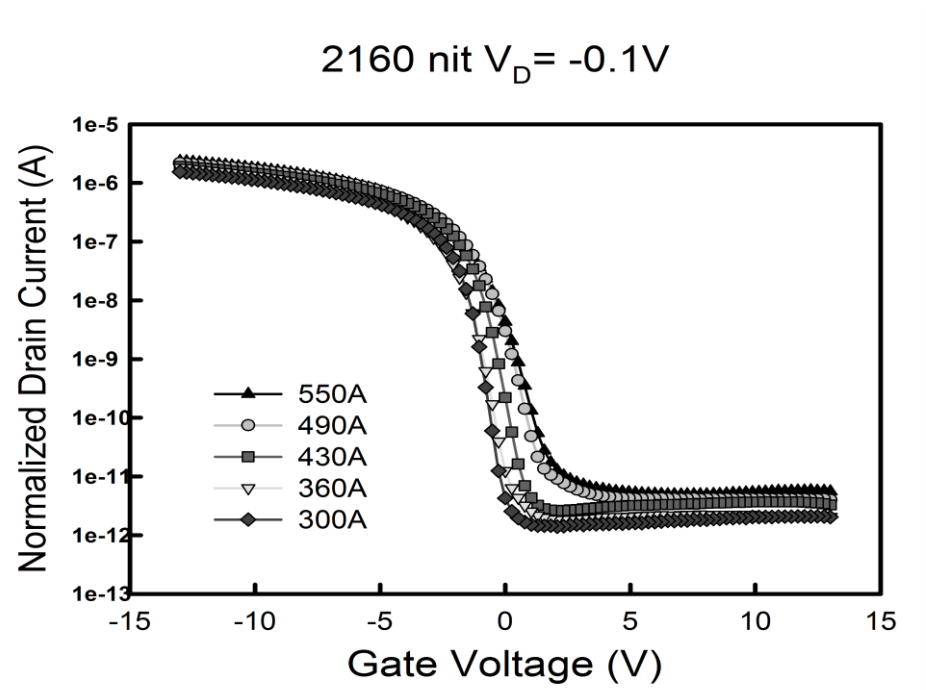
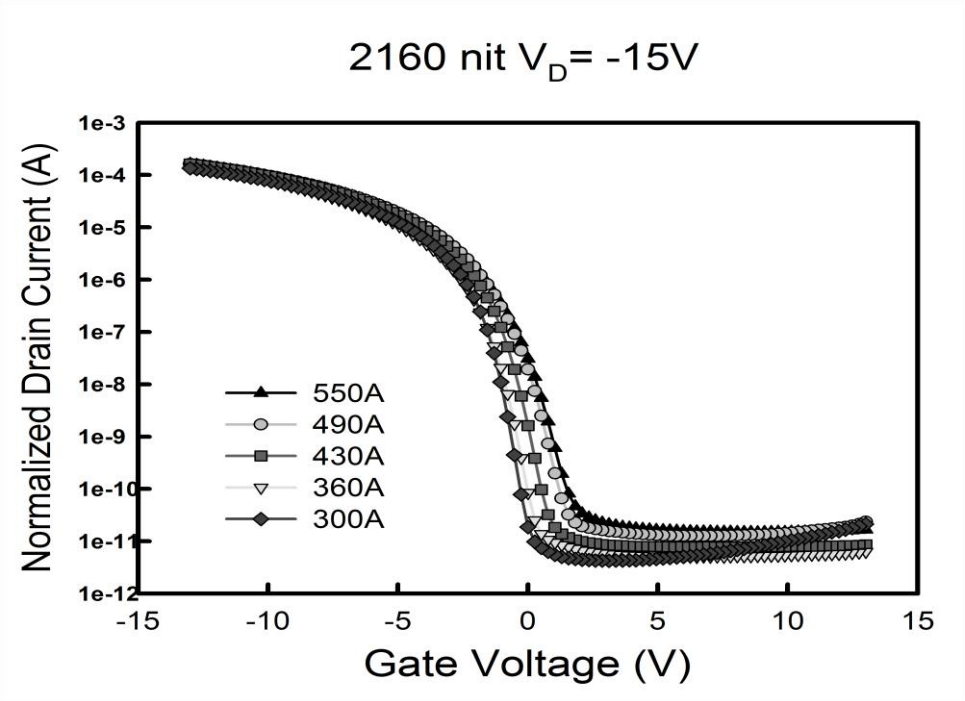


Fig.3. 11 The dark current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V.



(a)



(b)

Fig.3. 12 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in the brightness of 2160nit.(b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in the brightness of 2160nit.

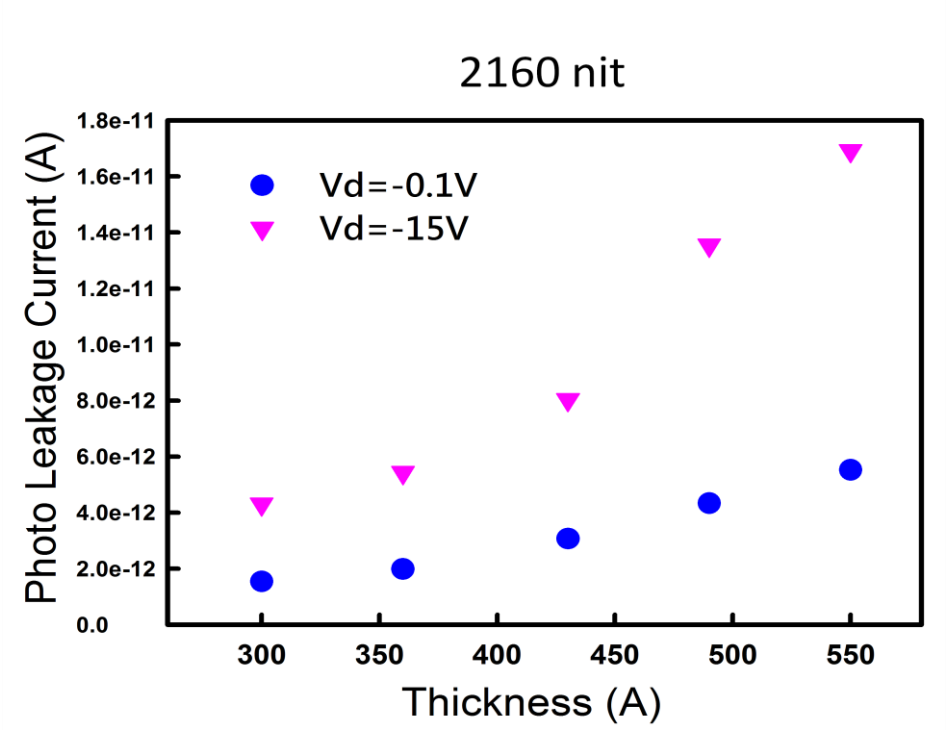


Fig.3. 13 The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 2160nit.

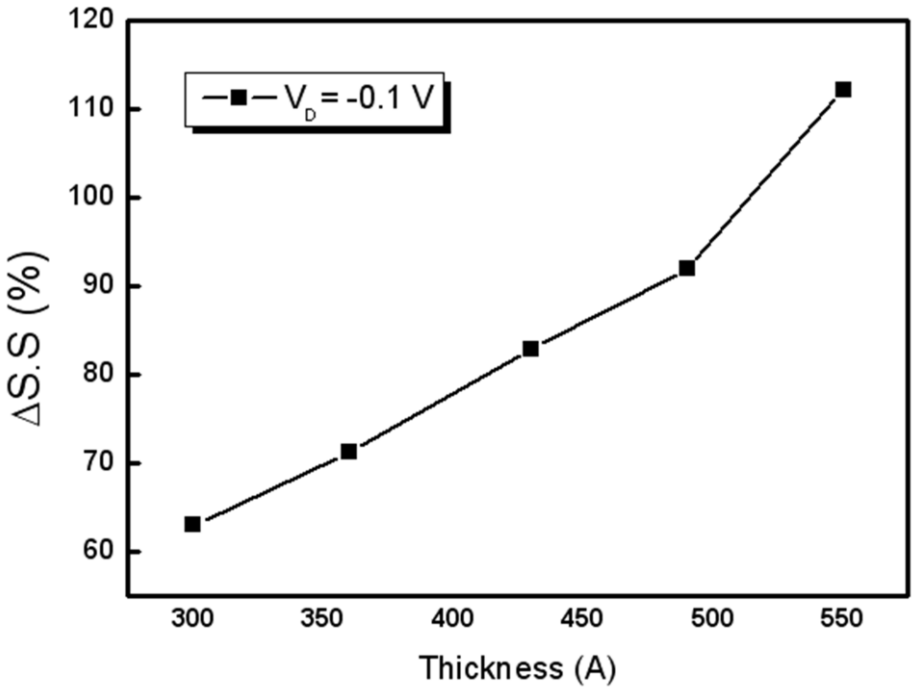
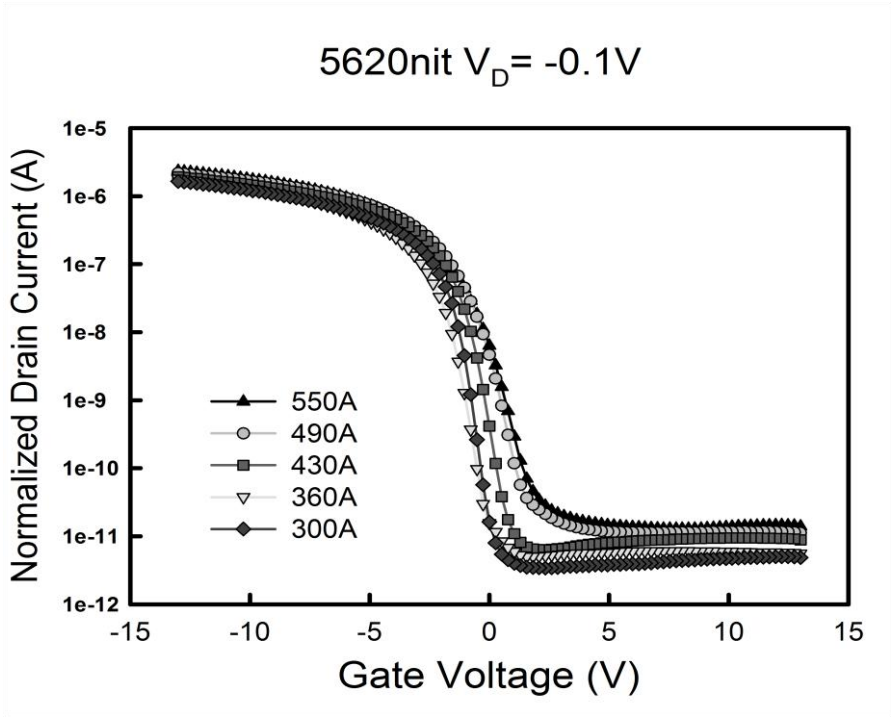
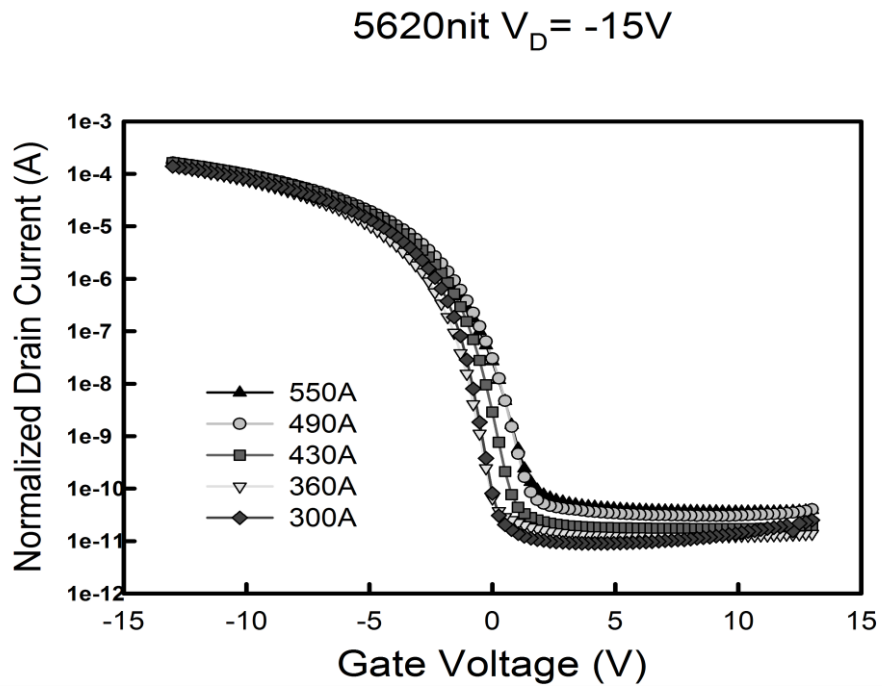


Fig.3. 14 The comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer the brightness of 2160 nit.



(a)



(b)

Fig.3. 15 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in the brightness of 5620nit.(b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in the brightness of 5620nit.

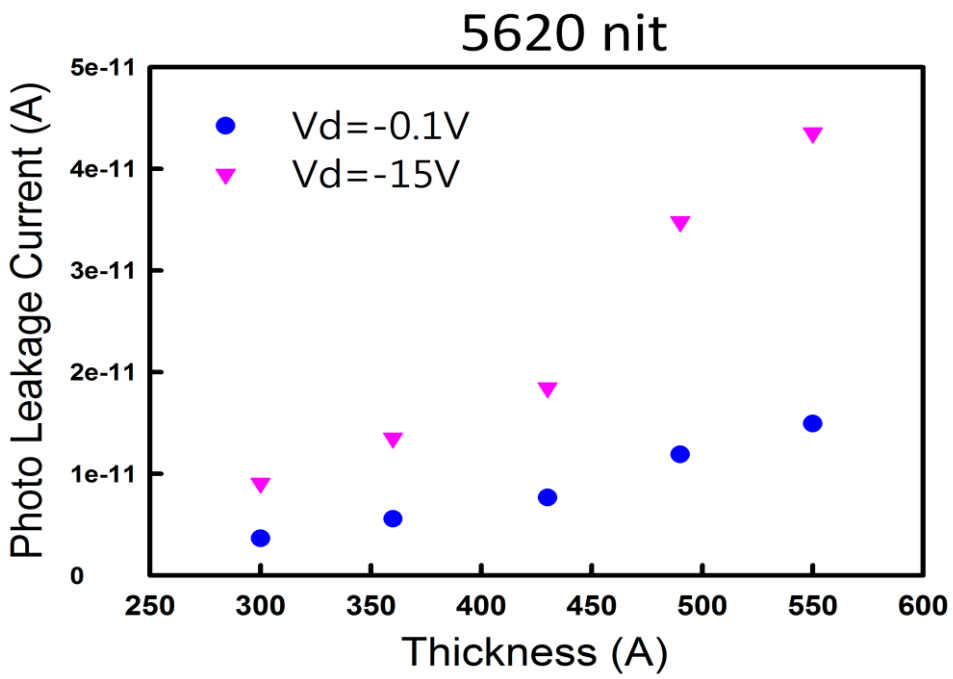


Fig.3. 16 The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 5620nit.

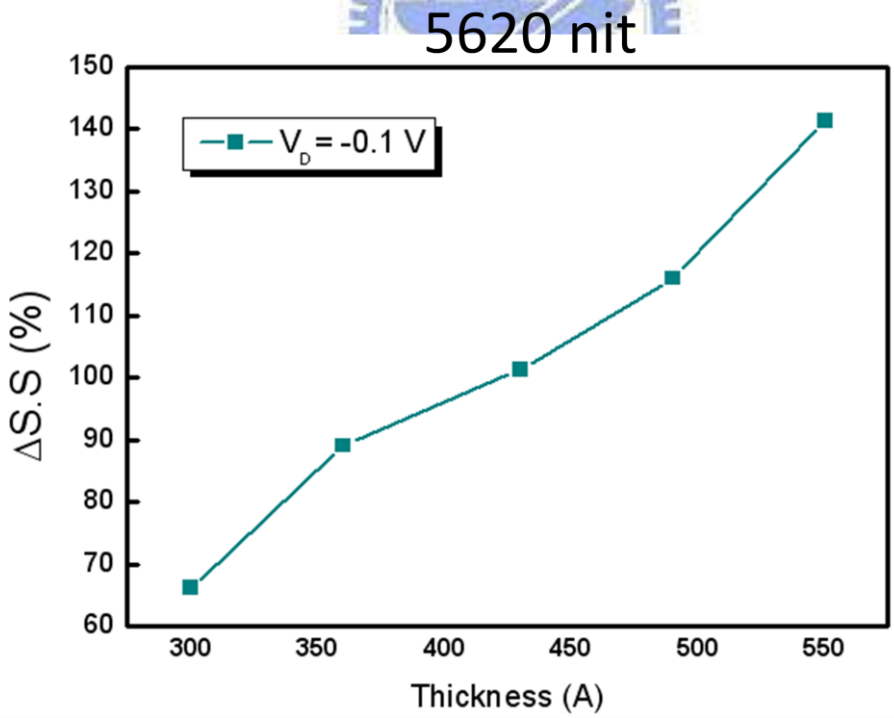


Fig.3. 17 The comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer in the brightness of 5620nit.

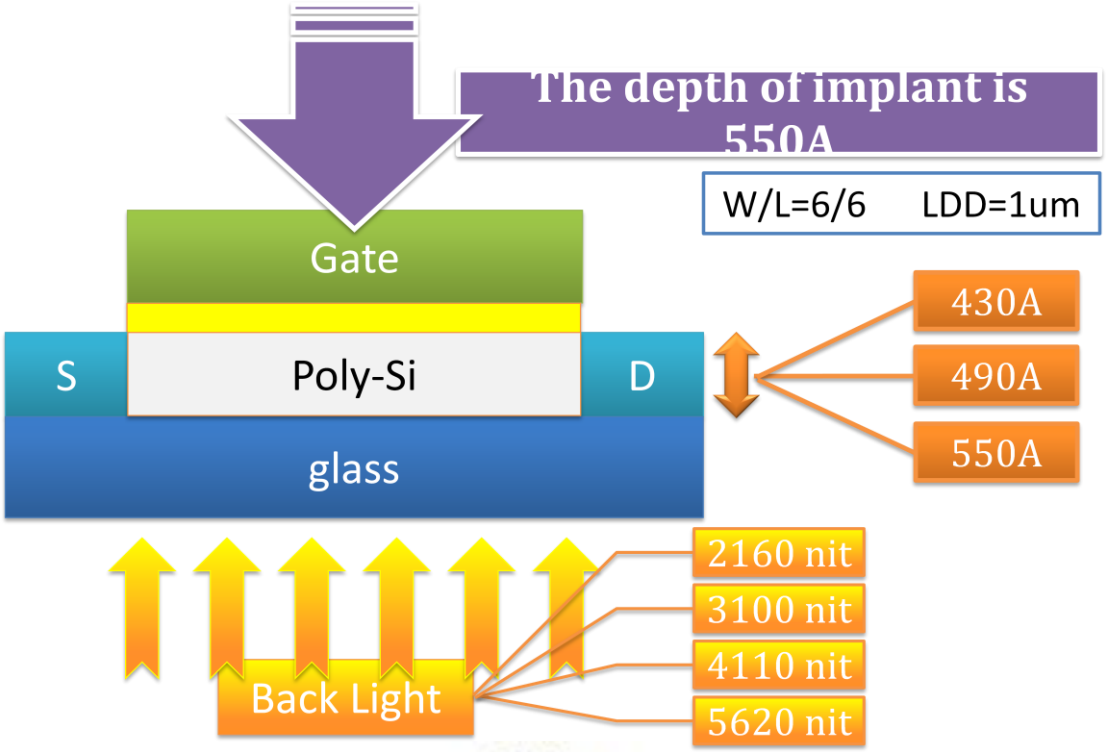
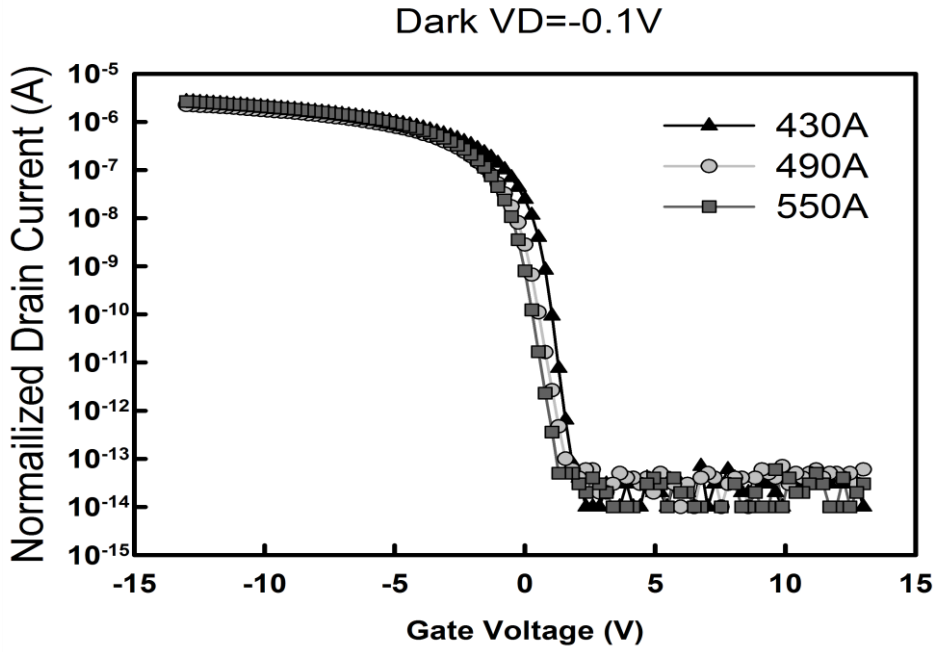
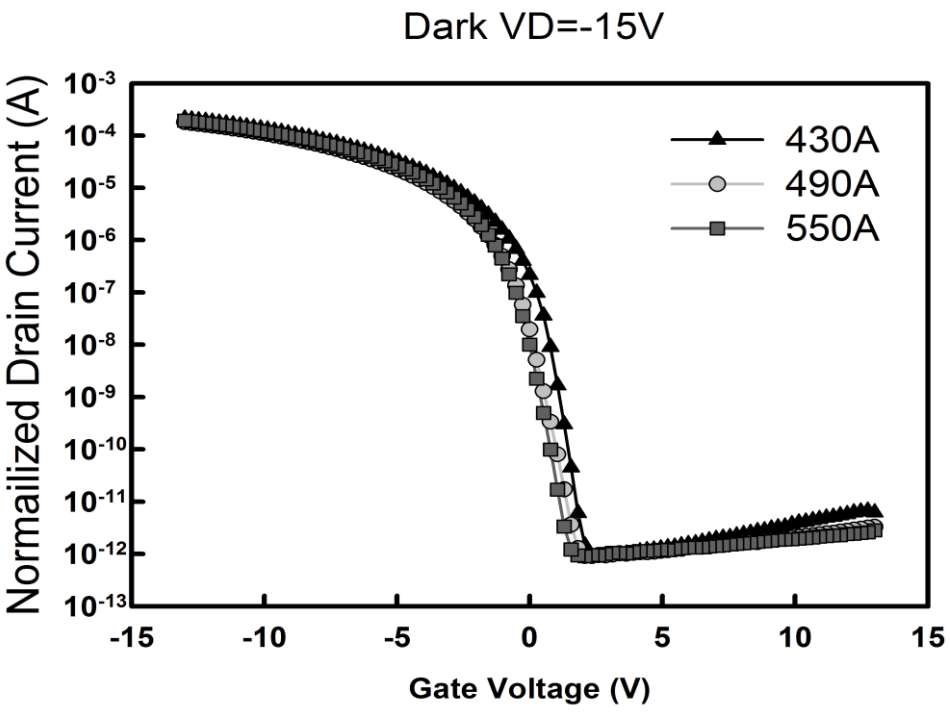


Fig.3. 18 The top gate Poly TFTs with lightly drain doping (LDD). The thickness of active layer is 430A, 490A, and 550A. These devices were treated by the ion-implant. The depth of implant reaches the bottom of semiconductor layer.



(a)



(b)

Fig.3. 19 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in dark. (b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in dark.

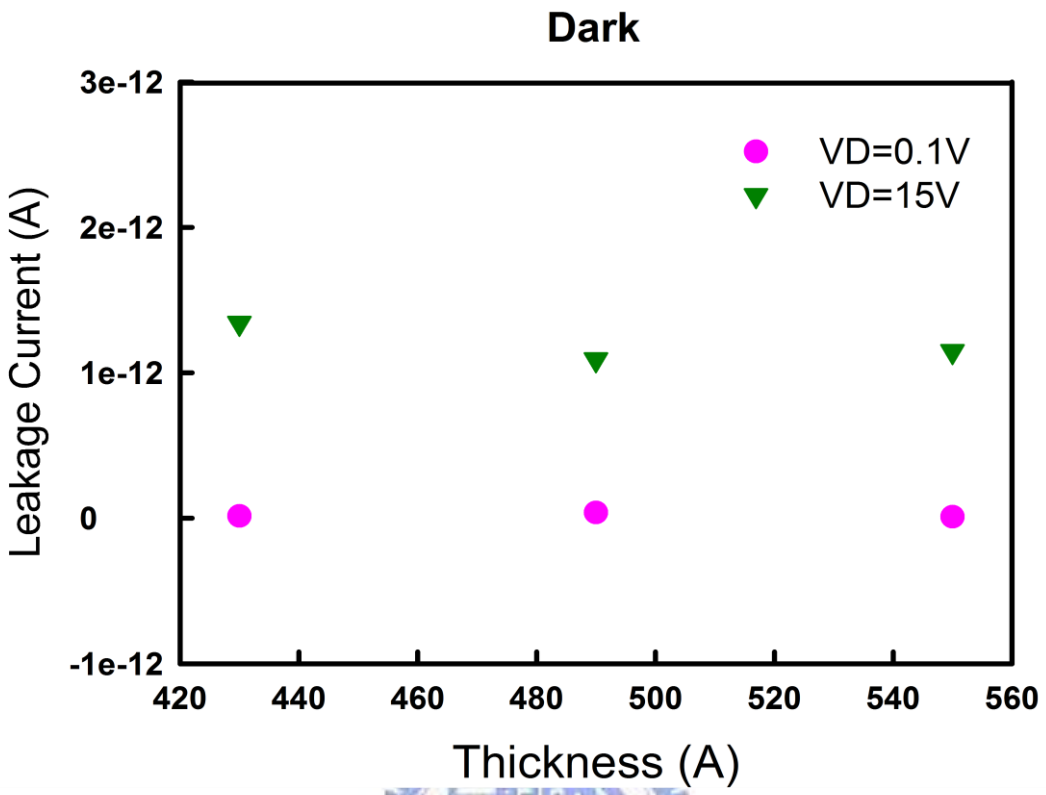
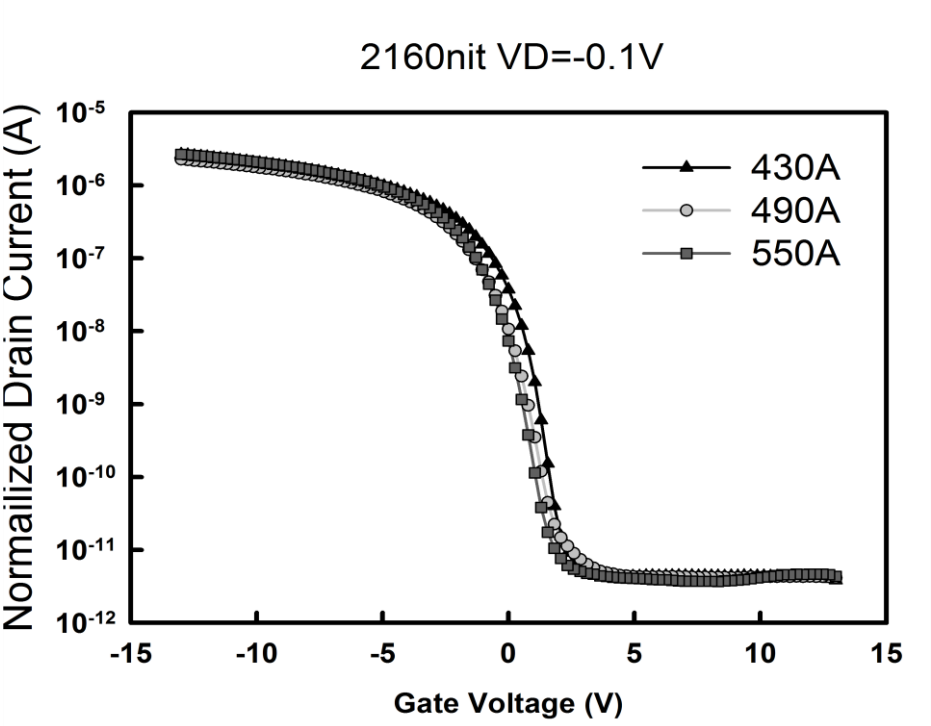
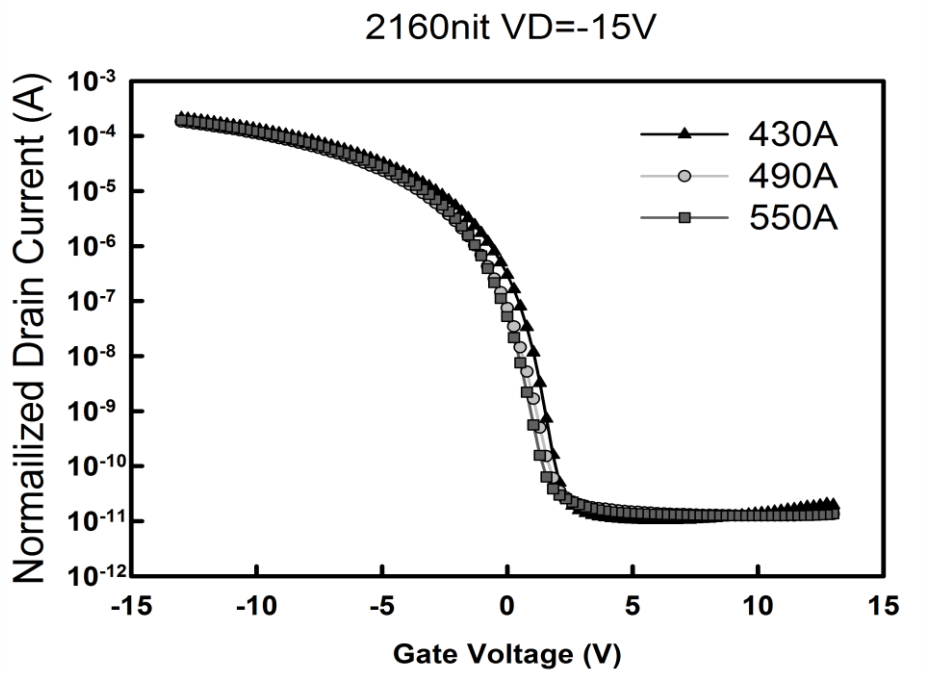


Fig.3. 20 The dark current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V.



(a)



(b)

Fig.3. 21 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in the brightness of 2160nit.(b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in the brightness of 2160nit.

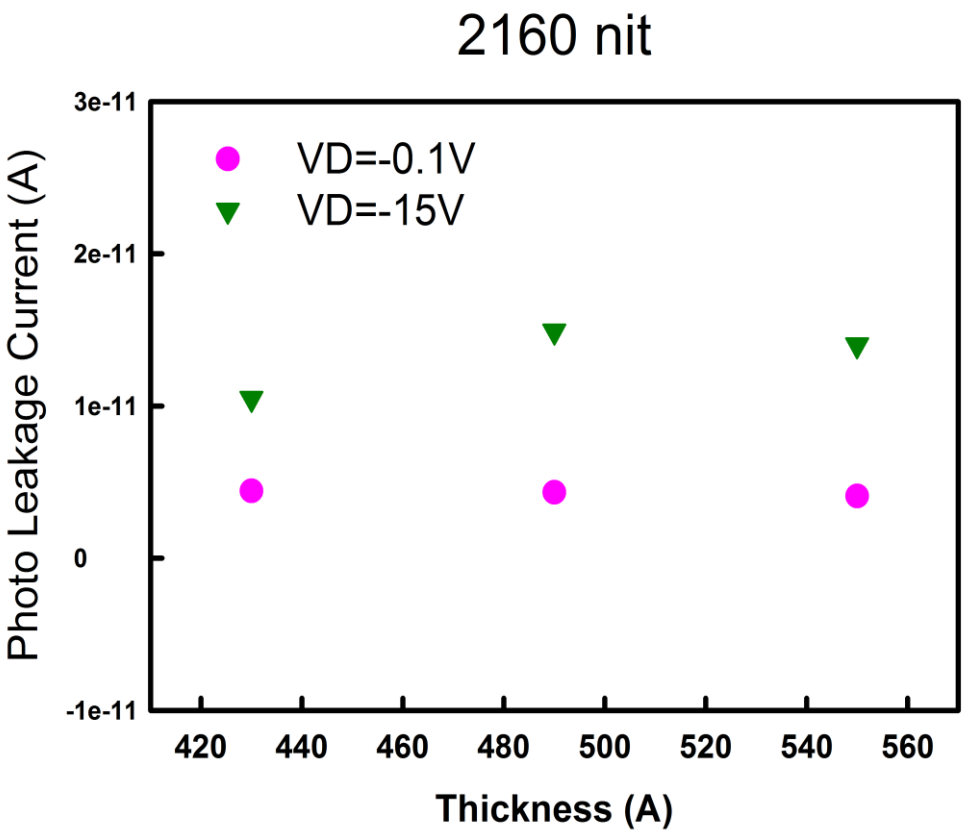
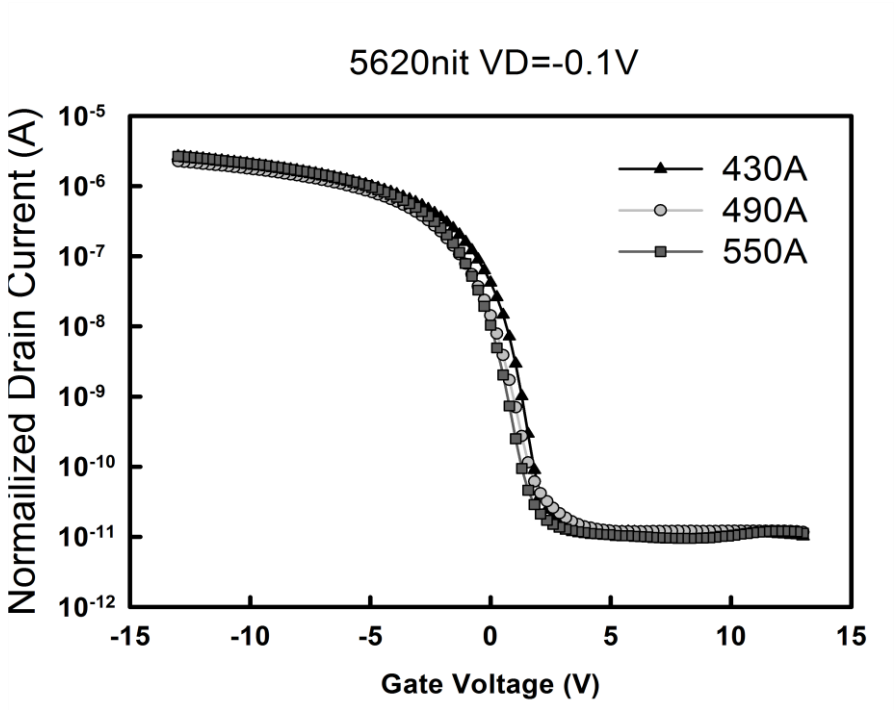
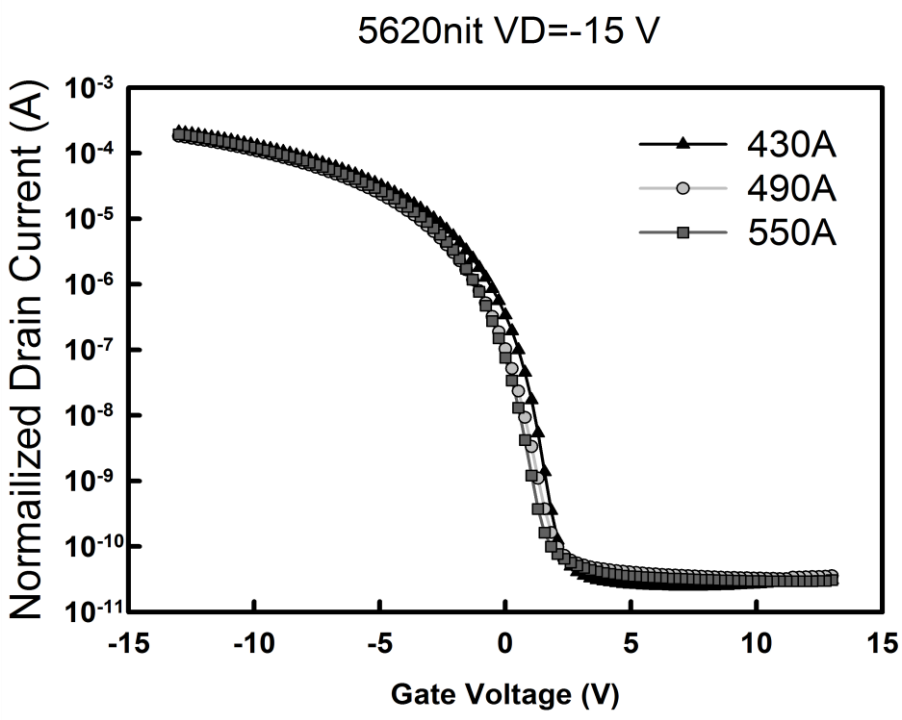


Fig.3. 22 The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 2160nit.



(a)



(b)

Fig.3. 23 (a) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-0.1V in the brightness of 5620nit. (b) The NI_D-V_G of the Poly-Si TFTs with different thickness as the V_D=-15V in the brightness of 5620nit.

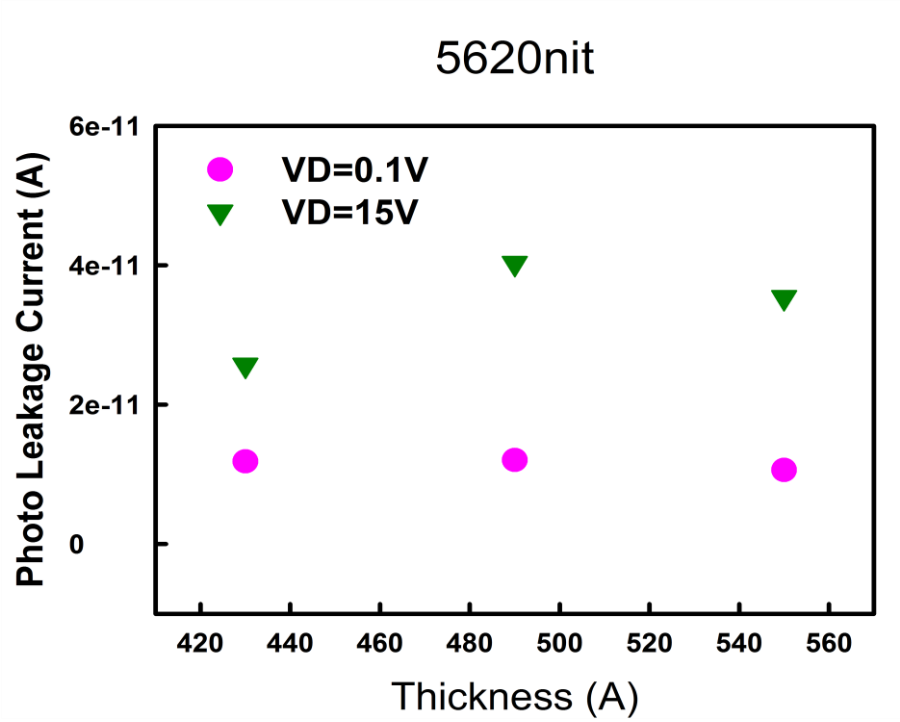


Fig.3. 24 The photo current of the proposed devices, which is extracted at a voltage $|V_G-V_{TH}|$ of 5V as V_D is -0.1V and -15V in the brightness of 5620nit.

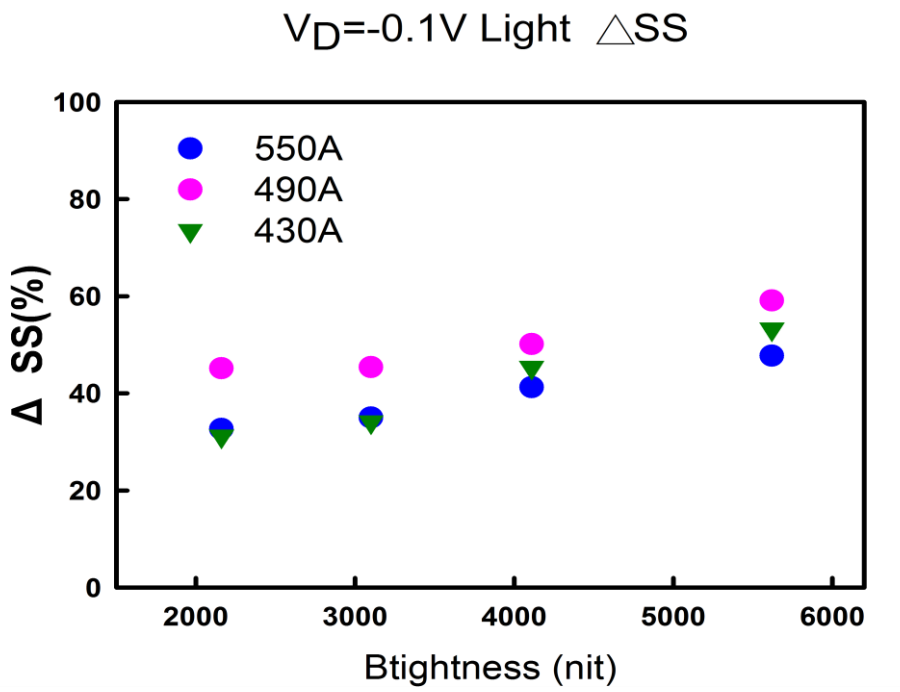


Fig.3. 25 The comparison of sub-threshold swing in the TFTs with varied thickness of semiconductor layer (430A, 490A, 550A) and varied brightness of back-light (2160, 3100, 4110, 5620 nit).

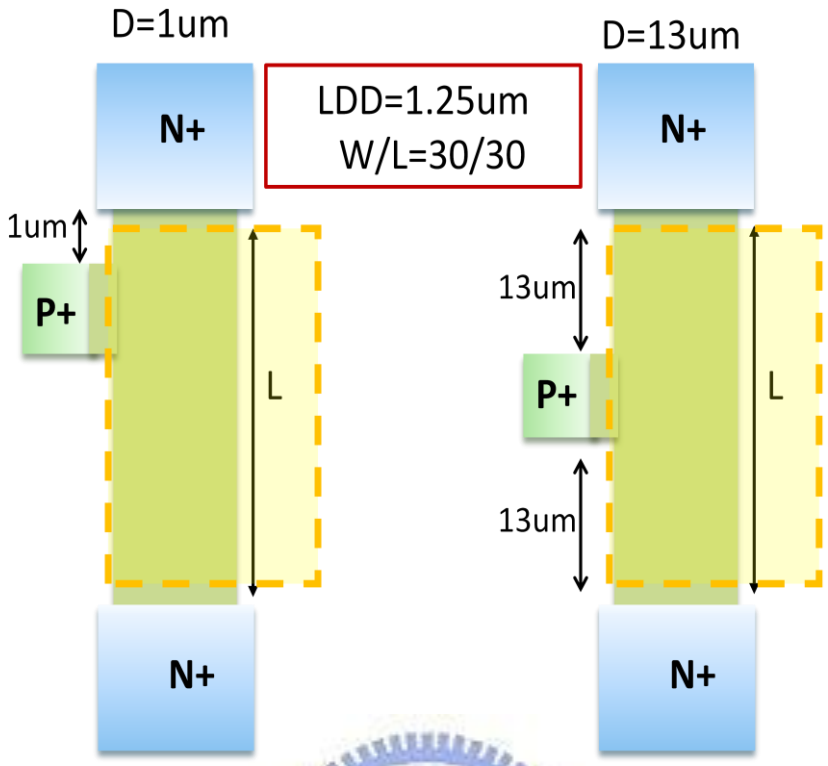


Fig.4. 1 The devices structures of the LBT TFTs with varied LBT position.

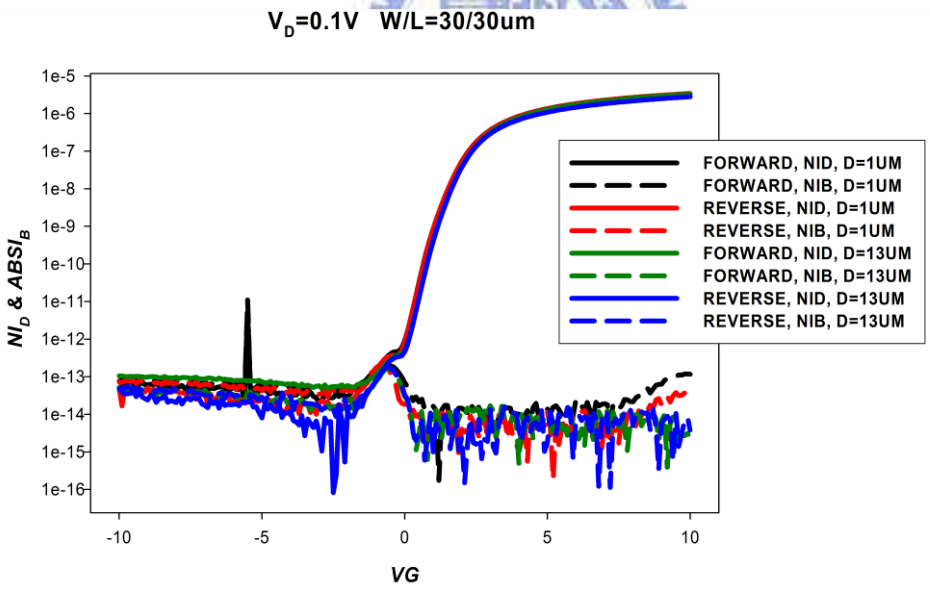


Fig.4. 2 The NI_D&$ABSI_B$-V_G of LBT poly-Si TFTs with lightly doped drain (LDD) structure in linear region.

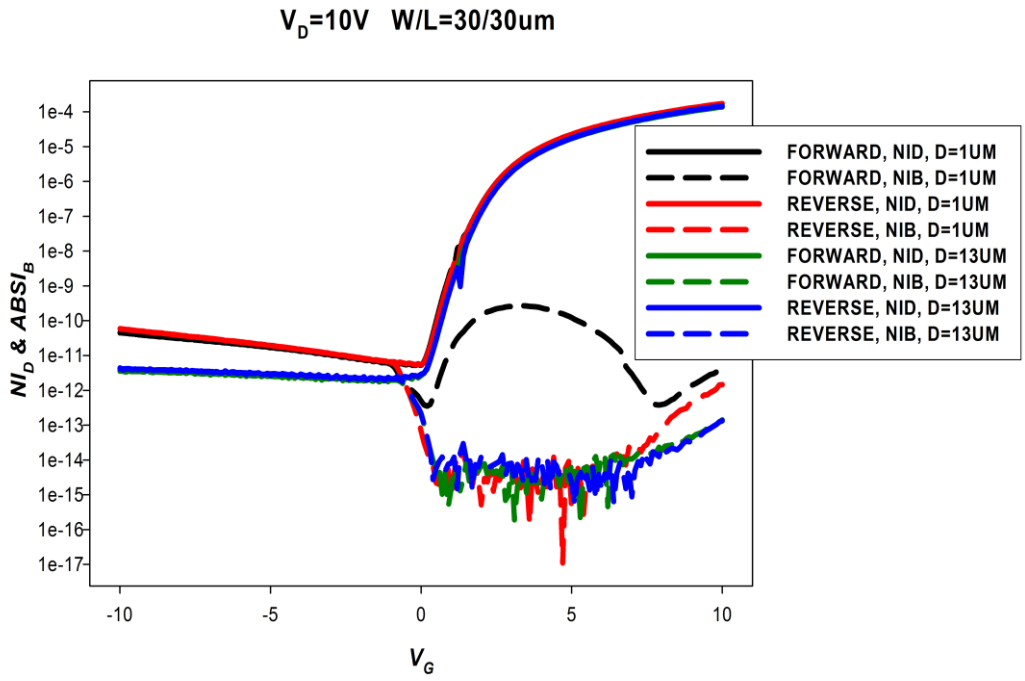


Fig.4. 3 The NI_D&$ABSI_B$-V_G of LBT poly-Si TFTs with lightly doped drain (LDD) structure in saturation region.

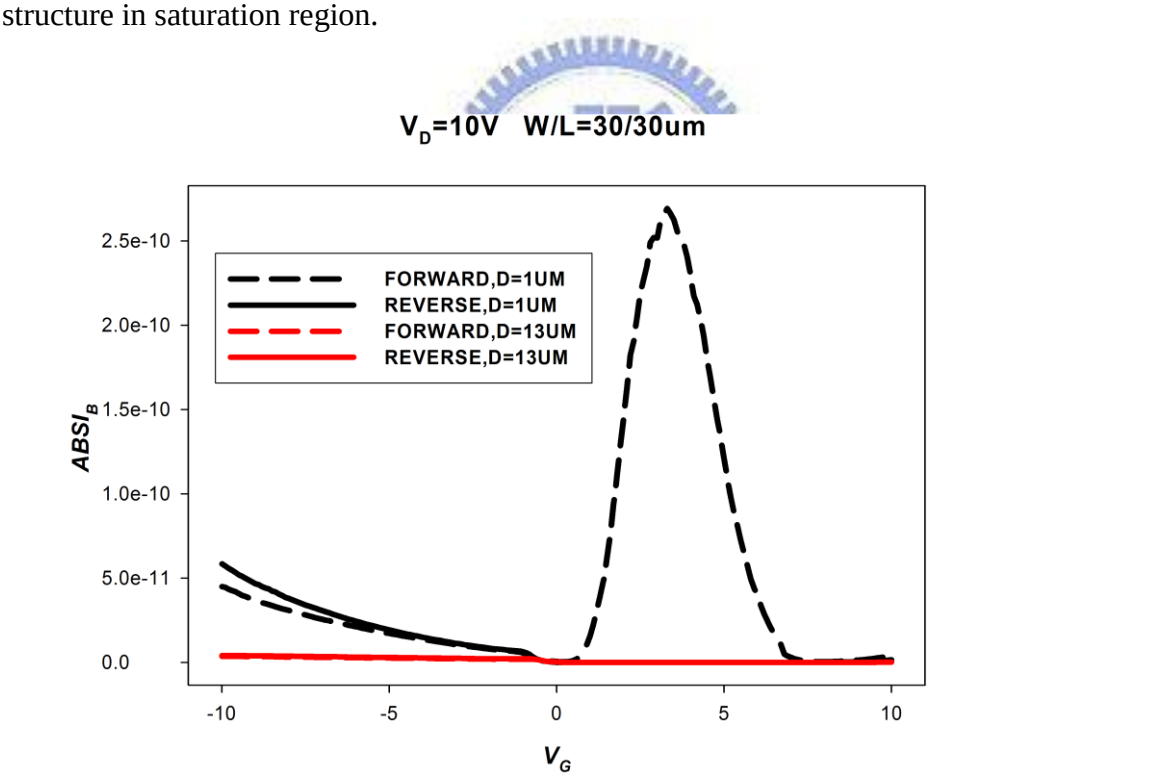


Fig.4. 4 The $ABSI_B$-V_G of LBT poly-Si TFTs with lightly doped drain (LDD) structure in saturation region. There is an ABSIB peak as LBT is near drain.

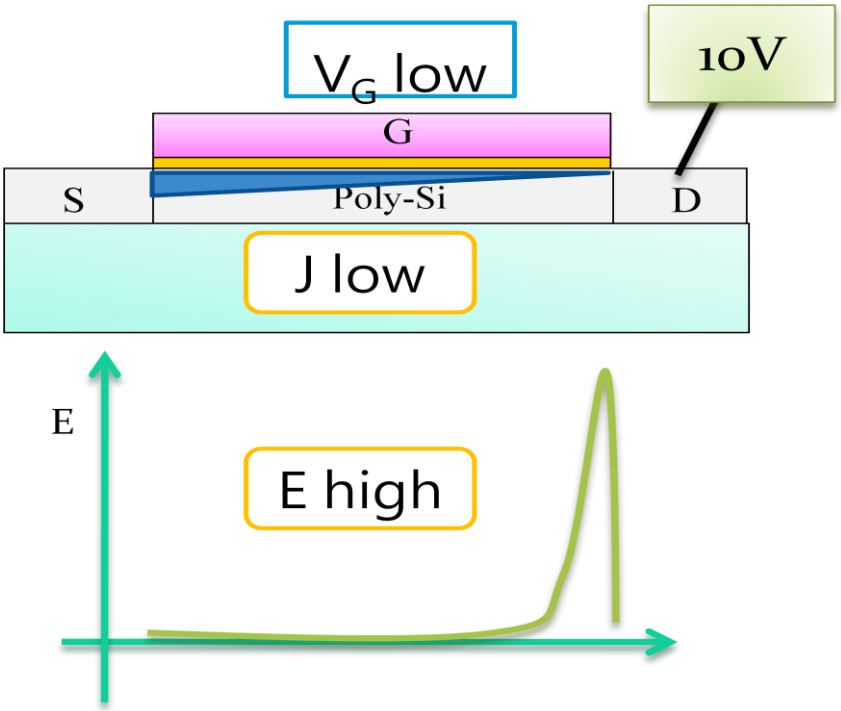


Fig.4. 5 As small V_G and high V_D are applied, there is high electric field in the junction of channel and drain.

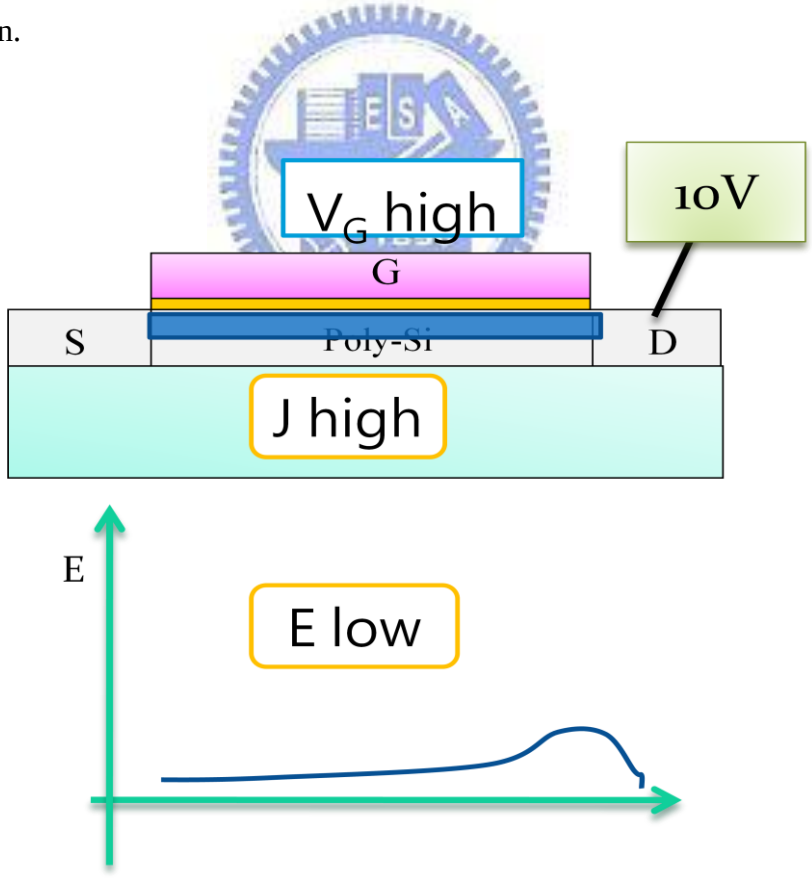


Fig.4. 6 As V_G increases, the $ABSI_B$ decrease rapidly, because of the electric field of drain becomes lower, and impact ionization becomes slightly.

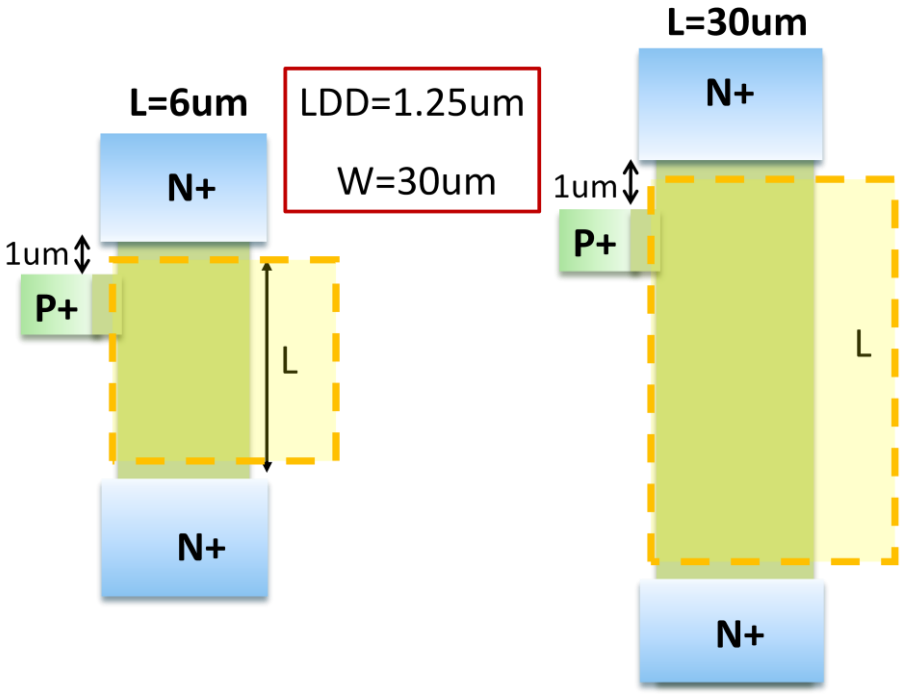


Fig.4. 7 The structure of two dimensions LBT TFTs.

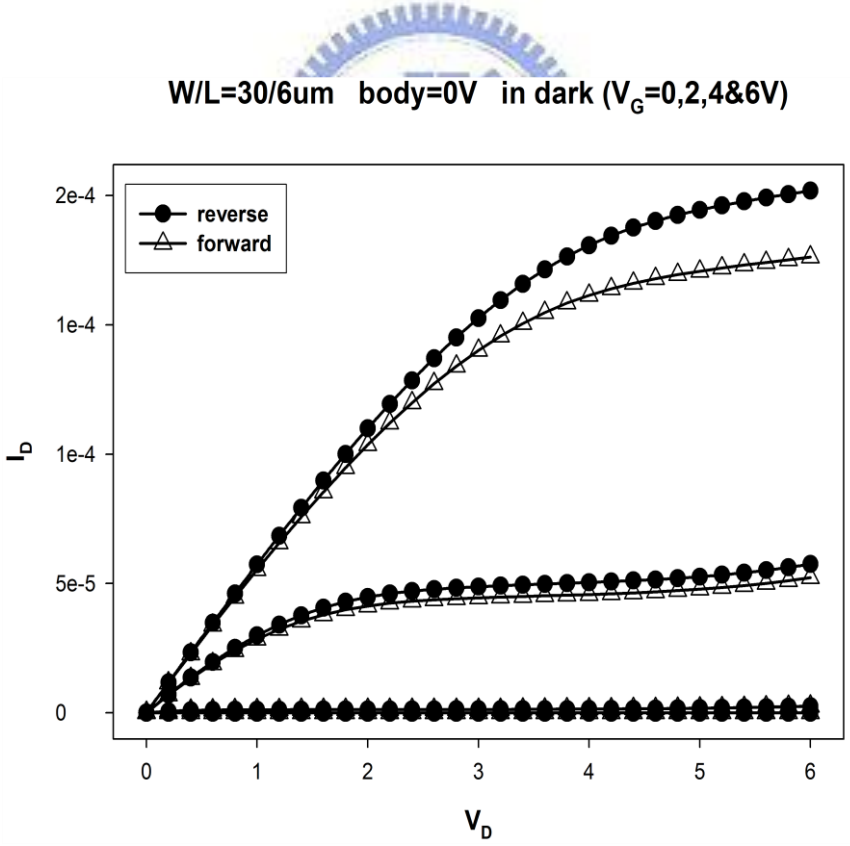


Fig.4. 8 The I_D-V_D of small size TFT which channel length is 6 um as forward bias and reverse bias is applied.

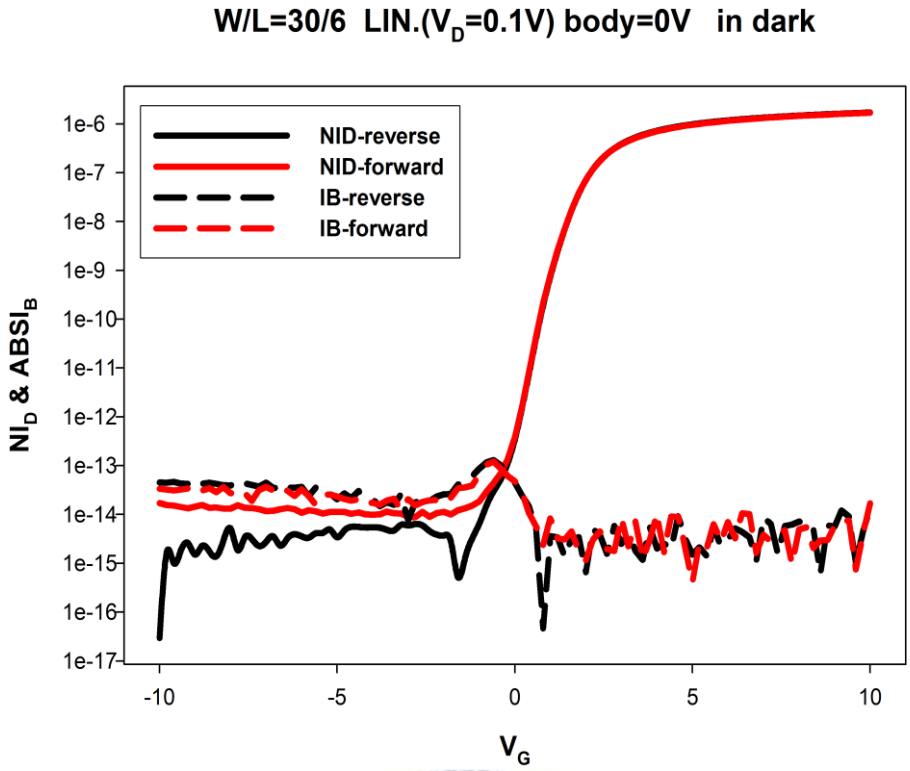


Fig.4. 9 The NI_D&$ABSI_B$-V_G of small size LBT TFTs as forward bias and reverse bias are applied in linear region.

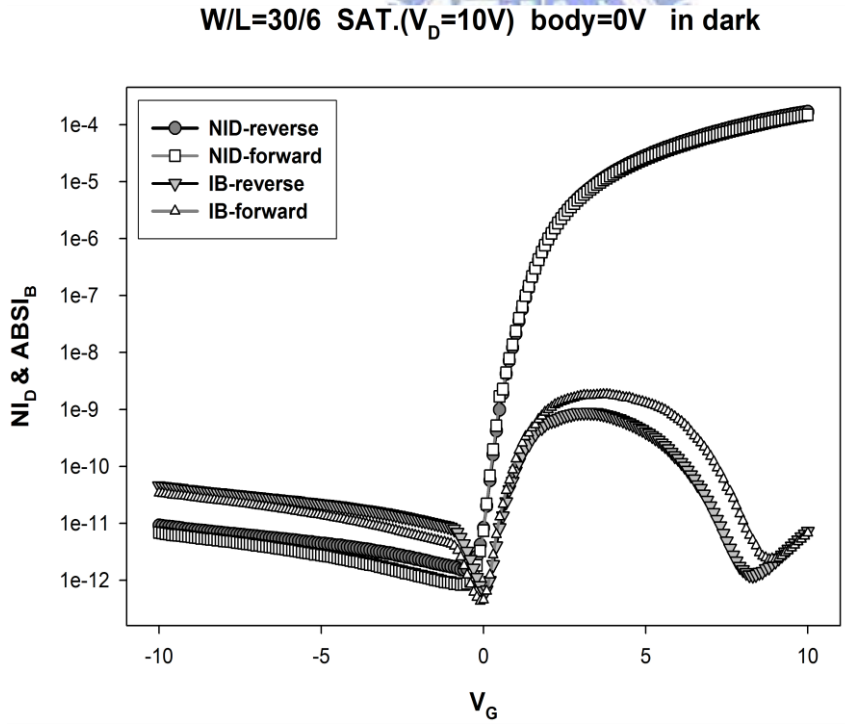


Fig.4. 10 The NI_D&$ABSI_B$-V_G of small size LBT TFTs as forward bias and reverse bias are applied in saturation region.

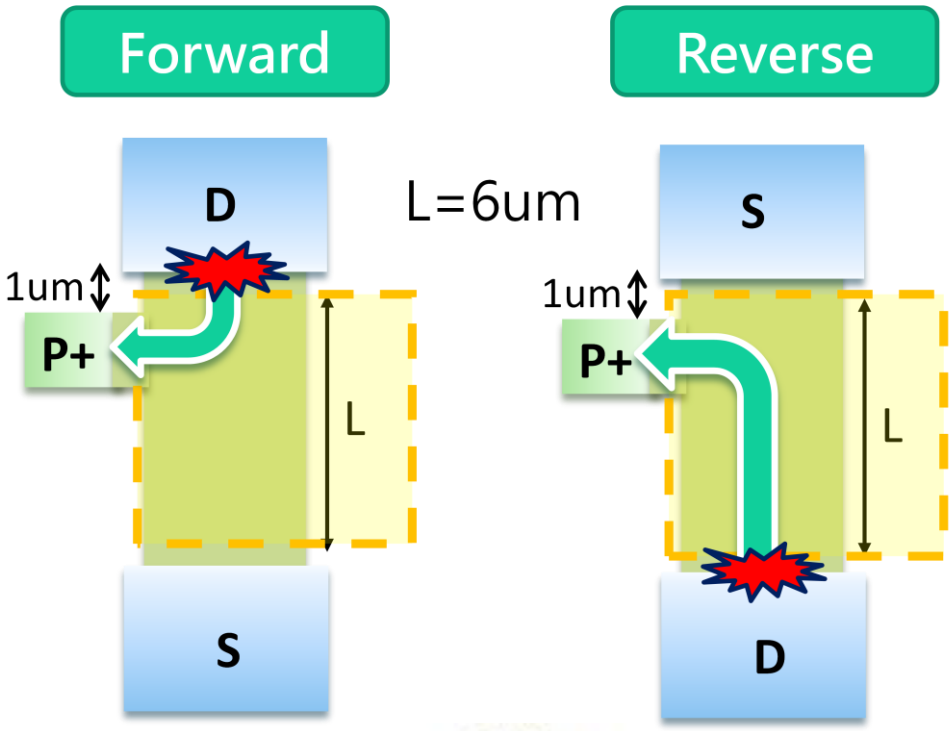


Fig.4. 11 The proposed model of small size LBT TFTs as forward bias and reverse bias are applied.

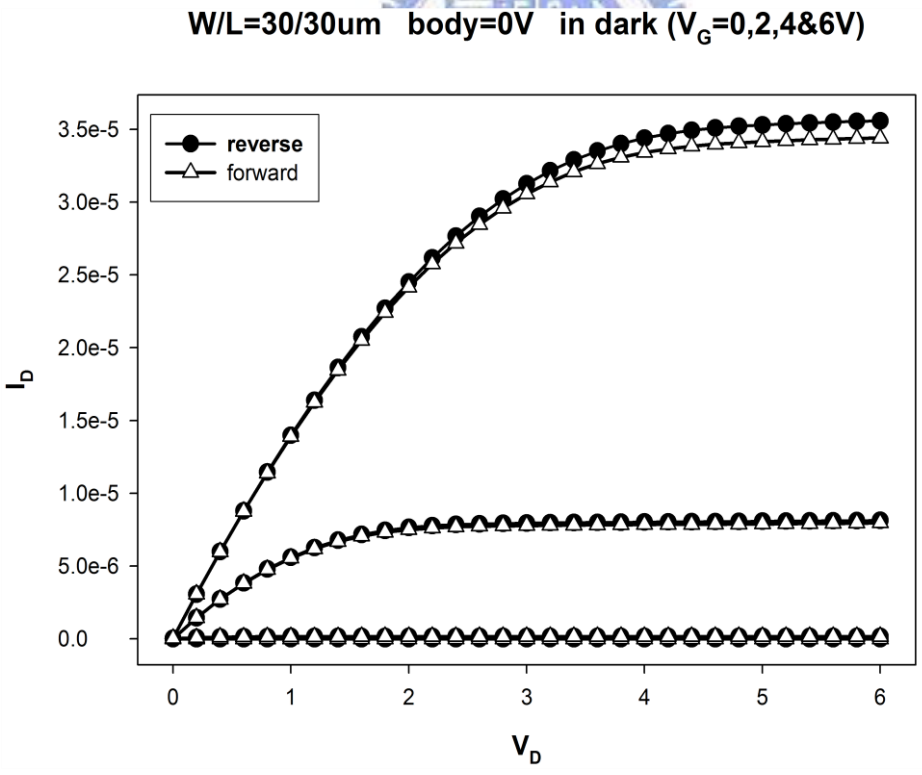


Fig.4. 12 The I_D-V_D of big size TFT which channel length is 30 um as forward bias and reverse bias is applied.

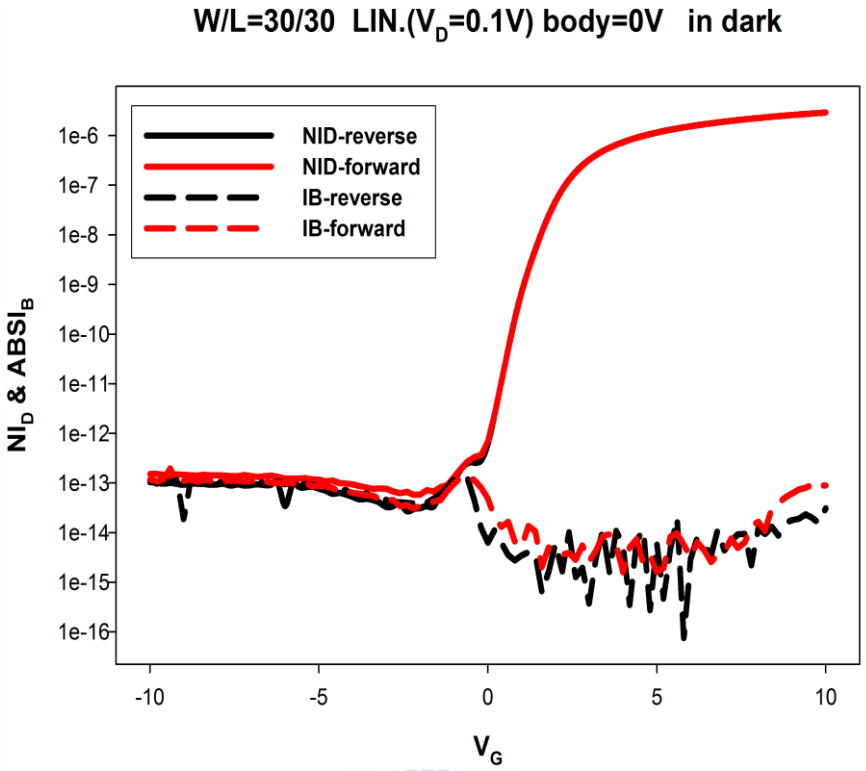


Fig.4. 13 The NI_D&$ABSI_B$-V_G of big size LBT TFTs as forward bias and reverse bias are applied in linear region.

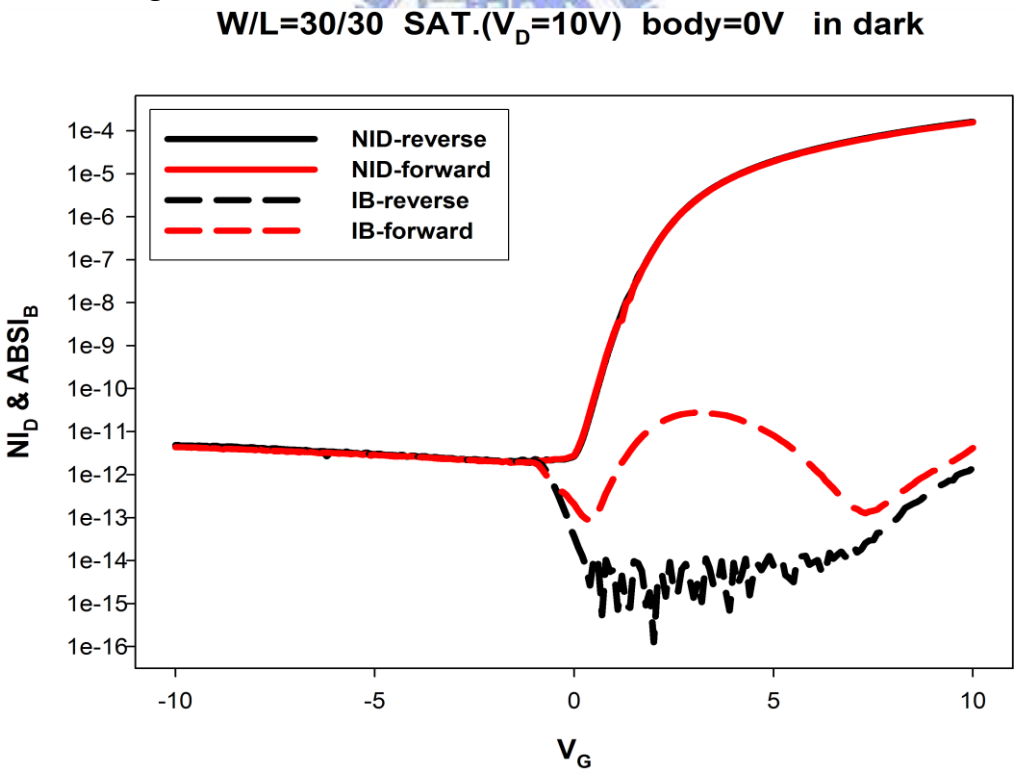


Fig.4. 14 The NI_D&$ABSI_B$-V_G of big size LBT TFTs as forward bias and reverse bias are applied in saturation region.

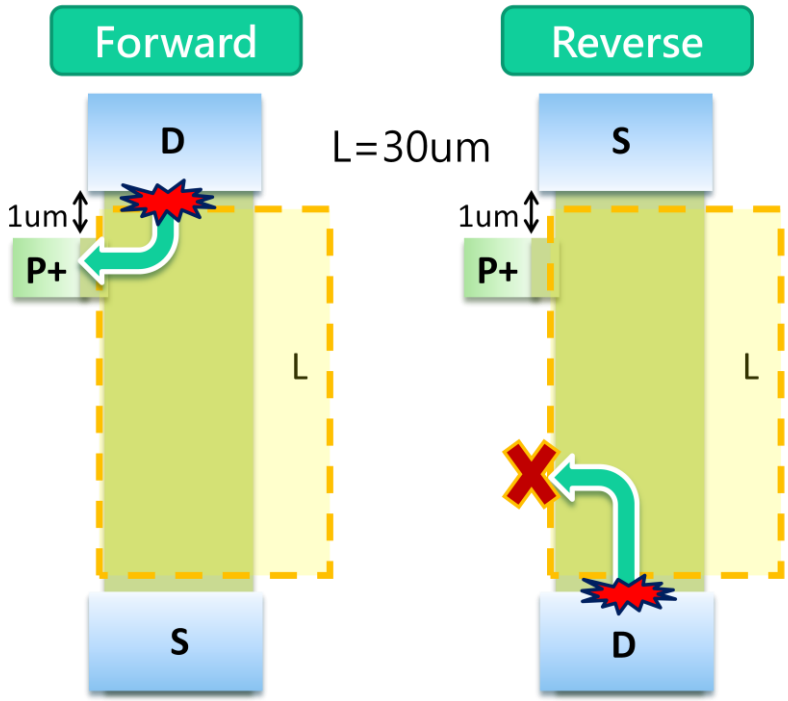


Fig.4. 15 The proposed model of big size LBT TFTs as forward bias and reverse bias are applied.

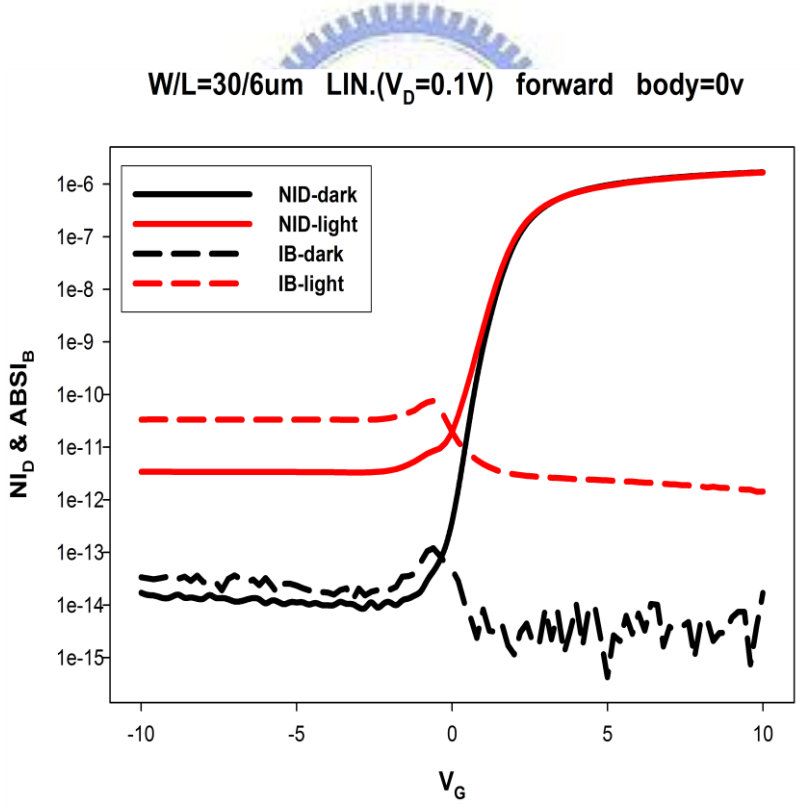


Fig.4. 16 The dependence of the LBT current ($ABSI_B$) and normalize drain current (NI_D) on the gate voltage (V_G) as forward bias is applied in linear region.

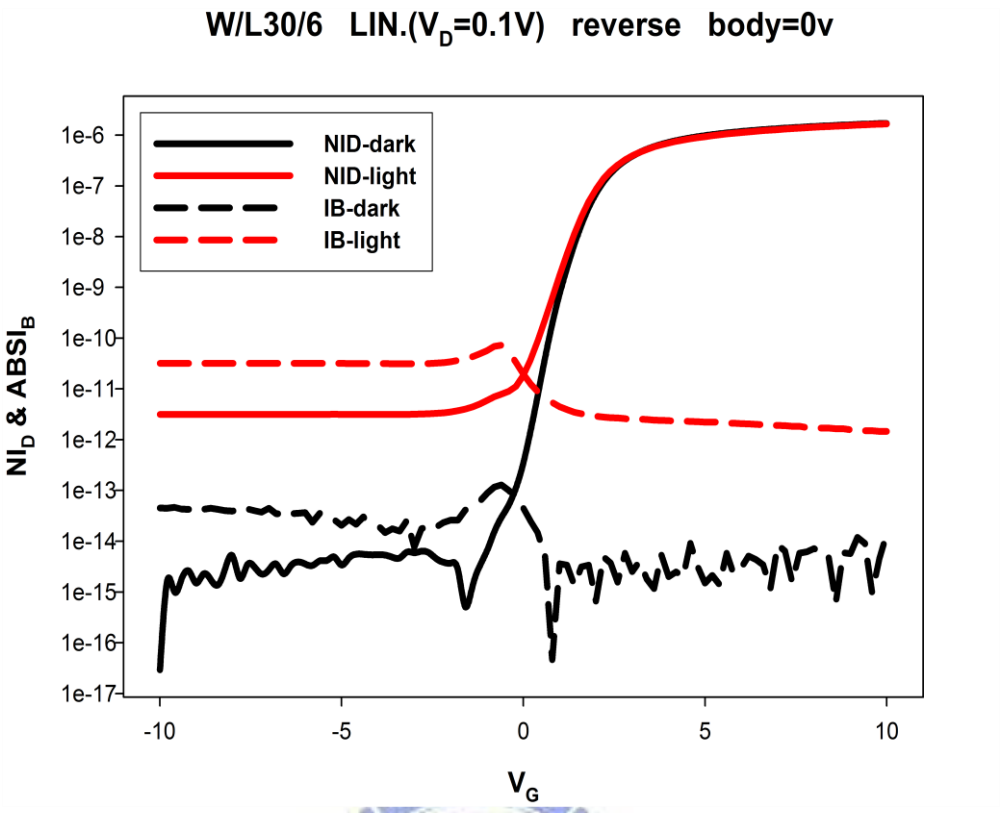


Fig.4. 17 The dependence of the LBT current ($ABSI_B$) and normalize drain current (NI_D) on the gate voltage (V_G) as reverse bias is applied in saturation region.

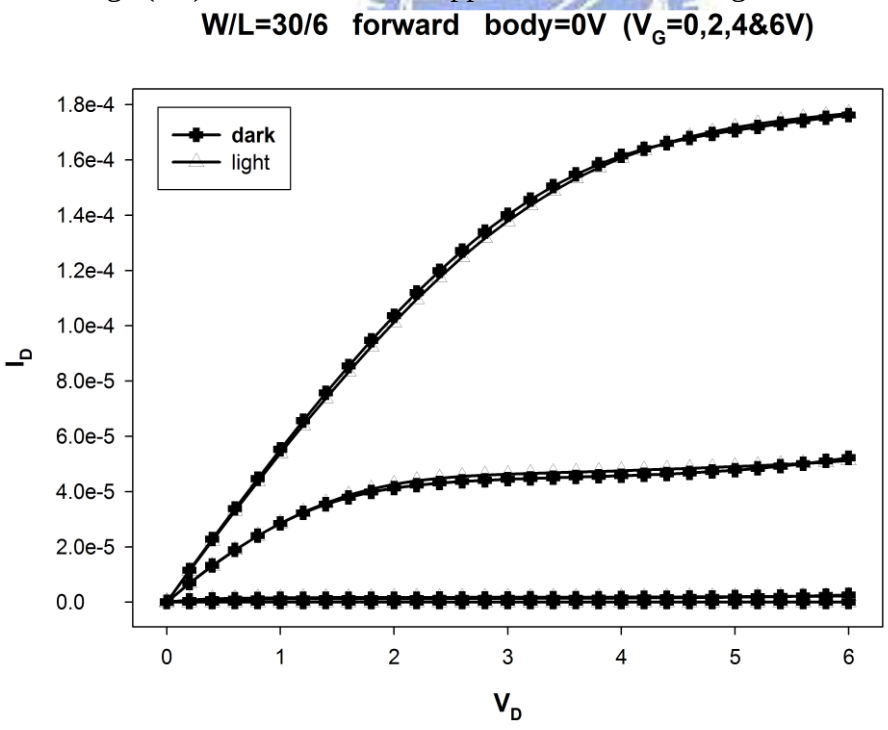


Fig.4. 18 The I_D-V_D of small size TFT which channel length is 6 um as forward bias is applied in dark and light.

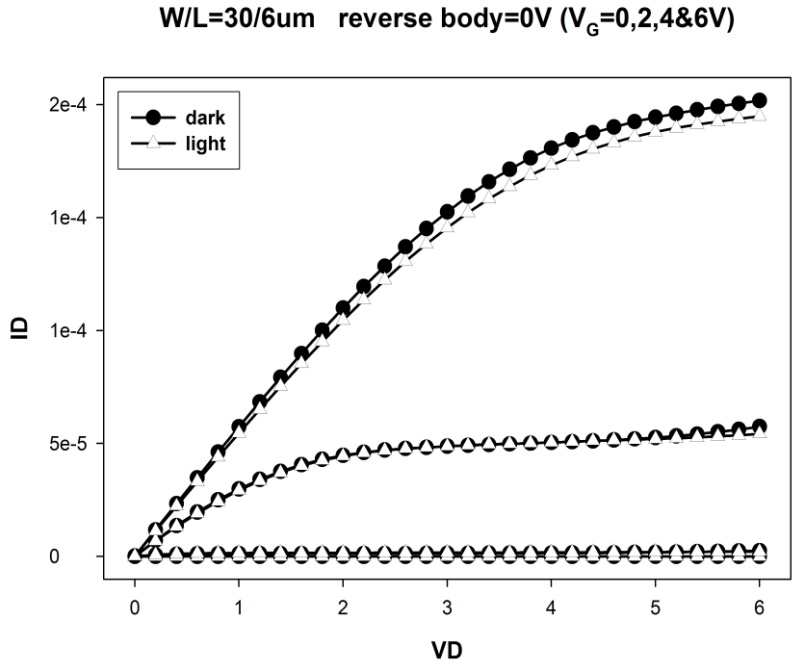


Fig.4. 19 The I_D-V_D of small size TFT which channel length is 6 um as reverse bias is applied in dark and light.

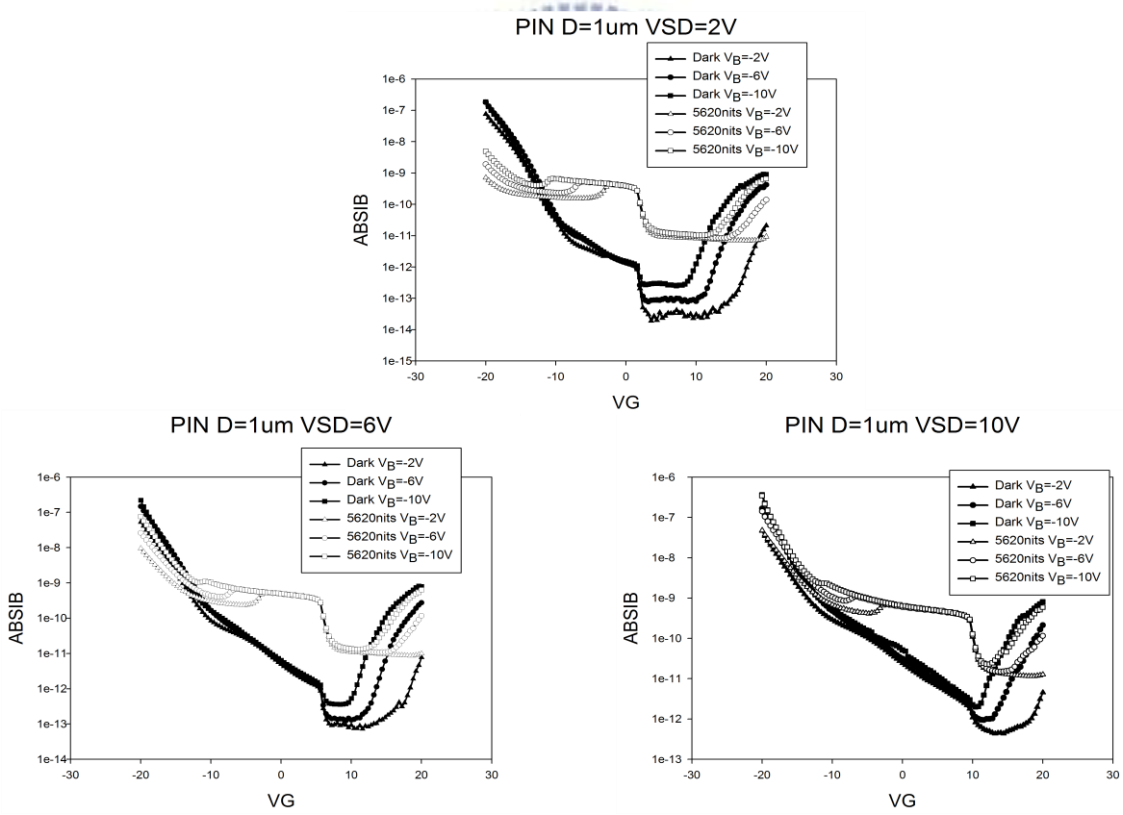


Fig.4. 20 The $ABSI_B$-V_G with fixed N+ region voltage (V_{SD}=2V, 6V, 10V) and variations in the LBT voltage (V_B=-2V, -6V, -10V) in dark and the brightness of 5620 nit.

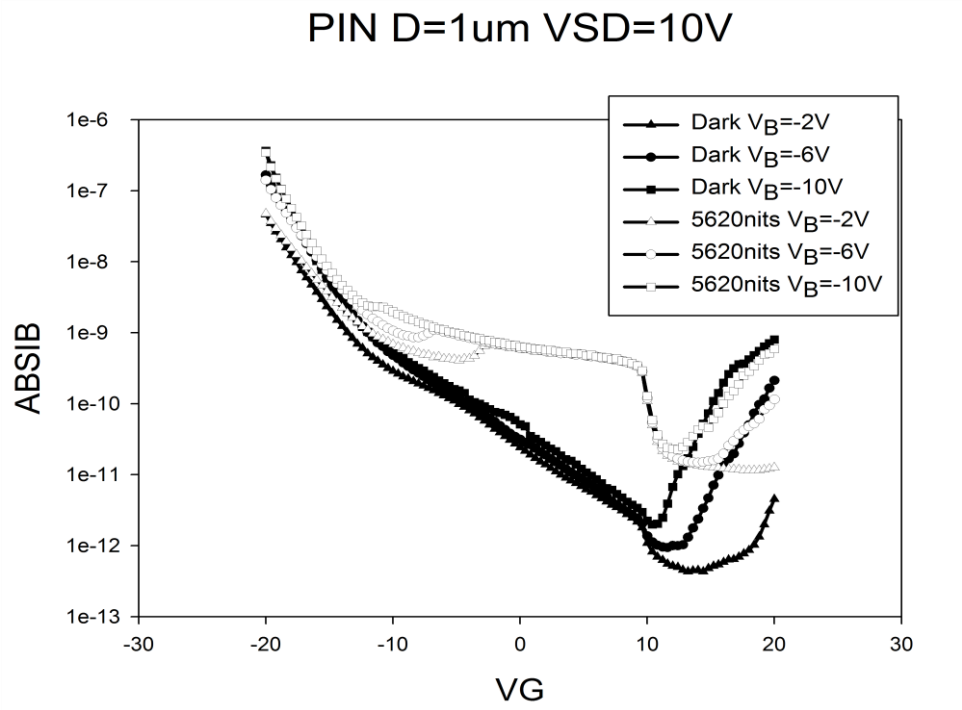


Fig.4. 21 The $ABSI_B$-V_G of the LBT poly-Si TFTs which the position of LBT near the n+ region with fixed V_{SD}=10V and variations in the LBT voltage (V_B=-2V, -6V, -10V) in dark and the brightness of 5620 nit.

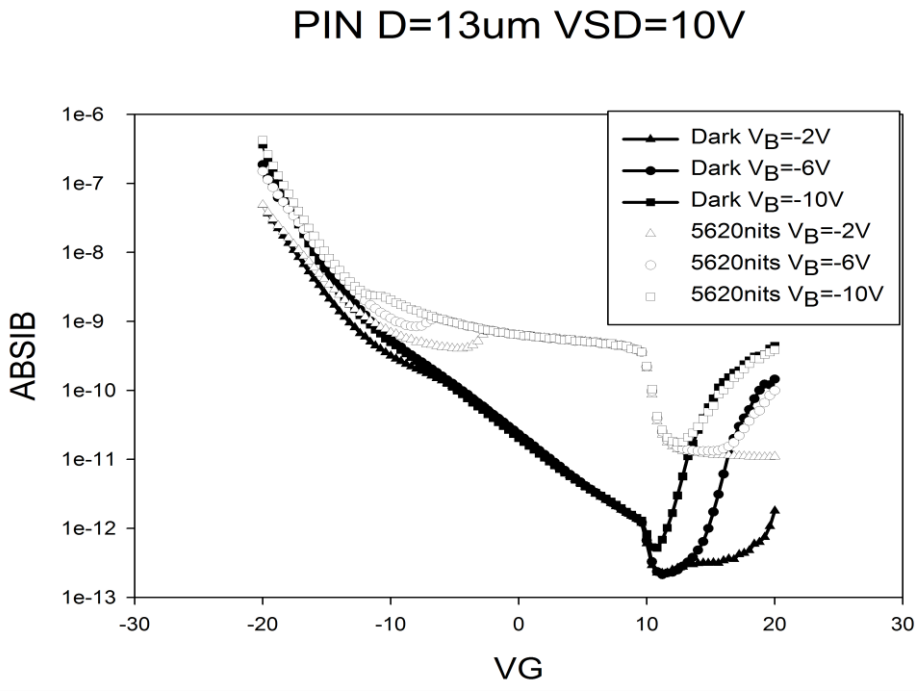


Fig.4. 22 The $ABSI_B$-V_G of the LBT poly-Si TFTs which the position of LBT near the channel middle with fixed V_{SD}=10V and variations in the LBT voltage (V_B=-2V, -6V, -10V) in dark and the brightness of 5620 nit.

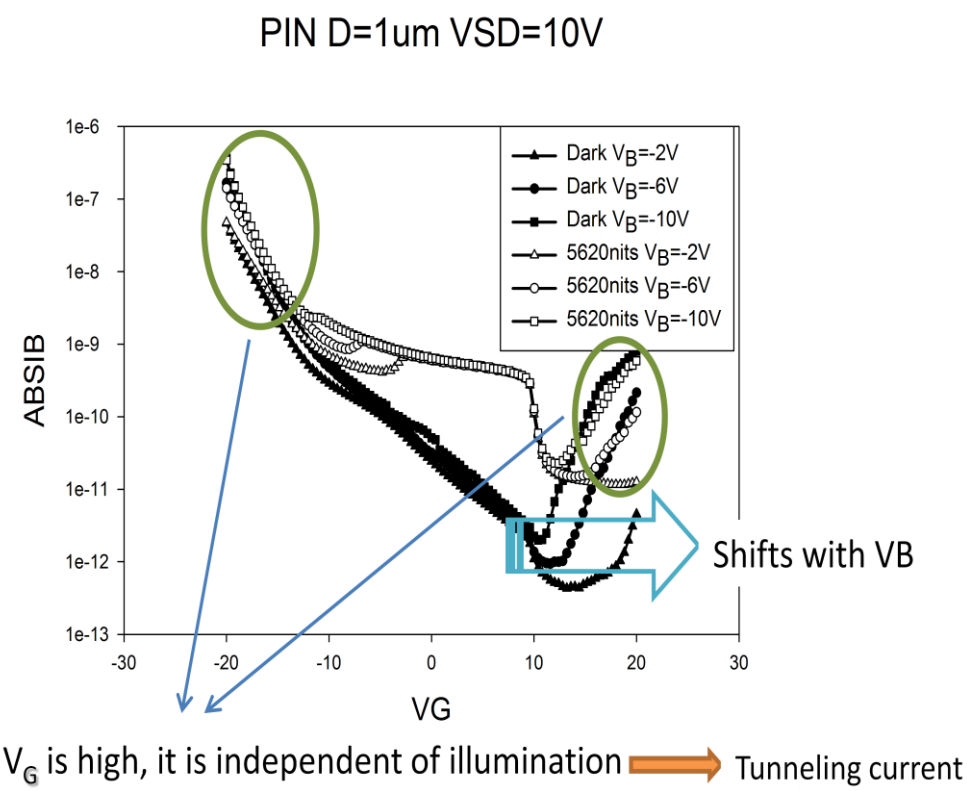


Fig.4. 23 The analysis of the $ABSI_B$-V_G as V_G is high.

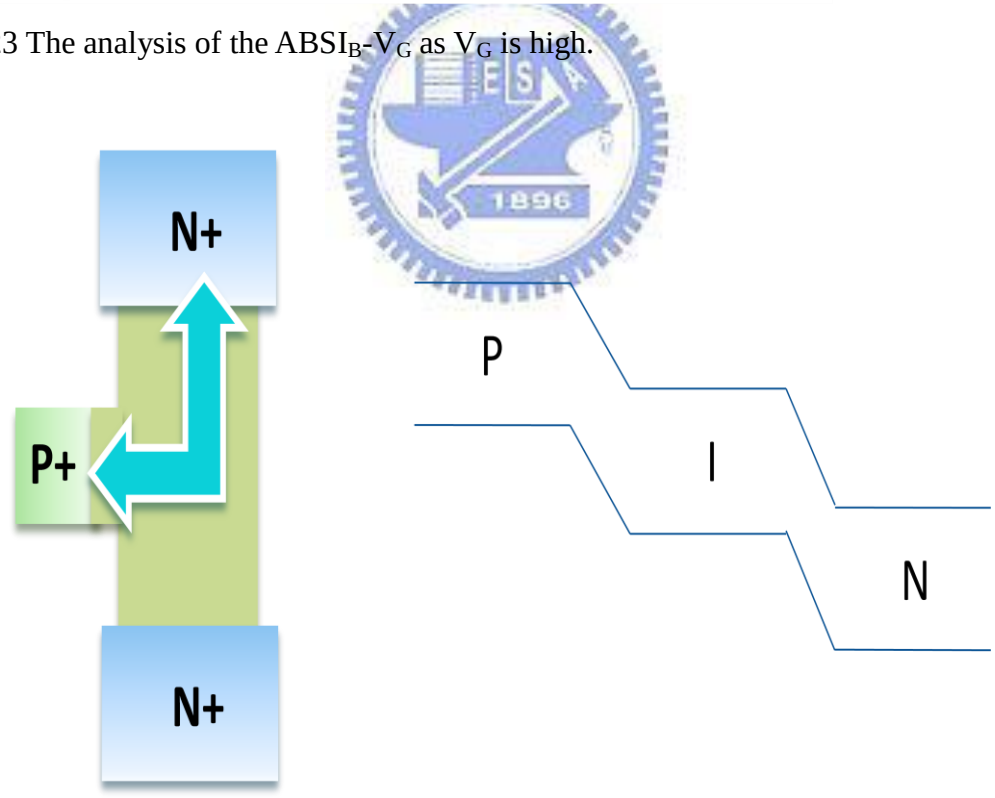


Fig.4. 24 Proposed band diagram for the PIN structure of LBT TFTs.

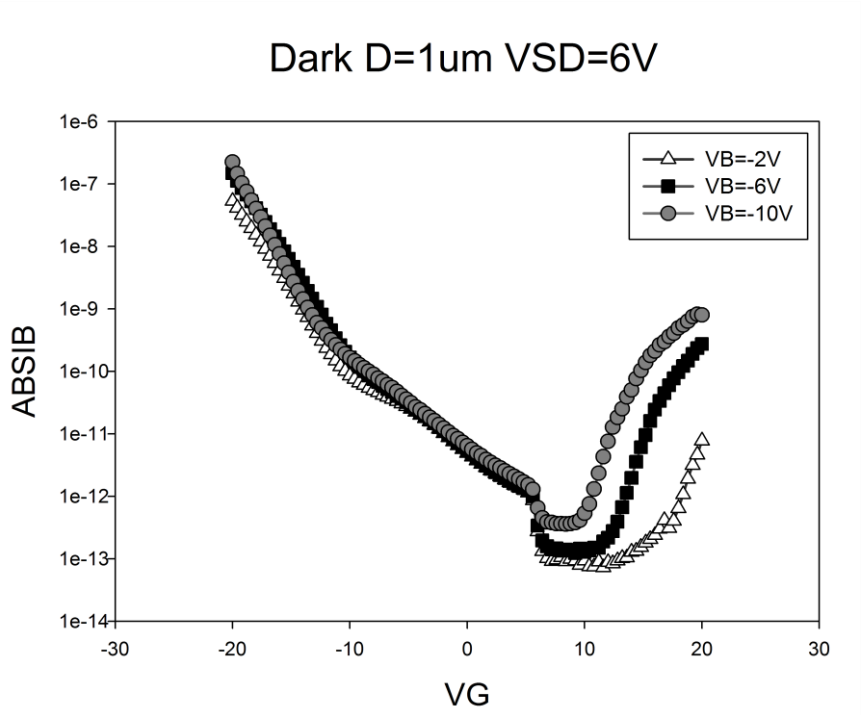


Fig.4. 25 The ABSIB-V_G of LBT TFT with fixed V_{SD}=6V and varied V_B in dark.

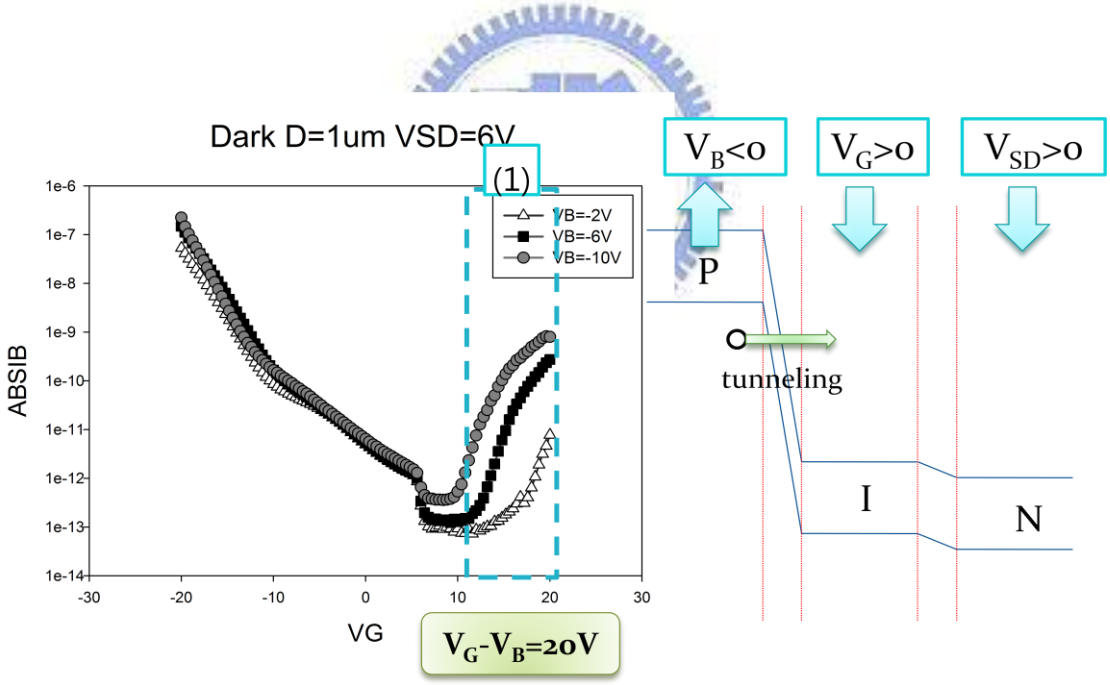


Fig.4. 26 The ABSI$_B$-V_G with fixed V_{SD} in dark. For region 1, the tunneling current is occurred as high positive V_G is applied.

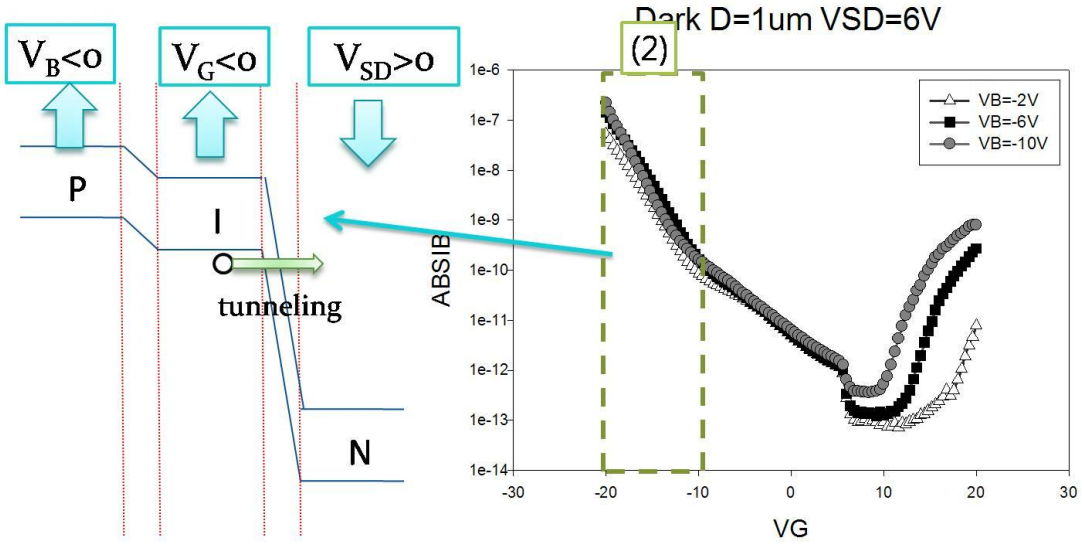


Fig.4. 27 The $ABSI_B$-V_G with fixed V_{SD} in dark. For region 2, the tunneling current was occurred as high negative V_G is applied.

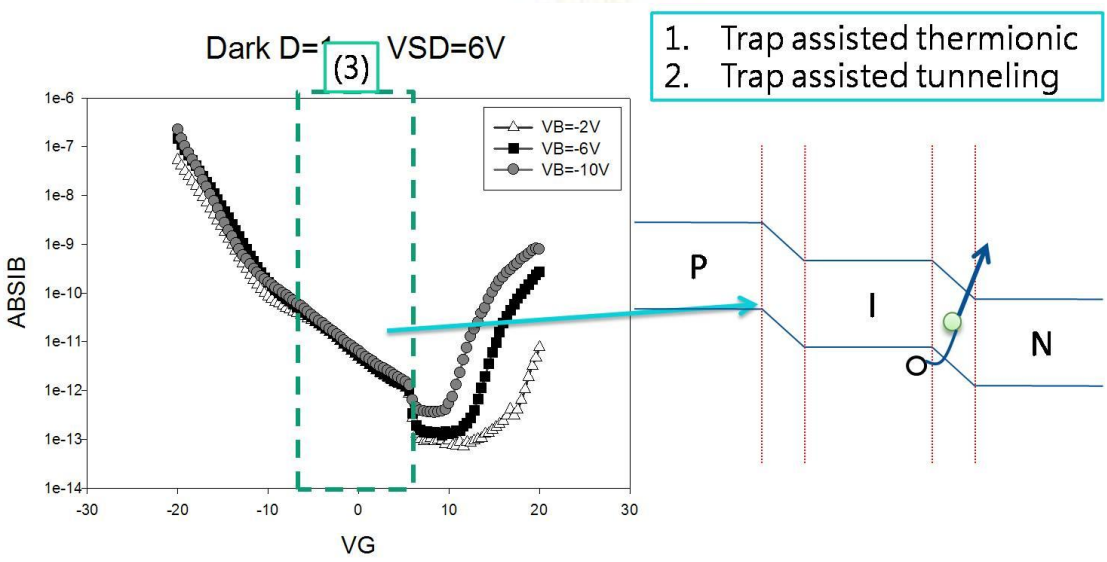


Fig.4. 28 The $ABSI_B$-V_G with fixed V_{SD} in dark. For region 3, because the current is independent of the energy band of p+ region, the current comes from the NI junction.

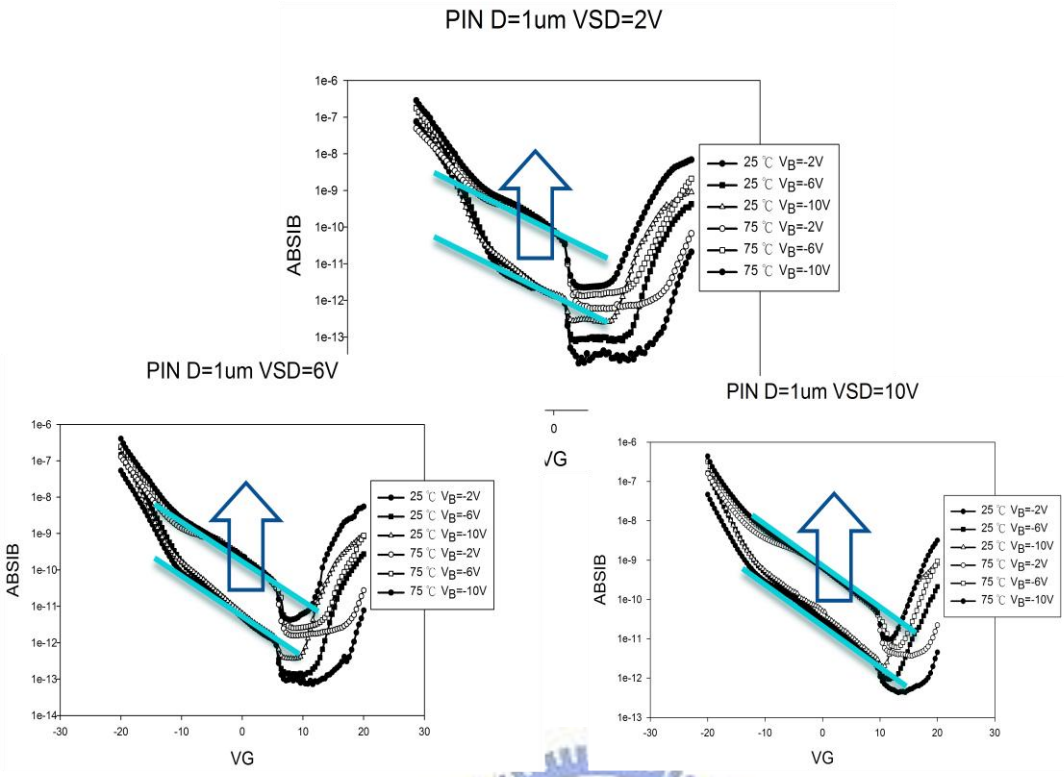


Fig.4. 29 The $ABSI_B$-V_G with fixed V_{SD} in dark. The device characteristics from 25℃ to 75℃. The LBT current horizontal increase from 25℃ to 75℃ as small V_G is applied.

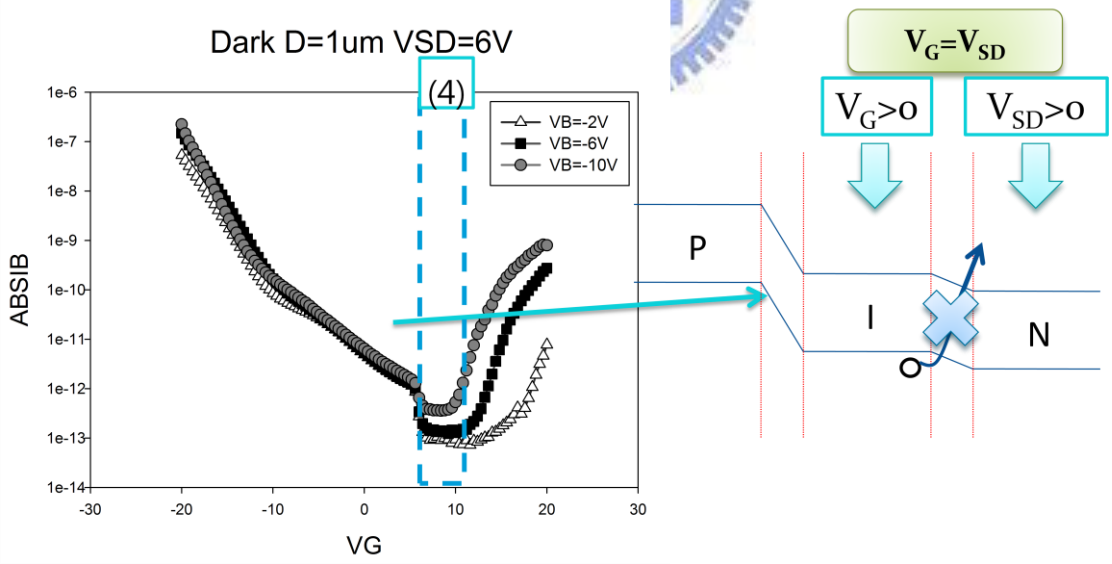


Fig.4. 30 The $ABSI_B$-V_G with fixed V_{SD} in dark. For region 4, the current decreases rapidly as high positive V_G increases.

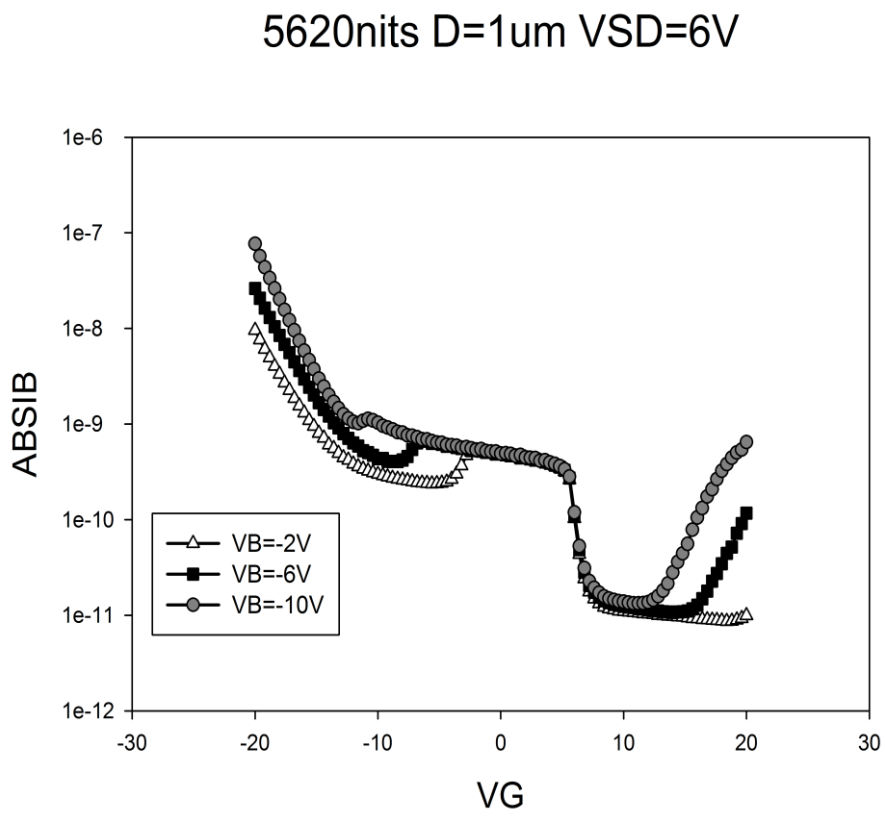


Fig.4. 31 The ABSIB-V_G of LBT TFT with fixed V_{SD}=6V and varied V_B in the brightness of 5620 nit.

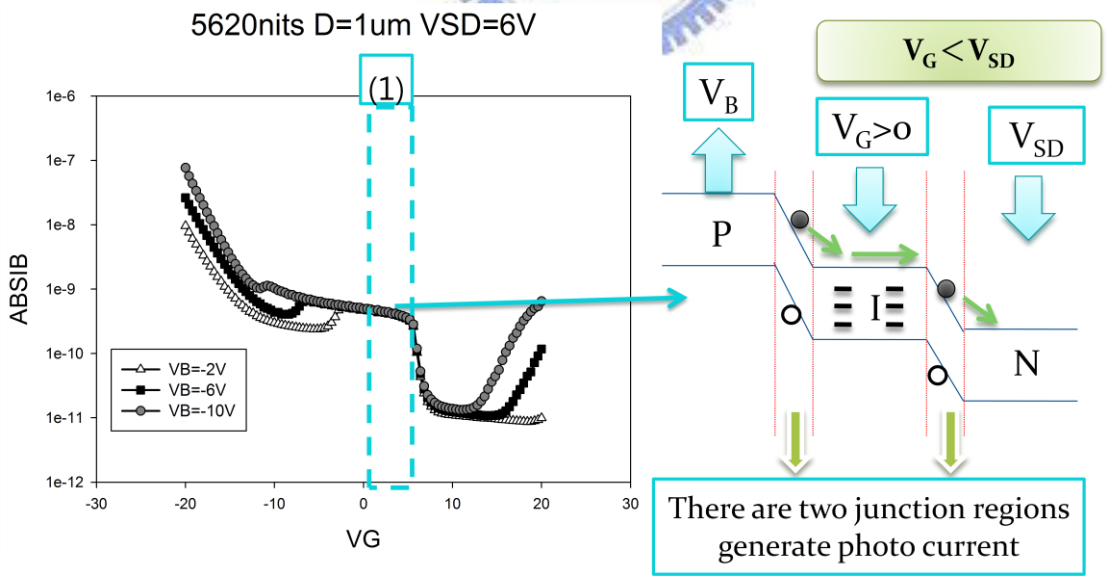


Fig.4. 32 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 1, the photo current is like a flat-top as small positive V_G is applied.

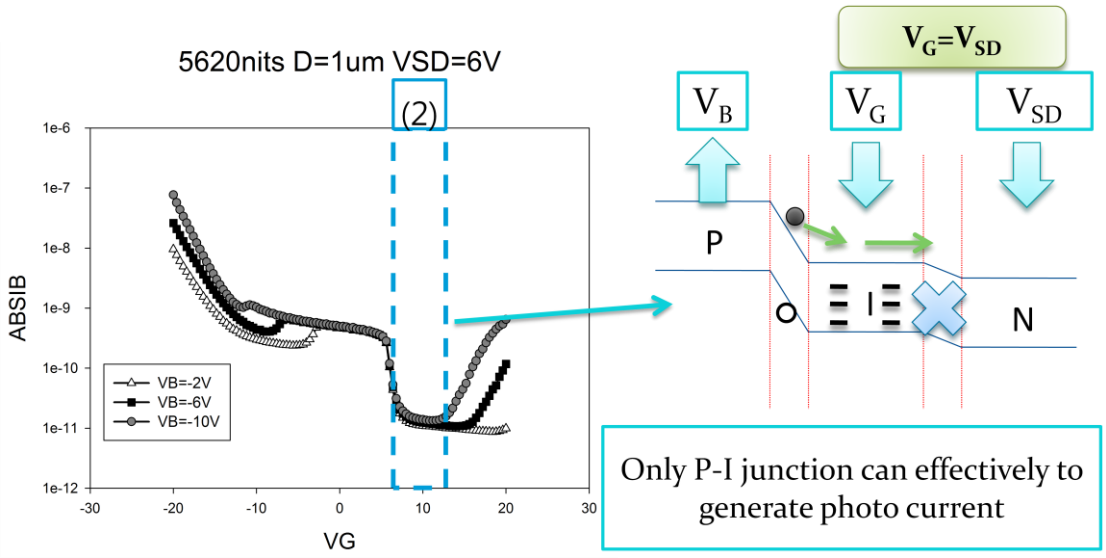


Fig.4. 33 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 2, the LBT current decreases rapidly as positive V_G increase to V_{SD}=V_G. Only P-I junction can effectively to generate photo current.

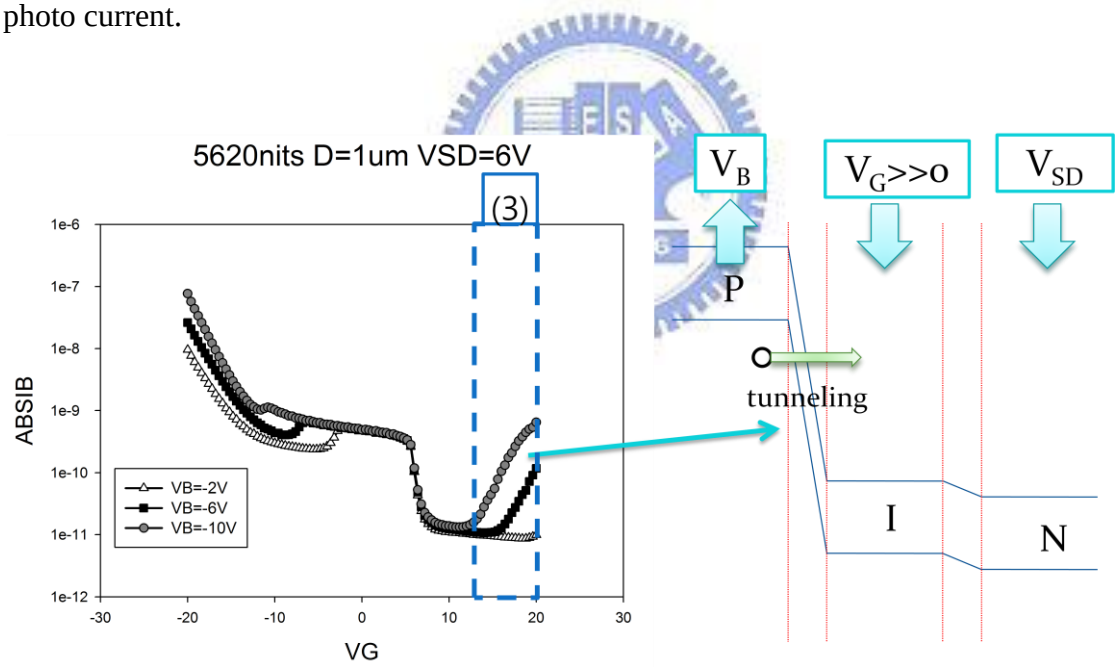


Fig.4. 34 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 3, the tunneling current is occurred as high positive V_G is applied.

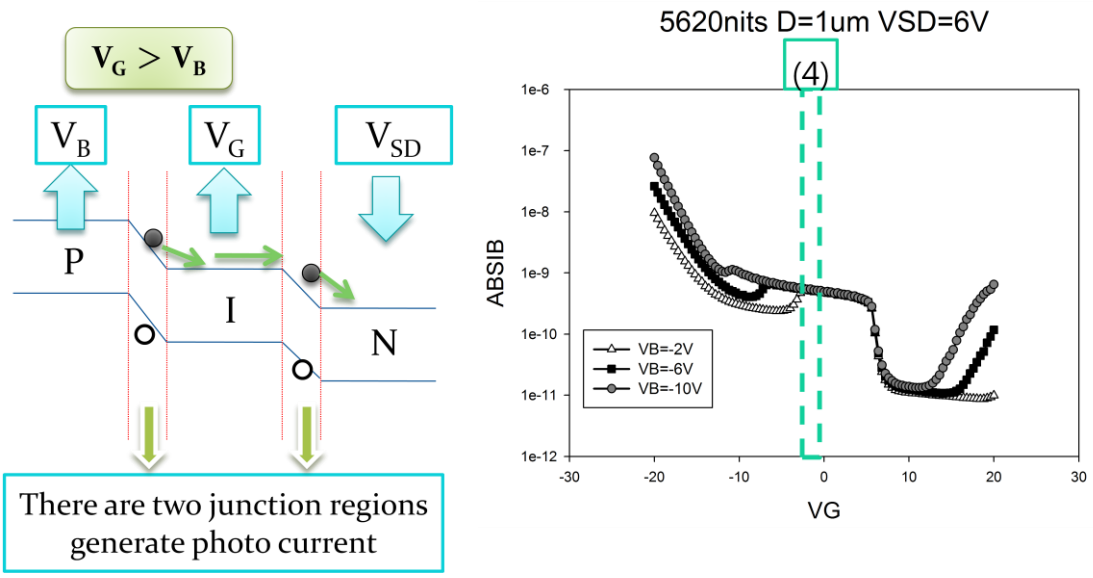


Fig.4. 35 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 4, the photo current is like a flat-top as small negative V_G is applied.

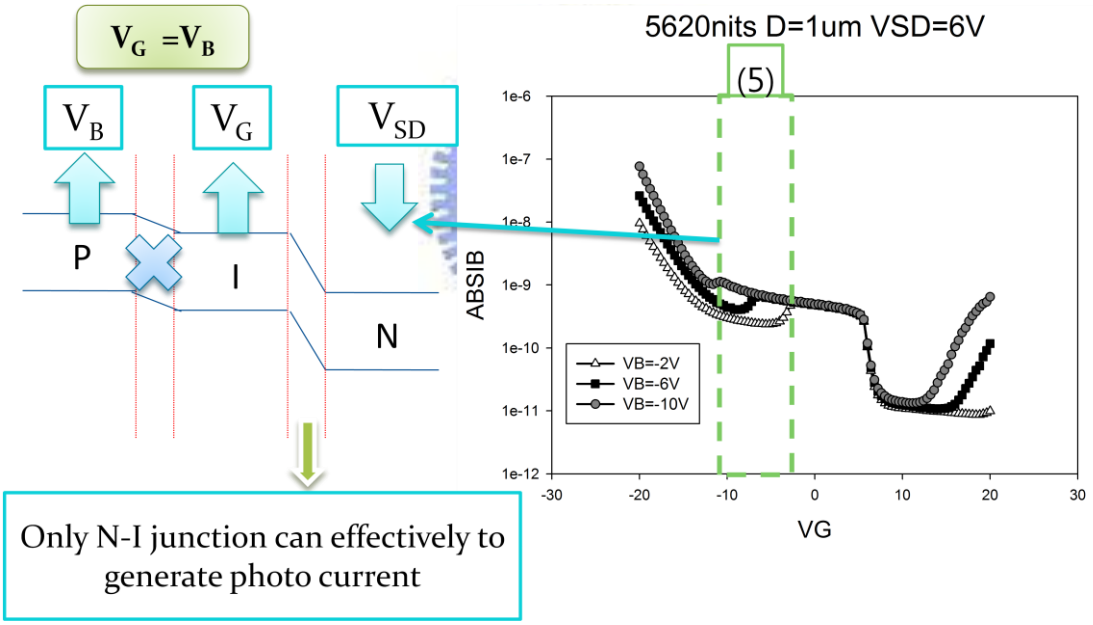


Fig.4. 36 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 5, the LBT current decreases rapidly as negative V_G increase to V_B=V_G. Only N-I junction can effectively to generate photo current.

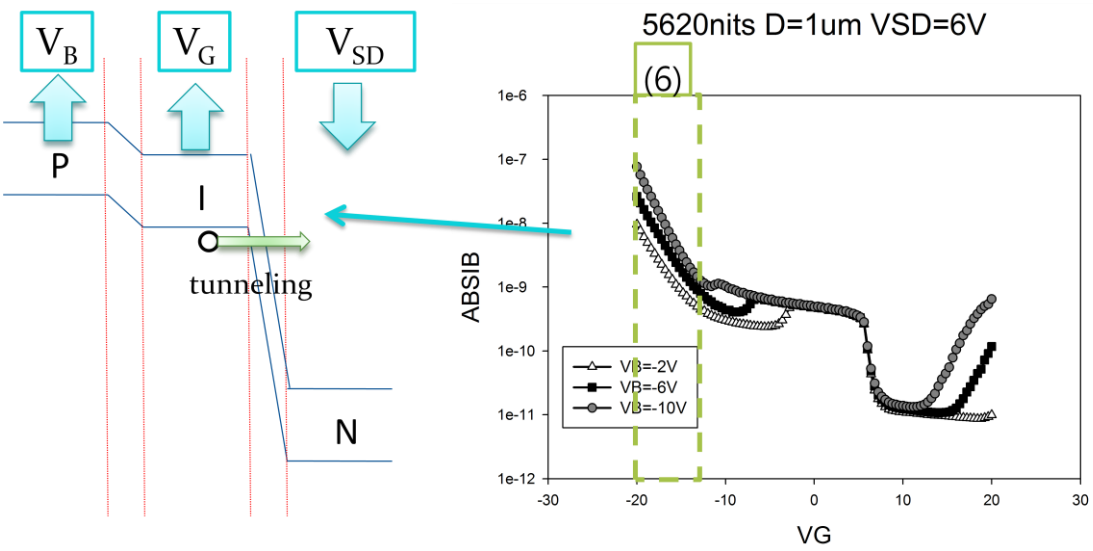


Fig.4. 37 The $ABSI_B$-V_G with fixed V_{SD} in light. For region 6, the tunneling current was occurred as high negative V_G is applied.

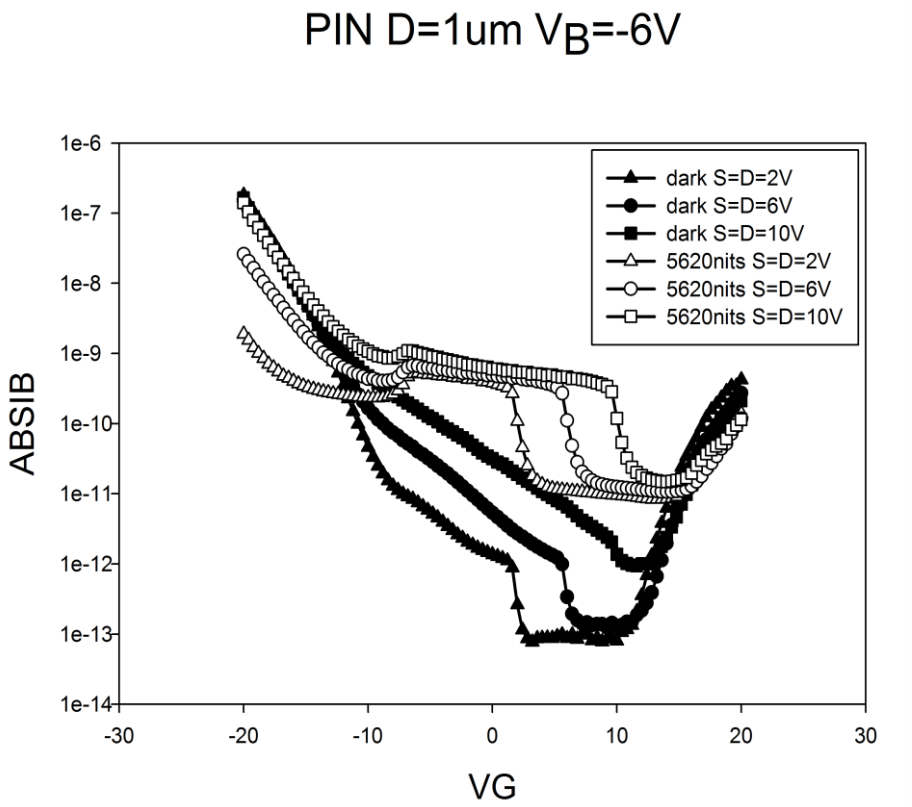


Fig.4. 38 The ABSIB-V_G of LBT TFT with fixed V_B =-6V and varied V_{SD} in Dark and in the brightness of 5620 nit. The black pattern is dark characteristic.

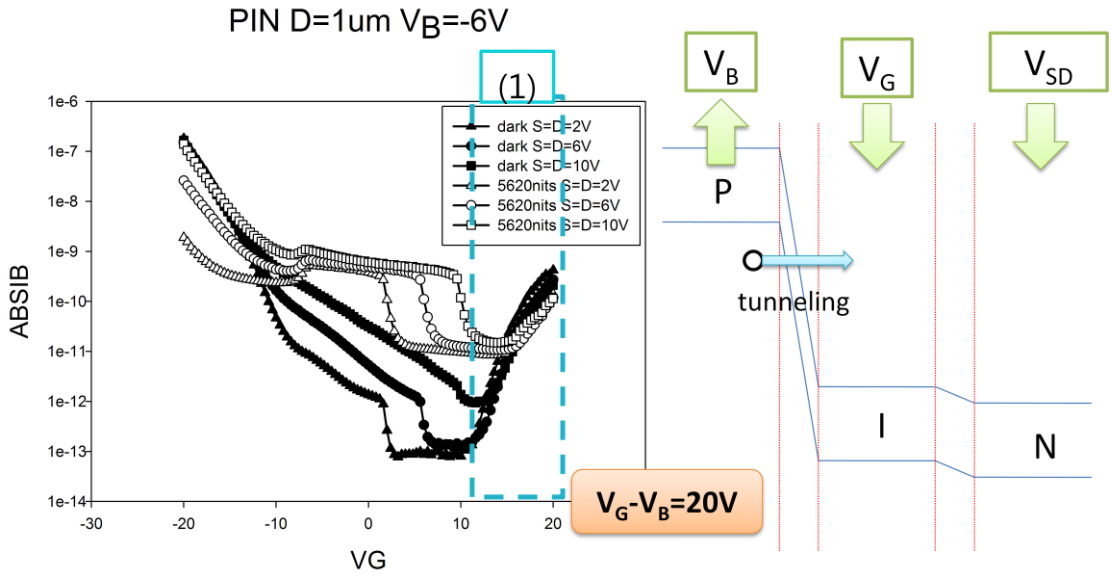


Fig.4. 39 The $ABSI_B$-V_G with fixed V_B in dark. For dark region 1, the tunneling current is occurred as high positive V_G is applied.

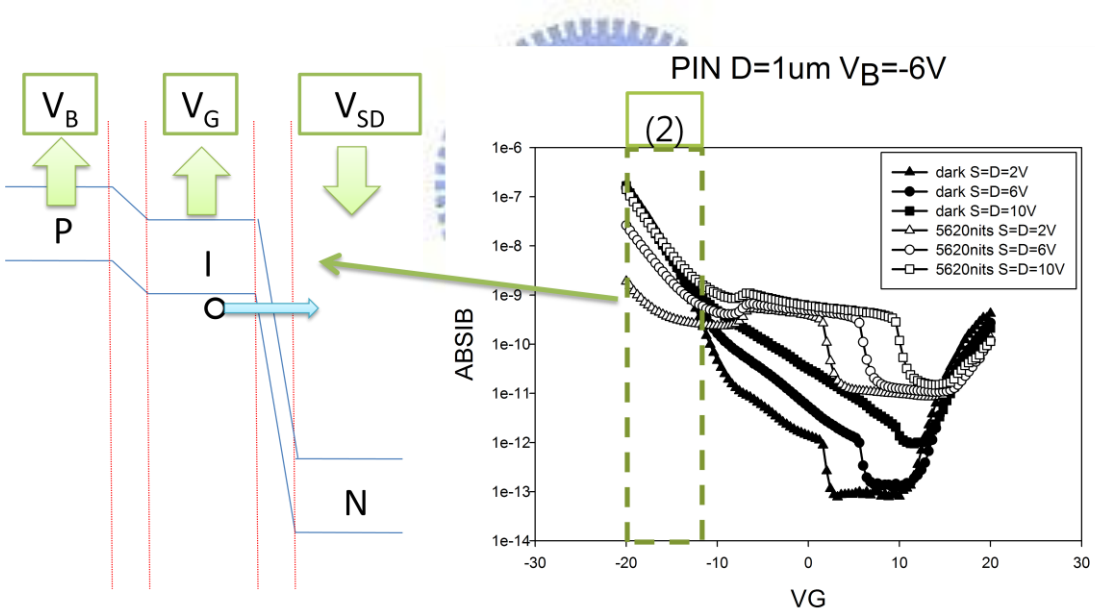


Fig.4. 40 The $ABSI_B$-V_G with fixed V_B in dark. For dark region 2, the tunneling current was occurred as high negative V_G is applied.

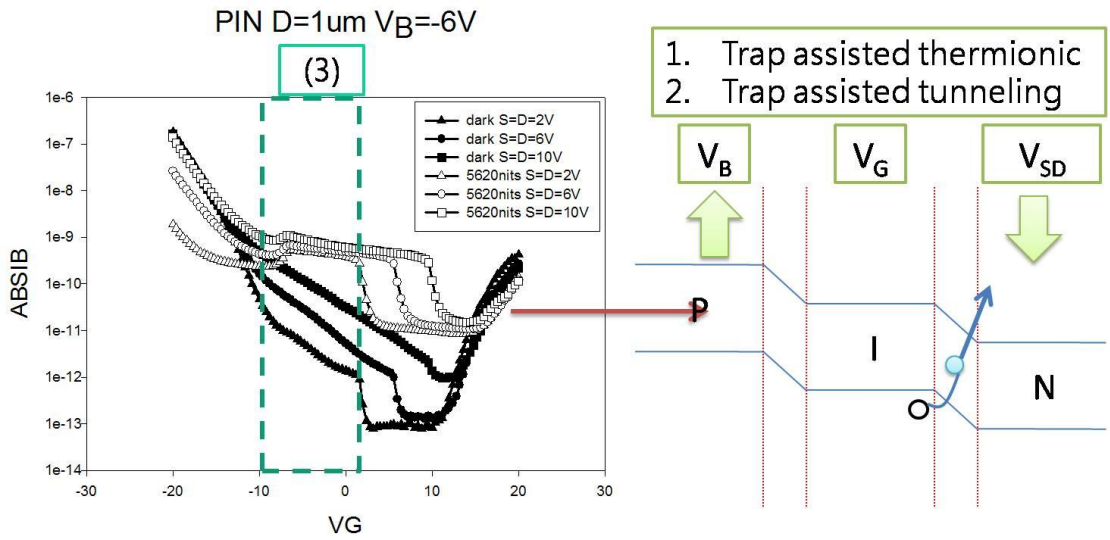


Fig.4. 41 The $ABSI_B$-V_G with fixed V_B in dark. For region 3, because the current is independent of the energy band of p+ region, the current comes from the NI junction.

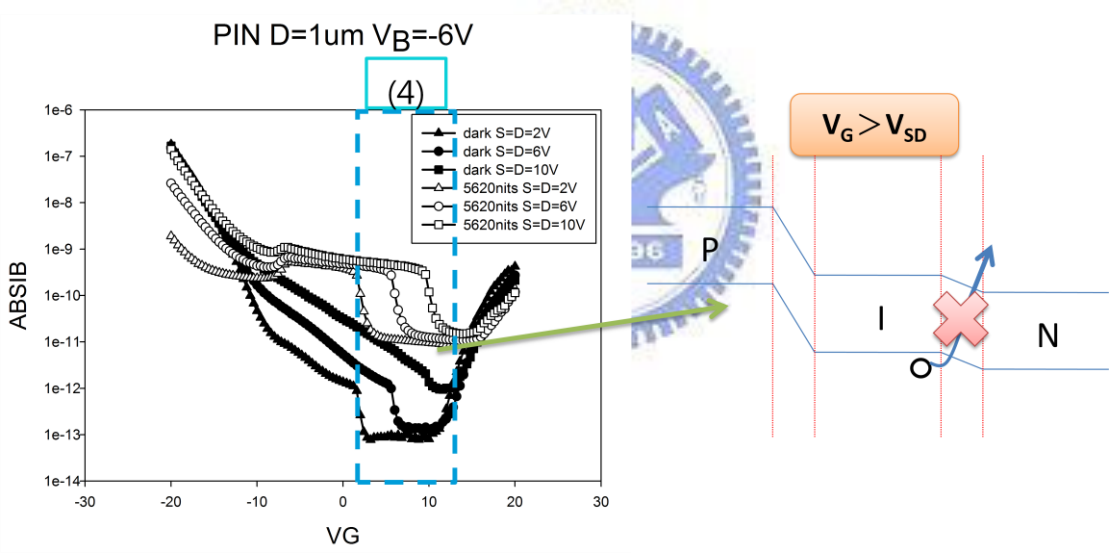


Fig.4. 42 The $ABSI_B$-V_G with fixed V_B in dark. For region 4, the current decreases rapidly as high positive V_G increases.

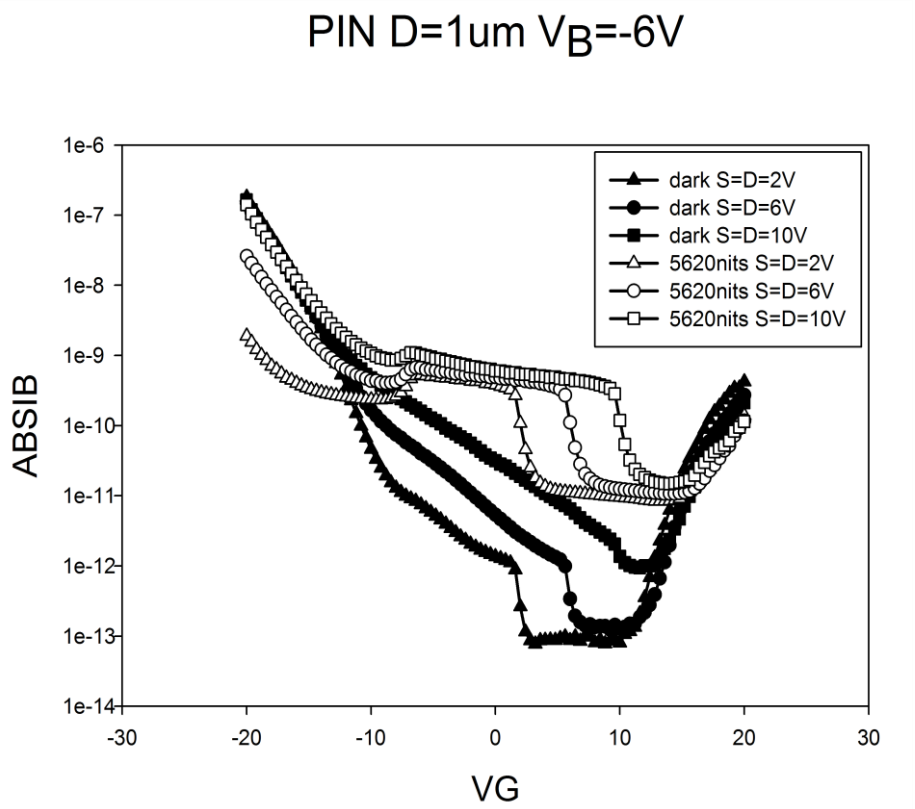


Fig.4. 43 The ABSIB-V_G of LBT TFT with fixed V_B =-6V and varied V_{SD} in Dark and in the brightness of 5620 nit. The white pattern is light characteristic.

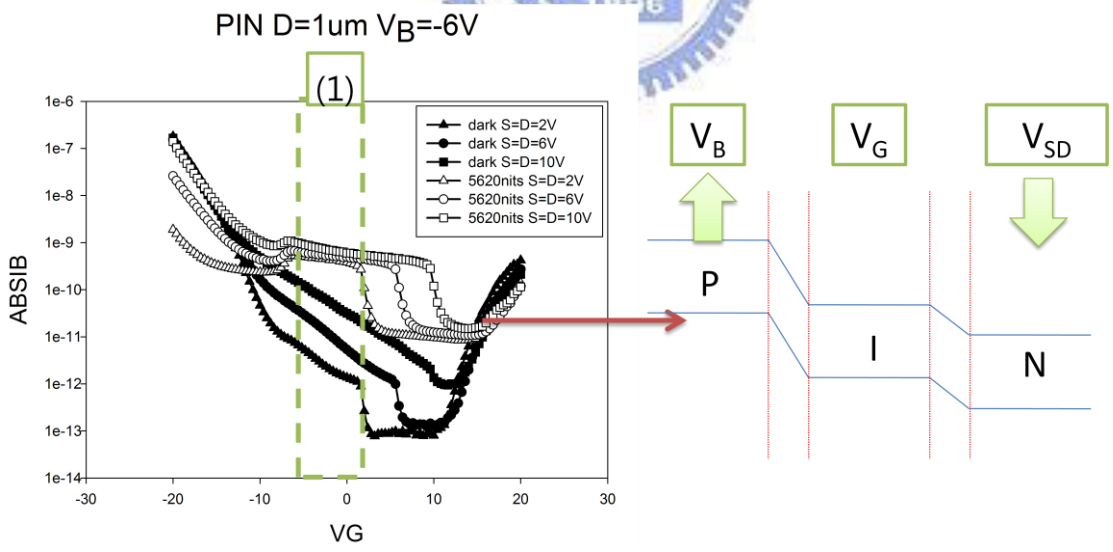


Fig.4. 44 The $ABSI_B$-V_G with fixed V_B in light. For region 1, the photo current is like a flat-top as small V_G is applied.

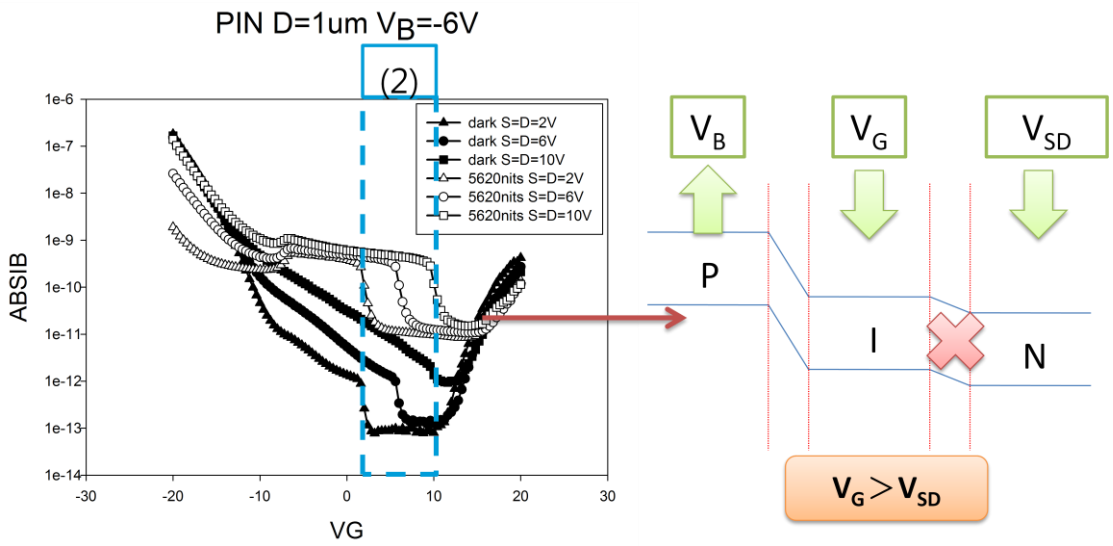


Fig.4. 45 The $ABSI_B$-V_G with fixed V_B in light. For region 2, the LBT current decreases rapidly as positive V_G increase to V_{SD}=V_G. Only P-I junction can effectively to generate photo current.

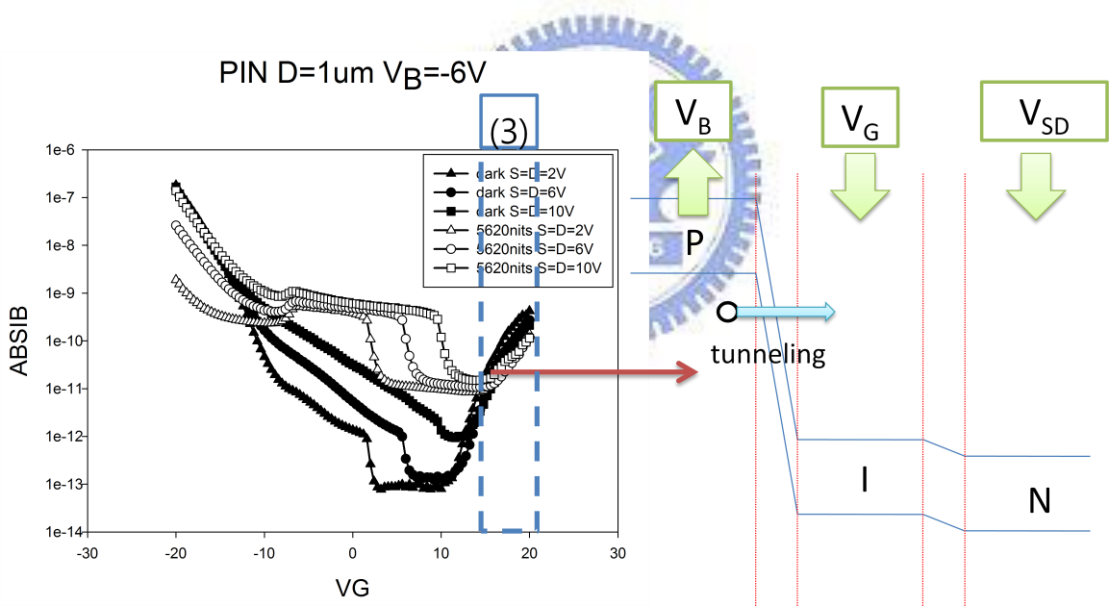


Fig.4. 46 The $ABSI_B$-V_G with fixed V_B in light. For region 3, the tunneling current is occurred as high positive V_G is applied.

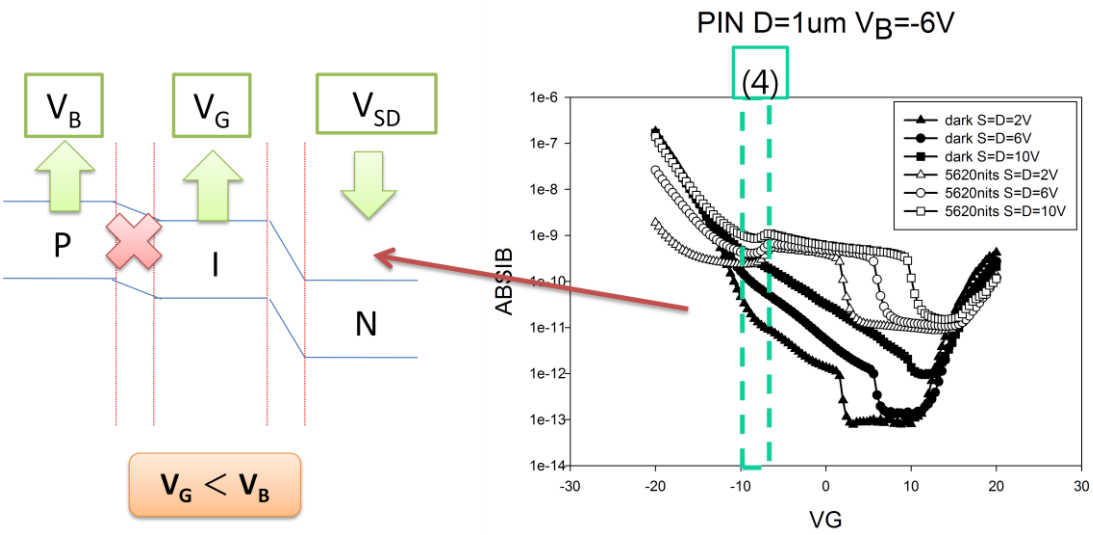


Fig.4. 47 The $ABSI_B$-V_G with fixed V_B in light. For region 4, the LBT current decreases rapidly as negative V_G increase to V_B=V_G. Only N-I junction can effectively to generate photo current.

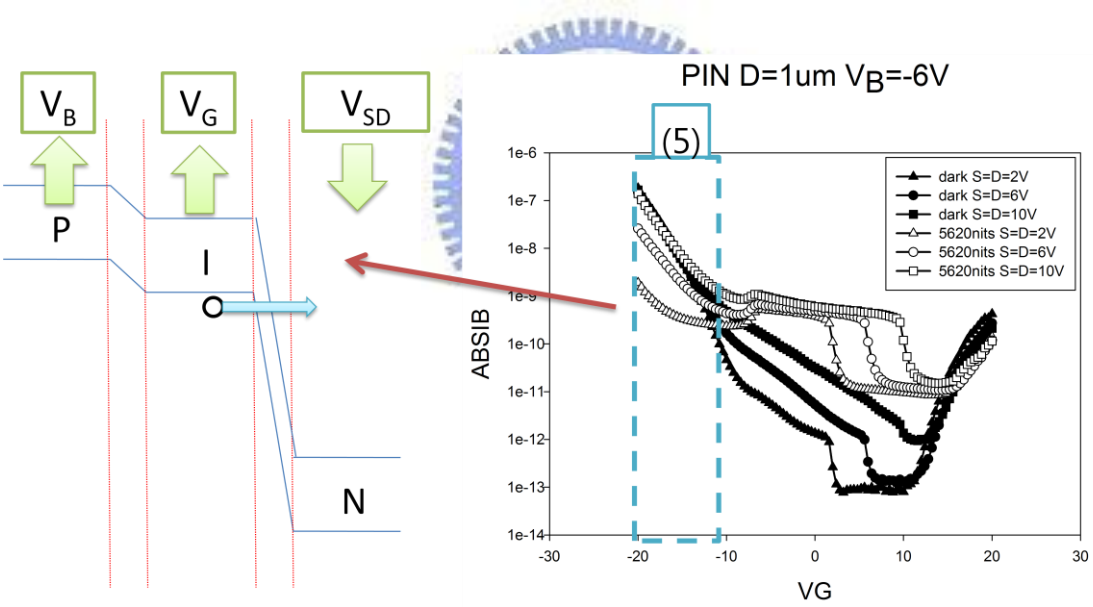


Fig.4. 48 The $ABSI_B$-V_G with fixed V_B in light. For region 5, the tunneling current was occurred as high negative V_G is applied.

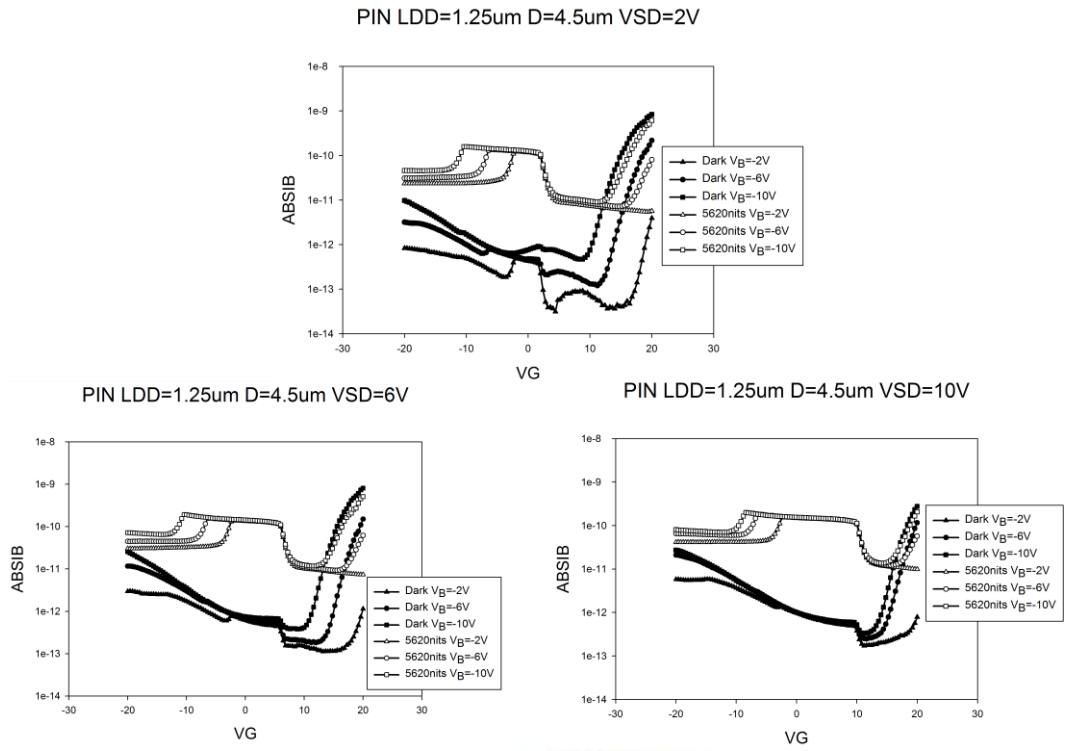


Fig.4. 49 The $ABSI_B$-V_G of LBT TFT with LDD. The $ABSI_B$-V_G with fixed N+ region voltage (V_{SD}=2V, 6V, 10V) and variations in the LBT voltage (V_B=-2V, -6V, -10V) in dark and the brightness of 5620 nit.

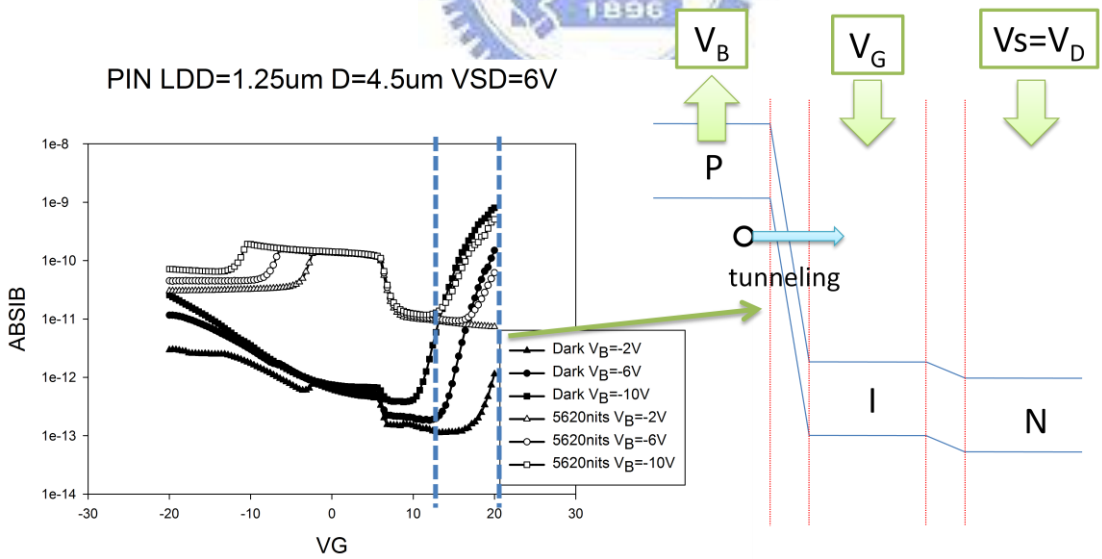


Fig.4. 50 The $ABSI_B$-V_G of LBT TFT with LDD. The tunneling current is occurred as high positive V_G is applied.

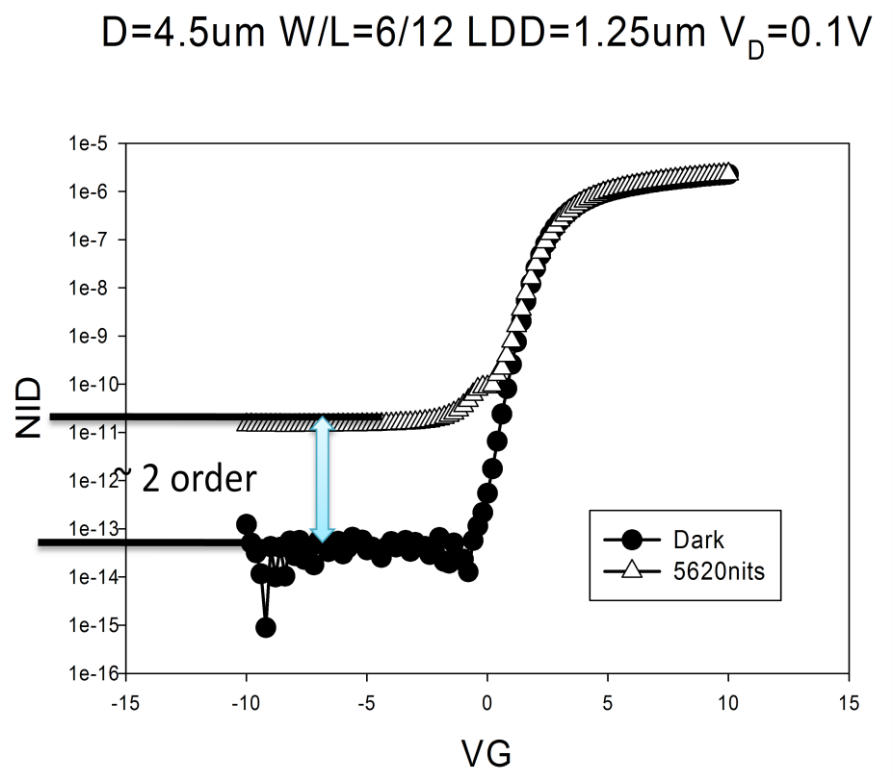


Fig.4. 51 The I_D-V_G of linear region of LBT TFT with LDD in dark and the brightness of 5620 nit

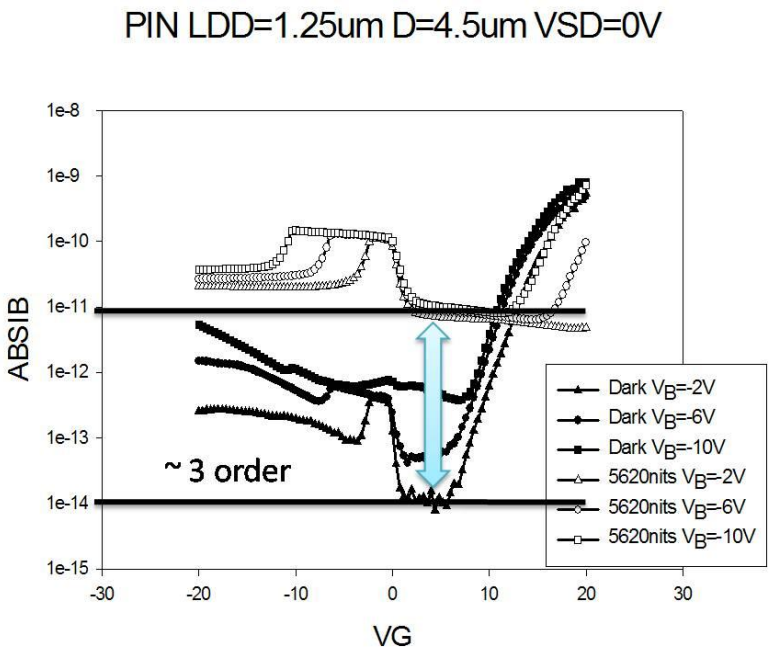


Fig.4. 52 The ABSIB-V_G of LBT TFT in dark and light. As V_{SD}=0V, V_B=-2V, and small V_G is applied, the LBT current increases 3 order from dark to the brightness of 5620 nit.

Table

	C.D. STD	3K-8E11	3K-9E11	3K-2E12	15K-2.8E12
Vth	-0.413	0.925	0.934	2.669	-0.887
Mobility	67.457	66.286	62.127	62.414	80.133
SS	0.263	0.304	0.300	0.3787	0.255
LC	5e-14	1e-14	7e-14	3e-14	2e-14

Table.3- 1 The common TFTs characteristic (V_{th}, mobility, SS, leakage current) with different channel doping.