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分散式控制混合型被動光纖網路之設計成果

Design and Implementation of Novel Distributed Control Hybrid Passive Optical Network

研 究 生：林 文 翔

指導教授：陳 智 弘 老師

中 華 民 國 九 十 七 年 六 月

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摘 要

近年來，數位化資訊的蓬勃發展，網際網路的普及，以往以數據為導向的網路服務漸漸轉成以視頻、語音和數據整合為主，所以用戶需要的網路頻寬也越來越大。以前用的非對稱數位用戶迴路網路系統已不敷使用，然而被動式光纖網路系統可以提供很大的網路頻寬，而受到極大的重視，漸漸取代了非對稱數位用戶迴路網路系統。標準的分時多工、分頻多工被動式光纖網路系統中，時槽和波長的利用是很沒效率的，因為閒置中的時槽或波長無法被共用，而造成頻寬浪費。集中式動態頻寬分配由於封包訊息無法即時的更新，使封包延遲造成即時資料停頓。因此我們提出了一個全新架構的系統：分散式控制混合型被動光纖網路。

分散式控制混合型被動光纖網路結合了分時多工與分波多工技術，以增加網路頻寬和降低成本，分散式動態頻寬分配可以將封包訊息即時的更新，使即時資料不會延遲。我們用元件可程式邏輯閘陣列來實踐光路線終端以及光網路單元，實際的架起一個分散式控制混合型被動光纖網路系統。

Design and Implementation of Novel Distributed Control Hybrid Passive Optical Network

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Abstract

Recently due to digital information flourishing and internet penetrating, formerly data-oriented network services changed into the integration of video, voice, and data. Users need larger and larger bandwidth. ADSL cannot support with bandwidth now, PON gradually replaces ADSL because of larger bandwidth. In the PON network system, TDM-PON and WDM-PON, the use of slot and wavelength is not very efficient since idle in the slot and wavelength cannot be shared. Then centralized control dynamic bandwidth allocation (DBA) cannot update packets information immediately, so it makes real-time data delay. For this reason, we propose a novel system：Distributed Control Hybrid Passive Optical Network (DHPON)

DHPON combines TDM-PON and WDM-PON to increase the network bandwidth and reduce costs, distributed control DBA can update packets information immediately avoiding real-time data delay. We use FPGA to set up optical line terminal (OLT) and optical network unit (ONU) constructing a DHPON system.

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我由衷地感謝每一個幫助我的人，我沒有辜負您們的期盼，我的成就與驕傲全因您們而得，我將一切的榮耀都奉獻給您們，謝謝。

謹將此論文獻給所有愛我及我愛的人

西元 2008 年 6 月 於新竹交大

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CHAPTER 1

Introduction

There are several technologies of broadband access network： digital subscriber line (DSL) , coaxial cable (Cable), passive optical network (PON), and wireless. In recent years, the access network technology is DSL, it includes asymmetric digital subscriber line (ADSL) and very high data rate DSL (VDSL).

The ADSL can operate in parallel with conventional analogue voice telephony over the same line. Asymmetric means that a higher speed is available from the exchange to the user (downstream) and a slower speed from the user to the exchange (upstream). Capability varies with distance - up to 8 Mbps downstream can be supported up to 2 km and 2 Mbps up to 5 km. 64 kbps is the usual speed in upstream. Then, VDSL is a new technology; it is expected to provide speed as high as 52 Mbps in downstream, but over shorter distances than ADSL - 20 Mbps in 1 km and 52 Mps in 0.3 km, and between 1.5 and 2.3 Mbps upstream [1].

In the meantime, at the user end, the drastic improvement of the performance of digital electronics and the computers has made possible expanding multimedia services such as video on demand, videoconferencing, high definition TV (HD-TV), e-learning, interactive games, voice over IP (VoIP), and others. The bandwidth of DSL cannot satisfy users. PON is considered an ultimate solution to meet higher bandwidth requirements in access network.

PON is a single, shared optical fiber that uses inexpensive optical splitters to divide the single fiber into separate strands feeding individual subscribers. PON is called "passive"

because, other than at the central office (CO) and subscriber endpoints, there are no active electronics within the access network.

The main advantage of PON is that it requires less wiring than point to point, that it mutualisms the service for several subscribers, and that it has no active element beyond the central exchange, in other words, only optical fibers and optical passive elements do not require any electrical power or active management. In addition, the lifetime of the outside passive plant should be greater than 25 years to justify the installation costs and maximize the savings in operational expenses.

There are several standard of PON to provide access network: APON (ATM PON), BPON (Broadband PON), GPON (gigabit PON), and EPON (Ethernet PON). BPON can provide 622Mbps in downstream to support 32 users, GPON can provide 2.488Gbps in downstream to support 64 users, and EPON can provide 1Gbps in downstream to support 16 users [2]. The bandwidth of per user of these competing technologies is shown as Table 1.1.

Service	Users	Bandwidth/User	Range
ADSL	1	2 Mb/s	5 Km
VDSL	1	20 Mb/s	1 Km
BPON	32	20 Mb/s	20 Km
GPON	64	40 Mb/s	20 Km
EPON	16	60 Mb/s	20 Km

Table 1.1. Bandwidth of per User

Although there is high bandwidth in PON, it is a fatal disadvantage, which is that round trip time (RTT) is too long. It causes the data packet information doesn't update immediately, that induces data packet delay and the waste of bandwidth, so we provide a new network structure: Distributed Control Hybrid Passive Optical Network to solve the problem. I will introduce in detail in the chapter 2.

CHAPTER 2

Conventional and Novel Architecture of PON

I will introduce several types of HTTx and technologies about PON in this chapter.

2.1 Passive Optical Network Overview

The architecture of Passive Optical Network is shown as Fig.2.1.

As Fig.2.1 show, passive optical network (PON) is a kind of tree topology. Optical Line Terminal (OLT) is the main element of the network, and it is usually placed in the local exchange. Optical Network Unit (ONU) serves as an interface to the network, and it is deployed on a customers' side. ONU connects to OLT by means of optical fiber, and there is no active element in PON. PON is a kind of a Point-to-Multiple-Points technology. A single OLT can serve several ONUs. An ONU can serve as a point of access for many customers, and be deployed at customers' houses (Fiber to the Home, FTTH), in buildings (Fiber to the Building, HTTB), or on the streets (Fiber to the Curb, HTTC) [3].

The data are sent to each ONU through the splitter by OLT. In downstream, although the structure and power are the same, the data signals are attenuated. In upstream, the data signals are from each ONU to OLT, the direction and condition are opposite to those of downstream. The data signals from each ONU at different time and arrive at the input of the splitter. After all data signals from each ONU traverse through the splitter, they are combined with each other. Then the mixture of all data signals is received by OLT. To avoid the interference of data from each ONU in upstream, we apply Time Division Multiple Access (TDMA) method or Wavelength Division Multiple (WDM) method.

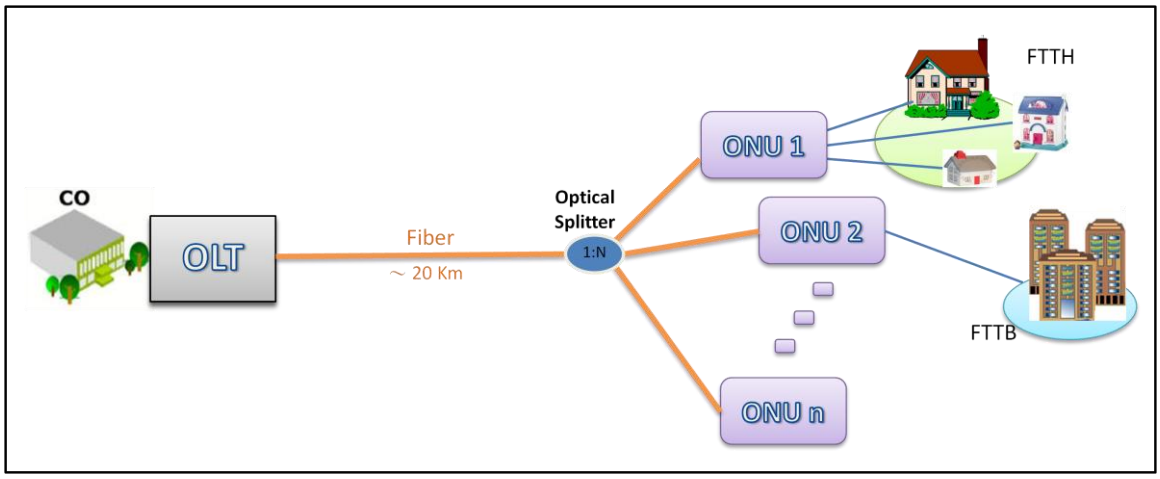

Figure 2.1 The Architecture of Passive Optical Network

2.2 Time Division Multiplexed PON

FTTX has been a long-cherished goal for carriers. The Time Division Multiplexed Passive Optical Network (TDM-PON) architecture as we know it today an economical method of sharing a single fiber and central office (CO) transceiver among many customers-was conceived in the late 1980s, when FTTX concepts were first developed.

The architecture of TDM-PON is shown as Fig 2.2. The main concept behind the TDM approach is to use a single high-performance shared transceiver at the central office to communicate with the “n” remote ONU transceivers. This approach requires the use of a 1 x n optical splitter to divide the optical power equally between the multiple ONUs. Since each remote ONU uses the same upstream wavelength, they must all take turns using dedicated and variable time slots where only a single ONU is allowed to transmit. A relatively complex processor located at the OLT controls the management and assignment of these individual transmission time slots. In the downstream direction a single data wavelength is used to broadcast to all the users. The ONUs identify their specific data packets by address information located in the header bit streams.

This traditional single-wavelength PONs combine the high capacity provided by optical fiber with the low installation and maintenance cost of a passive infrastructure. The optical carrier is shared by means of a passive splitter among all the subscribers. As a consequence, the number of ONUs is limited because of the splitter attenuation and the working bit rate of the transceivers in the central office (CO) and in the ONUs. Current specifications allow for 32 ONUs at a maximum distance of 20 km from the OLT and 64 ONUs at a maximum distance of 10 km from the OLT.

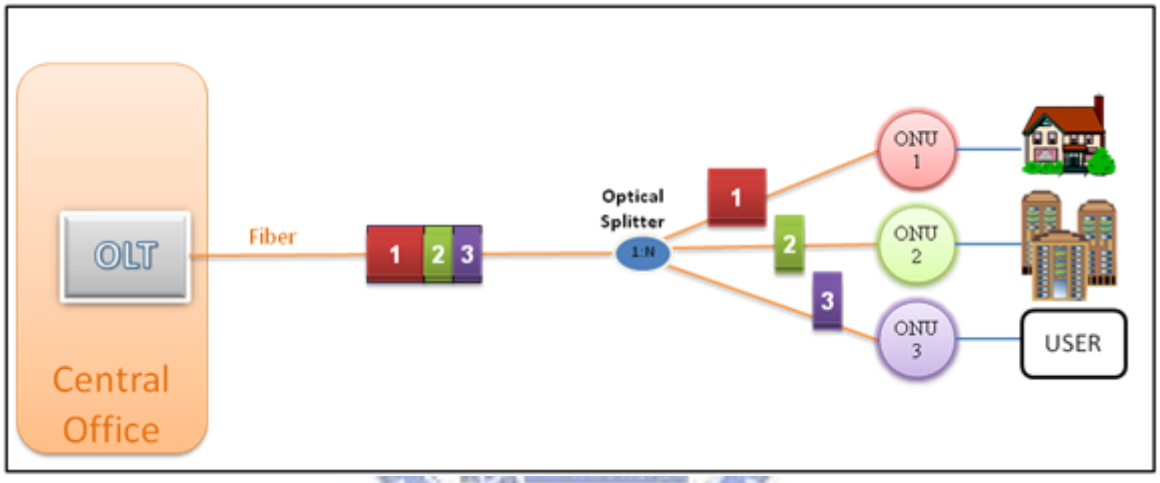

Figure 2.2 The Architecture of TDM-PON

TDM-PON has been developed for a long time such as ATM-PON (A-PON), Broadband-PON (B-PON), Gigabit-PON (G-PON), and Ethernet-PON (E-PON).

2.2.1 Broadband PON

The broadband PON (BPON) was first introduced, and it was accepted in 1996 by International Telecommunications Union (ITU). The standard was endorsed by a number of network providers and equipment vendors which cooperated together in the Full Service Network Access (FSAN) group. The FSAN group proposed the Asynchronous Transfer Mode (ATM) protocol should be used to carry users' data, and sometimes access

networks based on this standard are referred to as APONs.

The architecture of BPON is flexible and adapts well to different scenarios. The underlying ATM protocol provides support for different types of service by means of adaptation layers. The small size of ATM cells and the use of virtual channels and links allow allocating available bandwidth to the end users with a fine granularity. Moreover, the deployment of ATM in a backbone of metropolitan networks and easy mapping into SDH/SONET containers allows the use of only one protocol from one end user to another.

Yet, the advantages of ATM proved to be the main obstacle in deployment of BPON and despite many field trails BPON did not gain much popularity. The complexity of the ATM protocol was hard to implement and in many cases superfluous. Much simpler, data only oriented Ethernet protocols found a widespread use in local area networks and started to replace ATM in many metropolitan area and backbone networks [4].

2.2.2 Gigabit PON

In May, 2001, almost at the same time as EDMA presenting the concept of EPON, FSAN organization also started to set the standard of GPON, the object is not only operating at higher speed (up to 2.4GB/s) but also there is much higher efficiency than other PON in multi-work, operation, administration, maintenance and provisioning, (OAM&P),and expander. Finally at the beginning of 2003, ITU-T approved the standard of GPON in G984.1, G984.2, and G984.3. According to the standard, GPON can provide the bandwidth for 1.244 Gb/s in upstream and 2.488 Gb/s in downstream. The distance of transmission covers at least 20 km, which is three times longer than 6km of ADSL. However as a whole, GPON is better than BPON and EPON in video, voice, and data.

Although GPON is high performance in transmission, GPON is too expensive to use widespread.

2.2.3 Ethernet PON

At the beginning of 2001,IEEE set up 802.3 Ethernet in the First Mile to develop Ethernet network standard. EPON is the technology combine Ethernet with PON, it use standard format to load IP work without conversion, ONU can collect to a simple facility without adding extra exchange function. At the same time EPON doesn't require the expensive and complicated ATM and SONET, in order to simplify the network and share users with low-cost distribution of the bandwidth. Therefore, EPON is cheaper, wider bandwidth, and stronger in service than BPON and GPON.

EPON still use broadcasting method in downstream, by OLT sending Ethernet packet to ONT, every packet would record the address of destination, after receiving packet, ONU access packet of their own and throw others way; upstream is still in TDMA method, controlling slot signal is sent by OLT, the signal control ONUs packet of upstream in order. The length of EPON's upstream and downstream formats are both 2 ms, it is shown as Fig. 2.3, upstream format consists of a Header and many variable-length slots, every ONT has a corresponding slot, it contains the packet sending to OLT, some information about slots , and control bit. If ONU didn't send the data to slot which is allocated, it must be to fill the empty slot bytes, avoiding conflict at the compound. The downstream format also consists of many variable-length slots, in each slot in a byte contains the synchronization message signs, let ONU and OLT make a every 2 ms synchronal sending. EPON can provide 1Gb/s both in upstream and downstream [5]. Table 2.1 compares tree standardized TDM-PON : BPON, GPON ,and EPON.

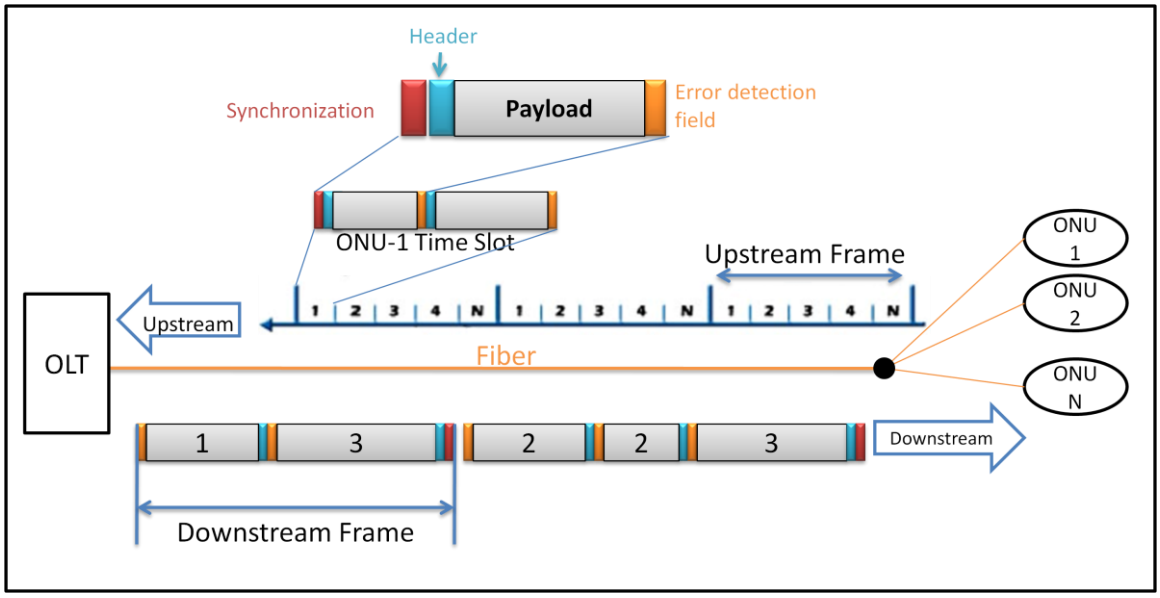

Figure 2.3 Upstream and Downstream Formats of EPON

	BPON	GPON	EPON
Stranded	ITU G.983	ITU G.984	IEEE 802.3ah
Framing	ATM	GEM/ATM	Ethernet
Max Bandwidth	622 Mb/s	2.488 Gb/s	1 Gb/s
Users/PON	32	64	16
Avg. Bandwidth/User	20Mb/s	40Mb/s	60Mb/s
Video	RF	RF/IP	RF/IP
Estimated Cost	Medium	high	Low

Table 2.1 Comparison of TDM-PON

2.3 Wavelength Division Multiplexed PON

The architecture of WDM-PON is shown as Fig. 2.4. The straightforward approach to build a WDM-PON is to reserve a separate wavelength channel from the OLT to each

ONU, for each upstream and downstream direction. In other word, each ONU gets a dedicated point-to-point optical channel to the OLT, so data collision will not happen when OUNs send out data simultaneously. In downstream, the specific wavelength channel is divided to specific ONU by a passive arrayed wavelength grating (AWG). In upstream, the function of AWG is like an optical filter. Because there is a specific wavelength for each OUN, which cannot be shared, so the cost of WDM-PON is very expensive [6].

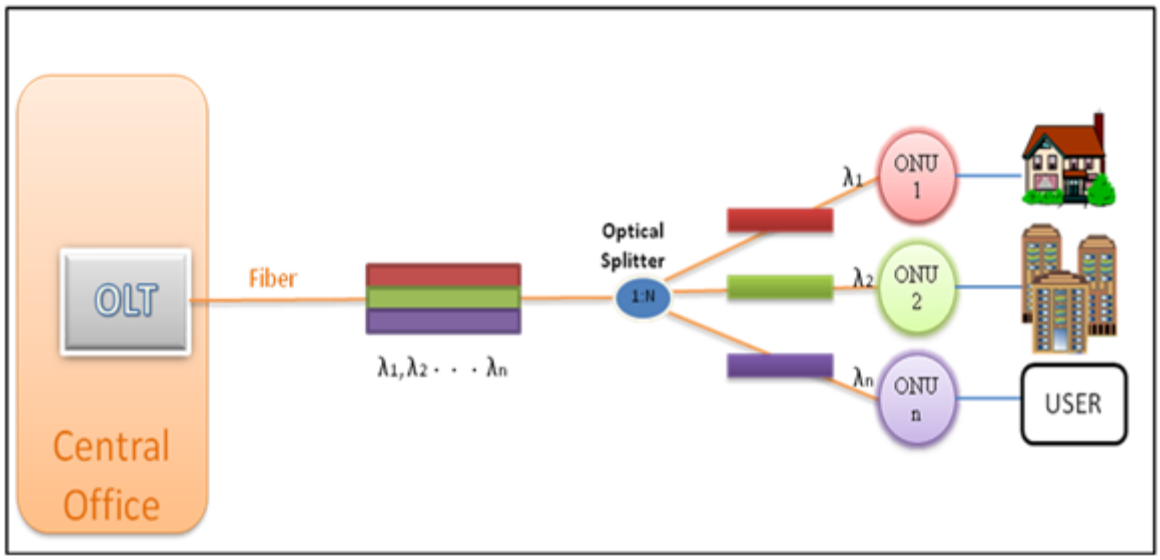

Figure 2.4 The Architecture of WDM-PON

2.4 Centralized Control Dynamic Bandwidth Allocation

The centralized control Dynamic Bandwidth Allocation (DBA) is shown as Fig. 2.5. the ‘centralized’ means that DBA control signal is sent form ONUs to OLT with the same wavelength as the one of data channel. ONUs send the buffer information to the OLT, then the OLT send the acknowledgement character signal to each ONU, after OLT receive the the buffer information. The prevailing method of centralized control DBA scheme is Interleaved Polling with Adaptive Cycle Time (IPACT) [7].

2.4.1 Interleaved Polling with Adaptive Cycle Time (IPACT)

In an IPACT scheme. ONU will send a message at the end of its data packets. The message is about that how many packets in its buffer want be sent at next time. As Fig. 2.5, the ONU that is scheduled next (say, in round-robin fashion) will monitor the transmission of the previous ONU and will time its transmission such that it arrives to the OLT right after the transmission from the previous ONU. Thus, theoretically, there will be no data collision and no bandwidth will be wasted [8].

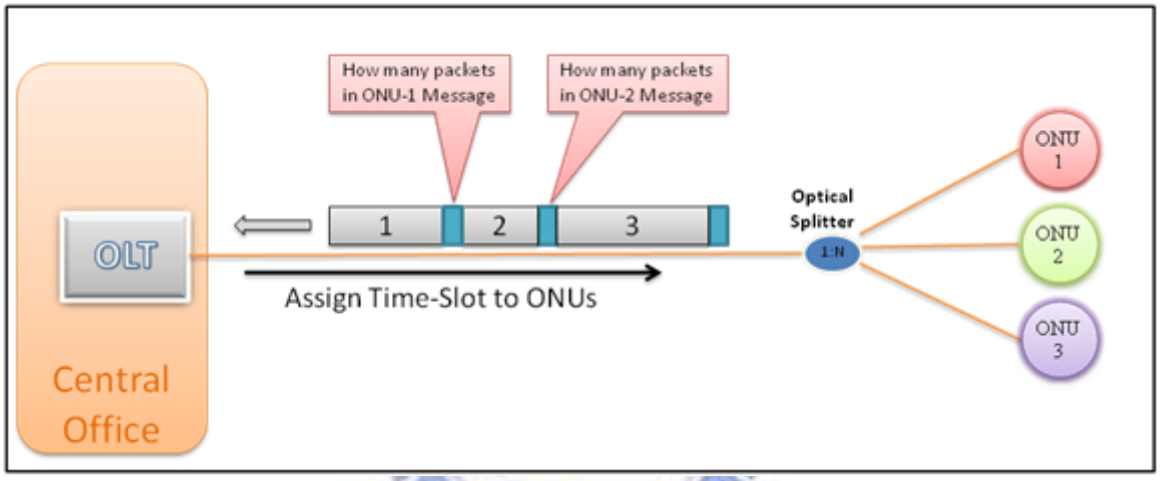

Figure 2.5 Concept of Centralized-Control DBA

For example as Fig. 2.6, we suppose that there are three ONUs and round trip time (RTT) of each ONU is 5 slot time. At first, there is not packet in each ONU, in other words, the queue size (Q-size) of packet of each ONU is zero. The OLT ask each ONU that how many packets be stored in the buffer. Then each ONU send an abbreviation to OLT, the abbreviation is a message with Q-size of packet in the buffer. After OLT receiver the message of each ONU, it will assign the slot of transmission to each ONU. After ONU finish the data transmission, it send the new Q-size of packet to OLT. As Fig. 2.6, the shadow means the slots be not used, so the bandwidth will be waste. This is a disadvantage of IPACT.

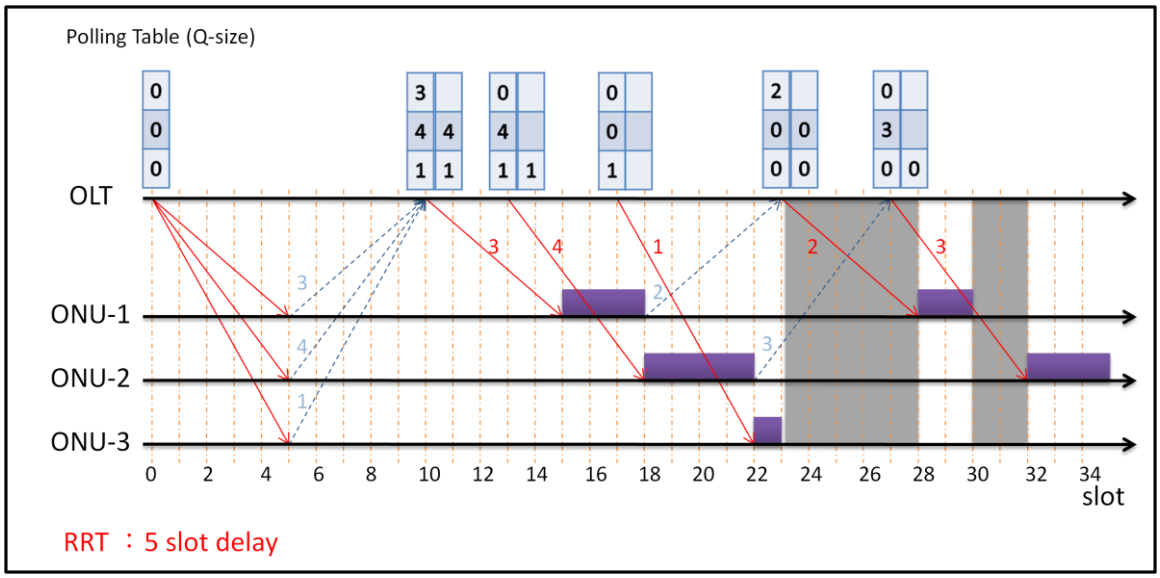

Figure 2.6 Example of IPACT

2.4.2 Round Trip Time

RTT is the key point of the PON structure, it means the required time for a signal from ONU to OLT. The calculation of RTT is shown as the Fig. 2.7. In the illustration, the signal is from ONU at T1, and the signal arrive OLT at T2, then the RTT is 2*(T2-T1). The distance from OLT to ONU is usually larger than 20 kilometers, which is very far, so RTT would be long in result (usually about 0.2 ms). If RTT is long, the DBA Q-size signal will not be updated immediately and the packet of data packet will be delay. The situation is not good to DBA. It makes real- time data, such as online games and videoconferencing, lagged. This is the main shortcoming of centralized control DBA. Based on the problem, we provide a novel architecture of DBA, Distributed Control Dynamic Bandwidth Allocation, to reduce RTT. We hope the method will improve centralized control DBA.

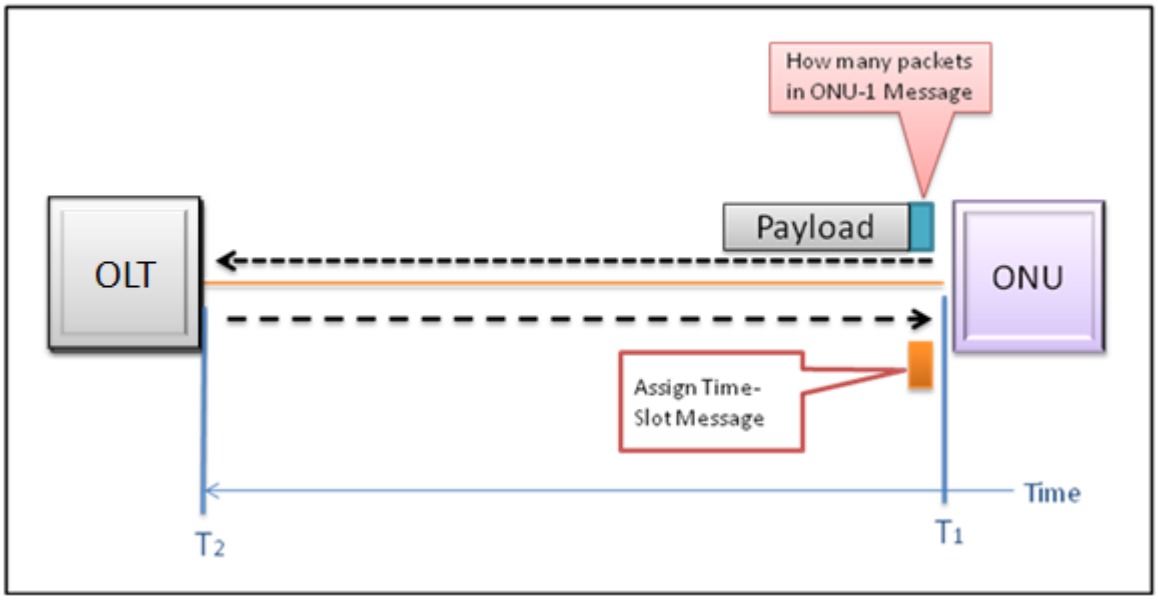

Figure 2.7 Round Trip Time of Centralized Control DBA

2.5 Distributed Control Dynamic Bandwidth Allocation

The architecture of distributed control DBA is shown as Fig. 2.8. Distributed control DBA means DBA control message isn't transmitted to OLT. In this method, DBA control message is transmitted to the splitter by each ONU with 1550nm- wavelength and goes back to each ONU directly, then DBA control signal of all ONUs could be received by each ONU. After gathering DBA control message of all ONUs, each ONU will determine to transmit the data or not by itself. Because the distance between ONU and the splitter (about 1 Km) is shorter than that between ONU and OLT, it will shorten RTT (about 0.01 ms) dramatically.

The main advantage of Distributed control DBA is that the DBA control signal will be updated immediately and the packet of data will not be delayed. The technology makes real-time data not lagged. It could be applied to online games and videoconferencing, and makes displays smooth.

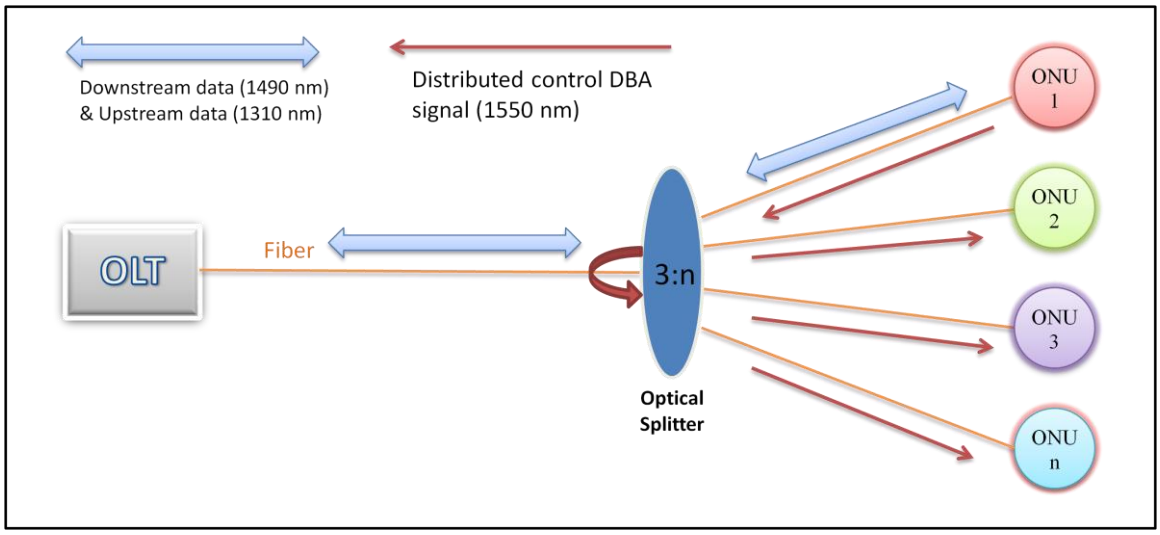

Figure 2.8 The Architecture Distributed Control DBA

2.6 Distributed Control Hybrid Passive Optical Network

We create a new architecture of passive optical network: Distributed Control Hybrid Passive Optical Network (DHPON). DHPON is based on EPON and combines with TDM-PON, WDM-PON and distributed control DBA to become a passive optical network with high bandwidth, short RTT, low cost, and simple structure. The architecture of DHPON is shown as Fig. 2.9. In this paper, I focus on the combination of TDMA and distributed control DBA.

2.6.1 DHPON Structure

As Fig. 2.9, the sub-PON is between the AWG (Arrayed Waveguide Grating) and an ONU. We use TDMA technology in each sub-PON, and it assigns a wavelength to each sub-PON. Because the distributed control DBA will share bandwidth with each ONU, a wavelength can service several ONUs. Furthermore, we use WDM technology to service several sub-PONs [9].

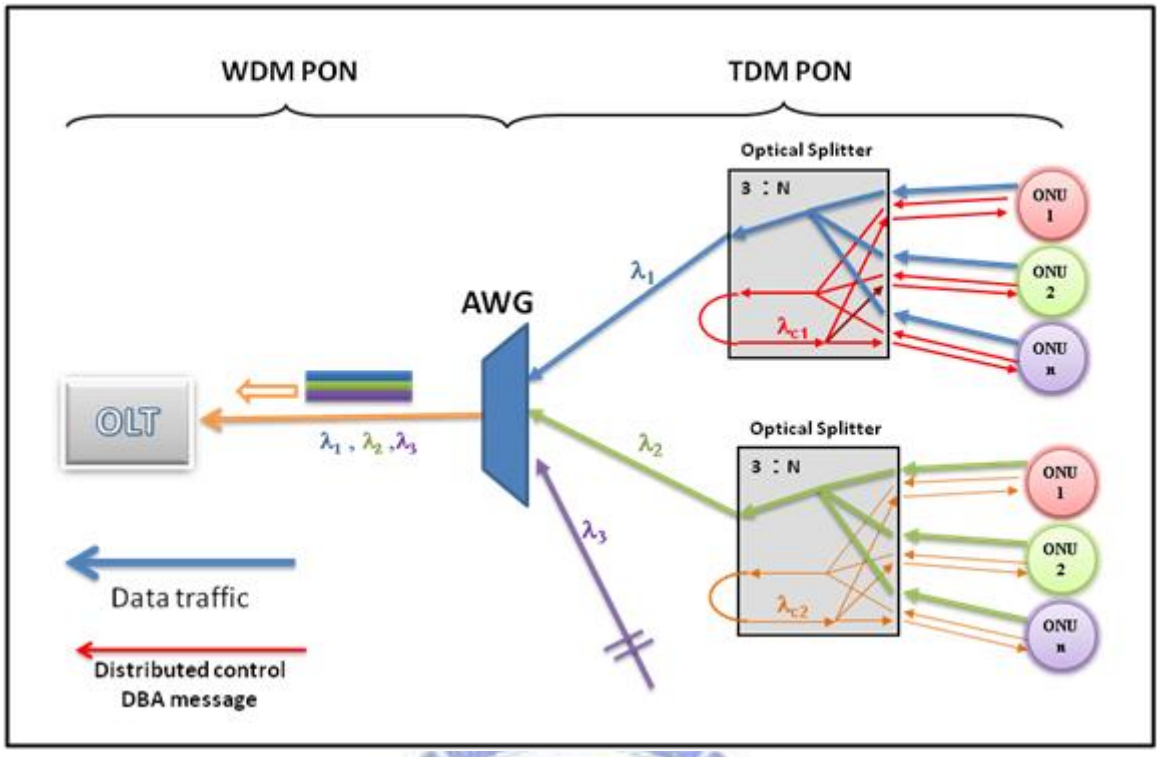

Figure 2.9 The Architecture of DHPON

2.6.2 Concept of the Distributed Control DBA

A basic concept of DHPON is shown as Fig. 2.10. Each ONU transmits its update DBA control message with λc1. The DBA control message contains (Q-size) information of ONU's buffer and goes back to all ONUs directly after going across the splitter. Because the data traffic and control messages are transmitted independently, the Q-sizes of ONUs are updated immediately and efficiently.

After each ONU receives the DBA control messages of all ONUs, each ONU uses the DBA algorithm to determine whether transmitting the data or not. At one moment, only single ONU can deliver data. If not, it will cause data to collide. Distributed control DBA is the main method to distribute bandwidth to avoid the data colliding [10].

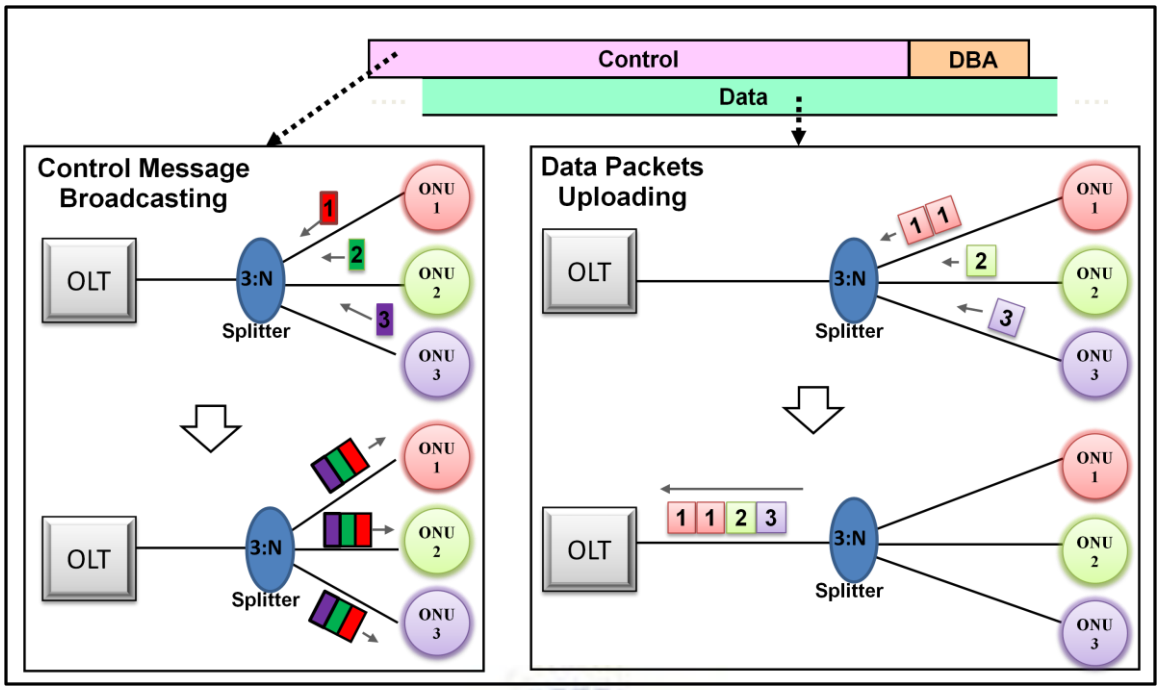

Figure 2.10 Basic Concept of Distributed Control DBA

2.6.3 An Example of the Distributed Control DBA

As Fig. 2.11, the DBA control message carries the packet Q-size of each ONU. Each ONU sends the Q-size message to the splitter and the message will be sent back to all ONUs. Each ONU can receive the Packet Q-size message of all ONUs. Then each ONU will determine whether delivering the data by itself or not.

We can see Fig. 2.12. In the first slot, the packet Q-size of the ONU1 is 2, the Packet Q-size of the ONU2 is 6, and the Packet Q-size of the ONU3 is 0. Because the Packet Q-size of the ONU2 is the largest, only ONU2 will transmit a date packet in the process of next slot.

It means that DBA control message of this slot will determine the data traffic of the next slot.

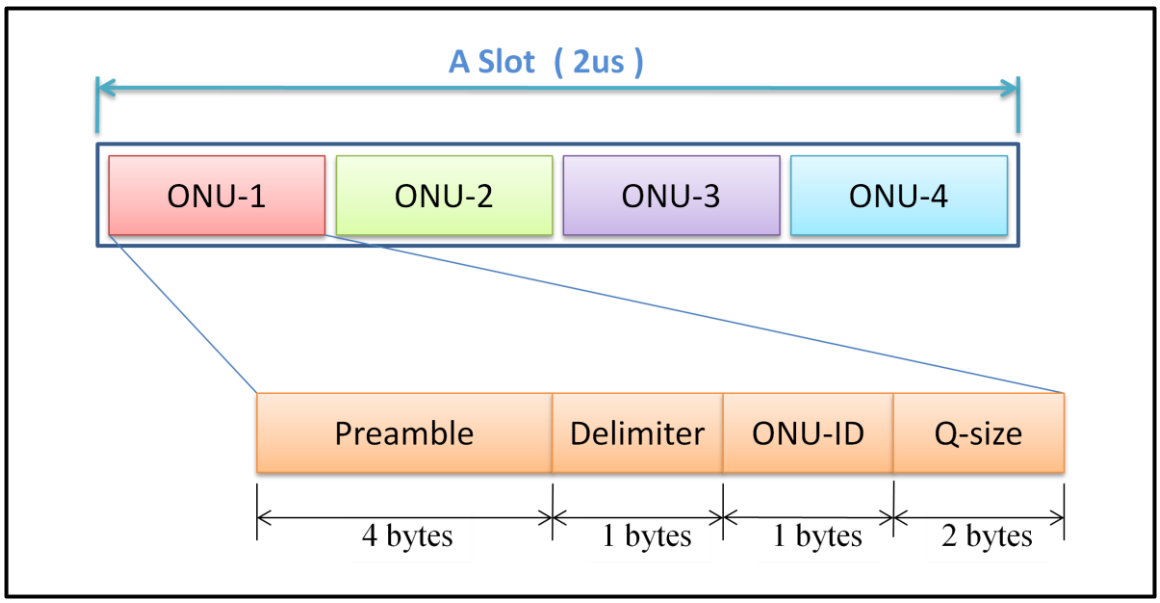

Figure 2.11 DBA Control Message of an ONU

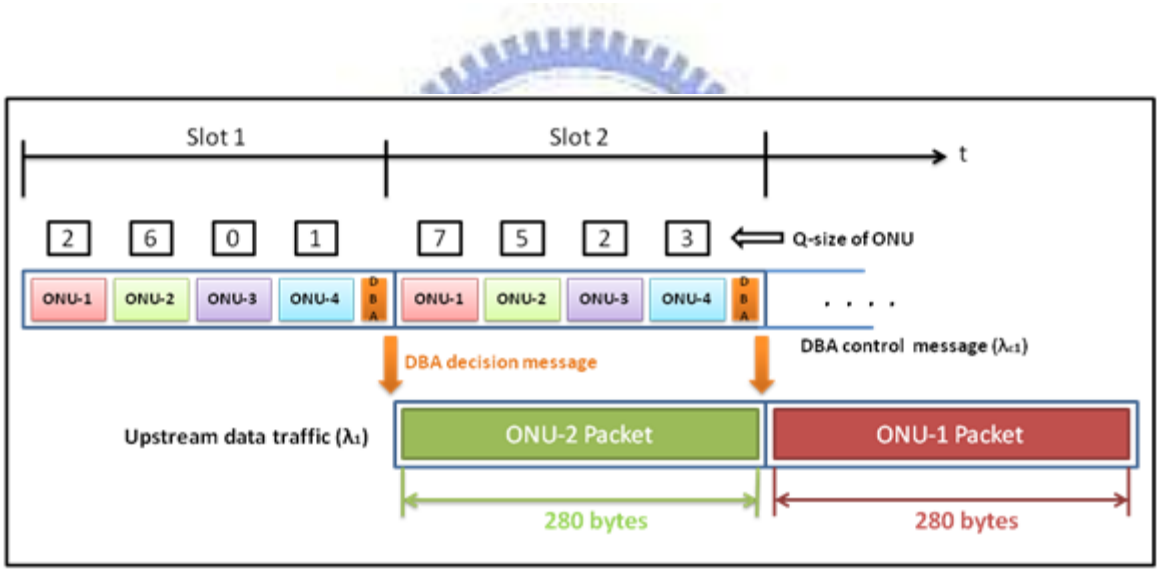

Figure 2.12 An Example of Distributed Control DBA

2.6.4 The Data Traffic of DHPON

In downstream, DHPON transmits data packets by broadcasting method. OLT transmits data packets to each ONU with 1490-nm-wavelength and 1.25 Gb/s data rate in downstream.

In upstream, DHPON transmits data packets by TDMA technology and Distributed

control DBA. Each ONU transmits data packets to OLT with 1310-nm-wavelength and 1.25 Gb/s data rate in upstream. The wavelength of distributed control DBA control signal is 1550 nm, and its control signal data rate is 125 Mbps.

In conclusion, the methods of transmitting data packets in downstream and upstream are totally different.

2.6.5 Advantage of DHPON

We will compare between distributed control DBA and centralized control DBA. The prevailing of centralized control DBA is IPACT. it has a fatal disadvantage. The RTT is long. The long RTT will make to packet of data mean delay. We have simulated to prove that. We assume a 32 ONUs scheme and are operated under different traffic load. The distance between OLT and ONU are 10 Km, 20Km and 30Km. Then the packet mean delay. is shown as Fig. 2.13. We can see as Fig. 2.13, the packet mean delay of IPACT increases rapidly, when the traffic load is over 0.7. And DHPON almost have no packet mean delay, because the RTT of DHPON is very short.

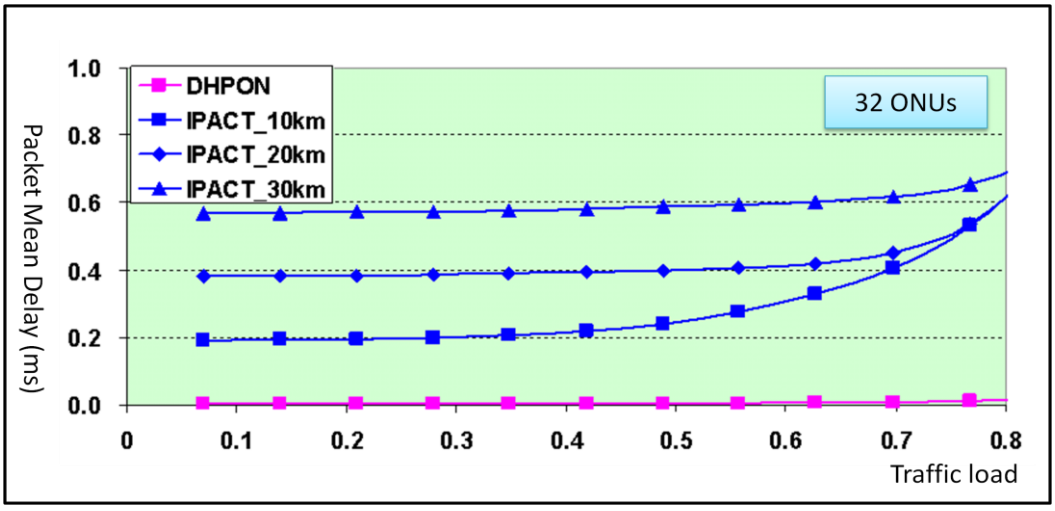

Figure 2.13 Packet Mean Delay of DHPON and IPACT

CHAPTER 3

Distributed Control Hybrid Passive Optical Network

In this chapter, we will explain the data format and the important module of DHPON.

In our experiment, we use Field Programmable Gate Array (FPGA) to implement OLT and ONU. The data flow diagram of OLT is shown as Fig. 3.1 and that of ONU is shown as Fig. 3.2. Both of them include two parts, one is the data traffic in downstream and the other is data traffic in upstream.

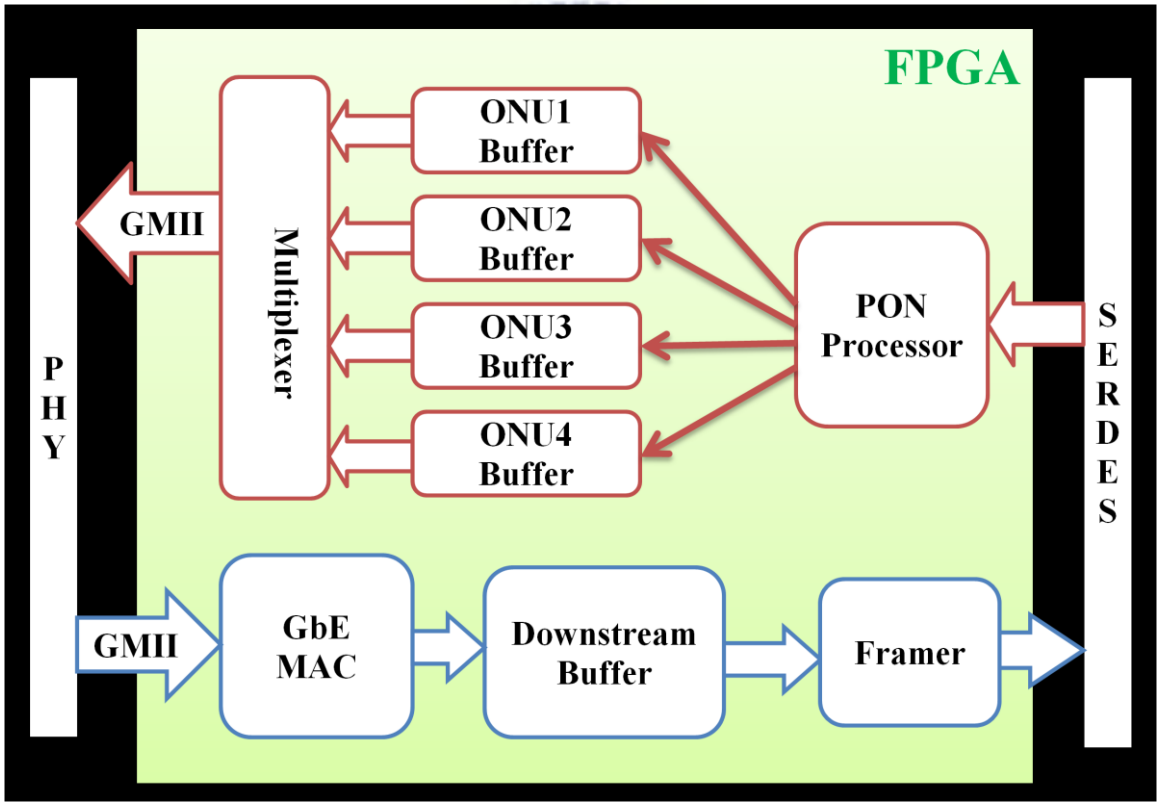

Figure 3.1 Data Flow Diagram of OLT

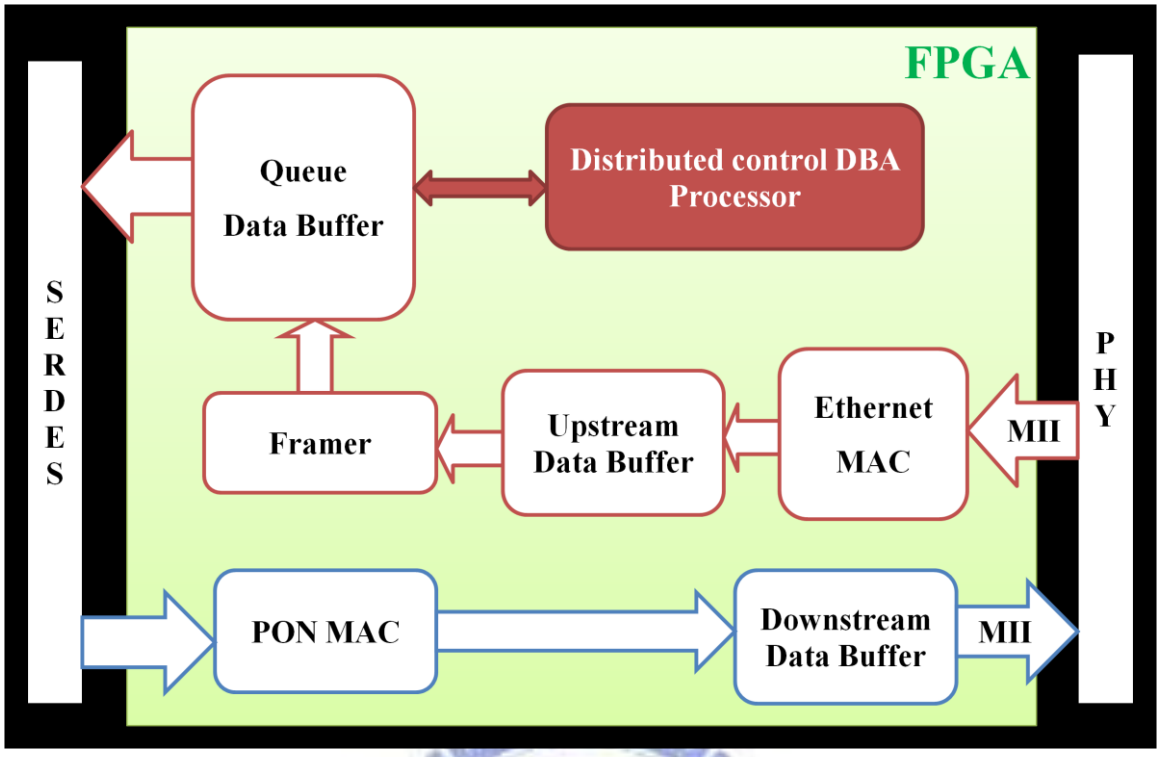

Figure 3.2 Data Flow Diagram of ONU

We will divide the system into two parts, downstream and upstream, in the following context.

3.1 The Data Format of DHPON

3.1.1 Data Format in Downstream

The data format in downstream has two parts: Header and Payload. As Fig. 3.3, Header is 6 bytes including 3-byte PSYNC, 1-byte Delimiter and 2-byte Payload-Length. The function of PSYNC is synchronization. When Delimiter shows up, we know that Payload is coming soon. Payload-Length represents the length of Payload. In fact, Payload is Ethernet packets. If there is no Ethernet packet transmitted, Idle will be delivered.

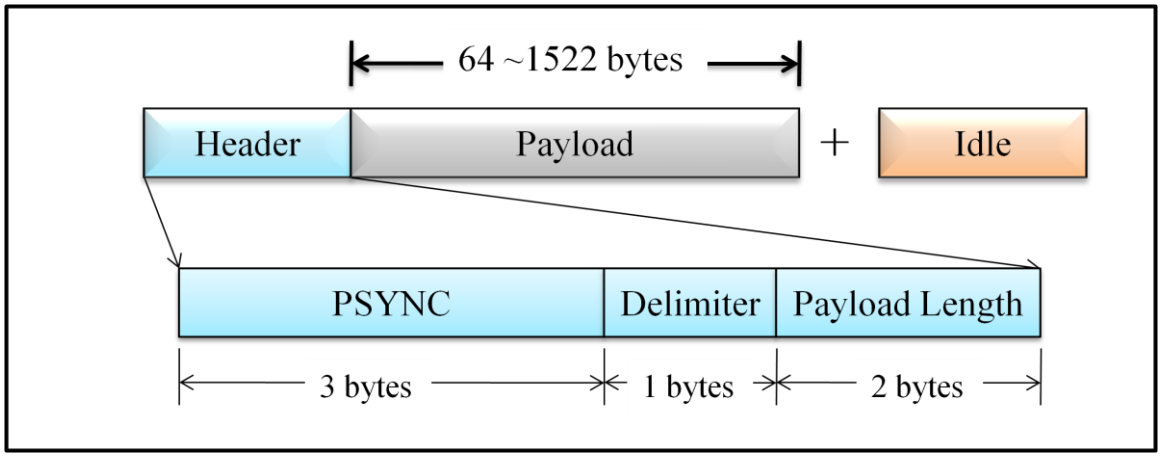

Figure 3.3 Data Format in Downstream

3.1.2 Data Format in Upstream

In upstream, each DHPON packet has fixed length with 280 bytes. The data format in the upstream includes Header, Payload and Idle. The data format in the upstream is shown as Fig. 3.4. Header is 12 bytes including 8-byte Preamble, 1-byte Delimiter, 1-byte ONU-ID, and 2-byte Payload-length. The function of Preamble is synchronization. We can know that which ONU the DHPON packet is from by ONU-ID. When Delimiter shows up, we know that Payload is coming soon. Payload-Length represents the length of Payload. The highest bit in the Payload-length is End of File Bit (EOFB). When EOF is high, it means this frame is the last frame of an Ethernet packet.

Payload has fixed length with 268 bytes and Ethernet packet is various lengths from 46 to 1518 bytes. Because we want to divide Ethernet packet into several Payloads, we can get 1 to 6 frames of Payloads. If the length of the latest frame of Payloads is less than 268 bytes, the Idle will be added to make the length be equal to 268 bytes.

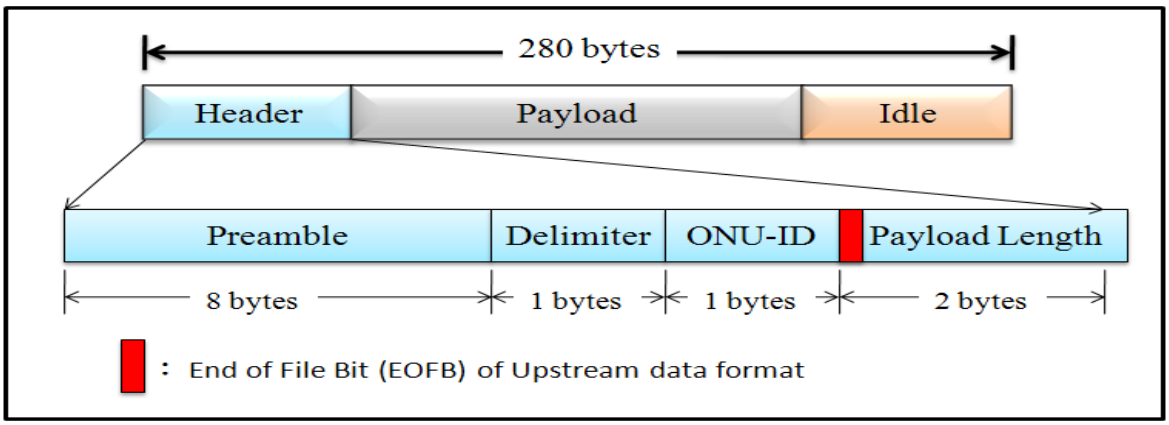

Figure 3.4 Data Format in Upstream

3.2 Downstream on DHPON

In downstream, OLT adds Header in front of Ethernet packets (input data), and sends the data packets to all ONUs. After transmitting by the fiber, ONU receive the data packets and remove Header and then send Ethernet packets (output data) to the users.

The data flow diagram in downstream is shown as Fig. 3.5. OLT in downstream has several modules including Gigabit Media Independent Interface (GMII), Downstream Data Buffer, and Framer. ONU in downstream has several modules including PON MAC, Downstream Data Buffer, and Media Independent Interface (MII).

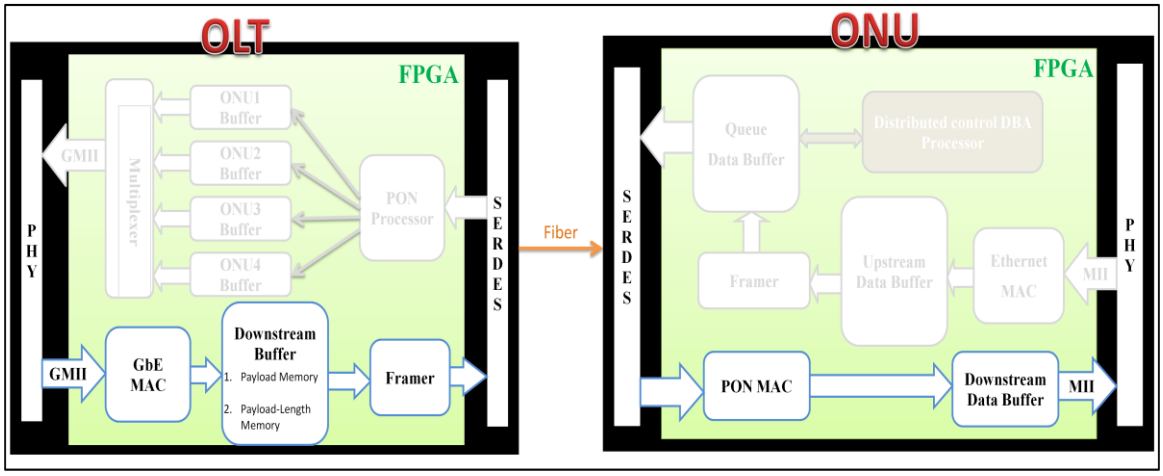

Figure 3.5 Data Flow Diagram of Downstream.

3.2.1 Gigabit Media Independent Interface (GMII) on OLT

Gigabit Media Independent Interface (GMII) is an interface between Physical Layer (PHY) and Media Access Control (MAC) device. The input data on the interface is framed using the IEEE Ethernet standard. The speed of the output interface is up to 1000 Mbps, and the implementation of the output interface is using 8-bit parallel data interface clocked at 125 MHz [11]. Then the date will be sent to GbE MAC module.

3.2.2 Downstream Data Buffer on OLT

In downstream, Data Buffer module is connected with GMII module, and its function is as a memory. Data Buffer module has two parts. One part, Payload Memory, stores Payload (Ethernet packets) and the other, Payload Length Memory, stores the length of Payload.

The input of Payload Memory is composited by 8-bit parallel data interface clocked at 125 MHz and the output of Payload Memory is composited by 16-bit parallel data interface clocked at 77.76 MHz. Payload Memory is a dual port block memory with two independent ports, portA and portB. It is shown as Fig. 3.6. We can set the portA to be write-only when Write Enable Pin of portA (WEA) is high. On the other hand, we can set the portB to be read-only when Write Enable Pin of portB (WEB) is low. For the reason, we can transfer data and change data rate more easily by portA and portB. Payload memory transfers the interface with 8-bit parallel data to the interface with 16-bit parallel data. The speed of the input interface is up to 1000 Mb/s, and the implementation of the output interface is using 16-bit parallel data interface clocked at 77.76 MHz. Then the speed of the output interface will achieve 1.25Gb/s.

When Ethernet packets are transmitted into GbE MAC module, GbE MAC module will count the length of the packet and store the result into Payload-Length Memory.

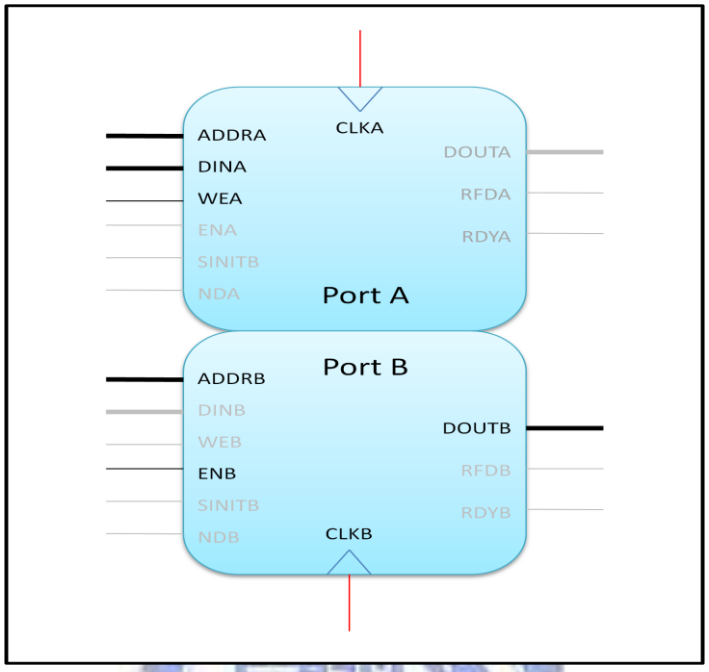

Figure 3.6 Dual Port Block Memory

3.2.3 Framer on OLT

Before the payload is transmitted, the framer module adds Header of downstream. There are Preamble (6 bytes), Delimiter (1 byte) and Payload-Length (2 bytes) on Header. We can see as Fig. 3.3. PSYNC is set to be 3 bytes “hAAAAAA”. Delimiter is set to be 1 byte “hE2”. Then we set Payload-Length to be from the Payload-Length Memory of Data Buffer module.

3.2.4 PON MAC on ONU

This module is Passive Optical Network Media Access Control (PON MAC). The main function of this module is to find out Payload (Ethernet packets) and removes

Header of downstream packet.

At the first, we should find out where the packet begins. Because we might receive something such as noise, shift of the data or Idle we don't want to have, we should shift the data to right place and find out Delimiter on Header. Then we can get Payload-Length and Payload (Ethernet packets). Then PON MAC will remove Header and send Payload and Payload-Length to Data Buffer module.

3.2.5 Downstream Data Buffer on ONU

Downstream Data Buffer module on ONU has two memories. One stores Payload (Ethernet packets), and the other stores Payload-Length. Both of them describe the same Payload. Payload-Length memory stores length of the payload.

The function of Downstream Data Buffer on ONU is almost the same as that on OLT. The single difference is as following. The input of Payload-Length memory of Downstream Data Buffer on ONU is 16-bit parallel data interface clocked at 77.76 MHz, and the output is 4-bit parallel data interface clocked at 25 MHz. The input data rate is 1.25 Gbps, and output data rate is 100 Mbps.

3.2.6 Media Independent Interface (MII) on ONU

Media Independent Interface (MII) is an interface between Physical Layer (PHY) and Ethernet Media Access Control (MAC) device. The input data interface of MII is used by 4-bit parallel data clocked at 25 MHz to achieve 100 Mbps speed [12].

3.3 Upstream on DHPON

In upstream, each ONU divides Ethernet packets (input data) into 268 bytes and adds Header in front each packet. The maximum length of an Ethernet packet is 1518 bytes, so we can get 1 to 6-parts payloads from an Ethernet packet. In the beginning of each payload, we add 12-bytes Header in upstream. The total length is 280bytes, and it is DHPON packet. Finally DHPON packets are stored into Queue Data Buffer. It will count how many DHPON packets in the Queue Data Buffer, then DBA Processor module will get this message. A DHPON packet will be sent at a slot (2us), after DBA Processor module give a control signal to Queue Data Buffer. Then the packet is sent to the OLT. The OLT will identify the packets from all ONUs and put in different ONU Buffer, and then the herder be removed. Then the OLT will send Ethernet packets (output data) to central office.

The upstream data flow diagram is shown as Fig. 3.7. There are several modules in the ONU, it include Media Independent Interface (MII), Ethernet Media Access Control (MAC), Upstream Data Buffer, Framer, DBA Data Buffer and DBA. There are several modules in the OLT, it include PON Processor, ONU Buffer and Multiplexer, and Gigabit Media Independent Interface (GMII).

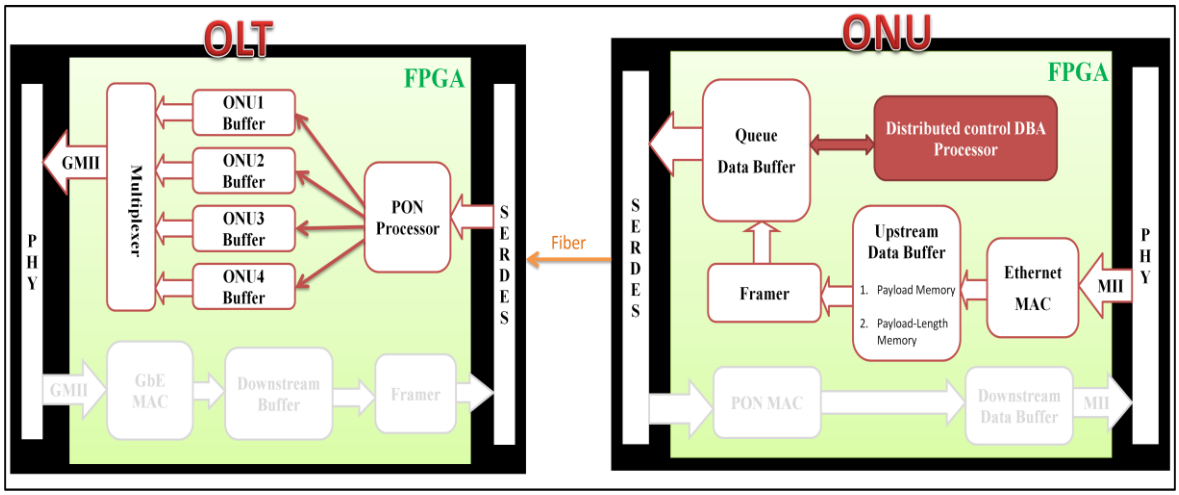

Figure 3.7 Data Flow Diagram of Upstream.

3.3.1 Media Independent Interface (MII) on ONU

The function of upstream MII is like downstream MII. The difference is that upstream MII is a receiver, and downstream MII is a transmitter. It transmit Ethernet packet to next module and output is 4 bits parallel data interface clocked at 25 MHz.

3.3.2 Ethernet MAC on ONU

When Ethernet packets are been sent to Ethernet MAC module, this module will count length of Ethernet packets. Then the Ethernet packets are sent directly to Data Buffer module. when the packets come to its end, we can get length of the Ethernet packet. Then Ethernet MAC module will send the length to Data Buffer module.

3.3.3 Upstream Data Buffer on ONU

In upstream, Data Buffer module is connected with the output of Ethernet MAC module, and it is regarded as a memory. Data Buffer module includes both Payload

Memory and Payload-Length Memory.

Payload Memory is a dual port block memory. We set the input port to be write-only with 4 bits, and the input data is triggered at 25 MHz. On the other hand, the output port is set to be read-only with 16 bits, and the output data is triggered at 77.76 MHz. It transfers the data interface from 4 bits to 16 bits. For Payload-Length Memory, we count the length of the Ethernet packets in Ethernet MAC module. After an Ethernet packet is sent out by Ethernet MAC module, the length of the Ethernet packet is stored in the Payload-Length Memory.

3.3.4 Framer on ONU

Framer module is the most important module and the key part in upstream. It divides Ethernet packet into several 268-bytes Payloads, and adds Header in front of each Payload. Before Framer sends Payload from Data Buffer, it sends Header first.

Header in upstream is 12 bytes including 8-bytes Preamble, 1-byte Delimiter, 1-byte ONU-ID, and 2-bytes Payload-Length. It is shown as Fig. 3.4. We set Preamble to be 8 bytes “h5555555555555555”, Delimiter to be 1 byte “hE2”. ONU-ID is decided by extra inputs from each ONU. Payload-Length is usually 2 byte “h010C”, and therefore Payload is 280 bytes. However, Payload-Length maybe isn’t “h010C” because of the remainders with less than 268 bytes. Payload-Length is the length of remainder packet. However, we can not know which packet is the last Payload for an Ethernet packet. For the reason, we set End of File Bit (EOFB) of Payload-Length of the last Payload of each Ethernet packet to be high. Therefore, Payload-Length of the last Payload for an Ethernet packet might be with 16 bits “h8XXX”.

After sending out Header, Framer reads Payload from the Data Buffer and sends them to Queue Data Buffer. The composite with 280 bytes of Header and Payload is DHPON packet. A DHPON packet is sent out in a slot (2 us).

3.3.5 Queue Data Buffer on ONU

Queue Data Buffer stores DHPON packets, and its main job is to connect with DBA Processor module.

An Ethernet packet is divided into several DHPON packets with 280 bytes by Framer module. They are stored in Queue Data Buffer. Queue Data Buffer module counts how many DHPON packets are stored in the memory and tells DBA Processor module. Then DBA Processor module will give a control signal to Queue Data Buffer.

Finally, we control the output in upstream. When Queue Data Buffer module gets a control signal from DBA Processor module, it makes the enable pin of the read-only part (partB) of Queue Data Buffer high. After 140 clocks goes, 280 bytes data (a DHPON packet) should be been sent out. Then the enable pin becomes low. Therefore, a DHPON packet can be sent by Queue Data Buffer in a slot. In other words, DBA Processor module can decide whether the DHPON packet in upstream is sent out or not.

3.3.6 PON Processor on OLT

PON Processor is the first module on OLT in upstream. Its inputs include data and clk. When the data is transmitted into PON Processor module, the DHPON packet may lose some Preamble on Header or be shifted. Hence, we must do something for calibration. We add two registers with 16 bits for shifting the data to the right place. Then we get the right

DHPON packet and find Delimiter on Header. After calibration, PON Processor will find out ONU-ID, Payload-length and Payload. Then PON Processor module sends them to ONU Buffer.

3.3.7 ONU Buffer and Multiplexer

Because there are four inputs from different ONUs, ONU Buffer includes 4 data memories. The inputs connect with the outputs of PON Processor module. We will store Payload to ONU memories depending on the ONU-ID.

An Ethernet packet may be divided into 1 to 6 parts. We must get EOFB of Payload-length on Heater to know that the payload is the last payload of each Ethernet packet. If EOFB of Payload-length is high, it means we get the last payload of an Ethernet packet. Then Multiplexer module will combine these payloads to be an Ethernet packet and send out the Ethernet packet to GMII.

3.3.8 Gigabit Media Independent Interface (GMII) on OLT

GMII is the last module in upstream, and its function is almost the same as that of GMII in downstream. The difference is that GMII in upstream transfer data from 16 bits to 8 bits. The input data is 16 bits parallel data, triggered by 77.76 MHz. The output data on the interface is framed by the IEEE Ethernet standard. The interface is set to be 1000 Mb/s speed, implemented using 8 bits parallel data interface clocked at 125 MHz.

CHAPTER 4

Devices on Board of DHPON

In this chapter, we will explain the components on the ONU board and OLT board of DHPON. ONU board is shown as Fig. 4.1. Because OLT board is not implemented yet, we modify ONU board a bit to regard it as OLT board. OLT board is shown as Fig. 4.x. Therefore, OLT and ONU board only connect with each other by continuous mode in the data traffic. We use Field Programmable Gate Array (FPGA) to implement OLT and ONU.

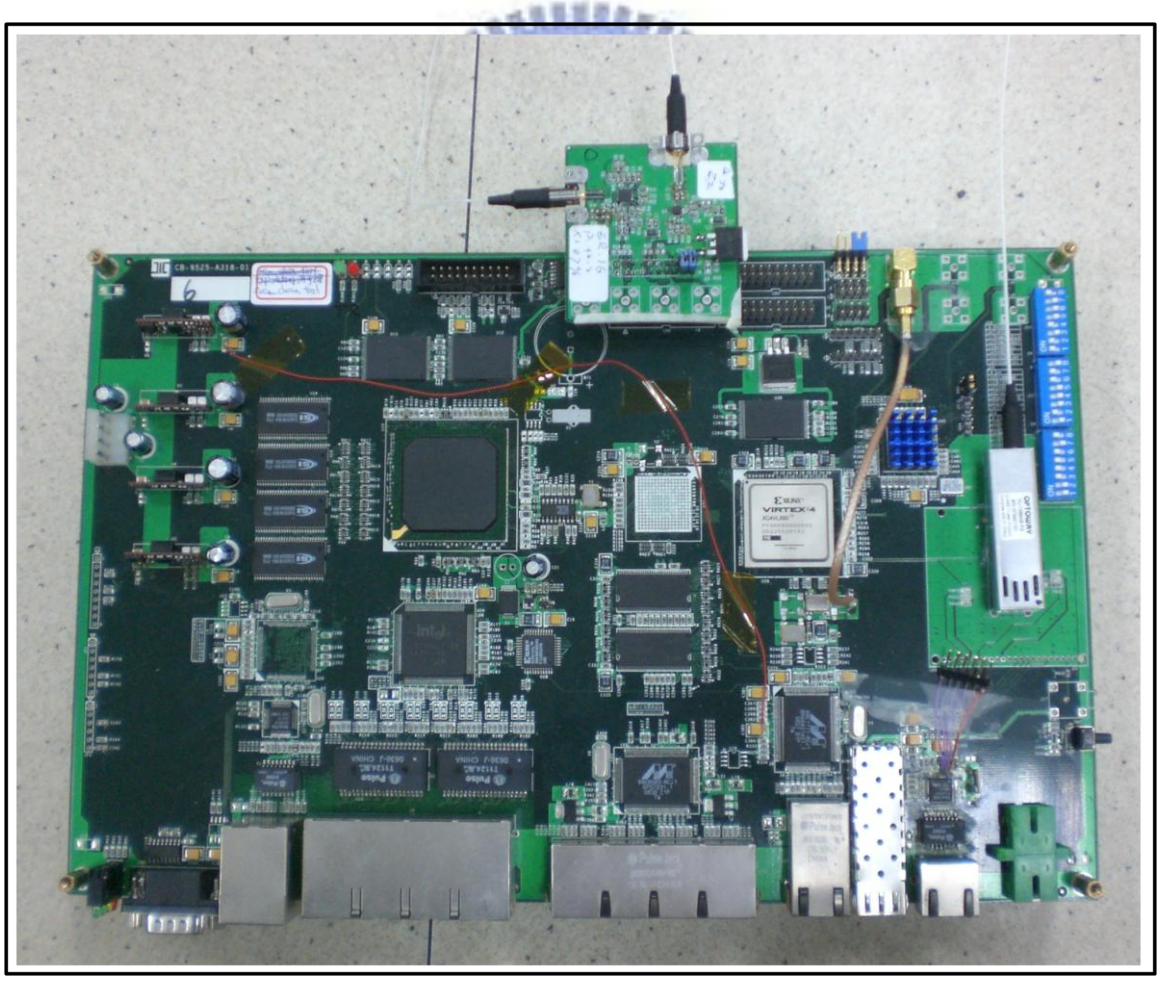

Figure 4.1 ONU Board

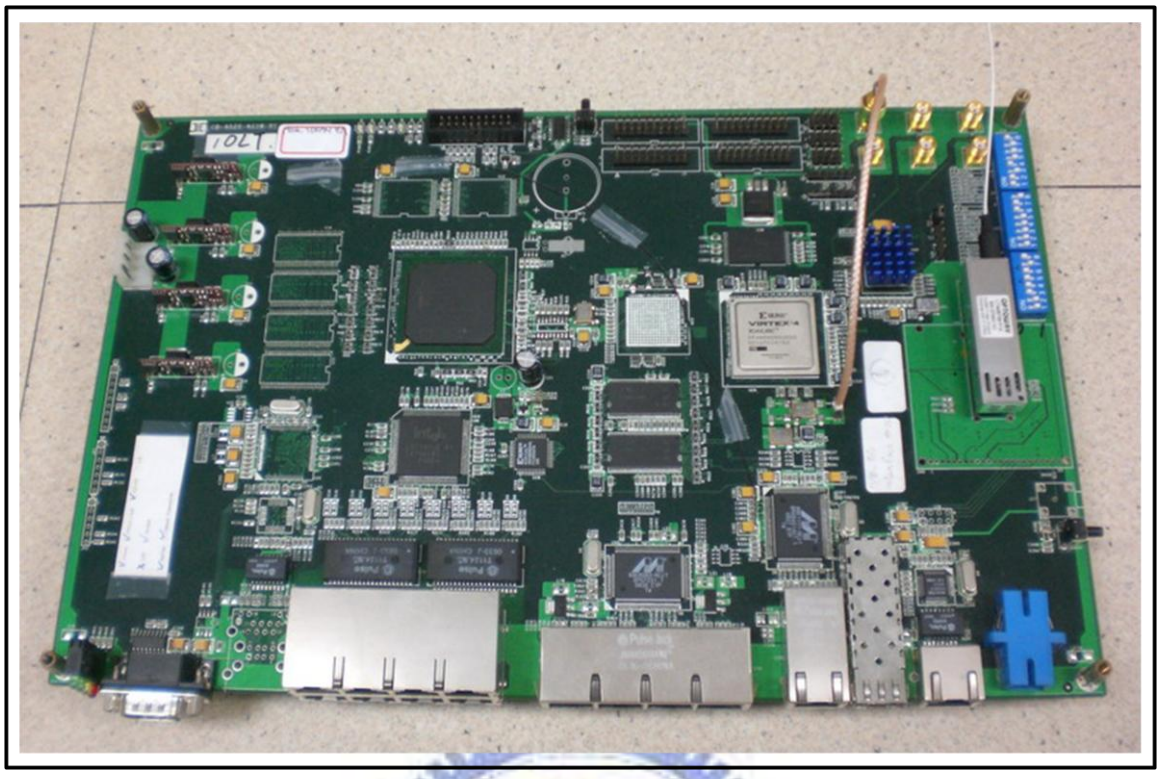

Figure 4.2 OLT Board

4.1 Field Programmable Gate Array (FPGA)

Field Programmable Gate Arrays (FPGAs) are programmable semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGA block structure is shown as Fig. 4.3. As opposed to Application Specific Integrated Circuits (ASICs) where the device is custom built for the particular design, FPGAs can be programmed to the desired application or functionality requirements.

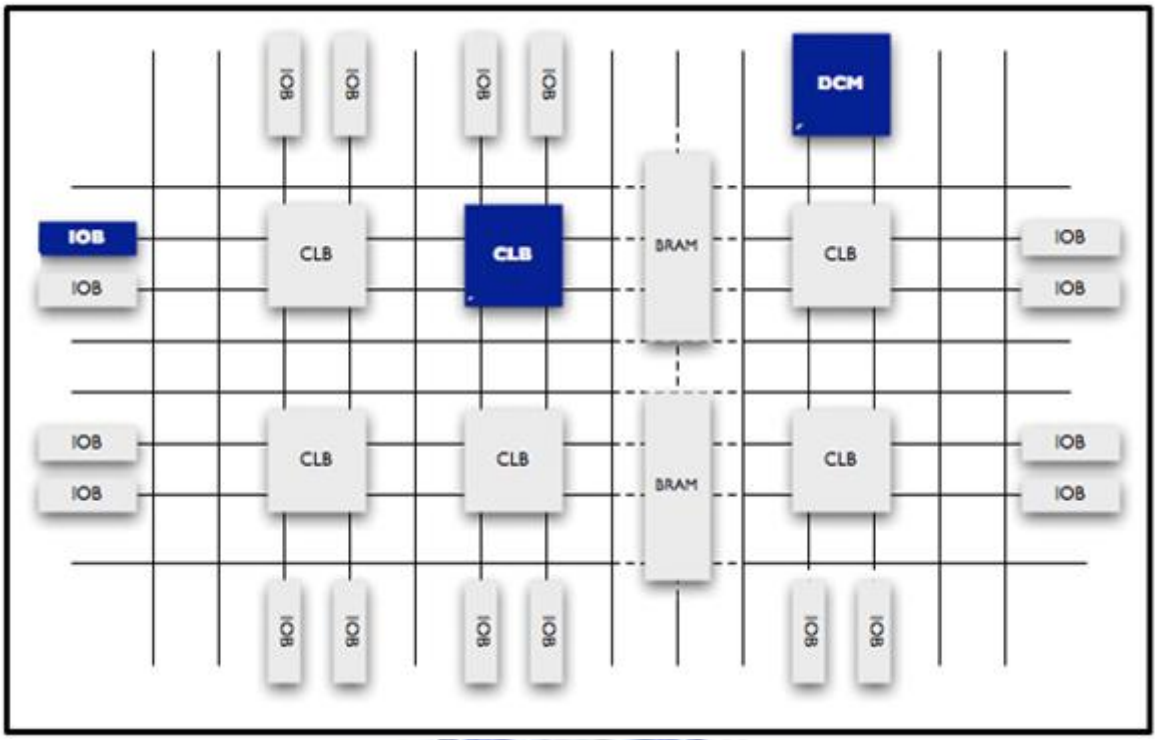

Figure 4.3 Block Structure of FPGA

4.1.1 FPGA Features

FPGA now has evolved far beyond the basic capabilities present in their predecessors, and incorporate hard (ASIC type) blocks of commonly used functionality such as RAM, clock management, and DSP. Following are the basic components in an FPGA [13].

1. Configurable Logic Block (CLBs)

The CLB is the basic logic unit in an FPGA. Exact numbers and features vary from device to device, but every CLB consists of a configurable switch matrix with 4 or 6 inputs, some selection circuitry (MUX, etc), and flip-flops. The switch matrix is highly flexible and can be configured to handle combinatorial logic, shift registers, or RAM.

2. Interconnect

While the CLB provides the logic capability, flexible interconnect routing routes the signals between CLBs and to and from I/Os. Routing comes in several flavors, from that designed to interconnect between CLBs to fast horizontal and vertical long lines spanning the device to global low-skew routing for Clocking and other global signals. The design software makes the interconnect routing task hidden to the user unless specified otherwise, thus significantly reducing design complexity.

3. Select IO (IOBs)

Today's FPGAs provide support for dozens of I/O standards thus providing the ideal interface bridge in your system. I/O in FPGAs is grouped in banks with each bank independently able to support different I/O standards. Today's leading FPGAs provide over a dozen I/O banks, thus allowing flexibility in I/O support.

4. Memory

Embedded Block RAM memory is available in most FPGAs, which allows for on-chip memory in your design. These allow for on-chip memory for your design. Xilinx FPGAs provide up to 10 Mbits of on-chip memory in 36 kbit blocks that can support true dual-port operation.

5. Complete Clock Management

Digital clock management is provided by most FPGAs in the industry (all Xilinx FPGAs have this feature). The most advanced FPGAs from Xilinx offer both digital clock management and phase-looped locking that provide precision clock synthesis combined with jitter reduction and filtering.

4.1.2 Design Flow of FPGA

The FPGA designs flow eliminates the complex and time-consuming floor-planning, place and route, timing analysis, and mask / re-spin stages of the project since the design logic is already synthesized to be placed onto an already verified, characterized FPGA device [14]. The design flow of FPGA is shown as Fig. 4.4.

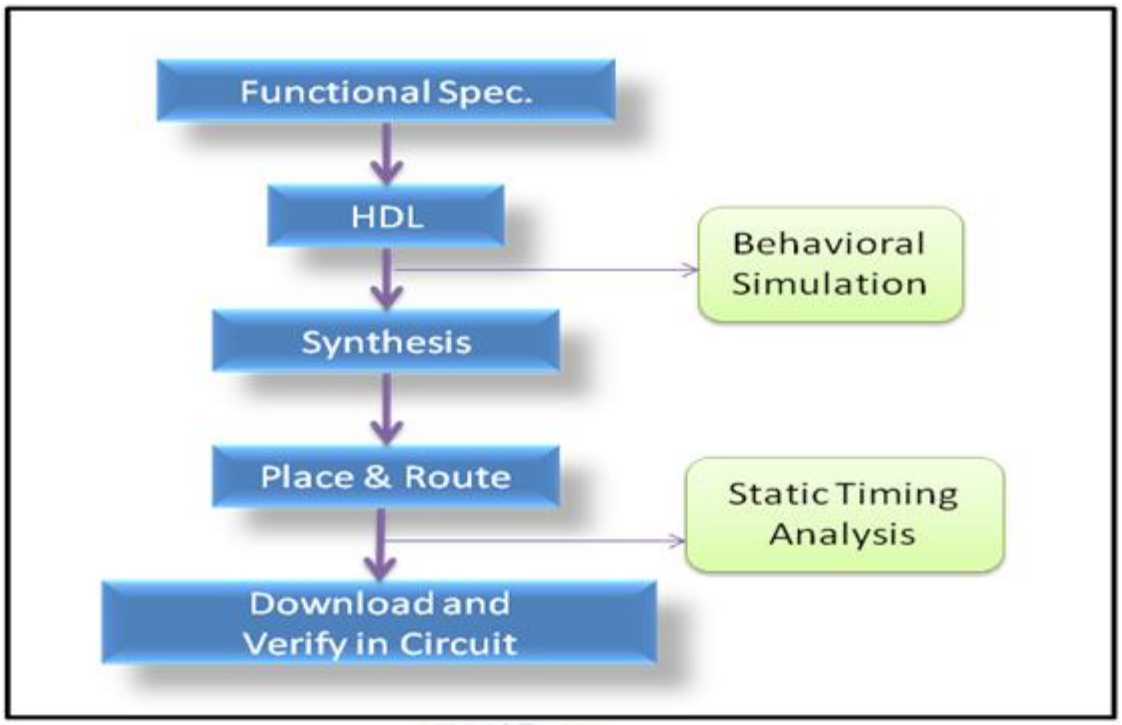

Figure 4.4 FPGA Design Flow

1. Hardware Description Language (HDL)

Hardware description language (HDL) is any language from a class of computer languages for formal description of electronic circuits. It can describe the circuit's operation, its design and organization, and tests to verify its operation by means of simulation. In this experiment, we use Verilog HDL.

2. Synthesis

Synthesis is the process of constructing a gate level netlist from a register transfer level

model of a circuit described in Verilog HDL [15]. In this experiment, we use Synplify Pro software.

3. Place & Route

Place & Route tool will then export a device configuration that can to target the FPGA in actual hardware.

4.1.3 FPGA on ONU

We use Xilinx Virtex-4 LX60 FPGA. Its data sheet is shown as Table 4.1. Its main job is to communicate with near chips on board, and it is the most important component on ONU board and OLT board.

Xilinx Virtex-4 XC4VL60 FPGA		
CLB Resources	CLB Array (Row x Column)	128 x 36
	Slices	26,624
	Logic Cells	59,904
	CLB Flip Flops	53,248
Memory Resources	Max. Distributed RAM Bits	425,984
	Block RAM/FIFO w/ECC (18 kbits each)	160
	Total Block RAM (kbits)	2,880
Clock Resources	Digital Clock Managers (DCM)	8
	Phase-matched Clock Dividers (PMCD)	4
I/O Resources	Max Select I/O	640
	Total I/O Banks	13
	Digitally Controlled Impedance	Yes
	Max Differential I/O Pairs	320

Table 4.1 Virtex-4 LX60 Data Sheet

4.2 Physical Layer

The Ethernet physical layer is the physical layer component of the Ethernet standard. It evolved over a considerable time span and encompasses quite a few physical media interfaces and several magnitudes of speed. The speed ranges from 3 Mb/s to 10 Gb/s in speed while the physical medium can range from bulky coaxial cable to twisted pair to optical fiber. In general, network protocol stack software will work identically on most of the following types.

The following sections provide a brief summary of all the official Ethernet media types (section numbers from the IEEE 802.3-2002 standard are parenthesized). In addition to these official standards, many vendors have implemented proprietary media types for various reasons—often to support longer distances over fiber optic cabling.

4.2.1 OLT Physical Layer

The OLT board use Gigabit Ethernet port. A 10/100/1000 Ethernet port supports 10BASE-T, 100BASE-TX, and 1000BASE-T. Ethernet adapters and switch ports support multiple speeds, using auto negotiation to set the speed and duplex for the best values supported by both connected devices.

4.2.1 ONU Physical Layer

The ONU use the 100 Megabits Ethernet port. A 10/100 Ethernet port supports 10BASE-T and 100BASE-TX.

4.3 Serializer/Deserializer (SerDes)

In DHPON, the SerDes chip is AMCC S3157. SerDes has two main functions. One is a Parallel to Serial converter, and it is called as the parallel to serial out (PTSO) block. The other is Serial to Parallel converter, and it is called as the serial to parallel out (STPO) block.

The PTSO block canonically has a parallel clock in and a collection of data lines coming into it. It may have some sort of Phase-Locked Loop (PLL) in it to multiply the incoming parallel clock up to the serial frequency. The STPO block canonically has serial clock and data inputs. The serial clock may have been recovered from the data stream using a clock recovery technique. This process is commonly known as clock and data recovery (CDR). The STPO block then divides the incoming clock down to the parallel rate.

The MACC S3157 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

1、 Transmitter Operations:

- 16-bit parallel input
- Parallel-to-serial conversion
- Serial output

2、 Receiver Operations:

- Clock and data recovery from serial input
- Serial-to-parallel conversion
- 16-bit parallel output

SerDes is sometimes combined with implementations of encoding/decoding blocks in

single blocks. The purpose of encoding/decoding is typically to place at least statistical bounds on the rate of signal transitions to allow for easier clock recovery in the receiver, to provide framing, and to provide DC balance. We use Scrambling-Code on PTSO and Scrambling-Decode on STOP with ONU and OLT.

4.4 Optical Transceiver of ONU

We use Optoway NU-73B94B-PG transceiver on ONU board of DHPON. NU-73B94B-PG is a transceiver for the ONU of G-PON with 2.488 Gbps in downstream and 1.244 Gbps in upstream. It is high performance module for single fiber communications by using 1310 nm burst-mode transmitter and 1490 nm continuous-mode receiver. The transmitter section uses a multiple quantum well 1310 nm laser and is a class 1 laser compliant according to International Safety Standard IEC 60825. The receiver section uses an integrated 1490 nm detector preamplifier (IDP) mounted in an optical header and a limiting post-amplifier IC. LVPECL interface is used for differential inputs and outputs. A LVTTL logic interface simplifies interface to external circuitry.

4.5 Optical Transceiver of OLT

We use Optoway LT-94B73B-PG transceiver on ONU board of DHPON. It is ITU-T G.984.2 Class B+ OLT for 2.488 Gbps/1490 nm in downstream and 1.244 Gbps/1310 nm in upstream. The transmitter section uses a multiple quantum well 1490 nm DFB laser and is a class 1 laser compliant according to International Safety Standard IEC-60825. The receiver section uses an integrated 1310 nm burst-mode detector preamplifier (IDP) mounted in an optical header and a burst-mode limiting post-amplifier IC. Unlike the conventional BM RX, the RX does not require reset pulse to receive optical data packets

with different optical power. LVPECL interface is used for differential inputs and outputs. A LVTTL logic interface simplifies interface to external circuitry.

4.6 Summary

We have introduced the functions and characters of each component above. We combine all components on ONU board and OLT board. The locations of all components on ONU board are shown as Fig. 4.5, and those on OLT board are shown as Fig. 4.6.

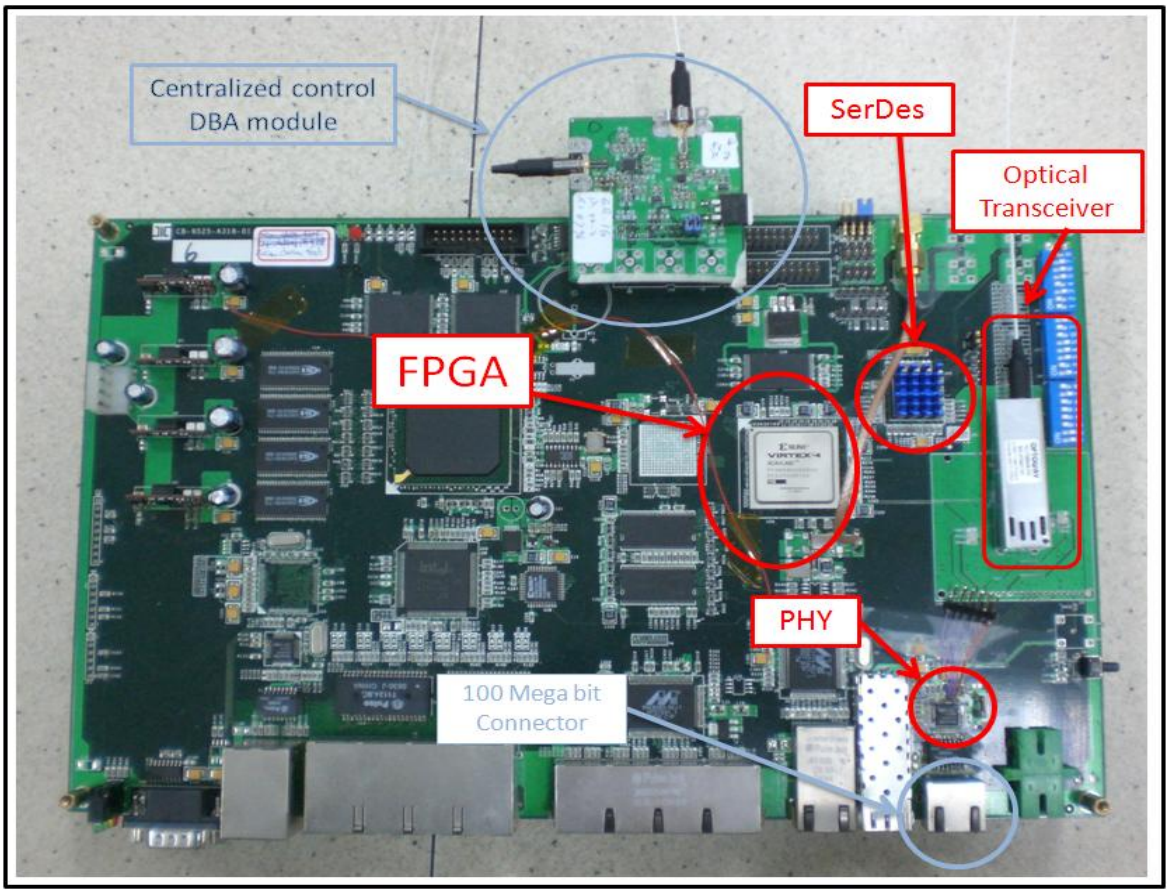

Fig. 4.5 Locations of All Components on ONU Board

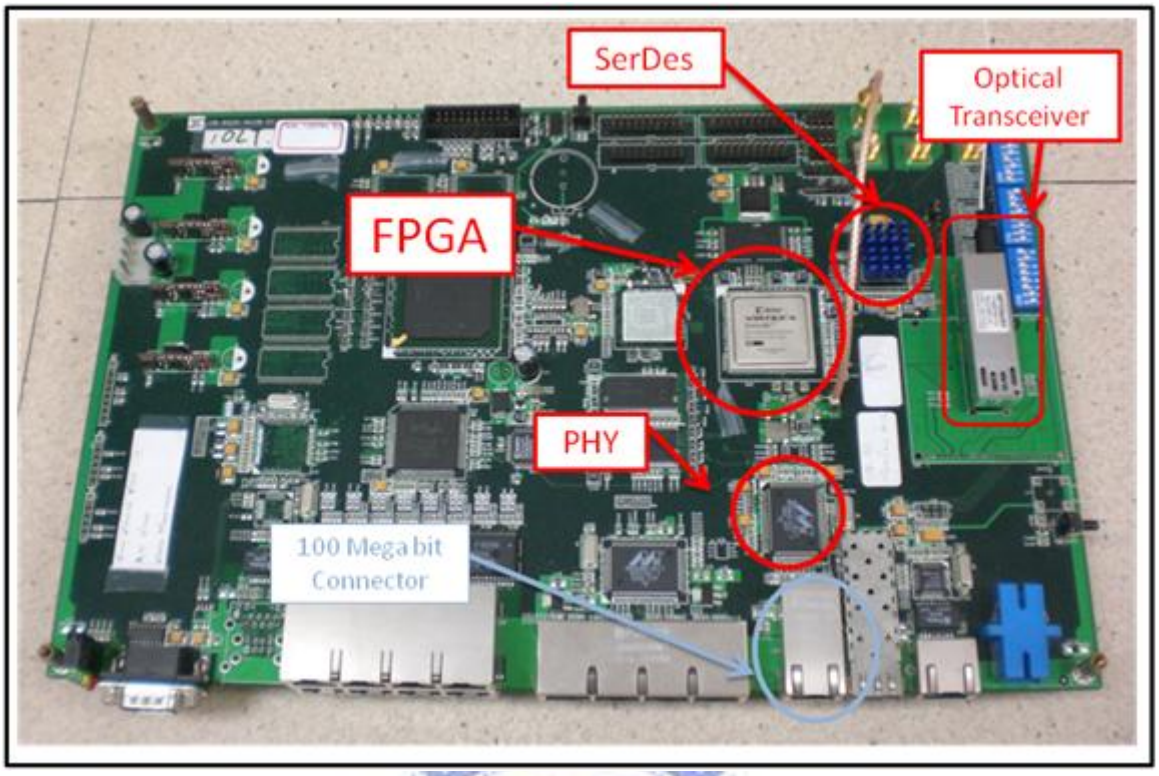

Fig. 4.6 Locations of All Components on OLT Board

We illustrate the whole system of DHPON with simple a block diagram. The block diagram of DHPON system is shown as Fig. 4.7.

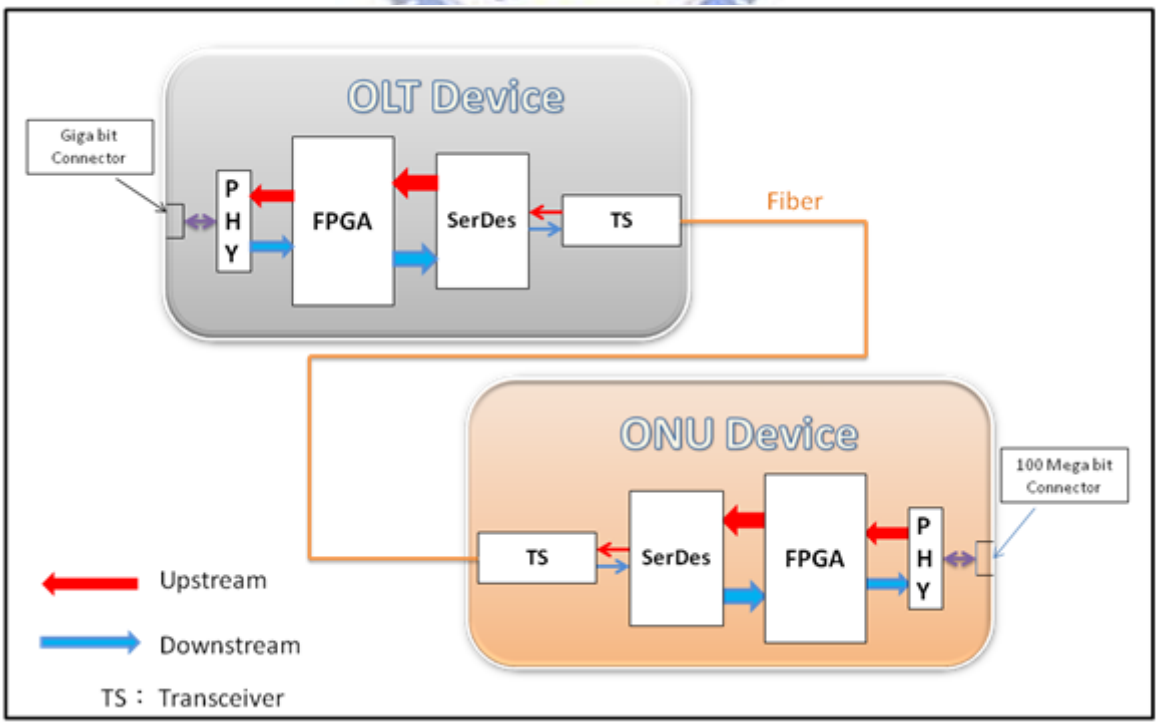

Figure 4.7 Block Diagram of DHPON System

In upstream, at the first, an Ethernet packet is transmitted from users to ONU Physical Layer. Then, an Ethernet packet is transmitted from ONU Physical Layer to FPGA with 4-bit parallel data at 25 MHz. Then a DHPON packet is transmitted from FPGA to Serdes with 16-bit parallel data at 77.76 MHz. Serdes transfers 16-bit parallel data to serial signal and then transmits serial signal to ONU Transceiver. ONU Transceiver sends the data to OLT Transceiver by the fiber. When OLT Transceiver receives the serial signal data, Serdes will transform the data into 16-bit parallel data at 77.76 MHz and then transmit the data with 16-bit parallel to FPGA. Last, FPGA transmits an Ethernet packet with 8-bit parallel data at 125 MHz to OLT Physical Layer. Then, the CO will get the Ethernet packet.

In downstream, at the first, an Ethernet packet is transmitted into OLT Physical Layer. Then, an Ethernet packet is transmitted from OLT Physical Layer to FPGA with 8-bit parallel data at 125 MHz. The Ethernet packet is transmitted to Serdes by FPGA with 16-bit parallel data at 77.76 MHz. Serdes transfers 16-bit parallel data to serial signal and then transmits serial signal to OLT Transceiver. OLT Transceiver sends the data to ONU Transceiver by the fiber. When ONU Transceiver receives the serial signal, Serdes on ONU will transform the data into 16-bit parallel data at 77.76 MHz and then transmit the data with 16-bit parallel to FPGA. Last, FPGA transforms the data to an Ethernet packet and then transmits the Ethernet packet with 8-bit parallel data at 125 MHz to ONU Physical Layer. Then, the user will get the Ethernet packet.

CHAPTER 5

Testing and Results on Hardware

In this chapter, we will focus on testing of data traffic. We set up a DHPON system with one OLT to one ONU. It's shown as Fig. 5.1. Then, we will analyze the data on ONU board and OLT board.

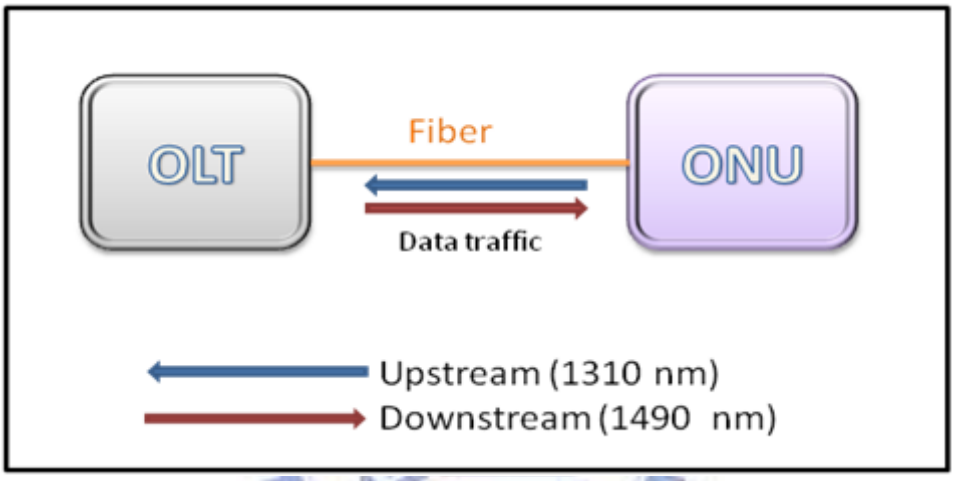

Figure 5.1 Testing Architecture of DHPON

5.1 Testing Results of Data Traffic

We complete the system of DHPON, and transfer data between CO and Users. We will use EthView to generate Ethernet packets. EthView is software for analyzing and generating Ethernet packets. Then, Ethernet packets are send into DHPON network. We assign the module I/O pin to the test pins of the board, and the module I/O pin is on the inside of FPGA. We can use Logic-Analyzer (LA) to store and display the data which is on the inside of FPGA. Logic-Analyzer is an electronic instrument that displays signals in a digital circuit that are too fast to be observed and presents it to a user so that the user can more easily check correct operation of the digital system. Then, we can get the data more

easily by connecting the probes of Logic-Analyzer with the test pins of the board. That is shown in Fig. 5.2.

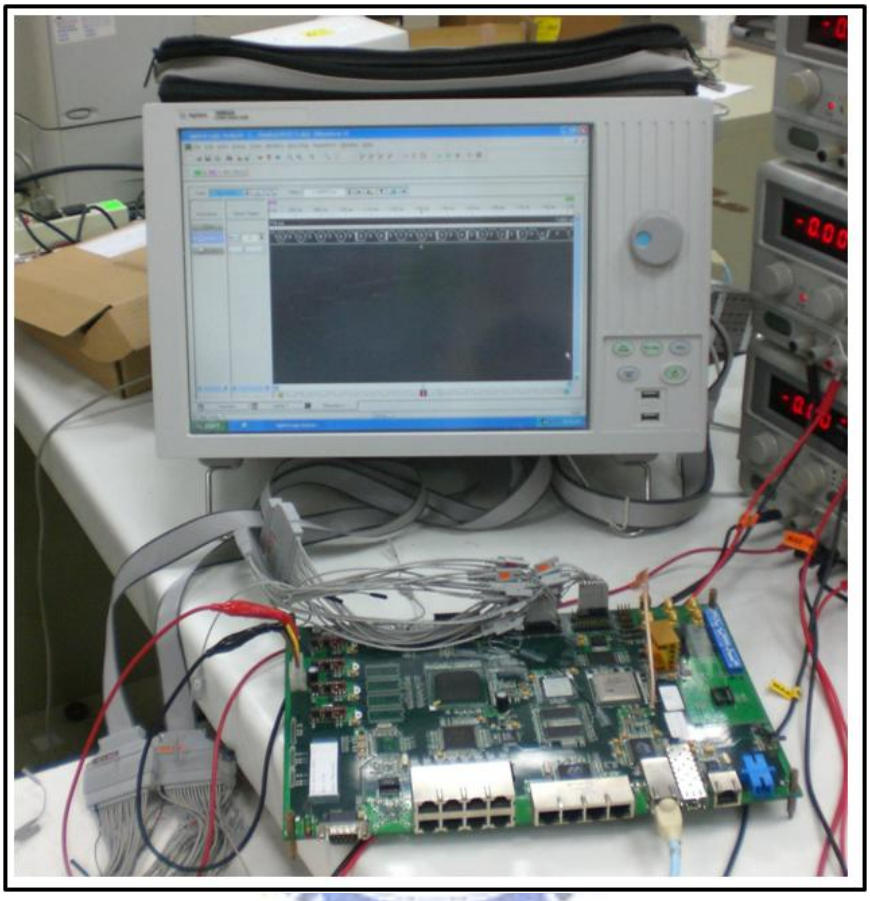

Figure 5.2 Connect Logic-Analyzer with the Board

I divide the system of DHPON into two parts, upstream and downstream parts, to analyze and explain the results.

5.1.1 Testing Results in Upstream

First, we use EthView to generate Ethernet packets, EthView is a software with Internet network. Then it sends the Ethernet packets to ONU by connecting ONU board with a computer through a Network-Line.

When the Ethernet packets pass PHY, they will be inputted to FPGA. The data is shown as Fig. 5.3. From the figure, we know that the data interface is 4-bits parallel data interface clocked at 25 MHz.

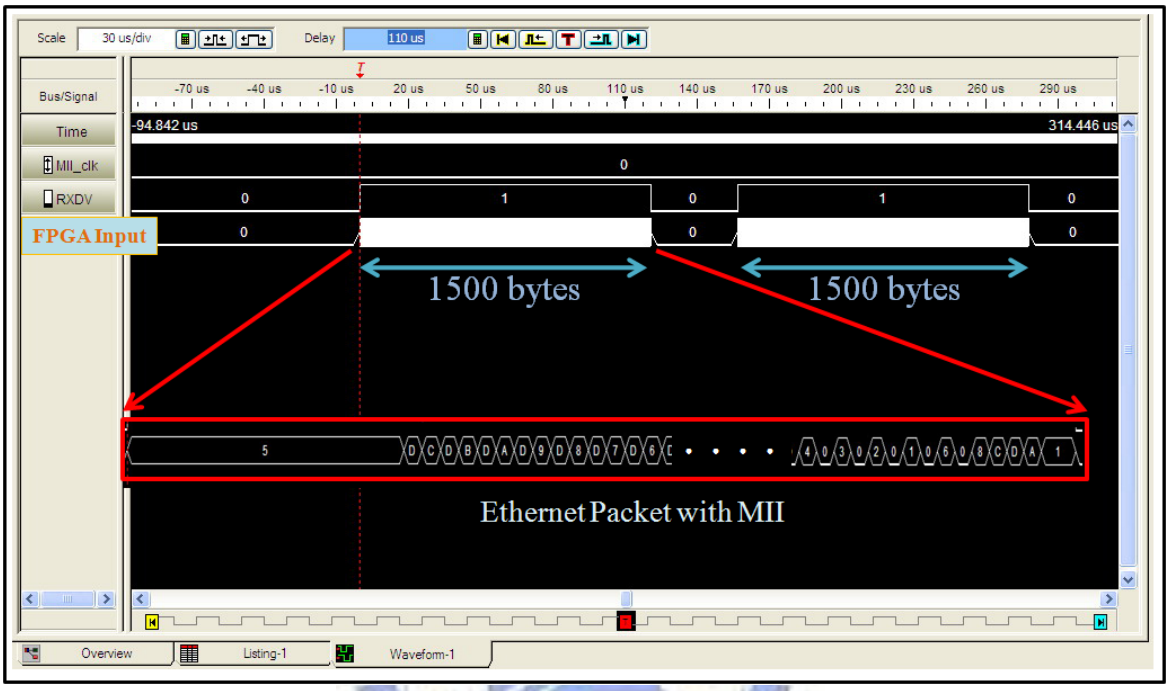

Figure 5.3 Inputs of FPGA on ONU Board

The output data of FPGA on ONU is shown as Fig. 5.4. From this figure, we know that these modules of ONU has divided the Ethernet packet into 268-bytes Payload, and added Header in front of Payload successfully. Through the process, the Ethernet packet becomes several 280-bytes DHPON packets. Fig. 5.5 shows that Header is added in front of Payload. From Fig. 5.5, we also know that the DHPON meets the data format of upstream and EOFB of the latest DHPON packet of an Ethernet packet is high. After PON packets pass SerDes and ONU Transceiver, we can send them to OLT by fiber with optical signals which is shown as Fig. 5.6.

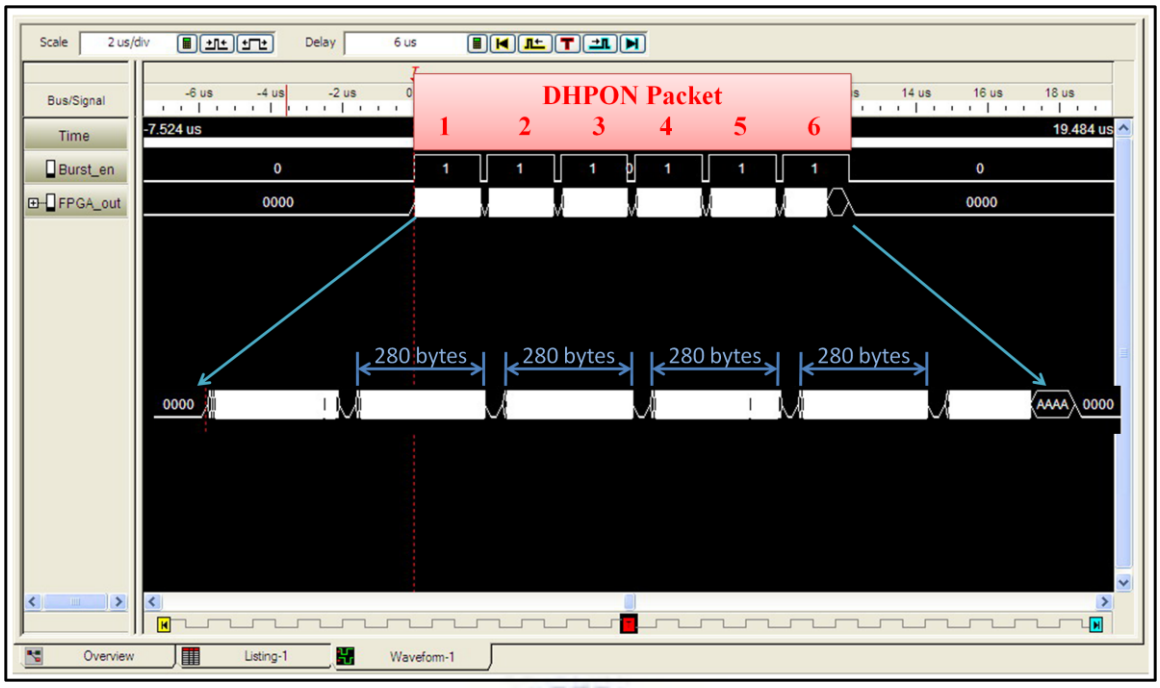

Figure 5.4 DHPON Packets

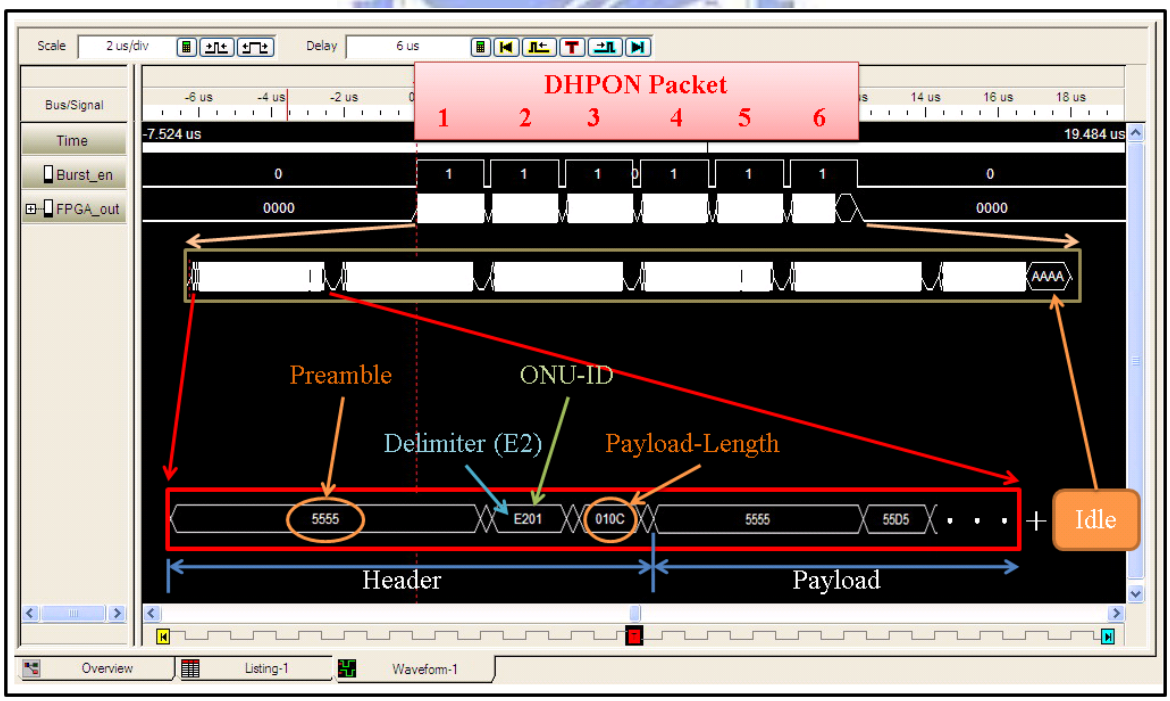

Figure 5.5 Header of DHPON Packet

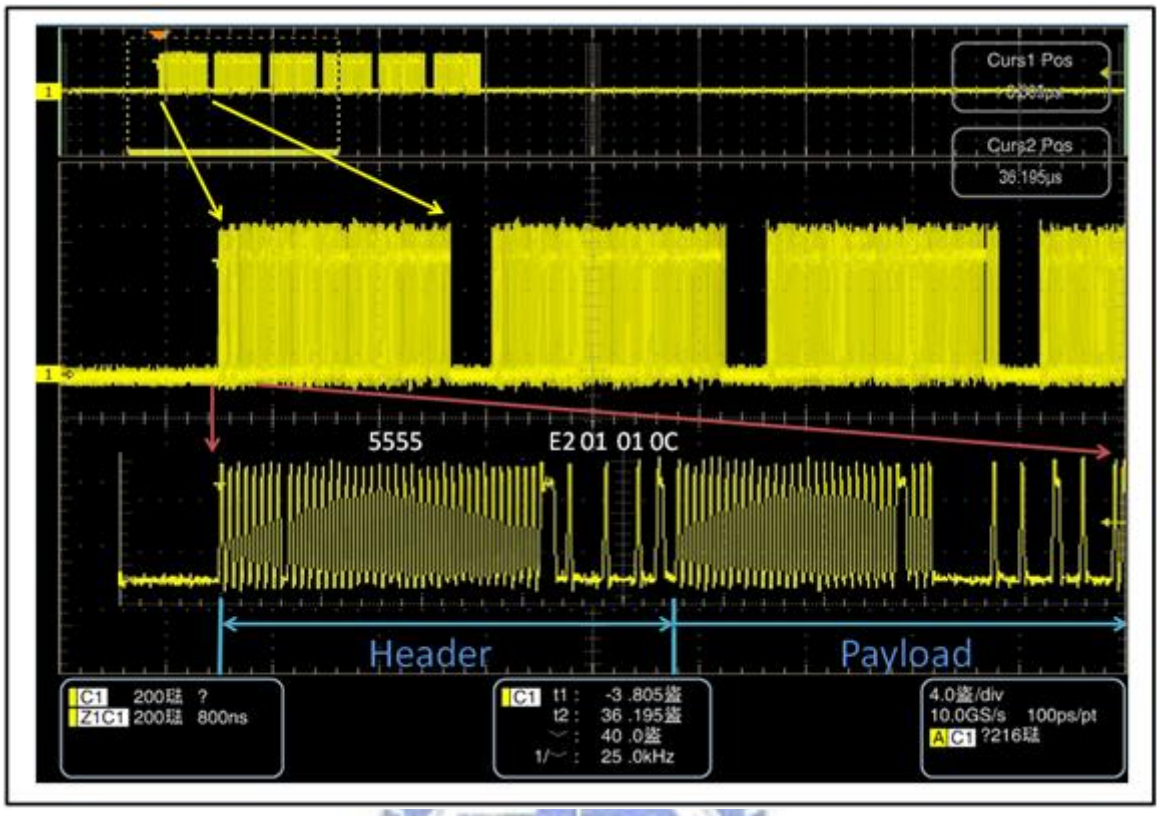

Figure 5.6 DHPON Packets with Optical Signal on Fiber

After OLT receives the data by the OLT Transceiver, the data is sent from SerDes to FPGA. on OLT. the it is shown as Fig. 5.7. Then PON Processor module will shift the data back to the right place and find ONU-ID and Payload-Length as Fig. 5.8 shows. Other modules on OLT remove Header of DHPON packets and combine Payloads to form an Ethernet packet successfully. It is shown as Fig. 5.9. The Ethernet packet will be sent to PHY on OLT by FPGA. From Fig. 5.9, we know that the data interface meets the requirement of GMII. Fig. 5.10 shows the locations of gathering data (Fig. 5.3 ~ 5.9).

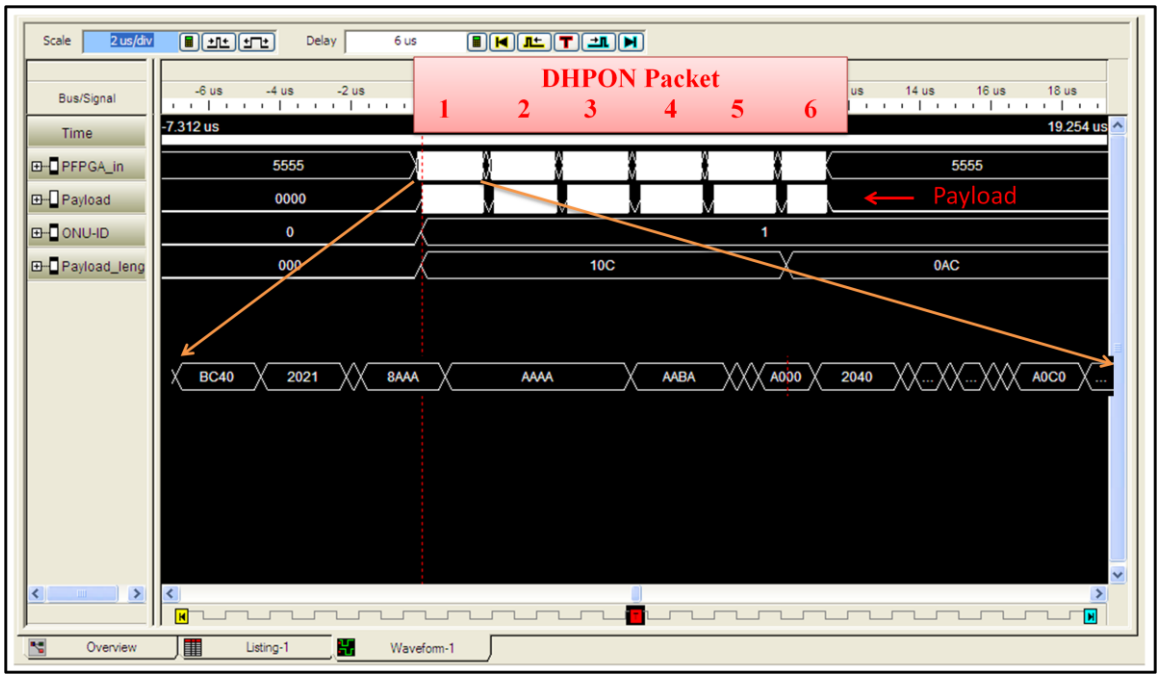

Figure 5.7 Input Data on OLT in Upstream

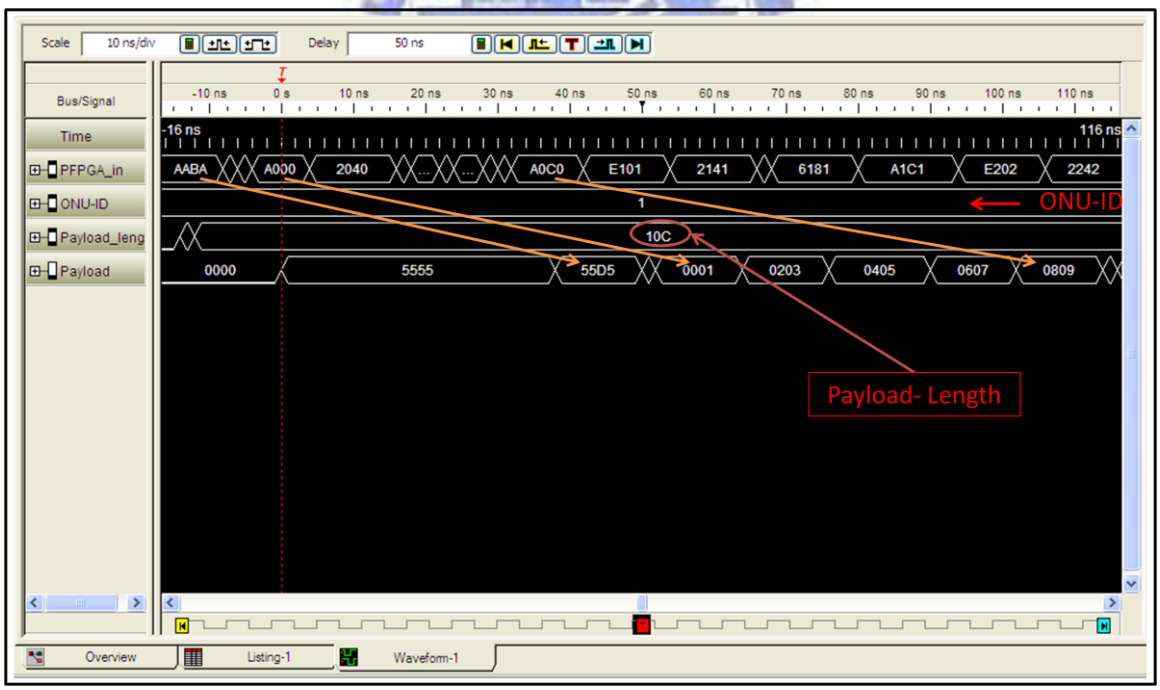

Figure 5.8 ONU-ID and Payload on OLT in Upstream

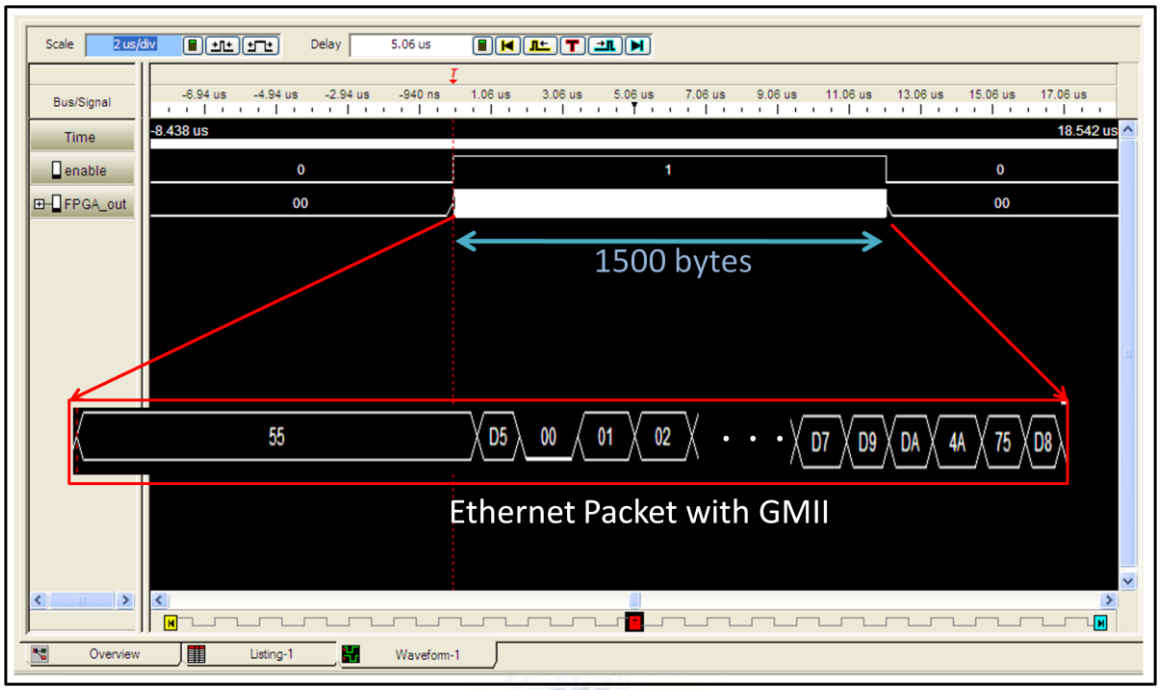

Figure 5.9 Output Packet on OLT in Upstream

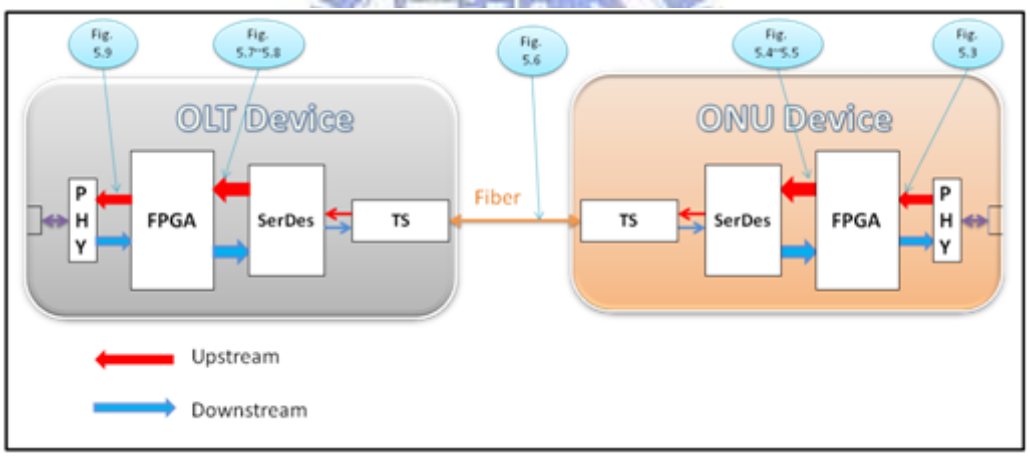

Figure 5.10 Locations of Gathering Data in Upstream

5.1.2 Data Results in Downstream

The testing method of downstream is almost the same as the method of upstream. The only difference is that the Ethernet packets are sent to OLT by connecting OLT board with a computer through a Network-Line by EthView. As Fig. 5.11 shows, the input data of FPGA on OLT is an Ethernet packet. These modules of OLT will add Header in front of

Ethernet packets, and create a packet which meets the requirement of data format of Downstream. Then, FPGA send the packet to SerDes on OLT. The packet of downstream is shown as Fig. 5.12, and we know that the packet matches with the data format of downstream. OLT sent the packet of downstream to NOU by fiber with optical signal, and we show the signal as Fig. 5.13.

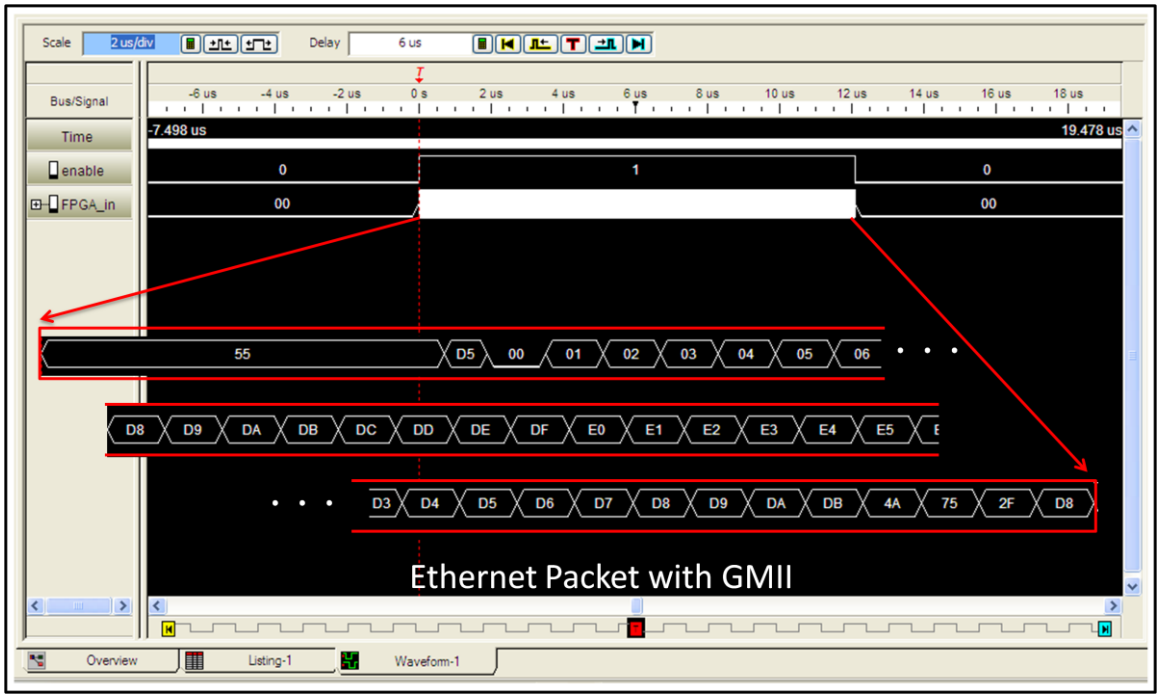

Figure 5.11 Inputs of FPGA on OLT

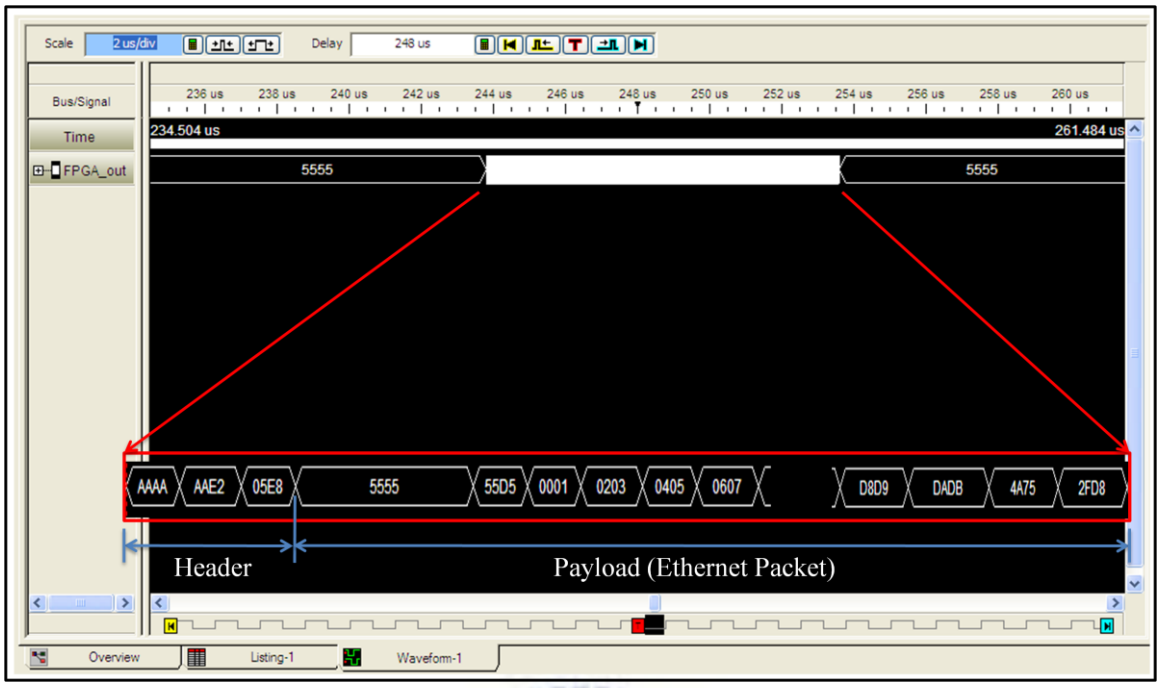

Figure 5.12 Packets of Downstream

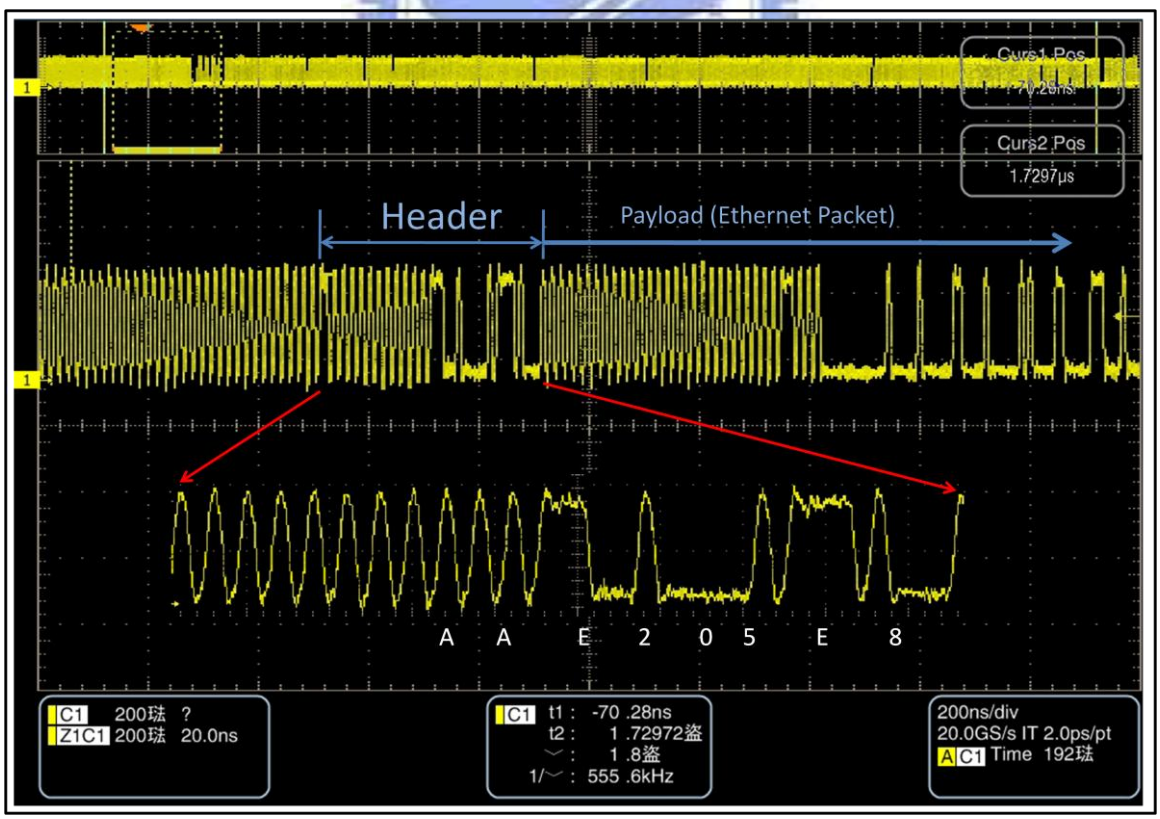

Figure 5.13 Packets of Downstream on Fiber

After ONU receives the data by the ONU transceiver, the data is sent from SerDes to FPGA.. PON MAC module on ONU will shift the data to the right place and find out Payload-Length as Fig. 5.14 shows. Then, the modules of ONU will remove Header and construct an Ethernet packet successfully, and it is shown as Fig. 5.15. The Ethernet packet will be sent to PHY on OLT from FPGA. From Fig. 5.15, we know that the data interface matches with MII. Fig. 5.16 shows the locations of gathering data (Fig. 5.11 ~ 5.15).

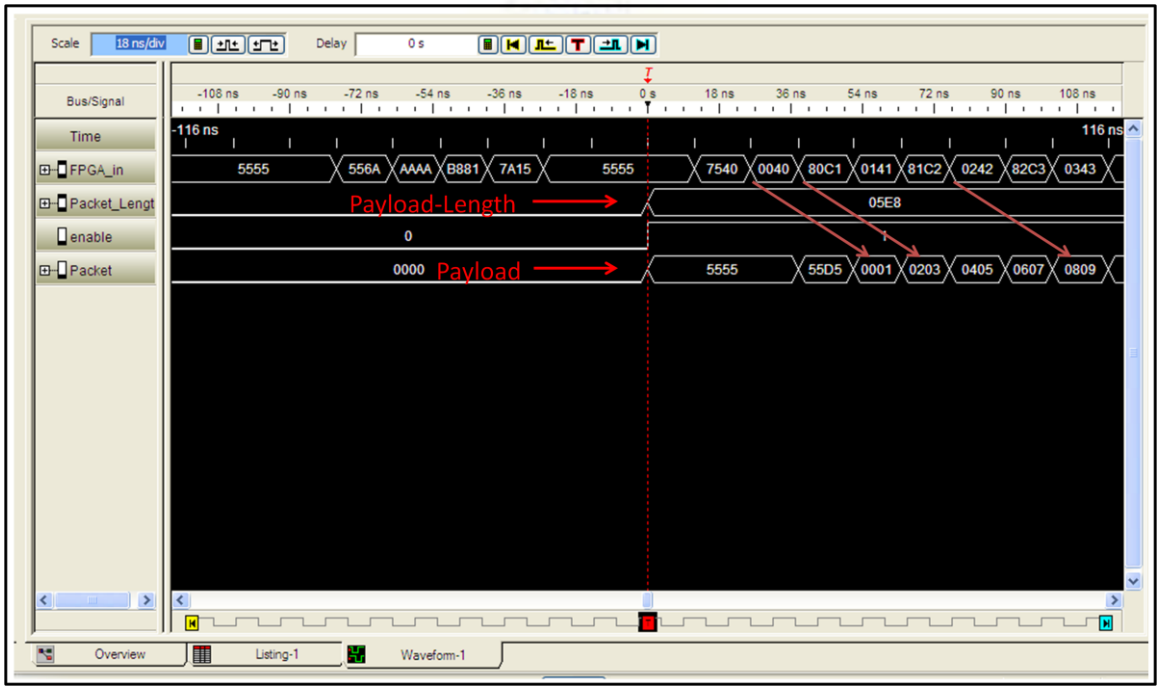

Figure 5.14 Input Data of FPGA on ONU

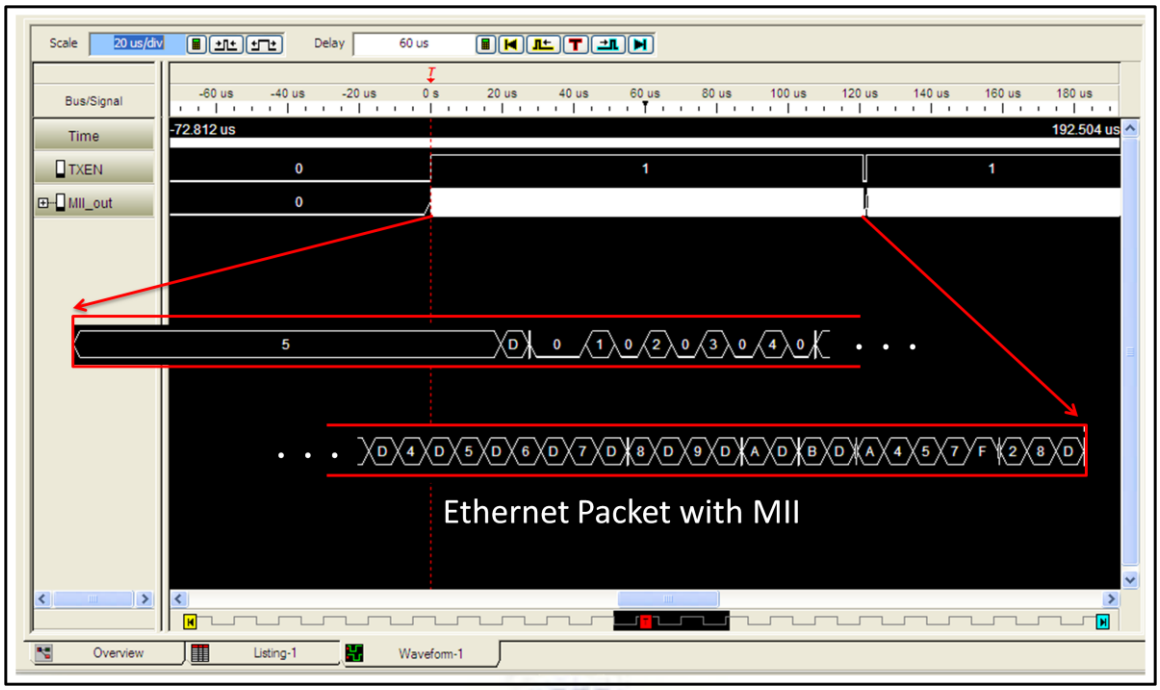

Figure 5.15 Output Packet on ONU in Downstream

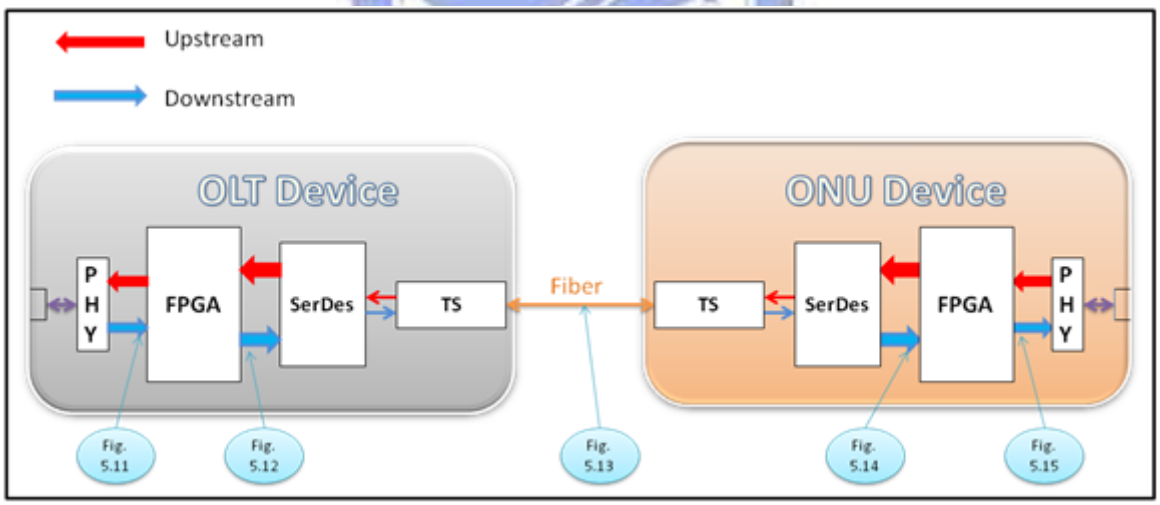

Figure 5.16 Locations of Gathering Data in Downstream

5.2 Testing Results of DHPON System

After we test Data Traffic of DHPON, we will test the performance, the efficiency and the work of our DHPON system.

5.2.1 Testing Results by SmartBits

First, we test the performance and efficiency of DHPON by SmartBits. SmartBits is a network performance testing equipment, which can generate, transmit, receive, analyze, and capture packets. The testing architecture is shown as Fig. 5.17. In downstream, we send the packets to OLT by SmartBits A, and receive the packets on ONU by SmartBits B. In upstream, we send the packets to ONU by SmartBits B, and receive the packets on OLT by SmartBits A. Then we can calculate the efficiency of DHPON in downstream and upstream.

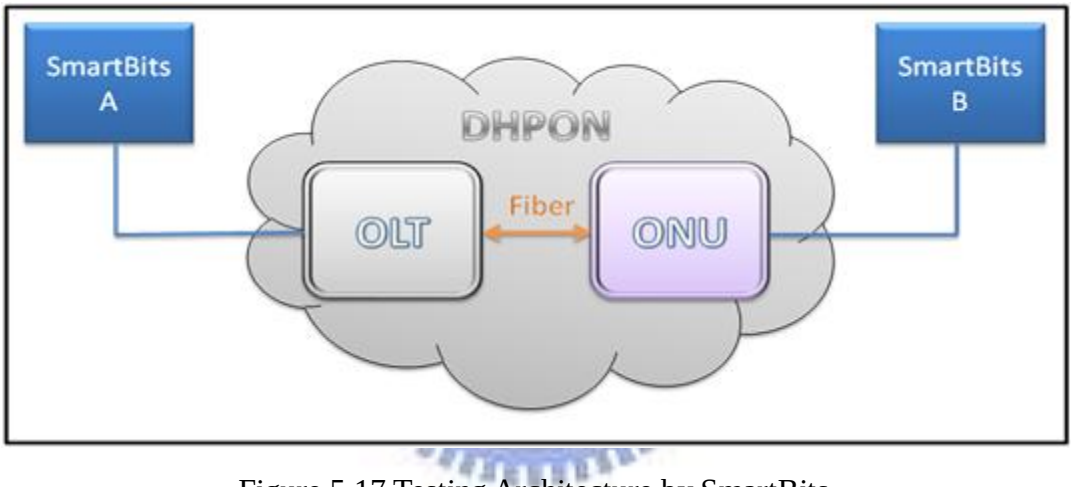

Figure 5.17 Testing Architecture by SmartBits

1. Transmitting 1,000,000 packets

We send 1,000,000 packets to OLT with 100 Mb/s speed in downstream, and receive on ONU by SmartBits B. On the other hand, we send 1,000,000 packets to ONU with 100 Mb/s speed in upstream, and receive on OLT by SmartBits A. All of packets by SmartBits sending out are random size and random background. The Result is shown as Fig. 5.18. In the Figure, we can know that SmartBits A receive 999,417 packets and SmartBits A receive 997,586 packets. So the efficiency in downstream is 99.94 %, and the efficiency in upstream is 99.76 %.

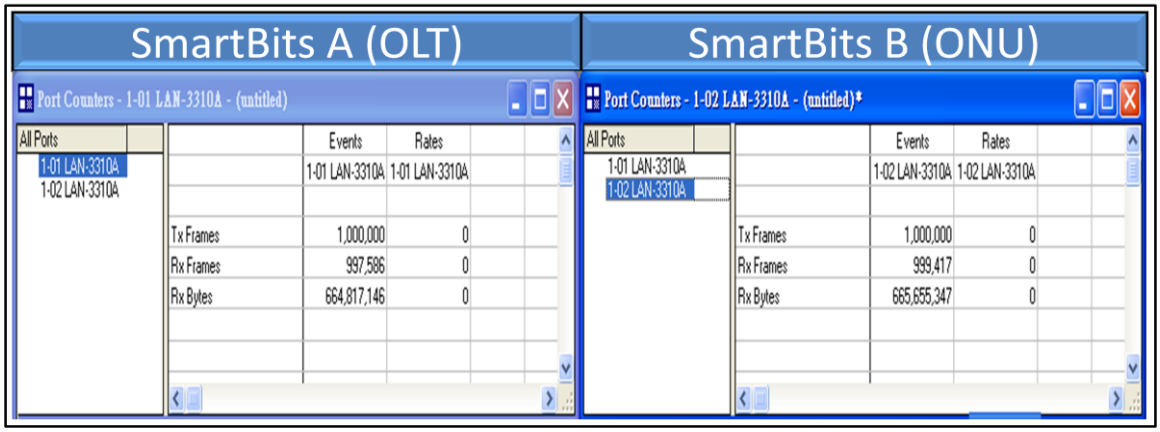

Figure 5.18 Results with Transmitting 1,000,000 packets

2. Transmitting 10,000,000 packets

We try transmitting more packets. This time, we send 10,000,000 packets to OLT and ONU with 100 Mb/s speed by SmartBits. The Result is shown as Fig. 5.19. In the Figure, we can know that SmartBits B receive 9,994,048 packets and SmartBits A receive 9.974,410 packets. So the efficiency in downstream is 99.94 %, and the efficiency in upstream is 99.7 4%.

Due to the result between two experiments is same, we can get that the DHPON is stable and the efficiency is almost perfect. Downstream efficiency DHPON is 99.95 %, and upstream efficiency DHPON is 99.75 %.

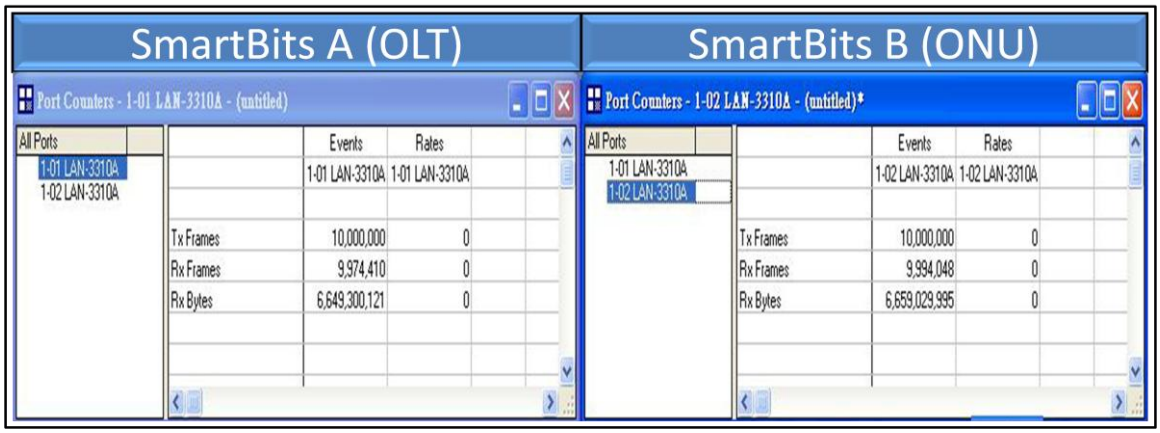

Figure 5.19 Results with Transmitting 10,000,000 packets

5.2.2 Testing Results by Video Streaming

We use VLC media player to generate a video streaming on the internet, then receive and display on a computer by our DHPON system. VLC media player is software with media player and streaming server. It can play various audio and video formats, also can be used as a server to generate video streaming stream on a high-bandwidth network.

We use VLC to generate a video streaming with Advanced Streaming Format (ASF) and 8 Mbps rate on network. As Fig. 5.20 , the two computers are connected by DHPON. The player can play the Video Streaming smoothly with few Caches. This means the DHPON can transmit real-time data, and it can work.

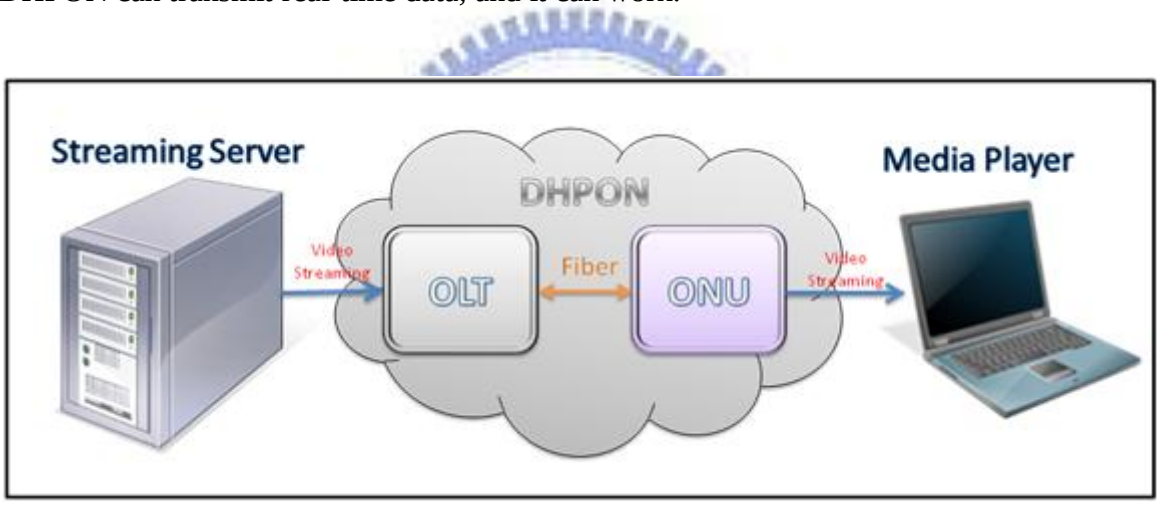

Figure 5.20 DHPON with VLC

5.2.3 Testing Results by Remote Terminal

We use VNC (Virtual Network Computing) to test DHPON system with real-time data. VNC is a remote desktop connection software, which allows you to view and fully interact with one computer desktop (the "VNC server") using a simple program (the "VNC viewer") on another computer desktop anywhere on the Internet, as Fig. 5.21 shows.

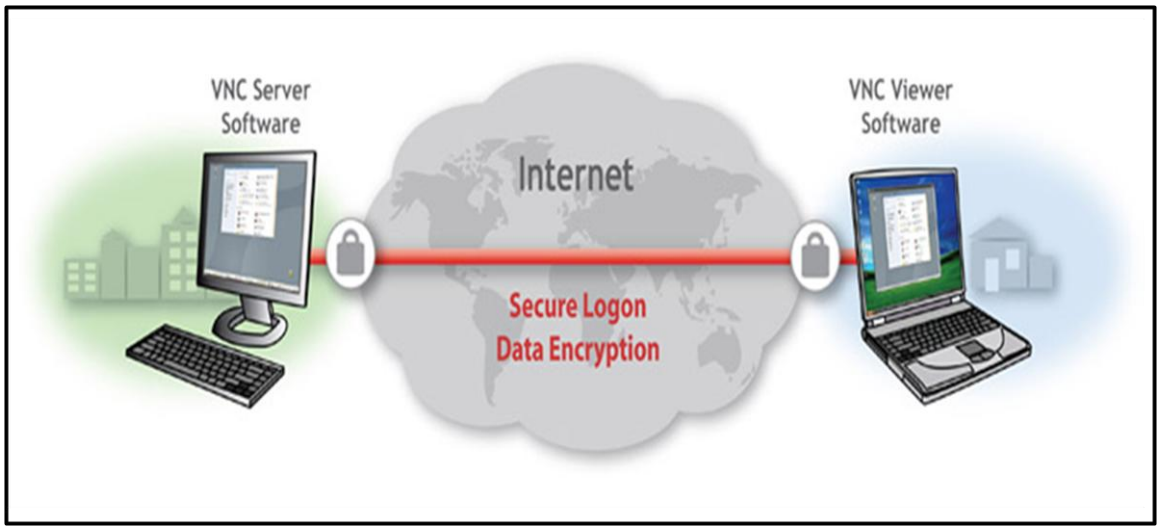

Figure 5.21 VNC System

If we replace the Internet with the DHPON system, as Fig. 5.22. VNC Server play a movie, then we watch the movie on VNC viewer which is one of the real-time data send by VNC server. As Fig. 5.23 shows, then the movie on VNC viewer will be played smoothly. It means DHPON can solve the problem that RTT is too long.

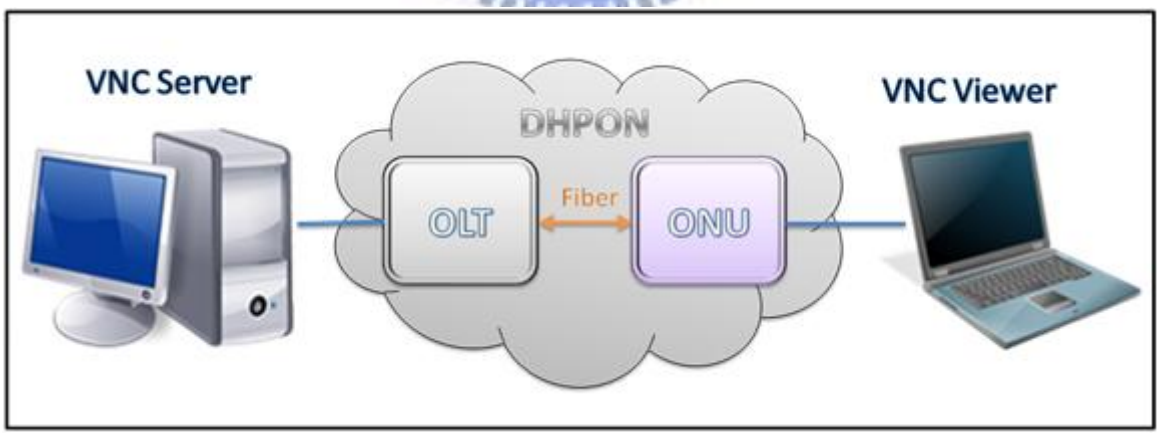

Figure 5.22 DHPON with VNC

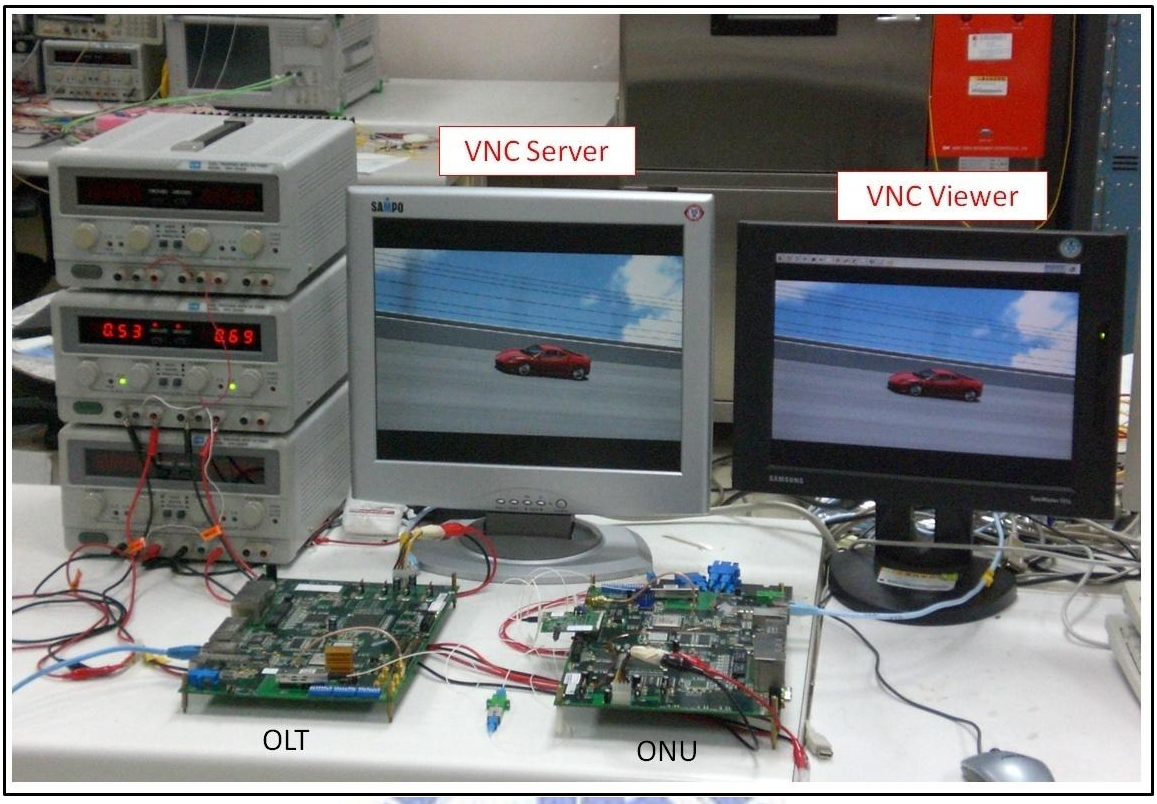

Fig. 5.23 Testing Results by VNC

CHAPTER 6

Conclusion

The experiment of my part is the data traffic of OLT and ONU. I verify that by the EthView and LA, and the final result is exact. I calculate the efficiency in downstream and upstream by the SmartBits. In downstream, the efficiency is 99.9 %. In upstream, the efficiency is 99.7 %.

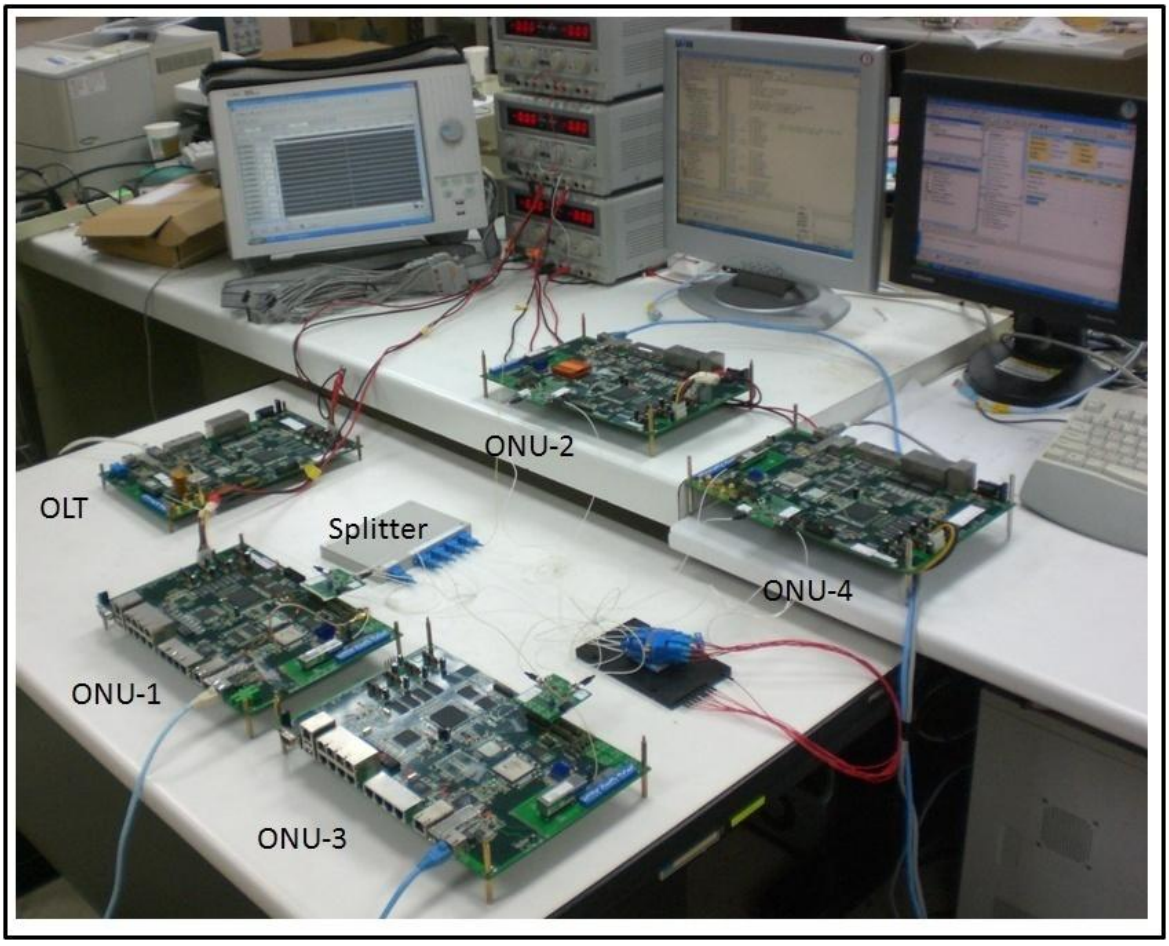

Figure 6.1 DHPON System

We have successfully set up a real DHPON system with an OLT and four ONUs, as Fig. 6.1. DHPON is based on the passive optical network and combined with TDM-PON, WDM-PON and Distributed control DBA to accomplish a passive optical network which

is high performance, shorter RTT, almost no packet delay, and simple structure. The high performance means bandwidth is not wasted and used effectively. The shorter RTT means the control message (Q-size of packet) can be updated immediately by distributed control DBA, therefore the packet delay problem is solved. In the end, we have proved that our DHPON can work exactly in the real work.

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