Available online at www.sciencedirect.com
ScienceDirect
Applied Surface Science 254 (2007) 236–241
applied surface science
www.elsevier.com/locate/apsusc

Advance in next Century nanoCMOSFET research

Huey-Liang Hwang [a,*], Yan-Kai Chiou [b], Che-Hao Chang [b], Chen-Chan Wang [b], Kun-Yu Lee [b], Tai-Bor Wu [b], Raynien Kwo [c], Minghwei Hong [b], Kuei-Shu Chang-Liao [d], Chun-Yuan Lu [d], Chun-Chang Lu [d], Fu-Chien Chiu [e], Chun-Heng Chen [a], Joseph Ya-Min Lee [a], Albert Chin [f]

[a] *Department of Electrical Engineering, National Tsing Hua University, Hsinchu, Taiwan, ROC*
[b] *Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu, Taiwan, ROC*
[c] *Department of Physics, National Tsing Hua University, Hsinchu, Taiwan, ROC*
[d] *Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan, ROC*
[e] *Department of Electronics Engineering, Ming Chuan University, Taoyuan, Taiwan, ROC*
[f] *Department of Electronics Engineering, National Chiao-Tung University, University System of Taiwan, Hsinchu, Taiwan, ROC*

Available online 21 July 2007

Abstract

It is well known that Taiwan's IC industry is in the very leading front of the world, and production of 65 nm devices was launched in 2006. Within a few years, the need of high-k dielectrics and metal gates is eminent and truly indispensable. Professor H.L. Hwang (the author) organized 12 professors and 50 graduate students of National Tsing Hua University and Chiao Tung University, and executed this particular project, which is sponsored by the Ministry of Economic Affairs of Republic of China, and is aimed at treating efficiently this problem and transferred the critical technologies to industry in a time frame of 3 years.

PACS : 73.40.Qv; 73.61.At; 73.61.Ng; 77.55.+f

Keywords: Nano; MOSFET; High-k dielectric; Metal gate

1. Introduction

Many high-k materials are currently considered as potential replacements of SiO_2 for gate dielectrics in future complementary metal-oxide-semiconductor (CMOS) technology [1–7]. Among the high-k candidates, HfO_2 has attracted much attention due to its higher dielectric constant ($k = 20$–25) and relatively large band gap ($E_g \sim 5.6$ eV) [8–10]. However, the HfO_2 suffers from poor thermal stability, low crystallization temperature and high oxygen diffusivity through the thin films. These disadvantages would limit its application in the CMOS devices. In contrast, Al_2O_3, the other candidate having a relatively lower dielectric constant, can remain amorphous up to 1000 °C and is known to have a much lower oxygen-diffusion coefficient compared to HfO_2 [11]. In addition, the Al_2O_3 has a large band gap of 8.8 eV and large band offset, which are helpful to reduce the tunneling leakage current. Many studies have been focused on the HfO_2 incorporated with aluminum in the form of $HfAlO_x$ alloy [12–14] or Al_2O_3/HfO_2 stack structure [15–17] as the gate dielectric to improve the thermal stability of HfO_2 thin films. However, the study on the effect of Al incorporation in these two different kinds of oxide structure has not been comparatively investigated in detail.

The quality and extent of charge trapping in the interfacial layer between high-k dielectric and silicon have been reported to strongly affect the electrical characteristics of high-k MOS devices [18]. Some reports have proposed an charge-pumping (CP) extraction method to evaluate the depth profile of border traps situated in the gate oxide of MOS device [19]. However, only few

* Corresponding author. Fax: +886 3 5720724.
E-mail addresses: hlhwang@ee.nthu.edu.tw (H.-L. Hwang), lkschang@ess.nthu.edu.tw (K.-S. Chang-Liao).

0169-4332/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.apsusc.2007.07.117

studies have been reported on measuring the spatial distribution of bulk traps in metal-oxide-semiconductor field-effect-transistor (MOSFET) with high-k gate dielectric by CP technique.

Therefore, in this work, the gate dielectrics of HfO_2, $HfAlO_x$ alloy and Al_2O_3/HfO_2 stack were prepared on p-type Si (1 0 0) substrate by atomic layer deposition (ALD), and the thermal stability in relation to structural and electrical properties of the respective gate dielectrics in MOS structure were simultaneously studied.

2. Experimental

The HfO_2, $HfAlO_x$ alloy and Al_2O_3/HfO_2 stack were deposited by ALD method at 200 °C on p-type (1 0 0) Si substrate. The Si wafers were cleaned by standard RCA process and dipped with dilute HF solution to remove the native oxide before the deposition of high-k dielectrics. Trimethyl aluminum [TMA, $Al(CH_3)$], tetrakis (ethylmethylamino) hafnium [TEMAH, $Hf[N((C_2H_5)CH_3)]_4$], and water (H_2O) were used as precursors, and argon was employed as carrier and purge gas. Three different kinds of samples were deposited for totally 40 cycles in sequence of 40H for HfO_2, (1A2H)*13 + 1A for $HfAlO_x$ alloy and 14A/26H for Al_2O_3/HfO_2 (Al_2O_3 followed by HfO_2) stack, where the ''H'' refers to one HfO_2 cycle and ''A'' one Al_2O_3 cycle. The cycle ratio of H/A was the same for alloy and stack structure to maintain the same Hf/Al composition ratio. After oxide deposition, all the samples were annealed by RTA (rapid thermal anneal) for 30 s in nitrogen atmosphere at different temperatures to improve the oxide quality and then changed to forming-gas atmosphere at 300 °C for 30 min to improve the interface quality.

3. Results and discussion

3.1. Formation of high-k gate dielectric in MOS devices

Fig. 1 shows the XPS spectra of Hf 4f core levels. The peak position of Hf 4f in $HfAlO_x$ sample shifts to higher binding energy as compared to that in HfO_2 and Al_2O_3/HfO_2 samples, which is because Hf is more ionic than Al in the $HfAlO_x$ matrix. It also indicates that a mixed structure with Hf–O–Al bonding is formed in the post-annealed films. In contrast, the Al_2O_3/HfO_2 stack retains a hetero-layer structure after post-anneal because the peak position of Hf core level remains the same as that of pure HfO_2 sample.

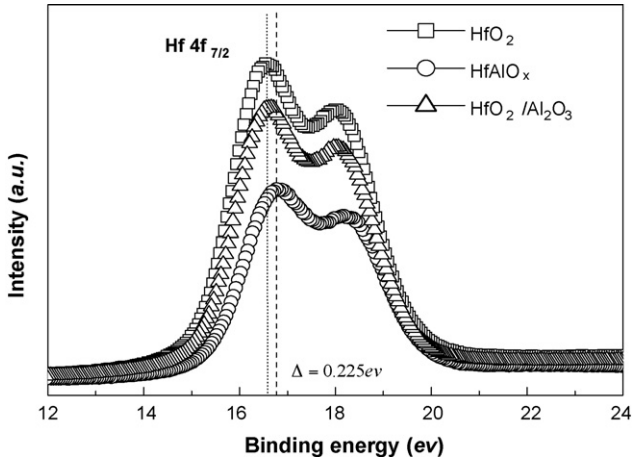

Fig. 1. The XPS Hf 4f spectra of pure HfO_2, $HfAlO_x$ alloy and Al_2O_3/HfO_2 stack, respectively, after 500 °C RTA post-deposition-annealing for 30 s in N_2 atmosphere.

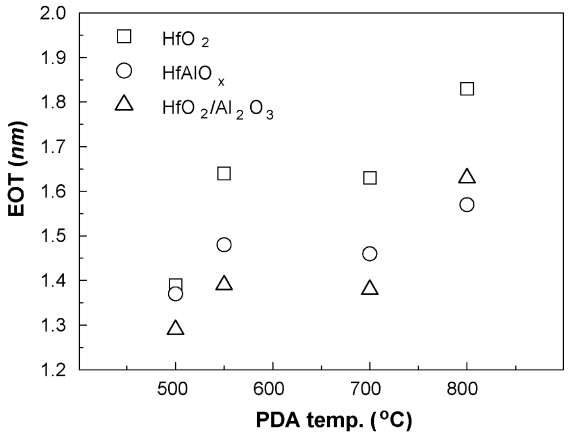

Fig. 2. The variation of EOT value of pure HfO_2, $HfAlO_x$ alloy and Al_2O_3/HfO_2 stack, respectively, as a function of post-deposition-annealing temperatures.

Fig. 2 shows the variation of equivalent oxide thickness (EOT) value as a function of post-annealing temperatures for the three samples. It increases with increasing the post-annealing temperature from 500 °C to 800 °C. However, the $HfAlO_x$ alloy and Al_2O_3/HfO_2 stack remain having lower EOT values than that of HfO_2 despite of the anneal temperatures. Moreover, the increment of EOT value against post-annealing treatment is lowest for the $HfAlO_x$ alloy, next is the Al_2O_3/HfO_2 stack, and the highest is that of HfO_2. Therefore, although the Al_2O_3/HfO_2 stack has lower EOT value at lower temperature of RTA treatment, it becomes larger than that of $HfAlO_x$ alloy after RTA treatment at 800 °C due to the larger growth of interfacial layer.

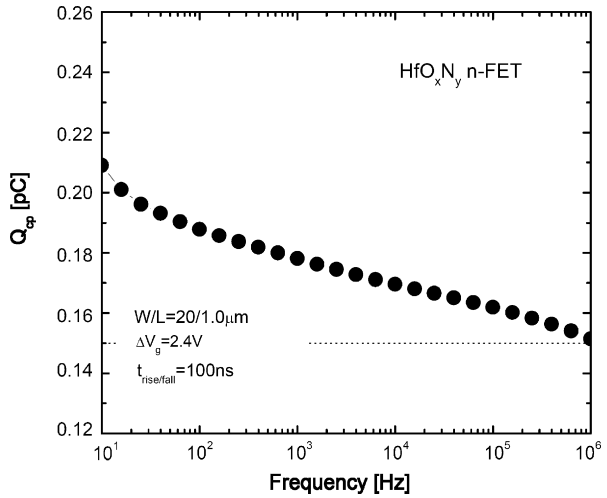

Fig. 3. The charge pumped per cycle (Q_{cp}) poltted as a function of the frequency for HfO_xN_y and SiO_2-gated nMOSFETs.

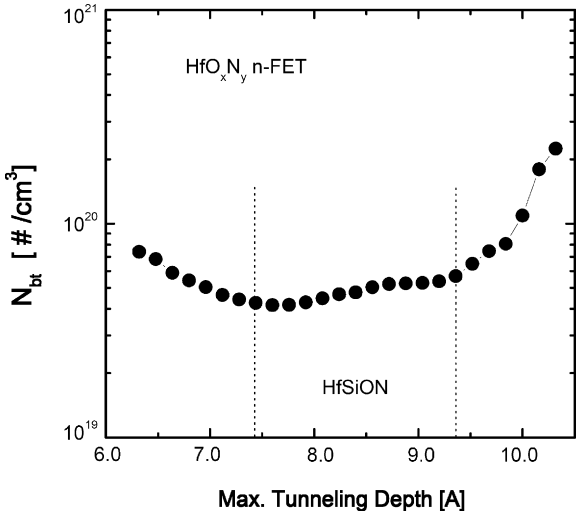

Fig. 4. Depth profiles of border traps in HfO_xN_y/SiO_2-film as extracted from the charge-pumping data shown in Fig. 3.

3.2. Profiling border traps in high-k gate dielectric

Fig. 3 shows that the charges pumped per cycle (Q_{cp}) contributed from the border-trap charges in high-k dielectric are different from those in conventional SiO_2. For high-k device, the Q_{cp} is strongly influenced by the border traps at high frequency and increases with decreasing charge-pumping (CP) frequency. Approximate depth profiles of border traps $N_{bt}(x)$ obtained by adopting the derivative $dQ_{cp}/d\log(f)$ [20] and the related physical parameters are shown in Fig. 4. The border trap density (N_{bt}) can be clearly detected by this novel CP technique.

3.3. Metal-gate/high-k devices

The Fermi-level pinning at metal-gate and high-k interface is the biggest challenge for high-k technology. As shown in Fig. 5, the pinning causes the undesired large threshold voltage (V_t) in MOSFETs. We have fabricated low-temperature fully-

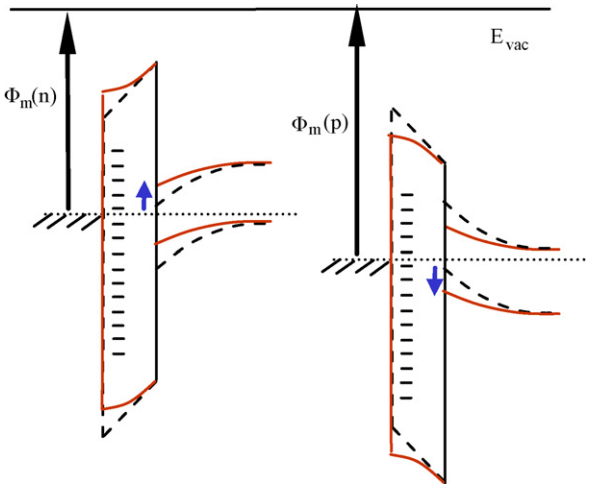

Fig. 5. Energy band diagram to show the increasing |Vt| in both n- and p-MOS, which may be due to the interface dipole and charged defects formed by MN-MO reaction or [poly-Si]-MO reaction at high temperature.

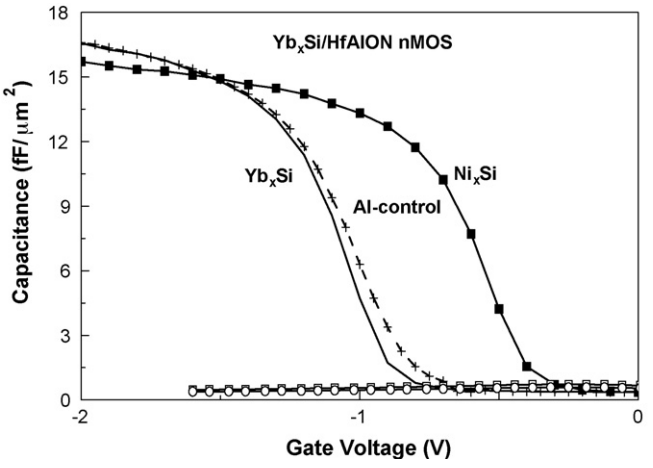

Fig. 6. C–V characteristics of FUSI Yb_xSi/HfAlON/p-Si n-MOS capacitors.

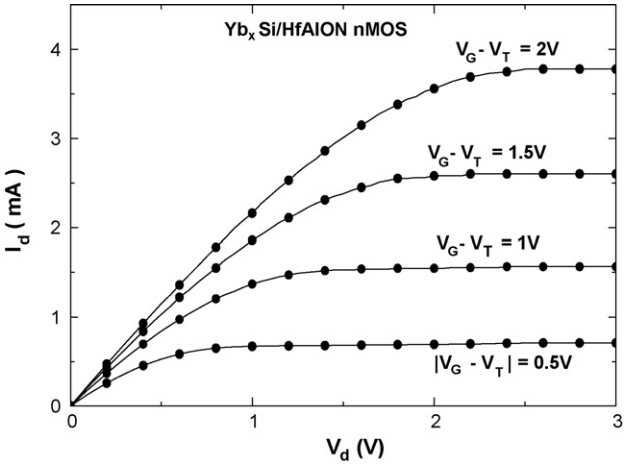

Fig. 7. $I_d - V_d$ of FUSI Yb*x*Si/HfAlON n-MOSFET.

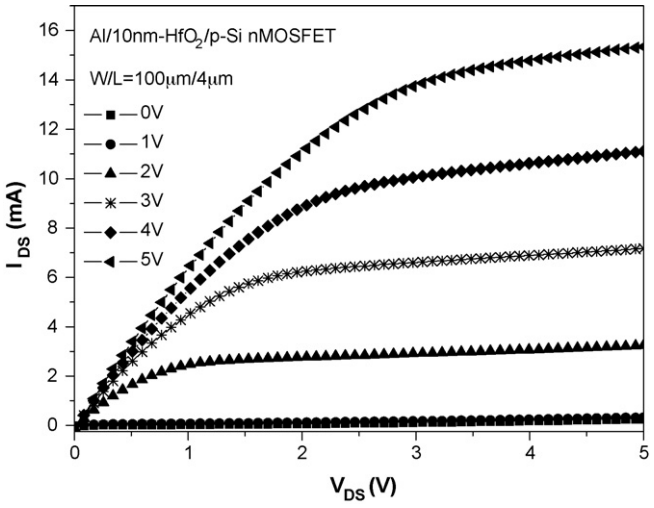

Fig. 8. The $I_{DS} - V_{DS}$ characteristics of n-channel MOSFETs fabricated with ALD HfO_2 gate dielectric.

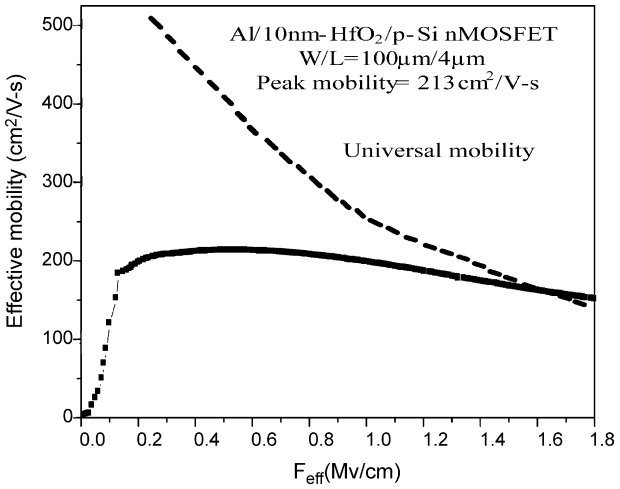

Fig. 9. The electron effective mobility of n-channel MOSFETs fabricated with ALD HfO_2 gate dielectric.

silicided $YbSi_{2-x}$-gated n-MOSFETs which used a HfAlON gate dielectric with an 1.7 nm EOT. After a 600 °C RTA, these devices displayed an effective work function of 4.1 eV (Fig. 6) that is close to conventional n^+-poly-Si gate on SiO_2. They have additional merit of well-behaved transistor $I_d - V_d$ characteristics (Fig. 7), good 180 cm^2/V s electron mobility and a process compatible with current VLSI fabrication lines.

3.4. The electron mobility of MOSFETs with HfO_2 gate dielectric using atomic layer deposition method

One of the major challenges for MOSFETs with high-k gate dielectrics is mobility degradation. In this work, n-channel MOSFETs with HfO_2 dielectric were fabricated using an ALD method. The HfO_2 films were annealed at 500 °C for 1 min. Fig. 8 shows the measured $I_{DS} - V_{DS}$ characteristics. The channel width and length are 100 μm and 4 μm, respectively. The electron mobility is extracted and compared with the universal mobility curve in Fig. 9. The maximum mobility is 213 cm^2/V s. Table 1 lists the electron mobility values of MOSFETs with HfO_2 gate dielectric reported in the literature. The mobility value measured in this work compares favorably with the literature results.

In this work, the structural and electrical characterizations were performed at the interfaces of HfO_2/Si and Al/HfO_2, respectively. The physical analyses in Fig. 10 reveal that an interfacial layer of Hf–silicate between 700 °C-annealed HfO_2 and Si was formed. The dominant conduction mechanisms of the Al/HfO_2/p-Si structure are Schottky emission at high temperatures (≥465 K) and low electric fields (≤2.2 MV/cm) as shown in Fig. 11 and Fowler-Nordheim tunneling at 77 K and high electric fields (≥2.6 MV/cm) as shown in Fig. 12, respectively. Using both the intercept of Schottky plot and the slope of Fowler-Nordheim plot, the electron effective mass in

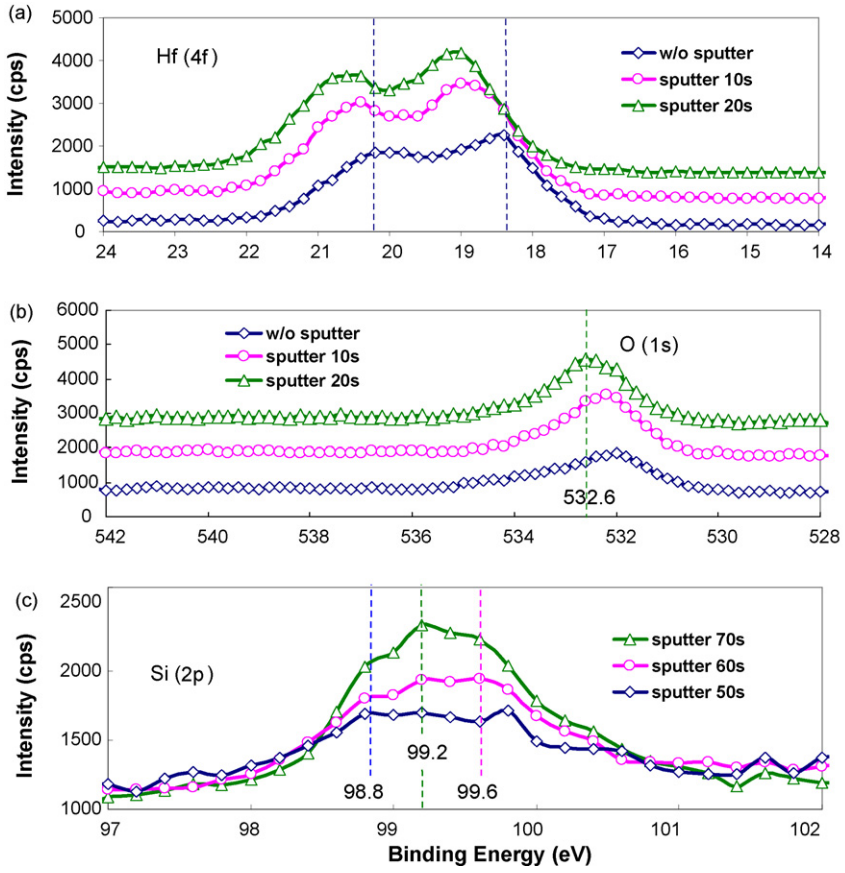

Fig. 10. XPS results of Hf 4f, O 1s and Si 2p for a 700 °C annealed HfO_2 film on Si substrate at various sputtering time.

Table 1
The electron mobility values reported in the literature and from this work

Author	nMOSFET peak mobility (cm^2/V s)	pMOSFET peak mobility (cm^2/V s)	Deposition method	Device structure	EOT (nm)	Source
Chau et al.	190	55	ALD	TiN/HfO_2/Si	1	IEEE EDL, vol. 25, no. 6, pp. 408–410, 2004
Han et al.	110	60	ALD	poly-Si/HfO_2/Si	2.4	IEEE EDL, vol. 25, no. 3, pp. 126–128, 2004
Tsai et al.	110	70	ALD	TiN/HfO_2/Si	0.8	IEEE IEDM, pp.311–314, 2003
Gusev et al.	190	NA	ALD	poly-Si/HfO_2/Si	1	IEDM, pp. 451–454, 2001
Singh et al.	80	NA	ALD	poly-Si/HfO_2/Si	1.3	IEDM, pp. 863–866, 2004
This work	213	NA	ALD	Al/HfO_2/Si	2.6	

HfO_2 and the barrier height at the Al/HfO_2 interface are determined to be 0.4 m_0 and 0.94 eV, respectively.

4. Summary and other related work of this project

This project treated particularly the interface problems, which employed Molecular Beam Epitaxy (MBE)-grown high-k dielectric nano-thick films Al_2O_3 and HfO_2 on Si (1 0 0) as templates to successfully suppress the oxide/Si interfacial layer formation during the subsequent home made ALD growth. The absence of the interfacial layer was confirmed using X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy [21]. A bi-layer composite of Al_2O_3 1.9 nm (ALD)/Al_2O_3 1.4 nm(MBE) shows a dielectric constant of 9.1 with an equivalent oxide thickness (EOT) of 1.41 nm. The interface trap density (D_{it}) was 2.2×10^{11} cm^{-2} eV^{-1} as deduced from the conductance method, with the leakage current density being 2.4×10^{-2} A/cm^2 at $V_{fb} - 1$ V. The second bi-layer of Al_2O_3 3.0 nm (ALD)/HfO_2 2.0 nm (MBE) shows a dielectric constant of 11.5 and an EOT of 1.7 nm. A D_{it} was estimated to be 2×10^{11} cm^{-2} eV^{-1} with the leakage at $V_{fb} + 1$ V being 1.1×10^{-4} A/cm^2. On the other end, the MOSFET device using the novel MBE template (ALD (4 nm)/MBE (2 nm) HfO_2) also shows excellent properties of Id of 155 mA/mm at Vg of 2.5 V and a Gm of 100 mS/mm. Further work on HfO_2/Hf_3N_4 nano composite stack layers and La_2O_3 by ALD was also underway. The etching properties of HfO_2 and related dielectrics and Si wafer with pattern were also investigated using inductively coupled high density plasma etcher, and the intensity of plasma species was also determined. Also, a Medium energy ion scattering (MEIS) facility was home constructed and tested for the composition analysis of the film structures. The unique strength of MEIS is its applicability to nano-scale material analysis that links surface science and thin-film studies. Furthermore, the high-k material was successfully integrated with fully silicide pMOSFET device. The extracted hole mobility was greater than 70% SiO_2 pMOSFET hole universal mobility of the first year target, also the proposal of Dual-Vt metal gate (NiSi and NiGe) on

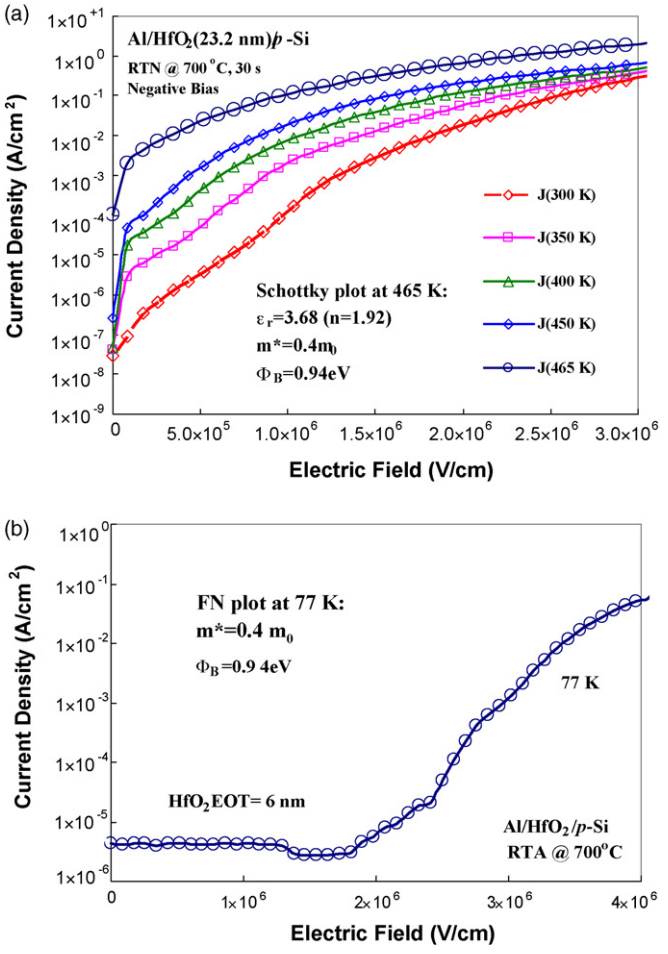

Fig. 11. (a) Characteristics of J–E plots for HfO2 MOS capacitor at various temperatures. (b) Characteristics of J–E plots for HfO2 MOS capacitor at 77 K.

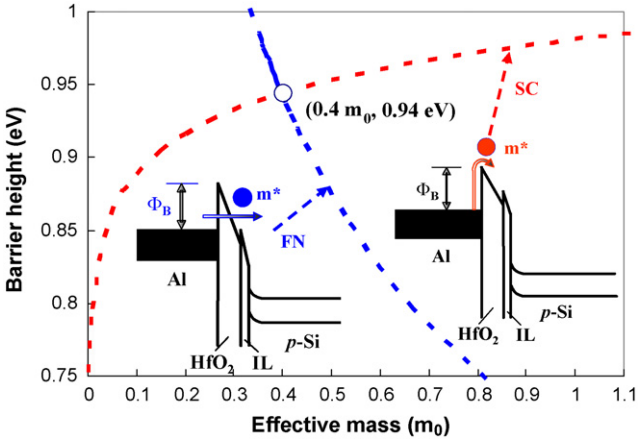

Fig. 12. The extracted relationships between electron effective mass and Al/HfO_2 barrier height from the intercept of Schottky plot at a high temperature (465 K) and the slope of F–N plot at a low temperature (77 K), respectively. The band diagrams for Schottky emission and F–N tunneling are also shown.

SiO_2(<2 nm) MOSFET was met for the requirement of integration and reliability studies of high-k gated MOSFETs.

Acknowledgements

The authors gratefully acknowledge the support from the Technology Development Program for Academia, Department of Industrial Technology, Ministry of Economic Affairs, Taiwan, Republic of China.

References

[1] C. Chaneliere, J.L. Autran, R.A.B. Devine, B. Balland, Mater. Sci. Eng., R. 22 (1998) 269.
[2] R.A. McKee, F.J. Walker, M.F. Chisholm, Phys. Rev. Lett. 81 (1998) 3014.
[3] E.P. Gusev, M. Copel, E. Cartier, I.J.R. Baumvol, C. Krug, M.A. Gribelyuk, Appl. Phys. Lett. 76 (2000) 176.
[4] M. Balog, M. Schieber, S. Patai, M. Michman, J. Cryst. Growth 17 (1972) 298.
[5] L. Kang, B.H. Lee, W.J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, J.C. Lee, IEEE Electron Device Lett. 21 (2000) 181.
[6] Y. Ma, Y. Ono, L. Stecker, D.R. Evans, S.T. Hsu, Tech. Dig. Int. Electron Devices Meet. (1999) 149.
[7] L. Manchanda, M.L. Green, R.B. van Dover, M.D. Morris, A. Kerber, Y. Hu, J.P. Han, P.J. Silverman, T.W. Sorsch, G. Weber, et al. Tech. Dig. Int. Electron Devices Meet. (2000) 23.
[8] G.D. Wilk, R.M. Wallace, J.M. Anthony, J. Appl. Phys. 89 (2001) 5243.
[9] M. Houssa (Ed.), High-k Dielectrics, Institute of Physics, London, 2004.
[10] International Technology Roadmap for Semiconductors, Semiconductor Industry Association, San Jose, CA, (2002), http://public.itrs.net.
[11] M.L. Green, E.P. Gusev, R. Degraeve, E.L. Garfunkel, J. Appl. Phys. 90 (2001) 2057.
[12] V. Mikhelashvili, R. Brener, O. Kreinin, B. Meyler, J. Shneider, G. Eisenstein, Appl. Phys. Lett. 85 (24) (2004) 5950–5952.
[13] M.-K. Song, S.-W. Kang, S.-W. Rhee, J. Electrochem. Soc. 152 (2) (2005) C108–C112.
[14] Q. Li, S.J. Wang, T.H. Ng, W.K. Chim, A.C.H. Huan, C.K. Ong, Thin Solid Films 504 (2006) 45–49.
[15] M.-H. Cho, K.B. Chung, H.S. Chang, D.W. Moon, Appl. Phys. Lett. 85 (18) (2004) 4115–4117.
[16] T. Nishimura, T. Okazawa, Y. Hoshino, Y. Kido, J. Appl. Phys. 96 (11) (2004) 6113–6119.
[17] T. Okada, M. Shahjahan, K. Sawada, M. Ishida, J. Appl. Phys. 44 (4B) (2005) 2320–2322.
[18] A. Kerber, et al. IEEE EDL (2003) 87–89.
[19] Bauza, Y. Maneglia, IEEE Trans. Electron Devices vol.44 (1997) 2262–2266.
[20] Y. Maneglia, et al. J. Appl. Phys. (1996) 4187–4192.
[21] K.Y. Lee, et al. in: Proceedings of the 14th International Conference on Molecular Beam Epitaxy (MBE2006), September 3–8, 2006.